




DG3000 SERIES/ DG4000 / TD3000 series Digital Pattern Generator user manual



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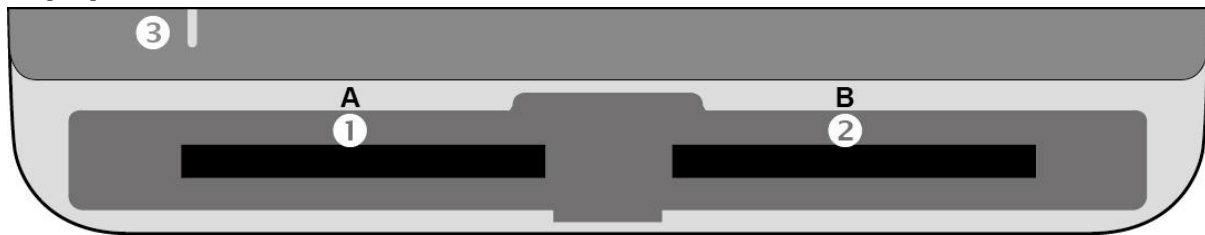
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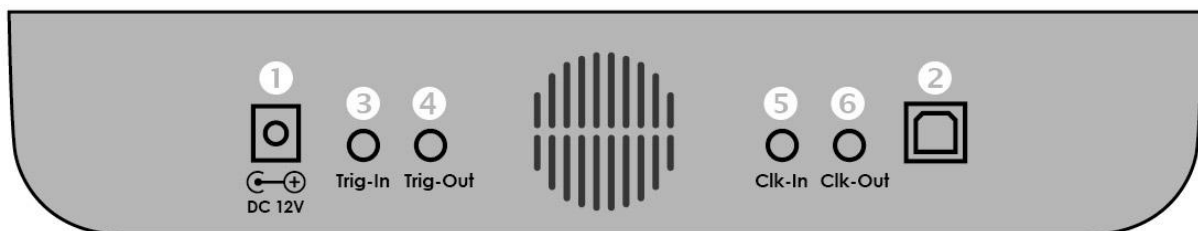
Chapter 1 Installation

Hardware Setup

Equipment



- ❶ Socket A
- ❷ Socket B
- ❸ Indicator LED
 - a. Green light : Show green light when powered and USB connected.
 - b. Red light : Show red light when the equipment is busy at transmission.



- ❶ DC 12V
- ❷ USB 3.0 Type B for computer
- ❸ Trigger In
- ❹ Trigger Out
- ❺ Reference Clock In
- ❻ Reference Clock Out

Flat Cable Installations

Push in: Hold the pod to face the slot of the master unit. Push the pod evenly into the slot until you hear the sound of click. Then, installation is completed.

Pull out: Use two fingers to simultaneously press the two connecting rods inside the slot, respectively, and the pod will pop out.

NOTE: For the convenience of describing the usage of DG flat cables, we need to define the meanings of some words, which is only used in this manual.

Considering the most of DG flat cables has two pairs of flat cable tip, each tip has 8 channels. Thus, we use these words to mention which pairs of flat cables we are talking with.

1. Tip Group 1: Ch.0 to Ch.15.
2. Tip Group 2: Ch.16 to Ch.31.

DG4000 series

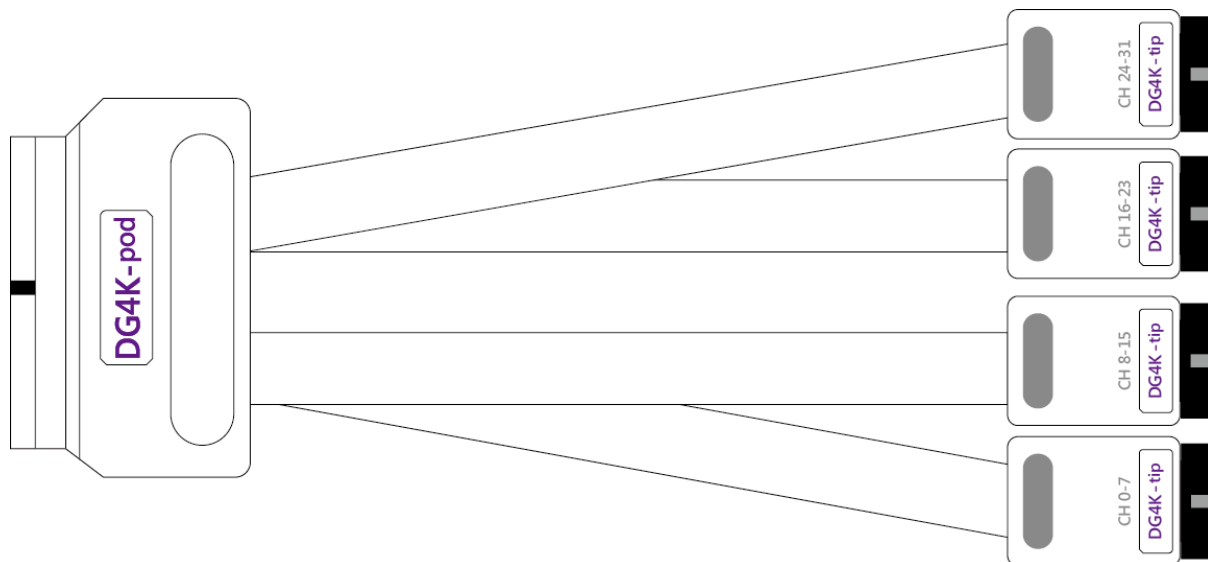
DG4K-pod Flat Cable

Supported Model:

DG3000 Series	DG4000 Series
•	•

The DG4K-pod flat cable can be used in any slot. It has 4 DG4K-pod flat cable tips, each of which has 8 signal output channels.

Usage: The DG4K-pod flat cable is able to output the square waveform, which can be used to simulate the digital signal.



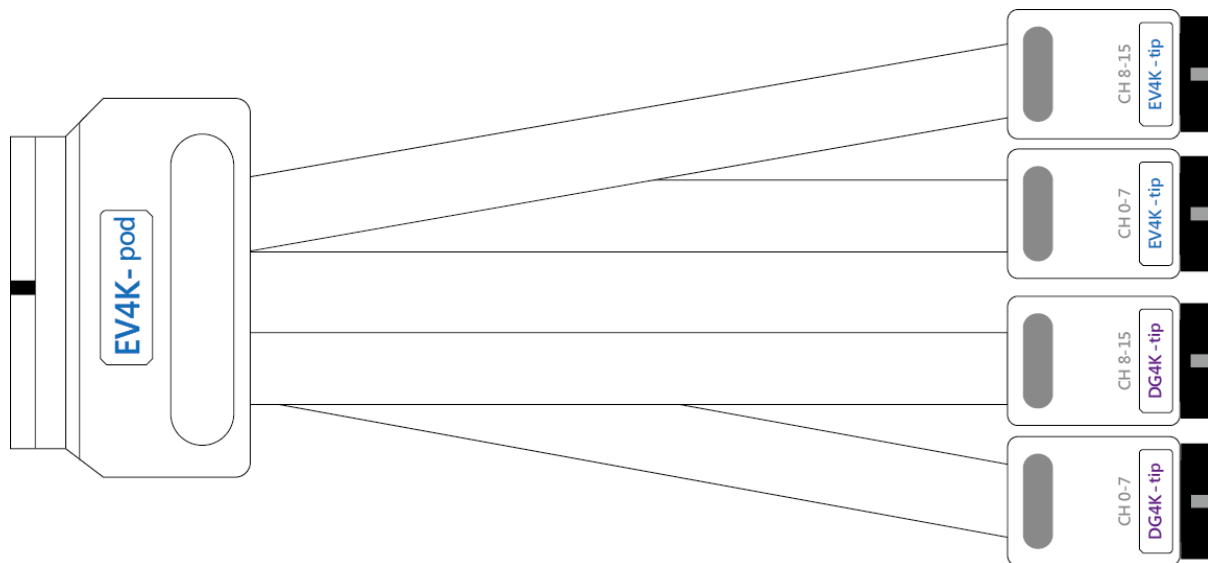
EV4K-pod Flat Cable

Supported Model:

DG3000 Series	DG4000 Series
•	•

The EV4K-pod flat cable can be used in any slot. It has 4 tips, 2 tips are DG4K-pod flat cable tip; 2 tips are EV4K-pod flat cable tip.

Usage: The usage of DG4K-pod flat cable is described above. The EV4K-pod flat cable tip can take the signal from outside to trig the DG to send out the square waveform. To our design, DG will be triggered if the input signal is 'high'.



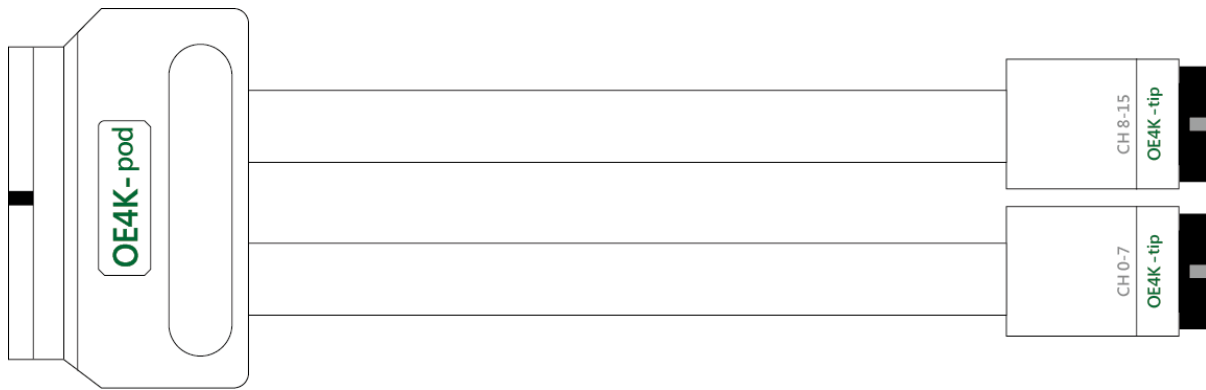
OE4K-pod Flat Cable

Supported Model:

DG3000 Series	DG4000 Series
•	•

The OE4K-pod flat cable can be used in any slot. It has 2 OE4K-pod flat cable tips, each tip has 8 channels for Hi-Z output.

Usage: In standard DG4K-pod flat cable, user can only set all the channels in tip group 1 or tip group 2 to Hi-Z. Instead, while using OE4K-pod flat cable, user can set the channels to Hi-Z respectively in both tips.



LVDS-pod Flat Cable (Option)

Supported Model:

DG3000 Series	DG4000 Series
	•

The LVDS-pod flat cable can be used in any slot. It has 2 LVDS-pod flat cable tips, each of which has 8 signal output channels.

Usage: The LVDS-pod flat cable is similar to the DG/DG4K-pod flat cable, both can output the square waveform. But LVDS-pod flat cable will output differential signal for the need of LVDS.



DG3000 SERIES series

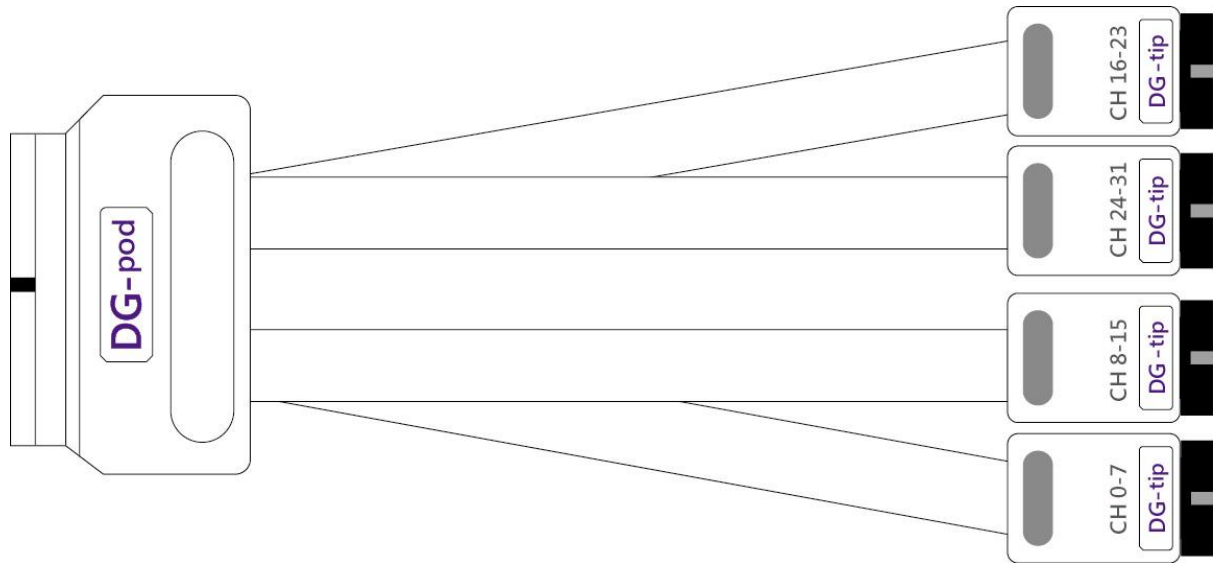
DG-pod Flat Cable

Supported Model:

DG3000 Series	DG4000 Series
•	•

The DG-pod flat cable can be used in any slot. It has 4 DG-pod flat cable tips, each of which has 8 signal output channels.

Usage: The DG-pod flat cable is able to output the square waveform, which can be used to simulate the digital signal.



Event-pod Flat Cable

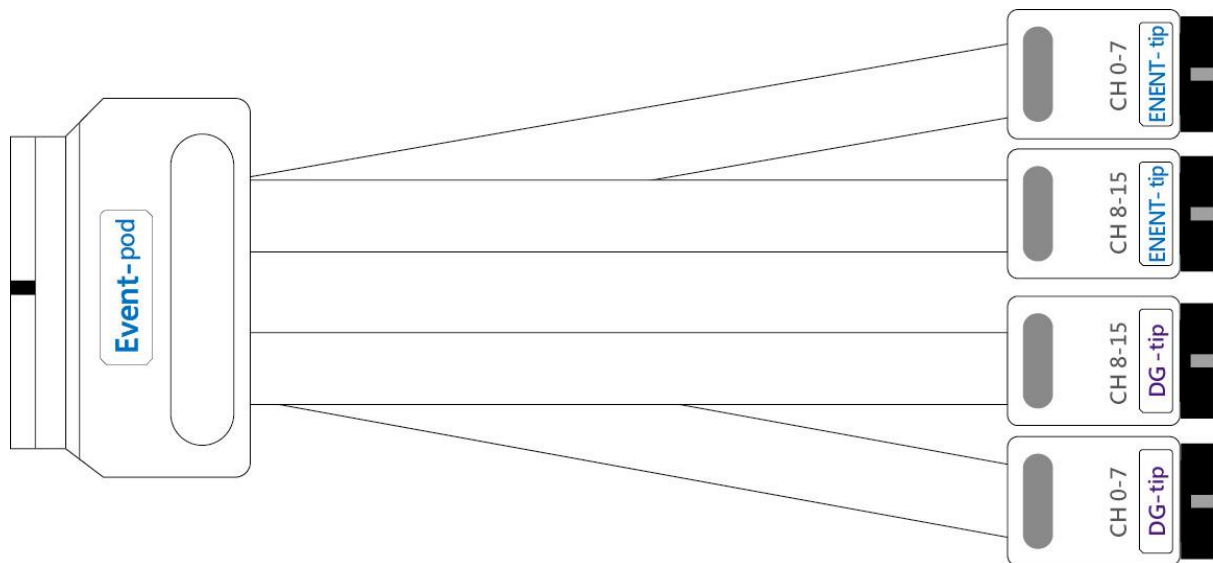
Supported Model:

DG3000 Series	DG4000 Series
•	•

The Event-pod flat cable can be used in any slot. It has 4 tips, 2 tips are DG-pod flat cable tip; 2 tips are Event-pod flat cable tip.

Usage: The usage of DG-pod flat cable is mentioned above. The Event-pod flat cable tip can take the signal from outside to trig the DG to send out the square waveform.

To our design, DG will be triggered if the input signal is 'high'.



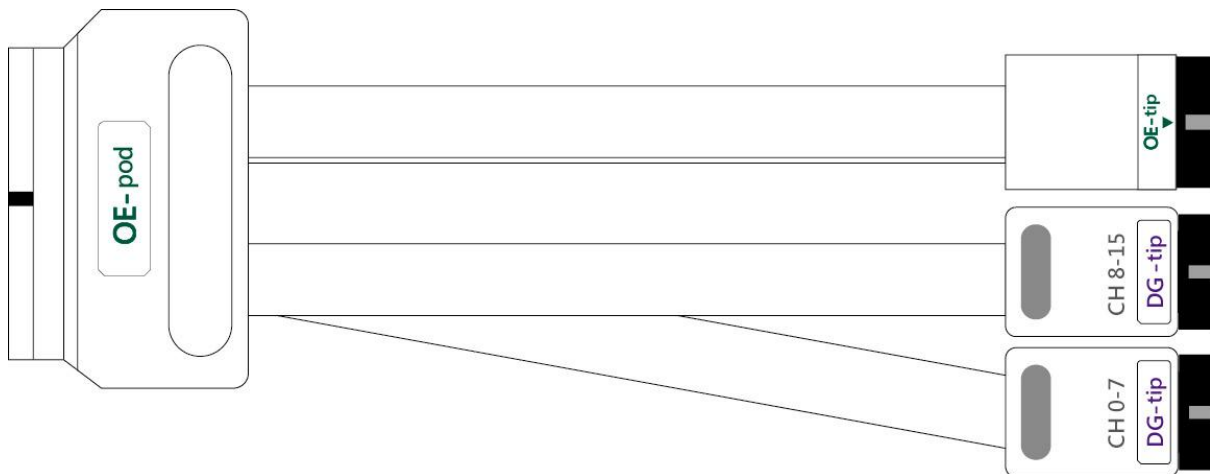
OE-pod Flat Cable

Supported Model:

DG3000 Series	DG4000 Series
•	•

The OE-pod flat cable can be used in any slot. It has 3 tips, 2 tips are DG-pod flat cable tip; 1 tip is OE-pod flat cable tip, which has 8 channels for Hi-Z output.

Usage: In standard DG-pod flat cable, user can only set all the channels in tip group 1 or tip group 2 to Hi-Z. Instead, while using OE-pod flat cable, user can set the channels in the OE-tip to Hi-Z respectively.

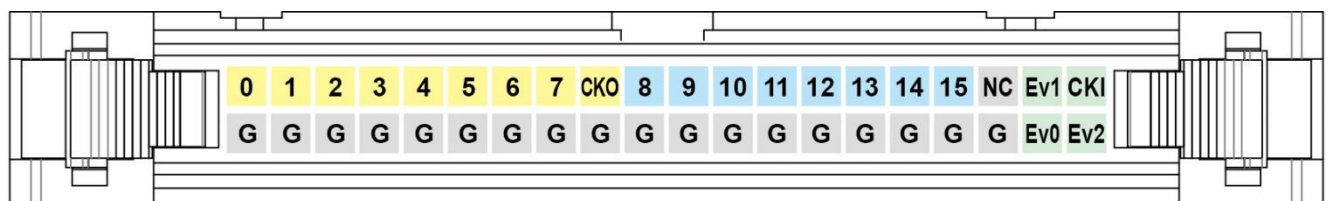


TD3000 series

18.5cm lead cable


※ Only provide by TD3000 series

TD3000 has 16 channels for data output; 1 channel for clock out (CKO); 1 channel for clock in (CKI) and 3 channels for event input (Ev0~2).



Software installation

NOTE: Since 2024, we will not provide x86(32 bit) software, only x64(64 bit) software. Whoever needs x86 software, please contact us.

Please visit the official website of Acute Technology Inc., go to the Download page->Software, and then select **[Digital Pattern Generator] Data Generator / TravelData** to download the Data Generator. After completion of installation, the “start icon” of Data Generator will appear on the desktop and the program set. You can select either one to start TD3000 Series /DG3000 Series /DG4000 Series ()

SDK

We provide SDK for user to control DG software. Please check the sample codes in the DG_installPack/DG/SDK or DG_installPack/DG/Protocol SDK; Or contact us with e-mail.

Specifications

DG4000 series

Model		DG4064B	DG4096B	DG4128B
Power	Power Source	12V Power Adapter		
	Static Power Consumption	9W	12W	18W
	Max Power Consumption	24W	30W	36W
Hardware Interface		USB 3.0		
Slot/Pod(1 Slot for 1 Pod)	Availabel Slots	2	3	4
	Availiable Data Output Channels (DG4K pods)	48	80	112*2
	Standard pod(s):	1/1/1/0	2/1/1/0	3/1/1/0

	DG4K/OE4K/EV4K/LVDS*1				
	Available Channels @ Max.	DG4K pod	32ch@300Mbps, 16ch@600Mbps, 8ch@1.2Gbps, 4ch@2.4Gbps		
		LVDS pod	16ch@300Mbps, 16ch@600Mbps, 8ch@1.2Gbps, 4ch@2.4Gbps		
	Internal Clock	OE4K/EV4K pod	16ch@300Mbps, 8ch@600Mbps, 4ch@1.2Gbps, 2ch@2.4Gbps		
DG4K-tip (Output ch, for DG4K/EV4K-pod)	Max. Output Data Rate		700Mbps (350MHz)		
	Min. Output Voltage at different data rates		0.9Vpp @ <= 40Mbps, 1.2Vpp @ <= 400Mbps, 1.5Vpp @ <= 500Mbps, 3.3Vpp @ <= 700Mbps		
	Output Voltage Range		0.9Vpp ~ 5.0Vpp		
	Rising Time		300ps @ 3.3V		
	Impedance		CMOS with 20Ω		
	Fan out		20mA/ch		
OE4K-tip (Output ch, for OE4K-pod)	Max. Output Data Rate		700Mbps (350MHz)		
	Min. Output Voltage at different data rates		0.9Vpp @ <= 40Mbps, 1.2Vpp @ <= 400Mbps, 1.5Vpp @ <= 500Mbps, 3.3Vpp @ <= 700Mbps		
	Output Voltage Range		0.9Vpp ~ 5.0Vpp		
	Rising Time		300ps @ 3.3V		
	Impedance		CMOS with 20Ω		
	Fan out		20mA/ch		
LVDS-tip (Output ch, for LVDS-pod)	Max. Output Data Rate		1.2Gbps (600MHz)		
	Output Voltage		±350mV*5		
EV4K-tip (Input ch, for EV4K-pod)*3	Channel (LA/Clk In)		16 / 1		
	Max. Frequency		200MHz		
	Threshold		-0.5V ~ 4.5V @ 0.1V Resolution		

	Input Voltage (Non-destructive)	±15V DC + AC peak(Max.)		
	Impedance	1MΩ 5pF		
	Sensitivity	~300mV		
Internal Clock Generation	Range	1Hz ~ 2.4GHz*4 (Periodd: 1s ~ 416ps)		
	Resolution	6 digits, Min. 1Hz		
External Clock Generation	Range	<= 200MHz		
Memory per Channel		256Mb		
Phase Tuning Delayed		Depend on Internal Clock, Min. 416ps		
Temperature Operating / Storage		5°C~45°C (41°F~113°F) / -10°C ~65°C (14°F~149°F)		
Event	Internal	Hot Key		
	External (Channel / Mode / Threshold)	16 / Logic AND OR / -0.5V ~ 4.5V		
Software Feature	Language	English / Tranditional Chinese / Simplified Chinese		
	Data Pattern File Format	DGW / DGV / VCD / CSV		
	Regular Waveform Generator	Sync. Counter, Async. Counter, I2C, MIPI I3C, REFE, PMBus, PWM, SPI		
	Flow Control	Loop / Jump / Hold / Wait For Event		
Accessories (Gripper / Flying Lead Cable)		80 / 10	120 / 14	160 / 18
Device Dimension		(L)270mm x (W)175mm x (H)55mm		
Weight Device / Accessories		800g / 1850g		

¹ DG: Single Ended; OE: Output Enable; EV: Event; LVDS: Low Voltage Differential Signal

² Only a half channels are available for the D slot

³ A half EV pod's channels (EV4K-tip) are inputs, the other half channels (DG-4K tip) are DG outputs

⁴ Max. 6 digits value adjustment

⁵ The DUT (Device Under Test) inputs must be terminated by the 100Ω termination resistor.

DG3000 series

Model		DG3064B	DG3096B	DG3128B
Power	Power Source	12V Power adapter		
	Static Power Dissipation	9W	12W	18W
	Max. Power Dissipation	24W	30W	36W
Hardware Interface		USB 3.0		
Number of Output Channels		48	80	112
Memory	Total Memory Size	32Gb		
	Pattern Depth	256Mb/ch		
Data Rate		400Mbps (Max.)		
Operation Clock System	Internal	Range	1Hz ~ 400MHz	
		Resolution	6 digits	
	External	Clock Range	<200MHz	
		Input Channels	1 Channel (TTL3.3V)	
Data Flow Control		Loop, Jump, Hold, Wait for Event		
Period Jitter	Clock Channel	< 200ps		
	Data Channel	< 200ps		
Event	Internal		Hot Key	
	External	Channels	16	
		Mode	Logic AND / Logic OR	
		Threshold	-0.5V ~ 4.5V	
Phase Tuning Delayed	Channels	All		
	Time	> 300Mbps : No, < 300Mbps : 8 Phases from 0 to 1UI		
Temperature	Operating/Storage	5°C~45°C (41°F~113°F) / -10°C~65°C (14°F~149°F)		
Software Features	Languages	English / Traditional Chinese / Simplified Chinese		
	Save & Load Waveform	Yes		
	Regular Waveform	Synchronous / Asynchronous Counter, I2C, MIPI		

	Generator	I3C, MIPI RFFE, PMBus, SPI/SIPI, ...		
	Waveform Editing Interface	Waveform Drawing/Script File		
Device Dimension	L x W x H (mm ³)	270 x 175 x 55		
Weight	Device / Accessories	800g / 1850g		
Flat Cable	DG-pod / Event-pod / OE-pod	1 / 1 / 1	2 / 1 / 1	3 / 1 / 1
	Flying lead cable: DG (DG) /Event (DG, Event) /OE (DG, OE)	4 / 2, 2 / 2, 1	8 / 2, 2 / 2, 1	12 / 2, 2 / 2, 1
	Grippers	80	120	160
DG-pod Flat Cable/ OE-pod Flat Cable	Channels	32 for DG / 24 for OE		
	Data Rate	400Mbps (Max.)		
	VoL	0V		
	VoH min. for DG-pod Flat Cable	0.8Vpp @ <= 50Mbps, 1.2Vpp @ <= 300Mbps, 1.5Vpp @ <= 400Mbps		
	VoH min. for OE-pod Flat Cable	1.1Vpp @ <= 50Mbps, 1.3Vpp @ <= 300Mbps, 1.5Vpp @ <= 400Mbps		
	VoH max.	5.0V		
	Min. Pulse Width	2.5 ns		
	Impedance	CMOS with 20 Ohms		
	Fan Out	20mA/ch		
	Output Enable	DG-pod Flat Cable	2 Group O.E. (16ch/O.E. * 2 = 32ch) ^{*1}	
OE-pod Flat Cable		1 Group O.E. + 8ch Independent O.E. (16ch+8ch=24ch) ^{*2}		
Event-pod Flat Cable	Channels	16 (DG) + 16 (Event)		
	Frequency	200MHz (Max.)		
	Operation	-1V~8V @ 0.1V Resolution		
	Input Voltage (Non-destructive)	±15V DC+AC peak (Max.)		
	Minimum Pulse Width	2.5 ns		
	Sensitivity	~300mV		
	Impedance	1M 5p		

¹OE Bus: Controls the output of a group of buses with a width of 16 channels each.

²OE Channel: Controls a single channel

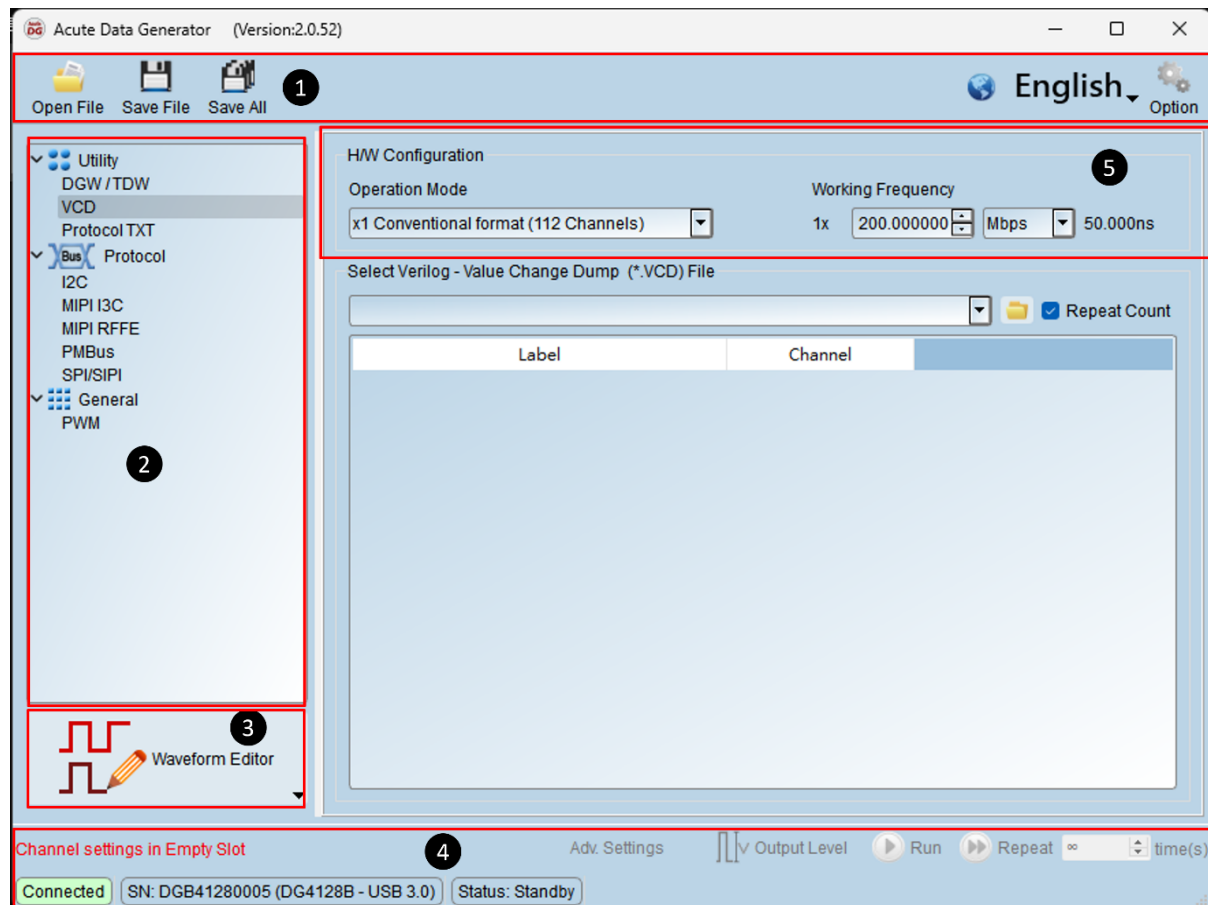
TD3000 series

Model		TD3008E	TD3116B	TD3216B	
Power	Power Source	USB 3.0			
	Static Power Dissipation	2.5W			
	Max. Power Dissipation	4.5W			
Hardware Interface		USB 3.0			
Number of Output Channels		8	16		
Memory	Total Memory Size	4Mb	16Mb	4Gb	
	Pattern Depth	512Kb/ch	1Mb/ch	256Mb/ch	
Data Rate		100Mbps (Max.)	200Mbps (Max.)		
Operation Clock System	Internal	Range	1Hz ~ 100MHz	1Hz ~ 200MHz	
		Resolution	6 digits		
	External	Clock Range	<100MHz	<200MHz	
		Input Channels	1 Channel (TTL3.3V)		
Data Flow Control		Loop, Jump, Hold, Wait for Event			
Period Jitter	Clock Channel	< 200ps			
	Data Channel	< 200ps			
Temperature	Operating/Storage	5°C~45°C (41°F~113°F) / -10°C~65°C (14°F~149°F)			
Software Features	Languages	English / Traditional Chinese / Simplified Chinese			
	Save & Load Waveform	Yes			
	Regular Waveform Generator	Synchronous / Asynchronous Counter, I ² C, MIPI I3C, MIPI RFFE, PMBus, PWM, SPI, ...			
	Waveform Editing Interface	Waveform Drawing/Script File			
Device Dimension	L x W x H (mm ³)	123 x 76 x 21			
Weight		680g			
Lead Cable (Data / CLK-IN / CLK-OUT / Event / GND / N.C.)		A 40-pin lead cable (16 / 1 / 1 / 3 / 18 / 1)			
Grippers		20	40		
Data Output	Channels	8 with OE	16 with OE		
	Data Rate	100Mbps (Max.)	200Mbps (Max.)		
	Group	1 (ch0~7 & CKO)	2 (ch0~7 & CKO, ch8~15)		
	VoH min.	0.8Vpp @ <= 15Mbps	0.8Vpp @ <= 15Mbps,		

		1Vpp @ ≤ 100Mbps	1Vpp @ ≤ 100Mbps, 1.1Vpp @ ≤ 200Mbps	
	VoH max.	4.5V		
	VoL	0V		
	Min. Pulse Width	10 ns	5 ns	
	Impedance	CMOS with 20 Ohms		
	Fan Out	20mA/ch @ 50 Mbps		
	Output Enable	All channels		
Event Input	Internal	Hot Key		
	External	Channels	3	
		Mode	Logic AND / Logic OR	
		Threshold	-4V ~ +6V	
		Frequency	200MHz (Max.)	
		Operation	-10V~10V	
		Non Destructive	±30V DC, 12Vpp AC (Non-destructive)	
		Min. Pulse Width	5 ns	
		Sensitivity	1.5V	
		Impedance	200KΩ 7pF	

Chapter 2 Operation


It will show as the following after executing software.





1 Tool Bar

 Open File : Open *.DGP file.

 Save File : Save *.DGP file (current protocol settings).

 Save All : Save *.DGP file (current all protocol settings).

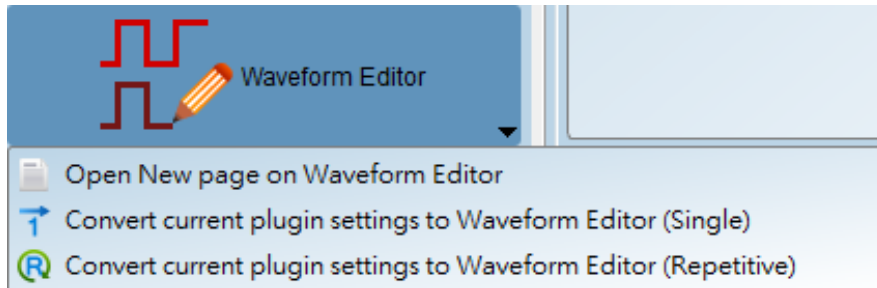
 Languages: Display language. You can select English, Traditional Chinese, or Simplified Chinese


 Option : System environment settings. Here you can set the working directory, the label

height and hot key.

2 Utility  / Protocol  /General 

③ Waveform Editor



 Open New page on Waveform Editor : Switch to the Waveform Editor, you can draw

waveform by manual.



Convert current plugin settings (waveform) to Waveform Editor (Single).



Convert current plugin settings (waveform) to Waveform Editor (Repetitive).

④



Output Level : Adjust the output voltage.

⑤

1. Operation Mode: Set the Convention format (x1, x2, x4, x8), which will influence the final output frequency.
2. Working Frequency: set the device working frequency, maximum is 300Mbps.
 ※ Ex. Output frequency = 150Mbps × x4 Conventional format = 600Mbps = 300MHz

DG4000 series : Set DG4K / EV4K / OE4K / LVDS / DG / EVENT / OE POD
output/input voltage.

H/W Configuration

Operating Mode: Timestamped format (96 Channels)

Probe Configuration (Maximum Available Channels: 128)

Working Frequency Multiple Factor: 1 x
Available Channel Number: 96
Command Availability: Every points
Group controlled Output Enable: Supported

Clock Mode: Internal

Working Frequency (1bps - 300Mbps, resolution: 6 digits): 1 x [200.000000] Mbps = 200Mbps interval 5ns

Device Memory: 10 M points (3.91%)

Legend:
 - DG Tip with Group controlled Output Enable
 - OE Tip with individual Output Enable
 - Event Tip for input
 - LVDS Tip for differential output

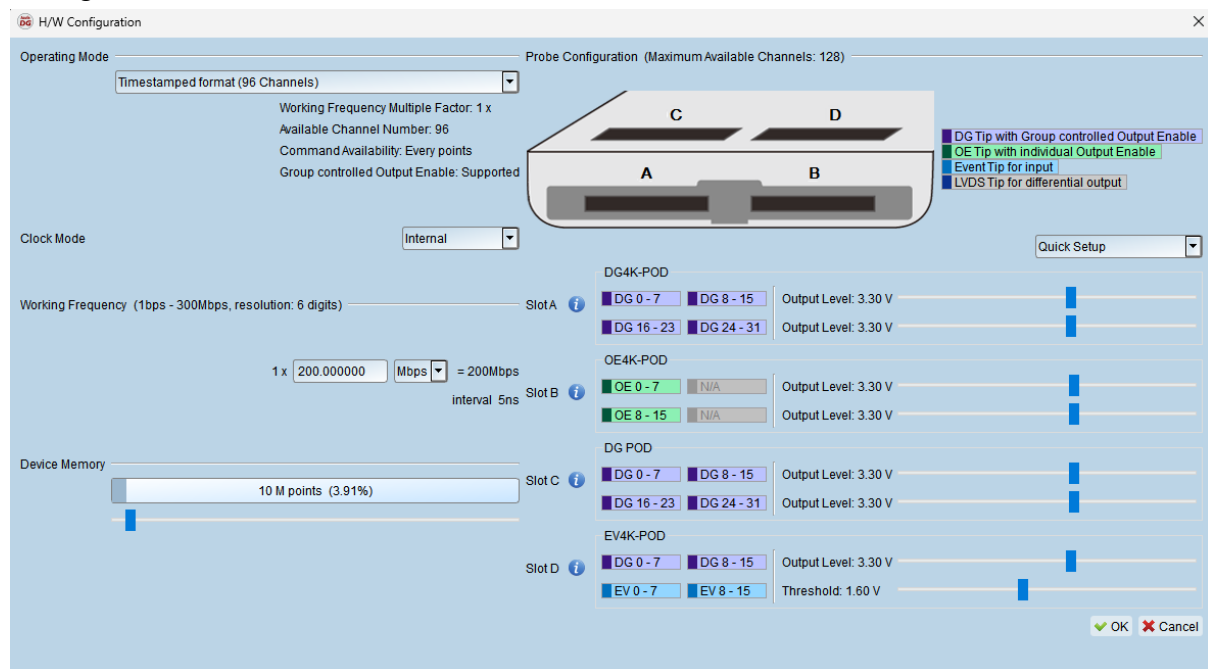
Slot A (DG4K-POD):
 - DG 0 - 7, DG 8 - 15, Output Level: 3.30 V
 - DG 16 - 23, DG 24 - 31, Output Level: 3.30 V

Slot B (DG POD):
 - DG 0 - 7, DG 8 - 15, Output Level: 3.30 V
 - DG 16 - 23, DG 24 - 31, Output Level: 3.30 V

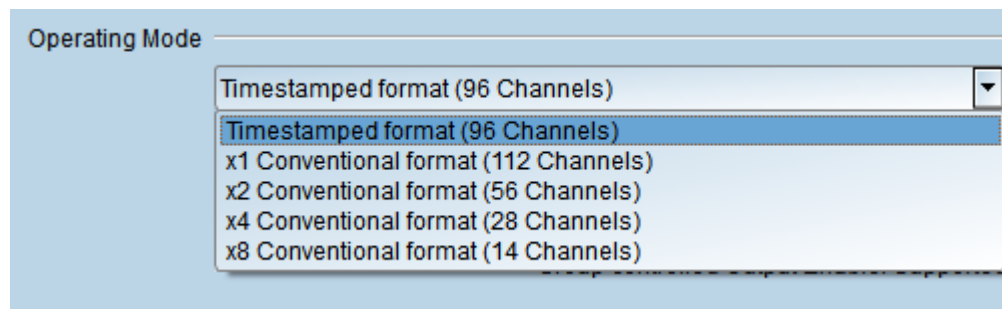
Slot C (OE4K-POD):
 - OE 0 - 7, N/A, Output Level: 3.30 V
 - OE 8 - 15, N/A, Output Level: 3.30 V

Slot D (EV4K-POD):
 - DG 0 - 7, DG 8 - 15, Output Level: 3.30 V
 - EV 0 - 7, EV 8 - 15, Threshold: 1.60 V

DG3000 series : Set DG4K / EV4K / OE4K / DG / EVENT / OE POD output/input voltage.



Operating Mode :



Timestamped format (96 Channels):

Enable the repeat count function, the maximum output rate is 300 Mbps.

x1 Conventional format (112 Channels):

Disable the repeat count function, the maximum output rate is 300 Mbps.

x2 Conventional format (56 Channels):

Enable the x2 base frequency, the maximum output rate is 600 Mbps.

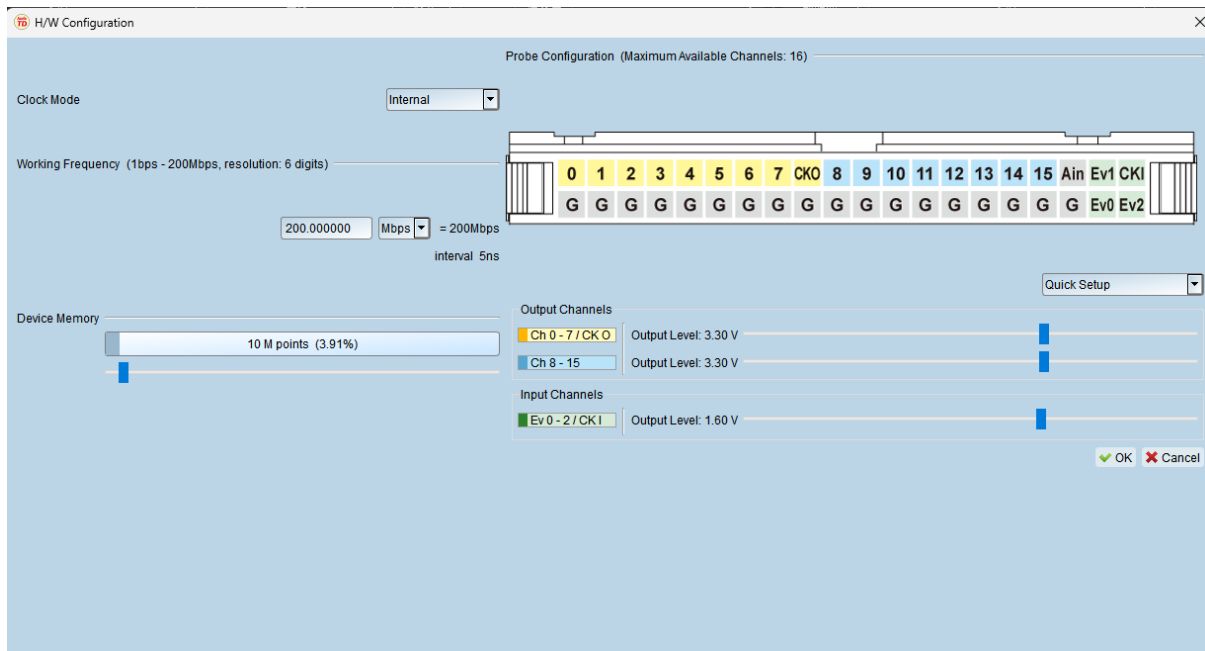
x4 Conventional format (28 Channels):

Enable the x4 base frequency, the maximum output rate is 1.2 Gbps.

x8 Conventional format (14 Channels):

Enable the x8 base frequency, the maximum output rate is 2.4 Gbps.

TD3000 series : Set CH0~CH15/Ev0-2/CKO/CKI output/input voltage.



Clock Mode : select Internal / Clk-In (MCX port) / CLK (I) or CKI.

- **Internal:** select the internal clock.
- **Clk-In (MCX port):** select the Clk-In of MCX port to input the external clock signal.

DG3000 Series/4000 Series Clk-In (MCX port)



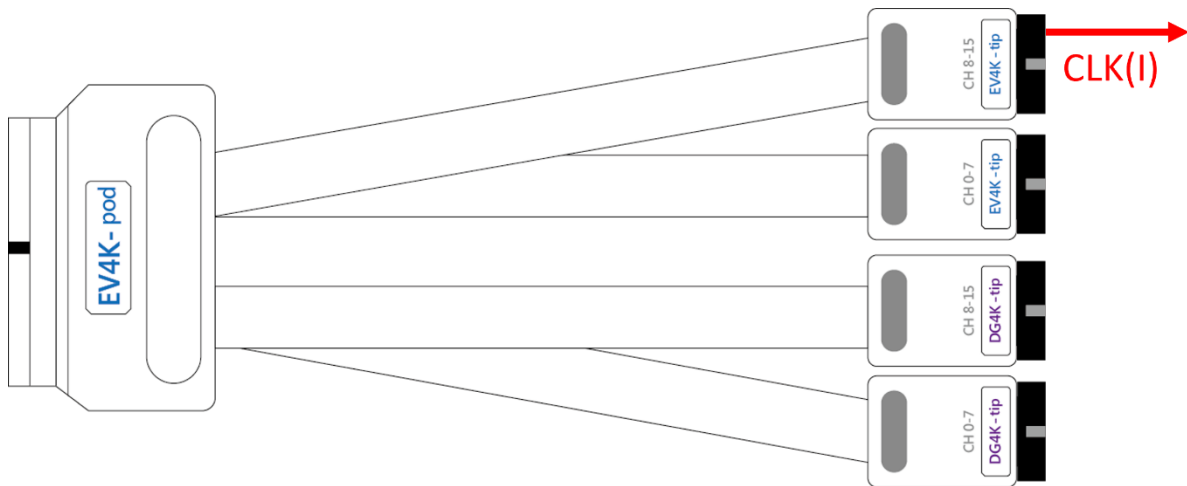
TD3K Clk-In (MCX port)



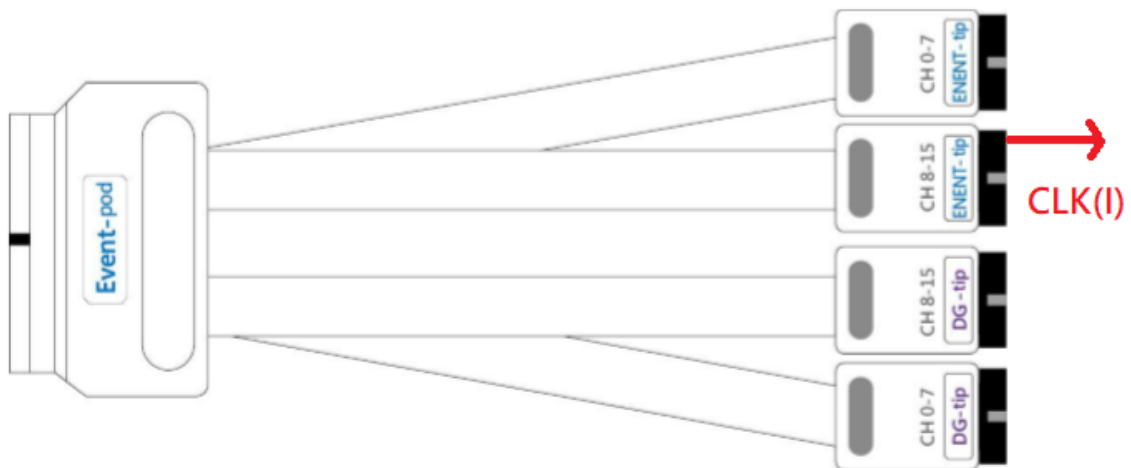
This specification is TTL3.3V, the input voltage must be higher than 2.4V (identified as 1), DG3000 Series / DG4000 Series / TD3000 Series can work normally in External Clock mode, and the maximum input frequency is 200 MHz.

CLK (I):

DG4000 Series CLK(I)

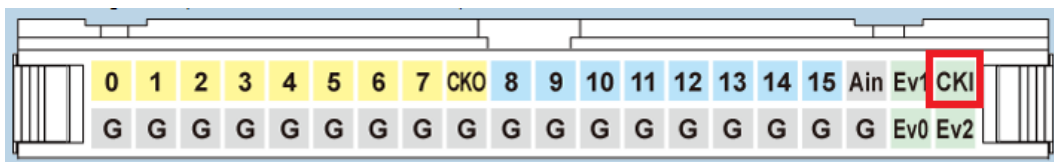


DG3000 SERIES CLK(I)



The input voltage is adjustable, and the input voltage range is -0.5V ~ 4.5V.

TD3000 Series CKI



The input voltage is adjustable, and the input voltage range is -5V ~ 5V.



Run : Output the waveform once.



Repeat: Output the waveform 1~∞ times..

Utility

DGW/DGV

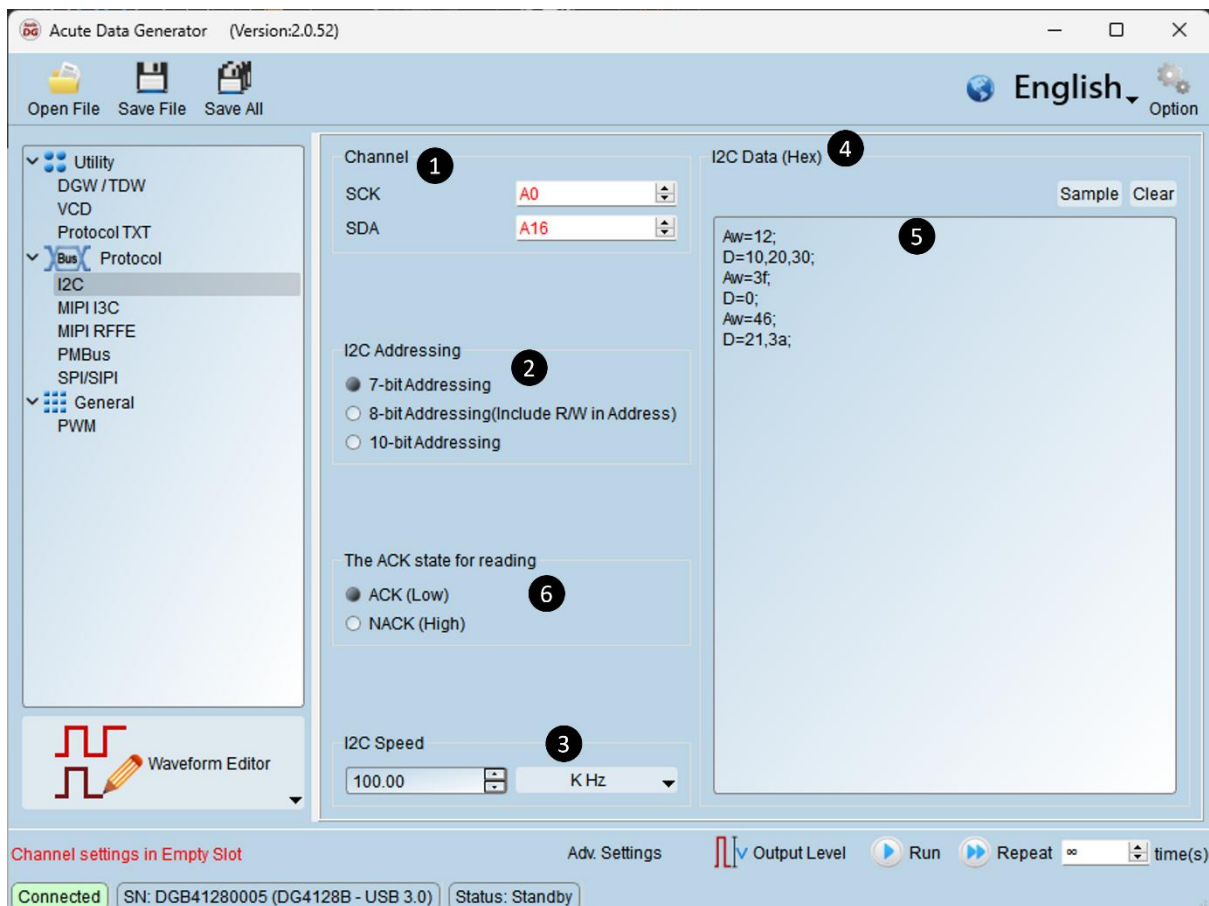
This function can output the waveform from the waveform file of DG3000 Series /DG4000 Series /TD3000 series (*.DGW/*.TDW/*.DGV).

VCD

This function can output the waveform from Value Change Dump (*.VCD).

Bus Protocol

I2C



❶ Channel : Select SCK/SDA channel.

❷ I2C Addressing : Select 7-bit Addressing/8-bit Addressing (include R/W in Address)/10-bit Addressing.

❸ I2C Speed (bit/s) : Range: 10 bps ~ 50 Mbps.

❹ I2C Data(Hex) :

Sample : Generate I2C data.

Clear : Clear I2C data.

5 I2C data format :

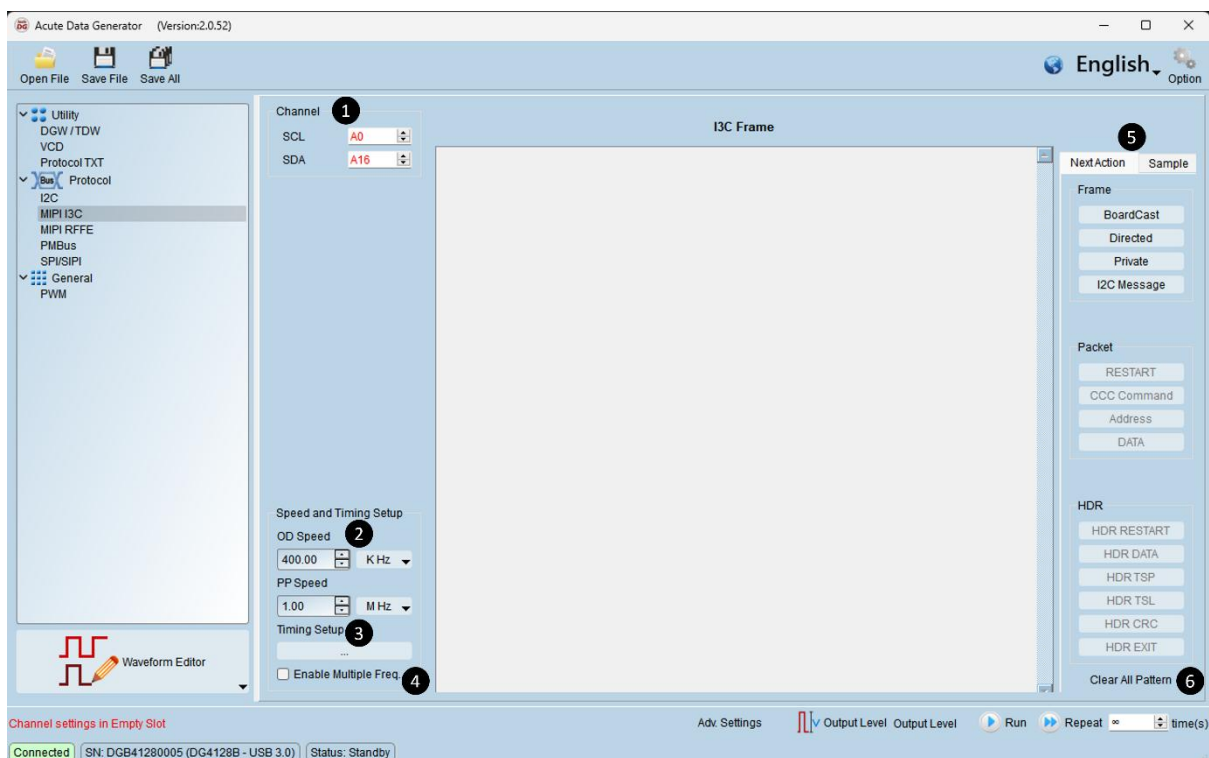
Aw/Ar: I2C Address Write / Address Read.

D : I2C data.

Each I2C data is separated by a comma (,) and each row ends with a semicolon (;).

6 ACK/NACK: Simulate the slave behavior, but only available while the "Disable Hi-Z" being checked in Advance Setting.

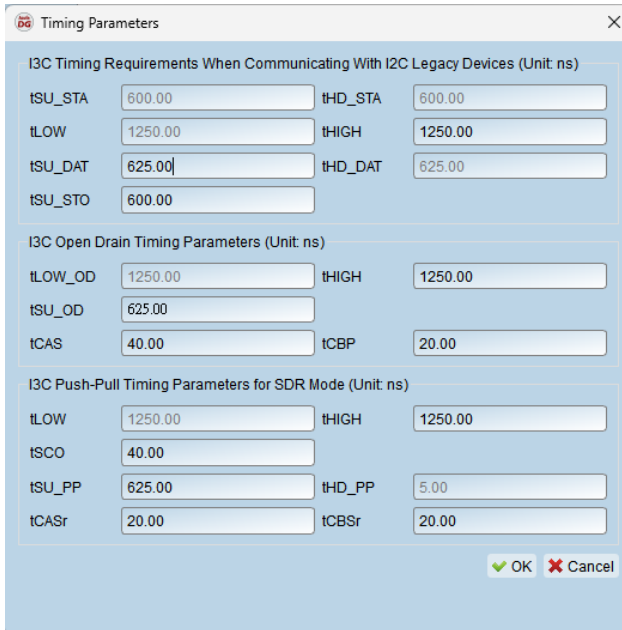
MIPI I3C



1 Channel: Set SCL/SDA channel.

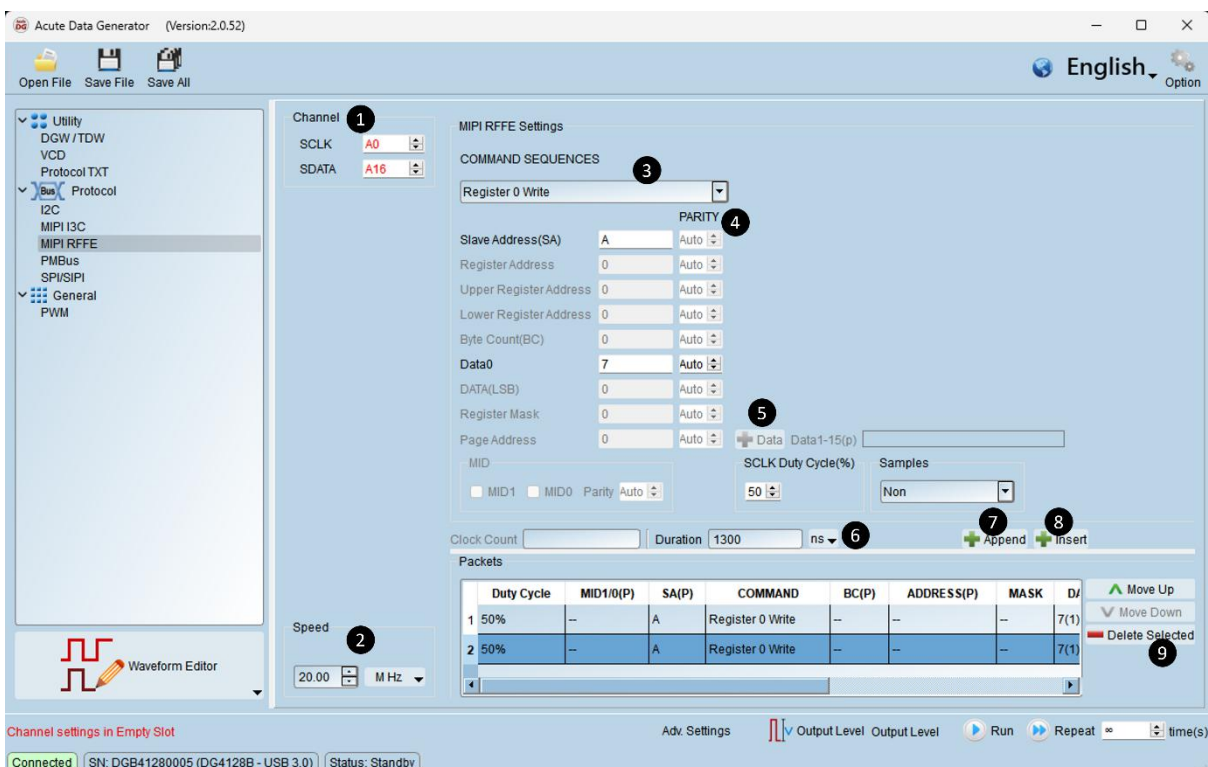
2 Speed Setup: Set the speed.

3 Timing Setup: Detail timing setting.



- ④ Enable Multiple Frequency: Enable multiple frequency function while being checked.
- ⑤ Next Action/Sample: Add some I3C template.
- ⑥ Clear All Pattern: Clear all appended template.

MIPI RFFE



- ① Channel : Set SCLK/SDATA channel.
- ② Speed : The maximum speed is 100 MHz.

③ MIPI-RFFE COMMAND SEQUENCES

1. REGISTER 0 WRITE
2. REGISTER WRITE/READ
3. EXTENDED REGISTER WRITE/READ
4. EXTENDED REGISTER WRITE/READ LONG
5. INTERRUPT SUMMARY AND IDENTIFICATION
6. MASKED WRITE
7. MASTER OWNERSHIP
8. MASTER WRITE/READ
9. MASTER CONTEXT TRANSFER WRITE/READ

④ PARITY : It will generate the parity automatically when select AUTO and become red color when select invalid parity.

⑤ DATA : Append data when the quantity > 1 byte.

Packets											▲ Move Up	
	Duty Cycle	MID1/0(P)	SA(P)	COMMAND	BC(P)	ADDRESS(P)	MASK	DATA(P)	CLOCK COUNT	DURATION		▼ Move Down
1	50%	--	A	Register 0 Write	--	--	--	7(1)	--	1300 ns		■ Delete Selected
2	50%	--	A	Register 0 Write	--	--	--	7(1)	--	1300 ns		

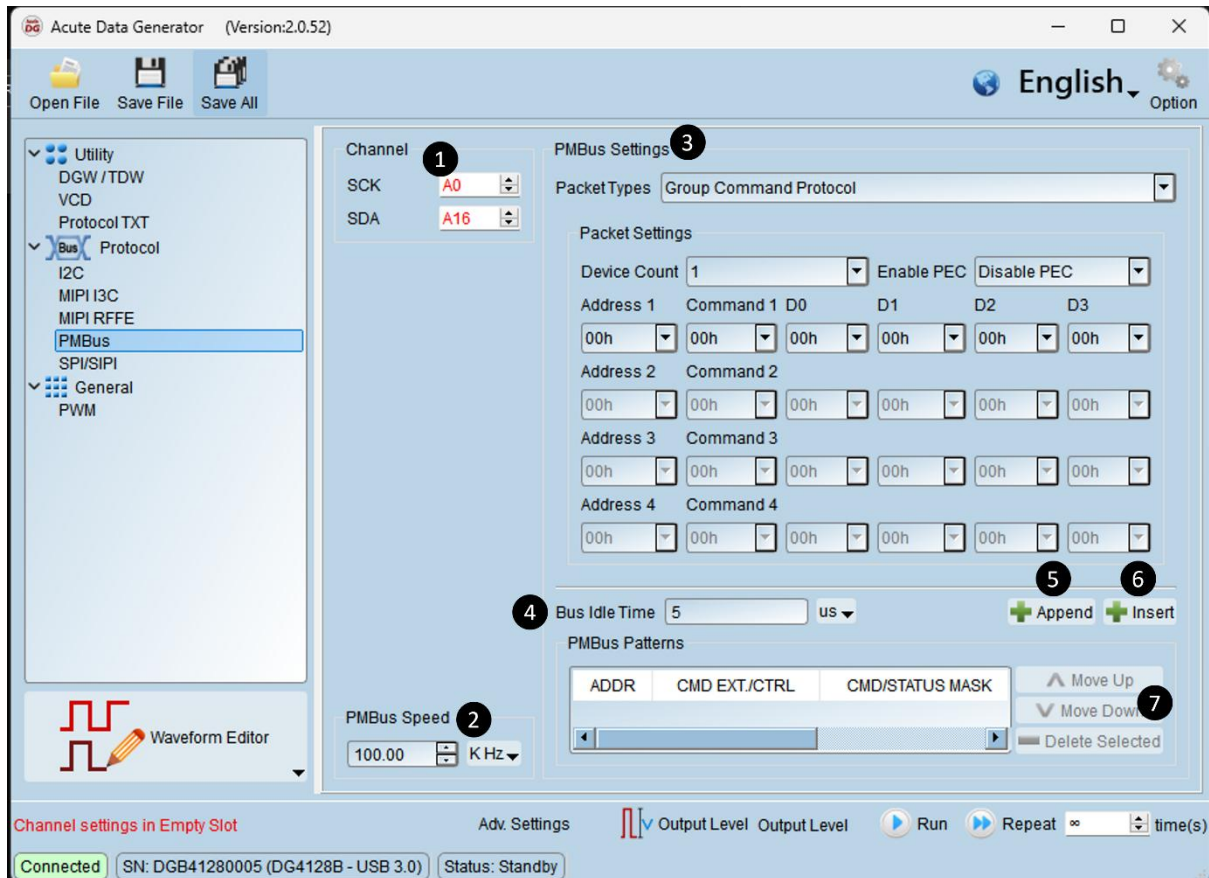
⑥ Duration : Set the Idle time, the minimum idle time is 5 ns, 0 means no idle time.

⑦ Append : Append a new packet in the list.

⑧ Insert : Insert a new packet after the selection.

⑨ Move up/ Move Down/ Delete Selected : Move up/move down/delete the selection.

PMBus



❶ Channel : Select SCK/SDA channel.

❷ PMBus Speed : Set PMBus protocol speed, its range is 1 KHz ~ 100 MHz.

❸ PMBus Settings :

Packet Types: Select PMBus packet, each packet has different frames, it will show these frames on the following section.

❹ Bus Idle Time : Set the Idle time, the minimum idle time is 5 ns, 0 means no idle time.

❺ Append : Append a new packet in the list.

❻ Insert : Insert a new packet after the selection.

❼ Move up/ Move Down/ Delete Selected : Move up/move down/delete the selection.

SPI/SIPI



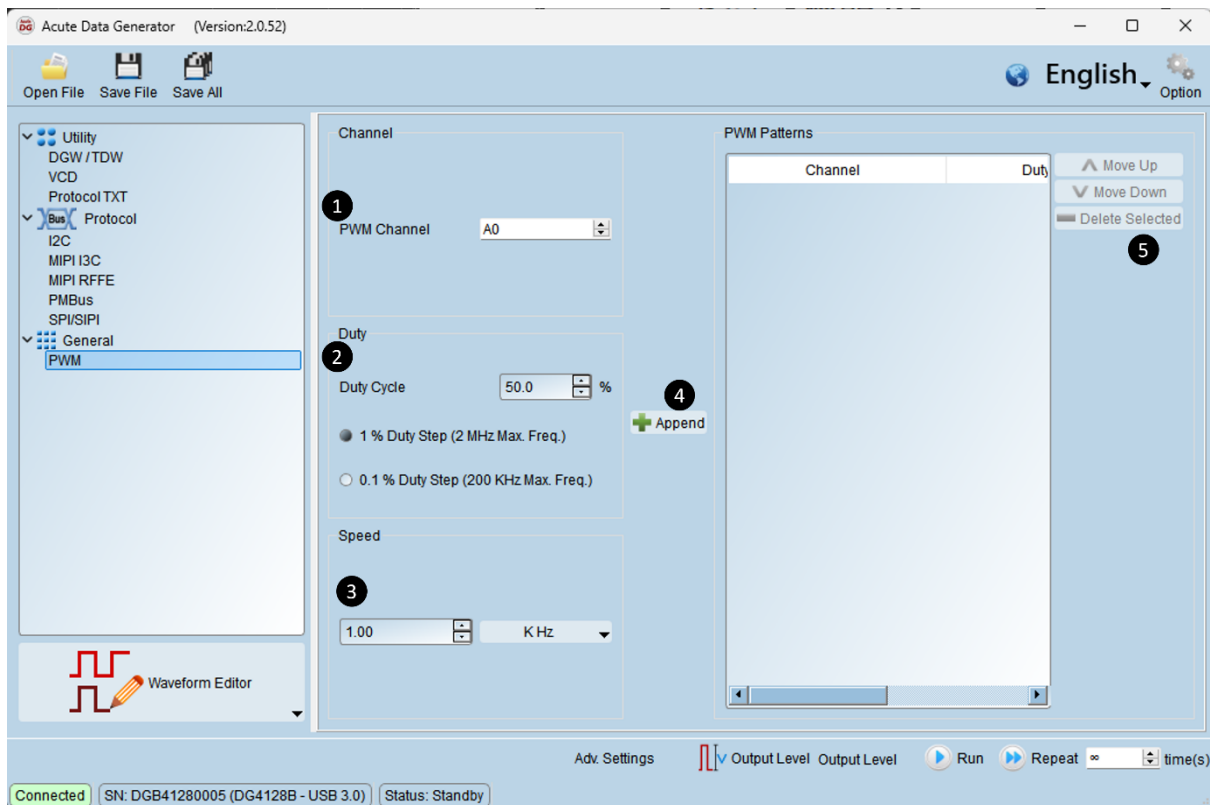
- ❶ Type : 4 Wire-SPI, 3 Wire-SPI, 3 Wire-SPI (Unused Chip Slave), 2 Wire-SPI (Unused Chip Slave) and SIPI included.
- ❷ Channel : Select Chip Select/SCK/SDI/SDO channel.
- ❸ Word Size: Select the word size, its range is 4 ~ 40 bits.
- ❹ SPI/SIPI Speed : Set SPI/SIPI protocol speed, its range is 1Kbp ~ 100Mbps.
- ❺ SPI/SIPI Data Settings
 - SPI Data: Only hex format supported.
 - SIPI Clock/Data: SIPI clock number and SIPI data.
 - Load from file: The bin/txt file format supported, selecting the type before loading file.
 - SDI(Write)-Latency-SDO(Read): Set SDI-Latency-SDO mode, the parameters are as the following:
 1. Write Length: Write character width.
 2. Read Length: Read character width.
 3. Latency: Latency width.
 4. Frame Guard Time: Interval time.
- Bus Idle Time : Set the Idle time, the minimum idle time is 5 ns, 0 means no idle

time.

- ⑥ Append : Append a new packet in the list.
- ⑦ Insert : Insert a new packet after the selection.
- ⑧ Move up/ Move Down/ Delete Selected : Move up/move down/delete the selection.
- ⑨ Overwrite: Overwrite the selected data with the new SPI data.

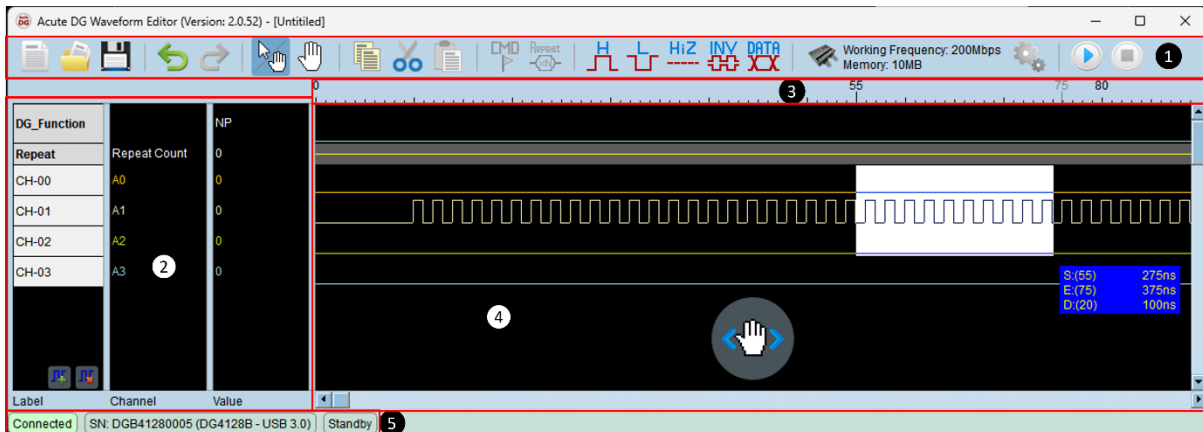
General

PWM



- ① PWM Channel: set the PWM channel.
- ② Duty Cycle: set the PWM Duty Cycle ◦
- ③ Speed: set the PWM speed, Range: 100 Hz ~ 2 MHz.
- ④ Append: append the settings in the PWM pattern list.
- ⑤ Move up/ Move Down/ Delete Selected: Move up/move down/delete the selection.

Waveform Editor



1 Tool Bar



New Page : Empty the waveform.



Open File : Open the *.dgw/*.dgv/*.tdw file.



Save File : Save the settings and waveform as a *.dgw/*.dgv file.



Undo



Redo



Drag Waveform : Switch the mouse operation to the drag mode.



Auto : Switch the mouse operation to the auto mode.



Copy : Copy the selected waveform to the clipboard.



Cut : Cut the selected waveform to the clipboard.



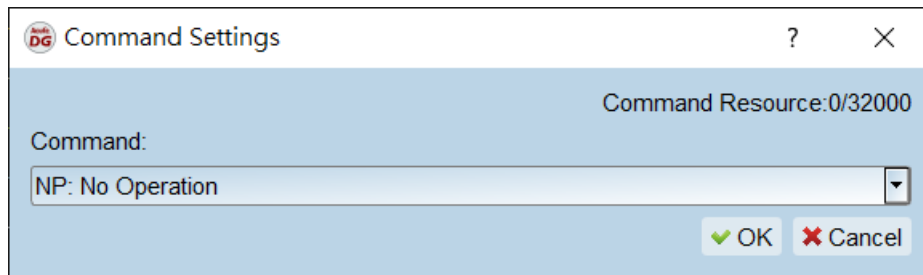
Paste : Paste the waveform from the clipboard to the selected area.



Edit Command : Insert a command to the selected position.

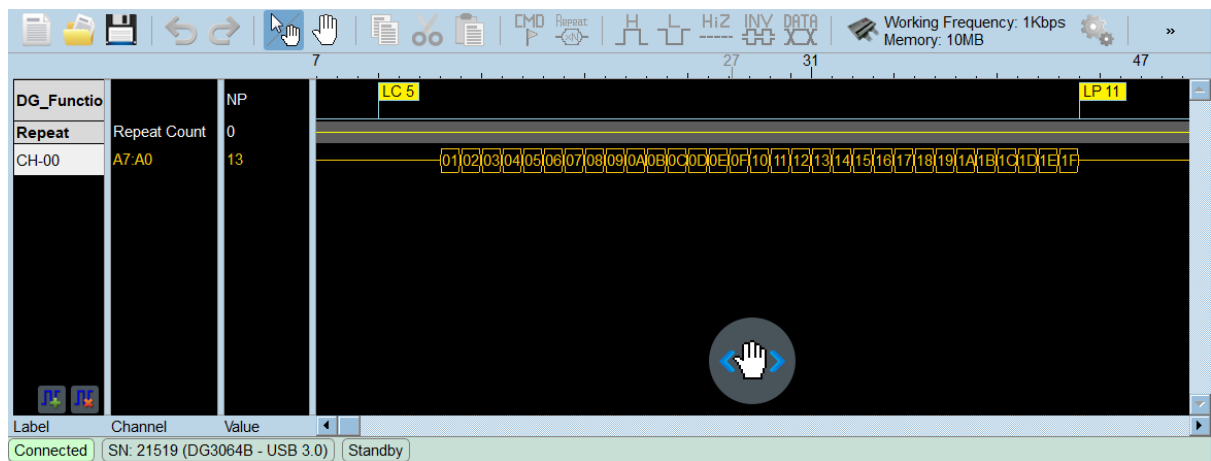


Delete Command : Delete the selected commands.



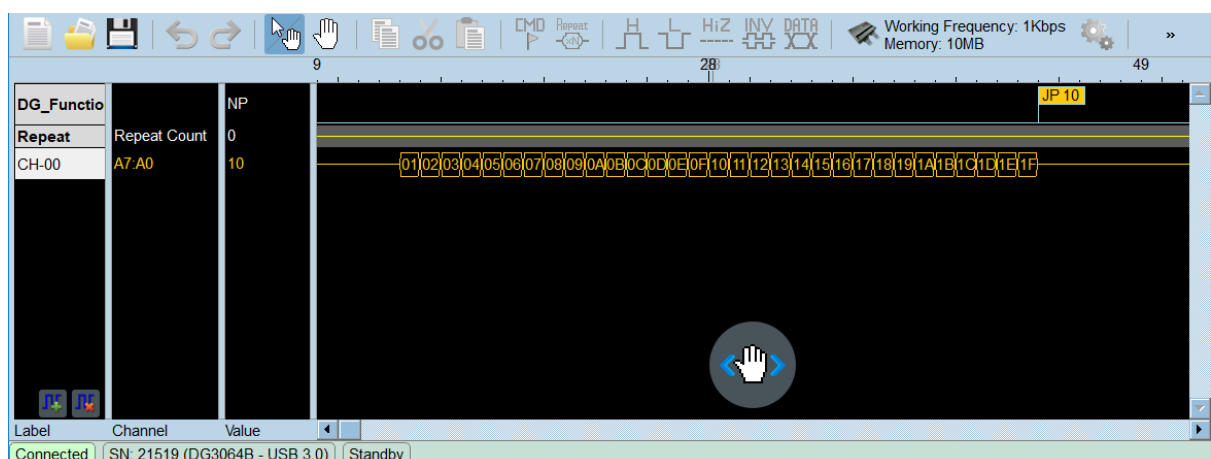
1. No Operation (NP): No commands (default).
2. Loop Count (LC): Set the loop count, its range is 1~ 8,388,607.
3. Loop to New Address (LP) : Set a limited count to output the waveform with LC.

Output the waveform 5 times:



4. Jump to New Address (JP) : Jump to a new address to output the waveform repeatedly.

Output the waveform repeatedly until press the Stop button.



5. Wait Event (WE): Set an event command, support the Event 0~2 / Keyboard Event / Event Invert.

Event 0~2 means that Event-tip (DG3000 Series) channel 0~2 or Ev0~2 (TD3000

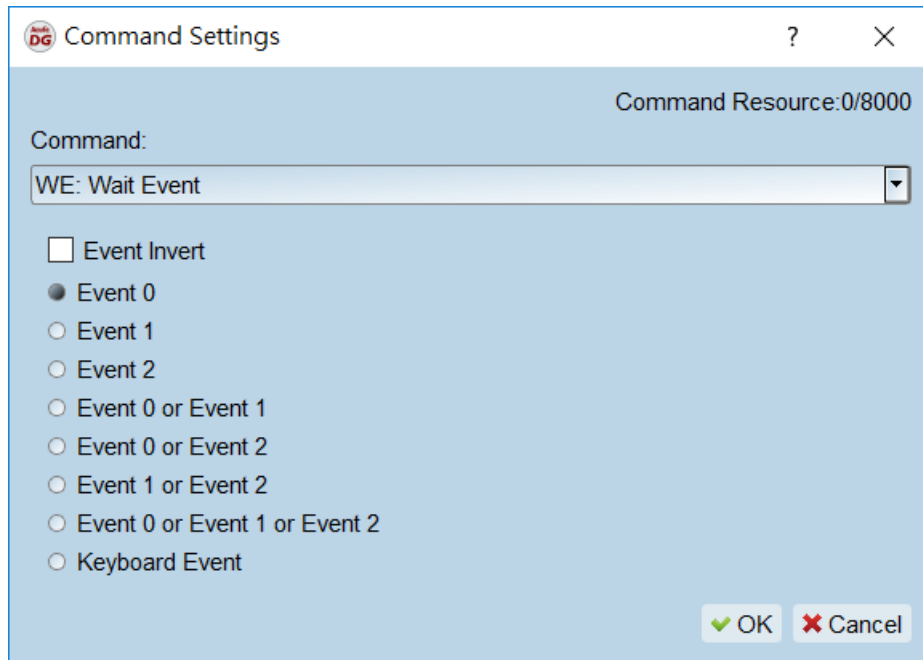
Series) channel.

The event occurred when these channels received a pulse.

6. Keyboard Event means the Space (default) or Enter key from the computer keyboard.

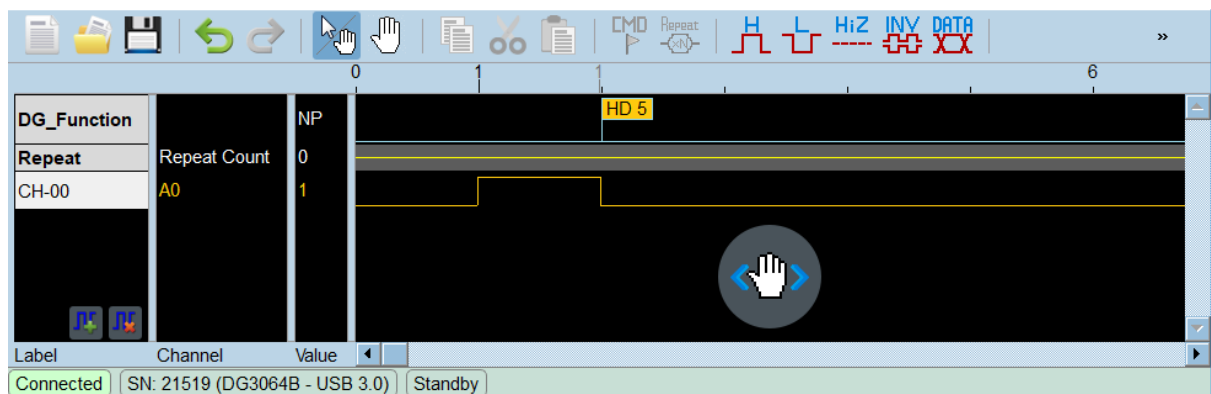
The event occurred when the Space or Enter key was pressed.

Event Invert means that invert the event waveform.



7. Hold Count (HD): Set the count of the waveform, its range is 1~ 8,388,607.

The width of the pulse is 5 ns, it will become 25 ns when insert a HD 5 command.



These 2 functions are only provided for by DG3000 Series/DG4000 series:

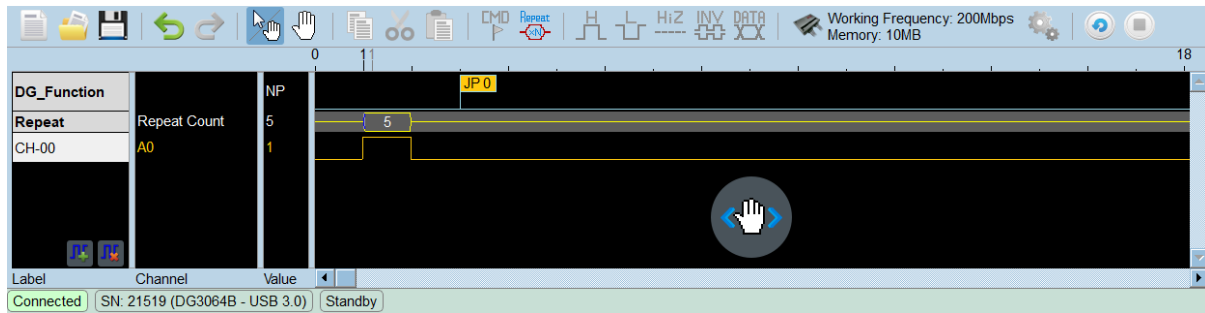



Edit Repeat Count : Insert a Repeat Count command.





Delete Repeat Count : Delete the Repeat Count command.

The width of the pulse is 5 ns, it will become 25 ns when insert a Repeat Count = 5.



 High – Draw high (1) waveform.


 Low – Draw low (0) waveform.


 High Impedance – Draw the high impedance waveform.


It is 16 channels for a group when use the DG-tip to set the high impedance, e.g. set channel 0 as high impedance and channel 1 ~ 15 will be at high impedance, too.

Channels of OE-tip or TD3000 series can be set the high impedance each by each.

 Inverse : Invert the waveform.

 Edit Data : Generate the patterns that value/step counter/clock or bit/ baud rate data.

 Hardware Settings : Set the working frequency, device memory and output level/threshold.

 Environment settings : Set the path of working directory and hot key about the event.

 Run : Output the waveform.

 Run again : Output the waveform again.



Stop: Stop the waveform output.

② Channel

Label : Show the channels.

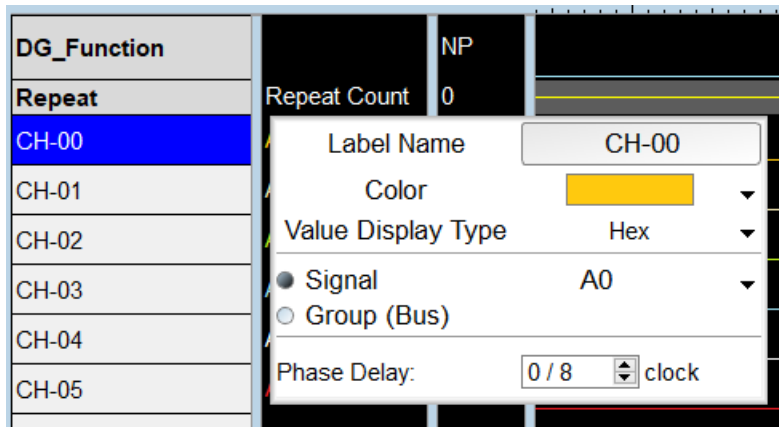


() add new channel label, () delete the selected channels label.

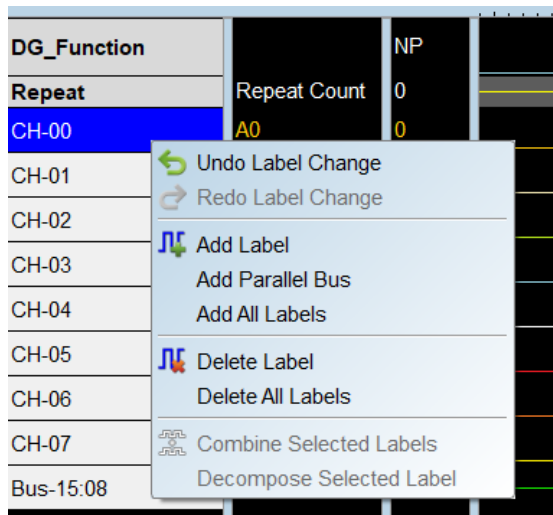


Selected the label and click the left button of mouse.

Phase Delay only works at DG3000 Series/DG4000 series and the data rate must be set less than or equal to 300Mbps.



Click the right button of mouse.



Channel : Show the channel number.

Value : Show the channel value at the position of the cursor.

③ Waveform Scale Area

Black color value of the left side : Show the start address of the selected range.

Black color value of the right side: Show the end address of the selected range.

Black color value in the range of waveform area: Show the address at the position cursor clicked.

Gray color value in the range of waveform area: Show the address at the position cursor stamped.

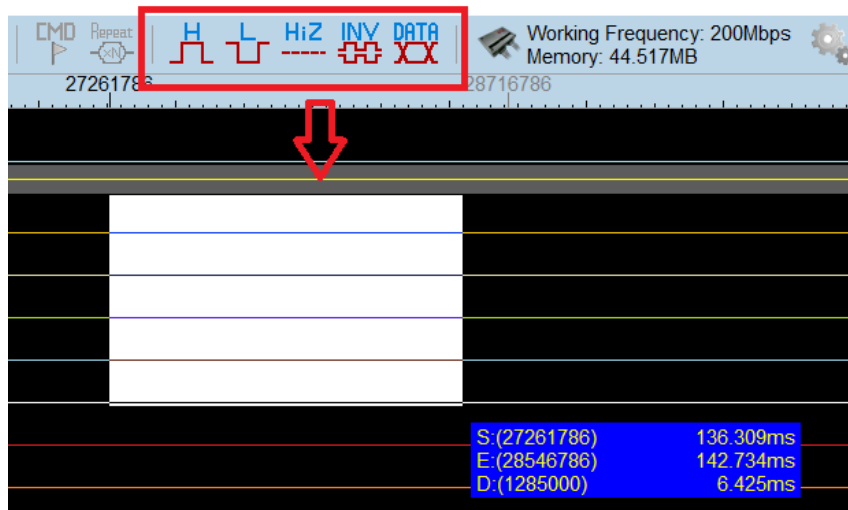
④ Waveform Area

Zoom in/out the waveform by scrolling the mouse wheel to make the waveform.

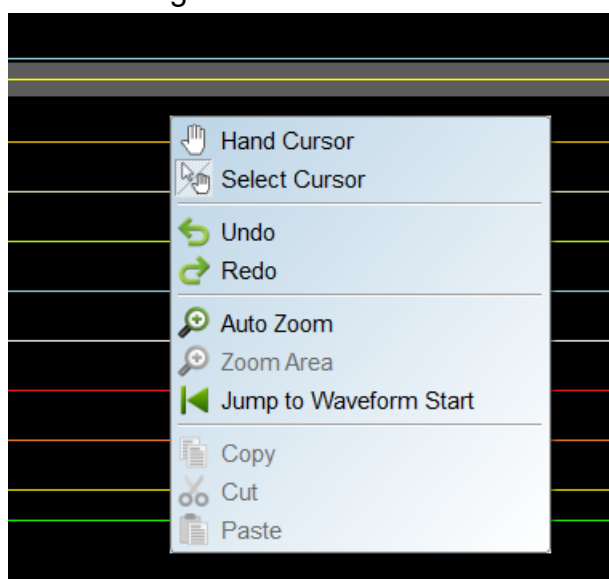
Drag the waveform by press the button of the following:



Select an area to edit the waveform:



Press the right click in the waveform area.



⑤ Device Status

Show the device connection status/serial number/interface.

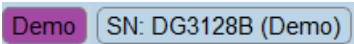
Chapter 3 Technical support

Contact information

Acute website : <http://www.acute.com.tw>

E-Mail : service@acute.com.tw

Tel: +886-2-29993275 Fax: +886-2-29993276

If  shows up in the Demo mode during the execution of software,

please try the following steps to solve the issue:

(1) Install the latest version of the software, please go to the official website of Acute Technology Inc. - Download - Software, and then select the Data Generator to download and install.

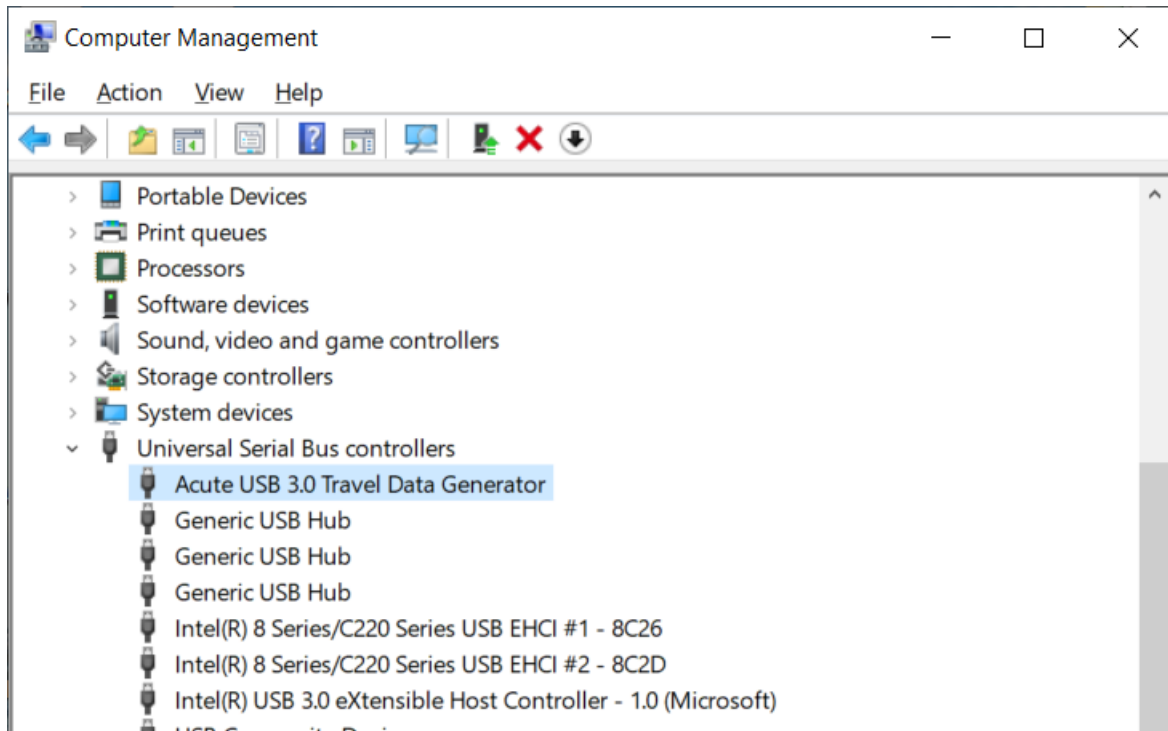
(2) Please use the original USB3.0 Cable in the kit.

(3) Go to the device manager and check the driver status.

Please connect the device USB cable to the computer and then go to the system device

manager to check whether the Acute USB 3.0 (Travel) Data Generator shows up.

Please go to the Acute Website - Download - Software, download the USB3.0 driver and follow the troubleshoot manual in the package to reinstall the driver.



(4) Remove all flat cables and re-plug the USB3.0 Cable or restart the computer to check

whether the driver appears.

(5) After the above steps are taken but the problem is still there, please contact us.

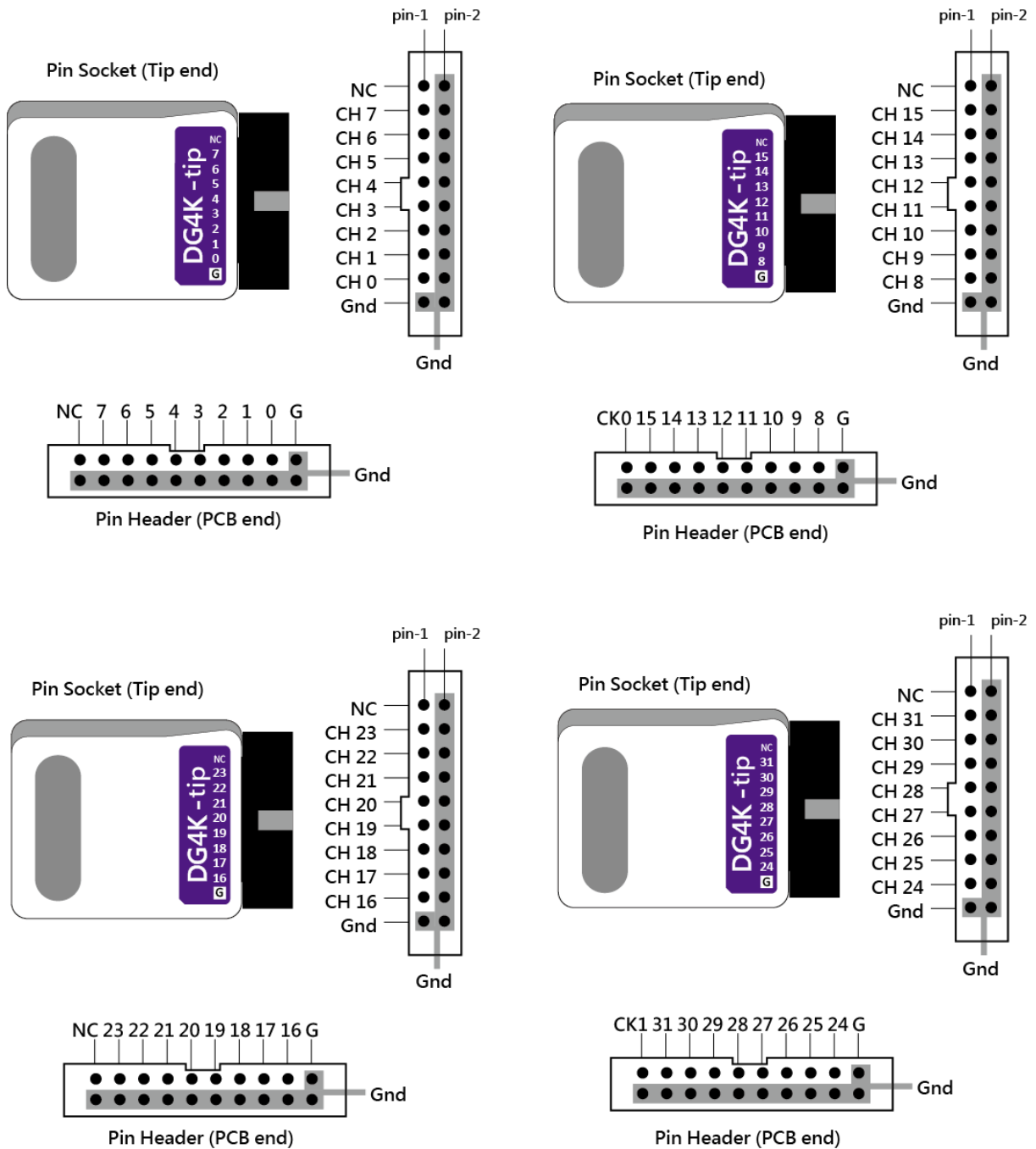
Appendix 1 Flat Cable pin defined & Dimension

DG4000 series

DG4K-pod Flat Cable

DG4K-pod flat cable tip pin defined

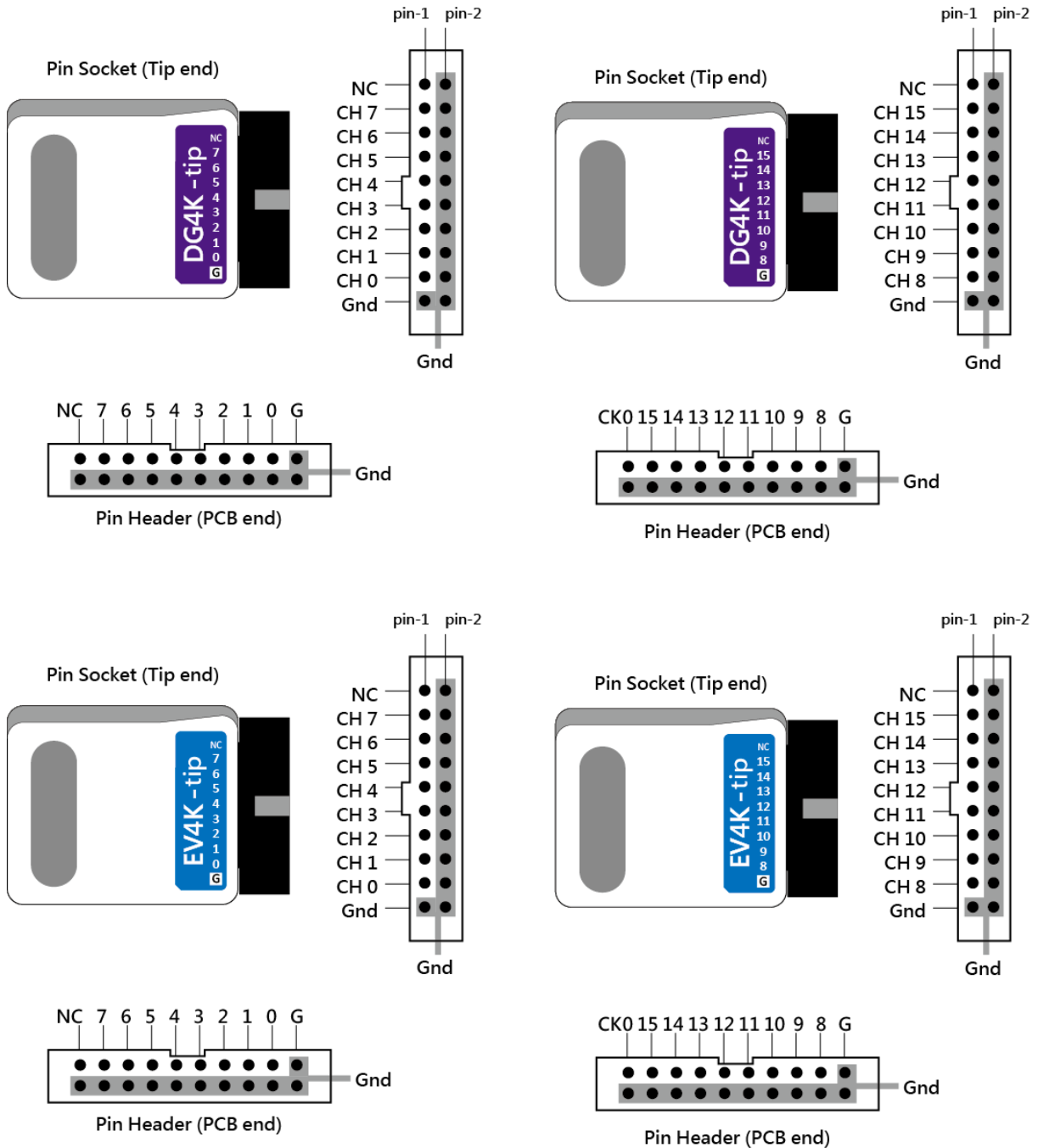
The following figure shows the definition of the four single-ended flat cable tips of the DG4K-pod flat cable.



EV4K-pod Flat Cable

EV4K-pod flat cable tip pin defined

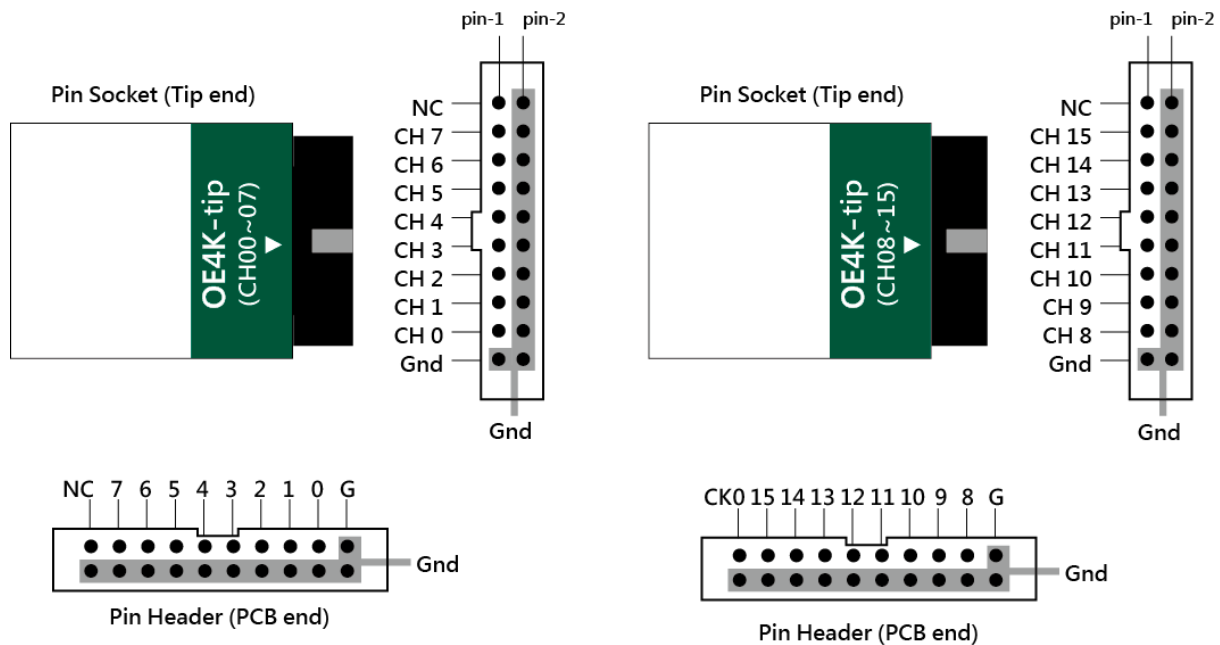
EV4K-pod flat cable has 2 single-ended DG4K-pod flat cable tips and 2 single-ended EV4K-pod flat cable tips, the following figure shows the definition of EV4K-pod flat cable tip.



OE4K-pod Flat Cable

OE4K-pod flat cable tip pin defined

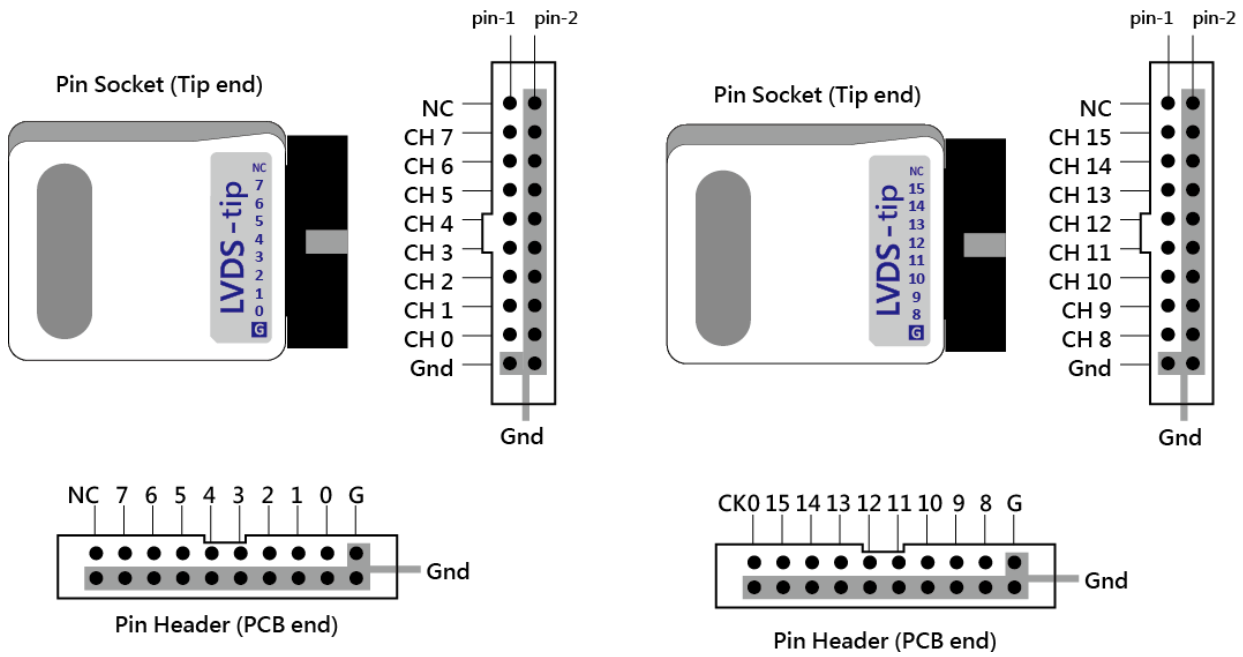
OE4K-pod flat cable has 2 single-ended DG4K-pod flat cable tips and 1 single-ended OE4K-pod flat cable tip, the following figure shows the definition of OE4K-pod flat cable tip.



LVDS-pod Flat Cable (Option)

LVDS-pod flat cable tip pin defined

LVDS-pod flat cable has two single-ended LVDS-pod flat cable tip, the following figure shows the LVDS-pod flat cable pin definition.

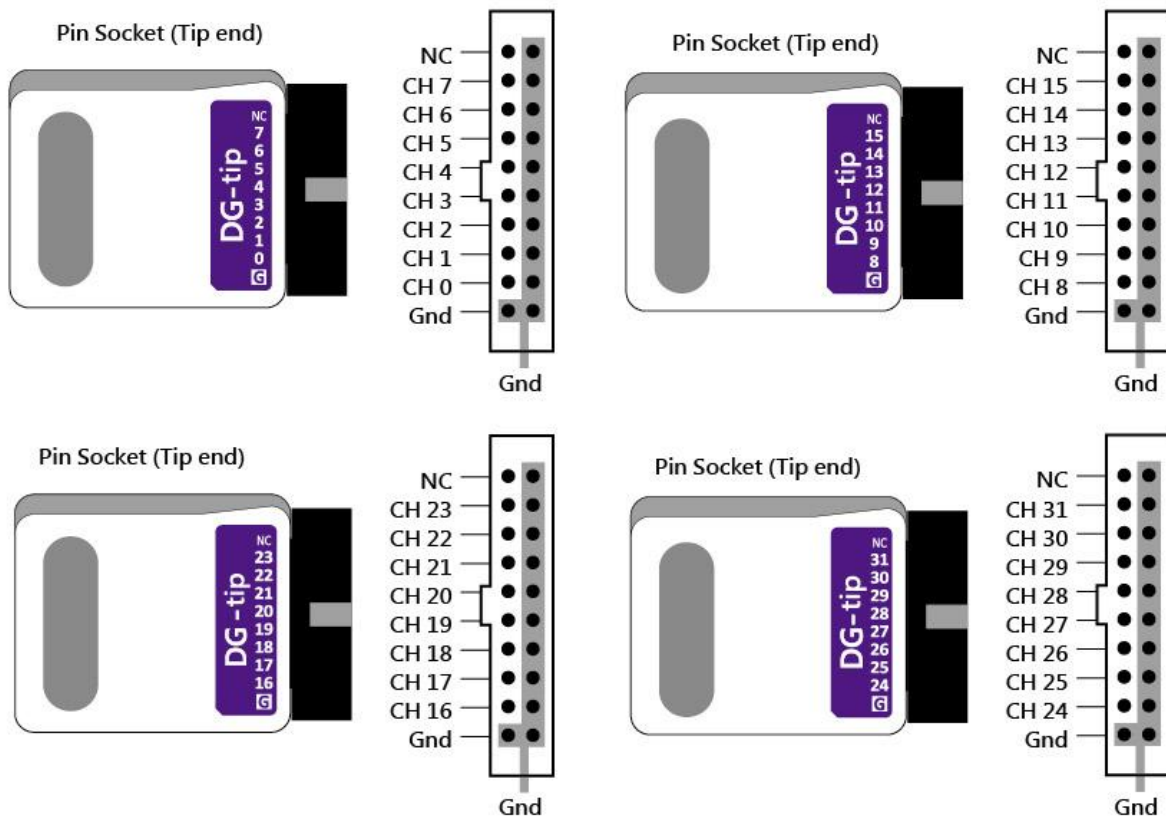


DG3000 series

DG-pod Flat Cable

DG-pod flat cable tip pin defined

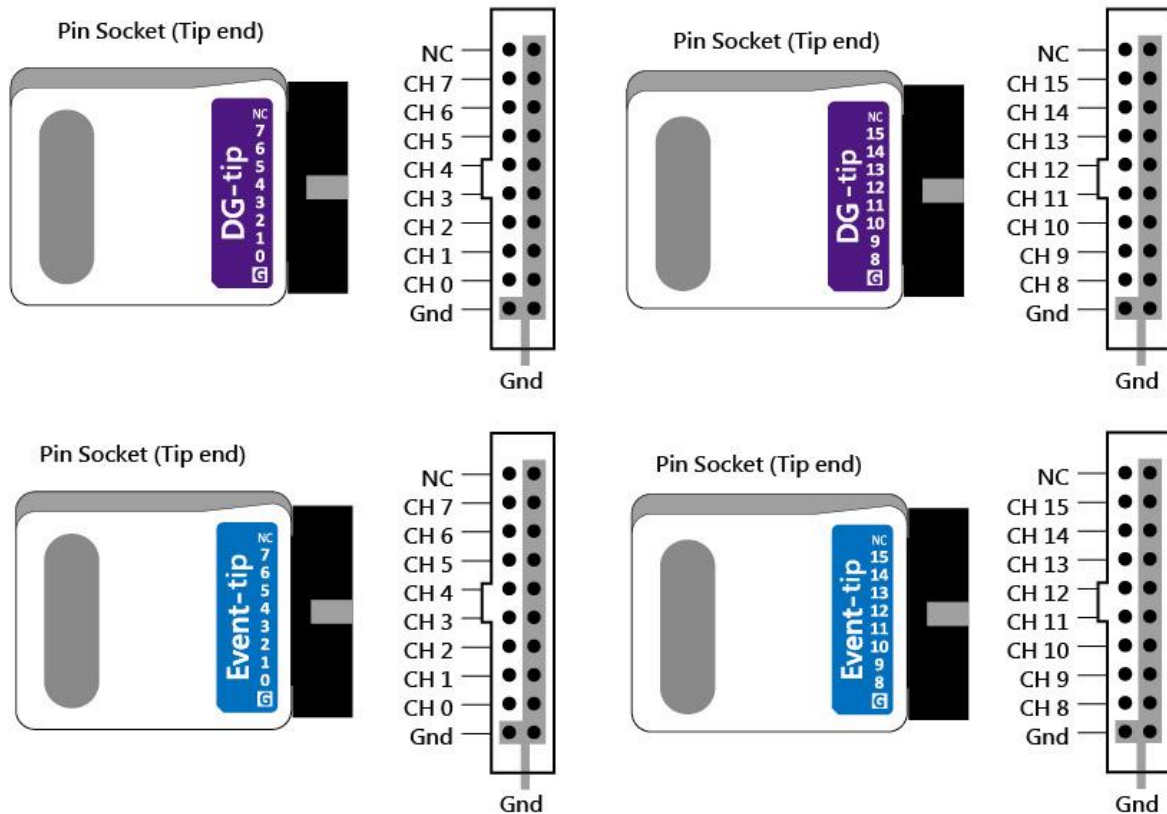
The following diagram defines the four single-ended flat cable tip pins of the DG-pod flat cable.



Event-pod Flat Cable

Event-pod flat cable tip pin defined

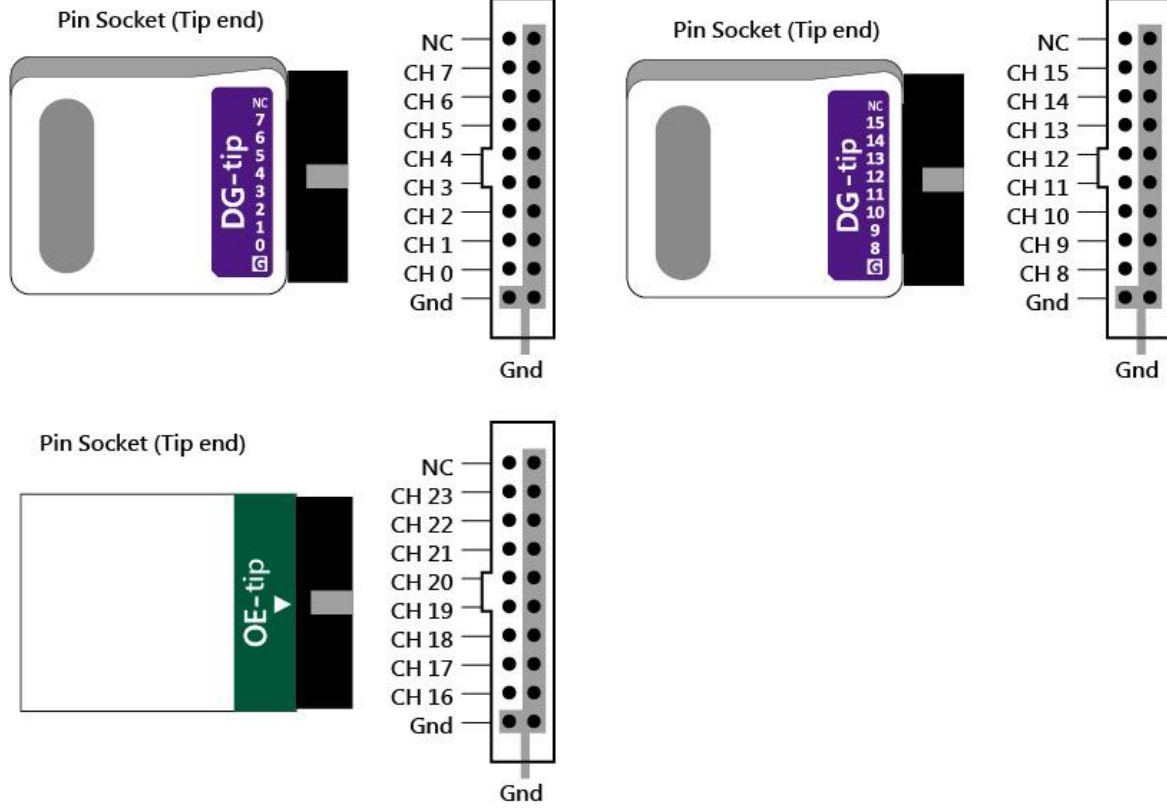
Event-pod flat cable has 2 single-ended DG-pod flat cable tips and 2 single-ended Event-pod flat cable tips, the following diagram defines the Event-pod flat cable tip.



OE-pod Flat Cable

OE-pod flat cable tip pin defined

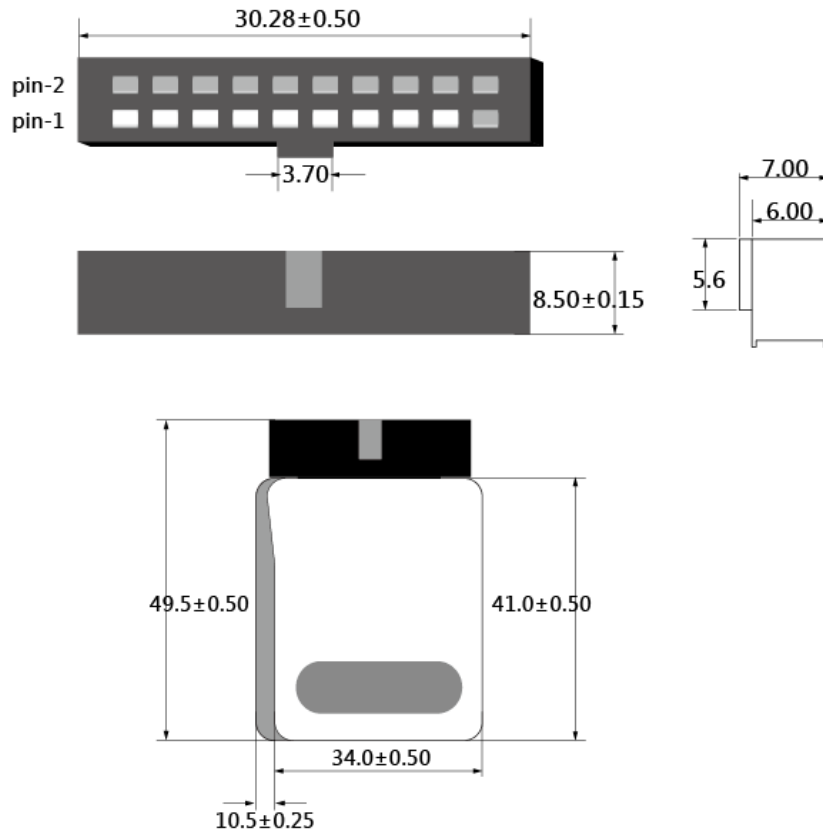
The OE-pod flat cable has two single-ended DG-pod flat cable tips and one single-ended OE-pod flat cable tip, the following diagram defines the OE-pod flat cable tip.



Flat Cable Tip Dimension

Mates with: 2.54mm box header or pin header

20-pin Data Generator: Flat Cable tip = Pin Socket , Pitch=2.54 , Unit : mm.



Appendix 2 Use text editor tool to edit vector file(dgv)

File Content

```

INPUTS
DG_CMD:-2,
DG_PARA:-1,
Clk:0,
Reset:1,
Write:2,
Check:3,
DataA[7..0]:15..8,
DataB[7..0]:23..16,
DG_OE0:120;
INTERVAL 125ns;
//FREQUENCY 8MHz;
VOLTAGE
2.5,3.3,3.3,3.3,3.3,3.3,3.3,1.6;
//DG_CMD, DG_PARA, Clk, Reset, Write, DataA, DataB, DG_OE0
PATTERN
:Start
    NP      0  0  0  0  1  00h  00h  0
    NP      0  1  0  0  0  00h  00h  0
    LC      5  0  0  0  0  00h  00h  0 //LC 5
    NP      0  1  0  0  0  00h  00h  0
:A0
    NP      0  0  0  1  0  55h  00h  0
    NP      0  1  0  0  0  55h  00h  0
    LC      3  0  0  0  0  55h  00h  0 //LC 3
    NP      0  1  0  0  0  55h  00h  0
    NP      0  0  0  0  0  55h  00h  0
    NP      0  1  0  0  0  55h  00h  0
    NP      0  0  0  0  0  55h  00h  0
:A1
    NP      0  1  1  0  0  00h  FFh  0
    NP      0  0  0  0  0  01h  FEh  0
    NP      0  1  0  0  0  02h  FDh  0
    NP      0  0  0  0  0  03h  FC  0
    NP      0  1  0  0  0  04h  FBh  0
    NP      0  0  0  0  0  05h  FAh  0
    NP      0  1  0  0  0  06h  F9h  0
    NP      0  0  0  0  0  07h  F8h  0
    NP      0  1  0  0  0  08h  F7h  0
    NP      0  0  0  0  0  09h  F6h  0
    NP      0  1  0  0  0  0Ah  F5h  0
    NP      0  0  0  0  0  0Bh  F4h  0
    NP      0  1  0  0  0  0Ch  F3h  0
    NP      0  0  0  0  0  0Dh  F2h  0
    NP      0  1  0  0  0  0Eh  F1h  0
    LP      A1  0  0  0  0  0Fh  F0h  0 //Loop to A1
    NP      0  1  0  0  0  00h  00h  0
    NP      0  0  0  0  0  00h  00h  0
    NP      0  1  0  0  0  00h  00h  0
    LP      A0  1  0  0  0  00h  00h  0 //Loop to A0
    NP      0  0  1  0  0  00h  00h  0
    NP      0  1  1  0  0  00h  00h  0
    NP      0  0  1  0  0  00h  00h  0
    NP      0  1  1  0  0  00h  00h  0
    NP      0  0  1  0  0  00h  00h  0
    NP      0  1  1  0  0  00h  00h  0
    NP      0  0  1  0  0  00h  00h  0
    JP      Start 1  1  0  0  00h  00h  0 //Jump to Start
;

```

There are 4 parts to form a DGV file contents, they are **INPUTS**, **INTERVAL** or **FREQUENCY**, **CLOCK_MODE**, **VOLTAGE**, **PATTERN**.

INPUTS: a key word to input the signals.

DG_CMD:-2,
DG_PARA:-1,

These 2 items must be reserved and the channel number is fixed, -2 and -1.

They are data generator instructions and parameters, the DG instructions are shown as following:

NP(No Operation)

LC(Set Loop Count) :parameter: $1 \sim 2^{23} - 1$ (count).

LP(Loop) / JP(Jump) :the parameter of JP & LP is a label or address.

WE(WaitEvent) :parameter 0: Keyboard Event, 1: EV0, 2:EV1, 3:EV2, 4:EV0 or EV1,

5: EV0 or EV2, 6: EV1 or EV2, 7: EV0 or EV1 or EV2, 8 = reverse the result of parameter = 0, 9 = reverse the result of parameter 1....

RP(Repeat) :parameter $1 \sim 2^{23} - 1$ (count).

Each signal is separated by “,” and signal name and channel number is separated by “:”.

Clk:0 : set the label name “Clk” and channel number is channel 0.

DataA[7..0]:15..8 : set the label name “DataA[7..0]” and channel number is channel 8~15,

it’s a data bus, 8..15, from LSB to MSB.

Set delay $x/8$ clock when type “#x”, $x = 0 \sim 7$, assuming that the working frequency = 125 MHz, it means that a clock cycle is 8 ns, $x = 5$, it will delay 5 ns.

DG_OE0:120, DG_OE1:121, ... ,DG_OE6:126 :

it also a reserved signal to set output enable or disable, 120 ~ 126 for DG 3000 series; 16 ~31 for TD 3000 series.

DG_OEx = 0, Output Enable ; DG_OEx = 1, Output Disable.

DG_OE0 include CH0~CH15 (DG 3000); CH0 (TD 3000),

DG_OE1 include CH16~CH31 (DG 3000); CH1 (TD 3000)

DG_OE2

INTERVAL

FREQUENCY: only select INTERVAL or FREQUENCY mode, the range of frequency is

100Hz~400MHz (DG 3000), 100Hz~200MHz(TD3116B/3216B),

100Hz~100MHz(TD3008E).

CLOCK_MODE: select internal clock or external clock to output the waveform.

Internal Clock → **CLOCK_MODE** Internal;

External Clock → **CLOCK_MODE** Clk-In or CKI;

VOLTAGE: there are 8 voltage values, each for the output voltage of 8 or 16 channels, 1st

voltage value is for CH0~CH7 /CH0~CH15 (TD 3000/DG 3000), 2nd voltage value for CH8~CH15/ CH16~CH31/ (TD 3000/DG 3000)...

3rd / 8th voltage value is the threshold of Event Pod (TD 3000/DG 3000).

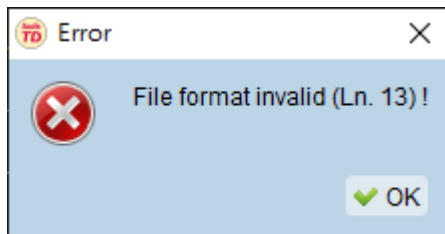
The range of voltage value is 0.8 ~ 5.0 (DG 3000 series); 0.8 ~ 4.5 (TD 3000 series).

The range of threshold value is -1.0 ~ 8.0 (DG 3000 series); -5.0 ~ 5.0 (TD 3000 series).

PATTERN: it's a waveform area; a row is a clock sample. ":Start" or ":A0" means a label,

they are jump(JP) points.

Note: The software provides a text vector file format check function. If the text vector file format is incorrect, then the software will display an error message and tell which line is incorrect.



```

INPUTS
DG_CMD:-2,
DG_PARA:-1,
SPICS:0,
SPICLK:1,
MOSI:2,
MISO:3,
TESTM:4,
TRIGGER:5,
CH-06:6,
CH-07:7;
FREQUENCY 10000000Hz;
CLOCK MOD Internal; // Invalid keyword
VOLTAGE
3.3,3.3,1.6,3.3,3.3,3.3,3.3,3.3;
PATTERN
NP      0      1      0      1      0      0      0      1      1
NP      0      1      0      1      0      0      0      1      1
NP      0      1      0      1      0      0      0      1      1
NP      0      0      0      1      0      0      0      1      1
NP      0      0      0      1      0      0      0      1      1
NP      0      0      1      0      0      0      0      1      1
NP      0      0      0      0      0      0      0      1      1

```