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# Chapter 1 Bus Decode

### **Basic operation**

### Add a Bus Decode

Connect Quick Settings	Der Free Run	Sample Rate 200MHz (5ns)	Memory 250Mb - 16CH	HT Threshold	Run I	() Repeat					Zoom .	Stack Phase I EXT DSO 0 ps					
nelDiv= 200 us		117.85 us	500us 216.71 w	353.65 us	471.42.03	519.27 ed	510ur 707.12 us	024.00 ud	5 101111	Latima	5.0 1.17 ms	0um 1.20 ma	1.41 ma	1.13 ma	1.84 ma	500us 1.76 ms	1.01 ma
H-00 A0	-XXXXXX																
H-01 A1																	
H-02 A2																	
H-03 AD														4			
2																	

#### Method 1:

Click the Quick Setting in the menu (number 1 in the figure above), and select the bus decode.

#### Method 2:

Click Add Bus Decode (number 2 int the figure above) in the Label menu or right-click the label field to show the dialog box.



#### Time/Div = 200 us 117.86 us 235.71 us e Label Name CH-00 Color CH-00 Hex Value Display Type Signal CH 0 MMC Group (Bus) ö Bus Decode MMC ¥ # HDMI-CEC \* HDQ HIDoverl2C 12C I2C(EEPROM) 12S 13C 180 IDE **IrDA** ITU656 JTAG LCD1602 LED\_CTRL LIN Line Decoding Line Encoding JV. Lissajous LPC LPT Label Channel Math MBus MDIO CH-00 Bus 111 34 MHL-CBUS CH-01 MICROWIRE MII / RMII MIPI DSI MIPI RFFE MIPI SPMI MMC

### Advance channel setting

- 1. Bus Name: Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
- 2. Color: Set the waveform color.
- 3. Display the waveforms with decode
- 4. Display the waveforms with its decode together.
- 5. Advance:



Set the decode parameters or press  $\mathbf{OK}$  to use default settings. There are

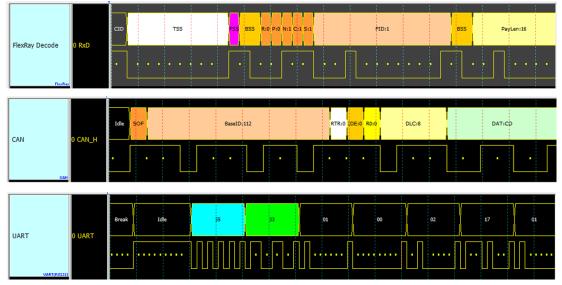
"Channel"/"Parameter', "Color", "Range" settings	S
×	
Parameters	
Color	
• • • • • • • • • • • • • • • • • • •	
Range	
Decode Range	
From To	
Buffer Head 💌 Buffer Tail 💌	
Obefault ✓OK ★Cancel	



### **Specially Bus Decode**

The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode...), image, analog waveform (ADC decode) etc.

UART/CAN/FlexRay..bus decodes (released since 2009/9, LA Viewer Ver2.0): The data is displayed according to bit points in order to calculate the bit number •



#### S/PDIF analysis (released since 2010/11, LA Viewer Ver2.5):

Display the data in sound waveform.

6572 4496 5706 5766 11 Juliu Juliu 00:00:00:39 32 00:00:00:78.64 00:	
	×
Block	Data Bits
192 (32 ~ 192) frames	16 💌
Bit Order	Parity mode
Aux Data LSB first 💌	Even parity 👻
Audio Data LSB first 👻	✓ Playback
	4496 5706 5766 00:00:00:39:32:00:00:00:78:54:00: Block 192 (32 ~ 192) frames Bit Order Aux Data LSB first •



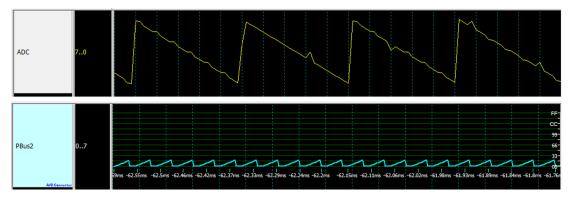
### I<sup>2</sup>S analysis (released since 2011/9, LA Viewer Ver2.6.3):

Display the data in sound waveform •

▶ 12S	A2:A0	Max. 30197 Min: 28314 Min: 26065 Min: 23668 Min: 23668	
Channel	I		Sound reduction
Ì	Clock Channel (SCK) Word Select Channel (WS) Data Channel (SD) Data Bits	A0	<ul> <li>Display the audio waveform</li> <li>Save as WAV file</li> <li>Playback</li> <li>Align common sample rate</li> </ul>

#### ADC bus decode:

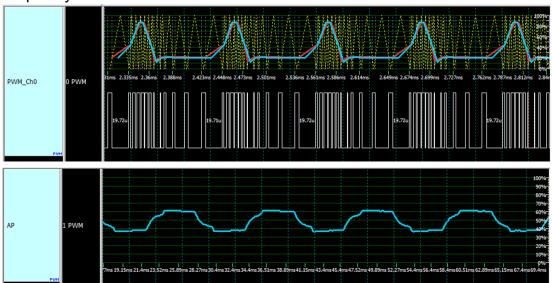
Display the input data in graph  $\,{}^\circ$ 





#### PWM analysis (released since 2012/8, LA Viewer Ver2.7.3):

Restore and display the data in the waveform window as percentile or frequency  $\ensuremath{\,^\circ}$ 





## **Bus Decode Settings Introduction**

Please note: All are prefixed with 'Ch' except BusFinder or LA in the channel, which are prefixed with 'A'.



### 1-Wire

Developed by Dallas Semiconductor, the 1-Wire protocol defines several signal types such as Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, and Read 0, and combines these signal types into a command sequence. The transmission mode is LSB (Least-significant bit) to MSB (Most-significant bit), and the transmission speed is divided into Overdrive speed and Standard speed.

#### Settings

🚾 1-Wire Settings		×
Channel	Timing Setting	
Channel A0	Slot Time Slot Interval	7 us
Bit Order	min	2 us
● Isb First ○ msb First	Max	6us
Data Column Byte Amount 8	ResetTime	
Color	min	48 us
	Max	80 us
	Presence Time	
<b>–</b>	min	8 us
Reset Pulse	Max	24 us
Presence Pulse	Sampling time 5 us	I <del>€→</del> I
Range		
Decode Range		
From To Buffer Head	Default	✓OK XCancel

Channel: Setting the Data Channel Source

Bit Order: Set whether the analyzed data is LSB first or MSB first.

**Data Byte Column Amount:** Set how many bytes of data are displayed in a row of the Data field in the Report area; user can select 8, 16, or 32.

Timing Setting: all unit is us.



1. **Slot Time:** Setting the duration of the slot

#### 2. Slot Interval:

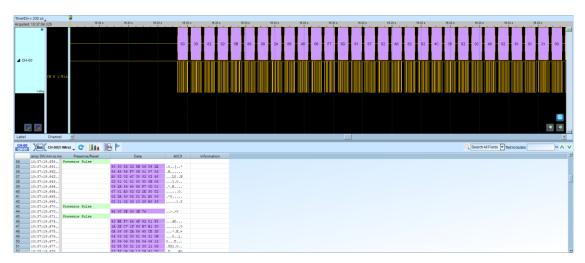
- I. Min: Set the minimum length of time between each slot.
- II. Max: Set the maximum length of time between each slot.

#### 3. Reset Time:

- I. **Min:** Set the minimum length of time for the Reset pulse waveform to pull low.
- II. **Max:** Set the maximum length of time for the Reset pulse waveform to pull low.

#### 4. Presence Time:

- I. **Min:** Set the minimum length of time for the Presence pulse waveform to pull low.
- **II. Max:** Set the maximum length of time for the Presence pulse waveform to pull low.
- 5. **Sampling Time:** Set how long after the start of a slot the Master will latch the data.





### 10BASE-T1S

10Base-T1S uses Differential Manchester Encoding (DME). DME encodes data based on whether there is a transition within the clock period, indicating the logical state of the signal. If there is no transition within the clock period, the data state is logical 0. If transitions (either positive or negative) occur within the clock period, the data state is logical 1.

10BASE-T1S operates in a half-duplex bus configuration with a maximum length of 25 meters. It supports multipoint connections with two to eight nodes. The "S" in the standard name denotes short-range implementation. The intended use of 10BASE-T1S is to replace existing bus architectures that often result in "communication islands," such as CAN, CAN FD, LIN, and RS-485.

#### Settings:

10BASE-T1S Settings	×
Channel	Color
Data A0	
Option	•
Show Sync Code Hide BEACON FCS in Byte Order	SYNC_COMMIT
Display 5B Code Show MAC fo Each Row	SSD MAC Data 🗸
✓ Show MAC Data	BEACON
Turned un Date	ESDHB
Transport Layer Data 👻	ESDBRS
Data Filter: 20 bytes	ESDJAB
Report Data: 8 Byte 💌	
Range	
Decode Range	
From To	
Buffer Head   Buffer Tail	
Default	✓OK XCancel

Show Sync Code: Show Commit, SSD in report; enabled when checked.Hide BEACON: Hide Beacon data is not shown; enabled when checked.FCS in Byte order: Present FCS in report in byte order; enabled when checked.

Display 5B Code: Show special code value



#### Show MAC Data: Show MAC Packet.

In IPv4(0800h), there will be 20bytes header. The Data column is able to show

Transport Layer Data only or including the header.

Transport Layer Data	-
Transport Layer Data	
Transport Layer Data & Header	

#### Transport Layer Data:

Total Length	Protocol	IP Source	IP Destination	Data
0020h	UDP(11h)	192.168.0.20	192.168.0.255	75 30 75 30 00 0C 2C 93
				64 00 02 7E 00 00 00 00
				00 00 00 00 00 00 00 00
				00 00

#### Transport Layer Data & Header:

Total Length	Protocol	IP Source	IP Destination	Data
0020h	UDP(11h)	192.168.0.20	192.168.0.255	45 00 00 20 01 7B 00 00
				FF 11 37 EE CO A8 00 14
				CO A8 00 FF 75 30 75 30
				00 0C 2C 95 64 00 02 7C
				00 00 00 00 00 00 00 00
				00 00 00 00 00 00

#### **Results:**

ne/Div=5 us		<del>4</del>										
quired: 17:43:11.900		239.12 ms	239.12 ms	239.13 ms	239.13 ms	239.14 ms	239.14 ms	239.16 ms	239.15 ms 239.16 ms	239.16 ms	239.17 ms	239.17 ms
•		Pres	mble SF Dest. Addr.	Src. Addr.	0800 45 00 0	0 20 01 7D 00 00	FF 11 37 3C CO A8 0	0 14 00 A8 00 FF 75 3	0 75 36 00 C 2C 93 64 00 02 7E 00	00 00 00 00 00 00	00 00 00 60 00 00 00	FCS
I BUS_10Base- 10BASE-T1 N_BASE-T1	13-0											
ibel Channel	Value	۲.										
H-00 Vouv out 400-												Q Search
HIOI DUS BUS_10Ba	ase-T1S(10BASE-	T1S) 🖵 🧲 📗 🛛	8 r									Coearcin
:amp (hh:mm:ss.ms.	Special Code	MAC Destination	MAC Source	EtherType	Total Length	Protocol	IP Source	IP Destination	Data	FCS	Infor	mation
:amp (hh:mm:ss.ms. 17:43:13.105	Special Code	MAC Destination	MAC Source							FCS		mation
tamp (hh:mm:ss.ms. 17:43:13.105. 17:43:13.185. D	Special Code ESD_OK DATA			EtherType	Total Length	Protocol	IP Source	IP Destination	45 00 00 20 01 7D 00 00	FCS	Infor IP, Internet P	mation
amp (hh:mm:ss.ms. 17:43:13.105 E 17:43:13.185 D 17:43:13.185 D	Special Code SSD_OK DATA DATA	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 A8 00 14	FCS		mation
amp (hh:mm:ss.ms 17:43:13.105. 17:43:13.185. 17:43:145. 17:43:15. 17:45. 17:45. 17:45. 17:45. 17:45. 17:45. 17:45. 17:4	Special Code SSD OK DATA DATA DATA DATA	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 A8 00 14 C0 A8 00 FF 75 30 75 30	FCS		mation
amp (hhummss.ms. 17:43:13.105 17:43:13.185 17:43:13 17:43:14 17:43:13.	Special Code ESD OK DATA DATA DATA DATA DATA	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 A8 00 14 C0 A8 00 FF 75 30 75 30 00 0C 2C 93 64 00 02 7E	FCS		mation
samp (hh:mm:ss.ms           17:43:13.105.         I	Special Code ESD OK DATA DATA DATA DATA DATA	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 AB 00 14 C0 AB 00 FF 75 30 75 30 00 CC 2C 93 64 00 22 7E 00 00 00 00 00 00 00 00 00	FCS 774E0ABC		mation
samp (hh:mm:ss.ms           17:43:13.105.         E           17:43:13.185.         D           17:43:13.185.         D           17:43:13.185.         D           17:43:13.185.         D           17:43:13.185.         D	Special Code ESD OK DATA DATA DATA DATA DATA DATA	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 A8 00 14 C0 A8 00 FF 75 30 75 30 00 0C 2C 93 64 00 02 7E			mation
ismp (hhmmss.ms.           17:43:13.105           17:43:13.105           17:43:13.105           17:43:13.105           17:43:13.105           17:43:13.105           17:43:13.105           17:43:13.105           17:43:13.105	Special Code ESD OK DATA DATA DATA DATA DATA DATA DATA ESD HB	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 AB 00 14 C0 AB 00 FF 75 30 75 30 00 CC 2C 93 64 00 22 7E 00 00 00 00 00 00 00 00 00			mation
amp (hh:mm:s.ms. 17:43:13.105. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D	Special Code SSD OK DATA DATA DATA DATA DATA DATA SSD HB ESD OK	MAC Destination	MAC Source						45 00 00 20 01 7D 00 00 FF 11 37 EC C0 AB 00 14 C0 AB 00 FF 75 30 75 30 00 CC 2C 93 64 00 22 7E 00 00 00 00 00 00 00 00 00			mation
amp (hh:mn:s.ms. 17:43:13.105. E 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. E 17:43:13.185. E 17:43:13.185. E 17:43:13.18. E	Special Code ESD OK DATA DATA DATA DATA DATA DATA ESD HB ESD HB ESD OK	MAC Destination	MAC Source	0800	0020h	UDP(11h)	192.168.0.20	192.168.0.255	45         00         00         20         01         7D         00         00         F         11         37         EC         CO         A8         00         I4           C0         A8         00         FF         75         30         75         30           00         0C         27         54         64         00         27         E           00         0C         20         00		IP, Internet P	mation
amp (hhemmiss.ms. 17:43:13.105. B 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D	Special Code ESD OK DATA DATA DATA DATA DATA DATA ESD HB ESD HB ESD OK DATA DATA DATA DATA	MAC Destination	MAC Source	0800	0020h	UDP(11h)	192.168.0.20	192.168.0.255	45 00 00 20 01 7D 00 00 FF 11 37 EC C0 A8 00 14 C0 A8 00 FF 75 30 75 30 00 0C 2C 53 64 00 02 7E 00 00 00 00 00 00 00 00 00 00 00 00 00		IP, Internet P	mation
amp (hh:mm:s.ms. 17:43:13.105. E 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. D 17:43:13.185. E 17:43:13.185. E 17:43:13.185. E 17:43:13.185. E 17:43:13.317. D	Special Code ESD OK DATA DATA DATA DATA DATA DATA SSD HB ESD OK ESD OK DATA DATA	MAC Destination	MAC Source	0800	0020h	UDP(11h)	192.168.0.20	192.168.0.255	45 00 00 20 01 7D 00 00 FF 11 37 EC C0 A8 00 14 C0 A8 00 FF 75 30 75 30 00 0C 2C 93 64 00 02 7E 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00		IP, Internet P	mation
amp (hkmm:ss.m. 17:43:13.105 17:43:13.105 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.185 17:43:13.317 17:43:13.317 17:43:13.317	Special Code SSD OK DATA DATA DATA DATA DATA DATA SSD HB SSD HB SSD OK DATA DATA DATA DATA DATA	MAC Destination	MAC Source	0800	0020h	UDP(11h)	192.168.0.20	192.168.0.255	45         00         00         01         7D         00         00           FF         11         37         EC         0A         00         14           C0         A0         0F         75         30         50         00 <td></td> <td>IP, Internet P</td> <td>mation</td>		IP, Internet P	mation



 $\times$ 

### 3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

aramete			Color
(	Channel		
	CS A0	*	OPERATION
=	WR A1		ADDRESS
	✔ RD A3	<b>*</b>	COMMAND
	DATA A2		DATA
	Application		START
	LED Drive IC		Latch
	LCD Drive IC		Chip Select Edge
			Active High      Active Lo
	HT 1620x	•	
	HT93LC46	-	Data Edge
	x8	-	Rising      Falling
Range			
<mark>飛</mark> ,	Decode Range		
From	То		

**Channel:** Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

**EEPROM:** Select EEPROM application.

Active High: Select Active High.

Active Low: Select low chip select (CS).

**Rising:** Select Rising Data Edge.



Falling: Select Falling Data Edge.

ne/Div= 50 us	19 .		•				2.364ms				
	<u></u>	-10 us D	n 50 us 100 us	150 ur 2	200 ur	250 um 300 um 31	10 us 400 us	460 ur 500	ur 560 ur	500 ur 650 ur	700 ur 1150 ur
	Θ		¥ A:00 3:03:00:03:00:33:73:00:03:F3:E3:F	0.10.10.10.000	0.10.10.10	1200002020000200000000	200.020200.0200.0	2020002000020200	0200-020200-020		200.0200.0200
	CS-A2										
3-Wire	CS-A2										
3-Wire											
	WR-A1										
									To a tur ur u		needet di tarean tare
3-W	DATA-A0		61.53 m 24.08 m 18.7.	3 u 18.73 u 26.75 u	18.73 1						
н, н	é	Live									, <b>e</b> _e
bel	Channel										
	-										
YBu	us 3.Wire(3.)	Mire) 📿 🚺 🖬 🖂 🏱								Q Search All Fields Text	tincludes Includes
		Mire) 🗸 😋 🛄 💼 🏲		Address	Data					Q Search All Fields Text	t includes 🛛 🔍 🖊
1.3	Timestamp 335us	Mire) C Operation S (WRITE)	Command	Address 0	Data					Q Search All Fields Text	t includes 🔤 🖬 🖊
1.3	Timestamp 335us .115us	Operation		00 0	Data					C Search All Fields Text	tincludes 📃 🕬 🖊
1.3 36. 46.	Timestamp 335us .115us .015us	Operation		00 0 01 0 02 0	Data					Q Search All Fields Text	tincludes 🛛 🗠 🖊
1.3 36. 46. 57.	Timestamp 335us .115us .015us .52us	Operation		00 0 01 0 02 0 03 0	Data					Q Search All Fields Text	tincludesCx 🖊
1.3 36. 46. 57. 68.	Timestamp 335us .115us .015us	Operation		00 0 01 0 02 0 03 0 04 3 05 7	Data					🔍 Search All Fields 🛡 Text	tincludes 🔤 🛛 🖉
1.3 36. 46. 57. 68. 78. 89.	Timestamp 335us .115us .615us .52us .225us .925us .63us	Operation		00 0 01 0 02 0 03 0 04 3 05 7 06 0	Data					🔍 (Search All Fields 💌 Text	tincludes 🔤 🖉
1.3 36. 46. 57. 68. 78. 89. 100	Timestamp 335us .115us .615us .52us .225us .925us .63us 0.33us	Operation		00 0 01 0 02 0 03 0 04 3 05 7 06 0 07 0	Data					C Search All Fields Taut	tincludes k /
1.3 36. 46. 57. 68. 78. 89. 100 111	Timestamp 335us .115us .015us .225us .225us .63us 0.33us 1.035us	Operation		00 0 01 0 02 0 03 0 04 3 05 7 06 0 07 0 08 F	Data					C Bearch All Fields Thed	tincludes 🛛 🕅 🖉
1.3 36. 46. 57. 68. 78. 89. 100 111 121	Timestamp 335us .115us .015us .52us .225us .63us .63us 0.33us 1.035us 1.74us	Operation		00 0 01 0 03 0 04 3 05 7 06 0 07 0 08 F 09 B	Data					C Search All Fields 🖵 Tax	tincludes 🔤 🕬 🖊
1.3 36. 46. 57. 68. 78. 89. 100 111 121 132	Timestamp 335us .115us .015us .225us .225us .63us 0.33us 1.035us	Operation		00 0 01 0 02 0 03 0 04 3 05 7 06 0 07 0 08 F	Data					C. Search All Fields 🖵 Tax	tincludes or A
1.3 36. 46. 57. 68. 78. 100 111 121 132 143 153	Timestamp 335us .115us .615us .52us .225us .63us 0.33us 1.050us 1.74us 2.44us 3.145us	Operation		00 0 01 0 02 0 03 0 04 3 06 0 07 0 06 7 06 7 09 B 03 F 09 B 04 F 09 B	Data					C. Bearch All Fields 🗩 Tax	tincludes 👘 🖍
1.3 36. 46. 57. 68. 78. 89. 100 111 121 132 143 153 164	Timestamp 335us .115us .015us .225us .225us .43us 0.33us 1.035us 1.74us 2.44us 3.145us 3.845us 4.545us	Operation		00         0           01         0           02         0           03         0           04         3           05         7           06         0           07         0           08         B           0C         F           0B         B           0C         F	Data					C Search AI Fields P Trad	lincludes 🔤 🗠 /
1.3 36. 46, 57. 68. 70. 85. 100 111 121 132 133 143 153 164 175	Timestamp 335us .115us .615us .635us .225us .63us .63us 1.035us 1.74us 2.44us 3.145us 3.145us 3.145us 3.245us 3.245us	Operation		00         0           01         0           02         0           03         0           04         3           05         7           06         0           07         0           08         8           00         2           00         7           00         7           00         7           00         8           00         7           00         3           00         3           02         0	Data					C Search All Fails P Ted	si includes
1,3 36, 46, 57, 68, 1000 1111 122 133 153 154 175 164 175	Timestamp 335us .115us .615us .625us .225us .925us .63us 0.33us 1.035us 1.74us 2.44us 3.145us 3.145us 3.145us 5.25us 5.25us	Operation		00         0           01         0           02         0           03         0           04         3           05         7           06         0           07         0           08         8           000         3           000         3           000         3           02         02           03         0           04         3           05         0	Data					C Search Al Pasts P Ted	lincludes and a
1.3 36. 46. 57. 68. 100 100 101 111 122 132 143 153 155 164 175 185	Timestamp 335us .115us .615us .62us .225us .62us .63us 1.03us 1.035us 1.74us 2.44us 3.145us 3.845us 4.545us 5.25us 5.95us 6.6us	Operation		00 01 0 01 0 02 0 03 0 04 3 05 7 06 0 07 0 06 7 0 08 F 08 F 008 F 008 7 008 0 00 3 002 0 00 3 002 0 00 3 00 3 00 3 00 3 00 2 00 0 00 3 00 0 00 3 00 0 00 3 00 0 00 0 0	Data					C Search AF Pasts P Ted	si includes
1,3 36. 46, 57,68. 85, 100 111 122 133 153 153 154 175 196 207	Timestamp 335us .115us .615us .625us .225us .925us .63us 0.33us 1.035us 1.74us 2.44us 3.145us 3.145us 3.145us 5.25us 5.25us	Operation		00         0           01         0           02         0           03         0           04         3           05         7           06         0           07         0           08         8           000         3           000         3           000         3           02         02           03         0           04         3           05         0	Data					C Search AF Fails P Ted	includes and a



### 7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit		Â	В	С	D	Е	F	G
0	F G B E D DF	ON	ON	ON	ON	ON	ON	OFF
1	F G B F C D DP	OFF	ON	ON	OFF	OFF	OFF	OFF
2		ON	ON	OFF	ON	ON	OFF	ON
3		ON	ON	ON	ON	OFF	OFF	ON
4		OFF	ON	ON	OFF	OFF	ON	ON
5	F G B F C D DP	ON	OFF	ON	ON	OFF	ON	ON
6	F G B E C D DP	ON	OFF	ON	ON	ON	ON	ON
7		ON	ON	ON	OFF	OFF	OFF	OFF
8	F G B C DP	ON						
9		ON	ON	ON	ON	OFF	ON	ON



#### Settings

苎 7-Segment Settings		×
Channel		
<b>1</b>	A	
A 🗛 🌲 E	A4 D F B	
В [А1 🗘 F	A5 🗘 G B	
C A2 🗘 G	A6 🗘 E C	
D A3		
O Common anode 💿	Common cathode	
Color R:	ange	
	Decode Range From To	
Data 🗾 🔻	Buffer Head 👻 Buffer Tail 👻	
	Obefault ✓OK ¥Cancel	

Channel: Show the selected channel (CH 0).

**DP**: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.

	ult											
ne/Div=1 us		35.00 ur					09.376ms					
		-25.96 ur	-24.96 us	-22.96 ur -22	2.96 us	-21.98 us -20.98 us -19.	98 ur -10.98 ur -17.9	us -18.98	ur -15.96 ur -14.96 ur -	13.96 ur	-12.96 us -11.96 us	-10.96 ur
	•	E. E.	P	8 6		9 0 A 1	2 3 4	5 7	BCEE	F		θ.
	A-A0		1.6 w		2.00	a 000 a 000 a 000 a 000 a 900 a	100 n 200 n 200 n 900 m	a 005 a 005 a 005	2.1 m 200 a		3.2 m	500 au
	B-A1	200 %		400 ns	1.1 18	a 005 a 005 a 005 a 005 a 005 a 005		900 az 300 a	1.5 ts 000 n		4.7 w	400 x
	C-A2	200 x				a 004a 004a 004a 004a 004a 004a 004	000 n 000 n 000 n 000	300 a 300 a 300 a 30	a 000 a 000 a 000 a 000 a 000 a			
PBus1	D-A3	a 000 a 300 a 300 a	2.2 m	600 as	900 ns	300 a) 00 a) 00 a 1.5 w		300 n 900 ns	a 000 a 000 a 000 a 000 a 000 a 000 a		4.1 us	
	8-44	300 n 300 n 300 n 400 ns	700 ===================================	.1 w 600 m	15	z 200 x 200 x 200 x 900 x	300 n 27 v			700 as	3 115	
	0-04					* 00 a co a co a co a			200 a	200 18		
	F-AS	300 n 400 ns				a 006 a 900 a 900 a 900 a		300 a 900 as	300 n 300 n 300 n 900 ns 300 n 400 ns			
	G-A6	300 n300 n300 n 400 ns				a 000 a 000 a 000 a 000 a 000 a 000	005 n 005 n 005 n 005 n 005 n 005	300 n 900 ns	300 n 900 ns 300 n 300 n 400 ns			
	DP-A7	200 n 200 n 200 n 400 nz	700 m					142 m				
7-Sept	trent .											
15, IV		OLive										.•
abel	Channel											
H-00 Vo	v		1 1							0	Search All Fields Text includer	
		iegment) 🗸 😋 🛄 👔									search All Fields 🕑 lext includes	
	Timestamp	A B	С	D	E	F G	DP Value					
		° °	1			1 0 1	C. E.					
7815 -2	27.345					i i	E.					
7815 -2 7816 -2	26.7us	1 0	0	1								
7815 -2 7816 -2 7817 -2		1 0 1 0	0	0		1 1 1	F.					
7815 -2 7816 -2 7817 -2 7818 -2	26.7us 26.1us	1 0 1 0 1 1	0	1 0 1		1 1 1 1 1 0	F. 8					
7815 -2 7816 -2 7817 -2 7818 -2 7818 -2 7819 -2 7820 -2	26.7us 26.1us 25.4us	0 1 1 0 1 0 1 1 1 0	0 0 1 1	1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1 1 1 1 1 0 1 1 0	F. 8 6					
7815 -2 7816 -2 7817 -2 7818 -2 7818 -2 7819 -2 7820 -2	26.7us 26.1us 25.4us 23.6us	0 1 1 0 1 0 1 1 1 0 1 1 1 1	0 0 1 1 1	1		1 1 1 1 1 0 1 1 0 1 1 0	F. 8 6 9					
7815 -2 7816 -2 7817 -2 7818 -2 7819 -2 7820 -2 7821 -2 7822 -2	26.7us 26.1us 25.4us 23.6us 23.2us	0 1 1 0 1 1 1 1 1 0 1 1 1 1	0 1 1 1 1	1 0 1 1 1 1		1 1 1 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0	F. 8 6 5 8					
1815         -2           1816         -2           1818         -2           1818         -2           1819         -2           1820         -2           1821         -2           1822         -2           1823         -2	26.7us 26.1us 25.4us 23.6us 23.2us 22.1us	0 1 1 0 1 1 1 1 1 0 1 1 1 1 1 1	0 0 1 1 1 1 1 1	1		1 1 1 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0	F. 8 6 9 8 8 8					
1815         -2           1816         -2           1818         -2           1818         -2           1819         -2           1820         -3           1821         -2           1822         -2           1823         -2           1824         -2	26.7us 26.1us 25.4us 23.6us 23.2us 23.2us 22.1us 21.5us 20.9us 20.9us	0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1	1 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0		1 1 1 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 0	F. 8 6 9 8 8 8 1					
15         -2           1816         -2           1816         -2           1817         -2           1818         -2           1819         -2           1821         -2           1822         -2           1823         -2           1824         -2           1825         -1	26.7us 26.1us 25.4us 23.6us 23.2us 22.1us 21.5us 20.9us 20.3us 19.7us	0         1           1         0           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1	0 0 1 1 1 1 1 1 1 1 0	1 0 1 1 1 1 1 0 0 1 1 1 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 1 0 1		1 1 1 1 1 1 1 0 1 1 1 0 1 1 1 0 1 1 0 1 1 0 1 0 0 0 0 0 0 0 1 0	F. 0 6 9 0 8 1 2					
1815         -2           1816         -2           1818         -2           1818         -2           1819         -2           1821         -2           1822         -2           1823         -2           1823         -2           1824         -2           1825         -1           1826         -1	26.7us 26.1us 25.4us 23.4us 23.2us 22.1us 21.5us 20.9us 20.9us 19.7us 19.7us 19.1us	0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 0 0 1	1 0 1 1 1 0 0 0 1 1		1         1         1           1         1         0           1         1         0           1         1         0           1         1         0           0         0         0           0         1         0           0         1         0	F. 8 6 9 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8					
1815         -2           1816         -2           1817         -2           1818         -2           1819         -2           1821         -2           1822         -2           1823         -2           1823         -2           1825         -1           1826         -1           1827         -1	26.7us 26.1us 25.4us 23.4us 23.2us 23.2us 23.2us 23.2us 23.5us 20.5us 20.5us 19.7us 19.1us 18.5us	0         1           1         0           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           0         1           1         1           0         1	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 0 0 1 1 0 0 0 0 1 1 0 0 0 1 0		1 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 0 0 0 0 1 0 0 1 0 1 0	F. 8 8 8 2 1 2 3 4					
15         -2           7816         -2           7817         -2           7818         -2           7819         -2           7821         -2           7822         -2           7823         -2           7823         -2           7825         -1           7826         -1           7826         -1	26.7us 26.1us 25.4us 23.6us 23.2us 21.5us 20.5us 20.5us 20.3us 19.7us 19.1us 19.1us 19.1us	0         1           1         0           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         0	0 0 1 1 1 1 1 1 1 0 0 1 1 1 1	1 0 1 1 1 0 0 0 1 1 0 1 0 1		1         1         1           1         1         0           1         1         0           1         1         0           0         0         0           0         1         0           0         1         0           1         1         0           1         1         0           1         1         0           1         1         0	F. 8 6 9 8 8 1 1 2 3 4 5					
7815         -2           7816         -2           7817         -2           7818         -2           7820         -2           7821         -2           7822         -2           7823         -2           7824         -2           7825         -1           7826         -1           7827         -1           7828         -1           7828         -1           7828         -1           7828         -1	26.7us 26.1us 25.4us 23.6us 23.6us 22.1us 22.1us 20.9us	0 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 0 1 1 1 1 0 0 1 1 1 1 0 1 0 1 1 0		1         1         1           1         1         0           1         1         0           1         1         0           1         1         0           0         1         0           0         1         0           1         1         0           0         1         0           1         1         0           1         1         0           1         1         0           0         0         0         0	Γ. 8 6 9 8 λ 1 2 3 4 4 5 7					
7815         -2           7816         -2           7817         -2           7818         -2           7819         -2           7820         -2           7821         -2           7823         -2           7823         -2           7825         -1           7826         -1           7827         -2           7828         -1           7829         -2           7828         -1           7829         -1           7829         -1           7830         -1	26.7us 26.1us 25.4us 23.4us 23.4us 23.1us 22.1us 21.5us 20.5us 20.5us 19.7us 19.7us 19.1us 19.1us 19.1us 19.1us 10.5us 17.3us 16.7us	0         1           1         0           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           0         1           0         0	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 0 0 1 1 1 1 0 0 1		1         1         0           1         0         0           1         1         0           1         1         0           1         1         0           0         0         0           0         1         0           1         1         0           1         1         0           1         1         0           1         1         0           1         1         0           1         1         0	r. 8 6 8 8 8 1 2 3 4 5 5 7 7 8					
17815         -3           17816         -2           17816         -2           17818         -2           17819         -3           17820         -3           17821         -2           17822         -3           17823         -2           17825         -1           17826         -1           17826         -1           17827         -1           17828         -1           17829         -1           17830         -1	26.7us 26.1us 25.4us 23.4us 23.4us 22.1us 21.5us	0         1           1         0           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         1           1         2	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 0 1 1 1 1 1 0 0 1 1 1 1 1		1         1         0           1         0         0           1         1         0           1         1         0           1         1         0           0         1         0           0         1         0           0         1         0           1         1         0           1         1         0           1         0         0           1         0         0	7. 8 6 8 8 8 8 8 2 3 4 4 5 7 7 8 6 7 8 6 7 8 7 8 7 8 7 8 7 8 7 8 7					
7815         -2           7816         -2           7817         -2           7818         -2           7829         -2           7820         -2           7822         -2           7823         -2           7824         -2           7825         -1           7826         -1           7827         -1           7828         -1           7829         -1           7829         -1           7830         -1           7831         -1	26.7us 26.1us 25.4us 23.4us 23.4us 23.1us 22.1us 21.5us 20.5us 20.5us 19.7us 19.7us 19.1us 19.1us 19.1us 19.1us 10.5us 17.3us 16.7us	Image: Constraint of the second sec	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 1 0 1 0 0 1 1 0 1 1 0 1 1 1 1 1 1		1         1         0           1         0         1         0           1         1         0         0           1         1         0         0           1         1         0         0           1         1         0         0           0         1         1         0           1         1         0         0           0         1         0         0           1         1         0         0           1         1         0         0           0         1         0         0           1         0         0         0           1         0         0         0	T. 8 6 8 8 8 8 8 8 8 4 5 7 7 8 6 5 7 7 8 7 7 8 7 7 8 7 7 8 7 7 7 8 7					



### 8b10b Decoding

8b/10b encoding is a coding technique commonly used in high-speed digital communications to convert every 8 bits of data into a 10 bits format. It was first invented by IBM in the 1980s to improve the reliability and stability of data transmission.

#### Setting

📇 8b10b Decode Settings				×
Settings			Color	
Channel				
Data Channel	AO	*	K Code 💌	
Data Rate		Option	D Code	
Auto     Manual 400	Mbps	Invert Value	Range	
Sync Symbol			Decode Range	
✓ K.28.0 ✓ K.28.3	✔ K.28.6	✓ K.27.7	From To	
▼ K.28.1 ▼ K.28.4	✔ K.28.7	✓ K.29.7		
✓ K.28.2 ✓ K.28.5	▼ K.23.7	▼ K.30.7	Buffer Head 🔹 Buffer Tail 💌	
			Default OK Cancel	5

Data Channel: Set the signal on the DUT to the channel number of the logic

analyzer.

(LVDS signals need to be converted into single-ended signals or use LVDS

probes)

Data Rate: User can set the data rate manually, or choose the 'Auto', let

software calculate the data rate automatically.

**Option:** 

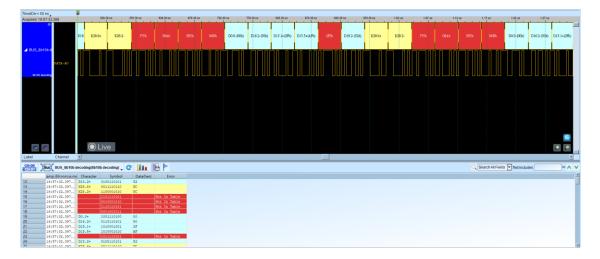
Invert Value: Invert the waveform.

Little Endian: The data would be sorted follow Little Endian when



checked.

**Sync Symbol:** Choose which k-code for syncing.





### A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

#### Settings

Channel Draw ( Curve: Time(X) - Data(Y) )
Diaw (Cuive, mile(x) - Data(1))
Color       Data Channel       Color       Output         Output         Color         Output         Output <t< th=""></t<>
Data Width 8 Bit  Channel Start From: A2
CLK Channel CH 0 CK CH 1 CH 1 CH 1 CH 1 CH 1 Use the Maximum and Minimum as the bound of Y-axis InsertY axis bound
Data Settings Bound Settings
MSB First
Mode O Signed O Unsigned Top (Decimal) 255
Chip Select Edge     Active High     Active Low       Data Edge     Rising     Falling
Color Range
DATA Decode Range From To
Buffer Head     ▼     Buffer Tail       ODefault     ✓OK     ¥Cancel

Data Channel Start From: ADC data channel start from

**CLK Channel:** CLK IN channel of ADC, enable CLK channel and Data Edge option when checked.

**CS(OE) Channel:** Chip Select channel of ADC, enable CS channel and Chip Select Edge option when checked.

**Data Width:** ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted



Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

**Curve: Time(X)-Data(Y)** Show the diagram in form of time as X axis; data as Y axis.

Ramp/Step Function: Select Ramp/Step curve, Ramp Function defaulted

Color: Select the curve color

#### Bound Value Range:

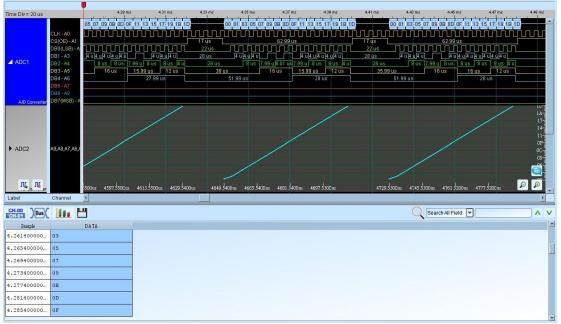
**Default:** The maximum value that can be represented using the data width is the upper bound.

**Use the maximum and minimum as the bound of Y axis:** Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis.

**Insert Y axis bound:** Set the maximum and minimum bounds of Y axis.

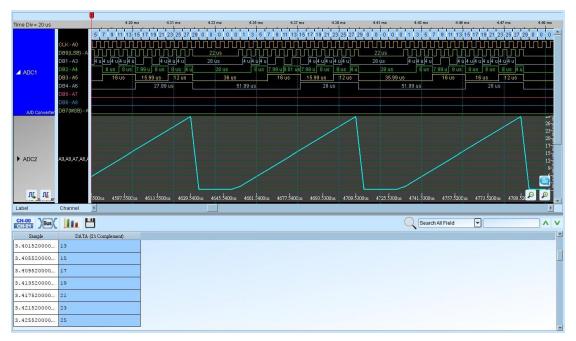
#### Result

Select 8-bit data, CLK/CS channels:





#### Select 8-bit data, CLK:





### Accelerometer

Accelerometer (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

#### Settings

🗯 AccMet	ter Settings				×
Parameter	Settings				
Channe	ls Settings		Edge Se	lect	
CS	AO	-	CS	Activate Low	•
CLK SDI SDO	A1 A2 A3		SDI SDO	Rising Rising	• •
Model	III-Scale	AIS326D0	2	• • G	
Delay So PI		Data (Y) de		Y	z )
Color					
R / W Address	3	•	M / S Data		•
Range	)ecode Range Head		To Buffer T	ail	-
Duiler	leau	ODefa			×Cancel

#### **Channel Setting:**

**CS:** Chip Select, must specified the active state of the CS pin.

CLK: Clock

**SDI:** Data Input Pin, must specified the data sampling edge.



**SDO:** Data Output Pin, must specified the data sampling edge.

#### Edge Setting:

**CS:** Set the trigger edge of Chip Select to High or Low.

**SDI:** Set the trigger edge of SDI to Rising or Falling.

**SDO:** Set the trigger edge of SDO to Rising or Falling.

Model: The IC model of the target accelerometer.

Initial Full-Scale: The default Full-Scale setting.

#### Display Setting, Enable when checked:

Plot: Enable/Disable to display the waveform in Time-Value curve.

Advanced Decode: Enable/Disable the address, value convert function.

**Calculate Average:** Enable/disable the average statistic function, the statistic range is ±255 data.

#### Result

Standard decoder result

ime/Div=	: 20 us _	2																			
			-8223360 s	9223350 s	-9223359 s	-42	20059 s	-0220090	5	-8223060 s	-9223	1360 s -0	223350 s -9223359 s	-0	220059 s	-0223350 s	4223360 s	4223350 s	-9223398 s	-0223359 s	-9223359 s
	0						1		· · ·					<b></b>		- <u></u>		-			
						&6ds 27		OF		00		00	00		F4		00 JD				
					11									_		1					
	A18 C3-	A18										214									
						-							1000000	100011107							
4 30_IN	att Als CLR	- 61				16.5 m				17.5 w			17.5 m				17.5 uz				
														шш							
																		Г			
	A16 SDI	-A1				19 m															
	417.750	- 4.1																			
	Acchieve																				
		$\sim$																			
л,			Live																		<u>ب</u> ا فر
ibel	Channe	•																			
H-00	V-V		: 🂵 📑	<b>b</b>																lds 🔻 Text includes	EX .
CH-00	ABUS JD_INIT	(AccMeter)	. 📶 🔜	r															Consideration	ius 🕶 iext includes	
	Timestamp	R/W	M/S	Addres		00 D1		D4	D5	Dő	D7										
	-9223359.2925.		01	27	OF		04	00	E4	00	3 <b>F</b>										
	-9223359.2726.		01	27	05	00	00														
	-9223359.2523.	Read						00	<b>F</b> 4	00	3D										
	-9223359.2328.		01	27	07	00	0.3	00	FE	00	46										
			01	27	07	00	03	00	FE F9	00	46 4D										
	-9223359.2130.	Read	01	27 27	0F 0F	00	03 02 03	00 00 00	FE F9 F2	00	46 4D 51										
	-9223359,2130. -9223359,1931.	Read Read	01 01 01	27 27 27	0F 0F 0F	00	03 02 03 06	00 00 00	FE F9 F2 EC	00 00 00	46 4D 51 4A										
8 -	-9223359.2130.	Read Read Read	01 01 01 01	27 27 27 27	0F 0F 0F	00	03 02 03 06 04	00 00 00 00	FE F9 F2 EC EF	00	46 4D 51										
8 - 9 -	-9223359.2130. -9223359.1931. -9223359.1733.	Read Read Read Read	01 01 01	27 27 27	0F 0F 0F	00 00 00 00 00 00	03 02 03 06	00 00 00	FE F9 F2 EC	00 00 00 00 00	46 4D 51 4A 3E										
8 - 9 - 0 -	-9223359,2130. -9223359,1931. -9223359,1733. -9223359,1533.	Read Read Read Read Read	01 01 01 01 01	27 27 27 27 27 27 27 27 27	0F 0F 0F 0F	00 00 00 00 00 00	03 02 03 06 04 03	00 00 00 00 00	FE F9 F2 EC EF FF	00 00 00 00 00 00	46 4D 51 4A 3E 36										
8 - 9 - 0 - 1 - 2 -	-9223359.2130. -9223359.1931. -9223359.1733. -9223359.1533. -9223359.1335. -9223359.1335. -9223359.0938.	Read Read Read Read Read Read	01 01 01 01 01 01 01 01 01	27 27 27 27 27 27 27 27 27	0F 0F 0F 0F 0F	00 00 00 00 00 00 00 00 00	03 02 03 06 04 03 02	00 00 00 00 00 00	FE F9 F2 EC EF FF 03	00 00 00 00 00 00 00 00 00 00 00	46 4D 51 4A 3E 36 3E										
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188 - 199 - 100 - 11 - 12 - 133 - 14 - 15 - 16 - 17 - 18 - 19 - 19 - 10	-9223359,2130 -9223359,1533 -9223359,1533 -9223359,1533 -9223359,1137 -9223359,058 -9223359,058 -9223359,058 -9223359,0542 -9223359,0542 -9223359,0542 -9223359,0547	Read Read Read Read Read Read Read Read	01 01 01 01 01 01 01 01 01 01 01 01 01 0	27 27 27 27 27 27 27 27 27 27 27 27 27 2	OF OF OF OF OF OF OF OF OF OF OF OF OF	00 00 00 00 00 00 00 00 00 00 00 00 00	03 02 03 06 04 03 02 00 FF FF FF 04 03 03 03 FF FF FF FF FF FF FF FF FF FF FF FF FF	00 00 00 00 00 00 00 00 00 00 00 00 00	FE F9 F2 EC EF FF 03 F7 F0 F0 F0 F0 F0 F0 F0 F0 F0 F0 F0 F0 F0	00 00 00 00 00 00 00 00 00 00 00 00 00	46 4D 51 36 38 38 41 42 41 43 49 38 38 39										
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#### Advanced decode result + Time-Value curve display

Div=1 s	*								30.193#							
		-9223362 s	-9223381 s	-9223360 s	-9223359 s	-0223368 s	-\$223367 #	-9223366 s		9223354 s -9223	63 s -4222062 s	-9223361 s	-9223350 s	-9223348 s	-9223340 s	-9223047 s
•		_ X							2.00							
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U_INTI(1) 417,416,																
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۰																
D_INT1 A17, A16																
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		OLive	. 🖻 🕨											Q Search All Fie	ids 💌 Text include	15 <b>X</b>
Bus 3D_INT1	(1)(AccMete	m <b>C</b>	Address	Data	Acc. X	Acc. Y	Acc. Z							Q Search All Fie	ids 💌 Text include	IS
Bus 3D_INT1	(1)(AccMete		Address REG (27)	TT	Acc. X -0.016G		Acc. Z							Q Search All Fie	ids 💌 Text include	16 <b></b> .
Bus 3D_INT1	(1)(AccMete	m <b>C</b>	Address REG (27)			Acc. Y								Q Search All Fie	ids 💌 Text include	15 X
Bus 3D_INT1	(1)(AccMete		Address REG (27) 20)	TT			Acc. Z							Q Search All Fie	ids 💌 Text include	8 <b>a</b>
Bus 3D_INT10 Timestamp -9223361.6925. -9223361.6925. -9223361.6924.	(1)(AccMete	M/S 01 STATUS_ 00TK_L() 00TK_B() 00TY_L()	Address REG (27) 20) 29) 2A)	FF 00 01 00		0.0005								Q Search All Fie	ids 💌 Text Include	18
C 3D_INT16 Timestamp -9223361.6925. -9223361.6925. -9223361.6925. -9223361.6925. -9223361.6924. -9223361.6924.	(1)(AccMete	M/S 01 STATUS_1 OUTK_L() OUTK_R() OUTK_R()	Address REG (27) 20) 29) 28) 28)	FF 00 01	-0.016G		0.016G							Q (Search All Fie	ids 👻 Text include	19 D
Bus 3D_NT10 Timestamp -9223361.6925. -9223361.6925. -9223361.6924.	(1)(AccMete	M/S 01 STATUS_ 00TK_L() 00TK_B() 00TY_L()	Address REG (27) 20) 29) 28) 28)	FF 00 01 00 F5 00	-0.016G	0.0005								् Search All Fie	ids 💌 Text include	18 C
C 3D_INT16 Timestamp -9223361.6925. -9223361.6925. -9223361.6925. -9223361.6925. -9223361.6924. -9223361.6924.	(1)(AccMete	M/S M/S OUTX_L() OUTX_B() OUTY_B() OUTY_L()	Address 200 (27) 29) 28) 28) 20)	FF 00 01 00 F5 00	-0.016G	0.0005	0.016G			_				C. Search All Fie	ids 🖵 Text include	р 19
Bus 3D_INT10 	(1)(AccMete RAV Read	M/S 01 STATUS_1 00TX_L(: 00TX_R): 00TY_R(: 00TY_R): 00TY_R(:	Address 8EG (27) 20) 29) 28) 28) 20) 20) 20)	FF 00 01 00 F5	-0.016G	0.0005	0.016G							Q (Search All Fie	ids 💌 Text include	8
Bus 3D_NT1 Timestamp -9223361.6925. -9223461.6928. -922361.6924. -9223361.6924. -9223361.6924. -9223361.6924.	(1)(AccMete RAV Read	M/S 01 STAIOS_ 01 OUTX_L( 00TX_L( 00TY_R( 00TY_R( 00TZ_L( 0	Address REG (27) 20) 23) 24) 25) 26) 20) 20) 20) 20) 20) 20) 20) 20)	FF 00 01 00 F5 00 3F	-0.016G	0.0005	0.016G							C Search All Fie	ids 💌 Text Include	18 <b></b> a
Bus 3D_NT11 Timestamp -923361.6925. -922361.6925. -922361.6924. -9223361.6924. -9223361.6924. -9223361.6924. -9223361.6924. -9223361.6924. -9223361.6924. -9223361.6924.	(1)(AccMete RAV Read	Mys Mys D1 STATUS_1 OUTE_8(: OUT	Address REG (27) 20) 29) 22) 22) 22) 22) 22) 22) 22) 22) 22	FF 00 01 00 F5 00 3F 0F 00	-0.0166 0.0006 0.9846	0.0005	0.0166							Q (Search All Fie	ids 💌 Text Include	9 <b>9</b>
Bus 30_INT11 	(1)(AccMete RAV Read	M/S M/S OTTX_1(: OTTX_1	Address REG (27) 20) 259 220 220 20) 200 200 200 200 200	FF 00 01 00 FS 00 37 07 00 FC	-0.016G	0.0005	0.0166							C. Search All Fie	ids 🐨 Text include	8 <b></b> .
30.000 30.0000 -9223361.6525. -9223361.6525. -9223361.6524. -9223361.6524. -9223361.6524. -9223361.6524. -9223361.6524. -9223361.6524. -9223361.6525. -9223361.6765. -922361.6765. -9256.776.776.776.776.776.776.776.776.776.7	(1)(AccMete RAV Read	M/S OTT_1( OTT_1( OTT_1( OTT_1( OTT_1( OTT_1( OTT_1( OTT_1( OTT_1( OTT_1(	Address AEG (27) 29) 20) 20) 20) 20) 20) 20) 20) 20	77 00 01 00 75 00 37 07 00 00 70 00 00	-0.0166 0.0006 0.9846	0.0005 -0.1725 0.2345	0.0166 0.0006 0.0005							Q (Search All Fie	ids 💌 Text include	is a
3 (Ban) 3D_NT11 Timestamp -9223361.6525 -9223361.6525 -9223361.6525 -9223361.6525 -9223361.6525 -9223361.6526 -9223361.6526 -9223361.6526 -9223361.6765 -9223361.6765 -9223361.6765	(1)(AccMete RAV Read	M/S 01 STATUS_1 OUTX_1(:	Address EEG (27) 29) 20, 20, 20, 20, 20, 20, 20, 20,	FF 00 01 00 F5 00 3F 07 00 FC 00 F2	-0.0165 0.0005 0.9845 -0.0636	0.0005 -0.1725 0.2345	0.0166							C. Search All Fie	ids 🖵 Text include	9
Dem( 30_MTH) Timestamp 9223961.6925. 9223961.6925. 9223961.6924. 9223961.6924. 9223961.6924. 9223961.6924. 9223961.6924. 9223961.6924. 9223961.6765. 9223961.6765. 9223961.6765.	(1)(AccMete RAV Read	M/S 01 STATUS_1 OUTL_8(: 01T_8(: 0TT_8(: 01T_8(: 01T_8(: 01T_8(: 0TT_8(: 0TT_8(: 0TT_8(: 0TT_8(:	Address EEG (27) 28) 29) 20, 20) 20) 20) 20) 20) 20) 20, 20, 20, 20, 20, 20, 20, 20,	FF 00 01 00 F5 00 07 F2 00 F2 00	-0.0166 0.0006 0.9846	0.0005 -0.1726 0.2345 0.0005	0.0166 0.0006 0.0005							🔍 Search All Fie	ids 💌 Text Include	15 <b></b>
<sup>9</sup> ) Bm( 30.0111) — Temestamp — 222341.6225. — 222341.6225. — 222341.6225. — 222341.6235. — 222341.6235. — 222341.6245. — 222341.6255. — 222341.6	(1)(AccMete R/W Read	M/S M/S 01 STATUS_ OUTL_B(C OUTL	Address EE6 (27) 28) 59) 28) 28) 28) 28) 28) 26) 28) 28) 28) 28) 28) 28) 28) 28) 28) 28	FF 00 01 00 F5 00 F5 00 F7 00 F2 00 F2 00 39	-0.0165 0.0005 0.9845 -0.0636	0.0005 -0.1725 0.2345	0.016G 0.000G 0.000G -0.219G							् (Search All Fie	ids Text include	9 <b>9</b>
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### AD-Mux Flash

AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

#### Settings

Amax: Setting the number of address pin.

**Quick Setup/User Defined:** Only set ADQ[0](LSB) when select the Quick Setup, other channels will be set automatically. When check User Defined and press the button will show the dialog below:

📥 Address / L	Data Bus						×
ADQ[0]	A6	\$ ADQ[8]	A14 🗘	A[16]	A22	\$ A[24]	AO 📮
ADQ[1]	A7	\$ ADQ[9]	A15 🗘	A[17]	A23	•	
ADQ[2]	A8 :	DQ[10]	A16 🗘	A[18]	A24	•	
ADQ[3]	A9	ADQ[11]	A17 🗘	A[19]	A25	•	
ADQ[4]	A10	ADQ[12]	A18 🗘	A[20]	A26	\$	
ADQ[5]	A11	DQ[13]	A19 🗘	A[21]	A27	÷	
ADQ[6]	A12	DQ[14]	A20 🗘	A[22]	A28	\$	
ADQ[7]	A13	\$ ADQ[15]	A21 🗘	A[23]		-	
						OK	Cancel

Flash: Control pins of flash.

**PSRAM:** Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when "has PSRAM" is checked.

**Configuration:** The default setting of configuration register. User must set here to make a correct analysis.



	545.45 ns
Outcome         Outcome <t< th=""><th></th></t<>	
Descere         Descere         Descere         Adda           2 frag         Probat         Bables         Spin_2xites         370         100         101         01         02         014         05         01	
2748.4         93284         93270         900.*Exts         700         100	ides D
452.00         978.04         0.2010         000-Refer to 100         000-Ref	
Sides         Tam.         Dates         Open.Red         Old         FEA         FEA         FEA         Side         FEA         Side         FEA         Side         Side <th< td=""><td></td></th<>	
Team         File         TRAME         CATTOR         OpenArtice         TOP         OLD         COLD         EAD         CEL         EAT         TEAT         SADE         TAT         Cold         TAT         Cold         TAT         Cold         TAT         Cold         TAT         Cold         Cold         Cold         EAD         Cold         TAT         Cold	
Pfew         PRAM         D2376         Prom.Nr:te         D258         Prom.N	
1.05cm         Tash         03384         Open.Red         713         EXT         000         151         EXT         010         EXT         151         EXT         010         EXT         011         EXT         0111         011         011	
1.54         TRAM         0.276         Tra         0.276         0.20 <t< td=""><td></td></t<>	
1.44         Tam         83380         Tyme.Red         600         EED         FIGURE         Core         Set of the test         Set of test<	
1.55.00         TRAM         0.2376         Open Series         TV         ODE         EAS         FILT         EAS         EAS         FILT         Series         Series         Series         S	
D.144         PRAM         B2380         Pynn-Krite         REF         ONA         EAST         EAST         ONA         EAST         ONA         EAST         EAST         ONA         EAST	
J. 646         Flash         033804         0pm.8-md         6010         520         011         Earry         Flash         Earry         Earry         Flash <th< td=""><td></td></th<>	
J. State         FIRMA         C23800         Open-Verse         800         FILI         FILI         EAT         C038         FILI         EAT         C038         FILI         EAT         C038         FILI         FILI         C038         FILI         EAT         C038         FILI         C038         FILIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	
3.50me         FIRM         623310         pps.%rite         KED         DAC         DAT         DAT         DAT         DAT         DAT           3.50me         Firsh         633840         pps.%rite         KED         DAC         DAT	
2.880us         Fineh         033840         Sync.Read         0020         EMA         1000         EMA         1000         EMA         0027         EMA	
2.45m 783AH 02010 70c.45tc 010 100 100 100 100 100 100 100 100 10	
3.056us P5RAH 023820 Sync.Write E92D 0017 E800	
3,100us Flash 033850 Sync.Read 1004 E594 0820 EIA0 1078 E201 1FC0 E381 1004 E584 0000 E350 4010 088D FESC 0AFFx.	
3.4us 2783A4 023820 Sync.M:tto 8320 TFET FTET TITE ATT TALE HAT TAGE EAST 0400 EAS 0000 EAS 020 0	

### APML

APML protocol is established by AMD for it's Opteron CPU platform.

Settings	
APML Rev. 1.06 Settings	×
Parameter Channel SCL	Color Command Address
SDA A1	
Address	Write / Read
8-bit Addressing (Include R/W in Address)	Start / Stop / Sr
PEC	PEC / Byte Count / Word
Ignore Glitch	Data 🗾
Range	
From To Buffer Head Buffer Tail	
	ODefault ✓OK XCancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

8-bit addressing (Include R/W in Address): Show 8-bit addressing (include



7-bit addressing and 1-bit R/W). Enable when checked.

**PEC:** Packet Error Check. Enable when checked.

**Ignore glitch:** Ignore the glitch when the slow transitions. Enable when checked.



me/Div=100 us	3			8,076												
	-700 us	-800 us	-500 us	-400 us	-360 us	-200 us	-100 us	D pa 100 us	200 us	300 us	400 cu	600 us	600 us	700 us	800 us	933 us
0					11 I I I I I I I I I I I I I I I I I I				1							
				ALALTE TRUCK	WA DAM SETSI MI	011		S Addr SB_TSI(4C) R	A Dets CpeTempInt	200 N						
				MUULED_INC(#C)	The Domand Long And			S None and Intelling)	of a parchasemin	277 A.						
						0 0 0										
APU-SIC SCL-0																
									n n							
3DA-1				16.95 u			188 94 m	96.95 w	45.03 w	38.52 v						
APML							188.94 m									_
PU-SID			U				188,94 m		45.05 W [] [	he 25 A						
15. IS	OL	ive														, <b>e</b> _ 5
abel Channe	4 4															
NO0 3/5-7/5													0.0			R .
Bus APU-SH	C(APML) 🚽 😋 📗												Q Search	1 All Fields 🔻 Tex	t includes	× /
Timestamp	Address		Value				Descriptio	n								
-479.96us	SB-TSI(4C)	SBISI_x01(01)			CPU Temperatu:		Register									
0pa	SB-TSI (4C)	CpuTempInt(29)			CPU Integer to											
49.515925ms	SB-TSI (4C) SB-TSI (4C)	SBT51_x01(01)			CPU Temperatu:		Register									
49.995005ms 99.51101ms	SB-TSI(4C) SB-TSI(4C)	CpuTempInt(29) SBTSI x01(01)			CPU Integer to		Bandanaa									
99.99177ms	SB-TSI (4C)	CpuTempInt(29)			CPU Temperatu CPU Integer to		Regiscer									
149.5077ms	5B-TSI (4C)	SBISI x01(01)			CPU Temperatu:		Register									
149.98766ms	SB-TSI (4C)	CpuTempInt(29)			CPU Integer to											
199.503585mm	SB-TSI (4C)	SBT51 x01(01)			CPU Temperatus		Register									
199.903545ms	SB-TSI (4C)	CpuTempInt (29)			CPU Integer to											
249.49947ms	SB-TSI (4C)	SBTSI x01(01)			CPU Temperatu:	re High Byte	Register									
249.97943ms	SB-TSI (4C)	CpuTempInt(29)			CPU Integer to	emp. 41										
299.495355ms	SB-TSI (4C)	SBT51_x01(01)			CPU Temperatu:		Register									
299.975315ms	SB-TSI (4C)	CpuTempInt(29)			CPU Integer to											
349.491235ms	SB-TSI(4C)	SBT51_x01(01)			CPU Temperatu:		Register									
349.971195ms	SB-TSI(4C)	CpuTempInt(29)			CPU Integer to		-									
7 399.48712ms	SB-TSI(4C)	SBTSI_x01(01)			CPU Temperatu:	re migh Byte	Register									
399.96708ms	SB-TSI(4C)	CpuTempInt(29)			CPU Integer to											
449.483005ms 449.962965ms	SB-TSI (4C) SB-TSI (4C)	SBTSI_x01(01) CpuTempInt(29)			CPU Temperatu:		Register									
449.96296588 1 499.4788988	SB-TSI (4C) SB-TSI (4C)	SBT51_x01(01)			CPU Integer to CPU Temperatus		Designer									



### **AVSBus**

AVS stands for Audio-Visual Coding Standard, which is a video and audio coding standard used to compress, transmit and decode digital video and audio data.

🛋 AVS Settings	×
Parameter	Color
Channel	
CLK A0	
MOSI A1	Start Code 🗸 🗸
MISO A0	CMD
AV/ODur	CMD Group
AVSBus MData	CMD Data Type 🔍
	Select 🔹
Range	CMD Data
Decode Range	Slave Ack 🔹
From To Buffer Head V Buffer Tail V	Status Response 🔹
Butter Head 👻 Butter Tail 👻	ODefault ✔OK ¥Cancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

**AVSBus:** Set the decoded data type to SData or MData.

Detail Report: Show details in report area, enabled when checked.



Time/Div=	500 ns	2										
			4241 4241	s 424 <i>s</i> 424 <i>s</i>	4245 4245	4241 4241	4241	4245 4245	4243	4243 4243	4245	4241
	0			3 3 0 Reserved_16(F99F)	5 1 3 3 mfm.(1)	Reterved_16(FFFF) 2		All IN GDLED				
	CLK-A0											
🔺 Bus 1											_	
	MOSI-A1		150	a 150 x 200 ne 850 xe	150 n 150 n 150 n	850 na 15	i0 n					
	MISO-A2			1.05 ==	] [50 m] 50 m]   450 m	200 ns 250 ns 1	80 al 50 a	450 m 250				
	AVSBus				كتقل ابتان ا		_ ل تقات					
	0		3	14 Reserved_21(1FFFFF)	1 0 14 0	190 IF 1	0 14	0164 11				
						000000000000000000000000000000000000000	00000000	000000000000000000000000000000000000000	10000			
	CLK-A0											
📕 Bus 2				<u>,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,</u>								
	NOSI-AL			) n 0.50 m 200 m 850 m	150 n 150 n 150 n	850 as						
	MISO-A2				1 50 a 1 50 a	200 ns 250 ns 11	8	450 m				
	AV58us		Ļ									
	_											
<b>D</b> \$.			ive									<b>,</b>
Label	Channel	•										•
CH-00	Bus Bus 1(AV	SBus) 🖵 💽 📗	L 🖻 🕨							Q Search All Fie	ds 👻 Text includes	× ∧ ۱
	Timestamp	Cmd	CmdGroup	CmdDataType	Select	CmdData	CRC	Information				
	4.2429086s 4.243150335s	ALL_1_IDLE Read(3)	AVSBus (0)	Temperature Read(3)	RailSel(0)		_					
	4.2431503358	Read(3)	AVSBUS(0) AVSBUS(0)	Temperature Read(3) Temperature Read(3)	mfrs.(1)		2					
	4.243153735s 4.24392667s	ALL_1_IDLE										
	4.24392667a 4.24392837a	Read(3) Read(3)	AVSBus (0) AVSBus (0)	Current Read(2) Current Read(2)	RailSel(0) mfrs.(1)		4					
687	4.24393007#	ALL 1 IOLE										
	4.243979075a 4.243980775a	Read(3) Read(3)	AVSBus(0) AVSBus(0)	Temperature Read(3) Temperature Read(3)	RailSel(0) mfrs.(1)		3					
690	4.243902475#	ALL_1_IDLE										
	4.244791215#	Read(3) Read(3)	AVSBus(0) AVSBus(0)	Temperature Read(3) Temperature Read(3)	RailSel(0) mfrs.(1)		5					
693	4.244794615s	ALL_1_IOLE										
	4.2449454558	Read (3)	AVSBus(0)	Current Read(2)	RailSel(0)		1					
	4.244947155#	Read(3) ALL 1 IDLE	AVSBus (0)	Current Read(2)	nfrs.(1)							



### **BiSS-C**

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings	
🚐 BiSS-C Rev.C6 Settings	×
Channel	Color
MA A0 SLO A1	Ack / ADR
Type of Data     Single Cycle Data       Serial Data Length (bits)     12     (Range: 1 ~ 64)	Start 🗾 💌
Data Channel 1	
SLO Phase 0 \$ samples	Flag / IDL / ID
Range	CRC 🔽
Decode Range	Stop / Ex 🗾 🗸
From To	Read / IDS
Buffer Head 💌 Buffer Tail 💌	Write / IDA
ODefault	✓OK XCancel

**MA/SLO:** Setting the channel of MA and SLO.

**Type of data:** Setting the type you want to decode. It include "Register Data-CDM", "Register Data-CDS", "Single Cycle Data".

**Serial data length(bits):** Setting the data length when Single Cycle Data mode.

**Data Channel:** Startup setting, users need to provide the number of slaves as the base information for decoding.

**SLO Phase:** Sets the delay phase of the SLO.





ime/Div= 5 us couired: 07:37:22.554	-	-440.19 us -405.	.18 us -400.	1.17 us -426.16	us -420.15 us	-415.13 US	-410.12 us -405.11 us	. 062a.s -400.1 vs	-395.09 us -390.09 us	-385.05 US	-380.05 us	-375.84 us	-370.03 us	-365.02 us
0 (guiled: 07:37:22:554					111		· · · · · · · ·		<b>II</b> · · · · · · · ·			1		
				A	5 <mark>C</mark> 0	7E	A6 1F	E11 CRC:3F	P CDM:1	-				
					U									
					100000000000000000000000000000000000000	100000000	100000000000000000000000000000000000000	10000000000						
BUS_BISS-C NA-A1														
								0000000000						
SLO-A	0						1.3 u 2.56 u							
855-C						J UL								
														_
														(1)     (2)
<b>15 16</b>	$\bigcirc$	Live												.0
abel Chan														,
CH.00 3/5-7/												Search All Fields	<b>D</b>	
CHLOO BUS BUS	BISS-C(BISS-C)													
												•(		
:amp (hh:mm:ss.m		nError nW	larning (		CDM Information									
07:37:22.557	07EA61F		laming (	CRC CDS	CDM Information									
07:37:22.557	07EA61F 07EA61F	nError nW	aming 0 37 3F	0	CDM Information									
07:37:22.557 07:37:22.557 07:37:22.557	07EA61F 07EA61F 07EA61F	nError nW	aming ( 37 37 37	0	CDM Information									
07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557	07EA61F 07EA61F 07EA61F 07EA61F	nError nW	aming 0 37 35 35 37	0	CDM Information									
07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557	07EA61F 07EA61F 07EA61F 07EA61F 07EA61F	nError nW	laming ( 37 37 37 37 37	0	CDM Information									
07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557 07:37:22.557	07EA61F 07EA61F 07EA61F 07EA61F 07EA61F 07EA61F	nError nW	laming ( 37 37 37 37 37 37 37	0	CDM Information									
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07:37:22.587. 07:37:22.587. 07:37:22.587. 07:37:22.587. 07:37:22.587. 07:37:22.587. 07:37:22.588. 07:37:22.588. 07:37:22.588. 07:37:22.588. 07:37:22.588.	07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F 07EA41F	nError nW	aming 0 37 37 37 37 37 37 37 37 37 37 37 37 37	0 0 0 0 0 0 0 0 0	CDM Information									
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07,17722,557. 07,177	07EA41F 07EA41F	nError nW	taming 0 37 37 37 37 37 37 37 37 37 37 37 37 37	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										
07:37:122.557.           07:37:122.557.	07EA41F 07EA41F	nError nW	taming 0 37 37 37 37 37 37 37 37 37 37 37 37 37	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										



# BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

### Settings

📥 BSD Settings				×
Channel	Color			
<b>1</b>				
•-#	DIR	•	Read / Write	-
Data 🗛 🌲	Address	•	Sync	-
Bit Rate Auto 💌	Data		Parity	•
Range				
Decode Range				
From	То			
Buffer Head 🔹	Buffer Tail	ODefa	ault VOK	Cancel

### Data: The BSD data.

Bit rate: The bit rate of the BSD data

Div=2ms	2	283.£6 ma	286.26 ms	287.05 ms	209.05 mit	291	1.05 ma	293.05 ma	295.05 ms 297	26 ma 299.26 ma	301.05 mil	303.05 ma	305.05 ms	307.05 ma	309.26 ma	311.05 ma	313.05 ma
<b>0</b> 155					Syn	۰ . د	Master 3	Salve Aðdr: 6	Weite Register Addr. :	E P1 Ok	Date: 1		P2 Ok				
820- <b>X</b> 880	•				749.2 % 749	vo 749 vo						64	55 w				
P. 15	0	Live															
el Chan	nel 🔳														O Search All Fie	ulda 💌 Taat kardunda	
Bus Bsse	nel 🔳	<u>III 🖻 🏲</u>	Register Addr	Read / Writ	e P1	Deta	P2	Ack							🔍 Search All Fie	elds 💌 Text Include	
Dens Bass(E Timestamp 190.8714ms	nel ( ISD) <b>C</b> DIR Master		Register Addr	Read / Writ Read	Ok			Ack							Q Search All Fie	Hds 💌 Text Include	
Channel Busk BSS(E Timestamp 190.8714ms 290.0030ms	ISD) C	<u>III 🖻 🏲</u>	Register Addr 2 1	Read. Write	Ok Ok		P2 Ok	Ack							Q Search All Fie	elds 💌 Text include	
Channel Bask BSS(E Timestamp 190.0714ms 290.0031ms 390.065ms	ISD) C	<u>III 🖻 🏲</u>	Register Addr 2 1 2	Read Write Read	Ok Ok Ok	01	Ok	Ack							🔍 Search All Fie	elds 💌 Text Include	
Chann Channel	ISD) C DIR Master Master Master Master Master	<u>III 🖻 🏲</u>	Register Addr 2 1 2 0	Read Write Read Write	Ok Ok Ok Ok	01		Ack							Q Search All Fie	elds 💌 Text Include	
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Chann Composition	NSD) C DIR Master Master Master Master Master Master	<u>III 🖻 🏲</u>	Register Addr 2 2 2 2 2 2 2 3 0 0	Read Write Read Write Read Write Read Write	Ok Ok Ok Ok Ok Ok Ok Ok	01 6a 01	Oiz Oiz	Ack							🔍 Search All Fie	ilds 👻 Text Include	
Chare Timestamp 190.0714m5 290.0828ms 390.0858ms 490.9054ms 590.072ms 790.0986ms 590.0972ms	isD) C DIR DIR Master Master Master Master Master Master Master Master Master Master	<u>III 🖻 🏲</u>	Register Addr 2 1 2 2 1 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read	Ok Ok Ok Ok Ok Ok Ok Ok	01 6a 01 6a	ok Ok Ok	Ack							🔍 Search All Fie	elds 💌 Text include	
Charr Ch	Nel * ISD) C DIR Master Master Master Master Master Master Master Master Master Master Master Master	<u>III 🖻 🏲</u>	Register Addr 2 1 2 2 2 1 2 2 2 1	Read Write Read Write Read Write Read Write Read Write	Ok Ok Ok Ok Ok Ok Ok Ok Ok Ok	01 6a 01 6a	Ole Ole	Ack							Q Search All Fie	ilds 💌 Text include	
Charr Charles Charl	Nel SDI C DIR Master Master Master Master Master Master Master Master Master Master Master Master	<u>III 🖻 🏲</u>	Register Addr 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read Write Read	0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k	01 6a 01 6a 01	Ok Ok Ok Ok	Ack							🔍 Search All Fie	Hds 🛡 Text Include	
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Chain           Chain         Chain           Composition         Composition	Nel SDI C DIR Master Master Master Master Master Master Master Master Master Master Master Master Master Master Master	<u>III 🖻 🏲</u>	Register Addr 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read Write Read Write Read	0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0	01 6a 01 6a 01 6a	Ok Ok Ok Ok Ok Ok	Ack							🔍 Search All Fie	Hds 🛡 Text Include	
Channel           001         Desc.         855(E           150.0714ms         250.0714ms           250.051ms         550.0714ms           550.0714ms         550.0714ms           550.0714ms         550.0714ms           550.0714ms         550.0714ms           1.050012ms         1.050012ms           1.1500012ms         1.1500012ms	Nel C ISD) C DR Master	<u>III 🖻 🏲</u>	Register Addr 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read Write Read Write Read Write	0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0	01 6a 01 6a 01 6a	Ok Ok Ok Ok	Ack							🔍 Search All Fie	ilds 💌 Text Include	
Chain           20         200.0         200.0         8556           Timestamp         150.0714ms         850.0714ms         850.0714ms           250.0.0318ms         550.0714ms         550.0714ms         550.0714ms           590.0.5714ms         550.0772ms         790.05058ms         1.0505128         1.15050128         1.15050128         1.35052305         1.35052328         1.35052328         1.55052346 <td>el « ISD) C C DIR Master M</td> <td><u>III 🖻 🏲</u></td> <td>Register Addr 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2</td> <td>Read Write Read Write Read Write Read Write Read Write Read Write Read Read</td> <td>0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0</td> <td>01 6a 01 6a 01 6a 01</td> <td>Ok Ok Ok Ok Ok Ok</td> <td>Ack</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>🔍 Search All Fie</td> <td>Hds 💌 Text Include</td> <td></td>	el « ISD) C C DIR Master M	<u>III 🖻 🏲</u>	Register Addr 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read Write Read Write Read Read	0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0k 0	01 6a 01 6a 01 6a 01	Ok Ok Ok Ok Ok Ok	Ack							🔍 Search All Fie	Hds 💌 Text Include	
Chare Chare Composition Comp	el X ISD) C I DR Master Ma	<u>III 🖻 🏲</u>	Register Addr 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read Write Read Write Read Write Read Write	Oir	01 6a 01 6a 01 6a 01	Ok Ok Ok Ok Ok Ok	Ack							Q Search All Fie	elds 💌 Text Include	
el Charn Charnel Char	el « ISD) C C DIR Master M	<u>III 🖻 🏲</u>	Register Addr 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Read Write Read Write Read Write Read Write Read Write Read Write Read Read	Ole           Ole	01 6a 01 6a 01 6a 01 6a	Ok Ok Ok Ok Ok Ok	Ack							🔍 Search All Fie	Hds 💌 Text Include	



## BT1120

### Digital interfaces for HDTV studio signals

The BT1120 is used for bit serial port transmission of HDTV signals. It mainly provides image format parameters and data transmission signals for HDTV production and international program exchange, and is backward compatible with old image frequencies of 60, 50, 30, 25 24Hz (progressive, interlaced, frame segmentation), total line number 1125, valid line number 1080 to cover both commercial and developing products. This interface will include all equipment necessary for broadcast and industrial applications.

ettings BT1120 Settings	;
Parameter	Color
Observat	SAV
Channel	YA/CA 🗸
CLK A0	YD/CRD 🗸
Data 0 🗚 🌲 🗸 Quick Setting	CBD
Data 1 A2	YCR / CCR
Data 2 A3	LN
Data 3 A4	EAV
Data 4 A5	Range
Data 5 A6	Decode Range
Data 6 A7	From To
Data 7 A8	Buffer Head 💌 Buffer Tail 💌
Stream	Obefault ✓OK ★Cancel

**Channel setting:** Set the object to be tested, CLK, each Data 0-7, the channel number connected to the logic analyzer,

**Quick Setting:** the Data channel setting will be automatically incremented. **Stream:** Y, CB/CR stream



Div= 20 ns	3,632	s									9	10.982ms	9						
red: 20:23:32.046			-93.98 ma	-93.98 ma	-93.98 ma	-93.98 ms	-44	196 ma	-93.	al ma	-93.98 m		-93.98 ma	-93.98 ma	-60.56 mi	-93.98 ma	-93.98 ma	-93.98 ma	-93.98 ma
۰																			
JS_BT1120( A1)	S, A14, A1	EAAG EAAG ENOD FA		AUYCAUYCAUY CAU	CAUSCAUS	CKUY CKU C	AGS CRUSC	AD CAU	(LEG9C)	(I) CA(I) C	K(I CAGIS	CRUYCI	AU CAUSCAUSC	AUY CAU CA	19°CK(19°CA(19°C	nu cruscritecr	() CACIFICACIÓN CA	uycan canyc	AU9 CAU9 CAU CAU9 CA
	O Liv	e																	
	hannel J		•					-			_					Q Search All	Fields	Text inc	ludes 📃 🗖
Bus BU	US_BT1120(1)(BT1120) 🚽 😋			S/EAV3	LN	YCR/CCR	D0 D1	D2	D3	D4 D	5 D6	D7	Information			Q Search All	Fields	Text inc	ludes 📃 🖂
Bus BU			S/EAV2	S/EAV3 CRD/CBD[1904 : _			D0 D1 3C 3D	38	37	40 41	42	43	Information			Q Search All	Fields	Text inc	ludes a
Bus BU tamp (h) 20:23:1 20:23:1	US_BT1120(1)(BT1120) C htmm:ss.ms S/EAVO 32.051 32.051	S/EAV1	S/EAV2		-			38	37	40 41		43	Information			Q Search All	Fields	Text inc	ludes p
Bus BU 2012311 2012311 2012311 2012311	US_BT1120(1)(BT1120) C htmm:ss.ms S/EAVD 32.051 32.051 32.051			CRD/CBD[1904 :	-		3C 3D	38	37	40 41	42	43	Information	5 		Q Search All	Fields	Text inc	ludes
Bus BU 2012311 2012311 2012311 2012311 2012311	US_BT1120(1)(BT1120) C htmm:ss.ms S/EAVD 32.051 32.051 22.051 E:FF 32.051	S/EAV1	S/EAV2	CRD/CBD[1904 : CRD/CBD[1912 : E:9D	-	1010	3C 3D 44 45	3E 46	3 <b>F</b> 47	40 41 48 49	42 4λ	43 48	Information			Q Search All	Fields	Text inc	udes o
Bus BU 2012311 2012311 2012311 2012311 2012311 2012311 2012311	US_BT1120(1)(BT1120) C hummiss.ms S/EAV0 32:051 32:051 22:051 22:051 32:051	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:9D CA[1928 : 1921]	-	1010	3C 3D 44 45	3E 46 10	37 47 10	40 41 48 49 10 10	42 4A 10	43 48 10	Information			Q Search All	Fields	Text inc	udes o
Bus Bu 20:2311 20:2311 20:231 20:231 20:231 20:231 20:231	US_BT1120(1)(BT1120) C hmmxs.ms S/EAVO 32.051 32.051 32.051 32.051 32.051	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:9D CA[1928 : 1921] CA[1936 : 1929]	-	1010	3C 3D 44 45 10 10 10 10	3E 46 10 10	3F 47 10 10	40 41 48 49 10 10 10 10	42 4A 10 10	43 48 10	Information			Q Search All	Fields	Text inc	ludes e
Bus BU amp (h) 2012311 2012311 2012311 2012311 2012311 2012311 2012311 2012311	US_BT1120(1)(BT1120) C humenses ms S/EAVO 32.051 32.051 32.051 32.051 32.051	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:9D CA[1928 : 1921] CA[1936 : 1929] CA[1944 : 1937]	-	1010	3C 3D 44 45 10 10 10 10 10 10	3E 46 10 10	37 47 10 10	40 41 48 49 10 10 10 10 10 10	42 4A 10 10	43 48 10 10	Information			Q Search All	Fields	Text inc	udes b
Bux BU 20:23: 20:23: 20:23: 20:23: 20:23: 20:23: 20:23: 20:23: 20:23:	US_BF1120(1)(BT1120) htmmss.ms \$2.051 32.051 32.051 32.051 22.051 22.051 22.051	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:9D CA[1928 : 1921] CA[1936 : 1929] CA[1936 : 1929] CA[1952 : 1945]	-	1010	3C 3D 44 45 10 10 10 10 10 10 10 10	3E 46 10 10 10 10	37 47 10 10 10 10	40 41 48 49 10 10 10 10 10 10 10 10	42 4Å 10 10 10 10	43 48 10 10 10 10	Information			Q (Search All	Fields	Text inc	udes p
Bus(BU) 201231 201231 201231 201231 201231 201231 201231 201231 201231 201231	US_BF11201()(BT1120) 22.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:9D CA[1928 : 1921] CA[1936 : 1929] CA[1944 : 1937] CA[1952 : 1945] CA[1960 : 1953]	-	1010	3C 3D 44 45 10 10 10 10 10 10 10 10 10 10 10 10	3E 46 10 10 10 10 10	37 47 10 10 10 10 10	40 41 48 49 10 10 10 10 10 10 10 10 10 10 10 10	42 4A 10 10 10 10 10	43 48 10 10 10 10 10	Information			Q (Search All	Fields	Text inc	udesP
Bux Bux 20:23:1 20:23:1 20:23:2 20:23:2 20:23:2 20:23:2 20:23:2 20:23:2 20:23:2 20:23:2	US_BF1120()(BT1120) hmmss.ms \$/\$AV0 22.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051 23.051	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:9D CA[1928 : 1921] CA[1936 : 1929] CA[1936 : 1929] CA[1944 : 1937] CA[1960 : 1963] CA[1960 : 1963]	-	1010	3C 3D 44 45 10 10 10 10 10 10 10 10 10 10 10 10 10 10	3E 46 10 10 10 10 10 10	37 47 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10	43 48 10 10 10 10 10 10	Information			Q (Search All	Fields	Text inc	udes p
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A constant of the second secon	US_BF1120(1)(BF1120) C htmmssms S(EAVO 22.051.	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:SD CA[1928 : 1921] CA[1928 : 1921] CA[1944 : 1937] CA[1952 : 1945] CA[1960 : 1953] CA[1966 : 1953] CA[1976 : 1959] CA[1976 : 1957]	-	1010	3C         3D           44         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10	3F 47 10 10 10 10 10 10 10	40 41 48 49 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	42 4A 10 10 10 10 10 10 10 10	43 45 10 10 10 10 10 10 10 10 10	Information			C Search All	Fields	Text inc	udes p
Bus Bus 201231 201231 201231 201231 201231 201231 201231 201231 201231 201231 201231 201231 201231 201231	US_BT1120(1)(BT1120) C Thrmensame S/EAVO 22.081. 22.08	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:SD CA[1926 : 1921] CA[1936 : 1928] CA[1936 : 1928] CA[1944 : 1907] CA[1950 : 1945] CA[1940 : 1945] CA[1946 : 1945] CA[1916 : 1945]	-	1010	3C         3D           44         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10	37 47 10 10 10 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4Å 10 10 10 10 10 10 10 10 10	43 45 10 10 10 10 10 10 10 10 10	Information			C Search All	Fields	Text inc	udes o
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Bus	US_BT1120(1)(BT1120) C Internasione S(EAVO 22.031. 22.	S/EAV1	S/EAV2	CRD/CBD[1904 : _ CRD/CBD[1912 : _ E:SD CA[1928 : 1921] CA[1936 : 1922] CA[1946 : 1925] CA[1946 : 1987] CA[1946 : 1983] CA[1946 : 1984] CA[1946 : 1984] CA[1946 : 1984] CA[1946 : 1984] CA[1942 : 1985] CA[2000 : 1985] CA[2000 : 2001]	-	1010	3C         3D           44         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10 10 10	37 47 10 10 10 10 10 10 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10 10 10 10 10 10 10 10	43 48 10 10 10 10 10 10 10 10 10 10 10 10	Information			C Search All	Fields	Text inc	udeso
Bus	US_BT1120(1)(BT1120) C kmmras.ms 5/6AVO 22.081. 23.081	S/EAV1	S/EAV2	CRD/CRD[1904 : CRD/CRD[1902 : E:9D CA[1928 : 1921 : CA[1928 : 1921] CA[1936 : 1925] CA[1946 : 1953] CA[1952 : 1945] CA[1952 : 1945] CA[1954 : 1951] CA[1954 : 1951] CA[1954 : 1952] CA[1952 : 1955] CA[2006 : 1953] CA[2006 : 1953] CA[2006 : 2005]	-	1010	SC         3D           44         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10 10 10 10	37 47 10 10 10 10 10 10 10 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10 10 10 10 10 10 10 10	43 48 10 10 10 10 10 10 10 10 10 10 10 10 10	Information			Search.All	Fields	Text inc	udes)o
Bung (Bu) amp (b) amp (b) a	US_BT1120(1)(BT1120) SJEAU0 SJEAU	S/EAV1	S/EAV2	CB0/CB0[1904 : . CB0/CB0[1912 : . E190 CA[1926 : 1921] CA[1936 : 1921] CA[1936 : 1923] CA[1944 : 1937] CA[1952 : 1945] CA[1946 : 1953] CA[1946 : 1953] CA[1946 : 1965] CA[1984 : 1965] CA[2000 : 1963] CA[2016 : 2005] CA[2014 : 2017] CA[2014 : 2017]	-	1010	SC         SD           44         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10 10 10 10	37 47 10 10 10 10 10 10 10 10 10 10 10 10 10	40         41           42         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10 10 10 10 10 10 10 10	43 48 10 10 10 10 10 10 10 10 10 10 10 10 10	Information			C Search All	Fields	Text inc	udes 📃 🔿
<ol> <li>JBan ( BU</li> <li>Bun ( BU</li></ol>	US_BT1120(1)(BT1120) homesem S(EAVO 22.051 22.05	S/EAV1	S/EAV2	CBD/CBD[1904 : _ CBD/CBD[1912 : _ Z150 CA[1928 : 1921] CA[1928 : 1921] CA[1938 : 1297] CA[1938 : 1297] CA[1938 : 1297] CA[1938 : 1953] CA[1946 : 1953] CA[1946 : 1953] CA[1946 : 1959] CA[1952 : 1969] CA[1952 : 1969] CA[200 : 2001] CA[200 : 2003] CA[200 : 2003] CA[200 : 2003]	-	1010	BC         BD           64         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10 10 10 10	37 47 10 10 10 10 10 10 10 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10 10 10 10 10 10 10 10	43 48 10 10 10 10 10 10 10 10 10 10 10 10 10	Information			Search All	Fields	Text inc	udesjo
Image (h)         Image (h)           9         0.0231           10         0.0231           10         0.0231           2         0.0231           3         0.0231           4         20.0231           5         0.0231           6         0.0232           8         0.0231           9         0.0231           10         0.0231           12         0.0231           13         0.0231           14         0.0231           15         0.02331           16         0.0231           17         0.02321	US_BTV120(1)(BT120) C homsame CANO 22.011.	S/EAV1	S/EAV2	CB0/CB0[1904 : _ CB0/CB0[1912 : _ E750 CA[1968 : 1922] CA[1936 : 1922] CA[1936 : 1923] CA[1946 : 1937] CA[1946 : 1937] CA[1946 : 1943] CA[1946 : 1944] CA[1946 : 1944]	-		BC         BD           64         45           10         10	3E 46 10 10 10 10 10 10 10 10 10 10 10 10 10	37 47 10 10 10 10 10 10 10 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10 10 10 10 10 10 10 10	43 45 10 10 10 10 10 10 10 10 10 10 10 10 10	Information			C Search All	Fields	Text inc	udes o
Jean (Bu)           20:23:5	US_BT1120(1)(BT1120) homesem S(EAVO 22.051 22.05	S/EAV1	S/EAV2	CBD/CBD[1904 : _ CBD/CBD[1912 : _ Z150 CA[1928 : 1921] CA[1928 : 1921] CA[1938 : 1297] CA[1938 : 1297] CA[1938 : 1297] CA[1938 : 1953] CA[1946 : 1953] CA[1946 : 1953] CA[1946 : 1959] CA[1952 : 1969] CA[1952 : 1969] CA[200 : 2001] CA[200 : 2003] CA[200 : 2003] CA[200 : 2003]	-		BC         BD           64         45           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	3E 46 10 10 10 10 10 10 10 10 10 10 10 10 10	3F 47 10 10 10 10 10 10 10 10 10 10 10 10 10	40         41           48         49           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10           10         10	42 4A 10 10 10 10 10 10 10 10 10 10 10 10 10	43 48 10 10 10 10 10 10 10 10 10 10 10 10 10	Information			C Search All	Fields	Text inc	udes}



# CAN 2.0B/ CAN FD

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN\_H) and CAN Low (CAN\_L).

The data rate is flexible in CAN FD (CAN with Flexible Data-Rate). When CAN FD is transferring, it is 64 (bytes/per data) and including CRC17/CRC21.

苎 CAN 2.0B/ CA	N FD Settings		×
Setting Channel CAN_	L(Rx) •	CAN_L A0	<ul> <li>Auto detect Data Rate</li> <li>125</li> <li>Kbps</li> <li>(5 Kbps ~ 1 Mbps)</li> <li>Show scale in the waveform</li> <li>CAN FD</li> <li>ISO-CRC</li> <li>Non ISO-CRC</li> </ul>
Color —			Data phase 1000  Kbps Sample Point [80%]
Start of Fr Identifier Data leng Data CRC ACK Slot	pth code	RTR bit SRR bit IDE bit Reserved bit Delimiter bit Error Frame	
Range	·	To Buffer Tail	•
ODefa	ult		✓OK ★Cancel

### Settings

### **Channel Settings:**

CAN\_H/CAN\_L(RX): Can directly measure the stabilized physical layer or the



logic signal converted by the transceiver, the best signal to measure is the logic signal Rx.

### Auto Detect Data Rate:

- I. When checked, the program assists in calculating the data rate.
- II. When unchecked, user can choose the built-in Data Rate setting or input Data Rate by yourself.
- III. The allowable input data rate range is 5Kbps-1Mbps.
- IV. If CAN FD function is checked, this function will be disabled automatically because the Data Rate will be changed.

**Show Scale in Waveform:** When the box is checked, a scale point is displayed on the top of the waveform, which is convenient to check the bit cutting status. This function is not available if CAN FD is checked.

### CAN FD Setting:

**ISO CRC/Non ISO CRC:** User can adjust the rules of ISO CRC analysis and calculation.

### Data Only:

- I. When checked, this function enables you to set the amount of data to be displayed in the analysis report, which can be set from 8 bytes to 60 bytes, and the data outside the set range will be deleted and not be displayed in the report, which is convenient for you to use when you view the report quickly.
- II. When unchecked, all Data will be displayed.

**Report Format:** Check this box to set the width of the data fields to be displayed in the analysis report, which can be set to 8, 16, or 32 bytes. 8 bytes will be displayed when the box is unchecked, and the following is an example of the application:

### Data field width set to 8 bytes.

Frame Type	ID	DLC				C	)ata				CRC(h)
FD Ext Data	01F587D6(07D;187	64	81	82	83	84	85	86	87	88	
			89	8A	8B	8C	8D	8E	8F	90	
			91	92	93	94	95	96	97	98	
			99	9A	9в	9C	9D	9E	9F	A0	

### Data field width is set to 16 bytes.

	Frame Type	ID	DLC									Data	1						
F	D Ext Data	01F587D6(07D;187	64	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90
				91	92	93	94	95	96	97	98	99	9A	9в	9C	9D	9E	9F	A0
				A1	A2	A3	Α4	Α5	<b>A6</b>	Α7	<b>A</b> 8	Α9	AA	AB	AC	AD	AE	AF	в0



Use the CAN\_L(Rx) signal for analysis.

	10. 10. 10. 10. 10. 10. 10. 10. 10. 10.	22 93 94 95 96 97 90 99 24 28 26 37	078 98 MAALADADAAASAGATAIDADAAASAC	IL 4.5. AF 37. 81 82 83 04 85 86 87	8089343E3C3C8E869C0 109	9 1D 1D 1D 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
Label Channel						Search All Fields Text includes
		CRC(h) ASCII(Data)	Information	Frame Duration		
	64 81 82 83 84 85 86 87 88			The order of the o		
2 15:39:06.634	89 8A 88 8C 8D 8E 8F 90					
B 15:39:06.634	91 92 93 94 95 96 97 98					
15:39:06.634.	99 9A 98 9C 9D 9E 9F A0					
15:39:06.634.	A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF B0					
15:39:06.634.	B1 B2 B3 B4 B5 B6 B7 B5					
15:39:06.634.			Data Rate: 1000 Kbps	604.16 us		
15:39:06.635 FD Ext Data 048D2345(123;12345) 64	4 81 82 83 84 85 86 87 88					
15:39:06.635 FD Ext Data 040D2345(123;12345) 64	89 8A 8B 8C 8D 8E 8F 90					
15:39:06.635.         FD Ext Data         048D2345(123;12345)         64           0         15:39:06.635.         1         15:39:06.635.         64	89 8A 8B 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98					
15:39:06.635         FD Ext Deta         048D2345(123)12345)         64           1         15:39:06.635         2         2           1         15:39:06.635         2         2	59 5A 5B 8C 5D 8E 8F 90 91 92 93 94 95 96 97 90 99 9A 98 9C 9D 9E 9F A0					
15:39:04.635     10 Ext Data 048D2345(123;12345) 64     125:39:04.635     125:39:04.635     15:39:04.635	89 8A 88 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98 99 9A 98 9C 9D 9E 9F A0 Al A2 A3 A4 A5 A6 A7 A8					
15:39:06.635         FD Ext Deta         048D2345(123)12345)         64           1         15:39:06.635         2         2           1         15:39:06.635         2         2	59 5A 5B 8C 5D 8E 8F 90 91 92 93 94 95 96 97 90 99 9A 98 9C 9D 9E 9F A0					



# CEC

Consumer Electronics Control, used for transmitting industrial specification AV Link protocol signals to support a single remote control to operate multiple AV machines, is a single-core, bi-directional serial bus.

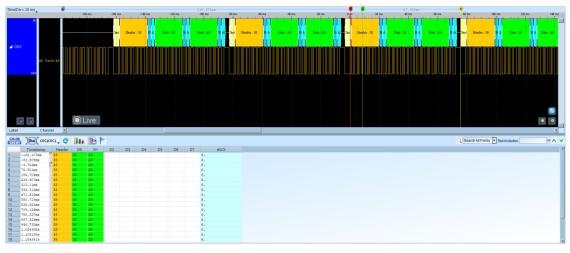
Settings	
🛋 CEC Settings	×
Channel	Color
Channel A0	Start Bit 🔹
Report Format	Header Block 🔹
Default     Advanced	Data Block 🔹
	EOM Bit
Range	ACK Bit
Decode Range	OPCode Block
From To	
Buffer Head 👻 Buffer Tail 👻	ODefault ✔OK ★Cancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

**Report Format:** There are two types of settings, Advanced and Default. The Advanced mode explains the meaning of the Header and OPCode of the waveform.



### Normal



### Advanced

JDiv= 20 ms	-102 ma -160 ma	-140 ms -120 ms -100 ms	. 671ms -80 ms	-83 ma	-40 ma	-20 ma			7.069m.s Dms 10ms	00 ma 100 r	ma 120 ma 146
© CEC A0 Dat		(14) M (22) M (22) M (2) → 21022 B A Shadby B A Dun. A		i III i	Shafby B A		STB1 (3) → 1	· 📊 · ·		9 Ar = 3mr 2101 (0) → 2182 - 8	
CEC								U LI JIII II U U LIU			
15. 15	OLive										
el Channe											•
	iel 🧃									Q Search All Field	ds 🛡 Text includes
		OPCode	D0	D1 D2	D3 D4	D5 D6	D7	ASCII		C Search All Field	
Bus CECICE	lel . EC) . C	Standby (36)	D0 <del>X3</del>	D1 D2	D3 D4	D5 D6	D7 .	ASCII		C Search All Field	
Bus CECICE	Hel ■ EC) C Header STB1 (3) -> STB2 (6) STB1 (3) -> STB2 (6)	Standby (36) Standby (36)	D0 25 23	D1 D2	D3 D4	D5 D6	D7	ASCII		Q Search All Field	
Bus CECICE Timestamp -162.107ms -82.905ms -3.702ms	et 4 EC) C LILE P Header STB1 (3) -> STB2 (6) STB1 (3) -> STB2 (6) (3TB1 (3) -> STB2 (6)	Standby (36) Standby (36) Standby (36)	D0 23 15 25	D1 D2	D3 D4	D5 D6	D7	ASCII		Q Search All Field	
Bus CECICE Timestamp -162.107ms -82.905ms -3.702ms 75.501ms	el 4 EC) C La P Header TE1 (3) -> STE2 (6) STE1 (3) -> STE2 (6) STE1 (3) -> STE2 (6) STE1 (3) -> STE2 (6) STE1 (3) -> STE2 (6)	Standby (36) Standby (36) Standby (36) Standby (36)	D0 29 29 29 29 29 29	D1 D2	D3 D4	D5 D6	07	ASCII		C Search All Field	
Bus CECICE Timestamp -162.107ms -2.905ms -3.702ms 75.501ms 154.704ms	el EC) C IIII I III III TTE (3) → STE2 (6) STE3 (6) → STE2 (6)	Standby (36) Standby (36) Standby (36) Standby (36) Standby (36)	D0 2x 2x 2x 2x 2x 2x 2x 2x 2x 2x 2x 2x 2x	D1 D2	D3 D4	D5 D6	07	ASCII		Q Search All Field	
Bus CECICE Timestamp -162.107ms -82.905ms -3.702ms 75.501ms 154.704ms 233.907ms	el s EG) C III E P TTL (3) → STE2 (6) TTL (3) → STE2 (6)	Standby (36) Standby (36) Standby (36) Standby (36) Standby (36) Standby (36)	00 25 29 29 29 25 25 25 25 25 25 25 25 25 25 25 25 25	D1 D2	D3 D4	D5 D6	D7 - - - -	ASCII		Q Search All Field	
CEC(CE Timestamp -62.107ms -82.905ms -3.702ms 75.501ms 154.704ms 233.907ms 313.11ms	Hele         Header           BTB1         (3) -> 5TB2         (6)           STB1         (3) -> 5TB2         (6)	Standby (36) Standby (36) Standby (36) Standby (36) Standby (36) Standby (36) Standby (36)	D0 29 29 29 29 29 29 29 29 29 25 25 25 25 25	D1 D2	D3 D4	D5 D6	D7 - - - - -	ASCII		Q Search All Field	
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Timestamp           -162.107ms           -82.905ms           -3.702ms           35.501ms           154.704ms           233.11ms           962.312ms           471.515ms           590.712ms	el	Standby (36) Standby (36) Standby (36) Standby (36) Standby (36) Standby (36) Standby (36)	D0 38 49 39 39 39 39 39 39 39 39 39 39 39 39 39	D1 D2	D3 D4	D5 D6	D7 - - - - - - - - - - - -	ASCH		C, Search Al Fiel	
Bask         CECICE           Timestamp         -162.107ms           -162.107ms         -162.107ms           -2.702ms         -162.107ms           -3.702ms         -162.107ms      <	H EC) C III C III FEE (1) → 575 (4) FEE (1) → 5	Standby (36) Standby (36) Standby (34) Standby (34) Standby (34) Standby (36) Standby (36) Standby (36) Standby (36)	00 22 23 24 25 25 25 25 25 25 25 25 25 25 25 25 25	D1 D2	D3 D4	D5 D6	D7	ASCH		C Search All Field	
Year         CECCCE           Timestamp         -62.107m           -62.107m         -63.702ms           -57.02ms         -57.501ms           154.107m         -3.702ms           154.704ms         -3.702ms           23.311ms         -3.702ms           154.107ms         -3.702ms           23.311ms         -3.702ms           90.115ms         -3.702ms           92.312ms         -3.702ms </td <td>H CO CO CO CO CO CO CO CO CO CO</td> <td>5tanSy (34) 5tanSy (34)</td> <td>D0 2.9 2.9 2.9 2.9 2.9 2.9 2.9 2.9 2.9 2.9</td> <td>D1 D2</td> <td>D3 D4</td> <td>D5 D6</td> <td>D7</td> <td>ASCII</td> <td></td> <td>् Search Al Field</td> <td></td>	H CO CO CO CO CO CO CO CO CO CO	5tanSy (34) 5tanSy (34)	D0 2.9 2.9 2.9 2.9 2.9 2.9 2.9 2.9 2.9 2.9	D1 D2	D3 D4	D5 D6	D7	ASCII		् Search Al Field	
Part         CECCCE           Timestamp         -162.107m         **           -162.107m         **         -9.702m         *           -3.702m         *         -7.104m         *           23.507m         313.11m         *         *         *           592.312m         *	HI         Image: second s	Standy (34)	00 23 24 24 24 25 25 25 25 25 25 25 25 25 25 25 25 25	D1 D2	D3 D4	D5 D6	D7	ASCH		Q (Search Al Field	
Phone         CEECCE           Timmestamp         -162.107ms           -162.107ms         -162.107ms           -3.702ms         -163.107ms           3.501ms         -154.704ms           313.11ms         -155.317ms           471.515ms         -150.711ms           471.515ms         -150.711ms           471.515ms         -150.711ms           472.321ms         -150.711ms           473.521ms         -150.711ms           475.521ms         -150.711ms           476.231ms         -150.711ms           476.231ms         -150.711ms           476.231ms         -150.711ms           477.531ms         -150.711		Statey (34)	00 30 37 37 37 37 38 38 38 38 38 38 39 39 39 39 39 39 39 39 39 39 39 39 39	D1 D2	D3 D4	D5 D6	D7	ASCII		Q Seath Al Field	
Basic         CECCC           Trenstamp         -142.107ms           -142.107ms         -142.107ms           -23.907ms         -155.01ms           -37.02ms         -154.07ms           -31.312ms         -154.07ms           -42.307ms         -154.07ms           -42.307ms         -154.07ms           -57.02ms         -154.07ms           -57.02ms         -154.07ms           -57.02ms         -154.07ms           -71.515ms         -150.07ms           -57.52ms         -154.07ms           -704.124ms         -154.07ms           -57.52ms         -54.47ms           -54.52ms         -54.52ms		Statey (3)           Statey (34)	D0 28 84 84 84 84 84 85 85 85 85 85 85 85 85 85 85 85 85 85	D1 D2	D3 D4	D5 D6	D7	ASCII		C Search Al Field	
Phone         CEECCE           Timmestamp         -122.107ms           -122.107ms         -123.005ms           -3.702ms         -154.704ms           23.507ms         -154.704ms           33.11ms         -155.007ms           93.3.11ms         -155.007ms           95.0.12ms         -155.007ms           95.0.212ms         -107.0007ms		<ul> <li>Banky (H)</li> </ul>	00 20 20 20 20 20 20 20 20 20 20 20 20 2	D1 D2	D3 D4	D5 D6	D7	ASCII		C Seach Al Pet	
Phone         CEECCE           Timmestamp         -122.107ms           -122.107ms         -123.005ms           -3.702ms         -154.704ms           23.507ms         -154.704ms           33.11ms         -155.007ms           93.3.11ms         -155.007ms           95.0.12ms         -155.007ms           95.0.212ms         -107.0007ms		Statey (3)           Statey (34)	00 27 27 28 28 28 28 28 28 28 29 29 29 29 29 29 29 29 29 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20	D1 D2	D3 D4	D5 D6	D7	ASCII		Q Search Al Fast	



# **Closed Caption**

Closed captioning is the process of displaying text on a TV or video screen. The text is encoded in the video data stream.

Settings				
🛤 Closed C	aption Settings			×
Setting -				
	Channel	CH 0 🗢		
Color				
-	Clock run-in			-
	Start			•
	Data			•
	Parity			•
Range				
<del>M</del> .	Decode Ra	ange		
<b>₩</b>	From		То	
	Buffer Hea	id 👻	Buffer Tail	•
ODefaul	It		<b>√</b> 0К	*Cancel

LA Channel: Show the selected channel.

ninevO	Jir= 5 US		1	4.1 #	4.1 4	1a -2.1a	4.1		-2.1 #	-2.1 #	-2.1	-2.1 #	-2.1#	4.1#	-2.1 x	-2.1 #	-2.1#	-2.14	4.1#	i
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					12u 14u	1.4 uu 1.4 uu 1.4 uu	1.4 00 4.2 1													
Label		hannel		ive																
(				14 - E		_		_		_		_		_			0		-	1
CH-0				<u>III</u> 🖹													Q Search All Fie	lds 💌 Text includes		
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2	-2.0607414	a 00		00																H
3	-2.0353746	a 00		00																
4	-2.0020078	s 00		00																
5	-1.9606418	00		00																
6	-1.9352742			00																
7	-1.9019074	a 00		00																
8	-1.8685406			00																
9	-1.8351738	s 14		25	.4															
10	-1.801807s -1.7684402	00 oo		00 00																
11 12	-1.7684402			00																
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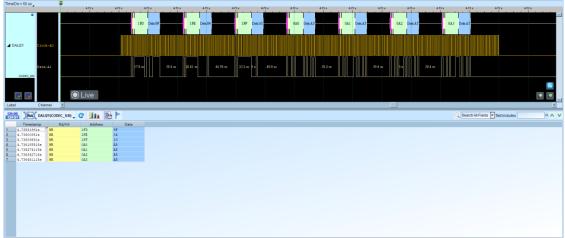
# Codec SSI

Serial Synchronous Interface (SSI) signal used by the codec (CODEC) inside the phone

### Settings

🚐 CODEC_SSI Settings	×
Parameters	Color
Channel	
CLK A0	
Data A1	RD Z V
	WR 🔽 DATA 🔽
Range	
Decode Range	
From To	
Buffer Head 💌 Buffer Tail 💌	
	ODefault VOK XCancel

**Channel:** Set the signal on the DUT to the channel number of the logic analyzer.





# DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings	
苎 DALI2 Settings	×
Parameters	
1	
Data	A0
Color	
Start	•
ShortAddress	•
Group Address	•
Broadcast	•
Special Command	•
Response	•
Stop	•
Range	
Decode Rang	je
From	То
Buffer Head	Buffer Tail
Default	✓OK XCancel

Data Channel: Show the selected channel.



Time/Div=10 ms	2									
DALJ DALJ DATZ-S DALZ Label Channel	(0.11) 29min 0,097	21.71 m	2.4 *	l l l	24.65 m	144 8.7 4.75 Januar 0.097	3.00 × 3.8	* 3.8 * 3.4 (3.1), 12++4 25, 471,824	23 19 mg	27+ 27+ 4 09%) Broats 121_TOEE C
CH-00 Bus DALI(DALI2	. C 🛄 🖹								Q Search All Fields	Text includes
Timestamp	Data(h)	Type	Address		100.00	Description		Information		
1 3,55910753# AL		Special command	Address	(256) TERMINATE = 0		Description		intormation		
2 3.59924867s A5		Special command		(258) INITIALISE = 0						
3 3,639259095# A5		Special command		(258) INITIALISE = 0						
4 3.674471505# A3	TT	Special command			REGISTER (DTR) = 255					-
5 3.71457376s FF	50	Broadcast	A11	(128) STORE DIR AS S	HORT ADDRESS					
6 3.75450423# FE		Broadcast	A11	(128) STORE DIR AS S						
7 3.789710795s FF		Broadcast	A11	(112) REMOVE FROM GR						
8 3.829721285s FF		Broadcast	A11	(112) REMOVE FROM GR						
9 3.064777278 FF 10 3.904787748 FF		Broadcast Broadcast	A11 A11	(113) REMOVE FROM GR (113) REMOVE FROM GR						
10 3.904757749 FF 11 3.939844058 FF		Broadcast Broadcast	A11 A11	(113) REMOVE FROM GR (114) REMOVE FROM GR						
12 3.97905460s FF		Broadcast	A11 A11	(114) REMOVE FROM GR						
13 4.014911565s FF		Broadcast	A11	(115) REMOVE FROM GR						
14 4.054922135# FF		Broadcast	A11	(115) REMOVE FROM GR						
15 4.089979365s FF		Broadcast	A11	(116) REMOVE FROM GR						
16 4.129989905s FF	74	Broadcast	A11	(116) REMOVE FROM GR						
17 4.165047735# FF	75	Broadcast	A11	(117) REMOVE FROM GR						
18 4.20505825s FF		Broadcast	A11	(117) REMOVE FROM GR						
19 4.240116495# FF										
		Broadcast	A11	(118) REMOVE FROM GR						
20 4.280127078 FF	76	Broadcast	A11 A11	(118) REMOVE FROM GR (118) REMOVE FROM GR	OUP 6					



# DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings	i				
🚞 DDC(EI	DID) Sett	ings			×
Paramete	r Setting				
	Channel	Setting			
	SCL	A0	SDA	A0 🌲	
	Address	Mode			
	• 7-E	BitAddressing	3		
	0 8-6	Bit Addressing	g (Include R/W i	n address)	
(	Ignor	e glitch	Statistic	cs Mode	
Color					
Start		•	Read / Write	•	
Stop		•	ACK	-	
Addres	s [	•	NACK	•	
Data		•			
Range					
	Decode I	Range			
From			То		
Buffer	Head	•	Buffer Tail	•	
	(	Oefault	≪ок	Cancel	

SCL: CLK of I<sup>2</sup>C.

SDA: Data of I<sup>2</sup>C.

Address Mode:

7-bit addressing: Show 7-bit addressing



8-bit addressing(Include R/W in Address): Show 8-bit

addressing(include 7-bit addressing and 1-bit Rd/Wr).

**Ignore glitch:** Ignore the glitches occurred due to the slow transitions.

**Statistic Mode:** Collect all the data frames into one report by register address order.

e/Div=100 us	8						10.648#								
		5.49 # 5	48 S.48 S.48 S.48 x	6.49 =	5.49 x	5.49 x	5.49 #	6.49 x 6	5.49 = 5.4	54 5.4		5.49 #	5.49 x	6.49 x	6.49 x
e	17	NA Stop	Wr.40 A 00	A BIAI	A 00	A 77	A PF	4 17	A 77	A 979	A 177		CO A	D4	A 72 A
Bust CH 1 SCI		121.48 to													
CH O SDA	-a		65.42 uu 106.56 uu	46.41 us		95.66 us	97.11 us		95.89 m				0) w 6	9.25 m	
	0	Live													
el Channel	*														
Bus PBus1(D	DC(EDID)) _ C											Q Se	earch All Fields	Text inclu	ides
				EDID Register Na	me				EDID Data			Q Se	earch All Fields	Text inclu	ides 🗌
00 Bus PBus1(D Timestamp 5,495306148	DC(EDID)) C Address(h) A1 (EDID)	Offset(h)		EDID Register Na	me		Ffh		EDID Data			Q Se	earch All Fields	Text inclu	ides
Timestamp	Address(h) A1 (EDID) A0 (EDID)	Offset(h)		EDID Register Na	me		Ffh		EDID Data			Q Se	earch All Fields	Text inclu	ides
Timestamp 5.495306148 5.4961023958 5.496440518	Address(h) A1 (EDID)	Offset(h) Current Addr Rea Sequential Read 0x00	d Offset(00h) Eeader	EDID Register No	me		00 FF FF FF	FF FF FF 00h	EDID Data			Q Se	earch All Fields	Text inclu	ides
Timestamp 5.49530614# 5.496102395# 5.49644051# 5.49644051# 5.497305135#	Address(h) A1 (EDID) A0 (EDID)	Offset(h) Current Addr Rea Sequential Read 0x00 0x08	d Offset(00h) Eeader ID Manufacturer Name	EDID Register Ne	me		OO FF FF FF	FF FF FF OOL	EDID Data			Q Se	earch All Fields	Text inclu	ides
Timestamp 5.495306148 5.4961023958 5.496440518 5.4973051358 5.4975210858	Address(h) A1 (EDID) A0 (EDID)	Offset(h) Current Addr Rea Sequential Read 0x00 0x08 0x08	d Offset(00h) Eeader ID Manufacturer Name ID Froduct Code	EDID Register Na	me		00 FF FF FF ACR 01 84h		EDID Data			Q Se	earch All Fields	Text inclu	ides
Timestamp 5.49530614s 5.496102395s 5.49644051s 5.497305135s 5.497321085s 5.497737655s	Address(h) A1 (EDID) A0 (EDID)	Offset(h) Current Addr Rea Sequential Read 0x00 0x08 0x0A 0x0C	d Offset(00h) Eeader ID Menufacturer Name ID Froduct Code ID Srotal Number		me		00 FF FF FF ACR 01 84h 13 50 42 7A	h				C Se	sarch All Fields	Text inclu	ides
Timestamp 5.49530614s 5.496102395s 5.4964051s 5.497305135s 5.49730505s 5.497377655s 5.49737655s	Address(h) A1 (EDID) A0 (EDID)	Offset(h) Current Addr Res Sequential Read 0x00 0x08 0x08 0x0A 0x0C 0x10	d Offset(00h) Exader ID Manufacturer Name ID Forduct Code ID Serial Number Week and Year of Manufacture		me		00 FF FF FF ACR 01 84h 13 50 42 7A Manufacture					Q Se	sarch All Fields	Text inclu	ides
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Timestamp 5.49530614# 5.496103395# 5.4964051# 5.497305135# 5.49737655# 5.49737655# 5.49737655# 5.49612646# 5.4933509# 5.49849355# 5.49849355#	Address(h) A1 (EDID) A0 (EDID)	Offset(h) Current Addr Res Sequential Read Ox00 0x08 0x00 0x0A 0x0C 0x10 0x12	d Offset(30h) Bader 1D Fondst Code 1D Senial Namber Week and Year of Manufacture DED Version Namber EDD Werision Namber EDD Merision Namber	e or Model Year	me		00 FF FF FF ACR 01 84h 13 50 42 7A Manufacture 01h 03h Analog	h Year = 2011, Wee				Q Se	earch All Fields	Text inclu	ides
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# DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings
🔤 DMX512 Settings 🛛 🗙
Channel
<b>:</b>
Channel
Data
✓ Auto Detect
Baud 250000
Range
Decode Range
From To
Buffer Head 💌 Buffer Tail 💌
ODefault ✔OK ★Cancel

Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

### Result

Use grayscale to display the decode results.

No.       N	erDiv = 50 us	- <b>B</b> -											25.0									
		0.84	60		100 ur			200 ur	250 um		200 ur	260 ur	400 um	460 us	56	10 um	550 un	600 us	650 us	700-ue	790 us	000 us
	Ø	mknown	Data: AE		r.			Date: A1	Des	× 70	Detr 26	Dete: FB	Data 62		Data: EF	Data: A5	Dots: FA	Dots: BB	Deta: B9	Dets: A5	Dets: F0	
Charactic     Control     Control <td>Data-0</td> <td></td> <td>8 u 12 u</td> <td>16 w B</td> <td>9</td> <td>12 u A</td> <td>103 u 163 u</td> <td>a 16 to</td> <td>Bu</td> <td>28.3 w</td> <td>3 12 11 3 11</td> <td>3 w 28 3 w</td> <td>12 u B u</td> <td>12 u 20<i>3</i> us</td> <td>16 to: 20.3 t</td> <td>as B w</td> <td>283 0</td> <td>12 Bū 02a</td> <td>Bujižu</td> <td>) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) )</td> <td>157u 283m</td> <td>12 v 12 u 163 u</td>	Data-0		8 u 12 u	16 w B	9	12 u A	103 u 163 u	a 16 to	Bu	28.3 w	3 12 11 3 11	3 w 28 3 w	12 u B u	12 u 20 <i>3</i> us	16 to: 20.3 t	as B w	283 0	12 Bū 02a	Bujižu	) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) )	157u 283m	12 v 12 u 163 u
Normal Data         Obs         Ob		O	) Live																			
Note:         State         O         O         D	Channel	•																				
171.000         101.0000         101.0000		512) _ C																	Q Sea	rch All Fields 👻	Text includes	DX
Stock       Other       Stock       Stock <th< td=""><td></td><td></td><td></td><td></td><td>D4</td><td>05 06</td><td>07 0</td><td>4 09</td><td>D10 D</td><td>11 012</td><td>012 01</td><td>4 D15</td><td>Inform</td><td>ation</td><td>_</td><td></td><td></td><td></td><td>Q Sea</td><td>rch All Fields 💌</td><td>Text includes</td><td>a .</td></th<>					D4	05 06	07 0	4 09	D10 D	11 012	012 01	4 D15	Inform	ation	_				Q Sea	rch All Fields 💌	Text includes	a .
21.4may	Bus DMX(DMX)	State			D4	D5 D6	D7 D	8 D9	D10 D	11 D12	D13 D1	4 D15	Inform	ation					Q Sea	rch All Fields 👻	Text includes	Di
111000       110000       <	Timestamp	State			D4	D5 D6	D7 D	8 D9	D10 D	11 D12			Inform	ation					QSea	rch All Fields 👻	Text includes	Di
$\begin{array}{                                    $	Dimestamp         Timestamp           -75.35us         Hg On           350ns         Id           16.6us         DI	State iknown lle 0:15]			D4	D5 D6	D7 D						Inform	ation		_			QSea	rch All Fields 👻	Text includes	α.
1.1054m     01.111     12     64     71     70 </td <td>Timestamp           -75.35us         % 0n           350ns         Id           16.6us         D(           720.9us         D(</td> <td>State           iknown           ile           0:15]           16:24)</td> <td></td> <td></td> <td>D4</td> <td>D5 D6</td> <td>D7 D 78 27</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>Inform</td> <td>ation</td> <td></td> <td></td> <td></td> <td></td> <td>Q Sea</td> <td>rch All Fields 💌</td> <td>Text includes [</td> <td>DA</td>	Timestamp           -75.35us         % 0n           350ns         Id           16.6us         D(           720.9us         D(	State           iknown           ile           0:15]           16:24)			D4	D5 D6	D7 D 78 27						Inform	ation					Q Sea	rch All Fields 💌	Text includes [	DA
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1.4755400       1040000       1	Description         OMX(DMX2           Timestamp         -75.35us         ig Un           -75.35us         ig Un         350ms           14.4us         D1         120.9us         D1           1.1005sm         D1         1.1005sm         D1           1.0005sm         D1         1.0005sm         D1           1.0005sm         D1         2.6695ms         D1           2.6005sm         D1         2.5005sm         D1	State known (16:24) 2 (16:24) 2 (16:24) 2 (16:31) (16:31) (16:31) (16:32:47) (16:35)			D4 A1 77 59 54 81 59 50 87	D5 D6	07 D 78 E 27 S 86 S 33 S 89 DE						Inform	ation					Q Sea	rch All Fields 👻	Text includes [	Part and a second se
3.6456m     9.041     Mar	Ont         Date         OMAX(DAXX)           Timestamp         -75.35us         % 07.35us           -75.35us         % 07.35us         % 07.35us           16.4us         Di         1.116ms           1.116ms         Id         1.1199ms           1.1169ms         Di         1.116ms         Id           1.1199ms         Di         2.2499ms         Di           2.5609ms         Di         3.47225ms         Di           3.40735ms         Id         3.4735ms         Id	State           kmown           lle           0:15]           if::24]           r::6:24]           r::6:31]           32:47]           48:56]           le			D4 A1 77 50 57 50 81 60 77 00 27 00 24	D5 D6	D7 D 78 5 57 5 88 5 33 55 83 75						Inform	ation					C Sea	rch All Fields 💌	Text includes (	P
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	Date         Date         Date           Trenetary         Trenetary           -73. 350:a         10           350:a         10           350:a         10           140. 50:a         10           150:a         10           140. 50:a         10           1.10 ms         10           1.10 ms         10           1.10 ms         10           1.260 Stan         0           1.276 Stan         0	State           kmown           le           00103           16:243           21           kmown           00153           16:243           23:471           16:563           le           kmown           00163           le           kmown           0010           le           kmown           10:151           16:201	D0 D1		3.1 77 56 57 59 89 10 77 03 24 37 70	D5 D6	D7         D           FB         E           Z7         E           BB         E						Inform	ation					Q Sea	rch All Fields 🖉	]Text includes [	



# DP Aux Ch

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard. (Support DP 2.1, eDP 1.5)

ettings				
DP AUX CH Settings				
ttings		С	olor	
Channel		(		
			Request	-
Aux	AO	<b>\$</b>	Reply	•
Analysis Mode			CMD	<b>•</b>
Mode	DP_Aux	•	Address	•
Aux Option			Data	•
Startup Transaction	Request	-	Stop	•
Show DPCD		R	ange	
• DP Version	1.4a	-		
🔿 eDP Version	1.2	-	From	То
DPCD 00108}	86/106	-	Buffer Head	▼ Buffer Tail ▼
Show EDID				
SHOW EDID				
		[	Oefault	✓OK XCancel

Channel: Set the channel to decode

Show DPCD: Show the Display Port Configuration data. Enable when checked.

- I. DP Version supported to 2.1
- II. eDP Version supported to 1.5
- III. DPCP 00108h: 8b/10b or 128b/132b encoding options are available.

Mode: Choose the mode DP\_Aux / HPD / PWR

Show EDID: Show the EDID information. Enable when checked.

Startup transaction: Set the transaction type of the first frame

Reply Timeout: Set the value of timeout



### Without the DPCD information

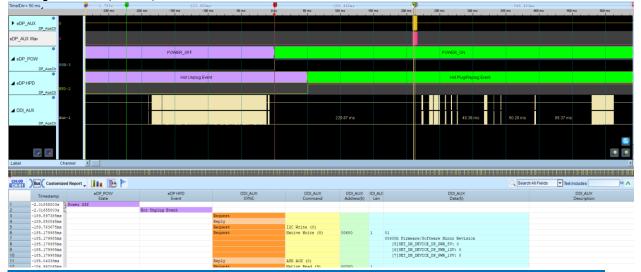


### Show the DPCD information

me/Div= 200 us	277.99 ms	278.08 ms 278.27 ms	278.46 ms	278.85 ms 278.84 ms	275.315ks 279.03 ms 279.22 ms 279.	41 ms 279.61 ms 279.8 ms	278.99 ms	290.10 ms 2	90.37 ms	210.56 ms	290.75 md
ال مربع من	21	17 0	- 57 0 571 - - 70.5 - 7	27 0) 7 5 a			581.5 to	51 	ay 11.05 • 70.	5 m	70.5 m
abel Channe	el I							05		Text includes	
Bus AUX(DE	P_AuxCh) _ 😋 🚺 🚺 🏴										EX A
										Text includes	
Timestamp	SVNC	Command	Address(h)		Data(h)	Descriptio	1	Data rate	earch All Fields Error	Text includes	
Timestamp 270.63415ms			Address(h) 00103 4	38 38 38 38		Descriptio	ı			Text includes	
Timestamp 278.63415ms 278.63415ms	SVNC	Command		38 38 38 38 00103h TRAINING_LANE0_SR	E7		1			Text includes	
Timestamp 278.63415ms 278.63415ms 278.63415ms	SVNC	Command		38 38 38 38 00103h TRAINING_LANE0_SU (1:0)VOLTAGE SWING SU	ET ET: 0	Descriptio Voltege swing level 0	1			Text includes	
Timestamp 278.63415ms 278.63415ms	SVNC	Command		30 30 30 30 30 00103h TRAINING_LANE0_SI [1:0]VOLTAGE SWING SI [2]MAN_SWING_REACHED [4:3]FRE-EMPHASIS_SE	ET ET: 0 1: 0 T: 3		1			Text includes	
Timestamp 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms	SVNC	Command		38 38 38 38 00103h TRAINING_LANE0_SU [1:0]VOLTAGE SWING SU [2]MAX_SWING_REACHED [4:3]FRE-EMFERSIS_E [5]MAX_FRE-EMFERSIS_]	ET ET: 0 1: 0 T: 3 FRACHED: 1	Voltage awing level 0	1			Text includes	
Timestamp 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms	SVNC	Command		28 38 38 38 00103h TRAINE_LANE0_S1 (110)V0LTAGE SKING 38 (2)MAX_SWING_REACHED (4:3)FRE-EMPRASIS_E (5)MAX_FRE-EMPRASIS_ 00104h TRAINISE_LANE1_S1	ET ET: 0 1: 0 T: 3 REACHED: 1 ET	Voltage swing level 0 Fre-emphasis level 3	1			Text includes	
Timestamp 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms	SVNC	Command		38 38 38 38 00103h TRAINING LANED_SI (110]VOLTAKE SHING SI (2)MAX_SHING FRACHED (4:3)FRF_EMPHASIS_SE (5)MAX_FRF_EMPHASIS_ 00104h TRAINING_LANEL_SI (110)VOLTAKE SHING SI	ET ET: 0 1: 0 7: 3 REACHED: 1 ET: ET: 0	Voltage awing level 0	1			Text includes	
Timestamp 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms	SVNC	Command		38 38 38 38 00103h TRAINING LANEO_SI (1:0)VOLTAGE SWIDG 38 (2)MAX_SWIDG REACHED (4:3)FRE_EMERASIS_3 (5)MAX_FRE_EMERASIS_3 00104h TRAINING LANEI, SI (1:0)VOLTAGE SWIDG 33 (2)MAX_SWIDG, REACHED	ET ET: 0 1: 0 Tr 3ED EEACED: 1 ET ET ET: 0 1: 0	Voltage swing level 0 Fre-emphasis level 3 Voltage swing level 0	1			Text includes	
Timestamp 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms 278.63415ms	SVNC	Command		38 36 36 36 36 00103h TRAINING_LANED_SI (1:0)VOLTARE SWING 31 (2)NAL_SWING_SYLNED (4:3)PRE-EDERASIS_SE (5)NAL_PRE-EDERASIS_SE (1:0)VOLTARE_SWING 31 (1:0)VOLTARE_SWING (2)NAL_SWING_STATES) (4:3)PRE-EDERASIS_SE	ET ET: 0 1: 0 T: 3 PEACED: 1 ET: ET: 0 1: 0 1: 0 1: 3 T: 3	Voltage swing level 0 Fre-emphasis level 3	1			Text includes	
Timestamp 278.4315m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m 278.63415m	SVNC	Command		38 38 38 38 00105h TRAINING LANGO, SI (10)VOLTANG: SHIDB S (2)MAX, SHIDB, REALING (4) 3]FRE-EMERATIS_FE (5)MAX, FRE-EMERATIS_FE (10)VOLTANG SHIDB S (2)MAX, SHIDB, REALEMENTS (2)MAX, SHIDB, REALEMENTS (4) 3]FRE-EMERATIS_FE (5)MAX, FRE-EMERATIS_FE	ET ET: 0 1: 0 REACHED: 1 ET ET: 0 1: 0 T: 3 REACHED: 1	Voltage swing level 0 Fre-emphasis level 3 Voltage swing level 0	1			Text includes	
Timestamp           270.43415ms	SVNC	Command		34 35 36 36 00103h TRAINING LANEL SI (110)VOLTAKE SWING 38 (21)MAL SWING RACHED (41)JDAL SWING RACHED (51)MAL RE-BERNASTS (51)MAL RE-BERNASTS (110)VOLTAKE SWING RACHED (41)JEK-BERNASTS (51)MAL RE-BERNASTS (51)MAL RE-BERNASTS	ET ET: 0 1: 0 T: 3 ET: 2 ET: 0 1: 0 T: 3 FEACHED: 1 ET: 5 FEACHED: 1 ET: 5 FEACHED: 1 ET: 5 FEACHED: 1	Voltage swing level 0 Pre-emphasis level 3 Voltage swing level 0 Pre-emphasis level 3	3			Text includes	
Trmestamp           277.43415ms           278.43415ms           277.43415ms           278.43415ms           278.43415ms	SVNC	Command		38 38 38 38 38 01035 TRATING LARED 51 (110)VOLTAGE WITH 58 (21)WAY STRUES (21)WAY	ET ET: 0 1: 0 T: 3 ET: 5 ET: 5 E	Voltage swing level 0 Fre-emphasis level 3 Voltage swing level 0	1			Text includes	
Timestamp           278.63415ms           6 278.63415ms           727.63415ms           278.63415ms           278.63415ms	SVNC	Command		38 38 38 38 001035 TRAITING LANED 51 (110)VOLTAGE 991105 51 (140)VOLTAGE 991105 52 (141)FRR-DEPRASTS 55 (10045 TRAITING LANEL 51 (10045 TRAITING LANEL 51 (10045 TRAITING LANEL 51 (10045 TRAITING LANEL 51 (10055 TRAITI	ET ET 0 ET	Voltage awing level 0 Fre-emphasis level 3 Voltage awing level 0 Fre-emphasis level 3 Voltage awing level 0	1			Text includes	
Timestamp           277.4315m           278.4315m           278.4315m           278.4315m           278.4315m           278.4315m           278.4315m           278.4315m           277.4315m           278.4315m           277.4315m	SVNC	Command		10 30 30 30 010357 REALITING_LANGU_SI (1:0)VOLTAGE SWITES SI (1:0)VOLTAGE SWITES SI (1:0)VOLTAGE SWITES (1:0)VOLTAGE SWITES (1:0)	ET 0 ET 0 T: 0 T: 3 ET 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Voltage swing level 0 Pre-emphasis level 3 Voltage swing level 0 Pre-emphasis level 3	1			Text includes	
Trmestamp           277.43415ms           278.43415ms           278.43415ms           277.43415ms	SVNC	Command		38 38 38 38 001035 TRAITING LANED 51 (110)VOLTAGE 991105 51 (140)VOLTAGE 991105 52 (141)FRR-DEPRASTS 55 (10045 TRAITING LANEL 51 (10045 TRAITING LANEL 51 (10045 TRAITING LANEL 51 (10045 TRAITING LANEL 51 (10055 TRAITI	ET () () () () () () () () () ()	Voltage awing level 0 Fre-emphasis level 3 Voltage awing level 0 Fre-emphasis level 3 Voltage awing level 0	,			Text includes	

#### Accessories:

https://www.acute.com.tw/en/product/detail143



### Analysis Aux, HPD, PWR



### eSPI

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings				
🚐 Enhanced SPI (eSPI) Pa	rameter Settings			×
Channel Settings				
CS#	A0	SCK	A1 🗘	Advanced Decode Settings
I/O 0	A2 🌲	I/O 1	A3 🌲	Show RAW Byte Only
I/O 2	A4 🌲	I/O 3	A5 🌲	Show Configuration Detail
Alert	A6	Reset#	A7	Show Status Bit Def.
Enable Glitch F	ilter			Show VWire Detail
	CS Work Mode	Active Low	•	Show EC/KBC Command
Re	sponse latched on	Clock Falling	•	Show RPMC Detail
Startup Settings				Reduced Report
	I/O Mode Setting	Auto	•	Default Display -
	Default Alert Mode	From I/O[1]	•	PUT_PC V
✓ Auto-select pro	tocol timing by cloc	k speed		GET_PC
Command desel	ect time 💶		50ns	PUT_NP
Clock LOW to out	put valid 💶		15ns	GET_NP
✔ Pop-up Messa	geBox when found	CRC mismatch(es	5)!	
Color				
<b>••</b>	OpCode	•	Ad	ddress 🗾 👻
Cy	cle Type	•		Data 🗾
	Tag	•	Res	ponse 🔹
	Length	•		Status 🔹
Range				
Decode Range	•			
From		То		
Buffer He	ead	<ul> <li>Buffer Tail</li> </ul>	•	
Default				OK Cancel

### 0 - 11:

### **Channel:**

CS#:

Chip Select (Active Low)



SCK:ClockI/O0 – I/O3:Data input / outputAlert:Alert signal (Optional)Reset:Reset signal (Optional)

### Startup Settings:

I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I /

O state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

**Command deselect time:** Set tSHSL, Chip Select# Deassertion Time.

**Clock LOW to output valid:** Set tCLQV, Output Data Valid Time.

### Advanced Decode Setting:

Show Configuration Detail: Show details of SET\_CONFIG / GET\_CONFIG. Show Status Bit Def.: Show details of Status.

Reduced Report: Reducing the report is easy to check the Command Flow. Filter Setting: To show or hide the specific OP Code / Cycle Type or Address range in the report.

**Note:** The setting of Address Filter would be saved as LA\eSPI\eSPIFilterX.bin in the work directory.

ne/Div=1us, 🎔	17.16 ur	10.06 uz 18	.08 ur ::	23.05 uz	21.06 us		2.06 uz		16 uz		02.232 M us	25.05 us	28.06 us	27.86 uz	28.86 us		2.86 us	33.06 us	31.08	ur 32.66 s	
auired: 10:01:35.176				22.00 Gi	11.00 04					<sup>.</sup>		20.00 01	20.00 0					30.00 00			·
•																					
	0BT 00 20	CRC TU RESI 00 07	00 00 SIS S	IS CRC (AP)	SET	00 20	01 00	07 00	CRC TU	REFISTS	SIS CRC (	0	ST 00 20	CRC IN RES 00 0	77 00 00 ST	STS CRC	(AF)	SET 00	20 01 00	07 00 CRC TUR	EE SIS SIS
			1																		
CS#-0								3.98 12													
CS#-0								3.96 (8													
	nnnnn			nnn														nnnn			
SCR-1					845 ns							940 ns					845 xc				
										յասս						JUUUUL					
							1	Π		Г	1		7		Π	חחר		п			
BUS_eSPI I/0 0-2	400 as		665 as				395 1	as   400 n	a 405 na	400 as	735 at	400 ж			665 as			925 w	395 xe	400 m 405 ns 4	00 xe
											ᆛᆮᆮ										
1/0 1-3	465 m 400 m		665 m 2	70 a 790 m		100						85 m 485 m	400 as		665 au	770 a 77	80 m	M1 -		1.21 w	270
170 1-3	400 III 400 III		007.00	700 10		10.7					~ "     <sup>2</sup>	57 M 167 M	100 10		007.8	101 /		000 M		1.21 %	- I ľ"
											ᅮ⊢			Π		┑└─┌					
1/0 2-4		1.06 w	665 as	400 as 650 :							400 xzs	870 m	935 as	1.06 us	665 as	400 as	650 m			1.21 us	
																					L
1/0 3-5																					
45P1																					
	<u></u>																				_
<b>PC PC</b>	OLive																				<b>.</b>
abel Channel 4																					
				_	_	_	_	_	_	_	_		_			_	_		_		_
Bus BUS_eSPI(eSPI	) - C 🛄 📑																	Search All Fie	elds 🔻 Text	includes	EX
tamp (hh:mm:ss.ms	OpCode/Response	CycTyp	04	Tan LEN	Address	D0 D	1 D2	D3 D4	D5 0	D6 D7	ASCII	Status	CRC		Memo						
10:01:35.179. AC												0107	30								
	T_CONFIGURATION(21)				0020								CB								
10:01:35.179. AC							00					0107	λř								
10:01:35.179. SE 10:01:35.179. AC	T_CONFIGURATION(22)				0020	01 00	07	00				0107	01								
	T CONFIGURATION(21)				0020								Ci								
10:01:35.179. AC						00 07	00	00				0107	28								
10:01:35.179. 52	T_CONFIGURATION(22)				0020		07						01								
10:01:35.179. AC												0107	30								
10:01:35.179 GE	T_CONFIGURATION(21)				0020								CB								
10:01:35.179. AC	CEPT(08) T_CONFIGURATION(22)				0020		00					0107	A.2								
0 10:01:35.179. AC					0020	01 00	07	00				0107	30								
	CONTRACTOR (DI)				0030								-								



# FlexRay

FlexRay is an in-vehicle communication network standard that supports two communication channels, each with a speed of up to 10 Mbps.

Setting				
	Channel		✓ Auto detect E	)ata Rate
0- <i>4</i>	Communication Data (RxD	RxD A0	0.00     (1 Mbps ~ 20	- Mbps Mbps)
			FlexRay Channe	el
			Channel A	-
olor			Show scale	in the waveform
	Indicator Bits	•	700	
	Frame ID	• •	TSS	· · · · · ·
	Payload Length		BSS	•
	Header CRC		FES	•
	Cycle count Data		DTS	
		-	WUS	<b></b>
	CRC	•	CAS/MTS	-
			Error	
Range				
Decode	Range			

Channel: Set the channel, Communication Data (TxD)

**Communication Data (TxD):** The TxD data is from the TxD and TxEN of the FlexRay transceiver.

**Communication Data (RxD):** The RxD data is from the RxD and RxEN of the FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.FlexRay Channel: Channel A or B, for Frame CRC checking.



#### Errors are:

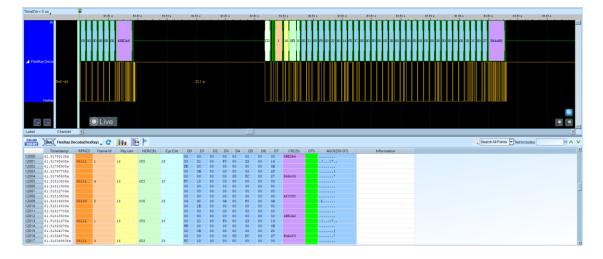
Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

### Abbreviations are:

Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol
WUP	Wakeup Pattern
CID	Channel Idle Delimiter

### Result

10Mbps FlexRay Communication Data(RxD)





# HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

ettings			
HD Audio Settings			
etting			
-			
:7			
SYNC	CH 0	I/O 0	CH 3
BCLK	CH 1	\$	Direction
DODA	CHI	<b></b>	O SDO 💿 SDI
olor			
Stream Data			
Preamble		✓ Stream ID	
Length		<ul> <li>Sample</li> </ul>	<b></b>
Response (SDI)			
Valid		▼ UnSol	•
Reserved		<ul> <li>Response</li> </ul>	•
Command (SDO)			
Reserved		▼ CAd	•
NID		<ul> <li>Verb ID</li> </ul>	<b>•</b>
Payload		Ŧ	
ange			
Decode Rang	le		
		То	
From			

Channel: Show the selected channel.



**Direction:** Determines whether the I/O data decoding is SDI or SDO; this selection affects the rules of the analysis and causes the color-coded options in the lower field to change.

Div= 500 ns			165.95 us	167.42 us	147.0	aus .	199.38 vr		169.05 us		169.33 us		19.01 us	171	.29 us	170.77		171.24 us		171.72 us	172.2	4	172.67 us	173.15	45	173.)	63 us	174.11 us	
0		X 99 0		Response:00	000000		0 Leng	<mark>a.00</mark> Sam	apde:00	Sample (00	Şanşk	100 Sam	up36:00	Sample:00	Sample 9	0 Sample	:00 3an	gle:00 Sa	unple:00	Supple:00	Sample 00	Sample 0	) Sample (	0 Sample)0	) San	12 of all	Sample:00	0 Sample D	0 Sample
	SYNC-A1	165 m	670 au	$\Box$																									
Bus	BC1K-AO																												
HD Audo	SDI-A2			100 000 000 0	1000000	0000000	10000000	10000	00000	000000	1000000		00000			000000	000000		000000				1000 0000	0000000			000000	00000000	00000
0		X FF 00	0 MD SC VI	D0 E 1 3	RC 4D	4A FF	49 A.D	00	00 00	00	00 00	00	00 0	00	00 00	00 00	00	00 00	00 0	0 00	00 00	00 00	00 00	00 00	00	00 0	00	00 00	00
	SVIIC-AL	165 m																											
Bus	BC1K-AO																												
HD Audio	SD0-A3			12	5	165 ni																							
5 <b>I</b> V			Live																										
	Channel	Ŧ						_		_		_					_		_							_			_
Bus	SDO_Bus(	(HD Audio) 🚽 🤇		8 🕨																				Q Search	All Field	ts 💌 Te	ext include	15	
-875.0	estamp	Frame Sync	Reserved	CAd	NID		VID			Payload	Str	ream Tag				Sample													
-875.0		m	00	0	00	0					1			00 00 9															
-868.6													00 00					00 00 00											
-866.0													00 00	0 00 00 0	0 00 00 0	0 00 00	00 00 00	00 00 00											
-063.3													00 00					00 00 00											
											_			0 00 00 0															
-860.6											_			0 00 00 0		0 00 00	00 00 00	00 00 00											
-858.0					00								00 00 FF 60					00 00 00											
-858.0																		00 00 00											
-858.0 -855.3 -854.2	12.9	FF	00	×																									
-858.0	us Jus	FF	00	Ŭ.							_		00 00					00 00 00											
-858.0 -855.3 -854.2 -850.5	3us 3us 65us	IT	00										00 00		0 00 00 0	0 00 00	00 00 00												
-858.0 -855.3 -854.2 -850.5 -847.8	12.8 312.8 16512.8 12.8	π	00	v									00 00	0 00 00 0	0 00 00 0 0 00 00 0	0 00 00	00 00 00 00 00 00	00 00 00											



# HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

### Settings

📥 HDLC Settings	×
Parameters	Color
	Flag  Address
Channel Setting	
Data 🗛	Control
	I-Frame
Option	S-Frame
Mode NRZI-0 -	U-Frame
Parity Low -	Information -
Baud Rate 9600 -	FCS
Address Bits 8	Range
Control Bits 8	inni
FCS Bits 16 -	Decode Range
Order LSB -	From To Buffer Head
	ODefault ✔OK ★Cancel

HDLC: Set the channel of the signal.

Option: Start up Setting of signal analysis

- I. Mode: Choose the analysis method.
- II. Parity: Set Parity (High / Low)
- III. Baud Rate: Set Baud rate



- IV. Address Bits: Set the length of Address Bits.
- V. Control Bits: Set the length of Control Bits.
- VI. FCS Bits: Set the length of FCS (Frame Check Sequence) Bits.
- VII. Order: Bit order of transmission.

A de 3 <sup>°</sup> A de 3	Addr 37 Colds CS B5 C5 B5 C1 C2 B7	imelDiv=1 ms	*	1.12 ms	10.12 ms	11.12 ms	12.12 ms	10.12 ms	14.12 ms	20. 15.12 ms	542ms 10.12 ms	17.12 ms	10.12 ms	19.12 m		.12 ms 3	1.12 ms	22.12 md	23.12	- <b>X</b>	. 12 ms
	2479 037.5 cs 037.5 cs 037.5 cs 037.5 cs 037.5 cs 027.5 cs 027.	•								l i i i											
다	0100 (00 1900.0, 0 ) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	DATA-0		937.5 us	937.5 us	937.5 us	937.5 us	937.5 us	625 us						625 us	937.5 u	8 937	:5 us			
Timestamp Flag Address CTRL Frame N(S) S/C.Code P/F N(R) R.Code Data FCS Flag.End Reserved	Timestamp Rag Address CTRL Frame N(S) S/C Code P/F N(R) R Code Data FCS Rag End Reserved																				• •
																				1	
					RI Frame	N(S) S	C Code P/F	N/R)	B Code		Data				EC'S	Flag Fod	Reserve		<b>奖擘所有欄位</b> ▼	)文字包含	D A



# HDQ

Developed by TEXAS INSTRUMENTS for battery management display applications, primarily in consumer electronics, HDQ is available in two data width formats, 8-bit and 16-bit, with a fixed 7-bit address. An HDQ packet mainly consists of Break, 7 bits Address, 1 bit R/W and 8 bits Data or 16 bits Data. The transmission method is LSB (Least-significant bit) to MSB (Most-significant bit), and the maximum transmission rate is 5 Kbit/s. The maximum transmission rate is 5Kbit/s.

### Settings

🛤 HDQ Settings	×
Channel	Color
Set The HDQ Channel 🛛 🗍	Break
Show Battery Information	Break Recovery
IC Model	Address 🔹
bq27000 bq27010	Read
bq27510 bq27541	Write
bq27541-V200 bq27546-G1	Data 💌
	Range
	Decode Range
	From To
Inverse Waveform (IDLE Low)	Buffer Head 👻 Buffer Tail 👻
	ODefault ✓OK ★Cancel

Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.

Invese Waveform (IDLE Low): Invert the waveform. Enabled when



### checked.

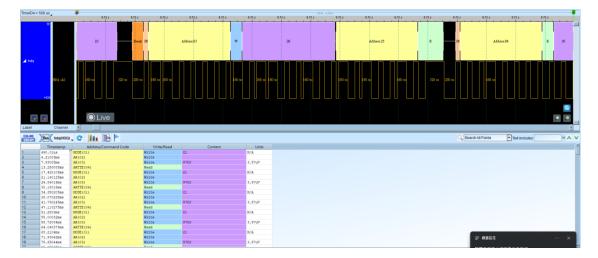
### Result

Write: Indicates that the data is written and followed by the data.

**Read:** Read Indicates that the data is read, followed by the data.

ime/Div= 500	0 us									1355							
			6.72 s	6.72 s	6.72 s	0.72 s	6.73 s	6.73 s	6.73 s 6.73 s	6.73 4	6.73 s	6.73 s	6.73 s	6.73 s	6.73 s	6.70 s	6.73 s
▲ hdg	•		23	Book 3R		Aðtæs:DJ	π		25		Aðtmu:25		R	3R		88.04	R
	100 Q - A.O		160 w	320 m 200 m	160 us 160 us		260 m	160 m 11	160 w	160 vs	160 m	160 w	)20 m	200 10	160 vs		
	_		O Live														
	Channel			• • • • • • • • • • • • • • • • • • •										Q Sea	rch All Fields	Text include	
Label	Bus hdq(HDQ)	_			Wee Band			1100	to farmation					Q Sea	rch All Fields	Text include	
abel 24.00 X	Bus hdq(HDQ)	C		d Code	Write/Read		Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
87 6	Bus hdq(HDQ) Timestamp	. C		d Code	te	23	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
bel 1101 X 87 6 88 6	Bus hdq(HDQ) Timestamp .72545862s .729178645s	C 02 03		d Code Wri Wri	te te		Data/Content	Units	Information					C Sea	rch All Fields	Text include	
100 X 101 X 17 6 18 6 19 6	Bus hdq(HDQ) Timestamp .72545862a .729178645a .73237866a	02 03 25		d Code Wri Wri Rea	te te	23 26	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
bel 1001 X 101 6 18 6 19 6 90 6	Bus hdq(HDQ) Timestamp .72545862s .729178645s .73237866s .734498675s	02 03 25 04		d Code Wri Rea Rea	te te d d	23 26 30	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
87 6 88 6 89 6 90 6 91 6	Bus hdq(HDQ) Timestamp .72545862a .729178645a .73237866a .734498675a .7386687a	02 03 25		d Code Wri Rea Rea Wri	te te d d te	23 26 30 21 23	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
bel 101 X 101 X 10 X 101 X	Bus hdq(HDQ) Timestamp .72545862a .7291786458 .73237866 .732469675a .7386667a .74230072a	02 03 25 04 01		d Code State Mail Rea Rea Mail Mail Mail	te d d te te	23 26 30	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
bel 100 X 101 X 87 6 88 6 99 6 90 6 91 6 92 6 93 6 93 6 94 6	Bus hdq(HDQ) .72545862s .72545862s .725478665s .732378665 .7386687s .7386687s .74830872s .74810874s	02 03 25 04 01 02		d Code Wri Rea Rea Wri	te d d te te	23 26 30 21 23 26	Data/Content	Units	Information					QSea	rch All Fields	Text include	
87 6. 88 6 99 6 90 6 91 6 92 6 92 6 92 6 94 6 95 6	Bus hdq(HDQ), Timestamp 72545862a 7259176645a 732370666 732458675a 7386687a 74230675a 74610874a 74610874a 74610874a 751422077a	02 03 25 04 01 02 03 25 04		d Code	te d d te te te d d d	23 26 30 21 23 26 30	Data/Content	Units	Information					C Sea	rch All Fields	Text include	
bel 100 X 100 X 87 6 88 6 99 6 90 6 90 6 91 6 92 6 93 6 93 6 94 6 95 6 96 6 96 6 96 6 96 6 96 6 96 6 96 6 96 6 97 6 99 6 99 6 99 6 99 6 90 6	Bus hdq(HDQ) Timestamp 72545862a 729176645a 733378665 733458675a 734498675a 74430876a 74430876a 74430876a 755598755a	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01		d Code Ver Ver Rea Ver Rea Ver Ver Rea Rea Rea Rea Rea Rea Rea Rea Rea Rea	te d d te te d d d te	23 26 30 21 23 26 30 21	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
Hoto         X           87         6           88         6           90         6           91         6           92         6           93         6           94         6           95         6           96         6           97         6	Bas hdg(HDQ), Timestamp .72545862s .72545862s .73337665s .73337665s .7334667s .7346667s .7346667s .74610874s .74610874s .74610874s .75631815s	02 03 25 04 01 02 03 25 04 01 02 04 01 02		d Code	Ce Ce Ce Ce Ce Ce Ce Ce Ce Ce Ce Ce Ce C	23 26 30 21 23 26 30 21 23 21 23	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
Hoto         X           87         6           88         6           90         6           91         6           92         6           93         6           94         6           95         6           96         6           97         6           98         6	Mag(HDQ) Timestamp 72545862a 729178645a 732379666 734498075a 734498075a 73449075a 74410874a 74410874a 74510874a 755598795a 755310815a	02 03 25 04 01 02 03 25 04 01 02 03 02 03		d Code Ver Ver Rea Rea Rea Rea Rea Rea Rea Rea Rea Rea	te d d te te te te te te te te te	23 26 30 21 23 26 30 21	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
B         C         C           87         6         88         6           89         6         90         6           91         6         92         6           92         6         94         6           95         6         6         96           97         6         99         6           98         6         99         7	Bas hdg(HDQ), 72545862s 72545862s 72817664s 73849675s 73449675s 73449074s 74510074s 74510074s 755596795s 755596795s 75531015s 766230855s	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25		d Code Ver Res Res Res Res Res Res Res Res Res Res	Co Co Co Co Co Co Co Co Co Co Co Co Co C	23 26 30 21 23 26 30 21 23 26	Data/Content	Units	Information						rch All Fields	Text include	
Hot         Hot           1101         X           1101           1	Ban hdg(HDQ) Timestamp 72545862a 725176645a 734459675a 734459675a 74430676a 74430076a 75542077a 75542077a 75542077a 75542075a 76503084a 76603084a 766030857a	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04		d Code 422 Maria Rea Maria Rea Maria Rea Rea Rea Rea Rea Rea Rea Rea Rea Re	50 50 51 52 50 50 50 50 50 50 50 50 50 50 50 50 50	23 26 30 21 23 26 30 21 23 26 21 23 26 30	Data/Content	Units	Information					Q Sea	rch All Fields	Text Include	
Hot         Hot           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100           1100         1100	Res hdg(HOQ) Timestamp .72545862a .72517665s .732370668 .73436675a .7345067a .74510874a .74510874a .755589795a .755589795a .75630804a .76630805a .76630805a	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 03 25 04 00 25 03 25 04 00 25 00 25 0 25 0 25 00 25 00 25 00 25 00 25 0 2 0 2		d Code	ce d d ce ce d d ce ce ce ce ce ce ce ce ce ce ce ce ce	23 26 30 21 23 26 30 21 23 26 30 22 26 30 21	Vata/Context	Units	Information				_	Q Sea	rch All Fields	Text include	
abel 21-00 21-	Ban hdg(HOQ) Timestamp 72545962a 725479645 732379645 732379645 734490675a 734490675a 74430675a 74430675a 74430675a 74502755 755310815a 766330855 766330855a 776249815a	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03		d Code	te d d te te d d te te d d te d d te d te te d te	23 26 30 21 23 26 30 21 23 26 30 21 23 26 30 21 23 22 30 21 23	Data/Content	Units	Information					Q Sea	rch All Fields	Text include	
abel	Ban hdg(HOQ) .72545862a .72517665a .72517665a .732377666 .73249675a .73249675a .7354667a .7354667a .74510874a .74510874a .75559675a .75559675a .76503084a .76529855a .775249515a .775249515a	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 03 25 04 04 02 03 25 04 04 02 03 25 04 04 02 03 25 04 04 02 03 25 04 04 00 25 0 25 0 25 0 25 0 25 0 25 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 0 25 25 0 0 25 0 0 0 25 0 0 0 0		d Code	Ca Ca Ca Ca Ca Ca Ca Ca Ca Ca Ca Ca Ca C	23 26 30 21 23 26 30 21 23 26 30 22 26 30 21	Data/Context	Units	Information					Q Sea	rch All Fields	Text include	
abel 2103 X 2103 X 187 6 188 6 188 6 189 6 199 7 199 6 199 7 199 6 199 7 199 7 1	hdq(HOQ)     Timestamp     72545862a     729170645a     733470646     73449875a     73349875a     7430076e     74340076a     74510076a     75558075a     76303084a     7633085a     76303084a     77520855a     775240915a     775240955a	02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03 25 04 01 02 03		d Code	59 59 50 50 50 50 50 50 50 50 50 50 50 50 50	23 26 30 21 23 26 30 21 23 26 30 21 23 26 30 21 23 22 30 21 23	Data/Content	Units	bifemation					Q Sea	rch All Fields	Text include	

### Show the battery information





# HID Over I<sup>2</sup>C

HID Over I2C (Human Interface Device Over I2C) is mainly used in Windows 8, ARM platform architecture; the other is HID Over USB is used in x86 system, in Windows 8 common support for HID Over I2C bus protocol device is touch pad.

### Settings

HID over I2C Settings				×
Settings		Color		
Channel Clock Channel (SCL) Data Channel (SDA) ATTN/Interrupt	A0		Start Repeat Start Address Data Write	<ul> <li></li> &lt;</ul>
Custom Format Address Mode • 7-bit Addressing 8-bit Addressing (Inclue 10-bit Addressing	Settings de R/W in Address)	Range	Data Read Stop	· · · · · · · · · · · · · · · · · · ·
✓ Ignore Glitch Filter pulse with < 2	sample points (5ns)		From Buffer Head	To Buffer Tail
			Default	OK Cancel

Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

Custom Format: Customizable partial analysis content.

Setting: Click on it to bring up Notepad to edit the decoding format, the format

is as follows: CMD, {Name of parse field 1, Number of bytes in parse field 1,

Arrangement of parse field 1}, .....

7-bit addressing: Show 7-bit addressing.

8-bit addressing (Include R/W in Address): Show 8-bit addressing (include

7-bit addressing and 1-bit Rd/Wr).



**10-bit addressing:** show 10-bit addressing.

**Ignore glitch:** Ignore the glitches occurred due to the slow transitions. Enabled when checked.

quired: 11:31:00.808		0 ps	20 us 40 us	60 us	80 us	100 us	120 us	140 us	160 us
•									
		A state						h h h h h h h h h h h h h h h h h h h	
		Addr(/	b):01 WA HID Descriptor Ad	A HID Descriptor Ad A w	HIDDescLength	AwHIDDescLengtr	A bcdversion(10)	A bcqversion(UU)	AwReportDe
CLK-0									
BUS_HIDover		4UUU	rennennennen	յիրորորորուն					
DAT-1		16.25 ι	is 26.91 us	21.9 us	7.5 us	14.99 us	7.49 u 11.91 us	21.9 us	9,99 us
ATTN-2		17	5 us	60.62 us		20.02 us	12.5 us		92.5
				0.02.00		20.02 00	12.0 00		
HID over I2C		L L							
14. IM									
<b>IX</b> bel Channel	1								
Del Channel									
Del Channel									
el Channel									
el Channel									
LOO DBux BUS_HIDover	rl2C(HID over I2C)								
LOC DUS BUS_HIDover	rl2C(HID over I2C) Status	Address(7b)	Field						Information
Bus	rl2C(HID over I2C) Status	Address(7b) Wr 01 H	Field ID Descriptor Address(00						Information
100 )Bus BUS_HIDower 101 )Bus BUS_HIDower 101 )131:00.868" St 11:31:00.868" St	rl2C(HID over I2C) Status	Address(7b) Wr 01 H	Field ID Descriptor Address(00 HIDDescLength(033B)			HID Descriptor			Information
100 101 200 201 200 200 200 200	rl2C(HID over I2C) Status	Address(7b) Wr 01 E	Field ID Descriptor Address(00 HIDDescLength(033B) cdVersion(0010)		Compliant	with Version 1.			Information
LOO LOT XBus BUS_HIDOver imp (hhmmss.ms 11:31:00.868 11:31:00.868 11:31:00.868 11:31:00.868	rl2C(HID over I2C) Status	Address(7b) Wr 01 F ir	Field ID Descriptor Address(0) HIDDescLength(033B) cdVersion(0010) ReportDescLength(000A)	000)	Compliant 10 bytes H	with Version 1. Report Descripto	r		Information
100 BBC BUS_HIDOver	rl2C(HID over I2C) Status	Address(7b) Wr 01 B b b	Fiek ID Descriptor Address(0) HIDDescLength(033B) cdVersion(0010) ReportDescLength(000A) ReportDescRegister(070B]	000)	Compliant 10 bytes H Identifier	with Version 1. Report Descripto r to read Report	r Descriptor		Information
400 101 1031 100.865. 113100.865. 113100.865. 113100.865. 113100.865. 113100.865. 113100.865.	rl2C(HID over I2C) Status	Address(7b) Wr 01 E	Field ID Descriptor Address(0( HIDDescLength(033B) cdVersion(0010) ReportDescLength(000A) ReportDescRegister(070B) InputRegister(6400)	000)	Compliant 10 bytes H Identifier Identifier	with Version 1. Report Descripto r to read Report r to read Input	r Descriptor Report		Information
100 100 100 1131:00.868 1131:00.868 1131:00.868 1131:00.868 11:31:00.868 11:31:00.868 11:31:00.868 11:31:00.868	rl2C(HID over I2C) Status	Address(7b) Wr 01 E E K K K K K K K K K K K K K K K K K K	Field ID Descriptor Address (00 HIDDescLength (033B) cdVersion (0010) ReportDescLength (000A) ReportDescRegister (0709) InputRegister (6400) MaxInputLength (IFB4)	000)	Compliant 10 bytes H Identifier Identifier 8116 bytes	with Version 1. Report Descripto r to read Report r to read Input s length field o	r Descriptor Report f Input Report		Information
400 101 200 860 805 HDover 113100.866. 113100.866. 113100.866. 113100.866. 113100.866. 113100.866. 113100.866. 113100.866.	12C(HID over 12C Status art	Address(7b) Wr 01 B k k k k k k k k k k k k k k k k k k k	Fiek ID Descriptor Address (01 HIDDescLength (033B) cdVersion (0010) ReportDescLength (000A) ReportDescRegister (070B) InputRegister (6400) MaxInputLength (IFB4) OutputRegister (2A80)	000)	Compliant 10 bytes H Identifier Identifier 8116 bytes	with Version 1. Report Descripto r to read Report r to read Input	r Descriptor Report f Input Report		Information
100 100 100 100 100 100 100 100	12C(HID over 12C Status art	Address(7b) Wr 01 B b b b b b b b b b b b b b b b b b b b	Field <b>ID Descriptor Address (0</b> HIDDescLength (033B) edVersion (0010) ReportDescRegister (070B) InputRegister (6400) MaxInputLength (IFB4) OutputRegister (2880) ommand Register (2880)	000)	Compliant 10 bytes H Identifier 8116 bytes Identifier	with Version 1. Report Descripto r to read Report r to read Input s length field o r to read Output	r Descriptor Report f Input Report Report		Information
100 BBC BUS_HIDOver	12C(HID over 12C Status art	Address(7b) Wr 01 B F F Wr 01 C	Field ID Descriptor Address (0 HIDDescLength (033B) cdVersion (0010) ReportDescLength (000A) ReportDescLengthster (0400) MaxIngutLengister (2A80) ommand (033B)	000)	Compliant 10 bytes H Identifier 8116 bytes Identifier	with Version 1. Report Descripto r to read Report r to read Input s length field o r to read Output	r Descriptor Report f Input Report	), ReportID:B	Information
100 100 100 100 100 100 100 100	12C(HID over 12C Status art	Address(7b) Wr 01 E Wr 01 W Wr 01 C Ur 01 C	Field <b>ID Descriptor Address (0</b> HIDDescLength (033B) edVersion (0010) ReportDescRegister (070B) InputRegister (6400) MaxInputLength (IFB4) OutputRegister (2880) ommand Register (2880)	000)	Compliant 10 bytes H Identifier 8116 bytes Identifier	with Version 1. Report Descripto r to read Report r to read Input s length field o r to read Output	r Descriptor Report f Input Report Report	), ReportID:B	Information



# HID Over SPI

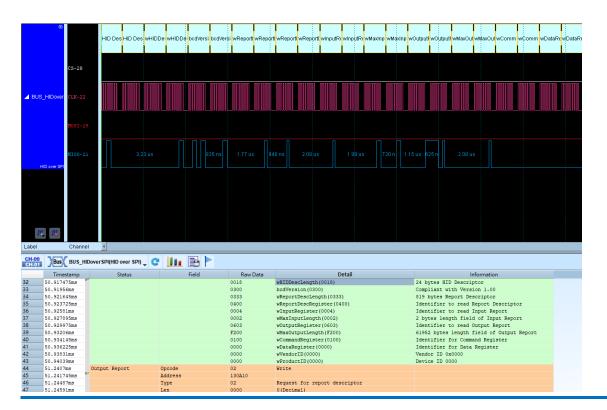
HID Over SPI (Human Interface Device Over SPI) protocol is established by

Microsoft. It's applied for Windows 8 ARM platform.

### Settings

🔜 HID	over SPI Settings					×
Settings			Color			
: <b>&gt;</b> ^	Channel			Input Report		•
	CZ	A0 🌲		Output Report		•
	CLK	A1 🗘		HID Descriptor		•
	MOSI	A2		Report Descriptor		•
	MISO	A2				
			Range			
			<b>7</b>	From	То	
				Buffer Head 💌	Buffer Tail	•
				Default	OK Cancel	

Channel: Show the selected channels (CS, CLK, MOSI, MISO).





### HTSensor

An HTSensor is a sensor designed to measure and monitor environmental conditions. It typically measures environment-related parameters such as temperature and humidity and provides the corresponding data to a system or device for processing or control. These sensors are widely used in a variety of devices and systems, such as smart homes, automation systems, climate control systems, medical devices, and so on.

### Setting

🚢 HTSensor Settin	gs						×
Channel				Color			
Data A0	<b>•</b>			Humidity Temperature Check Digits		Start Echo End	• • •
Chip Settings							
Model: AM2120	) 👻					Tolerance:	0% 💌
	Min	Max			Min	M	ax
Start Low:	1000 🌲	~ 20000	🌲 us	Start High:	10	200	🌲 us
Echo Low:	75	~ 85	🌲 us	Echo High:	75	\$ ~ 85	🌲 us
Logic 0 High:	22	~ 30	🌲 us	Elogic 1 High:	68	~ 75	📮 us
Logic 0&1 Low:	48	~ 55	🌲 us	End Low:	45	\$ ~ 55	🔹 us
Display: Celsiu	ıs (°C) 🔹	•	Ca	Iculate Type: (H	High Low) / 1	0 -	
Range							
From Buffer Head	То	er Tail	•				
				ODef	ault	√ок	XCancel

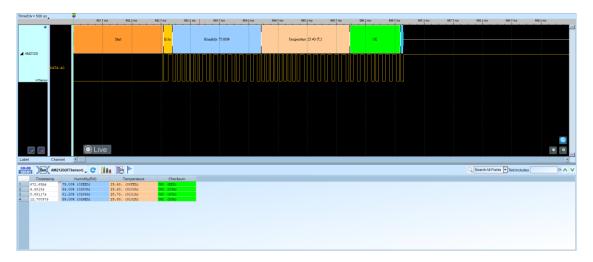
Data: Set the channel number of the Logic Analyzer to which each signal end is



connected on the object to be tested.

Chip Setting: Configure supported chip models or user-defined chip parameter

details.





# **HyperBus**

HyperBus is a high-performance memory interface technology designed to increase data transfer rates, especially in embedded systems such as smartphones, tablets, and IoT devices. Proposed by Micron Technology and adopted by several device manufacturers, HyperBus technology can support many different types of memory, most commonly used for connecting Flash memory and DRAM (Dynamic Random Access Memory), while providing faster data read and write speeds than traditional SPI and parallel memory interfaces.

### Settings

ameter					HyperRAM Options
=1					Phase Delay (CMD, Write Data)
Channel					CLK Delay 0 samples
Mode	HyperFlash			•	Latch Method and Phase Delay (Read Data)
Bus Width	8		•		
cs (	A0 🗧	RWDS1	A2	-	Delay 0      samples     RWDS
CLK	A1 🗧	RWDS2	A19	-	
D0 (	A3 🕻	D8	A11	\$	Latency Count
D1 (	A4 🗧	D9	A12	\$	Data Arrangement
D2	A5 🗧	D10	A13	-	
D3 (	A6 🗧	D11	A14	-	DQ[15:8]
D4	A7 4	D12	A15	×	Color
D5 (	A8	D13	A16	-	
D6 (	A9 🕻	D14	A17	*	
D7 (	A10	D15	A18	-	
Display	y CA[47:	)] in report			
Invert C	CLK				
					Read CMD
nge					Read Data
Deco	de Rang	e			Write CMD
rom		То			Write Data



Mode: Switching mode, can be set to Hyper Flash or Hyper Ram.

Bus Width: Setting the bus width, can be set to 8 or 16.

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

**Display CA[47:0] in report:** Displays CA[47:0] total 48bit information in the report. Available only when the mode is switched to HyperFlash. Enabled when checked.

**Invert CLK:** Invert CLK: Available only when mode is switched to HyperRam. Enabled when checked.

### HyperRAM Options:

- Phase Delay (CMD, Write Data): Sets the number of sample points for Delay, valid only when the mode is switched to HyperRam.
- II. Latch Method and Phase Delay (Read Data): Set the number of sample points for CLK (valid only when mode is switched to HyperRam) or RWDS Delay.
- **III.** Latency Count: Sets the number of Delay CLKs, valid only when the mode is switched to HyperRam.
- IV. Data Arrangement: Sets the mode of the Data Arrangement to one of two modes.



Div=10 ns		51 ma	2.50 ma	2.58 r		1.58 ma	531.1 2.50 ma		58 ma	2.68		2.58 #		2.58 ma		2.58 ma	2.58		2.51 ma	2.68		2.58 ma	2.58 mi	2.58 ma	
red: 13:35:35.745	80 80 80	1		1 1 L	· · · ·																				
	80 80 80	80 Leò	Latency-3 Lot	eacy-4 Lat	kncy-5 Lotency	y-6 Letracy-7	Longary-E	Letracy-9	Leancy	10 Lefency	11 Letrocy	-12 Lea	ency-13 Late	ncy-1,			04 80	04 8	0 04 80	04 80 D	4 80 04		8	0	
CS-A0 CLK-A1	3 33 m 91 m 3 33	- <u>12 12 -</u>	D 22	Te 32 -	3.33 n 891 n 8.	22 × 🗔 2 22			· []]	2	·	22	3.33 m	]3.33 n[	£	222 - 22 - 24	2 22 -	501.02.2	2 - 22 -						
RWDS1-A4	0.07 mg 91 10 27	191 0			0.00 mg 91 mg.			88.11	a) (22	/ 11p. 91 mp.						aren. gan (C.)	1 0.00 m		174 mil 5 nll 7	[]] <u>33 m</u> 4 m 2 5 m <sup>3</sup> 74 m	2.5 x 74 mi2	5 10			
00-45															5.82										
D1-A6																									
D2-A7																	2 <b>4 m</b> ) 27	4 14 2 5 14	374 m 25 m 37	4 mi 2.5 m <sup>3</sup> 74 m	2.5 1 3 74 1 2	5 1			
D3-88															5.41										
D 4-A9																									
US_HyperBu D6-A11																									
03_H)peloc 06-A11 07-A12								83.2 m								<b>EXT</b> 212	w 1174		111-55-1174	a 233 a	1000				
D8-A13								83.2 m								374 mel8 :	38.0 3.74		8 38 . 25 6 8 74	a 3.33 a	838.00	-			
D9-A14																									
D10-A15																									
D11-A16																									
D12-#17																									
D13-A18																									
D14-A19																									_
D15-A20	OLi	10																							
ΠL Hy Mater RHDS2-A21		ve																							•
el Channel	•																								
Bus BUS_Hyper	rBus(HyperBus) 🖕	C III	. 🖻 🏲																		Qs	earch All Field	s 💌 Text Includ	tes	D
amp (hhmm:ss.ms R/V	N AS	Type	System B	yte Addr.	CA0-	2 0	0 D1	D2	D3 D	4 D5	D6	D7	D8 D9	D10	D11	D12 D1	13 D14	D15	A	SCII					
13:35:35.755. Rd(1	1) Reg.(1)	Linear(1)	008080800		F0 80 80 80	0 80 80																			
13:35:35.758 <sup>2</sup> Rd (1	1) Reg.(1)	Linear(1)	008080800			0 80 80 04	80	04 80	04	80	04 8	0 0	4 80	04	80										
13:35:35.761 Rd (1		Linear(1)	008080800		FO 80 80 80																				
13:35:35.763 Rd(1	1) Reg.(1)	Linear(1)	008080800		F0 80 80 80	0 80 80																			



# l<sup>2</sup>C

I2C is a two-wire serial communications bus, using a multi-slave architecture, developed by Philips in the 1980s to enable motherboards, embedded systems, or cell phones to connect to low-speed peripheral devices, and is a commonly used type of electronic circuit system. I2C uses only two bi-directional signal lines, one clock line (SCL) and one data line (SDA). Signal content has a total of start (Start), address (Address), data (Data), read/write (Read/Write), etc., the transmission method is bidirectional, the data format is divided into two kinds of 8 bits and 10 bits. The transmission rate is 100kbit/s-3.4Mbit/s. The data format is divided into 8 bits and 10 bits.

#### Settings

I2C Settings			×
Settings	Color		
Channel Clock Channel (SCL) A0 Data Channel (SDA) A1 Address Mode Orbit Addressing Orbit Addressing (Include R/W in Address) Orbit Addressing	Start Repeat Start Address Data Write Data Read Stop		
Report Show data in report 8 Column Show NACK Unwrap the ASCII frame Clock Stretching Timeout Check us ✓ Ignore Glitch Filter pulse with < 2 \$ sample points	From Buffer Head	Range To To Buffer 1	Fail 💌
	Default	ОК	Cancel



Clock Channel (SCL): Transfer clock of I<sup>2</sup>C.

Data Channel (SDA): Transfer data of I<sup>2</sup>C.

## Address Mode:

- 7-bit addressing: Displays the address in 7-bit width and Rd/Wr in 1-bit width.
- II. 8-bit addressing(Include R/W in Address): Displays an 8-bit width address (7-bit width address plus 1-bit Rd/Wr).
- **III. 10-bit addressing:** Displays a 10-bit width address.

## **Report:**

- Show data in report: Displays the data in the report area with a choice of 8 or 16 fields.
- **II.** Show NACK: Marks the Byte as NACK in the field. enabled when checked.
- **III. Unwrap the ASCII frame:** Add "ASCII" field in the report area. Enabled when checked.

**Clock Stretching:** Set the length of time for Clock Streching. Enabled when checked.

Ignore Glitch: Ignore glitch caused by slow transitions when analyzing.

Enabled when checked.



## Result

Wr: Indicates that the data is written.

# Rd: Indicates reading data.

Time/Div		*																			
Acquired.	16:05:25.843		B14.00 Lat	914.83 w		t na	1.11 ma	· 1:	21 ma	1.31 ms	1.41 ms	1.51 ma	1.01 ma	121ma	1.01 ma	1.91 ms	2.01 ma	2.11 ma	2.21 mi	2.31 ma	
	•		M	ls(7b):12	10	20		30 <mark>A</mark>	Adds(7b):3F	00	A & &&dz(7b):46	21	38	λ				Aðir(75):12	10	20	30
∎ BUS,	ISC CTK-1	u													4	403.34 m					
	DATA-	AL						57.5 tts	60 ==	117.5 18	30 *** 5	0 mz 40 mz	30 = 3	0 m		993.34 m			60 w 70 v		186
			OLive																		
Pi abal			Live																		• •
Label	Chan	nel I			_			_									Q	Search All Field	s 💌 Text include	15	
Label CH-00	Chan	nel I	: III B		01 0			D5 D6	07 14								Q	Search All Field	s 💌 Text Include	15	j.
CH-00 CH-01	Chan	nel I	s Address(7b	) D0		2 D3	D4 I	D5 D6	D7 Infe	ormation							٩	Search All Field	s 💌 Text include	15	j.
Label CH-00 CH-01 99 100	Chan Bus BUS_ amp (hhmmas 16:05:25.003. 16:05:25.004.	nel 1 I2C(I2C) C Ims Statu Start Start	: III B	D0 21 10 10 10 10 10 10 10 10 10 10 10 10 10	D1 D 3A 20 30	2 D3	D4 I	D5 D6	D7 Infe	ormation							Q	Search All Field	s 💌 Text include	15	j.
Label CH-00 CH-01 99 100 101	Chan Bus BUS_ amp (hhmmss. 16:05:25.004. 16:05:25.004.	nel 1 IZC(IZC) C ms Statu Start Start Start	s Address(7b Rz 46	a) D0 21 10 00	3A 20 30	2 D3	D4 I	D5 D6	D7 Infe	ormation	_						Q	Search All Field	s 💌 Text Include	25	j.
Label CH-00 CH-01 99 100 101 102	Chan Bus BUS amp (hhmmss 16:05:25.883. 16:05:25.884. 16:05:25.884.	nel • IZC(IZC) • • Start Start Start Start Start	Address(7) Rr 46 Wr 12 Wr 3F Wr 46	D0 21 10 00 21	3A 20 30 3A	2 D3	D4 1	D5 D6	D7 Infe	ormation							٩	Search All Field	s 💌 Text Include	15	j.
CH-00 CH-00 CH-01 99 100 101 102 103	Chan Bus Bus_ amp (hhmmss 16:05:25.004 16:05:25.004 16:05:25.004	nel 4 I2C(I2C) ( Statu Start Start Start Start	s Address(7k Wr 46 Wr 12 Wr 37 Wr 46 Wr 12	D0 21 10 00 21 10 10	3A 20 30	2 D3	D4 I	D5 D6	D7 Inf	ormation							٩	Search All Field	s 💌 Text Include	15	j.
Label CH-00 CH-01 99 100 101 102 103 104	Chan Chan	nel (2C(12C) (C) (C) (C) (C) (C) (C) (C) (C) (C) (	8 Address(7) 8 46 9 12 9 27 9 46 9 12 9 27 9 2	D0 21 10 00 21 10 00	3A 20 30 3A 20 30	2 D3	D4 1	D5 D6	D7 Infe	ormation							Q	Search All Field	s 🛡 Text Include	15	j.
Label CH-00 CH-00 99 100 101 102 103 104 105	Chan Chan	nel (C) (CC) (C) (C) (C) (C) (C) (C) (C) (C	x Address(7b Wr 46 Wr 12 Wr 37 Wr 46 Wr 12 Wr 37 Wr 46	b) D0 21 10 00 21 10 00 21 21 21	3A 20 30 3A 20 30 3A	2 D3	D4 I	D5 D6	D7 Infe	ormation							Q	Search All Field	s 💌 Text Include	15	×
CH-00 CH-00 CH-01 99 100 101 101 102 103 104 105 106	Chan Chan	nel ( IZC(IZC) ( ms Start Start Start Start Start Start Start Start	8 Address(7) 8 46 9 12 9 27 9 46 9 12 9 27 9 2	D0 21 10 00 21 10 00	3A 20 30 3A 20 30 3A	2 D3	D4 1	D5 D6	D7 Inf	ormation							Q	Search All Field	s 💌 Text Include	55	×
Label CH-00 CH-01 99 100 101 102 103 104 105 106 107 108	Chan Bus Bus_ amp (hhmmas de105:25.084. de105:25.085. de105:25.086. de105:25.086. de105:25.086. de105:25.086. de105:25.086. de105:25.086.	nel (2C(12C) ) ms Statu Start Start Start Start Start Start Start Start Start Start Start Start Start Start	a Address(7) Wr 46 Wr 12 Wr 37 Wr 46 Wr 12 Wr 37 Wr 46 Wr 12 Wr 37 Wr 46	a) D0 21 10 00 21 10 00 21 10 00 21 10 00 21	3A 20 30 3A 20 30 3A 20 30 3A 3A	2 D3	D4 1	D5 D6	D7 Inf	ormation							Q	Search All Field	s 💌 Text Include	15	1
Label CH-00 CH-01 99 100 101 102 103 104 105 106 107 108 109	Chan Bus Bus amp (hummas de105:25.083. de105:25.084. de105:25.084. de105:25.086. de105:25.086. de105:25.086. de105:25.086. de105:25.087. de105:25.087. de105:25.087. de105:25.087.	nel ( IZC(IZC) ( Start	Address(7) Wr 46 Wr 12 Wr 46 Wr 12 Wr 46 Wr 13 Wr 46 Wr 12 Wr 46 Wr 12 Wr 46 Wr 12 Wr 46 Wr 12 Wr 46 Wr 12 Wr 46	a) D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10	3A 20 30 3A 20 30 3A 20 30	2 D3	D4 1	D5 D6	D7 Inf	ormation							٩	Search All Field	s 💌 Text Include		×
Label CH-00 CH-01 99 100 101 102 103 104 105 106 107 108 109 110	Chan (bus) BUS_ amp (hhmmas, 16:05:25.084, 16:05:25.084, 16:05:25.084, 16:05:25.086, 16:05:25.086, 16:05:25.086, 16:05:25.087, 16:05:25.087, 16:05:25.088, 16:0	nel * IZC(IZC)  IStart Start S	Mr         46           Wr         46           Wr         12           Wr         37           Wr         46           Wr         12           Wr         37           Wr         46           Wr         12           Wr         37	a) D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10 00	3A 20 30 3A 20 30 3A 20 30 3A 20 30 3A 20 30	2 D3	D4 1	D5 D6	D7 Inf	ormation							Q	Search All Field	s 🐨 Text Include	15	×
Label CH-00 CTIOT 999 100 101 102 103 104 105 106 107 108 109 110 111	Chan Bus BUS_ amp (hummas, 16105125.084, 16105125.084, 16105125.086, 16105125.086, 16105125.086, 16105125.086, 16105125.088, 161051	nel ( IZC(IZC) ( Start	Nr: 46           Wr: 46           Wr: 12           Wr: 37           Wr: 46           Wr: 12           Wr: 46           Wr: 12           Wr: 46           Wr: 42           Wr: 46           Wr: 46           Wr: 46           Wr: 37           Wr: 46	D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10 00 21	3A 20 30 3A 20 30 3A 20 30 3A 20 30 3A 3A 3A	2 D3	D4 1	D5 D6	D7 Inf	ormation							Q	Search All Field	s 💌 Text Include		×
Label 99 100 101 103 104 105 106 109 110 111 111 112	Chan 2007 Bus Bus amp (htmmcas 4105:25.084 4105:25.084 4105:25.084 4105:25.084 4105:25.086 4105:25.086 4105:25.086 4105:25.088 4105:25.088 4105:25.088 4105:25.088	nel (CRC) (CC) (CRC) (CR	Address(1)           No. 46           No. 46           No. 12           No. 12           No. 12           No. 12           No. 12           No. 46           No. 12	a) D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10 10 10	3A 20 30 3A 20 30 3A 20 30 3A 20 30 3A 20 30	2 D3	D4 1	D5 D6	D7 Infe	ormation							Q	Search All Field	s 💌 Text Include	15	×
CH-00 CH-00 CH-00 101 102 103 104 105 106 107 108 109 110 111 112 113	Chan Chan	nel (Caracteria)	Nr: 46           Wr: 46           Wr: 12           Wr: 13           Wr: 14           Wr: 16           Wr: 16           Wr: 17           Wr: 46           Wr: 18           Wr: 19           Wr: 46           Wr: 12           Wr: 13           Wr: 46           Wr: 46           Wr: 46           Wr: 46           Wr: 12           Wr: 37           Wr: 46           Wr: 12           Wr: 37           Wr: 46           Wr: 12           Wr: 37	b) D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10 00 21 10 00 00 00	3A         30           20         30           3A         20           20         30           3A         20           3A         20           3A         20           3A         20           3A         30           3A         30           3A         30           3A         30	2 D3	D4 1	D5 D6	D7 Inf	ormation							Q	Search All Field	s 💌 Text Include	15	×
CH-00 CH-00 CH-01 99 100 101 102 103 104 105 106 107 108 109 110 111 111 112 113 114	Chan XBux, BUS_ amp (blummas 16:05:25.035,04 16:05:25.035,04 16:05:25.045,0 16:05:25.045	nel ( IZC(IZC) ( Start) Start Star	n Address(/1 No: 46 No: 46 No: 12 No: 12 No: 12 No: 46 No:	a) D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10 10 10	3A 20 30 3A 20 30 3A 20 30 3A 20 30 3A 3A 3A	2 D3	D4 1	D5 D6	D7 Inf	ormation							9	Search All Field	s 🔽 Text include	18	×
CH-00 CH-00 CH-01 99 100 101 102 103 104 105 106 107 108 109 110 110 111 112 113 114 115 116	Chan Chan	nel (Caracteria)	Nr: 46           Wr: 46           Wr: 12           Wr: 13           Wr: 14           Wr: 16           Wr: 16           Wr: 17           Wr: 46           Wr: 18           Wr: 19           Wr: 46           Wr: 12           Wr: 13           Wr: 46           Wr: 46           Wr: 46           Wr: 46           Wr: 12           Wr: 37           Wr: 46           Wr: 12           Wr: 37           Wr: 46           Wr: 12           Wr: 37	b) D0 21 10 00 21 10 00 21 10 00 21 10 00 21 10 00 21	3A         30           20         30           3A         20           20         30           3A         20           3A         20           3A         20           3A         20           3A         30           3A         30           3A         30           3A         30           3A         30           3A         30	2 D3	D4 1	D5 D6	D7 Inf	ormation							Q	Search All Field	3 💌 Text include	15	j.



# I<sup>2</sup>C EEPROM

EEPROM, or E<sup>2</sup>PROM, is known as Electrically-Erasable Programmable Read-Only Memory, and the interface of EEPROM components can be classified into serial and parallel, with I<sup>2</sup>C EEPROM belonging to the 2-wire serial EEPROM, and its model is a series starting with 24. I<sup>2</sup>C EEPROM belongs to the 2-wire serial EEPROM, and its model number is a series starting with 24.

#### Settings

🔜 I2C(EEPROM 24 Series) Settings	×
Parameters	Color
Channel	Start   Output Enable
Clock Channel (SCL) A0	Control   Device ID
Data Channel (SDA) A1	Address 🗾 👻 Command Select 📃 👻
	Read 🗾 🗸 Data 🗾
Device Address	Write Stop 💌
Control Code	ACK
7-bitAddressing	NACK
O 8-bit Addressing (Include R / W in Address)	Chip
Word Address	Range
Address Width 8	Decode Range
24LCS61/24LCS62	From To
✓ Ignore Glitch	Buffer Head 🔹 Buffer Tail 💌
	ODefault ✔OK ★Cancel

**Clock Channel (SCL):** Transfer clock of I<sup>2</sup>C.

Data Channel (SDA): Transfer data of I<sup>2</sup>C.

**Device Address:** 



- 1. Control Code: Display Control Code.
- IV. 7-bit Addressing: Displays the address in 7-bit width and Rd/Wr in 1-bit width.
- 2. 8-bit Addressing (Include R/W in Address): Displays an 8-bit width address (7-bit width address plus 1-bit Rd/Wr).

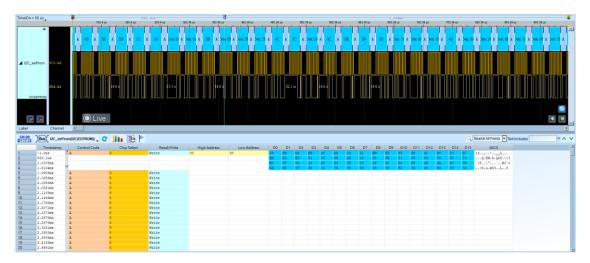
Word Address: Set the number of valid bits of I2C EEPROM address, the

default value is 8.

**24LCS61 / 24LCS62:** Select whether to analyze 24LCS61 / 24LCS62. enabled when checked.

**Ignore Glitch:** Ignore glitch caused by slow transitions when analyzing.

Enabled when checked.





# l<sup>2</sup>S

I<sup>2</sup>S is an interface standard for transferring digital audio data between ICs. It is a bus standard developed by Philips for transferring audio data between digital audio devices, and is often used for transferring PCM audio from a CD to a DAC in a CD player. The I<sup>2</sup>S standard specifies the hardware interface specifications and the format of the digital audio data, and uses a sequential approach to transmit two groups (left and right channels) of data. It consists of three transmission lines, a clock line (SCK), a word selection line (WS), and a data line (SD). The data format is up to 32 bits.

## Settings

🚢 12S S	ettings		×
Channe	I		Sound reduction
	Clock Channel (SCK) Word Select Channel (WS) Data Channel (SD) Data Bits	A0	<ul> <li>Display the audio waveform</li> <li>Save as WAV file</li> <li>Playback</li> <li>Align common sample rate</li> </ul>
Config			Color
	Enable meet ful	scale	
	Mode I2S Mode	•	R. Channel
	Report 8 Columns	•	
TDM Se	ttings		L. Channel
	Channel Size	16	Range
	Channel Length	16	m
	Word Length	8	⊭—• Decode Range
	Channel Offset	8	From To
	Latch	Rising -	Buffer Head 💌 Buffer Tail 💌
Det	fault		✓OK XCancel



**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

**Data Bits:** The number of bits of analyzed data ranges from 1 to 32 Bits; the default value is 16 Bits.

#### Sound reduction:

- 1. Display the audio waveform: User can draw the waveform of the sound in the Waveform area. Enabled when checked.
- 2. Save as WAV file: All Data can be saved as a sound file (.WAV) and saved in the working directory. Enabled when checked.
- 3. Playback: The default setting is off. This function collects all the data and plays it back after analyzing it. This is the fastest way to confirm that the sound is being transmitted correctly without having to go through the data one by one. Since the length of playback time depends on the depth of data that the Logic Analyzer can record, it is recommended that you increase the Logic Analyzer's data depth and reduce the number of channels used by the Logic Analyzer. Enabled when checked.
- Align common sample rate: Automatically archives the sound waveforms with the sampling rate closest to the commonly used ones (44.1KHz, 48KHz .....). Enabled when checked.

#### Config:

- 1. Mode: switch mode base on the needs.
  - i. I<sup>2</sup>S Justified
  - ii. MSB Justified
  - iii. LSB Justified
  - iv. PCM



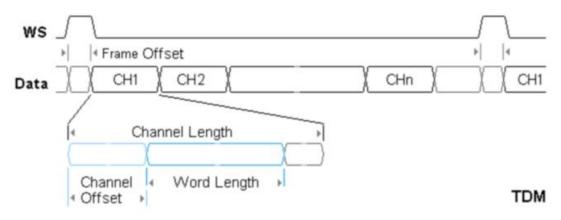
v. TDM

2. Enable meet full scale: Auto-completes missing bits in multiples of 8,

e.g., 15 bits to 16 bits, 17 bits to 24 bits, enabled when checked.

3. **Report:** User can select the number of columns displayed in the report area.

## **TDM Setting Parameter Definitions:**



lime/Div= 500	Dus,	~	12.91		3.41 mg	13.91 mg	14.41 r		01 ms	15.41 ms 15.91 ms	10.41 ms	10.91 ms	17.41 ms	17.91 ms	18.41 mg	18.91 ms	19.41 mg	19.91 ms	20.41 ms	
		_			2.41 mg	10.01110						10.31 110	1 1 1 1 1 1 1				14741114		10.41 mg	in the second
	0				10.0	1.111	1.1.1		1 1 1								1 10 1			
		L.7	R-5(L-6E) R-652	1:75 R-5( L-6E I	2.651 L.75 R.	5(L6E R651L2	5 R:5( L:5E R:	551 L:75 R-54 L:6	E R:651 L:75 R:5	Life Riffi L 75 R 5( Life R	:651 L:75 R:5( L:6E R:f	51 L:75 R:5( L:6E R:	651 L-75 R-5( L-6E R	1651 L:75 R 50 L 6E R	651 L 75 R 5( L 6B)	R:651 L:75 R:50 L:6	E R:651 1:75 R:50	L6E R651 L75 R5	CLISE R:651 L:75 R:5	X LISE R:
									1 1 1											
	SCK-A0																			
4 128																				
14.10																				
	WS-A1		136 u	136 u	152 m	136 u 152 i	a 1.36 u	152 us 136	α 152 υ	136 o 152 o	152 m 136 m	152 u 136 u	152 us 136 u	152 u 136 u	152 us 136 u	136	u 152 u	136 u 152 u	136 u 152 u	136 u
			n armtina e							יות כתר הנכודה ומנות כוו	ת הרוח הרוחה							nnin nnin		
	5D-A2																			
	128																			
						and a part of	and the boot of the			IIA G BIT ATAG			THE REAL PROPERTY AND ADDRESS OF			ALC: NOT				
PK 1	10		O Liv	e																۰,
	-			-															<i>a</i> -	
abel	Channe	1 1																		
																	_			_
	Bus (12 S(12 S)	C C															C Search All Fi	alds 💌 Text inclus	tes	
Tr	mestamp	DO	D1	D2	D3	D4	D5	D6	D7	Informat	tion									
		R:65D1	L:75F5	R:5C74	L:6E9A	R:65D1	L:75F5	R:5C74	L:6E9A											
		R: 65D1	L:75F5	R:5C74	L: 6E9A	R:65D1	L:75F5	R:5C74	L:6E9A											
		R:65D1	L:75F5	R:5C74	L:6E9A	R:65D1	L:75F5	R:5C74	L:6E9A											
14.9		R:65D1	L:75F5	R:5C74	L:6E9A	R:65D1	L:75F5	R:5C74	L:6E9A											
15.9		R:65D1	L:75F5	R:5C74	L: 6E9A	R:65D1	L:75F5	R: 5C74	L:6E9A											
		R:65D1	L:75F5	R:5C74	L:6E9A	R:65D1	L:75F5	R:5C74	L:6E9A											
18.1		R: 65D1	L:75FS	R:5C74	L:6E9A	R:65D1	L:75F5	R: 5C74	L: 6E9A											
19.2		R:€5D1	L:75F5	R:5C74	L: (E9A	R:65D1	L:75F5	R:5C74	L:629A											
20.2		R: 65D1 R: 65D1	L:75F5	R:5C74	L:6E9A	R:65D1 R:65D1	L:75F5 L:75F5	R: 5C74 R: 5C74	L:6E9A L:6E9A											
21.3		R: 65D1 R: 65D1	L:75F5 L:75F5	R:5C74 R:5C74	L:6E9A L:6E9A	R:65D1 R:65D1	L:75F5 L:75F5	R:5C74 R:5C74	L: 6E9A L: 6E9A											
23.5		R165D1	L:75F5	R15C74	LIGERA	R165D1	L175F5	R15C74	LIGERA											
24.5		R: 65D1	L:75F5	R:5C74	L:6E9A	R:65D1	L:75F5	R15C74 R:5C74	L: 6E9A											
25.6		R: 65D1	L:75F5	B:5C74	L: (E9A	R:65D1	L:75F5	R:5C74	L: (E9A											
26.7		R: 65D1	L:75F5	R:5C74	LIGERA	R:65D1	L17525	R:5C74	LIGENA											
27.8		R: 65D1	L:75F5	R:5C74	L: 6ESA	R:65D1	L:75F5	R:5C74	L: 6E9A											
28.81		R: 65D1	L:75F5	R:5C74	L:(E9A	R:65D1	L:7525	R:5C74	L: (E9A											
29.9		R: 65D1	L:75F5	R:5C74	L: 6E9A	R:65D1	L:7525	R:5C74	L: 6E9A											
		R: 65D1	L:75F5	R:5C74	L:6E9A	R:65D1	L:75F5	R:5C74	L: 6E9A											
		R: 6501	L:75F5	R:5C74	L: (E9A	R:65D1	L:7525	R:5C74	L: (E9A											
				R:5C74	LIGESA	R:65D1	L:75F5	8:5074	LIGERA											
32.1																				
32.1	875aa	R:65D1 R:65D1	L:75F5 L:75F5																	
32.1	62ma	R:65D1 R:65D1 R:65D1	L:75F5 L:75F5	R:5C74 R:5C74 R:5C74	L:6E9A	R:65D1 R:65D1	L:75F5 L:75F5	R:5C74 R:5C74	L:6E9A L:6E9A											



# 180

The Inter 8080-series interface is mainly used for LCM data transfer.

It is simply called I80 interface. To analyze the 8080-series, 3 or 4 Ctrl Buses (WR, RD, CS, and D/C) are required, and the Data Bus requires at least 4 bits depending on the user's definition, so at least 7 channels are required: WR, RD, CS, D0-D3, and 8 channels if there is a D/C Pin. The channel numbers of these signals can be adjusted. The channel numbers of these signals can be adjusted. The 8 bits Data bus requires 11 signals: WR, RD, CS, D0-D7, and so on... WR to CH0, and so on.

#### Settings

🗯 180 Sett	tings								×
Channel									
	Select (	Channe	I.						
1			D0	A3	D8	A11	D16	A19 🌲	
	WR	A0	D1	A4	D9	A12	D17	A20	
	RD	A1	‡ D2	A5	\$ D10	A13	D18	A21 🌲	
	CS	A2	D3	A6	‡ D11	A14	D19	A22	
			D4	A7	\$ D12	A15	D20	A23 🌲	
	✓ 0	n D/C	D5	A8	D13	A16	D21	A24 🌲	
	D/C	A27	D6	A9	D14	A17	D22	A25 🌲	
			D7	A10	D15	A18	D23	A26	
C	Option								
	Data	Bus		Bit Or	der		Report Da	ita	
	8 Bi	t	*	LSB	First	•	8 Colum	n 👻	
Color									
Setting	Color								
					Deed				
Data	mand			•	Read Write				
Data					Wille				
Range									
<b>11</b>	Decode	Range	•						
From					То				
Buffer H	lead			•	Buffer	Tail			•
					Default		<b>∀</b> 0К	×Can	cel



Select Channel: Show the selected channels (WR, RD, CS, D0, D1, D2, D3,

D4, D5, D6,...).

**On D/C:** Use the D/C pin as Command (Low) or Data (High).

Data Bus: Select 4 Bit, 8 Bit, 12 Bit, 16 Bit, 20 Bit, or 24 Bit.

Bit Order: Select LSB First or MSB First.

Report Data: Select 8 columns or 16 columns.

		2.03 ma	2.04 mg	2.04 ma	2.06 ma	2.05 ma	2.08 ma	2.00 ma	2.07 ma	2.07 ma	2.06 ma	2.08 ma	2.09 ma	2.09 ms	2.1 ma	2.1 ma	2.11 ma
		20310	101112	104112	1000	1.00 00			101 102	1.1.1.1		2.00 mg	104110		1.110		
				I	E	01		00									
	WR-A2				6.95 111		7.34 to:										
	RD-A3																
	CS-A0				3.66 to	3.66 w	4.02 ts 3.6	58 w									
	D0-84						7.68 m										
							1.00 %										
	D1-A5																
	D2-A6				7.32 00												
	D3-A7																
	04-18																
	D5-A9																
	D6-A10																
	D7-A11																
	D/C-A1				6.58 us												
100	D/C-AL				6.36.03												
K, N		OLive															.•
		0															
	Observal																
	Channel I					_											
Bus	Channel 💽			_											🔍 Search All Field	Is 👻 Text includes	
Times	(180(180) C	mand Write/Read	d Data	ASCI											Q Search All Field	19 💌 Text includes	)
Times 1.86us	(180(180) Constant	mand Write/Read	89	ASCII										(	Q Search All Field	Is 💌 Text includes	)
Times 1.86us 9.54us	(180(180) Com stamp Data/Cor Command Data	mand Write/Read	89	ASCII •										(	🔍 Search All Field	Is 💌 Text includes	
Times 1.86us 9.54us 17.24us	(180(180) Comand Data/Com Data Data	mand Write/Read	89 00 00	ASCII - -										(	Q Search All Field	Is Text includes	)
Times 1.86us 9.54us 17.24us 1.0268ts	IB0(B0) Comend Data Data Data Command Data	mand Write/Read	89 00 00 8A	ASCII - -										(	C Search All Field	Is 💌 Text includes	)
Times 1.86us 9.54us 17.24us 1.02688t 1.0342m	stamp Data/Con Command Data Data Data Data Data	Write/Read	89 00 00 8A 18	ASCI										(	Q Search All Field	IS Text includes	· · · · · ·
Times 1.86us 9.54us 17.24us 1.0268ts 1.0342ms 1.04154s	stamp Data/Cor Command Data ms Command is Data ins Data	Write Write Write Write Write Write Write Write	89 00 00 8A 18 00	ASCII										(	Q Search All Field	IS Text includes	, ,
Times 1.86us 9.54us 1.02688 1.03428 1.03428 1.04154 2.05118	stamp Data/Con stamp Data/Con Data a Data a Data a Data a Data a Data a Data a Command	mmand Write/Read Write Write Write Write Write Write Write Write	89 00 00 8A 18 C0 DE	ASCII - - - - -		_								(	Q Search All Field	is 💌 Text includes	
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Times 1.86us 5.54us 1.0268ts 1.0342m 1.04154s 2.05118t 2.0585m 2.0662m	stamp Data/Con Data Data Ins Command Ins Data Ins Command Ins Data Ins Data Ins Data Ins Data	mand Write/Read Write Write Write Write Write Write Write Write Write	89 00 00 8A 18 00 00 01 00	ASCII - - - - - - - - - - - - -										(	Q Search All Field	is 💌 Text includes	
Times 1.86us 9.54us 17.24us 1.0268ts 1.0342m 1.04154s 2.0511ts 2.0585m 2.0662m 3.07584s	K 180(180) C Command Stamp Data Data Data Data Sas Data Sas Data Sas Data Sas Data Sas Data Sas Data Sas Command Sas Data	wmand Write/Read Write Write Write Write Write Write Write Write Write Write	89 00 00 8A 18 C0 00 00 88	ASCII - - - - - - - - - - - - - - - - -										(	Search All Field	is 💌 Text includes	
Times 1.06us 9.54us 17.24us 1.0260t 1.0342m 1.04154t 2.0511tt 2.0555m 2.0662m 3.07504t 3.07504t	teone of the teone of	wmand Wike/Read Write Write Write Write Write Write Write Write Write Write Write Write	89 00 00 00 8A 18 C0 00 00 00 88 0A	ASCII - - - - - - - - - - - - - - - - - -										(	Search All Field	is 👿 Text includes	)
Times 1.86us 9.54us 17.24us 1.02688 1.0342m 1.04154 2.05188 2.0662m 3.07584 3.07584 3.09086	stamp Data/Con Command Data	wmand Write/Read Write Write Write Write Write Write Write Write Write Write Write Write	89 00 00 8A 18 C0 02 01 00 85 04 00	ASCII - - - - - - - - - - - - - - - - - -											Search All Field	is 🛡 Text includes	,
Times 1.86us 9.54us 17.24us 1.0268ts 1.0342m 1.04154s 2.0511ts 2.051ts 2.0565m 3.07584s 3.07584s	K 160(10) C Comand Stamp Data/Cor Comand Data Data So Data So Data	wmand Wike/Read Write Write Write Write Write Write Write Write Write Write Write Write	89 00 00 00 8A 18 C0 00 00 00 88 0A	ASCI - - - - - - - - - - - - - - - - - - -											Rearch All Field	is Text includes	



# IDE

IDE (Integrated Device Electronics) is a standard interface for hard disks, solid-state drives, CD-ROMs, etc. IDE was first used by Western Digital in the U.S. for its hard disk sales business. The name IDE was first used by Western Digital in the United States for their hard disk sales business. The official specification name is ATA/ATAPI (Advanced Technology Attachment/AT Attachment Packet Interface). The ATA specification has continued to be added to due to the increased capacity of hard disks, the need for higher transfer speeds, and the constant evolution of storage devices. In 1998, the ATAPI specification was added to ATA-4, allowing ATA to connect to optical drives and other storage media. In 2003, the SATA (Serial ATA) specification was released, which retroactively renamed the original Parallel ATA to PATA (Parallel ATA) to differentiate it.

To analyze IDE, because it is a parallel transmission, it needs to use more channels, so we have to divide it into three types.

Normal channel (11 pin): Its signals are DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP, DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-, RESET-, CSEL and IOCS16. -.

Register channel (5 pin): its signals are CS(0:1)- and DA(2:0).

Data channel (16 pin): its signal is DD(15:0).

IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4

We recommend that IDE bus of the target system to be connected to the instrument as the following table:



			PC-based T&W Instruments
Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14
Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25	DIOR-:HDMAR DY- :HSTROBE	Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMAR DY- :DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24



Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		

# Settings

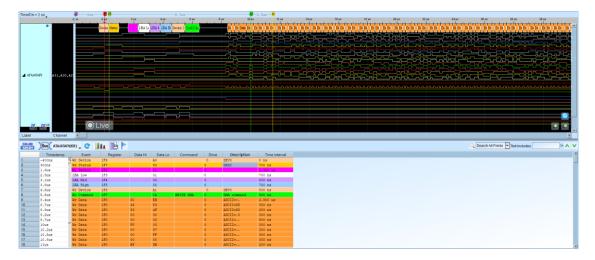
Gene							
Gene	al Register	Data E	Bus				
DIOR-	HDMARDY-HS		A20	PDIA	G-:CBLID-	A24	-
DIOW	STOP		A17	DASE	0_	A28	\$
DMAR	Q		A18	RESI	ET-	A19	-
IORD	CDDMARDY-:D	STROBE	A22	CSEI	-	A23	-
DMAC	к-		A26	IOCS	16-	A0	-
INTRO	Σ		A31	-			
and Setting							
Trans	ferring mode	Register	Color	Analysis Repo	t		
	Transferring	Mode	M	lax Transferring F	late Stand	dard	
O UI	TRA DMA Mo	de 1	25M	lByte/sec	ATA-4		
	.TRA DMA Mo .TRA DMA Mo			IByte/sec IByte/sec	ATA-4 ATA-4		
		de 2	33M	-			
	.TRA DMA Mo	de 2 de 3	33M 44M	Byte/sec	ATA-4		
	.TRA DMA Mo .TRA DMA Mo	de 2 de 3 de 4	33M 44M 66M	Byte/sec	ATA-4 ATA-5		
	.TRA DMA Mo .TRA DMA Mo .TRA DMA Mo	de 2 de 3 de 4	33M 44M 66M	IByte/sec IByte/sec IByte/sec	ATA-4 ATA-5 ATA-5		
	.TRA DMA Mo .TRA DMA Mo .TRA DMA Mo	de 2 de 3 de 4	33M 44M 66M	IByte/sec IByte/sec IByte/sec	ATA-4 ATA-5 ATA-5		v
	TRA DMA Mo .TRA DMA Mo .TRA DMA Mo .TRA DMA Mo	de 2 de 3 de 4	33M 44M 66M 100	IByte/sec IByte/sec IByte/sec	ATA-4 ATA-5 ATA-5		
	TRA DMA Mo TRA DMA Mo TRA DMA Mo TRA DMA Mo Decode Range	de 2 de 3 de 4	33M 44M 66M 1001	IByte/sec IByte/sec IByte/sec MByte/sec	ATA-4 ATA-5 ATA-5		•



Channel: Set channel number for General, Register, and Data Bus.

**Transferring Mode:** User can specify which specification will be used by the device to be tested so that commands can be interpreted correctly during IDE analysis. If it is not specified correctly, the analysis can be performed.

**Analysis Report:** User can specify that only those registers are displayed in the Display Report window. For example, if the Data Register is unchecked, data about the data register will not appear in the Report window. In this way, the contents of the data registers are filtered out when viewing the analysis results.





# IO-Link

IO-Link is a communication system that connects smart sensors and actuators to automation systems, in accordance with the Single-drop digital communication interface for small sensors and actuators (SDCI) in the IEC 61131-9 standard. This specification includes electrical connections and digital communication protocols through which smart sensors and actuators can interact with automation systems.

Settir	ngs	
🔛 IO-	Link Settings	×
Settings	Channel CAQ AO Timing Constraints Transmission Timeout > 30 T <sub>BIT</sub> Response Time < 10 T <sub>BIT</sub>	Color Direct Parameter CMD Data Storage Event
	Analysis Mode	Wakeup/Fallback  Range  From To  Buffer Head Default OK Cancel

**Channel:** Set the C/Q signal terminal on the object under test to be connected to the channel number of the logic analyzer.

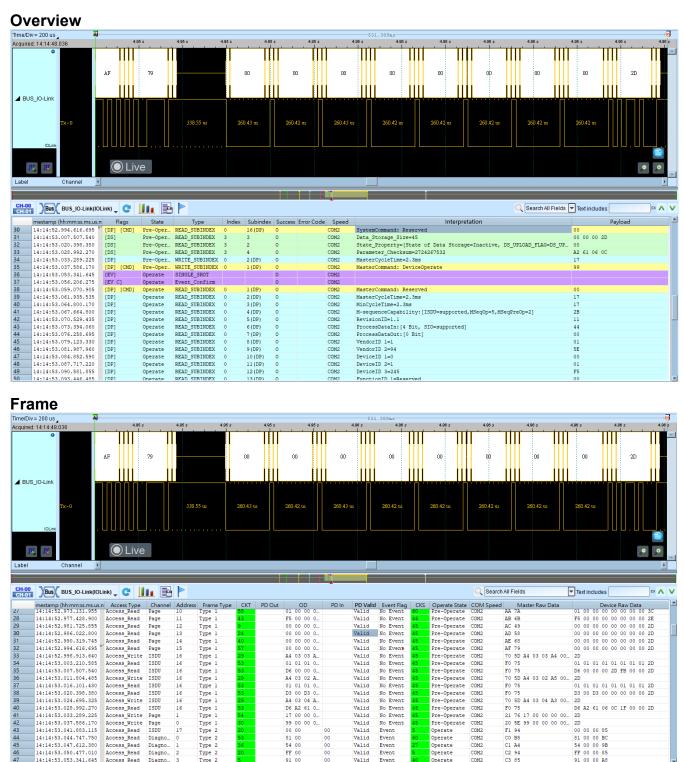
## Timing Constraints:

- **Transmission Timeout:** The default is 30 TBIT. If IDLE is larger than this value, the next data will be decoded and analyzed by the Master.
- **Response Time:** The default is 10 TBIT. If IDLE is less than this value and greater than 3 TBIT, the next data will be decoded and analyzed by Device.

**Analysis Mode:** The report will be analyzed in the selected mode (Overview, Frame, ISDU, Event).



#### Result



Valid

Valid

Valid

Valid

Valid

Valid

Valid

Valid

Valid Event Event

Valid

Valid Event

Valid

No Event No Event No Event

No Event No Event No Event Event

70 5D A4 03 04 A3 00... F0 75 21 76 17 00 00 00 00... 20 5E 99 00 00 00 00... F1 94 C0 B5 C1 A4 C2 94 C3 85

D3 00 D3 00 00 00 00 00 2D 2D D6 A2 61 06 0C 1F 00 00 2D 2D 2D 00 05 61 00 00 85 54 00 00 98 FF 00 00 85 91 00 00 A8

COM2

COM2

COM2

COM2

COM2

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COM2 COM2

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COM2

Pre-Operate

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Pre-Operate Pre-Operate

Pre-Operate

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A4 03 02 A... 01 01 01 0... D3 00 D3 0... A4 03 04 A... D6 A2 61 0... 17 00 00 0... 99 00 00 0... 00 00

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ISDU

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Page ISDU

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Access\_Write Access\_Read

Access\_Read Access\_Read

Access\_Read

Access Read

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Туре Туре

Туре Туре

Type 2

Type

Type

Type

14:14:53.016.101.430 14:14:53.020.398.380 14:14:53.024.695.325

14:14:53.028.992.270 14:14:53.033.289.225

14:14:53.037.586.170 14:14:53.041.883.115

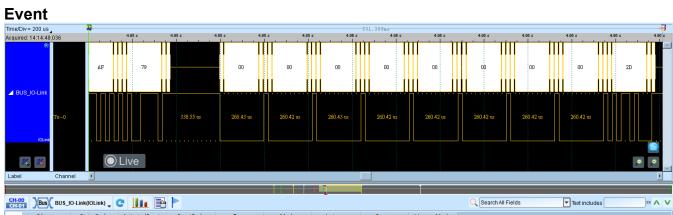
14:14:53.044.747.750 14:14:53.047.612.380

14:14:53.050.477.010 14:14:53.053.341.645



'Div = 200 us	A							389ms						>
red: 14:14:48.036		4.95 s 4.95 s	4.95 s	4.95 s	43	4.95 s	4.96 s	4.96 s	4.96 s	4.96 s	4.96 s	4.96 s	4.96 s	4.96
♥ IUS_IO-Link	ÅF	79	00		00		00	00		Op	00	00	2D	
Tx-0		338.55 us	260.43 v	8	260.42 us		260.43 us	260.42 us	260.42 us	260.42 us	260.42 us	260.42 us		
L Channel		Live											,•	
BUS_IO-Link	(IOLink) 🖵 🧲	: 🛄 🖻 🏱								Q Search All F	Fields	Text include	es 📃	EX /
imestamp (hh:mm:ss.ms.			Length		Subindex	Error Cod	de Payload Lengt	jth	Payload	Chkpdu		Raw Data		
14:14:52.917.271.635		Read Requset(8_Index)		21							93 15 86			
14:14:52.921.568.585 14:14:52.925.865.535		Busy Read Response+	8				5	30 30 30	20.00		01 01 01 01 01 01 D7 30 30 30 30			
							3	30 30 30 .	30 00			00 57		
14:14:52.925.005.555		Read Requset (8_Index_Subinde	x) 4	3	3					164 A	A4 03 03 A4			

5	14:14:53.003.210.585	Device	Busy	8						01 01 01 01 01 01 01 01
6	14:14:53.007.507.540	Device	Read Response+	6			4	00 00 00 2D	251	D6 00 00 00 2D FB
7	14:14:53.011.804.485	Master	Read Reguset(8_Index_Subindex)	4	3	2			165	A4 03 02 A5
8	14:14:53.016.101.430	Device	Busy	8						01 01 01 01 01 01 01 01
9	14:14:53.020.398.380	Device	Read Response+	3			1	00	211	D3 00 D3
10	14:14:53.024.695.325	Master	Read Requset(8_Index_Subindex)	4	3	4			163	A4 03 04 A3
11	14:14:53.028.992.270	Device	Read Response+	6			4	A2 61 06 0C	31	D6 A2 61 06 0C 1F
12	14:14:53.107.769.645	Master	Read Requset(8_Index_Subindex)	4	3	3			164	A4 03 03 A4
13	14:14:53.116.363.540	Device	Read Response+	6			4	00 00 00 2D	251	D6 00 00 00 2D FB
14	14:14:53.122.092.805	Master	Read Requset (8_Index_Subindex)	4	3	2			165	A4 03 02 A5
15	14:14:53.124.957.435	Device	Busy	2						01 01
16	14:14:53.127.822.065	Device	Busy	2						01 01
17	14:14:53.133.551.330	Device	Read Response+	3			1	80	83	D3 80 53
18	14:14:53.142.145.225	Master	Write Requset(8_Index_Subinde	5	3	1	1	01	38	25 03 01 01 26
19	14:14:53.145.009.860	Device	Busy	2						01 01
20	14:14:53.147.874.490	Device	Write Response+	2					82	52 52
21	14:14:53.153.603.750	Master	Read Recuset(8 Index Subindex)	4	3	5			162	A4 03 05 A2



	:amp (hh:mm:ss.ms	StatusCode	ActivatedEvents	EventCode	Туре	Mode	Instance	Source	lsLegacyMode
1	14:14:53.053"	Type_2	el	FF91	Notification	SINGLE_SHOT	Application	DEVICE	False
2	14:14:53.056	Confirm							



# IrDA

The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

# Settings

📥 IrDA Settings	×
Channel	Color
<b>*</b>	Start  Data Stop
LA Channel A0	Address 🗨
Invert Waveform	CRC
Mode	
O SIR Transfer Rate	Kbps (2.4Kbps ~ 115.2Kbps)
O HDLC Transfer Rate	Mbps (0.576Mbps ~ 1.152Mbps)
• 4PPM(FIR)	
Range	
From To Buffer Head To	Opefault ✔OK ★Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Invert Waveform: Invert the waveform before analysis. Enabled when

checked.

Mode:



- SIR: After switching to SIR mode, enter the transfer rate to complete the setting.
- 2. **HDLC:** After switching to HDLC mode, enter the input rate to complete the setting.
- 3. 4PPM (FIR):

ne/Div= 2 ms																														
evolv= 2 ms	۳	2.21 s	2.21		2.22 s		2.22 :			22 s	2.22		2.22		2.23 s	2.23 s		.23 s	2.23 s		2.23 s		2.24 s		2.24 s		2.24 s		2.24 s	
			- to +	- <u>100 - 1</u>			- m+		<u> </u>	d to	nt ind		6 d	· · · ·	hr + 1	· · ·		tor -			n + r	<del>a 1</del> 1								
•						10		- 111								1														
			Date: CD Date		_		_										x P9 Data:					Data: FF				Date: 6B	Data: E9			
	24	e: C0 Dets: C0	Dete: CO Dete	C0 Dete: 0	CO Deb:	CU Jete	: CO Det	ste: 00 ]	Data: C0	Dete: CO	Dete: C0	Data: C0	Dete: CO	Date: FF Date: 3	F Data: 01	Data: 20 Data	n: F9 Data:	13 Dets: 0	Data: FF	Data: FF	Dets: FF	Data: PP	Dete: 01	Dete: 00	Date: 00	Jete: 6B	Data: E9	Date: CL		
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I IrDA															EI.															
Data-A														1.00					1.00	1.00	1.02 ms	1.00								
Data-A	· • •													1.02.00					1.02 m	1.02.383	1.04.005	1.02.00								
I/DA					1 1000																							1 1000		
																														_
		~																												
DX		Live																												0
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iel Channe	1																													
Bus IrDAII	A)_ C	li. 🖬																						Qs	earch All F	ields 🔻	Text inch	udes		∝ ∧
				05 06	D7	DA	09	D10	D11	012	D13 [	014 0	015	ASCII		Informa	ation							Qs	earch All F	ields 🔻	]Text incl	udes		]∝ ∧
Timestamp	D0 D	D2 D	3 D4	05 D6							D13 0			ASCII		Informa	ation							Qs	earch All F	ields 🔻	]Text incl	udes		]∝ ∧
Timestamp 691,32703ms	D0 D	D2 D	3 D4	45	58	48	41	4E	47	00	C8 43	A C1	1.A	CUTE_HANGJ.		Informa	ation							Qs	earch All F	ields 🔻	Text incl	udes		]∝ ∧
Timestamp 691.32703ms 2.2160209s	D0 D 25 00 C0 C0	D2 D 41 43 C0 C0	3 D4 55 54 C0 Ci	45 C0	SF C0	48 C0	41 C0	4E C0	47 C0	00 C0	C8 43 FF 31	A C1 F 01	\$.A	CUTE_HANGJ.		Informa	ation							Qs	earch All F	ields 🔻	Text incl	udes		.∝ ∧
Timestamp 691.32703ms 2.2160209s 2.232660355s	D0 D 25 00 C0 C0 2D F9	D2 D 41 43 C0 C0 11 00	3 D4 55 54 C0 Ci FF FI	45 C0 FF	5F C0 FF	48 C0 01	41 C0 00	4E C0 00	47 C0 68	00 C0 E9	C8 43 F7 31 C1 C0	A C1 F 01 D C0	N.A	CUTE_HANGJ.		Informa	ation							Qs	earch All F	ields 🔻	]Text incl	udes		]∝ ∧
Timestamp 691.32703ms 2.2160209s 2.232660355s 2.320461205s	D0         D           25         00           C0         C0           2D         F9           C0         C0	41 43 C0 C0 11 00 C0 C0	3 D4 55 54 C0 C1 FF F1 C0 C1	45 C0 EF C0	5F C0 FF C0	48 C0	41 C0 00 C0	4E C0 00 C0	47 C0 68 TT	00 C0 E9 3F	C8 43 FF 38 C1 C0 01 25	C1 F 01 C0 C0 F F9	•.A	CUTE_HANGJ. ?k?		Informa	ation							Qs	earch All F	ields 🔻	Text incl	udes		<b>∝</b> ∧
Timestamp 691.32703ms 2.2160209s 2.232640355s 2.320441205s 2.34508066s	D0         D           25         00           C0         C0           2D         F9           C0         C0           11         00	D2 D 41 43 C0 C0 11 00 C0 C0 FF FF	3 D4 55 54 C0 C0 FF F1 C0 C0 FF F1	45 C0 FF C0 01	5F C0 FF C0 01	48 C0 01	41 C0 00 C0 B3	4E C0 00 C0 F0	47 C0 68	00 C0 E9 3F C0	C8 43 FF 38 C1 C0 01 21 C0 C0	C1 F 01 C0 C0 F9 C0 C0	9.A	CUTE_HANGJ. 		Informa	ation							Q	earch All F	ields 🔻	Text incl	udes		]∝ ∧
Timestamp 691.32703ms 2.2160209s 2.232660355s 2.328441205s 2.34508066s 2.440965505s	D0         D           25         00           C0         C0           2D         F9           C0         C0           11         00           C0         C0	D2 D 41 43 C0 C0 11 00 C0 C0 FF FF C0 C0	3 D4 55 5- C0 C1 FF F1 C0 C1 FF F1 C0 C1	45 C0 FF C0 01 C0	5F C0 FF C0 01 C0	48 C0 01	41 C0 00 C0 B3 FF	4E C0 00 C0 E0 3F	47 C0 68 FF C1 01	00 C0 E9 3F C0 2D	C8 43 FF 33 C1 C0 01 22 C0 C0 F9 11	L C1 F 01 D C0 D F9 D C0 L 00	9.A	CUTE_HANGJ. ?		Informa	ation							Qs	earch All F	ields <b>v</b>	Text incl	udes		)¤ ∧
Timestamp 691.32703ms 2.2160209a 2.232660355s 2.320441205s 2.34508066a 2.440965505s 2.45760496s	D0         D           25         00           C0         C0           2D         F9           C0         C0           11         00           C0         C0           FF         FF	D2         D           41         43           C0         C0           11         00           C0         C0           FF         FF           C0         C0           FF         FF           FF         FF	3 D4 55 5- C0 C1 FF F1 C0 C1 FF F1 C0 C1 01 02	45 C0 FF C0 01 C0 C0 00	5F C0 FF C0 01 C0 DB	48 C0 01 C0 00 C0 EA	41 C0 00 C0 B3 FF C1	4E C0 00 C0 F0 3F C0	47 C0 68 FF C1 01 C0	00 C0 E9 317 C0 2D C0	C8 43 FF 31 C1 C0 01 21 C0 C0 F9 11 C0 C0	C1 F 01 C0 C0 F9 C0 C0 C0 C0 C0 C0 C0 C0	•	CUTE_HANG3. ?		Informa	ation							Qs	earch All F	ields 🔻	Text incl	udes		]¤ ∧
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Timestamp 691, 32703ms 2, 2160209s 2, 32660355s 2, 32640355s 2, 44508066s 2, 440945505s 2, 457604965 2, 55388501s 2, 6550611s 2, 662445565s 2, 770222415s	D0         D           25         00           C0         C0           2D         F9           C0         C0           11         00           FF         FF           C0         C0           FF         FF           C0         C0           FF         FF           C0         C0           FF         C0           C0         C0	D2         D           41         43           C0         C0           11         00           C0         C0           FF         FF           C0         C0           FF         FF           C0         C0           01         03           C0         C0           00         08           C0         FF	3 D4 55 54 C0 C1 C1 C2 C1 C2 C2 C1 C2	45 C0 FF C0 C0 C0 C0 C0 C3 3F C0 2D	5F C0 FF C0 01 C0 DB FF C1 01 C0 F9	48 C0 01 C0 00 C0 E& 3F C0 2D C0 11	41 C0 00 B3 FF C1 01 C0 F9 C0 00	4E C0 C0 F0 3F C0 2D C0 2D C0 11 C0 FT	47 C0 68 FF C1 01 C0 F9 C0 00 C0 C0 FF	00 C0 E9 37 C0 2D C0 11 C0 FF C0 FF C0 FF	C8 43 FF 33 C1 C0 01 25 C0 C0 F9 11 C0 C0 C0 C0 FF F5 C0 C0 FF F5 C0 C0 FF F5 F7 01	L C1 F 01 0 C0 F F9 0 C0 1 00 0 C0 F FF 0 C0 F FF 0 C0 0 C0	· · · · · · · · · · · · · · · · · · ·	CUTE_HANGJ. ?. .k. ?- .? ? .?		Informa	ation							Qs	earch All F	ields 🔻	Text inclu	udes		
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Timestamp 61.1270ba 2.32660356 2.32660356 2.32640356 2.46096505 2.46096505 2.46096505 2.46096505 2.45076286 2.5533551a 2.7702242 2.77022415 2.77022415 2.77022415 2.77022415 2.77022415 2.77022415 2.7702545 2.7702545 2.7705	D0         D           25         00           C0         C0           2D         FS           C0         C0           I1         00           FF         FF           C0         C0           FF         FF           C0         C0           00         D3           C0         FF           25         00           C0         C0           20         FF           C0         C0           21         F0	D2         D2           41         43           C0         C0           11         00           C0         C0           FF         FF           C0         C0           01         03           C0         C0           C0         C0           C1         03           C0         FF           F0         F0           37         01           34         41           43         C0           C0         C0           11         00           C0         C0	B         D4           55         5           C0         C0           C1         C0           C2         27           C0         C1           C1         C1           C2         P1           S5         S           C0         C1           C1         C1           C1         C1           C2         P1           S5         S           C0         C1           C1         P1           C2         P1           S5         S           C0         C1           P1         P1	45 C0 FF C0 01 C0 C0 C3 SF C0 C0 C1 C0 FF C0 FF C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	5F C0 FF C0 01 C0 28 FF C1 01 C0 FF C0 00 SF C0 00 SF C0 00 SF C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 01 C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	45 C0 01 C0 00 C0 20 C0 20 C0 21 C0 21 C0 27 45 C0 57 45 C0 01 C0 20 20 C0 20 20 20 20 20 20 20 20 20 2	41 C0 00 B3 FF C1 01 C0 F9 C0 00 C0 F7 41 C0 00 C0 F7 41 C0 00 C0 F7 83	4E C0 00 F0 337 C0 2D C0 2D C0 11 C0 FF 4E C0 FF 4E C0 FF 4E C0 FF 4E C0 C0 FF 70 FF 70 FF 70 FF 70 75 75 75 75 75 75 75 75 75 75	47 C0 68 FF C1 01 C0 F9 C0 00 C0 FF C0 FF C0 FF C1 C0 C0 FF C1 C1 C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	00 C0 E9 3F C0 2D C0 11 C0 FF C0 01 00 C0 E9 3F C0 2D C0 C0 2D C0 2D C0 2D C0 2D C0 2D C0 2D C0 C0 2D C0 2D C0 C0 2D C0 C0 2D C0 C0 2D C0 C0 2D C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	CB         43           FF         33           C1         C0           C1         22           C0         C1           C0         C2           C0         C2           C0         C2           C0         C3           C0         C4           FF         01           C0         C3           C0         C4           FF         04           FF         04           FF         04           FF         04           FF         04           FF         05           C3         C4           FF         05           C4         C4           FF         05           C5         C4           FF         05           C1         C5           C3         C5           C4         C5           C5         C4           C5         C5	A         C1           F         01           D         C0           D         F9           D         C0           F         FF           D         C0           D         C0           D         844           L         C1           D         C0           L         00		CUTE_HAMG. J 		Informa	ation								earch All F	ields 💌	] Text incl	udes		<b>∧</b> ¤(
Timestamp 68., 2703m 2.12020m 2.3260355 2.3260355 2.3400066 2.46096505 2.4500665 2.4500655 2.4500655 2.45002825 2.7702244 2.7702244 2.7702244 2.7702245 2.7702245 2.7702245 2.7702245 2.7702245 2.770254 2.5072647 2.50767 2.50767 2.50767 2.50767 2.507677 2.5076777 2.507677	D0         D           25         00           C0         C0           2D         FS           C0         C0           11         00           C0         C0           FF         FF           C0         C0           01         04           C0         C0           01         04           C0         C0           C1         C0           C0         C0	D2         D2           41         43           60         C0           11         00           C0         C0           FF         FF           C0         C0           PF         FF           C0         C0           00         00           00         08           C0         C0           97         C1           3F         01           41         43           C0         C0           D1         00           C0         C0           FF         FF           FT         TT           ST         C1           ST         ST           ST         <	B         D4           55         5           C0         C1           FF         F1           C0         C1           FF         F1           C0         C1           FF         F1           C0         C1           FF         F1           C0         C1           FF         F1           C0         C1           FF         F1	45 C0 FF C0 01 C0 C0 C0 C3 SF C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	5F C0 FF C0 DB FF C1 C0 FF C0 00 SF C0 FF C0 00 SF C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	48 C0 01 C0 DA 3F C0 2D C0 11 C0 FF 48 C0 01 C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	41 CO 00 CO B3 FF C1 01 CO FF C0 00 CO FF 41 CO 00 CO FF 41 CO 00 CO EF FF 41 CO CO EF FF EF EF EF EF EF EF EF EF	4E C0 C0 F0 3F C0 2D C0 2D C0 FF FF 4E C0 FF 4E C0 00 C0 FF 9 SF 7 3F	47 C0 68 FF C1 01 C0 F9 C0 00 00 00 FF 47 C0 FF 47 C0 FF 47 C0 10 10 10 10 10 10 10 10 10 1	00 C0 E9 37 C0 2D C0 11 C0 FF C0 01 00 C0 E9 37 C0 2D C0 C0 C0 C0 C0 C0 C0 C0 C0 C0	CB         44           FF         31           C1         C1           C1         C2           C0         C2           C1         C3           C1         C3           C1         C3           C1         C3           C1         C3           C2         C3           C3         C3	A         C1           F         01           D         C0           D         C1		CUTE_HANG.J. 		Informa	ation								earch All F	ields 💌	] Text inch	udes		<b>∧</b> ¤(



# ISELED

ISELED (Integrated Smart Embedded LED) is a new smart embedded LED technology designed to provide more efficient and intelligent control of LED lighting systems. It combines the luminous performance of LEDs with integrated circuit (IC) technology to enable more precise and flexible control for a wide range of application scenarios, especially in automotive, architectural and consumer electronics.

## Settings

🗮 DigitalLED Settings	×
Parameters	Color
Channel Data A0	Downstream Address Upstream Data Freq. sync CRC Instruction EOC
Range	
PromToBuffer HeadBuffer Tail	OK Cancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal and is connected on the object to be tested

end is connected on the object to be tested.



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# ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

#### Settings

🚞 ITU-R I	BT.656	(CCIR6	56)	) Settings				$\times$
Channel								
<b>;</b>								
Channe	el							
CLK	(	A0	-	Data 5	A6	-	Data Bits	
Data	0	A1	\$	Data 6	A7	\$	8 👻 Bits	
Data	1 [	A2	\$	Data 7	<b>A</b> 8	•	Save Raw Data	
Data	2	A3	\$	Data 8	A9	-		
Data	3	A4	-	Data 9	A10	-		
Data	4	A5	\$					
Color								
SAV				-	CR		-	
EAV				•	СВ			
Blankin	g				Y		•	
Range								
1 <b>4</b> 4	Deco	de Ran	ge					
From Buffer	Hood			_	To	er Tai		
Builer	пеац			•		eria	II •	
				ODet	fault		✓OK XCancel	



**Channel:** Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Data Bits: Show the number of data bits.

Save Raw Data: Save the result as .bin file. Enabled when checked.

ime/Div=5us		9												5.119as									
			34 us	30.77 us		1.54 us	48.02	us	60.00 us	67	16 us	62.64 u	67,414	s 72.18 us	78.96	105 01	23 65	00.5 us	91.28 us	95.05 us	100.02 us	105.50	w
۰	•		SAVO	an CB 7 10		V(58): Enm	Rinakia			SAVOO	CRY	ICR V 10	EAV (98): Error Ba	nirin		AV (SO) CB Y	1CR V 10	EAV(58) Error E	akis		SAV(80) CB	VICR VIO E	AV(SR) Error Bi
	Cik-A0																						
				UUUU	ՄՄՍ	וטטנ	JUU	սսս	UШI	յսսւ	յսս	UUL	וטטטטו	JUUUUU	ШUU	UUUU	บบบ		JUUU		UUUUI	յսսև	וטטטו
	Date0-Al		3.44 us	7.53 m			9.21 05		3.44 1		7.53 m		-	21 ws	3.44 us	7.53 us		<b>1</b> 4	2.21 ms	3.44 us	7.53	u 1	1 1
	Datal-A2		<b></b>	7.53 m		4.95		04 10	4.67 w		7.53 w		4.95 w	2.03 m 4.67		7.53 u		4.95 m	2.03 m	4.67 10	w 7.53	-	
	Data2-A3																						
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	Date3-A4		1 00			212 10	]			1 ma		[	2.12 ==		2 10.0			2.12 10			w 7.53		2.12 us
	Date4-AS		4	ar= 🗖		212		m 1.92		41	-		212-	301	Stall we as	417 m		212 -	3 m	92 m h 54 m h m h	4.17		212 **
	DataS-A6																						
		_																					
	DateS-A7	2	:58 m 1 m	7.53 te			.16 w	1.92	u 2.9 u	1 =[	7.53 us		7.16	a 1.93 w	2.58 w i w	7.53 w		7.16	02 12	92 w 2.58 w 1	w 7.53	u	
ITU-R BT 656 (CC	Data7-A8				1.52 0		3 105		3.57 0			1.51 m	2.15 m 0.81 m			98 m	1.52 -	2.15 us 1.8 us			1.98 ts	1.51 0	2.15 us 1.81 us
110-R 51:000 (00																							
DX DV		C	)Live																				
R, N		C	Live																				.•
IX, IX	Channel	•	Live																				
Label		•		line in																O Report A	Deside and Texas	di di s	5
abel		•	CIR656)) 🖵 😋																	Q Search A	I Fields 💌 Text in	cludes	۲ ۲ ۲
abel		•				CR	У	CB	Y	CR	у		EAV	Informati	on					Q Search A	I Fields 💌 Text ir	cludes	5
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tel 101 Bus 1013 Inns 12.605 33.69u 54.775	PBus1(ITU estamp los 8 los 8 los 8 los 8	+RBI656 (C)	CIR656)) C SAV 1, elsewhere. 1, elsewhere. 1, elsewhere.	80 80 80	10 10 10	80 80 80	10	CB	Y	CR	90 90 90	: Error : Error : Error	EAV	Informati	DM	_				Q Search A	I Fields 💌 Text ir	cludes	
bel H-00 H-01 Data 10na 12.605 33.69ta 54.775 75.865	PBus1(ITU estamp las 8 las 8 las 8 las 8	+RBI656 (C) 10: Field 1 10: Field 1 10: Field 1 10: Field 1 10: Field 1	CIR656)) C SAV 1, elsewhere. 1, elsewhere. 1, elsewhere.	80 80 80 80	10 10 10 10 10	80 80 80 80	10 10 10	CB	Y	CR	90 90 90 90	: Error : Error : Error	EAV	Informati	Dri					Q Search A	I Fields 💌 Text in	cludes	
bel 1008 1008 12,605 33,696 33,695 56,950	PBus1(ITU estamp los 8 los 8 l	I-R BI656 (C)	CIR656)) C SAV , elsewhere. , elsewhere. , elsewhere. , elsewhere.	50 50 50 50 50 50	Y 10 10 10 10 10	80 80 80 80 80	10 10 10	CB	Y	CR	90 90 90 90 90	: Error : Error : Error : Error : Error	EAV	Informati	Dn					Q Search A	I Fields 💌 Text in	cludes	
400 XBus 1013 XBus 10ns 12.60% 33.69u 54.775 75.86% 96.95u 118.033	PBust((TU estamp los 8 los 8 l	R BI656 (C)     Field 1     C: Field 1	CIR656)) C SAV i, elsewhere. i, elsewhere. i, elsewhere. i, elsewhere. i, elsewhere.	00 80 80 80 80 80 80 80 80 80 80 80 80 8	10 10 10 10 10	80 80 80 80 80 80	10 10 10 10	CB	Y	CR	90 90 90 90 90 90 90	Error Error Error Error Error Error Error	EAV	Informati	Dri	-				Q Search A	I Fields 💌 Text in	cludes	
LOC XBus 1015 1015 12.605 33.69u 54.775 75.665 96.95u 118.03 139.120	PBust((TU estamp las 8 las 8 las 8 las 8 los 8 l	HR BI656 (C)     Field 1	CIR656)) C SAV SAV (, elsewhere, (, elsewhere, (, elsewhere, (, elsewhere, (, elsewhere, (, elsewhere,	50 50 50 50 50 50 50 50 50	Y 10 10 10 10 10 10	80 80 80 80 80 80 80	10 10 10 10 10	СВ	Y	CR	90 90 90 90 90 90 90 90	Error Error Error Error Error Error Error Error	EAV	Informati	Dri					Q Search A	I Fields 👻 Text in	cludes	
bel 500 )Bus 1013 12.605 33.69us 54.775 75.665 96.95us 118.033 139.12 160.21 160.21 181.296	PBus1(ITU estamp las 0 las 8 las 8 l	HAR BI656 (C)     Field 1     10: Field 1	CIR656)) C SAV (, elsewhere, , elsewhere, , elsewhere, , elsewhere, , elsewhere, , elsewhere, , elsewhere,	00 80 80 80 80 80 80 80 80 80 80 80 80 8	Y 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80	10 10 10 10 10 10 10	CB	Y	CR	90 90 90 90 90 90 90 90 90	Error Error Error Error Error Error Error Error Error Error	EAV	Informati	Dri	_				Q Search A	I Fields 👻 Text ir	cludes	
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bel tona 10na 12x 605 33.69u 54.775 75.065 96.95u 118.033 139.122 160.211 181.292 202.305	PBust()TU estamp ias 8 ias 8 i 8 i 8 i 8 i 8 i 8 i 8 i 8 i 8 i 8 i	4 10: Field 1 10: Field 1 10	C(R656)) C SAV 1, elsewhere. 1, elsewhere. 1, elsewhere. 1, elsewhere. 1, elsewhere. 1, elsewhere. 1, elsewhere. 1, elsewhere.	CE 80 80 80 80 80 80 80 80 80 80 80 80	Y 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80 80 80	10 10 10 10 10 10 10 10 10	CB	Y	CR	94 96 96 96 96 96 96 96 96 96	: Error : Error	EAV	Informati	04					Q Search A	I Fields 👻 Text ir	cludes	
bel 400 DBs 100a 100	PBust(ITU estamp las 8 las 8 l	<ul> <li>Field 1</li> </ul>	CIR656)) C SAV ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere. ; elsewhere.	00 80 80 80 80 80 80 80 80 80 80 80 80 8	Y 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80 80 80 80 8	10 10 10 10 10 10 10 10 10 10	CB	Y	CR	94 94 94 94 94 94 95 95 95 95	: Error : Error	EAV	Informati	on					Q Search A	I Fields 💌 Text in	cludes	
bel 1008 12260 12360 12460 12460 12602	PBust((TU) estamp las 8 las	4 IR BI656 (CI IIII Field 1 IIII Field 1 IIIII Field 1 IIII Field 1 IIIIII Field 1 IIII Field 1 IIIII Field 1 IIIIIII FIELD FIEL FIELD FIELD FIELD FIEL	CIR656)) C SAV SAV , elsewhere. , elsewhere. , elsewhere. , elsewhere. , elsewhere. , elsewhere. , elsewhere. , elsewhere. , elsewhere.	CE 80 80 80 80 80 80 80 80 80 80 80 80 80	Y 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80 80 80 80 8	10 10 10 10 10 10 10 10 10 10 10	св	Y	CR	90 90 90 90 90 90 90 90 90 90 90 90	: Error : Error	EAV	Informati	00					Q Search A	I Fields 💌 Text in	cludes	
Hotol         Jean           1000         Jean           1000         12.605           33.690         33.690           54.775         75.866           95.911         12.602           120.02         12.003           120.03         12.002           120.03         12.002           120.03         12.002           120.03         12.002           120.03         203.062           120.042         205.464           120.042         205.464	PBust(ITU estamp tras 6 tras 7 tras 7	A     BI656 (CI     Field 1     10: Field 1	CIR656)) C SAV SAV (, elsewhere, (, elsewhere, (), elsewhere, (), elsewhere, (), elsewhere, (), elsewhere, (), elsewhere, (), elsewhere, (), elsewhere,	CE 80 80 80 80 80 80 80 80 80 80 80 80 80	Y 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80 80 80 80 8	10 10 10 10 10 10 10 10 10 10 10 10	CB	Y	CR	90 90 90 90 90 90 90 90 90 90 90 90 90 9	: Error : Error	EAV	Informati	on					C Search A	I Fields 💌 Text in	cludes	
Abbel           21:00         Xem           10:ns         10:ns           10:ns         33:6%           10:ns         10:ns           10:ns         20:ns	PBust(JTU)           restamp         r           ras         8           ras         8 <td>4 3. R BI656 (C 10: Field 1 10: Field 1</td> <td>C(R656)) C SAV SAV i, clasekhere, i, clasekhere, i, clasekhere, i, clasekhere, i, clasekhere, i,</td> <td>CE 80 80 80 80 80 80 80 80 80 80 80 80 80</td> <td>Y 10 10 10 10 10 10 10 10 10 10 10 10 10</td> <td>80 80 80 80 80 80 80 80 80 80 80 80 80 8</td> <td>10 10 10 10 10 10 10 10 10 10 10 10 10 1</td> <td>CB</td> <td>Y</td> <td>CR</td> <td>94 94 94 94 94 94 94 94 94 94 94 94 94 9</td> <td>Error Error</td> <td>EAV</td> <td>Informati</td> <td>09</td> <td></td> <td></td> <td></td> <td></td> <td>Q Bearch A</td> <td>i Fields 👻 Text in</td> <td>cludes</td> <td></td>	4 3. R BI656 (C 10: Field 1 10: Field 1	C(R656)) C SAV SAV i, clasekhere, i, clasekhere, i, clasekhere, i, clasekhere, i,	CE 80 80 80 80 80 80 80 80 80 80 80 80 80	Y 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80 80 80 80 8	10 10 10 10 10 10 10 10 10 10 10 10 10 1	CB	Y	CR	94 94 94 94 94 94 94 94 94 94 94 94 94 9	Error Error	EAV	Informati	09					Q Bearch A	i Fields 👻 Text in	cludes	
Label         Jona           21.00         Jona           10na         10na           12.605         33.684           53.694         100.39           10.01         100.39           10.02         100.39           100.22         20.347           22.23.47         244.55           20.02.98         244.55           20.01.01         20.36           20.37         325.59	PBust()TU           exitamp           isa	4 10: Field 1 10: Field 1 10	CIR656)) C SAV SAV ( clashbre: ( clashbre:	CE 80 80 80 80 80 80 80 80 80 80 80 80 80	Y 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80 80 80 80 80 8	10 10 10 10 10 10 10 10 10 10 10 10 10 1	CB	Y	CR	90 90 90 90 90 90 90 90 90 90 90 90 90 9	1 Error 2 Error	EAV	Informati	04					Q (Search A	I Fields 🛡 Text in	cludes	
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# JTAG

JTAG (Joint Test Action Group) is an international standard test protocol (IEEE 1149.1), mainly used for on-chip internal testing, and nowadays most advanced components support JTAG protocol, such as DSPs, FPGAs, etc. The standard JTAG consists of five signal interfaces: TCK, TMS, TDI, TDO and TRST, four of which are input signal interfaces and the other one is output signal interface. The standard JTAG consists of five signal interfaces: TCK, TMS, TDI, TDO and TRST, four of which are input signal interfaces and the other one is output signal interface. The standard JTAG consists of five signal interfaces: TCK, TMS, TDI, TDO and TRST, four of which are input signal interfaces and the other one is an output signal interface. The basic principle is to define a TAP (Test Access Port) inside the device and test the internal nodes with a dedicated JTAG test tool.

#### Settings

🗮 JTAG Sett	ings					×
Setting			Color			
Channel	ADV Report					
тск	CH 0	cJTAG(OScan1)	TEST_LOGIC_RESET	•	EXIT1_IR	•
TMS	CH 1	TRST CH 4	RUN_TEST_IDLE		EXIT1_DR	•
TDI	CH 2		SELECT_IR	•	PAUSE_IR	•
TDO	CH 3		SELECT_DR	•	PAUSE_DR	•
			CAPTURE_IR	•	EXIT2_IR	•
			CAPTURE_DR	•	EXIT2_DR	•
Range	Decode Range		SHIFT_IR SHIFT_DR	•	UPDATE_IR UPDATE_DR	•
	From Buffer Head	To Buffer Tail				
	Default				≪ок	*Cancel

**Channel:** Specify the channel number of the Logic Analyzer to be connected with the object to be tested, the TRST pin can be decided by the user, if you are going to use the function of interpreting commands, then the system will decide whether to use the TRST pin or not according to the data of the commands that you have selected, and the user can decide whether to turn on the cJTAG or not, if you turn on the cJTAG option, the TDI/TDO channels are displayed in If



cJTAG is enabled, the TDI/TDO channels will be grayed out, and the TCK/TMS

channels will be treated as TCKC/TMSC channels in cJTAG OScan1 mode.

### Advanced:

Cha	annel	ADV	Report				
	Interp	erpreter instr	uction				
	ID	D	Name		Len		<b>A</b>
1	000	0 ARM7~A	RM9		4		
2	001	1 ARM10			4		
3	002	2 ARM11			5		
4	003	3 Xilinx			5		
0	Test Da	ne test data is Data Input ( Data Output	TDI)	Refresh Test [ LSB		Edit t Order	•

- I. Show the test data is: User can select the state of TAP state as Shift-IR, Shift-DR. TDI or TDO data will be displayed in hexadecimal.
- II. **Test Data Bit Order:** The length of data may vary during data transmission by JTAG. Therefore, the user can specify whether the data is LSB First or MSB First when interpreting TDI/TDO.
- III. Interpreter Instruction: If you open the Explain Command function, you will see a list of commands, and the JTAG protocol analyzer will display the commands in the Instruction register during Update-IR. Users can select "Edit..." function to add and modify the instruction list file (JtagInst.txt) by themselves using the editor. After finishing the modification, click "Refresh" again to update the instruction list.
- **IV. Acute Jtag Instruction table(JtagInst.txt):** This file is provided by Jtag DLL, users can re-edit this file according to their own needs. We

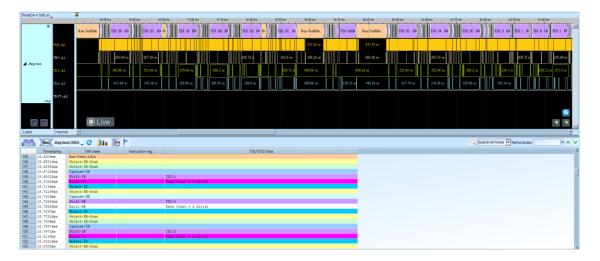


also supports BSDL format, user can directly add the BSDL file, user can save the time of editing instruction data, please see the last appendix of this unit Acute Jtag Instruction table syntax description.

**Report:** To enable report filtering, simply check the items to be displayed in the report window.

Channel ADV Report	
Show the state in the report	
✓ Test-Logic-Reset	✓ Exit1-DR
✓ Run-Test/Idle	✓ Exit1-IR
✓ Select-DR-Scan	✓ Pause-DR
✓ Select-IR-Scan	✓ Pause-IR
✓ Capture-DR	✓ Exit2-DR
✓ Capture-IR	✓ Exit2-IR
✓ Shift-DR	✓ Update-DR
✓ Shift-IR	✓ Update-IR
Show TDI or TDO	○ Show TDI and TDO

I. Show TDI or/and TDO: If choose "Show TDI and TDO", the report area will show the TDI and TDO at the same time.





### Acute JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

**#ID:** Command list number; the range is 00 - FF and , MUST be entered in order or will be seen as the end of commands.

**#NAME:** Command Name, 32 bytes most will be shown in the command list.

**#LENGTH:** Command length, unit in bits.

**#CAPTURE:** Command Capture Code, is stored in Instruction Register..

**#INST:** Command List, listed by Command Code and Command Name or will be seen as the end of commands..

**#TRST:** Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

**#BSDL:** Load the BSDL file. Use the BSDL file as step 1-6.

## Example:#ID:00

#NAME:ARM7-ARM9
#LENGTH:4
#CAPTURE:1
#INST:0, EXTEST
#INST:2, SCAN\_N
#INST:3, SAMPLE/PRELOAD
#INST:4, RESTART
#INST:5, CLAMP
#INST:7, HIGHZ
#INST:9, CLAMPZ
#INST:C, INTEST



#INST:E, IDCODE

#INST:F, BYPASS

#INST:

#ID:01

#BSDL:C:\3256at144\_1532.bsd



# JVC IR

JVC IR refers to products or systems related to infrared (IR) technology

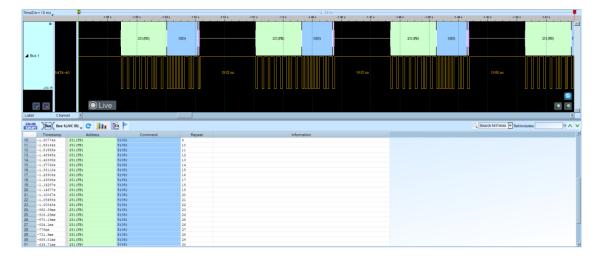
introduced by JVC (Japan Victor Company).

# Settings

JVC Settings				×
Channel		Color		
		Start Address Command		
Data	A0 🌻	Stop	•	
Range				
From Buffer Head	To Buffer Tail 👻	Opefault	✓OK XCancel	

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.





# LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits:

Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select

(E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

# Settings

📇 LCD16	02 Ver.1.0 Sett	ings							×
Paramete	ers								
	Channel								
: <b>-</b> /	RS	A0 :	DB0	ĺ	A3	DB4		A7	\$
	RW	A1 :	DB1	[	A4	DB5		A8	\$
	E	A2 :	DB2	[	A5	DB6		A9	\$
			DB3	(	A6	CB7		A10	\$
	Data Mode								
	8 Lines     8			(	🔿 4 Lii	nes			
	✔ To merge t	he same	command						
Color									
	SCREEN CLE	AR		•	CGRA	M AD SET			•
	CURSOR RET			•	DDRA	M AD SET			•
	INPUT SET			•	FUNC	TION SET			•
1	DISPLAY SWIT	гсн 📒		•	DATAV	WRITE			•
-	SHIFT			•	DATA F	READ			•
l	BUSY/AD REA	DCT		•					
Range									
<b>20</b>	Decode Rang	e							
From				То					
Buffer	Head		•	But	fer Tail				•
				De	efault	<	ĸ	<b>X</b>	Cancel



Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.

To merge the same command: Merge data with its command.

Time/Div = 1	0 ms						345.								
		114.93 #	114.94 s 114.95 s	114.96 # 1	114.97 # 114.98	114.99 #	116 #	115.01 #	115.02 #	115.03 #	115.04 x	116.06 #	115.26 #	115.07 *	115.00 #
	•														
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	CD 1902													(III) (i	
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ws															
110	î.														
E	2	7.93 mc 3.48 m	7.93 mc 3.48 m 7.93	ma 3.48 m 7.93 ma	: 3.48 m 7.93 m	3.48 m 1	93 ma 3.48 m 🗄	7.93 ma 3.48 m	7.93 mc 8.4	8 m 7.93 m	3.48 m	7.93 ms	3.48 m 7.93 ma	3.48 m 7.93 m	3.48 m
	_														
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		Ltive	81										Q Search All	ields 💌 Text include	
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# LED\_Ctrl

LED Controls are made specifically for digital type LEDs. These LEDs contain a special IC chips that allow the user to control each LED or section of LEDs.

# Settings

📇 LED_Ctrl Setting:	s				×
Parameters			Color		
Channel					
Data	A0	-	C1		-
Waveform Displa	ау		C2		*
value	O color		Data		•
			Data2		•
Chip Setting					
Model:	Custom -				
T0 Min:	300	us	T0 Max:	400 \$	us
T1 Min:	600	us	T1 Max:	1000 🗘	us
Reset:	Reset Low 👻	200	us		
Bit Size:	24-Bit 👻				
RGB Order:	R-G-B 💌				
Display:	Value 👻				
Range					
Decode R	Range				
From	То				
Buffer Head	▼ Buffer Ta	il 👻			
			ODefau	lt 🗸	Cancel

Channel: Show the selected channels.

Waveform display: show value or RGB color in waveform area.



### Chip setting:

#### Model: User can select the IC model. We now support TM1814 >

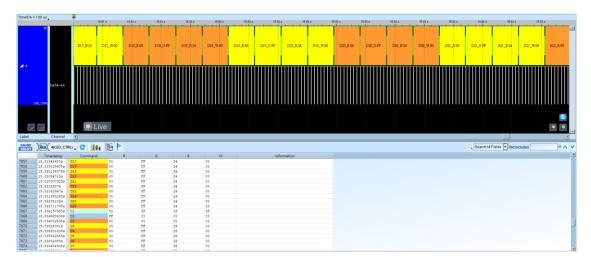
WS2811 VS2812 RT7905 HZ0028 and Custom

#### Condition: Idle high

If the time that waveform goes to low between T0 min and T0 max, the bit will decode as zero. If it's between T1 min and T1 max, the bit will decode as one.

**Reset:** if the waveform keeps at high potential over the time, the decoder will reset the start bit.

Bit size: choose 32-bit (WRGB) or 24-bit (RGB).





# LIN

LIN (Local Interconnect Network) is a serial network protocol used for communication between components in vehicles. LIN may be used also over the vehicle's battery power-line with a special LIN over DC powerline (DC-LIN) transceiver.

# Settings

LIN Settings	×
Settings	Color
LA Channel AO Show Scale Import LDF File Add Delete	Break  Delimiter Delimiter Sync Identifer Data Chusksum Wake-up Wake-up Range From To Buffer Head Buffer Tail U
Version          Image: Strain Strai	Default OK Cancel

LA Channel: Show the selected channel.

Show Scale: It will show the scales according to the bit width on the waveform.

Enabled when checked.

Import LDF File: Enable users to import the LIN Description File. Click on Add



and select LDF file.

**Version:** Different versions can be selected for LIN analysis. The Checksum verification after Lin version 2.0 has changed to two modes. If user need to use the enhanced verification below, user should select the version after 2.0 to use it.

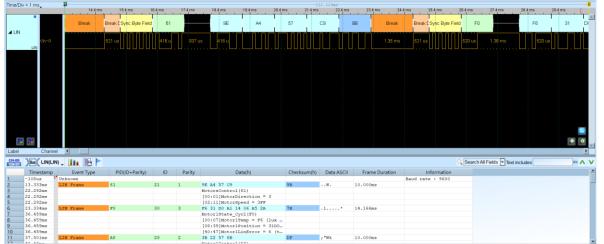
Baud rate: Show the selected baud rate.

**Checksum Mode:** Select the proper baud rate of the signal before the analysis. When set to auto, it will automatically detect the baud rate that matches the signal to be analyzed.

ne/Div = 1 ms	14.4 ms	s 15.4 ms	16.4 ms	17.4 ms	18.4 ms	19.4 ms 2	0.4 ms 21.4	132.324ms	ns 23.4 ms	24.4 ms	25.4 ms	26.4 ms	27.4 ms	28.4 ms	29.4 ms
•	13/4400001140	15 1 1 1	1			1	1	· · · · · · · · · · · · · · · · · · ·	· · · · · · · ·	· · · · · ·	1	1			1
	Break	Break E Sync Byte Fir	eld 61		9E	A4	57	C9	9B E	Break Brea	ak E Sync Byte Fie	ld FD		F6	31
N															
ch-0		521 us								.35 ms 521			1.36 ms		10
		521 US	416 U		us 1416 u						us	520 us	1.36 ms	520 us	
LIN															
															_
11 J.L															<i>,</i>
Chann	nel 🔳														
Bus LIN(LI	IN) 🖕 🚺 💼 🏲											C Search Al	I Fields 👻 Text i	includes	EX
Timestamp	Event Type	PID(ID+Parity)	ID	Parity		ta(h)	Checksum(h)			ion	Information				
13.333ms	LIN Frame	61	21		9E A4 57 C9		9B	W.	10.000ms						
23.334ms	LIN Frame	FO	30		F6 31 D0 A1 14	06 A5 2A	7B	.1*	14.166ms						
37.501ms	LIN Frame	A8	28		3B 22 57 6B		DF	;"Wk	10.000ms						
47.501ms	Diagnostic Frame	3C	3C	0	00 FF FF FF FF	FF FF FF	00		12.917ms						
64.377ms	LIN Frame	61	21		9E A4 57 C9		9B	W.	10.000ms						
74.377ms	LIN Frame	F0	30		F6 31 D0 A1 14	06 A5 2A	7B	.1*	14.167ms						
88.545ms	LIN Frame	A8	28		3B 22 57 6B		DF	;"Wk	10.000ms						
98.545ms	Diagnostic Frame		3C		00 FF FF FF FF	FF FF FF	00		12.916ms						
115.421ms	LIN Frame	61	21		9E A4 57 C9		9B	w.	10.000ms						
	LIN Frame	FO	30		F6 31 D0 A1 14	06 A5 2A	7B	.1*	14.166ms						
139.588ms	LIN Frame	A8	28	2	3B 22 57 6B		DF	;"Wk	10.000ms						
		10	20		00 mm mm mm mm				10.012						

#### Result

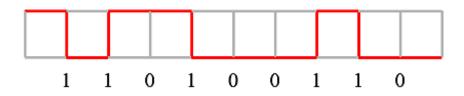
## The decoder with LDF



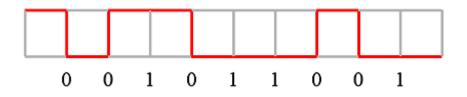


# Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes: NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.



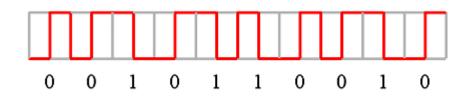
**NRZI (Transition occurs for a zero):** A 0 is represented by a transition of the physical level, a 1 has no transition.



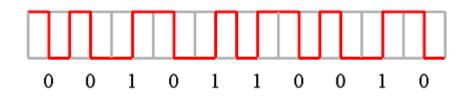
**Manchester:** In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

**Manchester (Thomas):** A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.

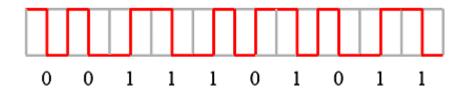




**Manchester (IEEE802.3):** A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



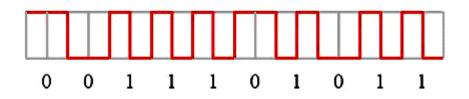
**Differential Manchester:** A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



**Bi-phase Mark:** The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult.



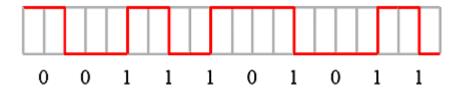
When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



**Modified Miller:** The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation



data demodulation circuit for producing NRZ - L data by utilizing the clock bits,

data bits and synchronizing clock pulses which are output from the data separation circuit.

This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



#### Settings

📇 Line Decoding Settings	;		×
Select Decoding			Select Waveform Format For Encode.
			And Set The Parameters
Data Channel	AO	÷	NRZI (Transition occurs for a one) 💌
Range			1 1 0 1 0 0 1 1 0
Decode Range			Show Unknown Show Bus
From	To Duffee Teil	_	✓ Auto-Detect Data Rate
Buffer Head 👻	Buffer Tail	× .	Data Rate 1 MHz
			Default VOK XCancel

Select Decoding: Set the channel number of the Logic Analyzer to which each

signal end is connected on the object to be tested.

Select the line code that user want to decode:

- I. NRZI (Transition occurs for a one)
- II. NRZI (Transition occurs for a zero)
- III. Manchester (Thomas)



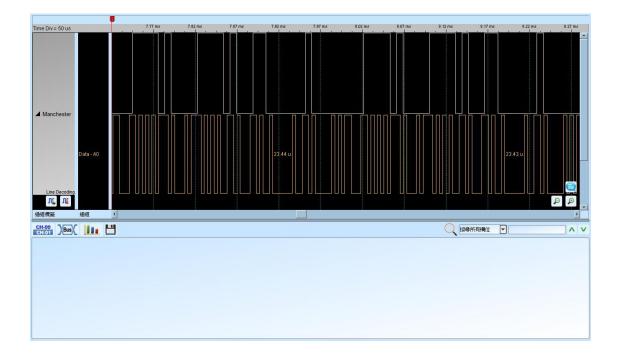
- IV. Manchester (IEEE802.3)
- V. Differential Manchester
- VI. Biphase Mark Decode
- VII. Miller
- VIII. Modified Miller

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date

Rate is not selected.





# Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes: NRZI (Transition occurs for a one): A 1 is represented by a transition of the

physical level, a 0 has no transition.

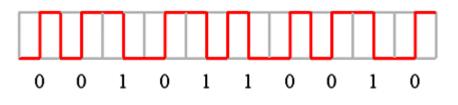


**NRZI (Transition occurs for a zero):** A 0 is represented by a transition of the physical level, a 1 has no transition.



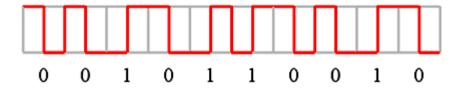
**Manchester:** In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

**Manchester (Thomas):** A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.





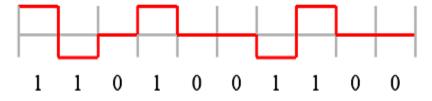
**Manchester (IEEE802.3):** A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



**Differential Manchester:** A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit, i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.

AMI (Alternate Mark Inversion): There are four modes:

**AMI (Standard):** AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.

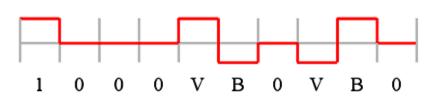


AMI (B8ZS): Bipolar-8-Zero Substitution

If 1 is +, 00000000 is represented to 000+-0-+

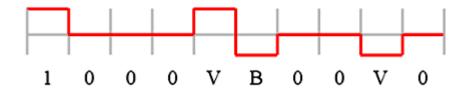
1 is -, 00000000 is represented to 000-+0+-





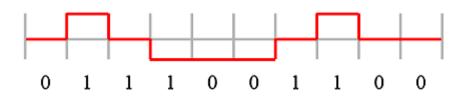
#### AMI (HDB3): High Density Bipolar 3

The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.

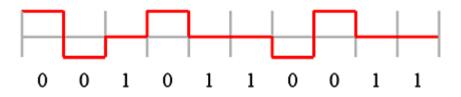




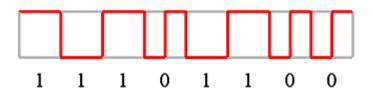
**MLT-3: Multilevel Transmission 3:** A 0 means no transition happens, a 1 is represented by a transition (0, +, 0, -).



Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).

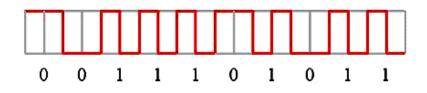


**CMI (Coded Mark Inversion):** A zero is sent a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].



**Bi-phase Mark:** The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.

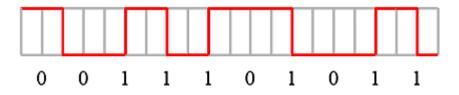




Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



**Modified Miller:** The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit.



This structure enables the M 2 modulation data which is input to the M 2

demodulation circuit to be easily demodulated to an NRZ - L type data signal by

means of a very simple circuit structure. An example is as below:



#### Settings

Line Encod	ding Settings				×
Select Enco		n occurs for a one) V	Channel	Data Channel A0	-
			Range	Decode Range From	
	Auto-Detec	t Data Rate		Buffer Head	~
	Data Rate	1 MHz		То	
	Data Kate	111112		Buffer Tail	~

Select Encoding: Set the channel number of the Logic Analyzer to which each

signal end is connected on the object to be tested.

Select the line code you want to encode:

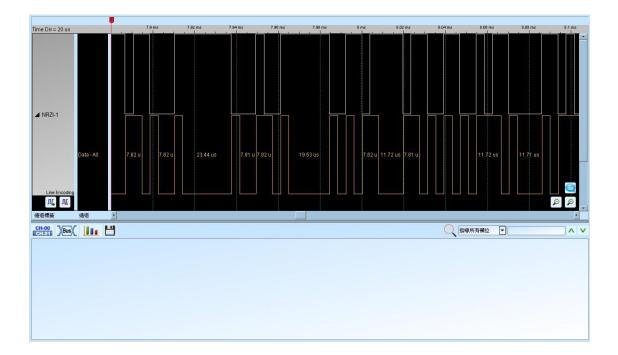
- I. NRZI (Transition occurs for a one)
- II. NRZI (Transition occurs for a zero)
- III. Manchester (Thomas)
- IV. Manchester (IEEE802.3)
- V. Differential Manchester
- VI. AMI (Standard)
- VII. AMI (B8ZS)



- VIII. AMI (HDB3)
- IX. Pseudoternary
- X. MLT-3
- XI. CMI
- XII. Biphase Mark Encode
- XIII. Miller
- XIV. Modified Miller

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date

Rate is not selected.





# LPC

The LPC bus, for the data transmissions, was developed by Intel to replace the

ISA bus.

#### Settings

📇 LPC Set	tings						$\times$
Setting							
	LFRAME# LAD[0]	A1	LAD[2] LAD[3]	A4 🗘	LCLK Data Edge	A0 🜲 Rising 💌	
	LAD[1] Show the field V START V CYCLETYF V SIZE V TAR						
Color –	ADDR     CHANNE     DATA     SYNC     SYNC	L				•	
	OTADT			ADDR			
	START CYCTYPE+DIR			DATA			
	CHANNEL	-		SYNC	-		
	TAR	•		IDSEL	•		
	SIZE/MSIZE	•		STOP	•		
Range	Decode F From Buffer He		To Buffer Tail	•			
	Default			[	<b>√</b> 0К	*Cancel	

**LCLK:** Transfer clock of LPC.

**Data Edge:** Latch the data to be analyzed when the LCLK is rising or falling.

LFRAME#: Marks the start of each Frame transfer cycle or is used to interrupt



Frame transfer.

**LAD[0-3]:** The data bus is used to transfer commands, addresses, and data.

Show the field in report: To enable report filtering, simply check the items to

be displayed in the report window.

Time/Div= 100 n	ns,	<b>a</b> 00.40	s 00.45 s	90.45 s	0.45 s 90.4	e5 s 90.45 s	271.37s 00.45 s 00.45 s	00.45 s 00.45 s 00.4	6 s 00.46 s 00.46 s	60.45 s 90.45 s 90.45 s
	•	TAR		STAF IA	R ADDR(0): 0064	TAR(0) 6	6 6 6 6 6 6 6 6 6	6 6 6 0 15 TAR	m	ETAN I/O R ADDR(0): 0066 TAR(0)
	LCLR-AO		35 16						35 86	
	LTRAME#-#	u		25 na						25 m
LPC Bus	LAD[0]-A2				175 au	65 m	415 as		445 m	375 na 65 na
	LAD[1]-A3	3		11	na 35 na 25 na		450 as	90 100	205 na	115 ns 25 ns
	LAD[2]-A4	1		11	ns		515 m	25 no 35 no 25 no	385 na	115 as
	EAD[3]-AS	;								175 m 60 m
U	~									
DX. DV		OLiv	9							
JK, JK Label	Channel	O Live	e							
Label		PC) , C							Q	Search All Fields Text includes
Bu	LPC Bus(L	PC) C		AD		Comment	a		٩	F
7712 90.	LPC Bus(L Timestamp 457239505a	PC) C III	#Clocks 2 FF			Commen	a		Q	
712 90. 90.	LPC Bus(L Timestamp 457239505a 45723980a	PC) C III Field TAR START	#Clocks 2 FF 1 0	Used for Memory	or 1/0 or EMA cyv	Commen	a		Q	
712 90. 7713 90. 7714 90.	LPC Bus(L Timestamp 457239505e 457239505 45723991s	Field TAR START CYCLETYPE+DIR	#Clocks 2 FF 1 0 1 0	Used for Hemory I/O Read	or 3/0 or IMA cyr	Commen	a		۹	<u> </u>
7712 90. 7713 90. 7714 90. 7715 90.	LPC Bus(L Timestamp 4572395058 4572395058 457239918 457239918	Field TAR START CYCLETYPE+DIR ADOR	#Clocks 2 FF 1 0 1 0 4 0064	Used for Hemory I/O Read	or 1/0 or EMA cyr	Commen	a		Q	<u> </u>
7712 90. 7713 90. 7714 90. 7715 90. 7716 90.	LPC Bus(L Timestamp 4572395058 457239508 457239918 457239948 4572400658	Field TAR START CYCLETYPE+DIR ADOR TAR	#Clocks 2 FF 2 0 1 0 4 0064 2 FF	Used for Hemory I/O Read	or 1/0 or DMA cyv	Commen	a		٩	<u> </u>
7712 90. 7713 90. 7714 90. 7715 90. 7715 90. 7717 90.	LPC Bus(L Timestamp 4572395058 457239508 457239918 457239948 457240658 4572405458	Field Field TAR START CYCLETYPE+DIR ADOR TAR TAR	#Clocks 2 FF 1 0 4 0066 2 IF 2 IS	Used for Hemory I/O Read	or 1/0 or IMA cyr	Commen	a		Q	<u> </u>
H-00         XBu           712         90.           713         90.           714         90.           715         90.           716         90.           717         90.           718         90.	LPC Bus(L Timestamp 4572395058 457239508 457239948 457239948 457240658 457240658	Field Field TAR BTART CYCLETYPE+DIR ADOR TAR DATA TAR DATA TAR	#Clocks 2 FF 2 0 1 0 4 006 2 FF 2 15 2 FF	Used for Hemory I/O Read		 Commen	4 		Q	<u> </u>
H-00         XBu           712         90.           713         90.           714         90.           715         90.           716         90.           717         90.           718         90.           719         90.	LPC Bus(L Timestamp 457239505# 45723958# 45723994# 45724005# 45724005# 45724005# 45724005#	Field Field TAR START CYCLETYPE+DIR ACOR TAR EATA TAR START	#Clocks 2 FF 1 0 1 0 4 006 2 FF 2 15 2 FF 1 0	Used for Hemory 1/0 Read Used for Hemory	or 1/0 or 100 cyn	 Commen	a		Q	<u> </u>
H-00         XBu           712         90.           713         90.           714         90.           715         90.           716         90.           717         90.           718         90.           719         90.           720         90.	LPC Bus(L Timestamp 457239505# 45723950# 45723954# 457240065# 457240545# 45724065# 45724065# 45724065# 45724098#	Field Field TAR STAR START CYCLETYPE+DIR ACCR TAR START TAR START CYCLETYPE+DIR	#Clocks         2         FF           2         FF         0           1         0         0           2         FF         2           2         FF         2           2         FF         1           1         0         0	Used for Hemory I/O Read Used for Hemory I/O Read		 Commen	4		Q	<u> </u>
H-00         But           7712         90.           7713         90.           7714         90.           7715         90.           7717         90.           7718         90.           7719         90.           7719         90.           7719         90.           7719         90.           7720         90.           7721         90.	LPC Bus(L Timestamp 457239505 457239505 457239948 457239948 457240655 457240655 457240655 457240655 457240165	Field TAR Field TAR START CYCLETYPE+DIR ADOR TAR DATA TAR DATA TAR DATA CYCLETYPE+DIR ADOR	Clocks  Clocks Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks  Clocks	Used for Hemory I/O Read Used for Hemory I/O Read		 Commen	4		٩	<u> </u>
H-00         But           7712         90.           7713         90.           7714         90.           7715         90.           7716         90.           7717         90.           7717         90.           7719         90.           7720         90.           7721         90.           7721         90.           7721         90.           7721         90.	LPC Bus(L Timestamp 457239505# 457239505# 45723954# 457240065# 457240065# 457240065# 457240065# 45724098# 45724104#	Field Field TAR BTART CCULETYDE+DIR ACCR TAR DATA TAR START CCULETYDE+DIR ACCR TAR TAR TAR	#Clocks           2         FF           1         0           4         0064           2         FF           1         0           4         004           0         4           0         1           1         0           4         004           2         FF           1         0           4         004           2         FF	Used for Hemory I/O Read Used for Hemory I/O Read		 Commen	a		q	<u> </u>
H-00         But           7712         90.           7713         90.           7714         90.           7715         90.           7716         90.           7717         90.           7718         90.           7719         90.           7720         90.           7722         90.           7723         90.	LPC Bus(L Timestamp 457239505 457239513 457239543 457240065 457240065 457240065 457240065 457240065 45724005 457241055 4572411655	Field TAR Field TAR TAR TAR TAR TAR TAR TAR CICLETIFEADIR ACCR TAR TAR TAR TAR TAR TAR TAR TAR TAR	#Clocks           2         FF           2         FF           1         0           4         0064           2         FF           1         0           4         0044           2         FF           2         2           1         0           4         0044           2         FF           2         15	Used for Hemory I/O Read Used for Hemory I/O Read		 Commen			Q	<u> </u>
24.00         But           7712         90.           7713         90.           7714         50.           7715         90.           7716         90.           7717         90.           7718         90.           7719         50.           7720         90.           7721         90.           7723         90.           7724         90.	LPC Bus(L Timestamp 457239505 457239505 457239505 457239513 4572400655 4572400655 4572400655 457240055 457240055 457241055 457241055	Field TAR TAR CULETIVE+DIR ACCR TAR TAR TAR TAR TAR TAR TAR TAR TAR	Clocks           2         FF           1         0           4         0064           2         FF           2         FF           1         0           4         0064           1         0           4         0064           2         FF           2         FF           2         TF           2         TF           2         TF           2         TF	Used for Memory I/O Read Used for Memory I/O Read	or 1/0 or IMA cy	Commen cles.	a		q	
CH.00         CH.00           C1101         XBu           77712         90.           77713         90.           77714         90.           77715         90.           77716         90.           77717         90.           77718         90.           77719         90.           7720         90.           7722         90.           7723         90.           7724         90.           7725         90.	LPC Bus(L Timestamp 457239505# 45723954 45723954 45723954 45724065# 45724065# 45724065# 45724065# 45724104# 45724116# 45724116# 45724116#	Field Field TAR TAR TAR TAR TAR TAR TAR TAR	#Clocks           #Clocks           2           1           0           4           0064           2           1           0           4           0           4           0           4           0           1           0           2           12           0           1           0           1           0	Used for Memory I/O Read Used for Memory I/O Read Used for Memory		Commen cles.			Q	F
Chool         Constraint           Chiloti         Constraint           Chiloti </td <td>LPC Bus(L Timestamp 457239505 457239508 457239518 4572400658 4572400658 4572400658 4572400658 457240058 457241018 457241048 4572411658 4572411058</td> <td>Field TAR TAR TAR TAR CULETIVE+DIR ACCR TAR START CULETIVE+DIR ACCR TAR TAR TAR TAR TAR TAR TAR TAR TAR TA</td> <td>#Clocks           2         FF           1         0           4         0044           2         FF           1         0</td> <td>Used for Hemory I/O Read Used for Hemory I/O Read Used for Hemory I/O Read</td> <td>or 1/0 or IMA cy</td> <td>Commen cles.</td> <td></td> <td></td> <td>q</td> <td>F</td>	LPC Bus(L Timestamp 457239505 457239508 457239518 4572400658 4572400658 4572400658 4572400658 457240058 457241018 457241048 4572411658 4572411058	Field TAR TAR TAR TAR CULETIVE+DIR ACCR TAR START CULETIVE+DIR ACCR TAR TAR TAR TAR TAR TAR TAR TAR TAR TA	#Clocks           2         FF           1         0           4         0044           2         FF           1         0	Used for Hemory I/O Read Used for Hemory I/O Read Used for Hemory I/O Read	or 1/0 or IMA cy	Commen cles.			q	F
CHOOL         CHOOL           CT101         Que           CT101         Que           T7712         90.           T7713         90.           T7714         90.           T7715         90.           T7716         90.           T7717         90.           T7718         90.           T7718         90.           T7728         90.           T7721         90.           T722         90.           T722         90.           T725         90.           T726         90.           T727         90.           T724         90.           T725         90.           T726         90.           T727         90.           T726         90.           T727         90.           T727         90.           T726         90.           T727         90.           T727         90.           T727         90.           T727         90.	LPC Bus(L Timestamp 457239963 457239963 457239963 457239964 457240965 457240055 457240055 457240055 4572411655 4572411655 4572411655 4572412455 4572412455	Field Field TAR TAR TAR TAR TAR TAR TAR TAR	#Clocks           2         FF           1         0           4         0064           2         FF           2         FF           2         FF           2         FF           2         FF           3         0           4         0064	Used for Hemory I/O Read Used for Hemory I/O Read Used for Hemory I/O Read	or 1/0 or IMA cy	Commen cles.	a		q	F
Ct-00         Ct-00           Ct-00 <td>LPC Bus(L Timestamp 45723960s 45723960s 45723960s 45723960s 45724060s 45724060s 45724060s 457240989 4572405989 45724104s 45724104s 45724104s 45724105 45724105 45724123</td> <td>Field TAR TAR TAR TAR CULETIVE+DIR ACCR TAR START CULETIVE+DIR ACCR TAR TAR TAR TAR TAR TAR TAR TAR TAR TA</td> <td>#Clocks           2         FF           1         0           4         0044           2         FF           1         0</td> <td>Used for Hemory I/O Read Used for Hemory I/O Read Used for Hemory I/O Read</td> <td>or 1/0 or IMA cy</td> <td>Commen cles.</td> <td>4</td> <td></td> <td>Q</td> <td>F</td>	LPC Bus(L Timestamp 45723960s 45723960s 45723960s 45723960s 45724060s 45724060s 45724060s 457240989 4572405989 45724104s 45724104s 45724104s 45724105 45724105 45724123	Field TAR TAR TAR TAR CULETIVE+DIR ACCR TAR START CULETIVE+DIR ACCR TAR TAR TAR TAR TAR TAR TAR TAR TAR TA	#Clocks           2         FF           1         0           4         0044           2         FF           1         0	Used for Hemory I/O Read Used for Hemory I/O Read Used for Hemory I/O Read	or 1/0 or IMA cy	Commen cles.	4		Q	F



# LPT

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals. This decode only support EPP Mode.

#### Settings

📇 LPT(EP	P) Setting			×
Channel			Color	
	Data0(LSB)	CH 0 🗘	Read Address	
	Data[7:0] => [ CH 7	: CH 0]	Write Address	
	/nWrite	CH 8 🌲	Read Data 🗸 🗸	
	/nWait	CH 9 🗘	Write Data 💌	
	/nDStrb	CH 10 🌲	Range	
	/nAStrb	CH 11 🌲		
	/nInit	CH 0	Decode Range	
	/nIntr	CH 0	From To Buffer Head - Buffer Tail -	
[	Address Table R	eport		
ODef	ault		✓OK ★Cancel	]

Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other

channel will be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

/nAStrb: Indicates the address cycle.

/nInit: Indicates a termination cycle in order to return the interface to the



Compatibility mode. User can option to use this channel or not.

/nIntr: This is an interrupt signal. User can option to use this channel or not.

			-000.52 us	-60	0.42 us		-606.32 us		-606.22 u	di i	-806.12	at i	-606.02 u		405.92 us	-605	82 us	-606.72 us	-806.82 us	-805.52 us	-005.4	2 US - 4	905.32 us	-605.22 us	-805.12 us	-805.02 usi
0		in in		R/D:2B				R/D:64			R/D:			RÆ	-	_	R/D BB		R/D.00		R/D.07	distant.	R/D:FF		R/D F3	
	Data0-A			100.00	1.1	15 m:		102.04	165 m			_	170 ns	110.		i5 m		170 ns		165 ns	and set		100.11			
	Datal-A					5 as							500 ns					170 m		165 m						
	Data2-A						-				335 as		200 10					500 m								
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100 )Bus Tim -606. -15ns	Bus 1(LI nestamp 49ua	PT) C R/W Read Rrite	Addr/Data	28 25									D9 D1	10 D11	D12	D13 D1	4 D15						C	L Search All Fit	elds 💌 Text inclu	desR
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el 	Bus 1(L1) nestamp 49us 205ms 59ms 465ms 465ms 465ms 665ms 34ms 665ms 665ms 675ms	Row Row Read Krite Rrite Rrite Krite Krite Krite Krite Krite Krite Krite	Addr/Data Data Address Address Address Address Address Address Address Data Data Data Data Data	28 25 72 76 70 27 28 54 28 54 00 06	64 0F 64 0F 5A FT	85 77 05 77 0F 5A	88 04 88 0C 77 0F	88 88 00 08 77	00 00 00 00 00 00	07 07 5A 00 22	FF 0F 5A 00	F3 77 0F 5A	0A 00 77 0C 0F 77	SA FF OB	0F 0F 00	77 OC 5A OF 00 SA	22 77 0F	+d					2	L Search All Fi	elds 💌 Text inclu	des
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### Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR, OR,NAND, NOR, XNOR, Bit Shift operation for the combined value of channel or bus.

#### **Parameters Settings**

Operand Math Lis Operand 1:	st Condition
<pre></pre>	List Item to Operand Delete List Item
Result Color Condition Color Range Decode Range From To Buffer Head Buffer Tail	efault

#### 1. Channels Settings

i. Operand: The channel or bus for which the calculation is to be performed is automatically listed with the labeled name of the channel or bus in the current waveform window.



- ii. Operator: We support
  - 1. Arithmetic operator: + > > × > /
  - 2. Logic operator: AND \ XOR \ OR \ NAND \ NOR \ XNOR \ >> \ <<
- iii.  $\Gamma = J$  button: Add the equation to the Math List
- iv. Invert Bit Order: By default, when adding a new bus, the smaller channel number is lsb and the larger channel number is msb.

Users can reverse the order of lsb and msb by setting this option.

🎭 Bus	Settings		×
Qui	ck Setup 🔾 Us	er Defined	
÷			
	MSB	5	LSB
*	<b>7 € 5</b>	4 → 3 → 2	<b>↓</b> 1 <b>↓</b> 0 <b>↓</b>
		🖌 ОК	X Cancel

- v. Bit Shift Method: We support (i)Arithmetic Shift `(ii)Logic Shift `(iii) Rotate Circular Shift and (iv)Rotate through Carry Shift. Use with
   > and << in logical operators.</li>
- vi. Numeric Display: We support Hexadecimal 
   Decimal 
   Binary.
- vii. Math List: Displaying the equations added by the user, up to a limit of 8.
- viii. 「Add List Item to Operand J button: Adding the selected item from *Math List* to operand for user to select for further operating with other channel or bus. Those item that was added to operand is enclosed in a set of parentheses when it operates with other operand. Up 2 levels of parentheses are supported.
  - ix. <sup>¬</sup> Delete List Item <sub>J</sub> button: Deleting the selected item from *Math List*.



- 2. Waveform Settings:
  - i. Setting the color of frame that represents the calculated result.
  - ii. Setting the comparison condition and the frame color that matches the condition.
- 3. Case Settings:
  - i. Comparison Condition: We support >= > > > > > <= > < <  $\circ$
  - ii. Comparison Value: Entering the value of the condition to be compared. Supports hexadecimal and decimal representation.
- 4. Configure: Lists all the configure names so that users can quickly switch between different configures. The configure records a list of different equations.

#### **Operating Methods**

- 1. After selecting the operand and operator, click "=" to add the equation to the *Math List*.
- 2. Choosing the equations to be operated on.
- 3. Setting the color of frame that represents the calculated result.
- 4. Setting the comparison condition and entering the comparison value, also setting the color for displaying the matches frame.



# 

**Note:** After setting, press OK to write all the settings to a file and save it to the working directory (AqMath.bin). The file will be overwritten every time user press OK, so when user save the file, user need to save a copy of AqMath.bin in addition to the waveform file. When user open the waveform file, user need to place AqMath.bin in the working directory before opening the waveform file.



### **M-Bus**

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

#### Settings

🚐 MBus Settings	×
Channel	Color
<b>1</b>	
Channel	Start / Stop 🗾 🗸 Cl Field 📃
Master A0 🜲	L Field 🗾 Data 🗾
Polarity Auto 👻	C Field  Check Sum
Slave A1	AField
Polarity Idle Low 👻	Range
	Decode Range
✓ Auto Detect	From To
Baud Rate 9600 -	Buffer Head 🔹 Buffer Tail 💌
Detail	
Parity None -	
MSB First	
Adv. Report	
	ODefault ♥OK ★Cancel

Channel: Set the signal channel and polarity. If there is a Slave on the bus,

user can set up additional Slave channels. Enable when checked.

**Baud Rate:** The transmission speed of the signal. Checking Auto Detection will detect the baud rate by itself.

#### Detail:



- I. **Parity:** Parity error detect.
- **II. MSB First:** Displayed in MSB first format. Enabled when checked.
- III. Adv. Report: Advanced report. Enabled when checked.

Div= 5 ms	30 S.O.I.	s :	1.91 s 0.	192 5	0.02 s 0.00 s	3.80 s 3.84 s	3.94 s 3.95	s 0.05 s 0.00 s	3.80 s	0.47 s 0.47 s 0.49 s	a 0.00 s
•		) 34h 34h 58h 53	PEA 500, 100, 310, 10	60 650 580 130 13	98h 38h 35h 73h 78h 56h 34h 12h 1	AAN 2001 659h 7EEN 2111 2001 2005 2005 2010 2010 2010	205 3C2 165 585 175 175	580, 201, 221, 723, 785, 565, 341, 125, 241, 405, 3	1h 27h 55h 20h 20h 30h 33h 13h 1	15h 31h 30h Dai 32h 18h 13h 31h 18h 50h 34h	375, 181, 323, 181, <b>153, 583,</b> 363, 363,
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Maste	z-40										
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	nel ·									Q Search All Fields 💌 Text	
Bus MBus	nel I		C Field(b)	A Field(b)	CI Faild(s)	Licar Data(h)	Check Sum(h)	León	mation	C Search All Fields 💌 Text	
	nel I		C Field(h)	A Field(h)	CIField(h) Application rest(50)	User Data(h)	Check Sum(h)	Info	rmation	C Search All Fields 💌 Text	
Bus MBus	(MBus) C III	L Field(h)	SND_UD(53)					Info	rmation	Q Bearch All Fields 💌 Text	
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Date         MBus           Trmestamp         >>1334775s           >>33374665s         >>353376664s           >>2400644s         >>2400644s           >>2400645s         >>5005045s           >>5005045s         >>5005045s           >>5005045s         >>5005045s           >>5005045s         >>5005045s           >>5005045s         >>5005045s           >>5005045s         >>5005045s           >>001056715s         +<001056715s	All a Allow C IIII Telegram Format Long Trase Long Trase Long Trase Long Trase	L Field(h) 04 13 17 06 00	SHD_UD(53) RSP_UD(00) RSP_UD(00) SHD_UD(53) SHD_UD(53)	FE 05 02 FE FE	Application reset(50) Fixed data respond(73) Variable data respond(7 Data send(51) Data send(51) Data send(51)	10 76, 54, 34, 12, 03, 00, 25, 72 81, 60, 00, 00, 35, 61, 00, 00 78, 54, 34, 12, 24, 40, 01, 07 55, 60, 00, 60, 01, 31, 15, 31 00, 33, 02, 35, 13, 10, 65, 60 04, 37, 18, 02 10, 78, 06 01, 75, 04, 03, 02, 01, 24, 40 01, 94 02, 75, 75, 64, 31, 12, 00, 66	B1 3C 10 25 95	i inte	mation	् िराल्फ्स मन्दर 🖻 १७	
Build         MBus           Trmestamps         3.9133470758           3.9133470758         3.924006449           3.924006449         3.924006449           3.924006449         3.924006458           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           3.950050459         3.950050459           4.0016947155         4.00124901659           4.0214901659         4.0214901659	AMILAS , C IIII MANUAS , C IIII Telegram Format Single Character Long Trane Long Trane Long Trane Long Trane Long Trane Long Trane	L Field(b) 04 17 06 00 07	SND_UD (53)     RSP_UD (00)     RSP_UD (00)     SND_UD (53)     SND_UD (53)     SND_UD (53)	FE 05 02 FE FE FE	Application reset(50) Fixed data respond(73) Variable data respond(7 Data send(51) Data send(51) Data send(51)	10 76, 56, 34, 12, 63, 00, E9, 7E 01, 00, 00, 00, 35, 01, 00, 00 75, 66, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 53 064, 77, 15, 02 07, 79, 04, 03, 02, 01, 24, 40 01, 04 67, 79, 56, 56, 34, 12, 02, 04	B1 3C 10 25 95 55	jafe	mation	C Second Facts Tools	
Date         MBus           Immestamp	Milusi C IIII Telegran Format Ecog Trans Ecog Trans Ecog Trans Ecog Trans Ecog Trans Ecog Trans Ecog Trans	LField(h) 04 13 17 06 00 07	SND_UD (53)     RSP_UD (00)     RSP_UD (00)     SND_UD (53)     SND_UD (53)     SND_UD (53)     SND_UD (53)	FE 05 02 FE FE FE 07	Application reset(50) Fixed data respond(72) Variable data respond(7.) Data send(51) Data send(51) Data send(51) Data send(51)	10 76, 36, 34, 12, 05, 00, 25, 7E 31, 00, 05, 00, 05, 35, 01, 00, 07 78, 36, 34, 12, 24, 40, 01, 07 55, 60, 06, 60, 65, 13, 15, 31 00, 48, 01, 34, 15, 02, 18, 60 60, 47, 15, 15, 02, 18, 40 04, 47, 15, 04 77, 75, 64, 03, 00, 01, 24, 40 04, 97, 75, 64, 33, 12, 20, 00, 66 07, 91, 00, 00 07, 13, 00, 00 77, 13, 00 77, 13, 00 77, 13, 00 77, 13, 00 78, 10, 10 78, 10 78	B1 3C 10 25 95 55 20	Inde	mation	C, Second Paris 💌 ted	
Dian         Milus           1,133/1075s         3.223764695           3.223764695         3.2240644s           3.2240644s         3.2240644s           3.5240644s         3.5260545s           3.55055545s         3.5905545s           3.5905545s         3.5905545s           3.5905545s         3.99395559           4.001596715s         4.001596715s           4.021490165s         4.021490165s           4.021490165s         4.03567135s           4.03567135s         4.0557135s	Milus) C III Milus) C III Telegam Format Ecop Trame Long Trame Long Trame Long Trame Long Trame Long Trame Long Trame Long Trame Long Trame	L Field(h) 04 13 17 06 00 07 07 06	SND_UD (63)     RSP_UD (00)     RSP_UD (00)     SND_UD (63)     SND_UD (53)     SND_UD (53)     SND_UD (53)     SND_UD (53)	FE 05 02 FE FE FE 07 01	Application reset(50) Fixed data respond(73) Variable data respond(7 Data send(51) Data send(51) Data send(51)	10 75, 84, 34, 12, 64, 60, 25, 72 8, 60, 60, 60, 35, 61, 60, 60 75, 84, 34, 12, 24, 40, 01, 67 80, 60, 00, 00, 01, 31, 35, 33 80, 80, 00, 60, 00, 13, 15, 53 80, 77, 15, 62, 93 90, 73, 90, 40, 02, 02, 02, 24, 40 90, 77, 50, 64, 03, 63, 12, 00, 04 60, 57, 75, 56, 34, 12, 00, 06 61, 61, 61, 60 61, 61, 61, 60 61, 61, 61 61, 61, 61 61, 61	B1 3C 25 95 55 20 2A	jan ka	maion	् िकाल्डेस्व ग्रिस्ट 🖻 फ	
001 (011) (011) Trinestamp 3.013470783 3.03740783 3.03740783 3.03740784 3.032400445 3.02400445 3.02400445 3.02400445 3.0000455 3.00000455 3.000000000000000000000000000000000000	Miles C III Telegan Tomat Cong Fram Stopic Character Long Fram Long Fram Long Fram Long Fram Long Fram Long Fram Long Fram Long Fram	LField(b) 04 12 12 12 06 00 07 06 04	SND_UD (53)     RSP_UD (00)     RSP_UD (00)     SND_UD (53)     SND_UD (53)     SND_UD (53)     SND_UD (53)     SND_UD (53)     SND_UD (53)	FE 05 02 FE FE 07 01 03	Application reset(50) Fixed data respond(73) Variable data respond(7.) Data send(51) Data send(51) Data send(51) Data send(51) Data send(51) Data send(51)	10 75, 84, 34, 12, 64, 60, 25, 72 8, 60, 60, 60, 35, 61, 60, 60 75, 84, 34, 12, 24, 40, 01, 67 80, 60, 00, 00, 01, 31, 35, 33 80, 80, 00, 60, 00, 13, 15, 53 80, 77, 15, 62, 93 90, 73, 90, 40, 02, 02, 02, 24, 40 90, 77, 50, 64, 03, 63, 12, 00, 04 60, 57, 75, 56, 34, 12, 00, 06 61, 61, 61, 60 61, 61, 61, 60 61, 61, 61 61, 61, 61 61, 61	P1 3C 25 95 55 20 24 26	Jack Provide State	mation	् उध्यत्त्रभा Paris 💌 ted	



# MCTP over l<sup>2</sup>C

MCTP (Management Component Transport Protocol) over I<sup>2</sup>C is a transport binding that enables communication between management controllers and other components in a system using I<sup>2</sup>C as the physical layer.

MCTP is a transport-independent protocol, meaning it can work over various underlying buses like PCIe, SMBus/I<sup>2</sup>C, UART, and Ethernet. When MCTP operates over I<sup>2</sup>C/SMBus, it follows the I<sup>2</sup>C/SMBus protocol for message passing between MCTP endpoints.

#### Settings:

📇 МСТР	over I2C Settings	×
Channel		
	SCL A0 🗢 SDA A1 🗢	Advanced Decode Setting Control PLDM
Destina	ation Address Configuration	NCSI     Ethernet
Color _		
	DestinationAddres 🗾 👻	NVME -
	MCTP 🗨	SPDM -
	Control 🗸	
	PLDM -	Vendor PCI
	NCSI	Vendor IANA 🗾 👻
_	Ethernet 🗾	Message 🗾 🗸
Range	Decode Range	
	From To	
	Buffer Head 💌 Buff	er Tail 🔹
	Defa	ult VOK XCancel



**Channel:** Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Destination Address Configuration: Set the device address and its

corresponding protocol.

Advanced Decode Setting: Show the detail meaning of the raw data.

0hr= 50 us _	2									1.089									
ed: 17:26:22.870		0.16 ma	0.21 ma	0.25 ma	0.31 ma	8.26 ma	8.41	ma	0.46 ma	0.51 ma	0.56 ma	0.61 ma	0.00 ma	0.71 ma	0.76 ma	0.01 ma	8.16 mi	8.91 ma	
•																			· · · ·
			WR 1D (3A)	CMD: 10		Bytes: 32		Address 3	7	WR 45 (0C)	CMD: 21						WR ID (JA)	CMD: 10	Bytes:
				1.1															
			nannnnn		TRACTOR OF TRACTOR	nnnnnnn	ann manna	nnnnnnn	nnnnnm	nannnannan	nnnnnnnn	nnnnn r					nnnnnnnn	nnnnnnnn	пппп
IS_MCTP ot SOL-0														201.66 tas					
						100000000		00000000		100000000000000000000000000000000000000	000000000000000000000000000000000000000						00000000000		n n
SDA-1			15 m	25 w 35	u: 40		76 uz   30		76 us	15 m 25 m	20 10 15	15 te		196.66 us			15 w 25	u 35 u	
CTP over I2C																			
R 63		Live																	•
		Live																	0,
Channel																			•
			· III. B	F											C Search All Fiel	Ids	Text inc		
Bus BUS_MCT	Pover I2C(MC Address	CTP over I2C) 🛫 C			DEID SEID	SOM EON	I PlaSeq. 1	TO MsgTag	IC	MsgType			MsgBo		Q Search All Fiel	ids PEC			
Bus BUS MCT	Pover I2C(MC Address	CTP over I2C) U C CMD code ByteC			DEID SEID	SOM EON	1 PidSeq. 1	TO MsgTag	IC	MsgType			MsgBo		🔍 [Search All Fiel				
Bus BUS_MCTI amp (hhmmss.ms 17:26:22.877 17:26:22.878	Pover I2C(MC Address 46 (WR) 2 1D (WR) 1	CTP over I2C) C CMD code ByteC 11 0 20			DEID SEID	SOM EON	1 PlaSeq. 1	TO MsgTag	IC	MsgType			MsgBo		Q Search All Fie				
Bus BUS_MCTI amp (hhmmss.ms 17:26:22.077 17:26:22.078 17:26:22.078	4 Pover 12C(MC Address 46 (WR) 2 1D (WR) 1 46 (WR) 2	CTP over I2C) CCMD code ByteC 10 20 11			DEID SEID	SOM EON	f PlaSeq. 1	TO MsgTag	IC	MsgType			MsgBo		🔍 (Search All Fie				
Bus BUS_MCTI amp (htmmss.ms 17126122.077 17126122.078 17126122.078 17126122.078	+ Pover I2C(MC Address 9 46 (WR) 2 1D (WR) 1 46 (WR) 2 1D (WR) 1	CTP ever I2C) CCMD code ByteC 11 0 20 11 0 20			DEID SEID	SOM EON	f PlaSeq. 1	TO MsgTag	IC	MsgType			MsgBo		् (Search All Fiel				
Bus BUS MCTI amp (hhmmss.ms 17126122.877 17126122.878 17126122.878 17126122.878 17126122.878	Pover I2C(MC     Address     46(NR) 2     1D(NR) 1     46(NR) 2     1D(NR) 1     46(NR) 2	CTP over I2C) CCMD code ByteC CMD code ByteC 10 20 11 20 112 10 20 10 20			DEID SEID	SOM EON	I PizSeq. 1	TO MsgTag	IC	MsgType			MsgBo		🔍 Search All Fiel				
Bus BUS_MCTI amp (hhmmas.ms 17126122.077 17126122.078 17126122.078 17126122.079 17126122.079 17126122.079	Pover I2C(MC     Address     46(NR) 2     1D(NR) 1     46(NR) 2     1D(NR) 1     46(NR) 2     1D(NR) 1     1D(NR) 1	CTP over I2C) CCMD code ByteC CMD code ByteC 10 20 11 0 20 11 0 20 11 0 20 11 0 20			DEID SEID	SOM EON	1 PktSeq. 1	TO MsgTag	IC	MsgType			MigBo		C Search All Fie				
Bus BUS_MCTH amp (httmm:ss.mc 17:26:22.076 17:26:22.076 17:26:22.076 17:26:22.076 17:26:22.079 17:26:22.079 17:26:22.079	P over 12C(MC Address 46(WR) 2 1D(WR) 1 46(WR) 2 1D(WR) 1 46(WR) 2 1D(WR) 1 46(WR) 2	CTP over (2C) CCMD code ByteC 11 0 20 11 0 20 11 0 20 11 0 20 11 1 20 11 1 20			DEID SEID	SOM EON	I PidSeq. 1	TO MigTag	IC	MsgType			Msg8o		् Search All Fiel				
Bus, BUS_MCTT amp (htmmssms 17:26:22.076 17:26:22.076 17:26:22.076 17:26:22.076 17:26:22.076 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079	Address           Address           46 (WR)           1D (WR)           1D (WR)           46 (WR)           21D (WR)           12 (WR)           146 (WR)           21D (WR)           10 (WR)           46 (WR)           21D (WR)           10 (WR)	CTP over I2C) _ C CMD code ByteC 11 0 20 11 0 20 11 0 20 11 0 20 11 0 20			DEID SEID	SOM EON	I PlaSeq. 1	TO MsgTag	IC .	MsgType			MsgBo		C Search All Fiel				
Bus, BUS_MCTI amp (htmmss.mc 17126122.077 17126122.078 17126122.078 17126122.079 17126122.079 17126122.079 17126122.079 17126122.079 17126122.079	Address     Address     Address     46 (WR)     1     1     46 (WR)     1     1     46 (WR)     1     1     46 (WR)     1	CTP over I2C) CCMD code ByteC CMD code ByteC 11 0 20 11 1 1 0 20 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			DEID SEID	SOM EON	I PicSeq. 1	TO MsgTag	IC	MsgType			MigBo		् (Search All Fie				
Bux BUS_MCTI amp (htmmss.ms 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070 17126122.070	Address           46(%R)         2           1D(WR)         1           1D(WR)         1           1D(WR)         1	CTP over (I2C) CCMD code ByteC (1) 0 20 (1)			DEID SEID	SOM EON	I PitSeq. T	TO MsgTag	IC	MsgType			MsgBo		🔍 Search All Fiel				
Bus, Bus, MCTI amp Phanmas.mc 17128:122.077 17128:122.078 17128:122.078 17128:122.078 17128:122.078 17128:122.078 17128:122.078 17128:122.078 17128:122.080 17128:122.080 17128:122.080	Address         Address           46(WR)         2           1D(WR)         1	CTP over 12C) C CMD code ByteC 10 20 11 20			DEID SEID	SOM EON	I PlaSeq. 1	TO MsgTeg	IC .	MsgType			MsgBo		Q (Search All File				
Bus, BUS, MCTI amp (bhrmns.mc 17:26:22.070 17:26:22.078 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079 17:26:22.079	Address         Address           46(WR)         2           1D(WR)         1	CTP over 12C) C CMD code ByteC 10 20 11 20			DEID SEID	SOM EON	I PitSeq. 1	TO MsgTag	IC	MsgType			MigBo		् (Search All Fie				
Bux, BUS, MCT amp bitmmss.mc 17126122.077 17126122.078 17126122.079 17126122.079 17126122.079 17126122.079 17126122.079 17126122.079 17126122.080 17126122.080 17126122.080	4         CR0           Address         4           4         CR0           1D (WR)         1           44 (WR)         2           1D (WR)         1           46 (WR)         2           1D (WR)         1	CTP over 12C) CMD code ByteC 0 20 1 20			DED SED	SOM EON	I PitSeq. 1	TO MsgTag	KC	MsgType			Мьдво		् Search All File				



# MCTP over I3C

MCTP (Management Component Transport Protocol) over I3C is a transport binding that enables standardized communication between system management controllers and peripherals using the MIPI I3C (Improved Inter-Integrated Circuit) bus.

MCTP is a transport-agnostic protocol, meaning it can operate over various physical layers like PCIe, SMBus/I<sup>2</sup>C, UART, and Ethernet. When using I3C, MCTP benefits from its higher speed, dynamic addressing, and in-band interrupt support, making it a more efficient alternative to I<sup>2</sup>C/SMBus.

#### Settings:

📇 МСТР	over I3C Settings	×
Channel		
	SCL A0 🗢 SDA A1 🗢	Advanced Decode Setting Control PLDM
Destina	ation Address Configuration	NCSI     Ethernet
Color		,
	DestinationAddres 🗾 👻	NVME 🗸
	MCTP	SPDM -
	Control 🗾	
	PLDM -	Vendor PCI 🗸 🗸
	NCSI	Vendor IANA 🗾 👻
Range	Ethernet 🗸	Message 🗾 🗸
	Decode Range From To Buffer Head 💌 Buffe	r Tail 👻
	ODefaul	t VOK XCancel



**Channel:** Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Destination Address Configuration: Set the device address and its

corresponding protocol.

Advanced Decode Setting: Show the detail meaning of the raw rata.

Div= 2 us 🚬 斗	2.1 <i>ma</i>	2.1 m		7.1 ma	7.1 ma	2.11 ma	2.11 ma	7.11 ma	7.1	1ma	2.11 ma	7.12 ma	7.12 ma	7.12 ma	7.12 ma	7.12 ma	7.13 mi	7.13 ma
۰	RnW (0)	ACK	10	, i	RnW (0)		01 FF T(1)	10 06	T (0) 0	0 80 T	(0) 08	38		т (1	0			
H-03 501-0		2.61 us			6 us		1 ==		t us		us il i		6.69 us			6 us		
SDA-1				11	5.68 us		t.69 us	ULU	1.92 us	1.92	us III			12.04	us			
0	[						1 us		1 us	•	us							
1					5.68 us		1.69 us		1.92 us	1.9	us			12.04	US			
•					WR 1D (3A)		0 1 DestEID: FF	10	MogTag: 0	0 Reser	ed: 0 (0B)			PEC:38				
IS_MCTPev SCL-0			I		5 US		1 us		1 US		US		6.69 us			5 US		
MCTPoverI3C SDA-1			[	11	5.68 us		1.69 us		1.92 US	1.93	us 👖	Л		12.04	US			
× 14																		.•
Channel																		
Bus BUS_MCTPove	r13C(MCTPover13C)	C III		Þ												Q Search All Fiel	ds 💌 Text Include	PS
	dr HeaderVer DE		M EOM	PktSeq.	TO MsgTag	IC				P	IsgBody		PEC					
7.10684ms 1D(MR) 7.16065ms 1D(RD)	1 FF	10 1	1	0 1	0 0	MCTP Con IBI(AE)	trol(0)-Request	80 OB					38					
10.10264ms 1D(RD)	1 10		1	0 0	0 0	MCTP Con	trol(0)-Response		0				65					
13.1034ms 1D(MR) 13.157745ms 1D(RD)	1 FF	10 1	1	0 1	0 0	MCTP Con IBI(AE)	trol(0)-Request	80 OC					20					
		<b>FF</b> 1	1	0 0		MCTP Con	trol(0)-Response	00 00 0	0				05					
16.102825ms 1D(RD)	1 10																	



# **MCTP over SMBus**

MCTP (Management Component Transport Protocol) over SMBus is a transport binding that enables communication between management controllers and other components in a system using SMBus as the physical layer.

MCTP is a transport-independent protocol, meaning it can work over various underlying buses like PCIe, SMBus/I<sup>2</sup>C, UART, and Ethernet. When MCTP operates over I<sup>2</sup>C/SMBus, it follows the I<sup>2</sup>C/SMBus protocol for message passing between MCTP endpoints.

#### Settings:

🔜 МСТР	over SMBus Settings		×
Channel			
1	SCL A0 🗢 SDA A1 🜩	Advanced Decode Setting	
Destina	ation Address Configuration		
Color _			
	DestinationAddres -	NVME	•
	MCTP 🗾	SPDM	•
	Control		
	PLDM -	Vendor PCI	•
	NCSI	Vendor IANA	•
	Ethernet 🔹	Message	•
Range			
	Decode Range		
	From To		
	Buffer Head 👻 Buff	er Tail 🛛 👻	
	Defau	ilt VOK XCand	el



**Channel:** Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Destination Address Configuration: Set the device address and its

corresponding protocol.

Advanced Decode Setting: Show the detail meaning of the raw rata.

hr= 50 us												0894								
ld: 17:26:22.870		8.98 ms	8.21	ms	8.25 ms	8.31 ms	8.3	lê ma	8.41 ms		0 ms 0.61 ms	8.56 ms	8.61 ms	8.00 ms	8.71 ms	8.76 ms	8.81 ms	8.86 m	a 8.91)	md
۲																				1
				WR 1D (3A)	CMD: 10		Byter 32	-		Addance 3F	WR 45 (9C)	CMD: 2						WR ID (3A)	CMD: 10	Byte::
				nnnnnn	nnnnnnn	nnnnnnn	nnnnnn	nnnnrin	nnnnn	nnnnnnn	innnn minnnnnnnnn	nnnnnnnnnn						nnnnnn	nnnnnnnn	nnnnn
S_MCTP ov SC1-0																				
						П		П	100000	7									Π	
5DA-1				15 10 25	w 35 t	70 40	3 185	28.76 m	30 115		us 15 m 25	10 20 10	15 10 15 10		196.66 tts			15 w	25 m 35 x	75
Pover SMBUS																				
2 12	(	O Live																		•
Channe																				.•
	н 🔸			C    11													Q. Search All	Fields Text	includes	
	CTP over SMB	BUS(MCTP over	SMBUS) 🖵			DEID SEID	D SOM 6	EOM Picse	Ng. TO	MsgTag	IC MegTyp	e		MsgBoo	by the second seco		Q Search All		includes	
Bus BUS_M	H CTP over SMB	BU S(MCTP over	SMBUS) 🖵			DEID SEID	D SOM 8	EOM Plase	N9. TO	MsgTag	IC MegTyp	e		MsgBoo	by				includes	
Bus BUS_M	CTP over SMB	BUS(MCTP over CMD code 21	SMBUS) 🖕			DEID SEID	D SOM 6	EOM Plase	nq. TO	MsgTag	IC MsgTyp	e		MsgBoo	y				includes	
Bus BUS_M amp (hhmmssn 17:26:22.877 17:26:22.878	H 4 CTP over SMB ms Address 46 (WR) 10 (WR)	BU S(MCTP over CMD code 21 10	SMBUS) 🖵			DEID SEIC	D SOM 8	EOM PlaSe	NQ. TO	MsgTag	IC MegTyp	e		MsgBoo	y				Includes	
Bus BUS_M amp (hhommas n 17:26:22.877 17:26:22.878 17:26:22.878	H 4 CTP over SMB ms Address 46 (WR) 1D (WR) 46 (WR)	CMD code	SMBUS) 🖕 ( ByteCount 20			DEID SEIC	D SOM E	EOM PlaSe	nq. TO	MsgTag	IC MsgTyp	ie in the second se		MsgBoo	by .				includes	
Bus BUS BUS M amp (htmmssn 17:26:22.878 17:26:22.878 17:26:22.878 17:26:22.878	H 4 CTP over SMB ms Address 46 (MR) 10 (MR) 46 (MR) 10 (MR)	CMD code 21 10 21 10 21	SMBUS) 🖕			DEID SEIC	D SOM E	EOM PleSee	NQ. TO	MsgTag	IC MagTyp	ie		MsgBoo	y				includes	
Bus BUS_M amp (hummasn 17126122.877 17126122.878 17126122.878 17126122.878 17126122.878	H 4 CTP over SMB ms Address 46 (MR) 10 (MR) 46 (MR) 10 (MR) 46 (MR)	CMD code 21 10 21 10 21 21	SMBUS) ByteCount 20 20			DED SED	D SOM E	EOM   PletSee	ng. TO	MsgTag	IC MegTyp	e		MsgBoo	y				Includes	
Bus Bus Bus M amp (htmmss n 17:26:22.877. 17:26:22.878. 17:26:22.878. 17:26:22.878. 17:26:22.879. 17:26:22.879.	H 4 CTP over SMB ms Address 46 (MR) 10 (MR) 46 (MR) 10 (MR) 10 (MR) 10 (MR)	CMD code 21 10 2 21 10 2 21 10 2 21 10 2	SMBUS) 🖕 ( ByteCount 20			DEID SEIC	D SOM 8	EOM   Patse	Nq. TO	MsgTag	IC MsgTyp	ie		MsgBoc	by .				Includes	
Bus Bus Bus M amp (htmmssn 17126122.877. 17126122.878. 17126122.878. 17126122.878. 17126122.879. 17126122.879.	H 4 CTP over SMB CTP over SMB S CTP over SMB 46 (MR) 46 (MR) 10 (MR) 46 (MR) 10 (MR) 46 (MR) 4	CMD code 21 10 2 21 21 21 21 21 21 21	SMBUS) ( ByteCount 20 20			DEID SEC	D SOM 6	EOM PlatSee	Nq. TO	MsgTag	IC MigTyp	e		MsgBoo	by .				includes	
Bus Bus Bus M amp (himmiss n 17:26:22.877. 17:26:22.878. 17:26:22.878. 17:26:22.879. 17:26:22.879. 17:26:22.879. 17:26:22.879. 17:26:22.879.	H  CTP over SMB CTP over SMB Address 46 (NR) 10 (NR) 46 (NR) 10 (NR) 46 (NR) 10 (NR) 1	CMD code 21 10 2 21 10 2 21 10 2 21 10 2 21 10 2 21 10 2	SMBUS) ByteCount 20 20			DEID SEIC	D SOM E	EOM PletSee	Rq. TO	MsgTag	IC MigTyp	e		Msglioc	h				includes	
Bus, BUS_M amp (hhmman 17126122.077 17126122.078 17126122.078 17126122.079 17126122.079 17126122.079 17126122.079 17126122.079 17126122.080	H 4 CTP over SMB ms Address 10(RR) 10(RR) 46(RR) 10(RR) 46(RR) 10(RR) 46(RR) 46(RR) 46(RR) 46(RR) 46(RR)	CMD code 21 10 2 21 10 2 21 10 2 21 10 2 21 21 21	<b>SMBUS) (</b> ByteCount 20 20 20 20			DEID SEIC	D SOM 6	EOM   Pirse	rq. TO	MsgTag	IC MigTyp	e		MigBoo	by				includes	
Bun BUS_M anp Bhrmmsan 17126122.077. 17126122.077. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.000. 17126122.000.	H  CTP over SMB CTP over SMB S 46 (MR) 10 (MR) 46 (MR) 10 (MR) 46 (MR) 10 (MR) 46 (MR) 10 (MR)	CMD code 21 10 2 21 10 2 21 10 2 21 10 2 21 10 2 21 10 2 21 10 2 21	SMBUS) ( ByteCount 20 20			DED SEC	D SOM 6	EOM Plase	Nq. TO	MsgTeg	IC MigTyp	e		MigBoo	by				Includes	
Bun Bus M 17126122.877. 17126122.878. 17126122.878. 17126122.878. 17126122.878. 17126122.878. 17126122.878. 17126122.879. 17126122.880. 17126122.880. 17126122.880. 17126122.880.	H 4 CTP over SMB ms Address 46 (HR) 10 (HR) 46 (HR) 10 (HR) 46 (HR) 10 (HR) 46 (HR) 10 (HR) 46 (HR) 10 (HR) 46 (HR) 10 (HR) 46 (HR)	CMD code 21 10 2 21 21 21 21 21 21 21 21 21 21 21 21 21	SMBUS) ( ByteCount 20 20 20 20 20 20			DEID SEIC	D SOM 6	EOM   PlatSee	kq. TO	MsgTag	IC MingTyp	e		Msglioc	by .				includes	
Bus Bus M amp Bhrmmsan 17126122.077. 17126122.077. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.079. 17126122.000.	H 4 CTP over SMB CTP over SMB S CTP over SMB Address 40(NR) 10(NR) 46(NR) 46(NR	CMD code 21 10 2 21 10 2 21 21 21 21 21 21 21 21 21 21 21 21 21	<b>SMBUS) (</b> ByteCount 20 20 20 20			DEID SEIC	D SOM 6	EOM PlaSe	sq. TO	MsgTag	IC MigTyp	a		MsgBoa	by				Includes	



# Mobile Display Digital Interface (MDDI)

The Mobile Display Digital Interface (MDDI) is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link for connecting portable computing, communication, and entertainment devices to wearable micro displays. This decoder is based on VESA Mobile Display Digital Interface Standard Version 1.2, only Type I communication is supported in this decoder.

#### Settings

MDDI Settings	×
Channel	
MDDI STB A0 MDDI D0 +	
Color	
Packet Length 🔹	
Packet Header 🔹	
Packet Data	
Range	
Decode Range	
From To	
Buffer Head 💌 Buffer Tail 💌	
ODefault ✔OK ★Cancel	j

#### **Channel Settings**

MDDI STB: MDDI Strobe



MDDI D0+/-: MDDI Data 0 +/-

Configure the Channel setup for the decoder, and choose the data

source from Data 0+ or Data 0-.





## MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

#### Settings

MDIO Settings	×
Channel	Color
MDC A0	User can assign color for specific pattern.
Enable Preamble Counter	Preamble (PRE)
32 bits	Start of Frame (ST)
Data	OP Code (OP)
Data Edge:   Rising  Falling	PHY Address (PHYADR)
Range	Turnaround (TA)
Decode Range	DeviceType (DEVTYPE)
From To	Address (ADDR)
Buffer Tail 👻 Buffer Tail 👻	Data (DATA)
	ODefault ✔OK ★Cancel

**MDC:** Transfer clock of MDIO.

**MDIO:** Transfer data input/output of MIDO.

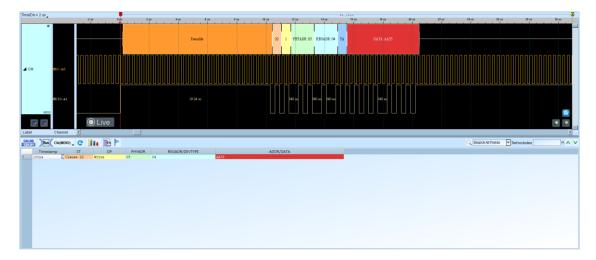
Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising

Edge default.

Enable Preamble Counter: Configurable MDIO Preamble width, 4 - 32 Bit,



default is 32 Bit. Enabled when checked.





## MHL-CBUS

Mobile High-definition Link (MHL) is an HD audio and video interface, Control

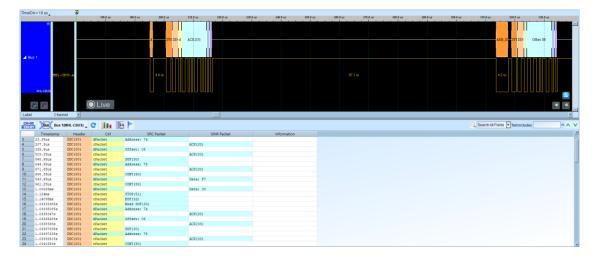
Bus (CBUS) is used to control it.

#### Settings

📇 CBUS Settings	×
Channel	Color
Channel	SYNC -
CBUS A0	HEADER
	cPacket 🗾
Banga	dPacket 💌
Range	CMD/DATA
Decode Range	PARITY -
From To	ACK 🗾
Buffer Head 💌 Buffer Tail 💌	Arbitration 🗾 👻
Defa	ult VOK XCancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.





# Microchip SWI

SWI usually refers to Single Wire Interface, a communication protocol provided

by Microchip Technology to simplify communication between devices.

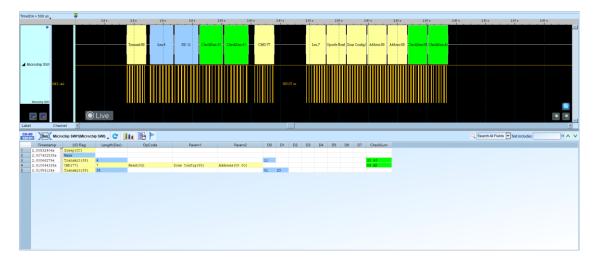
#### Setting

📇 Microchip_SWI Setting	s		×
Parameters		Color	
Channel			
SWI	A0	From Crypto	
Data Sheet	ATECC608B 👻	To Crypto 💌	
Range			
Decode Range			
From	То		
Buffer Head 👻	Buffer Tail 👻	ODefault ✓OK ¥Cancel	

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Data Sheet: Choose the supported IC model. We now support ATECC608B.





### Microwire

A serial signal format developed by National Semiconductor, the hardware structure and signal operation are the same as SPI (Serial Peripheral Interface). In the line structure, there are device selection line (CS: Chip Select), clock line (SK: Serial Clock) and data input/output line (DI: Data Input/DO: Data Output).

🚐 Microwire Settings	×
Channel	Color
Channel	ERASE / WRITE ENABLE
Chip Select Channel (CS) A0	ERASE / WRITE DISABLE
Clock Channel (SK) A1	ERASE -
Data In Channel (DI) A2	WRITE
Data Out Channel (DO) A3	READ -
	ERASE ALL -
Data	WRITE ALL
Chip Select Edge O Activate High O Activate Low Data Edge (DI) Rising Falling	Range
Data Edge (DO)   Rising   Falling	Decode Range
EEPROMs	From To
93xx46A or 93xx46C, 8 Bits -	Buffer Head 👻 Buffer Tail 👻
Report	
Show Data in Report 8 Columns -	
	ODefault ♥OK ¥Cancel

**Channel**: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Chip Select Edge: Active Low or Active High.

Data Edge: Rising or Falling.

**EEPROMs**: Select EEPROMs.



Report: Show data in report.

#### Result

Read

Time/Dir	= 20 US													90.503	ia.r																
		15.91 ms	15.93 ms		15.95 ma		15.97 ms		15.80 ms		16.01 ms	18.03 m	· N	.05 ms	16.07 ms	1	6.00 ms	16.11	ms .	16.1	ans	15	15 ms		16.17 ms		16.19	116	16.21	ns .	
	•		<u> </u>	<u> </u>	Т Т	<u>тт</u>	<u> </u>	ΤŤ	111	11				1111	<u> </u>	111	-	ŤΤΤ	T'T	TT	<b>T</b> <sup>+</sup> T	<u>'</u> T'T	111	<u> </u>	Т	11		11	11	1.101	
		Read Arti(	FF FF FF FF F	। जन्म	क क	ा जन चन	म मा मा	FFFF	यत् स्त व	FFF	स मा मा	FF FF FF	FFFFF	स स स	FFFF	FFF	स स म	FF FF	म म	म म	नग मन	ज्य यत	FF FF	17 17	FF FF	FFF	म मा	वित्र क	व पर स्व	FFFUA	
1			1 1 1 1	1.1	111	1.1	1.1	1.1	1 1 1	1.1	1.1	1 1 1 1		1 1 1	1.1	1 1 1	1.1	1 1 1	1.1	1.1	1.1	1.1	1.1	<u> </u>	1.1	1.1	1.1	1.1	1.1		
				_							_								_		_			_	_	_	_	_			
	Chip :	Selec																													
1																															
												Ш	ш																		
Micro	owire CLR-1																														
				_	_			_									_		_	_	_	_					_		_		
	Data	In-2 10.5																													
				ЦЦ		ШШ										ШШ			ШШ	ШШ									ШШ		
	Data	Out-3																													
L	ICROWIRE																														
																															_
		OLive																													
	5 <b>1 1 1</b>																													<b>P</b>	•
Label	Chann	nal I					_										_				_										
_	-			_	_	_		_	_	_	_				_	_		_	_	_	_	_	_	_	_	_	_	_	_	_	
CH-00 CH-01	Bus Micro	wire(MICROWIRE) 🖕 😋	lu 📑 🏲																					Q	Search Al	Il Fields	Text	t include	5	8	× ^ 1
CIT-OT	Timestamp	Command	Address	DO	D1	D2	D3	D4	D5 D	6 D7		CII(D0-D7)																			
32	12.2074ma	Commanu	Autoress	TT	FF	FF			FT FT	FF			-																		
	15.9050ms	Read	100						77 77	77																					
	15.9559ms	VCan.	100	77	77	77			7 77	TT																					
	15.993988			77	FF	FF			FF FF	FF																					
	16.0319ms			77	77	FF		77 1	77 77	TT																					
	16.0699ms			77	77	77	77 1	77 1	77 77	TT																					
	16.1079ms			77	FF	FF	TE I	FF 1	FF FF	FF																					
	16.1459ms			77	22	TT	77 1	FF I	TT TT	TT																					
	16.183988			TT	FF	TT	11 1	FF I	TT TT	FF																					
	20.2537ms	Read	140	TT	FF	FF	TE I	77 7	FE EE	TT																					
	20.2537ms 20.3038ms	Read	140		F7 F7	77 77	17 1 17 1	77 1 77 1	17 FF 17 FF	TT																					
42		Read	140		77 77 77	77 77 77	TT 1	17 1 17 1 17 1	17 17 17 17 17 17																						
42 43	20.3038ms	Read	140	77 77	22	TT	11 1 11 1	rr i	17 17 17 17	FF																					
42 43 44	20.3038ms 20.3418ms	Read	140	77 77 77	17 77	11 11	11 1 11 1	17 I 17 I	17 17 17 17	77 77																					
42 43 44 45 46	20.3030ms 20.3410ms 20.3790ms 20.4170ms 20.4550ms	Read	140	77 77 77 77	17 17 17	11 11		11 1 11 1 11 1 11 1	17 17 17 17 17 17	TT TT																					
42 43 44 45 46 47	20.3030ms 20.3418ms 20.3798ms 20.4170ms 20.4558ms 20.4558ms 20.4930ms	Read	140	77 77 77 77 77 77	17 17 17 17	11 11 11 11		11 1 11 1 11 1 11 1	17 17 17 17 17 17 17 17 17 17 17 17	77 77 77 77																					
42 43 44 45 46 47 48	20.3038ms 20.3418ms 20.3798ms 20.4178ms 20.4558ms 20.4558ms 20.4938ms 20.5318ms			77 77 77 77 77 77	17 17 17 17 17	11 11 11 11 11		11 1 11 1 11 1 11 1 11 1 11 1	17 17 17 17 17 17 17 17 17 17 17 17 17 17	TT TT TT TT																					
42 43 44 45 46 47 48	20.3030ms 20.3418ms 20.3798ms 20.4170ms 20.4558ms 20.4558ms 20.4930ms	Read	140	77 77 77 77 77 77 77	17 17 17 17 17	11 11 11 11 11 11			17 17 17 17 17 17 17 17 17 17 17 17 17 17	11 11 11 11 11 11																					

#### Write

ime/Div= 5	Sus,	-																			
			393.13 md	003.13 md	393.	.14 ms	200.	14 ms	360.15	ns .	393.15 ms	393.16 md	bm 01.000	200.17 md	200.17 ms	090.19 ms	393.99 md	003.10 md	bm 01.000	393.2 ms	300.2 ms
	•			Unknown					Weite	- 1	A-06D	98						aknown			
									_				_								
	Chip	p Selec						221													
Microwin	ire CLR-	-1							1	IMM	2.7 =	27 10									
	Date	a In-2							i i	: ce	2.5 m	3.1 12 1.3 1									
	ROWIRE	a Sut-3																			
MCR	HOWINE																				
			🔵 Live																		
Л.	- *																				₽.
.abel	Cha	• lenne																			
-H-00	Bus Micr	rowire(MICROWI	RE) 🖵 🔀 🚺																Q Search All F	ields 💌 Text Inclu	ides 🔤 e
	Timestamp		mmand	Address	DO	D1	D2	D3 D	4 D5	D6	D7 AS	CII(D0-D7)									
	89.5759ms	Write	06		D4																
	93.1489ms	Write	06		98																
13 39 14 40	96.722ms 00.295ms	Write	06		67						g										
	00.295ms 03.8681ms	Write Write	06		A8 28						+										
	03.8681ms 07.4411ms	Write	07		28 D4																
	11.0142ms	Write	07	1	72																
	14.5873ms	Write	07		12																
	10.1603ms	Write	07		12																
	21.7334ms	Write	07	5	76						v										
	25.3064ms	Write	07		47						0										
	28.8795ms	Write	07	7	1D																
	32.4525ms	Write	07		DD																
	36.0256ms	Write	07		41						à										
	39.5986ms	Write	07		68						0										
	43.1717ms	Write	07		C8																
	46.7447ms	Write	07	c	95																
	50.3178ms	Write	07		C7																
	53.8900ms	Write	07		36																
	57.4639ms	Write	07	T	67						g										
	64.6971ms	Write Enal																			
		Write	05		D5																
32 46	64.712ms																				



# MII / RMII / RGMII / GMII

MII: Media Independent Interface
RMII: Reduced Media Independent Interface
RGMII: Reduced Gigabit Media Independent Interface
GMII: Gigabit Media Independent Interface
Formulated by 802.3u that applied to Fast Ethernet, connecting MAC of
Data Link Layer and PHY layer. Its clock frequency is either 25MHz or
2.5MHz (Ethernet); they are TX\_CLK and RX\_CLK. TX [0:3], RX [0:3] are
4-bit-width bus and TX\_EN, RX\_EN enable the IN/OUT; TX\_ER, RX\_ER can
detect the errors on the bus; RX\_DV inform bus the data received is valid or not;
COL can detect the collision on the bus. Serial Management Interface (SMI),
also known as MDIO, is also an important part of MII.

### Settings

🚢 MII / RMII / GMII	/ RGMII Settings		×
Settings		Channel	
		Transmit(TX)	Receive(RX)
Protocol	MII	TX_CLK A0	RX_CLK A0
Mode	Transmit (TX) 💌	TX_D0 A1	RX_D0 A0
Data Edge	Rising	TX_D1 A2	RX_D1 A0
Report Columns	8 columns 🔹	TX_D2 A3	RX_D2 A0
RGMII Speed	1 Gbps 👻	TX_D3 A4	RX_D3 A0
RMII Clock	Normal	TX_D4 A8	RX_D4 A0
✓ DecodeEthern	et Packet (MAC)	TX_D5 A9	RX_D5 A0
Timing Specifics		TX_D6 A10	RX_D6 A0
Tskew = 0.000	ns	TX_D7 A11	RX_D7 A0
		TX_EN A5	RX_DV A0
		TX_ER A6	RX_ER A0
Color		TX_COL A7	
Ilser can a	ssign color for specific pattern.	Banaa	
		Range	
Data		Decode Range	
Collision	→ Idle	From To	
Preamble/SFD	✓ Others	Buffer Head 👻 But	fer Tail 👻
		Default	✓OK XCancel



Protocol: MII / RMII / GMII / RGMII can be selected. except BusFinder / LA,

TravelLogic and MSO do not support GMII.

**Mode:** Transmit (Tx) or Receive (Rx) mode can be selected.

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

### Data Edge:

**Rising:** Latch data when Clock edge is rising.

Falling: Latch data when Clock edge is falling.

### **Report Column:**

**8 Columns:** Set the data fields of the report window to be displayed in 8 columns.

**16 Columns:** Set the data fields of the report window to be displayed in 16 columns.

**RGMII Speed:** Set the speed of RGMII to 1Gbps or 100/10Mbps, valid only when MII is set to RGMII.

**RMII Clock:** Set the RMII Clock to Normal or Decrease Latch Frequency (x10).

Only available when MII is set to RMII.

**Decode Ethernet Packet (MAC):** Decode MAC packets. Enabled when checked.

**Timing Specifics:** Sets the delay or advance of the Data Latch. Available only when MII is set to GMII. Enabled when the check box is selected.



# Result

		£1.99 us	40 w 2 at 6 w 2 a 5.59 w	1.61 u 2 us 2.4 u 3. 61 u 2.61 u 2.4 u 3. 61 u 2.61 u 1.0000000000000000000000000000000000	2 1 2 1 6 1 2 1 2 1	15 m 2 m 1 m 2 m 12 m 2 m 2 m 1 m 2 m 12 m 2 m 2 m 1 m 2 m 12 m 2 m 2 m 1 m 2 m	2 w 2 w 24 w 1 2 w 2 4 w 3 6 w	6.4 us 6.4 us 5.6 us		
x (13-6) x (13-6) x (13-7) x (13		£1.99 us			──┘┟─┘└─┤└─┤└	124124 211 124	3.6 ts		1.5 w	
х (раз-р) х (раз-р										
R R										
Channel I	ive				57.59 m					
	(MII / RMI / RGMII / GMII) 🖵 💽						Q	Search All Fields 👻	Text includes	EX .
amp (hhmmss.ms Dest Addr (h) 14:21:159.766 14:21:159.766 14:21:159.766 14:21:159.766 14:21:159.766 14:21:159.766	Src. Addr (h)	Type(h) (rotocol)	45 00 00 27 50 11 38 DA C0 A8 01 FF 00 13 B2 19 6F 20 6C 73 00 00 00 00	33, 37 40 00 CO A8 01 65 LF 90 1F 90 E8 65 6C 6C 71 73 68 00	FC 8328633	5(h) 5				



# Mini / Micro-LED

The die positioning of display panel in Mini LED is  $100 \sim 200 \mu m$ , and Micro LED

is below 50µm.

Parameter S	Settings
-------------	----------

📇 MiniLED Settings			×
Parameters		IC Setting	
		Model User Defined	
Channel		Option	
DCLK		Mode	Data 👻
LE		Word Size	8 🔹
Data	A2 🗘	Bit Order	LSB First 👻
Quiles.		GCLK x	1 👻 🗌 DDR
Color		Data Edge	Rising -
		✓ Skip Data Bit	0 👻
CMD	•	(Skip Data Bit After CMD)	
Data Line 1	•	DelayTime	0 ns
Data Line 2	•	SDR max range is -GCLK DDR mas range is -GCLk (Unit: sample point)	
Range			
Decode Ran	ge		
From	То		
Buffer Head	▼ Buffer Tail ▼	○Default	Cancel

### Channel

- 1. DCLK: Default CLK channel
- 2. Data: Data channel
- 3. LE: The channel that can switch CMD or DATA

### IC Setting:

 Model: Setting the IC model number, currently supports ICND, MBI and User Defined; after selecting the model number, user can select the IC number again.



- 2. Mode: Set the Mode of the IC to Data or Command.
- 3. Word size: The number of the data bits.
- 4. Bit order: MSB/LSB first.

Docult

- 5. GCLK: The magnification of DCLK.
- 6. DDR: DDR mode. Enabled when checked.
- 7. Data Edge: Rising/falling latch.
- 8. Skip Data Bit: Set the number of skip data bit after LE falling
- 9. Delay Time: Set the time lead / delay in data line.

NDiv= 20 us	4.10 5 4.19 5	4.19 5	4.10 s	4.16 s	4.10 s	4.16 s	4.18 5	4.10 s	4.10 s	4.16 s	4.10 s	4.18 5	4.10 s	4.10 s	4.16 s
•	5 76			50							_				
DOLK-AO															
Command LE-A1		62.87 w		ΠΓ											
Data-A2	8.13 m		minim												
0	60 173 9	3 7D 73 83 2D 71 83	2D 71 83 2D	71				_							
DCLK-AO															
Data		62.87 w		пг											
Data-#2	0.13 w 11		החוורדורה												
MeetHoro LED															
	OLive														
· 推进 · 通道 ·															
00 VBus DALI21/MiniMicro I	ED) 🗸 🕑 🛄 📴 🏲												Q (ya)	所用欄位 💌 文字包含	DX
									D15	Information					



# **MIPI CSI**

MIPI CSI (Mobile Industry Processor Interface Camera Serial Interface) is a standardized data transfer protocol specifically designed to connect image sensors (such as camera modules) to processors (such as mobile phones, tablets or embedded devices). It was developed by the MIPI Alliance (Mobile Industry Processor Interface Alliance) to provide an efficient, low-power and high-speed data transfer channel.

### Settings

🚢 mipi	I CSI Settings		×
	el Settings LP Mode Channel	HS Mode Channel	
	Dp CH 0 🜲 Dn CH 1 🜲	Data Lane 1 D0+ Clock + CH 2 D2+ CH S Signal Source: BusFinder D-PHY Probe External DSO	CH 3 ♣ D1+ CH 4 ♣ CH 5 ♣ D3+ CH 6 ♣
[	<ul> <li>Advanced Decode</li> </ul>	Always o	goes to HS Mode
	Initial Bus Direction	Master -> S	Slave 💌
Color -	Start of Transmission	•	Word Count
	Transmission Mode		Data Frame
	Escape Mode Action	<ul> <li>End of Tra</li> </ul>	ansmission 🔹
	Data Identifier	- DSC	Command 🔹
Range	Decode Range		
	From	То	
	Buffer Head	✓ Buffer Tail	•
Def	ault		OK Cancel

**Dp**, **Dn**: The signal channel for DSI-LP mode.

Data Lane: The lane amount under DSI-HS mode.



Clock+, D0+, D1+, D2+, D3+: The signal channel under DSI-HS mode.

Enabled when checked.

Advanced Decode: Decodes the data in CSI format. Enabled when checked.

Always goes to HS Mode: Ignore the status of Dp and Dn in DSI-LP mode,

and always read the data as HS-Mode, enabled when checked.

**Initial Bus Direction:** Select the data transmission direction of the bus in the initial state.



# **MIPI DSI**

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

# Settings

🚞 MIPI I	DSI Settings	×
Channel	I Settings	
	P Mode Channel	HS Mode Channel
	Dp CH 0	Data Lane     1     •     D0+     CH 3     •     D1+     CH 4     •       Clock +     CH 2     •     D2+     CH 5     •     D3+     CH 6     •
	Dn CH1 🜲	HS Signal Source: BusFinder D-PHY Probe External DSO
V	Advanced Decode	Show DCS Command Always goes to HS Mode
In	nitial Bus Direction	Master -> Slave 💌
Color -		
	Start of Transmission	Word Count
	Transmission Mode	Data Frame
	Escape Mode Action	<ul> <li>End of Transmission</li> </ul>
	Data Identifier	DSC Command
Range -		
<b>*</b>	Decode Range	
	From	То
	Buffer Head	▼ Buffer Tail ▼
Defa	ult	OK Cancel

Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines



Advanced Decode: Enable DSI format decode and display.

Show DCS Command: Enable DCS Command decode and display.

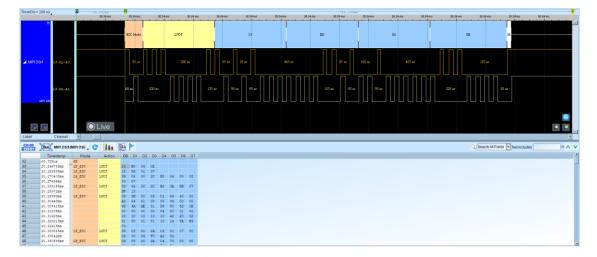
Always goes to HS Mode: Ignore the Dp and Dn status and decode all the

data frame in HS mode

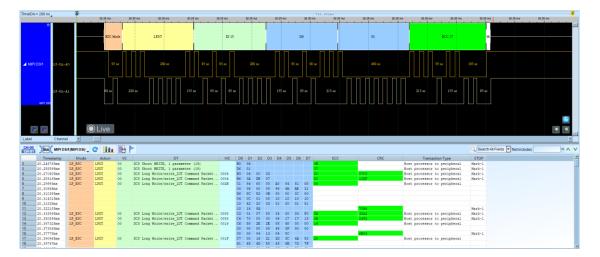
Initial Bus Direction: Select the Initial direction of the bus transmission.

#### Result

Advanced Decode Disabled:



Advanced Decode Enabled:





# **MIPI 13C**

MIPI I3C is an extension of I2C interface, so it still maintains the two-wire SCL (clock), SDA (data) as I2C. The frequency of MIPI I3C SCL clock is defined in spec. up to 12.9 MHz, and generally it is 12.5 MHz. It supports three operating voltages, 1.2 V / 1.8 V / 3.3 V. The MIPI I3C is a new generation of sensor interface specification, which integrates multiple sensor interfaces in one unified specification, mainly for simplifying the application of smart phone, smart phone, and sensor interface.

MIPI I3C is a new generation sensor interface specification that integrates multiple sensor interfaces in a unified specification, with the main application being to simplify sensor integration in smart phones, IoT devices, and automotive systems.

# Settings

📇 MIPI I3C Ver. 1.1.1 Settings						×
Channel		Color				
SCL	A0		S/Sr/P	•	RnW	•
SDA	A1 ;		ACK / NACK	•	T / PAR	•
Startup			Address	•	HDR Restart	•
Mode	I3C SDR Mode		Command	•	HDR Exit	•
Extended Operation			Data		HDR Flow Control	•
Extended Specification		Device C	onfiguration			
MIPI Debug Over I3C		DD	R5 Serial Presence Detect (	SPD)		
Report Detail Options		Cus	stom Device Settings		Add	Delete Edit
✓ Show CCC Datail			Device Type	Static Address	Dynamic Ad	dress
<ul> <li>Show Tenary Symbol</li> </ul>						
Range						
殿						
Decode Range						
From	То					
Buffer Head 👻	Buffer Tail					
Default						✓OK XCancel
Derault						



Channel:

- 1. Clock Channel (SCL): Transfer clock of I3C.
- 2. Data Channel (SDA): Transfer data of I3C.

**Startup:** Specifies the mode that is currently running on the bus. User can set the mode to:

- 1. I3C SDR Mode
- 2. I2C Mode
- 3. I3C HDR-DDR Mode
- 4. I3C HDR-TSP Mode
- 5. I3C HDR-TSL Mode

Extended Specification—MIPI Debug Over I3C: The command for debugging

I3C. Enabled when checked

### **Report Detail Options:**

- Show CCC Detail: Show the CCC(Common Command Code) information in report. Enabled when checked.
- 2. Show Ternary Symbol: Show the Ternary Symbol in report. Enabled when checked.

### **Device Configuration:**

- 1. DDR5 Serial Presence Detect (SPD): SPD function. Enabled when checked.
- 2. Custom Device Settings: Add user-defined device. User can add I<sup>2</sup>C

or MCTP device. Enabled when checked.

Device Type	
I2C -	
ddress	
Static Address (h)	DynamicAddress (h)
l	



# Result

Time/Div= 1		Ņ	442 #	4.42 s 4.42 s	4.42 z	442 1	4.42 = 4.42	16.99 • 442 =	9.5 s <b>4.42 s</b>	442 #	442 1		42 = 4.4	Q1 4/	42 x 4.42 x	442 1
Acquired: 16	20.19.711													in the t		
		7E 0		75	8F 1A 00		75 90 90	00 77 45		7E 0 3B 0/	4 00 FF		75	95 14 07		75
		12 0		12	ar 12 00			00 27 40		76 V DD A	0 00 FF		12	95 14 07		12
				100000												
∎ BUS_B	C_SLOT2 SC1-3							12.58								
	SDA-4	3 10		15.7 m 5.96 m	3 m 3.15 u		596 m 3 m	2.6 u 12.27	7 100	5.96 w 3 w	26u		596 m 3	au 200		5.96 m
R		(	OLive													
Label	Channe	_														•
		_	a <b>. C III</b>										QSeard	h All Fields	Text includes	
CH-00	Bus BUS_I3C_S	LOT2(MIPI I3	(c) <b>C</b> Address (h)	Comman		Data (h)		Error					C Seard		Text includes	
CH-00	Bus BUS_I3C_5	LOT2(MIPI I3	Address (h)	Comma	00	Data (h)		Emor	Provis	tioned ID Byte 0	1 (00)				Text includes	
CH-00 CH-00 CH-01 24 25	Bus BUS_I3C_S	LOT2(MIPH3 S/Sr S Wr			00	Data (h)		Emor	Provis [7:6]						Text includes	
CH-00 CHE01	Bus BUS_I3C_S amp (hhmm.ss.ms 16:20:24.138 16:20:24.138	LOT2(MIPH3 S/Sr S Wr	Address (h) 7E (Broadcast)	Comma	00 E)	Data (h)		Error		ISC Controlle: Supports optic	r-capable	nd capabiliti	Informati		Text includes	
CHL00 CHL01 24 25 26 27 28	Bus BUS_I3C_5 amp (hh:mm:ss.ms 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138	LOT2(MIPH3 S/Sr S Wr	Address (h) 7E (Broadcast)	Comma	00 E)	Data (h)		Error	(7:6) (5) (4)	ISC Controlle: Supports optio Not a Virtual	r-capable onal advance Target		Informati		Text includes	
24 25 26 27 28 29	Bus BUS_I3C_5 amp (hh:mm:ss.ms 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138	LOT2(MIPH3 S/Sr S Wr	Address (h) 7E (Broadcast)	Comma	00 E)	Data (h)		Error	(7:6) (5) (4) (3)	ISC Controlle: Supports option Not a Virtual Device will al	r-capable onal advance Target ilways respon	use to ISC Bu	Informati		Text includes	
CH-00 C1101 24 25 26 27 28 29 30	Bus BUS_J3C_5 amp 0h:mmss.ms 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138	LOT2(MIPH3 S/Sr S Wr	Address (h) 7E (Broadcast)	Comma	00 E)	Data (h)		Enor	(7:6) (5) (4) (3) [2]	ISC Controlle: Supports optio Not a Virtual Device will al One or more de	er-capable conal advance . Target ilways respon lata bytes fo	use to ISC Bu	Informati		Text includes [	
CH-00 CH-00 CH-01 24 25 26 27 28 29 30 31	Bus BUS_I3C_S amp (hh:mm:ss.ms 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138	LOT2(MIPH3 S/Sr S Wr	Address (h) 7E (Broadcast)	Comma	00 E)	Data (h)		Emor	(7:6) (5) (4) (3) [2] (1)	ISC Controlle: Supports option Not a Virtual Device will al One or more di IBI request co	er-capable conal advance . Target ilways respon lata bytes fo capable	nse to INC Bu	Informati		Text includes [	× ×
CH-00 CH-00 CH101 24 25 26 27 28 29 30 31 32	Bus BUS_J3C_5 amp (hh:mmss.ms 16:20:24,138 16:20:24,138 16:20:24,138 16:20:24,138 16:20:24,138 16:20:24,138 16:20:24,138 16:20:24,138	LOT2(MIPI I3 S / Sr S Nr Sz Rd	Address (h) : 7E (Broadcast) 0A	Comma Direct GETBCR (8	00 66	Data (h)		Emor	(7:6) (5) (4) (3) [2]	ISC Controlle: Supports optio Not a Virtual Device will al One or more de	er-capable conal advance . Target ilways respon lata bytes fo capable	nse to INC Bu	Informati		Text includes [	
24 25 26 27 28 29 30 31 32 33	Bus BUS_DC_5 amp (hhmmus.ms 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138	LOT2(MIPI I3 S/Sr S Wr Sr Rd	Address (h) 7E (Broadcast) 0A 7E (Broadcast)	Comma	E) 00 66 F)	Data (h)		Emor	[7:6] [5] [4] [3] [2] [1] [0]	ISC Controlle: Supports option Not a Virtual Device will al One or more de IBI request co No max data ap	er-capable conal advance . Target ilways respon lata bytes fo capable speed limitat	nse to INC Bu	Informati		Text includes [	× ×
CH-00 CH-01 24 25 26 27 28 29 30 31 32 33 34	Bux BUS_DC_5 amp 0hmmss ms 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130. 1612024,130.	LOT2(MIPI I3 S / Sr Sz Rd Sz Rd	Address (h) 7E (Broadcast) 0A 7E (Broadcast) 0A	Comma Direct GETBCR (8) Direct GETDCR (8)	E) 00 66 E) 00	Data (h)		Emor	[7:6] [5] [4] [3] [2] [1] [0]	ISC Controlle: Supports option Not a Virtual Device will al One or more di IBI request co	er-capable conal advance . Target ilways respon lata bytes fo capable speed limitat	nse to INC Bu	Informati		Text incluses (	
CH-00 CH-01 24 25 26 27 28 29 30 31 32 33 34 35	Bux, BUS_BC_S amp_thtmmss.ms 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138 16:20:24.138	S Wr Sr Rd	Address (h) 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast)	Comma Direct GETBCR (8	E) 00 66 F) 00 C) 00	Data (h)		Emor	(7:6) (5) (4) (3) (2) (1) (0) Generi	ISC Controlle: Supports opti- Not a Virtual Device will a One or more di ISI request or No max data sp c (for v1.0 Devi	er-capable conal advance . Target ilways respon lata bytes fo capable speed limitat	nse to INC Bu	Informati		Text includes [	
CH-00 CH-00 24 25 26 27 28 29 30 31 32 33 34 33 34 35 36	Ban, BUS, DC, S amp, Phomess me diciological, 188., 16120124, 188.,	S Wr Sr Rd	Address (h) 7E (Broadcast) 0A 7E (Broadcast) 0A	Comma Direct GETBCR (8) Direct GETDCR (8)	E) 00 66 F) 00 C) 00	Data (h)		Emor	(7:6) (5) (4) (3) (2) (1) (0) Generi MSB (00	<pre>ISC Controlle: Supports opti: Not a Virtual Device will a: One or more di IBI request o No max data sp c (for v1.0 Dev: )</pre>	er-capable conal advance . Target ilways respon lata bytes fo capable speed limitat	nse to INC Bu	Informati		Text includes [	× • • • •
CH-00 CH-00 24 25 26 27 28 29 30 31 32 33 33 34 35 35 35 35 37	Bux, BUS_BC_5 amp_themmus.ms 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138. 16:20:24.138.	S Wr Sr Rd	Address (h) 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast)	Comma Direct GETBCR (8) Direct GETDCR (8)	E) 00 66 F) 00 C) 00 FF	Data (h)		Enor	(7:6) (5) (4) (3) [2] (1) (0) Generi MSB (00 LSB (FF	ISC Controlle: Supports opti- Not a Virtual Device will al One or more di ISI request o No max data sp c (for v1.0 Dev: )	<pre>capable comal advance Target llways respon iata bytes fo apable upeed limitat rices)</pre>	nse to INC Bu	Informati		Text includes (	
CH.00 CCLO3 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38	Bun, BUS, DC, 5 amp, Ph. mmus.ms, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130,	LOT2(MIPH IS S/Sr S WE SE Rd S WE SE Rd	Addres(h) 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast) 0A	Comman Direct GEIBCR (8) Direct GEIDCR (8) Direct GEIBL (0)	E) 00 66 F) 00 C) 00 FT 66 00 FT 66 66 66 66 66 66 66 66 66 6	Data (h)		Enor	(7:6) (5) (4) (3) [2] (1) (0) Generi MSB (00 LSB (FF	<pre>ISC Controlle: Supports opti: Not a Virtual Device will a: One or more di IBI request o No max data sp c (for v1.0 Dev: )</pre>	<pre>capable comal advance Target llways respon iata bytes fo apable upeed limitat rices)</pre>	nse to INC Bu	Informati		Text Includes (	× × ×
24 25 26 27 27 28 29 30 31 32 33 33 34 35 36 37 38 39	BUS_DC_S BUS_DC_S 14:20:24.130. 14:20:24.130. 14:20:24.130. 14:20:24.130. 16:20:24.130. 1	LOT2(MIPI IS S/Sr S Wr Sr Rd S Wr Sr Rd S Wr Sr Rd S Wr	Addres(h) 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast)	Comma Direct GETBCR (8) Direct GETDCR (8)	E) 00 E) 66 F) 00 C) 00 E7 46 B)	Data (h)		Enor	(7:6) (4) (3) (2) (1) (0) Generi MSB (00 LSB (FF IBI Pa	<pre>ISC Controlle Supports opti Not a Virtual Device will a Device will</pre>	<pre>capable comal advance Target llways respon iata bytes fo apable upeed limitat rices)</pre>	nse to INC Bu	Informati		Test includes [	× ×
CHO0 CHO2 24 25 26 27 28 29 30 31 32 33 34 35 36 35 36 39 40	Bun, BUS, DC, 5 amp, Ph. mmus.ms, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130, 16:20:24,130,	LOT2(MIPI IS S/Sr S Wr Sr Rd S Wr Sr Rd S Wr Sr Rd S Wr	Addres(h) 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast) 0A	Comman Direct GEIBCR (8) Direct GEIDCR (8) Direct GEIBL (0)	E) 00 66 F) 00 C) 00 FT 66 00 FT 66 66 66 66 66 66 66 66 66 6	Data (h)		Enor	(7:6) (5) (4) (3) (2) (1) (0) (0) (0) (0) (0) (0) (0) (0) (0) (0	<pre>i3C Controlle Supports opti Not a Virtual Device will al One or more du 1B1 request o No max data sy o (for v1.0 Devi ) ) yload Size = 46 )</pre>	<pre>capable comal advance Target llways respon iata bytes fo apable upeed limitat rices)</pre>	nse to INC Bu	Informati		Text incluses [	× • • •
CH-00 CH-00 24 25 26 27 28 29 30 31 32 33 34 34 35 36 37 38 39 40 41	Bun, BUS, DC, 5 amp (b) mm is ma (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.) (4:20:24.130.)	LOTZ(MIP I S S/Sr S Wr Sr Rd Sr Rd S Wr Sr Rd S Wr Sr Rd S Wr Sr Rd	Addres(h) 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast) 0A 7E (Broadcast)	Comman Direct GEIBCR (8) Direct GEIDCR (8) Direct GEIBL (0)	E) 00 E) 66 F) 00 C) 00 ET 46 B) 00 ET FT	Data (h)		Enor	(7:6) (4) (3) (2) (1) (0) Generi MSB (00 LSB (FF IBI Pa	<pre>i3C Controlle Supports opti Not a Virtual Device will al One or more du 1B1 request o No max data sy o (for v1.0 Devi ) ) yload Size = 46 )</pre>	<pre>capable comal advance Target llways respon iata bytes fo apable upeed limitat rices)</pre>	nse to INC Bu	Informati		P Test includes [	× ×



# **MIPI RFFE**

MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

# Settings

MIPI RFFE Ver. 3.0 Settings	×
Parameters	Color
Operation	SSC Address / Mask
SCLK	SA/MID 🔽 Data 💽
SDATA A1 🗘 🔿 sRead	Command P
✔ User Define Slave ID	BC BP V
Slave ID Description Import	Range
	Decode Range
	From To Buffer Head
Save Protocol Data for Acute Data Generator (.PDT)	ODefault ✔OK ★Cancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

**Operation:** Set to Read or sRead.

User Define Slave ID: Add used-defined Slave ID. Enabled when checked.

**Save Protocol Data for Acute Data Generator (.PDT):** Save the analyzed result as .PDT file for the usage of Acute Data Generator. Enabled when checked.



# Result

ime/Div= 200 ns	<b>P</b>							
lcquired: 11:39:18.791	25.13 ms	25.13 ms 25.13 ms 25.13 ms	26.13 ms	25.13 ms	25.13 ms	25.13 ms 25.13 ms	25.13 ns 25.13 ns	25.13 ms 25.13 ms 25.13 ms 25.13 ms
×								
	Data: 04 P: 0 0	SDC SA:4 Ext. Reg.	Wr BC:0	P:0	Addams: CF	F 1 Dets: 00	P.1 0	SDC SA:4 Ext. Reg. Wy EC:0 P.0 Addusts: CC
			пппп			1		
BUS_MIPI RFF SOLR-0		195 as						
				JUUU				
SDATE-1	50 m	50 ns 100 ns 50 ns			as 100 ns 250 ns		50 ns 160 ns 50	D na 100 na 50 na 550 na 100 na 100 na
MIPL REFE								
and serve								
PL 11	OLive							• •
	0							
ibel Channel	•							
H-00 Bus BUS_MIPLE	RFFE(MIPI RFFE) 🔔 😋 🚺							Q Search All Fields Text includes
and a company								
:amp (hh:mm:ss.ms		Command	Byte Count		Mask	Data	Information	
	Spare (user-defined)(4)	Register Write Command		01	User-Defined R			
	Spare (user-defined)(4) Spare (user-defined)(4)	Extended Register Write Command Extended Register Write Command	0	CIF CC	User-Defined R User-Defined R			
	Spare (user-defined) (4) Spare (user-defined) (4)	Register 0 Write Command	0		Coer-Derined a	egiscers(00)		
	Spare (user-defined) (4)	Register Read Command		01	User-Defined B	egisters (00)	Parity Error	
	Spare (user-defined) (4)	Register Write Command		01	User-Defined R			
	Spare (user-defined) (4)	Extended Register Write Command	0	CF	User-Defined R			
	Spare (user-defined) (4)	Extended Register Write Command	0	CC	User-Defined R			
	Spare (user-defined) (4)	Register 0 Write Command			02			
	Spare (user-defined) (4)	Register Read Command		01	User-Defined R	egisters(00)	Parity Error	
	Spare (user-defined) (4)	Register Write Command		01	User-Defined R			
96 11:39:20.692	Spare (user-defined) (4)	Extended Register Write Command	0	CF	User-Defined R	egisters(00)		
	Spare (user-defined) (4)	Extended Register Write Command	0	CC 20	User-Defined R	egisters(00)		
	Spare (user-defined)(4)	Register 0 Write Command			02			
	Spare (user-defined) (4)	Register Read Command		01	User-Defined R		Parity Error	
	Spare (user-defined) (4)	Register Write Command		01	User-Defined R			
01 11:39:20.692	Spare (user-defined) (4)	Extended Register Write Command	0	CF	User-Defined R	egisters(00)		
02 11:39:20.692	Spare (user-defined) (4)	Extended Register Write Command	0	CC .	User-Defined R	egisters(00)		
	Spare (user-defined) (4) Spare (user-defined) (4)	Extended Register Write Command Register 0 Write Command	٥	cc	User-Defined R 02	egisters(00)		
103 11:39:20.692			0	01	02 User-Defined R	egisters(00)	Parity Error	
103 11:39:20.692 104 11:39:20.692	Spare (user-defined) (4)	Register 0 Write Command	0		02	egisters(00)	Parity Error	
103         11:39:20.692           104         11:39:20.692           105         11:39:20.692	Spare (user-defined) (4) Spare (user-defined) (4)	Register 0 Write Command Register Read Command	0	01	02 User-Defined R	egisters(00) egisters(04)	Parity Error	
103         11:39:20.692           104         11:39:20.692           105         11:39:20.692           106         11:39:20.692	Spare (user-defined)(4) Spare (user-defined)(4) Spare (user-defined)(4)	Register 0 Write Command Register Read Command Register Write Command	0	01	02 User-Defined R User-Defined R	ngisters(00) ngisters(04) ngisters(00)	Parity Error	



# MIPI SoundWire

Soundwire is a hardware interface and transport protocol developed by MIPI. It provides an expandable, simple, low-power, low-latency, dual-lead (clock and data) bus that can be used to transfer multiple audio streams such as amplifiers and microphones and embedded control commands.

Max Clock Rate:12.288MHz

annel		Startup Setting		Report Setting	s
Clock A0		Delay: Current Bank	40 ns		
		Bank 0	O Bank 1	Show Packet Table	
Data A1	<b>*</b>	Initial Frame Sha	pe		
ange		Bank 0	Bank 1		Ping OpCode
Decode Range		Row Colur 48 2			CP Frame Ctrl CMD
From Buffer Head	To Buffer Tail				
Enable PayLoad					
Туре:	PCM	<ul> <li>Sample Interval:</li> </ul>	96	Save as .wav	Save as .txt
Bank:	Bank 0	Offset 1:	0	O Full Scale	Playback
Device:	Device 0	Offset 2:	0		All
DPn:	DP0	Word Length:	0	Original	U 7 M
HStart	0	Audio Sample Rate	4000 Hz	Display Audio	O 5 Sec
	0	PDM Sample Rate:	4800 KHz	O Full Scale	
HStop				Original	🔘 3 Sec
HStop Block Packing Mode:	Block-per-Port				

**CLK:** Transfer clock of SoundWire.

Data: Transfer data of SoundWire.



Delay:	40 ns 🌲			
Current Bank				
Bank 0	O Bank 1			
nitial Frame Shape				
Bank 0	Bank 1			
Row Column	Row Column			
48 2 2	48 2 2			

**Delay:** Fix the position of latching data.

Bank: There are two types of parameters setting files, Bank0 and Bank1.

The Data port (DP) is the source or sink of the Payload Stream on the SoundWire bus, and the DP also divides the Payload Stream into one or more channels for each audio channel.

Initial Frame Shape: set the row and column of each setting file.

Column: 2~16(Only even) Row: 48~256 Report Settings Show Packet Table Hide all Ping OpCode

**Show Packet Table:** Show Packet Table (in 2-Dimension). Enabled when checked.

**Hide all Ping OPCode:** Hide all the Ping OPCode in report. Enabled when checked.

Ignore SCP Frame Ctrl CMD: Hide all SCP CMD in report for easy reading.



### Enabled when checked.

Enable PayLoad					
Туре:	PCM	Sample Interval:	96	Save as .wav	Save as .txt
Bank:	Bank 0	▼ Offset 1:	0	O Full Scale	Playback
Device:	Device 0	Offset 2:	0	Original	All
DPn:	DP0	Word Length:	0	Conginal	
HStart	0	Audio Sample Rate:	4000 Hz	Display Audio	O 5 Sec
HStop	0	PDM Sample Rate:	4800 KHz	O Full Scale	
Block Packing Mode:	Block-per-Port	- CH1 CH2	CH3 CH4	Original	🔿 3 Sec
Port Flow Mode:	Normal (isochronous)	- CH5 CH6	CH7 CH8	Conginal	

### DPn amount: 1~16, No. DP0~DP15

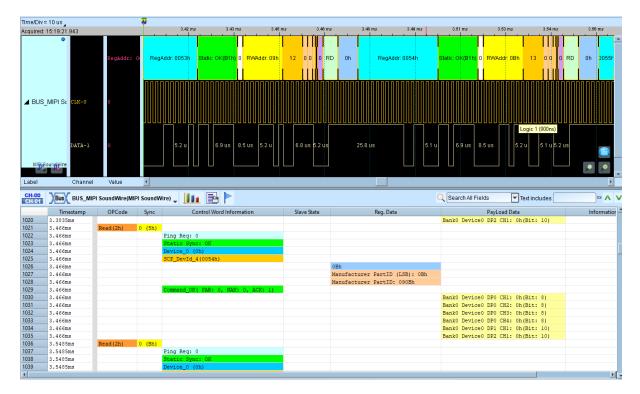
- 1. **HStart:** The start position of data in Frame Shape.
- 2. HStop: The stop position of data in Frame Shape.
- 3. Word Length: Data length of each channel in DPn.
- 4. Sample Interval: DPn sample interval.
- 5. Block Package Mode:
  - i. Block per port: Block Offset = Offset1 + (256 \* Offset2)
  - ii. Block per channel: Block Offset = Offset1 , Sub-Block Offset = Offset2.
  - iii. \*Block Offset range : 0 ~ 65535
  - iv. \*Sub-Block Offset range: 0 to 255
  - v. \*Offset1 range: 0~65535
  - vi. **\*Offset2 range:** 0~255
- 6. **Channel:** Divide a Data Port into different parts, commonly used in the left channel, right channel and so on for data distribution, user can choose up to 8 channels to use, and do not need to follow the order of selection.
- Port Flow Mode: it has four mode, Isochronous, Tx-Controlled, Rx-Controlled & Full-Asynchronous
  - \*Isochronous: 'Normal' mode, there is no valid data in each Payload
     Data Block.
  - ii. \*Tx-Controlled: 'Push' mode, whether the flow-control bit driven by the



Source Data Port transmits valid data in the Payload Data Block.

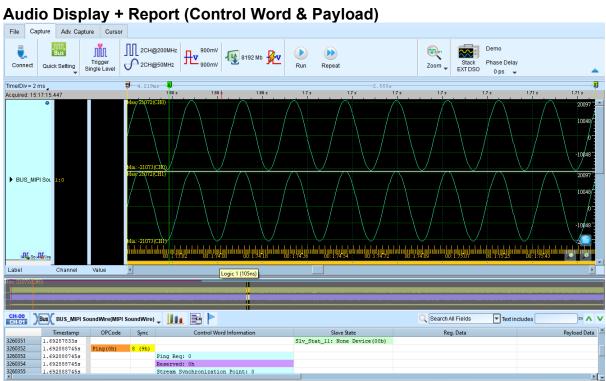
- iii. \*Rx-Controlled: 'Pull' mode, whether the flow-control bit driven by theSink Data Port transmits valid data in the Payload Data Block.
- iv. \*Full-Asynchronous: Whether the flow-control bit driven by the Sink and Source Data Port transmits valid data in the Payload Data Block.

#### **Result:**



#### Control Word + Report (Control Word & Payload):







# **MIPI SPMI**

MIPI SPMI(System Power Management Interface) designed by MIPI alliance. SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

# Settings

🗮 MIPI SPMI Settings						>
Channel		Color				
SCLK SDATA	A0 A1		Start C-bit	•	Address Byte Count / Data	<b>•</b>
Options			A-bit		No Response Frame	
Version	v2.0	-	SR-bit	•	Parity	•
Arbitration OFF			Arbitration	-	Bus Park / Handover	-
Report Options			SSC	•	ACK	•
	s into higher / lower addre	ISS	Command	•	Error	•
Range						
Decode Range						
From Buffer Head	To Buffer Tail	•				
Default					~	OK XCancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

### **Options:**

Version: Choose the version of MIPI SPMI. V2.0 and V1.0 are allowed to

be chosen.

Arbitration OFF: Means there is no arbitration on the bus. Enabled when checked.

Report Options: Split register address into higher and lower address in report.

Enabled when checked.



# Result

melDir= 500 ns		20.20 ma 20.28 ma 20.28 m	20.293ms a 28.29 ma	20.29 ma	20.29 ma	20.29 ma	20.29 ma 20.29 ma	20.29 ms	20.29 ma	20.29 ma	20.29 ms	20.29 ma	20.29 ma	20.29 mi
٥	IDLE			22-27 Mile 28 C 1472		SA-0	ERWE 06	59	P 01			24 - 21 ma	20-20 THU	
Bus 1 SCLK-	0													
3DAT-	L 0			280 % 560 :	x= 150 n	520 ns	210 ns 210 xs 260 ns		575 m					
MPI 25M	tel Value												ŀ	•
Bus Bus 1	MIPI SPMI) 🖵 😋	llu 🖻 🕨									Q Search All	Fields 🐨 Text Incl	ides	× /
Timestamp	Arbitration	Command	Addr. (h)	Reg. Addr. (h)	Byte Count		Data (h)		Error					
19.865305ms	MPL3	Extended Register Write Long	SA(0) 08	58 01	(1)	01								
20.292645ms	" MPL3	Extended Register Write Long	SA(0) 08			01								
37.580375ms	MPL3	Extended Register Read Long	SA(1) 53			80								
37.591835ms	MPL3	Extended Register Write Long	SA(1) 53		(1)	00								
37.71996ms	MPL3	Extended Register Write Long	SA(0) 08			01								
38.757605ma	MPL3	Extended Register Write Long	SA(0) 08			01								
39.276405ms	MPL3	Extended Register Write Long	SA(0) 08			01								
39.703745aa	MPL3	Extended Register Write Long	SA(0) 08			01								
40.131035ms	MPL3	Extended Register Write Long	SA(0) 08			01								
40.55832ms	MPL3	Extended Register Write Long	SA(0) 08			01								
41.13021ms	MPL3	Extended Register Write Long	SA(0) 08			01								
41.5655ms	MPL3	Extended Register Write Long	5A(0) 08			01								
41.99279ms	MPL3	Extended Register Write Long	SA(0) 08			01								
233.0620ms	MPL3	Extended Register Read Long	SA(0) 32			00								
233.88353ms	MPL3	Extended Register Write Long	5A(0) 32			50								
233.94384ms	MPL3	Extended Register Write Long	SA(0) 32			BC								
233.96051ms	HPL3	Extended Register Read Long	SA(0) 32			05 05								



# MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC)

version 5.1 is a flash memory card standard.

### Settings

Channel:

CM Da Da Da	LK B7 MD B23 ata0 B21 Da ata1 B22 Da ata2 B6 Da	DS     B16       ata4     B18       ata5     B19       ata6     B20       ata7     B4	Analysis  Command Data  Options  Adv. Report 3 Pin Mode No CLK Mode  Auto Phase Correction		Start Bit Host Device CMD Argument CRC Check	
	t Settings us Width 8-bit De 4-bit De 1-bit De	ata (Choose when	OT ACK the DUT is not powered on)		End Bit Data CRC Status Busy	
Bu	H\$200 -	Latch Method      SDR      DDR	Bus Width <ul> <li>8-bit Data</li> <li>4-bit Data</li> <li>1-bit Data</li> </ul>	Range	From Buffer Head Default	To Buffer Tail

Set the used LA Channels which are connected with DUT.

Analysis: (Combine with the feature – Customized Report) Command: Analysis Command only. Data: Analysis Data only. Command: Adv. feature Adv. Report: Advance report on CMD, DATA argument. 3Pin mode: Decode with CLK, CMD, D0 No CLK mode: Only use the CLK to decode When start to decode, set the DUT. status Startup mode: Need to set the DUT. Status. Including 1-8 bit data, DDR mode, Data Strobe and no BOOT ACK.



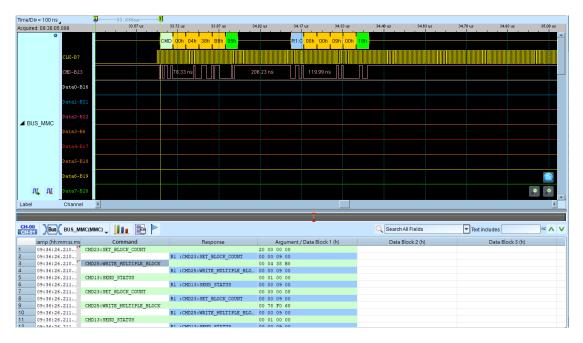
Auto	Phase	If it's checked, the decoder will auto adjust the phase of LA
		when

Correction:

measure the DUT..

### Result

#### Command:

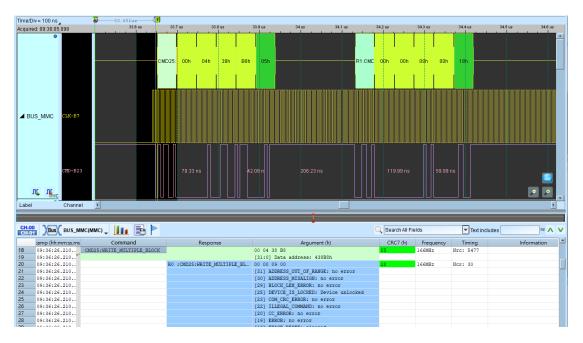


### Data:

uired: 09:36:05.098	36.87 us	36.89 us 36.91 us	30.93 us 30.95 us	: 36.97 us	36.99 us 37.01 u	ıs 37.03 us 37.05 us	37.07 (
¢							
· · · · · · · · · · · · · · · · · · ·	o oon ococococo	0(	CRC:OK		Stop	CRC Status:Non-Erro	Dr BUSY
	╧						
CLK-B7	15 ns						
CHD-B23							
Data0-B16			12.08 ns	8.75 ns	50.41 ns	11.66 ns	
Data1-B21							
Data2-B22							
US_MMC_2 Data3-B6							
Data4-B17							
Data4-B17							
Data5-B18		9.17 ns 1	4.58 ns 9.17 ns	8.75 ns 8.75 r	18		
Data6-B19		15 ns 15.4	11 ns 11.67 ns	15.41 ns 8.75 ns			
Data7-B20							
DS-B10							₽ ₽
JL JL DS-B10							
el Channel 💽				1	Q Search All Fields	Text includes	RE 🔨
I Channel J	(c)	Response	Argument / F	) Jata Block 1 (b)		Text includes	
l Channel 💽	IC) 🚽 🚺 💽 🕨	Response	Argument / C 34 81 00 00 DF 0	Data Block 1 (h)	Q Search All Fields Data Block 2 (h) 0 97 48 57 31 22 79 57	Text includes Data Block 3 AD 16 10 57 00 00 00	(h)
BUS BUS MMC_2(MMC_2(MMC_2)				3 00 00 A	Data Block 2 (h)	Data Block 3	(h) 50
BUS_BUS_BUS_MMC_2(MW tamp (hhrmm:ss.ms 09:36:26.210 <sup>25</sup> SC=1		D[0:31]	A4 81 00 00 DF 0	3 00 00 A	Data Block 2 (h) 10 97 4B 57 31 2E 79 57	Data Block 3 AD 16 10 57 00 00 00	(h) 00
Channel           Diagonalistic         Bus         BUS_MMC_2(MM           Image: Image (hhrmmss.ms)         09:36:26.210         SC=1           09:36:26.210         SC=1         09:36:26.210		D[0:31] D[32:63]	A4 81 00 00 DF 0 00 00 08 00 01 0	3 00 00 A 0 00 00 00 0 00 00 00	Data Block 2 (h) 10 97 4B 57 31 2E 79 57 1A F3 01 00 04 00 00 00	Data Block 3 AD 16 10 57 00 00 00 00 00 00 00 00 00 00	(h) 00 00 00
Channel Channel Bus_MMC_2(MMC lamp (hhrmmss.ms 09:36:26.210 SC-1 09:36:26.210 09:36:26.210		D[0:31] D[32:63] D[64:95]	A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 00 0	3 00 00 A 0 00 00 00 0 00 00 00 2 D9 9B 0	Data Block 2 (h) 10 97 4B 57 31 2E 79 57 1A F3 01 00 04 00 00 00 10 00 00 00 00 00 00 00	Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00	h) 00 00 00 00
It         Channel           Image: Channel         Image: Channel <td></td> <td>D[0:31] D[32:63] D[64:95] D[96:127]</td> <td>A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 00 0 00 00 00 00 A6 7</td> <td>3 00 00 2 0 00 00 00 00 0 00 00 00 00 2 D9 9B 00 F FE 91 00</td> <td>Data Block 2 (h) 10 97 4B 57 31 2E 79 57 12 F3 01 00 04 00 00 00 10 00 00 00 00 00 00 00 10 00 00 00 00 00 00 00</td> <td>AD         16         10         57         00&lt;</td> <td>(h) 00 00 00 00 00 38</td>		D[0:31] D[32:63] D[64:95] D[96:127]	A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 00 0 00 00 00 00 A6 7	3 00 00 2 0 00 00 00 00 0 00 00 00 00 2 D9 9B 00 F FE 91 00	Data Block 2 (h) 10 97 4B 57 31 2E 79 57 12 F3 01 00 04 00 00 00 10 00 00 00 00 00 00 00 10 00 00 00 00 00 00 00	AD         16         10         57         00<	(h) 00 00 00 00 00 38
Bus_mmc_2(m)           Bus_mmc_2(m)           Bus_mmc_2(m)           Bus_mmc_2(m)           09:36:26:210           09:36:26:210           09:36:26:210           09:36:26:210           09:36:26:210           09:36:26:210           09:36:26:210           09:36:26:210		D[0:31] D[32:63] D[64:95] D[96:127] D[128:159]	A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 00 0 00 00 00 00 A6 7 20 00 00 00 54 F	3 00 00 2 0 00 00 0 2 D9 9B 0 F FE 91 0 0 00 00 00 0	Data Block 2 (h)           0 97 4B 57 31 2E 79 57           10 0 00 00 00 00 00 00 00 00           10 00 00 00 00 00 00 00 00           10 00 00 00 00 00 00 00           10 00 00 00 00 00 00 00           10 00 00 00 00 00 00 00           10 00 00 00 00 00 00 00	Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00           00 00 00 00 00	(h) 00 00 00 00 38 00 00
Channel         Channel           iamo (thrmssmg)         09136126.210         SC=1           09136126.210         09136126.210         09136126.210           09136126.210         09136126.210         09136126.210           09136126.210         09136126.210         09136126.210		D[0:31] D[32:63] D[64:95] D[96:127] D[128:159] D[160:191] D[192:223]	A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 00 00 00 00 00 00 A6 7 20 00 00 00 54 F 00 00 00 00 00 00 54	3 00 00 2 2 00 00 2 2 00 00 00 00 00 00 0	Data Block 2 (h)           0.0         97         4B         57         31         2E         79         57           1A         F3         0.1         0.0         94         0.0	Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00	(h) 00 00 00 00 00 00 00 00 00
Channel         Channel           Image: Channel         Image: Channel         Image: Channel <td< td=""><td></td><td>D[0:31] D[32:63] D[64:95] D[96:127] D[128:159] D[140:191] D[192:223] D[22:225]</td><td>A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 0 00 00 00 00 A6 7 20 00 00 00 054 F 00 00 00 00 00 54 F 00 00 00 00 00 0</td><td>3         00         00         2           0         00         00         0         0           2         D9         D9         0         0           7         FE         91         0         0           0         00         00         0         0         0           0         00         00         0         0         0           0         00         00         0         0         0           0         00         00         0         0         0</td><td>Data Block 2 (h)           10         97         4B         57         31         2E         79         57           10         00         00         00         00         00         00         00           10         00</td><td>Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00</td><td>(h) 00 00 00 00 00 00 00 00 00 0</td></td<>		D[0:31] D[32:63] D[64:95] D[96:127] D[128:159] D[140:191] D[192:223] D[22:225]	A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 0 00 00 00 00 A6 7 20 00 00 00 054 F 00 00 00 00 00 54 F 00 00 00 00 00 0	3         00         00         2           0         00         00         0         0           2         D9         D9         0         0           7         FE         91         0         0           0         00         00         0         0         0           0         00         00         0         0         0           0         00         00         0         0         0           0         00         00         0         0         0	Data Block 2 (h)           10         97         4B         57         31         2E         79         57           10         00         00         00         00         00         00         00           10         00	Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00	(h) 00 00 00 00 00 00 00 00 00 0
Channel         Channel           Image: Channel         Image: Channel         Image: Channel <td< td=""><td></td><td>D[0:31] D[32:63] D[64:95] D[96:127] D[160:191] D[180:191] D[192:223] D[224:255] D[256:287]</td><td>A4         81         00         00         DF         0         00<!--</td--><td>3 00 00 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2</td><td>Data Block 2 (h)           10         97         4B         57         31         2E         79         57           10         07         4B         57         31         2E         79         57           10         07         4B         57         31         2E         79         57           10         00</td><td>Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00</td><td>h) 00 00 00 00 00 00 00 00 00 0</td></td></td<>		D[0:31] D[32:63] D[64:95] D[96:127] D[160:191] D[180:191] D[192:223] D[224:255] D[256:287]	A4         81         00         00         DF         0         00 </td <td>3 00 00 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2</td> <td>Data Block 2 (h)           10         97         4B         57         31         2E         79         57           10         07         4B         57         31         2E         79         57           10         07         4B         57         31         2E         79         57           10         00</td> <td>Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00</td> <td>h) 00 00 00 00 00 00 00 00 00 0</td>	3 00 00 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Data Block 2 (h)           10         97         4B         57         31         2E         79         57           10         07         4B         57         31         2E         79         57           10         07         4B         57         31         2E         79         57           10         00	Data Block 3           AD 16 10 57 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00	h) 00 00 00 00 00 00 00 00 00 0
el Channel Channel Car Bus Bus Bus Carlon 09:36:26.210. 00:36:26.210. 00:36:36.210. 00:36:36.210. 00:36:36.210. 00:36:36.210.		D[0:31] D[32:63] D[64:95] D[96:127] D[128:159] D[140:191] D[192:223] D[22:225]	A4 81 00 00 DF 0 00 00 08 00 01 0 00 00 00 00 00 00 00 00 00 00 00 00 A6 7 20 00 00 00 00 54 F 00 00 00 00 00 00 54 F 00 00 00 00 00 00 00 00 00 00 00 00 00	3         0.0         0.0         2           0         0.0         0.0         0           2         D.9         9B         0           0         0.0         0.0         0           2         D.9         9B         0           0         0.0         0.0         0           0         0.0         0.0         0           0         0.0         0.0         0           0         0.0         0.0         0           0         0.0         0.0         0           0         0.0         0.0         0           0         0.0         0.0         0	Data Block 2 (h)           0         97         4B         57         31         2E         79         57         31         2E         79         57         31         2E         79         57         31         2E         79         51         2E         79         57         31         2E         79         57         30         30         00         00<0	Data Block 3:           AD 16 10 57 00 00 00           G0 00 00 00 00 00 00 00           G0 00 00 00 00 00 00           G0 00 00 00 00 00 00           B0 74 85 76 67 312           G0 00 00 00 00 00 00 00           G0 00 00 00 00 00 00	30 00 00 38 38 00 00 00 00 00 00 00



### Adv. Report:



### No CLK mode





# Command + Data: (Customized Report)

Time/Div = 200 ns	2												
Acquired: 09:36:05.098		33.98 us	34.18 us	34.38 us	34.5	lus :	34.78 us	34.98 us	35.18 us 3	15.38 us	35.58 us	35.78 us	35.98 us
•													- <b>1</b>
BUS_MMC B23,87	0 38h B8l	h 05h	R1: <mark>OOh OO</mark> h	n 09h 00h <mark>18</mark> l	n								
ммс													
•							_				00		
CLK-B7													
CHD-B23	חוח	206.23 ns	] ∏]119.99	ns II II									
Data0-B16		U			J				י מרכות ר	1 141.	24 ns 129.15 ns	П	
Data1-B21								(35.295us)		180.4		m	
D							Logic	(35.295us)					
BUS_MMC_2 Data3-B6													
Data4-B17													
Data5-B18													
Data5-B10 Data6-B19											.10 ns 129.57 ns		
Data7-B20													
NL NH <sub>MC</sub> DS−B10													<u> </u>
Label Channel	4												•
		-					- 1						
CH-00 Bus Customize	d Report 🖕	111 📑 🏲							Q Search All Fields		Text include	s	
BUS_MMC Command		BUS_MMC Response		US_MMC ument (h)	S_MNBUS_MMG RC7 (IFrequency	BUS_MMC	JS_MMC omman	BUS_MMC_2 Response	BUS_MMC_2 Argument / Data Block 1 (h	h) [	BUS_MMC_2 Data Block 2 (h)		BUS_MMC -
3 CMD25:WRITE_MULT	IPLE			04 38 B8	05 166MHz	Nrc: 5477							
4	RO	:CMD25:WRITE_MULT	IPLE 00 0	00 09 00	18 166MHz	Ncr: 30							
5							SC=1	D[0:31]	A4 81 00 00 DF 03 00 00	A0 97 4	4B 57 31 2E 79 57	AD 16 10	57 00 00 00
6								D[32:63]	00 00 08 00 01 00 00 00	0A F3 (	01 00 04 00 00 00	00 00 00	00 00 00 00
7								D[64:95]	00 00 00 00 00 00 00 00		00 00 00 00 00 00		
8								D[96:127]	00 00 00 00 A6 72 D9 9E		00 00 00 00 00 00		00 00 00 00
9								D[128:159]	20 00 00 00 54 FF FE 91		00 00 00 00 00 00		57 68 73 12
10								D[160:191]	00 00 00 00 00 00 00 00				00 00 00 00
11								D[192:223]	00 00 00 00 00 00 00 00		00 00 00 00 00 00		00 00 00 00
12													
12								D[224:255]	00 00 00 00 00 00 00 00 00 A4 81 00 00 84 15 00 00		00 00 00 00 00 00 00 79 57 31 2E 79 57		00 00 00 00



# ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

### Settings

🚢 Modbus Setting	s	×
Settings		Waveform Area Settings
Channel		Decode Tx - Show Scale
Tx If the frame ga	A0         ♣         Rx         A1         ♣           p >         1000         ms, return to Tx state (When Tx = Rx)         ■	Color
Transmission Mo	ode	Tx/Rx -
O ASCII O	RTU	Address 🗸
Format		Function 🔹
Auto Detect	t	Data 💌
O Manual	Baud 9600 V Polarity Idle Low V Parity None V Data 8 V	Header  End
	Parity INdite Bits	Range
CRC Check		Decode Range
Adv. Report		From To Buffer Head
		Default OK Cancel

### Channel:

- **1. Tx:** Signal channel of Modbus Tx.
- 2. Rx: Signal channel of Modbus Rx.

Transmission Mode: It has ASCII and RTU mode.

### Format:



- 1. Auto Detect: Auto detect the value of all the options that can adjust by user if it was checked.
- 2. Manual: User can manually adjust the options below:
  - Baud Rate: Data rate (bits per second), and the range is 110 ~
     2M (bps).
  - II. Polarity:
    - Idle high: Idle condition shows High.
    - Idle Iow: Idle condition shows Low.
  - III. Parity: N-None Parity, O-Odd Parity, E-Even Parity.
  - **IV.** Data Bits: Set the data bits. User can set to 7, 8 or 9.

**CRC Check:** Do CRC check. Enabled when checked.

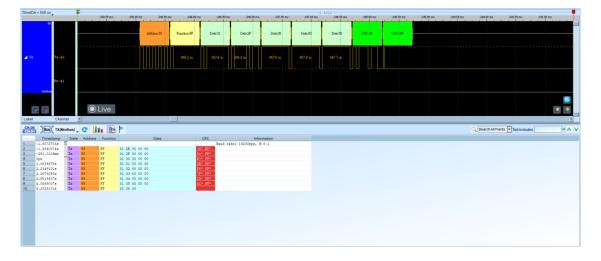
Adv. Report: Show the detail report in the report area. Enabled when checked.

**Big-Endian:** Data is arranged in Big-Endian style. Enabled when checked.

### Waveform Area Settings:

- Decode: Display the analyzed result of Tx or Rx in waveform area. Rx option only available when Rx is activated.
- 2. Show Scale: Display the waveforms with scales.

#### Result





# NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing.

NAND flash memory forms the core of the removable USB storage devices

known as USB flash drives, as well as most memory card formats and

solid-state drives available today.

# Settings

Channel				Device inform	ation
Device Width	● x8 ○ x16	#CE/RB		Vendors	Hynix 👻
<ul> <li>I/O Quick Set</li> <li>I/O User Defit</li> </ul>		● x1 ○ x2 ✓	○ x3 ○ x4 ✔	Model	HY27SF081G2A HY27SF161G2A HY27SF082G2B
1/00 (LSB)	CH 0 🗘	CE#1         CH 12         ↓           CE#2         CH 0         ↓	R/B#1         CH 13         ↓           R/B#2         CH 0         ↓		HY27SF162G2B HY27UF084G2M HY27UG088G5M HY27UG088GDM
CLE	CH 8	CE#3 CH 0 0	R/B#3 CH 0 0		HY27UH08AG5M
✓ ALE RE#	CH 9 🗘	CH 0	CH 0		
WE# DQS	CH 11 🗘	The Flash Startup mode	Mode	Color Color	mmand 🔹
Command Latch Cy		Data Out Cycles			dress 🗾 🔻
tDS >= 5.0ns	tDH >= 5.0ns	tREA >= 20.0ns	tDQSQ >= 0.5ns		ta In  ta Out
Save the NAND FI Don't show BUSY Erase Count Show/Hide Items		Invert RE#(W/Ra	¥) dress field of report	1 A	Decode Range From To
					Buffer Head 👻 Buffer Tail

# Channel:

Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel
RE	W/R	Read Enable and Write/Read channel
WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel



CE#	CE#	Chip Enable channel
	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

**The Flash Startup mode**: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O

Quick Setup, other channels will be set automatically. when check the I/O User

Defined and press the button will show the dialog below:

NAND Flash I/O								
		1100						
1/00	CH 0	1/08	CH 0					
I/01	CH 1 🌲	I/O9	CH 0					
1/02	CH 2 🌲	I/O10	CH 0					
I/O3	CH 3 🌲	I/O11	CH 0					
I/O4	CH 4 🌲	I/012	CH 0					
I/O5	CH 5 🌲	I/013	CH 0					
I/O6	CH 6	I/014	CH 14					
1/07	CH 7 🌲	I/015	CH 15					
	≪ок		Cancel					

User can set NAND I/O channel by channel.

**The Flash Startup mode:** Check Toggle /ONFI DDR Mode to run synchronous data interface.

**tREA / tDQSQ:** Set the delay time to access the NAND data under SDR / DDR.

To adjust the tREA/tDQSQ when the data out value of NAND Flash is invalid.

Save the NAND Flash Data: Save the read/write data. Program will save the

NAND Flash read/write data as a file when check Save the NAND Flash Data. It

will be saved into the LA work directory.



mode.

**Don't show BUSY State**: Show/hide the BUSY state information (e.g. BUSY START / BUSY END) in the report window.

**Erase Count**: Show/ hide NAND Erase command/address statistics.

Show/Hide Items: Show/hide the items in the report window.

**Invert RE# (W/R#) / Invert DQS:** check this item when connect the RE/DQS# pin under DDR mode.

**Not Filled the address field of report:** Filled the NAND write/Read address column in the report window or not.

Invert RE# (W/R#) / Invert DQS: Check this when connect the RE / DQS# under DDR mode.

**Don't care ALE/RB#/CE# signal:** Ignore the signal selected when decode.

Description of file name as following (Save the NAND Flash Data function):

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxh	Row Address
_Colxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF\_DI\_Row017821h\_Col0000h\_CE1\_1.bin

NF\_DO\_Row017821h\_Col0000h\_CE1\_2.bin

NF\_DO\_Row\_Col\_CE1\_3.bin

Compare the content of file with the one of report.



DO	Dl	D2	D3	D4	D5	D6	D7
5A	A6	6F	36	B2	38	B8	B7
06	8A	B7	0B	B1	19	C8	21
7E	CE	58	EF	BD	18	47	70
5E	DD	9A	E3	A5	E4	02	11
E9	2D	96	14	86	32	CE	F4
53	10	60	79	EA	B6	D6	CE
5A	22	53	A5	Fl	9E	DB	58
8A	73	B3	B1	82	19	B9	46
92	25	76	EA	E4	CE	74	A7
10	E5	20	3D	9F	74	BB	E5
55	54	68	4C	69	86	AC	OF

000000 5A A6 6F 36 B2 38 B8 B7 06 8A B7 0B B1 19 C8 21 000010 7E CE 58 EF BD 18 47 7C 5E DD 9A E3 A5 E4 02 11 000020 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE 000030 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 000040 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5 000050 55 54 68 4C 69 86 AC 0F F1 A2 47 FA 37 4B 04 0D

#### **Device information**

Vendors: Select the NAND Flash Vendor. Please refer to the

following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a AqNFCustom.txt file into the LA work directory

when select the **Custom** vendor item and edit NAND Flash Command set.

```
Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , Y, N, Y, 70
Cmd=Rwo-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10
```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description						
Manufacturer	NAND Flash Vendor.						
PartNo	NAND Flash IC Model.						
#CE/RB	Number of targets, only 1/2/4 acceptable.						
X16	8/16 bits device width, only Y/N acceptable.						
SyncMode	Only Y/N acceptable, Y: Synchronous data interface						



	supported; N: Not supported.				
	Cmd is composed of several parts, it's divided with comma.				
	1. Complete command name.				
	2. Abbreviation of command.				
	3. Name of first busy time check. Put a space and add a comma if unused.				
	4. Value of first busy time check. Its unit is micro seconds. Put a space and add a comma if unused.				
Cmd	5. Name of second busy time check. Put a space and add a comma if unused.				
	6. Value of second busy time check. Its unit is micro mseconds.				
	Put a space and add a comma if unused.				
	7. First flag. It's acceptable command during busy.				
	8. Second flag. It can be inserted by some command or not.				
	9. Third flag. It can insert into some multi plane command or not.				
	10. Command.				

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,

N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

Read Stat. / TPP Prog. : abbreviation of command.

Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is

5000 us. It will show some information when violation of busy time.

3 Flags: 1<sup>st</sup> flag of "Read Status" is Y means it's acceptable command

During busy; 2<sup>nd</sup> flag of "Two-Plane Page Program" and 3<sup>rd</sup> flag of "Read



Status" means any command between 11h and 81h is prohibited except

"Read Status (70h)".

Perform NAND Flash bus analysis, select Custom, the manufacturer name and model entered in the AqNFCustom.txt file will be displayed in the model; the analysis result will also be displayed according to the input command.

Vendors	Custom 👻	
Model	Toshiba-TH_UserDefined Samsung-K9XXXXXXXX Micron-3D NAND	<b>A</b>
	Edit	Refresh

NAND Bus Decode Timing Check function description

When using this function, please add the following description in the first

paragraph of the content of the custom file AqNFCustom.txt.

Manufacturer≓ PartNo=K9XXXX	
Spec=Toggle	ΔΔΔΔ
Version=2.0	
#CE/RB=1	
X16=N	
SyncMode=Y	
<u>TimingCheck=Y</u>	
StartupDDR=Y	
1	

1. Spec=Toggle



Only ONFI or Toggle can be filled in.

2. Version=2.0

ONFI fill in SDR/NV-DDR/NV-DDR2-3; Toggle fill in Legacy/1.0/2.0.

3. TimingCheck=Y

Only Y/N can be filled in, Y means the Timing Check function is enabled.

If you turn on the Timing Check function, please fill in the items that need Timing Check, the format:

### Item Name, Minimum Time, Maximum Time

The unit of time value is ns, and for the Timing Check item provided by the software, please fill in the item name specified in the appendix below according to the Spec/Version you set. These are the standard time check items listed in ONFI and Toggle NAND Flash. All other project names will be ignored.

If the time value check item of a certain item is not needed, please fill in X. If the two time values are both X, the item will also be ignored.

The time values listed in the appendix can be adjusted according to the actual NAND Flash specifications during use.

300, X TimingParam=tADL, TimingParam=tAR, 10, X TimingParam=tCALH, 5, X TimingParam=tCALS, 15, X TimingParam=tCAH, 5, X TimingParam=tCAS, 5, X TimingParam=tCAS, 5, X TimingParam=tCDQSH, 100, X TimingParam=tCH, 5, X TimingParam=tCLR, 10, X



The results will be displayed in the Information field of the report window, and

those that violate the set time range will be displayed in red font.

Normally, it will be displayed in black font.

The displayed information will include:

1. Time test item 2. Measurement time 3. Set time range.

### Appendix

ONFI								
	SDR		NV-DDR			NV-DDR2-3		
tADL	400	Х	tAC	3	25	tAR	10	х
tALH	20	Х	tADL	400	Х	tCAH	5	х
tALS	50	Х	tCADf	25	Х	tCAS	5	х
tAR	25	Х	tCADs	45	Х	tCALH	5	х
tCEA	x	100	tCAH	10	Х	tCALS	15	х
tCEH	20	Х	tCALH	10	Х	tCEH	20	х
tCH	20	Х	tCALS	10	Х	tCH	5	х
tCLH	20	Х	tCAS	10	Х	tCS	20	х
tCLR	20	Х	tCEH	20	Х	tCSD	10	х
tCLS	50	Х	tCH	10	Х	tCLR	10	х
tCOH	0	Х	tCK	50	Х	tCR	10	х
tCR	10	Х	tCKH(abs)	0.43	0.57	tDBS	5	х
tCS	10	Х	tCKL(abs)	0.43	0.57	tRHW	100	х
tDH	20	Х	tCKWR	0.43	Х	tWC	25	х
tDS	40	Х	tCS	35	Х	tWH	11	х
tITC	Х	1000	tDH	5	Х	tWHR	80	х



								Total Institutio
tRC	100	Х	tDQSCK	3	25	tITC	x	1000
tREH	30	Х	tDQSH	0.4	0.6	tRR	20	Х
tRHOH	0	Х	tDQSL	0.4	0.6	tWB	х	100
tRHW	Х	200	tDQSQ	х	5	tADL	400	Х
tRLOH	0	Х	tDSC	50	Х	tDQSH	0.43	Х
tRP	50	Х	tDSH	0.2	х	tDQSL	0.43	х
tRR	40	Х	tDSS	0.2	х	tWPRE	15	х
tWB	Х	100	tHP	0.43	Х	tWPST	6.5	Х
tWC	100	Х	tWPRE	1.5	Х	tWPSTH	15	Х
tWH	30	Х	tWPST	1.5	Х	tDH	0.3	Х
tWHR	120	Х	tWHR	80	Х	tDS	0.3	Х
tWP	50	Х	tFEAT	х	1000	tDSC	3.75	Х
tFEAT	Х	1000	tRST	х	500000	tAC	3	25
tRST	Х	500000				tDQSRE	3	25
						tQSH	0.37	Х
						tQSL	0.37	х
						tREH(abs)	0.43	х
						tRP(abs)	0.43	Х
						tWP	11	Х
						tRPRE	15	Х
						tRPST	4.875	х
						tRPSTH	15	Х
						tDQSRH	5	Х
						tRC	3.75	Х
						tCD	3.75	Х



			tFEAT	х	1000
			tRST	Х	500000

Note: Some Timing Check items will be multiplied by the average value of certain time items, including:

1. tDQSH/tDQSL: 0.45 x tDSC(avg)

- 2. tQSH/tQSL: 0.37 x tRC(avg)
- 3. tREH/tRP: 0.43 x tRC(avg)

If the above Timing calculation method is used, the following description must

be added to the front end of the file:

Manufacturer=Micron
PartNo=3D NAND
Spec=ONFI
Version=NV-DDR2-3
#CE/RB=1
X16=N
SyncMode=Y
<u>TimingCheck=Y</u>
UsedtRCavg=Y
UsedtDSCavg=Y

Then check the item input value at that time:

TimingParam=tQSH, 0.37, X TimingParam=tQSL, 0.37, X TimingParam=tREH(abs), 0.43, X TimingParam=tRP(abs), 0.43, X

If you do not use the above Timing calculation method, you only need to enter UsedtRCavg=N, UsedtDSCavg=N in the file header or remove this description completely, and the value entered for the time check item will be the minimum/maximum value of the time deal with.



				Toggle				
l	_egacy			1.0			2.0	
tCLS	10	х	tADL	300	Х	tADL	300	х
tCLS2	40	х	tAR	10	Х	tAR	10	х
tCLH	5	х	tCALH	5	Х	tCALH	5	х
tCS	15	х	tCALS	15	Х	tCALS	15	х
tCH	5	х	tCAH	5	Х	tCAH	5	х
tWP	10	х	tCAS	5	Х	tCAS	5	х
tALS	10	х	tCDQSH	100	Х	tCDQSH	100	х
tALH	5	х	tCH	5	Х	tCH	5	х
tDS	5	х	tCLR	10	Х	tCLR	10	х
tDH	5	х	tCOH	5	Х	tCOH	5	х
tWC	10	х	tCR	10	Х	tCR	10	х
tWH	10	х	tCRES	10	Х	tCRES	10	х
tADL	300	х	tCS	20	Х	tCS	20	х
tRR	10	х	tDH	0.9	Х	tDH	0.4	х
tRP	10	х	tDQSH	4	Х	tDQSH	2	х
tRC	20	х	tDQSL	4	Х	tDQSL	2	х
tCR	9	х	tDQSRE	х	25	tDQSRE	х	25
tCLR	10	х	tDSC	10	Х	tRC	5	х
tAR	10	х	tDS	0.9	Х	tREH	2	х
tRHOH	25	х	tRC	10	Х	tRP	2	х
tRLOH	5	х	tREH	4	Х	tRPP	30	х
tREH	7	х	tRP	4	Х	tRPRE	15	х
tWHR	30	Х	tRPP	30	Х	tRPST	27.5	Х



tWHC	30	Х	tRPRE	15	х	tRPSTH	25	х
tWHR1	180	Х	tRPST	27.5	х	tRR	5	х
tWHR2	300	Х	tRPSTH	25	х	tWB	x	100
tWB	Х	100	tRR	20	х	tWC	25	х
tFEAT	Х	1000	tWB	х	100	tWH	11	х
tRST	Х	100000	tWC	25	х	tWHR	120	х
			tWH	11	х	tWHR2	300	х
			tWHR	120	х	tWP	11	х
			tWHR2	300	х	tWPRE	15	х
			tWP	11	х	tWPST	6.5	х
			tWPRE	15	х	tWPSTH	25	х
			tWPST	6.5	х	tFEAT	х	1000
			tWPSTH	25	х	tRST	х	500000
			tFEAT	1000	Х			
			tRST	500000	Х			



### Result

Div=5us	2																
	2.6 mi	2.61 ma 2.61 ma	2.62 ma 2.62 ma	2.83 ma	2.03	l me	2.64 ma	2.84 ma		2.66 ma	2.65 ma	2.08 ma	2.66 ma	2.87 ma	2.87 e	2.68	ma
•	C0	00 <sup>°</sup> 00 <mark>54°2E 00</mark> °3E 34 5E 30°03 31°3E B	) 33 34 53 30 33 30 3E 30 33 32 33 EO 33 31 5E 3	10 13 31 3E ED	DC BD 33 30	) 3E 24 SE 30 3	2 21 3E EO 32 24 50	20 32 20 3E	ED 32 22 32	30 32 21 SE	30 32 21 3E ED 2E 18 3	1 20 XC 30 32 20 3E 3	4 SE 30 13 31 3E	30 33 34 53 BD 33 30	) 3E 80 33 32 33 80	33 31 3E 30 FF 2F 4	10 23 03 31 XE BO
1/00-4	17		2.16 w	2.88	us 🔲	4.33 to:	i i i i i i	10.8 m		21	6 to 2.89 to 7	6.48 w			16 m 🗌 🔲	أشافات	2.16 us
1/01-4	18				(6 m	hnr			216 ==			36 m 🗋 🗍			2.16 m		4.4
1/02-4		215 112 16 116	2,88 m 5,04 m 22	16 m	216 **	215 m 216		.68 w 🗖	5.04 =		2.16 - 2.16	m 216m 216	216 m		5.04 w		2.88 m
1/03-4			504 m2 504 m 2						5.04 a						5.04 m		
		└ └ └ └''뿌 └															20000
1/04-3		2.4 w 2.16 w 2.16	m 2.16 m 2.16 m 2.16 m 2.16					2 ws				5.04 =	2.16 m 2.1	0 W [2.10 W	2.16 m 2.16 v		
1/05-4		1.68 u 2.16 u		ЧЦ		2.16 w	2.16	•• 🗆 🛯	$\Box$ $\Box$	2.16 1	≝∐ ∐_ ∟		.16	2.16 to		5.04 to	
E 1/06-4	110 3.3 m 1.54 m 2	1.65 us 3.12 us 2.16 us	1.44 u2.16 u 2.16 u	2.16 m		<b>1</b> .44 u 2	16 w	2.16 m	2.16 w	1.44	102.16 us 2.16 us		1.44 u 2.16 uz	216	u: 2.16 u	2.16 w	2.16 m
1/07-4	14 2.74 to:	3.85 - 216	nt 2.15 us 2.16 us	1.44 0	2.88 m		2.16 us	2.1	5 w	2.16 ==	1.44 u 2.16 us	2.88 m	21	6 tes	2.16 m	2.16 📼 🦳 🚺	
CLE-AG																	
ALE-AL		3.84 m															
RE#-A3				UUUUL	JUUUL	וחחחה		JULUL	UUUL	IUUUL			UUUUUU	սսսսսս	JUUUUUL	UUUUUUU	UUUUL
CE#1-4																	
R/8#1-																	
NAND Flash R/B#1-	-84																
Revel Pass																	
Ford Plass	O Live																
	OLive																
Chann	O Live															_	
Chann	OLive												Q	arch All Fields	Text	includes	
Channe Channe Bus CLE(N Timestamp	O Live	Row Address(h)	Column / Feature Address(h)	D0	D1	D2	D3 D4	DS	D6	D7	ASCE(DO-D7)		•		Text	includes	
Chann Chann Bus CLEIN Timestamp 2.590525ms	AND Flash) C		Column / Feature Address(h)		D1	02	D3 D4	DS	D6	D7	ASCI(D0-D7)	BUSY END (R/B	•			includes	•
Chann Chann Mus CLE(N. Timestamp 2.59525tas 2.60515tas	AND Flash) Command		Column / Feature Address(h)	D0	D1	D2	D3 D4	DS	D6	D7	ASCI(00-07)	DO	•			includes	0
Chann Chann Chann CLE(N. CLE(N	AND Flash) C	Row Address(h)		co								00 00	•			includes	
Chann Chann 2.590525ms 2.606315ms 2.602395ms 2.602395ms 2.6022ms	AND Flash) Command		Column / Feature Address(h)	C0 8E	34		D3 D4	31	82	EO	.4nl	00 00 DI	•			includes	
Chann Chann 2.5952588 2.606315ms 2.606295ms 2.61022ms 2.61021ms	AND Flash) Command	Row Address(h)		co	34 34		20 03	31 30		EO		DO DO DI DI	•			includes	
Chann Chann 2.590525ms 2.606315ms 2.60239ms 2.61022ms	AND Flash) Command	Row Address(h)		C0 8E 83	34	6E 8 63 8 83 1	20 03 20 83	31	8E 38	EO	.4n1 .4c0	00 00 DI	•			includes	•
Chann	AND Flash) Command	Row Address(h)		C0 8E 83 83	34 34 32	6E 8 63 1 83 1 8E 8	E0 03 E0 83 E0 03	31 30 31	33 38 32	E0 E0 E0	.4n1 .4c0 .21n.	DO DO DI DI DI	•			includes	
Chann	AND Flash) Command	Row Address(h)		C0 8E 83 83 03 85 82	34 34 32 31 24 24	6E 1 63 1 83 1 8E 8 6E 1 62 1	20 03 20 83 20 02 20 02 20 02 20 82	31 30 31 E0 21 20	82 82 83 82 83	E0 E0 E0 E0 E0 E0 E0 E0	.4c0 .21n. .1 .6n! .6b	DO DI DI DI DI DI DI DI	•			includes	
Chann Chann	AND Flash) Command	Row Address(h)		C0 8E 83 83 03 85 82 82	34 34 32 31 24 24 22	6E 8 63 8 8E 8 6E 8 62 8	20 03 20 03 20 02 20 02 20 02 20 02 20 02	31 30 31 E0 21 20 21	82 82 83 83 82 82 82 82 82 82	E0 E0 E0 E0 E0 E0 E0 E0 E0	.4nl .4c0 .2ln. .l .¢n!. .¢b .*in.	DO DI DI DI DI DI DI DI DI DI	•			includes	
Chann Chann Chann 2.590525as 2.604515as 2.604515as 2.604235as 2.604235as 2.604235as 2.604235as 2.604235as 2.604235as 2.6345as 2.6345as 2.6345as 2.6345as	AND Flash) Command	Row Address(h)		C0 8E 83 83 03 85 82 82 82 02	34 34 32 31 24 24 22 21	6E 8 63 8 82 8 62 8 82 8 82 8 82 8 82 8	20 03 20 83 20 02 20 02 20 82 20 02 20 22 20 22	31 30 31 E0 21 20 21 18	82 82 83 82 83 82 82 82 82 82 82 82 82 82 82 82 82 82	E0 E0 E0 E0 E0 E0 E0 E0 E0	.4n1 .4c0 .21n. .1 .4n!. .4b 	DO DI DI DI DI DI DI DI DI DI	•			includes	•
Chann Chann Timestarpy 2.590525ms 2.000315m 2.002395ms	AND Flash) Command	Row Address(h)		C0 8E 83 83 03 82 82 82 02 02 0C	34 34 32 31 24 24 22 21 E0	6E 8 63 8 83 8 6E 8 62 8 82 8 82 8 82 8	20 03 20 03 20 0C 20 02 20 02 20 02 20 02 20 02 20 22 20 22 20 22	31 30 31 20 21 20 21 18 34	82 82 83 82 82 82 82 82 82 82 82 82 82 82 82 82	E0 E0 E0 E0 E0 E0 E0 E0 E0 E0 E0	.4m1 .4c0 .2n. .1 .4m1. .4m1. .4m1. .4m1. .4m1.	DO DI DI DI DI DI DI DI DI DI DI	•			includes	•
Chann Chann Chann Call Color C	AND Flash) Command	Row Address(h)		C0 8E 83 83 03 8E 82 82 82 02 02 02 02 02 02 02 02 03	34 34 32 31 24 24 22 21 E0 31	6E 1 63 1 8E 1 62 1 82 1 82 1 82 1 82 1 82 1 82 1 82 1 8	20 03 20 63 20 07 20 02 20 82 20 22 20 22 20 22 20 22 20 22 20 22 20 22 20 22 20 22 20 23	31 30 31 20 21 20 21 18 34 34	82 82 83 82 82 82 62 91 62 63	E0 E0 E0 E0 E0 E0 E0 E0 E0 E0 E0 E0 E0	.4n1 .4c0 .21n. .1 .4b  .4b       	DO DO DI DI DI DI DI DI DI DI DI DI	•			includes	
Chann Chann Chann Clevel Cleve	AND Flash) Command	Row Address(h)		C0 8E 83 83 83 82 82 82 82 82 82 82 82 82 82 82 82 82	34 34 32 31 24 24 22 21 20 31 30	6E 8 63 8 8E 8 62 8 82 8 82 8 82 8 82 8 82 8 82 8 82	20 03 20 03 20 03 20 02 20 02 20 02 20 02 20 22 20 22 20 22 20 22 20 23 20 83 20 83	31 30 31 20 21 20 21 18 34 34 32	02 02 62 63 02 62 01 62 63 03	E0 E0 E0 E0 E0 E0 E0 E0 E0 E0 E0 E0	.4n1 .4c0 .21n. .1 .4n1 .4b    	DO DO DI DI DI DI DI DI DI DI DI DI DI DI	•			incluées	•
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### Timing Check

	Timestamp (hh:mm:ss.ms.us.ns)	Command	Row Address(h)	Column / Feature Address(h)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
29	09:25:05.440.234.699													tWC(152.08 ns):Min(25 ns)
0	09:25:05.440.234.851													tWC(152.50 ns):Min(25 ns)
1	09:25:05.440.235.085													tAR(182.50 ns):Min(10 ns)
2	09:25:05.440.235.085													tWHR(234.17 ns):Min(80 ns)
3	09:25:05.440.235.186													tRPRE(100.83 ns):Min(15 ns)
4	09:25:05.440.235.186													tRP(abs)(100.83 ns):Min(0.43 ns)
5	09:25:05.440.235.189													tRC(103.75 ns):Min(3.75 ns)
6	09:25:05.440.235.189													tWHR(337.92 ns):Min(80 ns)
7	09:25:05.440.235.192													tWPRE(97.08 ns):Min(15 ns)
8	09:25:05.440.235.192													tDQSRE(3.33 ns):Min(8 ns)/Max(25 ns)
9	09:25:05.440.235.192													tQSL(97.08 ns):Min(0.37 ns)



# NEC IR

NEC IR (NEC Infrared) is a company that specializes in infrared technology and solutions, often referred to as NEC (Nippon Electric Company) products or services in the field of infrared technology.

### Settings

Kec Settings	×
Channel	Color
NEC Channel A0	Leader  Address
Option	/Address 🗨
Extended Mode	Command
<ul> <li>Display without idle in report</li> </ul>	/Command 🗨
Swap Bits	Repeat 👻
Ignore glitch	Stop 🗸
Range Decode Range From To Buffer Head To Buffer Tail	
	ODefault ✓OK ¥Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

**Options:** Enabled when checked.

1. Extended Mode: It integrates /Address and Address into 16 Bits Address,

/Command and Command into 16 Bits Command.

2. Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.



- 3. Swap Bits: Switch LSB First to MSB First.
- 4. **Ignore glitch:** Ignore glitch while analysis. Enabled when checked.

# 



# OA3p(PMD)

OA3p (OPEN Alliance 3-pin) is an important protocol in automotive Ethernet testing that defines the requirements for Physical Layer (PHY) testing in automotive environments to ensure the consistency, reliability and stability of the equipment under different operating conditions.

#### Settings

🚐 OA3p (PMD) Settings	>
Channel	Ethernet Settings (10BaseT1S)
TX A0 RX(MDC) A1 ED(MDO) A2 C	Show Sync Code       Show Single BEACON       FCS in Byte Order         Display 5B Code       Show MAC fo Each Row         ✓       Show MAC Data         Transport Layer Data       ▼
OA3p Settings	
Display Mode: TX Data + Config 💌	Data Filter:
Show RX Data in NORMAL State	Report Data:
	MDIO Settings (Config State)
Range	Enable Preamble Counter
Decode Range	32 bits
From To Buffer Head V Buffer Tail V	Data
Buffer Head	Data Edge:
	Default VOK XCancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

### OA3p settings:

- Display Mode: Display TX Data / RX Data + Config result in waveform area.
- 2. Show Rx Data in NORMAL State: Show RX analyzed result even the

Bus goes into Normal State. Enabled when checked.



Ethernet Settings (10BaseT1S): Set the parsing result of Ethernet in report

area. Enabled when checked.

- 1. Show Sync Code
- 2. Show 5B Code
- Show MAC Data: Enabling this option allows user to additionally set whether the Transport Layer Data or the Transport Layer Data & Header is displayed.
- 4. Show Single BEACON
- 5. Show MAC of Each Row
- 6. FCS in Byte Order
- 7. Data Filter: Displays only the data of the set number of bytes.
- 8. **Report Data:** Set the number of bytes displayed in the data field in report area, and the excess bytes are displayed in a new line.

### MDIO Settings (Config State):

 Enable Preamble Counter: Set the number of preamble bit. Enabled when checked.

Data Edge: Latch data at the rising or falling edge.

Rime/Div= 5 us			1.38 #	1.38 a	1	.38 z	1.08 a	1.38	0 x 1.30	. 1.3	.36 s	1.08	7n.s 1.38 s	1.38 a	13	6 2	13	81	1.38 a		1.38 #	1.38 s		.38 s
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			minim		mble SF	Dest Addr.	Szc. Add		00 00 00 93 97 98						4 85 86 87	68 89 32	A BE BC BU	E EP CO C1	2.3040	53073839	CLECTE.	ECF000100	203 04 05 06	57 DB D9 58 3E 30
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OA3p_TX																								
	PX-1																							
QA3erPM	₩D-2																							
		$\bigcirc$	Live																					
Label	Channel	•																						
		(OA3p(PMD))	C III											-	-		_			QSe	arch All Field	Is 💌 Text inc	ludes	≈ ∧
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CH-00 Bus Jamp (H 1 08:54:	CA3p_TX(					TX	Ethernet Dat	a	RX In MAC Destinati			3D-11-FE-72		Informe	ition		_			QSe	earch All Field	Is 💌 Text inc	Audes	
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CH-00 Bus CH-01 O8:54: 2 00:54: 3 08:54: 4 08:54:	CA3p_TX( http://www.same 157.850N 157.850N 157.850N 157.850N	State SORMAL Start SORMAL SORMAL SORMAL				TX	Ethernet Dat	18	MAC Destinati MAC Source Ad EtherType/Len	n Address Iress	FC-C2- 00FE	3D-11-FE-72 3D-11-FE-71		Informe	ition					QSe	earch All Field	IS 💌 Text inc	dudes	cx 🔨
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CHOOL         Death           amp (h)         00:54-50           3         01:54-50           4         00:54-50           5         01:54-50           6         01:54-50           8         01:54-50           9         01:54-50           10         00:54-51           10         00:54-51           10         00:54-51           10         00:54-51           10         00:54-51           10         00:54-51           10         00:54-51           10         00:54-51           10         00:54-51           11         00:54-51           12         00:54-51           13         00:54-51           15         00:54-51           16         00:54-51           17         00:54-51           18         00:54-51	CA3p_TX( bhrmmsami 157.550. "N 157.550. N 157.550. N	State SCRPAL Start SCRPAL Start SCRPAL Start SCRPAL SCRPAL SCRPAL SCRPAL SCRPAL SCRPAL SCRPAL SCRPAL SCRPAL SCRPAL				TX	Ethernet Dat	ia	MAC Destinati MAC Source Ad EtherType/Len DATA DATA DATA DATA DATA DATA DATA DAT	n Address Iress	FC-C2- 00FE 300 00 9B SC A3 A4 AB AC B3 B4 B3 B4 C3 C4 C8 CC C3 C4 C8 CC D3 D4 D5 DC E3 E4 E5 EC F3 F4 FB FC	3D-11-FE-72 3D-11-FE-71 4D 95 95 97 84 5D 95 87 98 5D 95 87 97 5D 97 97 97 97 97 97 97 87 97 97 97 97 97 97 97 97 97 97 97 97	99 58 Al 22 Al 24 Al 24 Bl 82 B9 82 Cl 05 68 Cl 05 68 Dl 82 Cl 05 68 Dl 82 Dl 82 E9 82 Fl 82 Fl 82 Fl 82 Fl 9 60 Cl 02	Informe	tion					Q. 84	earch All Field	is 💌 Text Inc	kudes	A 10
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# OATC6 over SPI

OPEN Alliance Technical Committee 6 (TC6) focuses on improving the media-independent communication interface (xMII) to enhance its use in automotive networks.TC6 develops recommendations for automotive xMII standards and defines related improvements.

🔤 OATC6 over SPI Setting	gs			×
Channel		Startup Settings		
		Protected Mode		
CLK	A0	Enable Timestamp	64-bit (Default) 👻	
CS SDI SDO	A1       A2       A3	Block Payload Size:	64-Byte (Default) 👻	
Report Settings		Ethernet Settings		
Show Ctrl Detail Waveform Display:	SDI 👻	FCS Byte Order		
Range		Data Filter: 20 byte	s 🌲	
Decode Range		Report Data:	3 Byte 👻	
From Buffer Head 👻	To Buffer Tail 🔹	✓ Show Ethernet Packet	ŧ	
		ODefault 🔶	OK XCancel	

#### Settings

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

### **Report Settings:**

1. Show Ctrl Detail: Show the Ctrl detail information in report area.

Enabled when checked.



2. Waveform Display: Display the SDI or SDO result in waveform area.

### Startup Settings, enabled when checked:

- 1. **Protected Mode:** Enable or disable the protected format int the control frame.
- 2. Enable Timestamp: Set the output timestamp format. User can choose 64 bit (default value) or 32 bit format.
- Block Payload Size: Assign the Block Payload Size. User can choose
   64 bit (default value) or 32 bit format.
- **4. Transmit FCS Validation Enable:** Enable Frame Check Sequence (FCS) validation during transmission to ensure data integrity.

### Ethernet Settings:

- 1. FCS Byte Order: Present the FCS in Byte order in the report.
- Data Filter: Only how many bytes of data are displayed (at least 20 bytes).
- 3. **Report Data:** Limits the maximum number of bytes of data that can be displayed in the Data field; the portion that exceeds the setting continues to be displayed on a new line.
- Show Ethernet Packet: Displays Ethernet data such as Address, Data, and FCS.



	0.17 s 0.17 s 0.17 s	0.17 s 0.17 s 0.17 s	9.140s 9.17 s 9.17 s 9.17 s	0.17 s 0.17 s	0.17 s 0.1	7 s 0.17 s	9.17 5 0.17 5	
uired: 11:55:49.761		17F-F9F-100-80 0						
		PF-IF-00-60 0	Dunany Distanty					
CLK-2								
OATC6_SDO(: 05=1		109.58						
SDI-4		3.27 0	9.61 m 36.24 m					
CATCS over SPI			48 w 3.6 w	7.47 w				
•		FF-FF 00-60 D	FF-FF 00-60 0	· · · · · · · · · · · · · · · · · · ·				
C1K-2								
DATC6_SDO 05-1								
3DI-4		3 27 v 10 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	9.61 m 36.24 m					
500-3			.48 us	7.47 10				
OATC8 over SPI					20.17 6			
R. R.	O Live							
el Channel I								
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# PCM

The format that describes sound as a series of numbers is often referred to as a raw audio file, and the term for it is PCM (Pulse-code modulation). Examples of this format include WAV files on Microsoft Windows (sound files recorded using the "Sound Recorder" software) and AIFF files on Apple platforms. These files belong to this format, typically with a header added at the beginning.

#### Settings

🚔 PCM Settings	×
Channel	Color
Clock(SCK) A0 Chip Select(CS) A1 Chip Select(CS) A2 Chip Select(SD) A2	User can assign color for specific pattern. CH1 CH5 CH5 CH2 CH6 CH3 CH7 CH7 CH7 CH7 CH7 CH7 CH4 CH8 CH8 CH8 CH8 CH4
Audio Settings	Range
Data bits:16 bit(s)ModePCM A ModeChannel Count2Latch EdgeFallingEnable PulseHighEnable full scaleLSB First	From To Buffer Head Buffer Tail Sound Reduction Display the audio waveform Save as WAV file Align common sampling rate Playback All 5 Sec 3 Sec
	ODefault VOK XCancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

### Audio Settings:



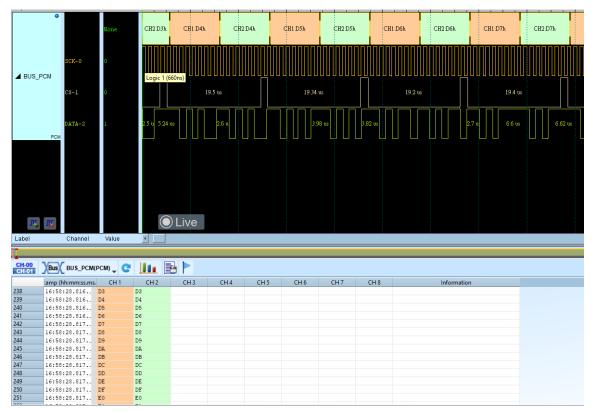
- 1. Data bits: Set the PCM Data bit amount.
- Mode: PCM mode settings. User can set to PCM A Mode, PCM B Mode, PCM Multi Mode.
- 3. Channel Count: PCM Channel Number Adjustment
- 4. Latch Edge: Latch data at the clock rising or falling edge.
- 5. Enable Pulse: CS operation settings, can be set to High or Low.
- 6. Enable full scale: Full scale function. Enabled when checked.
- 7. LSB First: Data is arranged in LSB first. Enabled when checked.

**Sound Reduction:** Display, playback or save the sound waveform. Enabled

when checked.

Result

Packet





### Audio

Time/Div = 2 ms	👃 🔋 CJ 🖡	<b>J I</b>							
Acquired: 16:58:28.812	0 ps		4 ms	6ms 8	rms 10	ms 12 r	ns 14m	s 16 m s	18 ms
*	Mex 255 (CH1)								
	Min: 1 (CH1) Mex: 255 (CH2)								
▶ BUS_PCM 2:0 None									
	Min: I'(CH2)								
PCM	CH2: E		00:00.53	nhenharinginginginahanna 00:00.71	dentustantin (kartantin dan kar 00:00.89	401001004000000000000000000 00:01.07 00:01.07	01.25 01.25 01.25	udan dan kan kan kan kan kan kan kan kan kan k	lanlarin (n. 1991) 00:01:79
		_ive							



# PDM

PDM (Pulse Density Modulation) is a digital signal modulation technique

primarily applied in the digitization and transmission of audio signals.

### Settings

🔤 PDM Settings		×
Parameter Settings	Color L.Channel R.Channel	
<ul> <li>Mono Latch on Risi</li> <li>Stereo LCH: Rising</li> <li>Show bit stream only</li> <li>Audio Information</li> <li>Decimation Parameted</li> <li>Audio Frequence:</li> </ul>	RCH: Falling	
Sound reduction	Range	
○ All ○ 5 sec	play audio waveform ull Scale riginal From Buffer Head Buffer Tail	
Default	✓OK XCancel	5

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

### Detail:

1. Mono & Stereo: Audio mono or stereo selection.



- 2. PDM Sample Rate: PDM Clock Speed
- 3. Decimation Parameter: Calculation parameter for PDM to PCM
- 4. **Audio Frequency:** PCM audio frequency

#### Sound reduction:

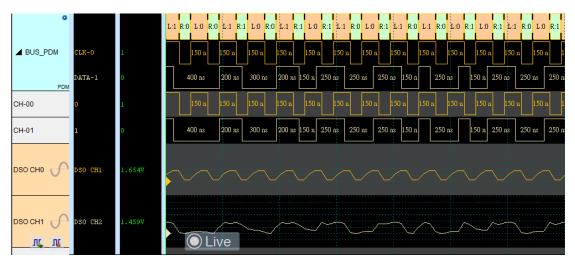
- 1. **Playback:** Set the playback time duration.
- 2. Display audio waveform: Use Full Scale or Original to draw sound waveform in waveform area.

Save as WAV file: Saves the restored sound waveform as a .wav. Enabled

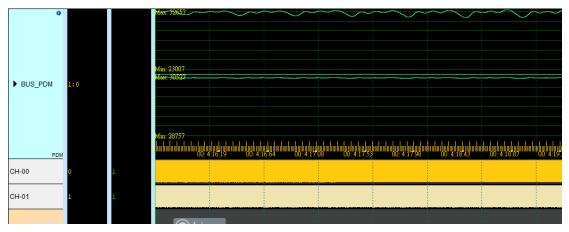
when checked.

#### Result

#### Normal mode



### Audio mode





# PECI

Platform Environment Control Interface, Platform management include thermal,

power and electrical error monitoring.

### Settings

🛤 PECI Settings		×
Parameter		
2		
Channel	Report Mode	
Data 🗛 🌲	Normal      Advance	
Do not detect SYN	IC frame	
Do not compare S	YNC packets	
Color		
Sync		•
Address		•
WL/RL		•
FCS		•
Data		•
Range		
Decode Range	e	
From	То	
Buffer Head	▼ Buffer Tail	•
Defaul	It ✔OK ¥Can	cel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Report Mode: User can choose between Normal and Advanced modes, and

the Advanced mode displays more detailed information.



Do not detect SYNC frame: Do not detect SYNC frame. Enabled when

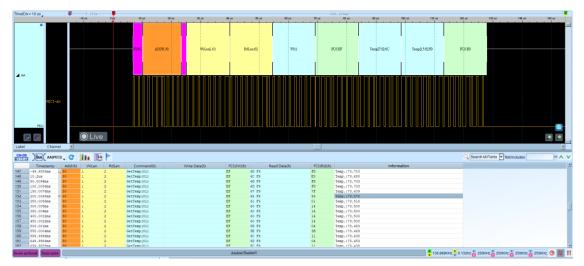
checked.

Do not compare SYNC packets: Do not compare SYNC packets. Enabled

when checked.

#### Result

#### Normal mode



#### Advance mode

/Div=10 us	7.373					230.203ms					
	-10 us 0	s 10 us 20 us	30 us 40 u	s 60 us	60 ur	70 us 80 us	90 us	100 us 110 us	120 us 13	0 us 140 us	150 us
e											
		SYNC ADDR:30	WrLend 01	RdLen 02	701)	FC2:EF	Temp[7:0]:6C	Temp[15:8];P9	FCS-E8		
		STRC ADDR:N	WILKIE UI	KALMANUZ	101)	PLOEP	temp[7:0]:00	temb[12:0]154	PQ-20		
						1 1					
							n mmi mmn n	ciencien à r			
PECI-A	٥										
PEO											
PK	O Live										
Channe											_
Channe										-	
	n, C 🛄 🖹 🏲								C Search All Fie	ilds 💌 Text includes	•
Timestamp -7.3498578#	Field <sup>47</sup> Client Address	Data(h)	Status	Data rate:547.98		Information					
-7.34903708	Write Length			Data reteros/.90	A1						
-7.3498268s	Read Length	01 02									
-7.349812#	Cmd Code	GetTemp(01)									
-7.34979748	FCS	EF									
-7.3497828s -7.349768s	Temp[7:0] Temp[15:0]	75 F9		Temperature:73.8							
-7.3497688	Temp(1510) FCS	02		resperature173.8	28						
-7,2998588#	Client Address	30									
-7.2998424#	Write Length										
-7.2998276s	Read Length	01 02									
-7.2990138	Cad Code	GetTemp(01)									
-7.2997984a	FCS	EF									
		75									
-7.2997836#	Temp[7:0]	10									
-7.2997836s -7.299769s -7.299769s	Temp[15:0] FCS	79		Temperature:73.0	20						



## **PMBus**

The Power Management Bus ("PMBus") is an open standard protocol that defines a means of communicating with power conversion and other devices.

PMBus Settings			×
Settings	Color		
Channel		Start	<b>•</b>
Clock Channel (SCL)		Repeat Start	
Data Channel (SDA) A1		Address	-
Options		Command	
		Data Write	<b></b>
8-bit Addressing (Include R/W in Address)		Data Read	•
▼ PEC decode		PEC	
Clock Stretching		Stop	-
Timeout Check us	Range		
✓ Ignore Glitch	- <u>FA</u>	From	То
Filter pulse with < 1 sample points		Buffer Head 🔹	Buffer Tail
		Default	OK Cancel

### Channel:

- **1. Clock Channel (SCK):** Transfer clock of PMBus.
- 2. Data Channel (SDA): Transfer data of PMBus.

### **Options:**

1.8-bit addressing (Including R/W in Address): Displays an 8-bit width

address (7-bit width address plus 1-bit Rd/Wr).

2. PEC decode: Set whether the analyzed data contains PEC.

**Clock Stretching:** Set the time of Clock Stretching. Enabled when checked.

Ignore Glitch: Ignore noise caused by slow transitions when analyzing.



Enabled when checked.





# ProfiBus

ProfiBus (PROcess Field Bus) was developed in 1987 by Siemens and other 14 companies and 5 research institutes in Germany, and is widely used in industrial control automation, transportation and power automation, etc. ProfiBus consists of 3 parts, PROFIBUS FMS (Fieldbus Message Specification), PROFIBUS DP (Decentralized Peripherals), and PROFIBUS PA (Process Automation). Currently, PROFIBUS DP and PROFIBUS PA are the most commonly used.

#### Settings

🛤 ProfiBus Settings	×
Channel	Color
Configuration Channel Channel CH 0	User can assign color for specific pattern. LE / LRr SD SA DA A
Option	DSAP FC FC
✓ Auto Detect	DU V SSAP V
	ED 🔽 FCS 🔽 🗸
9600 - bps Start bit: Low -	START STOP PARITY
	Range
	Decode Range
MSB first	From To
Show scale in the waveform	Buffer Head 🔹 Buffer Tail 👻
	ODefault ✔OK ★Cancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal



end is connected on the object to be tested.

Baud Rate/Auto Detect: Set the baud rate manually or auto detect

Start bit: Set the Start bit to be High or Low.

**MSB First:** The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section





# PS/2

PS/2 is a bi-directional synchronous serial protocol for communication between a keyboard or mouse and a PC, developed by IBM, it consists of six pins, namely Clock, Data, +5v, Ground and two blank pins. PS/2 uses a bi-directional synchronous transmission method, whereby data is exchanged between the two ends of the communication via Clock and Data.

👼 PS/2 Settings	×
Channel Clock CH 0	Device <ul> <li>Keyboard</li> <li>Mouse</li> <li>Other (Only Display Raw Data)</li> <li>Startup Setting</li> </ul>
Export Matlab File Color Host Device	Scan Code Set 2 Mouse Type Scroll Wheel Mouse
Range Decode Range From To 緩衝區開頭 • 緩衝區結尾 •	✓OK XCancel

### Settings

Channel: Show the selected channels.

**Export MATLAB file:** Export the data with MATLAB format as the following:



Time = [25.78484 25.785985 ... ]

Description = [DH DH ... ] DH = Device to Host, HD = Host to Device

Data = [ 58 FA 02 FA C4 ... ]

The file (PS2\_Matlab.m) will be saved at work directory

### Device:

Keyboard: Assign the current device is PS/2 keyboard.

Mouse: Assign the current device is PS/2 mouse.

Other (Only Display Raw Data): Other PS/2 device, only display raw

data in this mode.

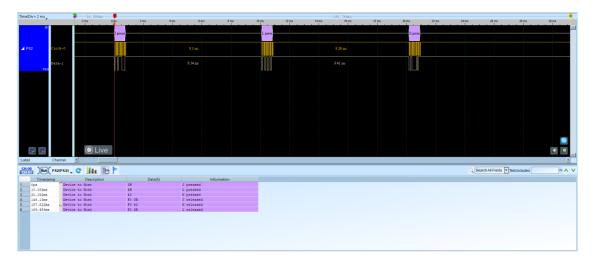
### Startup Setting:

Scan Code: Set the Scan Code Set of PS/2 keyboard.

**Mouse Type:** Set the Type of the PS/2 mouse.

#### Result

Keyboard:

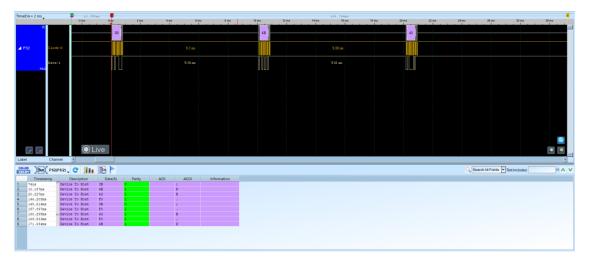


#### Mouse:



ne/Div = 5 ms		<b>P</b>					305.726ms					
· · · ·		35.7 ms	40.7 ms 45.7 ms	60.7 ms	65.7 ms	60.7 ms 65.7 ms	70.7 ms 75.7 ms	10.7 ms 16.7 ms	10.7 ms	96.7 ms	100.7 ms 106.7 ms	110.7 ms
0												
		18 17	F 00 00		18 FF 00 00		28 00 FF 00				18 FF 00 00	
							20001100				1011-0000	
P\$2			13.5									
	Data-1		13.2			12.97 mt						
P8/2		LUI										
01 01												
R, N		OLive										و او
	Channel	O Live										
pel	Channel PS2(PS/2)									C	Search All Fields 💌 Text includes	
Bus Timest	P\$2(P\$/2) , tamp	C Description	Data(h)		Information					C	Search All Fields 💌 Text includes	
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el	PS2(PS/2) tamp	C Description evice to Rost	Data(h)	Byte 1: FFh [7] Y Ove	Packet erflow bit: 1					C	🔾 Search All Fields 💌 Text includes	
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el CI XBuck Ops 36.607ms 36.607ms 36.607ms 36.607ms 36.607ms 36.607ms	PS2(PS/2) tamp De	C Description evice to Rost	Data(h)	Byte 1: FFh [7] Y Ove [6] X Ove [5] Y Sig [4] X Sig [3] Alway	Facket erflow bit: 1 erflow bit: 1 gm Bit: 1 gm Bit: 1 ys 1: 1					C	्रिडarch All Fields 🕝 Text includes	
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Display         Display           Timest         Ops           34.607ms         36.607ms           36.607ms         36.607ms           36.607ms         36.607ms           36.607ms         36.607ms           36.607ms         36.607ms	PS2(PS/2) tamp De	C Description evice to Rost	Data(h)	Byte 1: Ffh [7] Y Ove [6] X Ove [5] Y Sig [4] X Sig [3] Alway [2] Middl [1] Right	Packet erflow bit: 1 gn Bit: 1 gn Bit: 1 ys 1: 1 le Btn: Clicked t Btn: Clicked					C	L Gearch All Fields 🔽 Text Includes	
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el Con XBus ( Con XBus ( Co	PS2(PS/2) tamp De	C Description evice to Rost	Data(h)	Byte 1: FTh [7] Y Ove [6] X Ove [5] Y Sig [3] Alway [2] Middl [1] Right [0] Left Byte 2: Obh [7:0] X Move	Packet erflow bit: 1 gm Bit: 1 gm Bit: 1 ym Bit: 1 le Btn: Clicked Btn: Clicked Btn: Clicked ement: 64 mm					C	् (BarchAl Faids ि Tet Includes	
el Constant Co	PS2(PS/2) tamp De	C Description evice to Rost	Data(h)	Byte 1: Ffh (7) Y Ovr (6) X Ovv (5) Y Sig (3) Alway (2) Middl (1) Right (0) Left Byte 2: 00h (7:0) X Hove Byte 3: 00h	Packet erflow bit: 1 erflow bit: 1 gm Bit: 1 gm Bit: 1 yw J: 1 le Btn: Clicked Btn: Clicked Btn: Clicked ement: 64 mm					C	L (Bearch All Fields ) Text Includes	
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el 200 Deux 201 Deux 202 Deux 202 Deux 202 Deux 202 Deux 203 Deux 204 Deux 20	PS2(PS/2) tamp De	C Description evice to Rost	Data(h)	Byte 1: FTM [7] Y Ovr [6] X Ovv [5] Y Sig [3] Alway [2] Middl [1] Right [0] Left Byte 2: 00h [7:0] X Move Byte 4: 10h	Factors erflow bit: 1 erflow bit: 1 gn Bit: 1 gn Bit: 1 le Btn: Clicked Btn: Clicked Btn: Clicked ement: 64 mm	ſ				C	् िक्साफो Al Fields ि जिस Includes	
Image: Section 2010         Image: Section 2010           Timest         Section 2010           Section 2010         Section 2010	PS2(PS/2) tamp De	C LLE Pecopion Processor	Data(b) 00 00 10 77 00 00	Byte 1: FTM [7] Y Ovy [6] X Ovy [5] Y Saj [4] X Saj [3] Alway [2] Middl [1] Right [0] Left Byte 2: Oth [7:0] X Movy Byte 3: Oth [7:0] Y Movy Byte 4: 18h [3:0] 2 Movy	Factors erflow bit: 1 erflow bit: 1 gn Bit: 1 gn Bit: 1 le Bin: Clicked Bin: Clicked Bin: Clicked ement: 64 mm ement: 64 mm					C	L Gearch Al Finide D Taid Includes	
Open         Open           Copen         36.607as           36.607as         36.607as	P\$2(P\$/2) , tamp De	C Description evice to Rost	Data(h)	Byte 1: FTh [7] Y Ovy [6] X Ovy [6] Y Sij [3] Alwey [2] Middl [1] Right [0] Left Byte 2: 00h [7:0] Y Movy Byte 4: 10h [3:0] 2 Movy Byte 1: FTh	Factors erflow bit: 1 erflow bit: 1 gn Bit: 1 gn Bit: 1 le Bin: Clicked Bin: Clicked Bin: Clicked ement: 64 mm ement: 64 mm	ſ				C	L Bearch AI Fields D Test Includee	

Other (Only Display Raw Data):





# PWM

PWM (Pulse Width Modulation), called pulse width modulation, it is not a bus analysis protocol. It is a very effective technique to control analog circuits by utilizing the pulse width cycle, which is widely used in some rotational speed control, brightness control and temperature control.

#### Settings

🚐 PWM Settings	×
Channel	Color
PWM Channel A0	User can assign color for specific pattern.
Option	
RPM Conversion(cycles/1 revolution)	90% ~ 100%
Show 0%/100% Duty Cycle	80% ~ 89%
Unit of Period Frame s 🔹	70% ~ 79%
Draw PWM Curve	60% ~ 69%
	50% ~ 59%
Source	40% ~ 49%
	30% ~ 39%
Color	20% ~ 29%
Time(X) - Duty.(Y)	10% ~ 19%
Ξ	0%~9%
	Range
Time (X)         Time (X)           Time(X) - Freq.(Y)         Draw 0 Hz	Decode Range
Speed Curve	From To
Color	Buffer Head 🔹 Buffer Tail 💌
	ODefault ✔OK ★Cancel



**PWM Channel**: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

### **Option:**

- RPM Conversion (cycles/1 revolution): Set the number of PWM cycles.
- 2. Show 0% and 100% Duty Cycle: When Time (X)-Period (Y) is selected for plotting, check the box to draw 0% and 100% periods, then the curve will be drawn; otherwise, the curve will not be drawn. If 0% follows 100% or 100% follows 0%, the curve of the two periods will not be drawn.
- 3. Unit of Period Frame: Set the unit of time, user can set s, ms, us.

### Draw PWM curve:

- 1. **Source:** Show the source waveform of the PWM.
- 2. **Time(X)-Duty(Y):** Show the curve diagram with Time(X) and Duty(Y)
- 3. **Time(X)-Freq.(Y):** Show the curve diagram with Time(X) and Freq.(Y)
- 4. **Time(X)-RPM(Y):** Show the curve diagram with Time(X) and RPM(Y)
- 5. **Draw 0 Hz:** When select the Time(X)-Freq.(Y) drawing and check the item Draw 0 Hz, will show the Frequency from 0 Hz at Y axis.
- 6. **Speed Curve:** Supports up to three Curves for overlay drawing.



Pulse	AO	÷	Color
Direction	A1	•	Direction Message H(1):Positive 💌
Curve2			
Pulse	A2		Color 
Direction	A3		Direction Message H(1):Positive 💌
Curve3			
Pulse	A4	•	Color
Direction	A5	<b></b>	Direction Message H(1):Positive 👻

Pulse/Direction: Setting the pulse and direction of the signal

channel on the instrument.

**Direction Message:** Set the direction source to H(1): Positive or L(0):

Positive.

7. Encoder: Encode the PWM parsing result, enabled when checked.



### Result

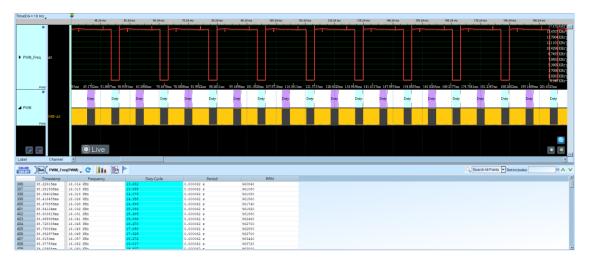
Pive Bel O	PVH-A0 Channel	Duty: 70		7 us		70.000%			Duty: 701	732.00 000%	Duty: 70		Daty: 70	.000%	Daty: 70		Duty: 70.0	772.09 5 000%	Duty: 70.0	00-5	Daty: 70.0	00%	Dety: 70.0	3.00	Duty: 70.0	000%	Duty: 70.0	422 m	Duty: 70		Dety: 70		Duty: 70.0009
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PWW Bel					J us 7	7 w 3 w	7 🗠	3 11	7 to:	3 w:	7 m	3 ш	711	3 დ	7 us	3 ња	7 uz	3 ш.	7 12	3 u.	7 122	3 w	7 m	3 භ	? <del>11</del>	3 102	7 w	3 ш.	7 cc	3 12	7 12	3 uz	7 10
bel (	Channel		) Live																														
	PWM_Ch0	0(PWM) 🔪 🖸	111		Þ			_	_	_	_	_	_	_	_	_		_	_	_		_	_	_	_	_	Q	Searc	th All Field	ts 💌 Te:	xt includes		a /
	istamp		requency			Duty Cyc	cle			Veriod				RPM																			
672.995u		100.000 KHz			70.000				00010 s			6000																					
682.9950		100.000 KHz			70.000				00010 8			6000																					
692.9950		100.000 MMm			70.000				00010 s			6000																					
702.9950		100.000 KHz			70.000				00010 s			6000																					
712.9950		100.000 KHz			70.000				00010 8			6000																					
722.9950		100.000 MHz			70.000				00010 s			6000																					
732.9950	5129	100.000 KHz			70.000			0.00	00010 s			6000																					
742.9950	Sus 3	100.000 KHz		_	70.000			0.00	00010 s			6000	0000																				
752.9950	Sus 1	100.000 MHz			70.000			0.00	00010 s			6000																					
762.9950		100.000 KHz			70.000				00010 #			6000																					
772.9950	Sue :	100.000 KHz			70.000			0.00	00010 #			6000	0000																				
782.9950		100.000 HHz			70.000				00010 s			6000																					
792.9950		100.000 KHz			70.000				00010 #			6000																					
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832.9950		100.000 KHz			70.000				00010 8				0000																				

Select Time(X)-Duty(Y)

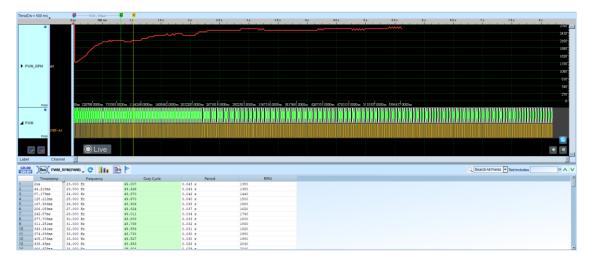
me/Div= 500 us	*								
	190.01 ms	100.01 ms 101.01 ms	101.01 ms 102.31 ms	182.81 ms 183.31 ms	183,81 ms 194,31 ms	184.81 ms 185.31 ms	195.81 ms 195.31 ms	186.81 ms 187.31	
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PWM_Duty A0			• A						40
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PWM	50m 100.0150m 10	Sussein issued in its second	190 21 Youns 190 045 005 191 0	020305 191401305 191770506 1	21515mB 1925525mB 1925050mB 195	5 2650m 195 b010m 194 b365b	a 194,400,000 194,700,000	190,100,000,000,000,000,000,000,000,000,	9155ma 190 2865ma 190 8000
	Dap Dap Dap Dap Dap D	lob Dob Dub Dab Dab Dab Dab Dab Dat	2 Dath Dath Dath Dath Dath Dath D	Dath Dath Dath Dath Dath Dath Dath Dath	6 Dath Dath Dath Dath Dath Dath Dath Dath	Dath Dath Dath Dath Dath Dath Dath D	op Dats Dats Dats Dats Dats Dats I	Sup Deb Deb Deb Deb Deb	Dap Dap Dap Dath Dap Dap Dap
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PWM									
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PWW									-
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_	●Live								
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Di Di Cha	inel I							Q Search All Fields 🛡 Tex	
Di IV Ibel Cha	LDuty(PWM) 🗸 😋 🚺	Duty Cycle	Period	RPM				Q Search All Fields Tex	
bel Char http://www.char http://wwww.char http://www.char http://www.char http://www.char http	LDuty(PWM) C III	Duty Cycle 1.200	0.000125 s	480000				Q Search All Fields Tex	
Image: Second	LDuty(PWM) C IIII 5 Frequency 6.000 2012 68.966 1252	Duty Cycle 1.200 13.793	0.000125 s 0.000014 s					C Search All Fields Tex	
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Log         Chai           tog         Chai <td>Image: Construction         Image: Construction         Image: Construction           construction         Construction         Frequency           construction         Frequency         Frequency</td> <td>Duty Cycle 1.200 13.793 0.452 13.793 0.452 13.793</td> <td>0.000125 s 0.000014 s 0.000110 s 0.000014 s 0.000110 s 0.000014 s</td> <td>480000 4137960 543000 4137960 543000 4137960</td> <td></td> <td></td> <td></td> <td>Q Search All Fields 🛡 Tex</td> <td></td>	Image: Construction         Image: Construction         Image: Construction           construction         Construction         Frequency           construction         Frequency         Frequency	Duty Cycle 1.200 13.793 0.452 13.793 0.452 13.793	0.000125 s 0.000014 s 0.000110 s 0.000014 s 0.000110 s 0.000014 s	480000 4137960 543000 4137960 543000 4137960				Q Search All Fields 🛡 Tex	
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bei         Chai           4.00         Timestam           101         Jean (           24         Timestam           25         Timestam           27         Timestam           28         Timestam           29         Timestam           20         Timestam           20         Timestam           21         Timestam           22         Timestam           23         Timestam           24         Timestam           25         Timestam           26         Timestam           27         Timestam           28         Timestam           29         100,0118           20         120,018           20         120,018           20         120,018	Image         Image <th< td=""><td>Duty Cycle 1.200 13.753 0.452 13.753 0.452 13.753 0.452 13.753 0.450 10.714</td><td>0.000125 s 0.00014 s 0.00014 s 0.000014 s 0.000014 s 0.00014 s 0.00011 s 0.00014 s</td><td>48000 4137960 543000 4137960 543000 4137960 540540 540540 4285740</td><td></td><td></td><td></td><td>Q Search All Fields 💌 Tex</td><td></td></th<>	Duty Cycle 1.200 13.753 0.452 13.753 0.452 13.753 0.452 13.753 0.450 10.714	0.000125 s 0.00014 s 0.00014 s 0.000014 s 0.000014 s 0.00014 s 0.00011 s 0.00014 s	48000 4137960 543000 4137960 543000 4137960 540540 540540 4285740				Q Search All Fields 💌 Tex	
Image: Second	Image         Image <th< td=""><td>Duty Cycle 1, 200 13,753 0,452 13,753 0,452 14,753 0,452 0,450 10,714 0,450</td><td>0.000125 s 0.00014 s 0.00010 s 0.00010 s 0.000014 s 0.000014 s 0.000014 s 0.000014 s 0.000014 s</td><td>480000 4137960 581000 4137960 54000 540540 540540 540540</td><td></td><td></td><td></td><td>G Search All Fields Tex</td><td></td></th<>	Duty Cycle 1, 200 13,753 0,452 13,753 0,452 14,753 0,452 0,450 10,714 0,450	0.000125 s 0.00014 s 0.00010 s 0.00010 s 0.000014 s 0.000014 s 0.000014 s 0.000014 s 0.000014 s	480000 4137960 581000 4137960 54000 540540 540540 540540				G Search All Fields Tex	
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Abel         Chai           24:00         XBao         PWA           24:00         XBao         PWA           25:01         XF         C+45           25:02         XF         C+45           25:01         XF         C+45           25:01         XF         C+45           26:01         XF         C+45           27:01         XF         C+45           28:01         100.015         100.015           28:01         100.015         100.015           28:01         100.015         100.015           29:01         100.015         100.015           20:01         XF         XF           20:02         XF         XF           20:02         XF         XF           20:02         XF         XF           20:02	net         Image: Construction of the construction of	Duty Cycle 1, 200 13, 759 0, 452 13, 759 0, 452 13, 759 0, 453 13, 759 0, 450 16, 714 0, 450 16, 714 0, 450 16, 714 10	0.000135 s 0.00014 s 0.00014 s 0.00010 s 0.000014 s 0.000014 s 0.000011 s 0.000014 s 0.000014 s 0.000014 s	48000 4137960 543000 543000 543000 4137960 540540 4285740 540540 4285740 540540 4285740				् ििक्सारों All Pields 💌 प्रिव	
Image: Characteristic         Characteristic           1000         Characteristic         Public           1100         Characteristic         Public           125         1179         1218           25         1179         1218           25         1179         1218           26         1179         1218           27         179         1218           28         100         0130           29         100         100           21         100         1218           23         100         1218           24         100         1218	Image         Image: Transmission of the transmission of transmission	Duty Cycle 1.200 13.795 0.452 13.795 0.452 13.795 0.452 0.455 0.455 0.455 0.455 0.450 0.45 0.45	0.000135 s 0.000014 s 0.000014 s 0.000016 s 0.000016 s 0.000016 s 0.000011 s 0.000011 s 0.000011 s 0.000011 s 0.000011 s	48000 4137960 543000 4137960 543000 54300 540540 4285740 560540 560540 560540				C. Beach All Fields 🕑 Tee	e e



### Select Time(X)-Freq.(Y)



### Select Time(X)-RPM(Y)





# QEI

QEI (Quadrature Encoder Interface) is a feedback signal (encoder) for small motor control. The QEA/QEB signal is used to obtain the RPM of the motor, and the INDX signal can be used to obtain the angle of rotation of the motor.

### Settings

🚐 QEI Se	ettings			×
Setting			Color	
	Channel QEA QEB	A0 🗘		Angle  Speed
		A2	Range	
		400 e at Rising Edge	From Buffer Head	To Buffer Tail 👻
			ODefault	✓OK XCancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

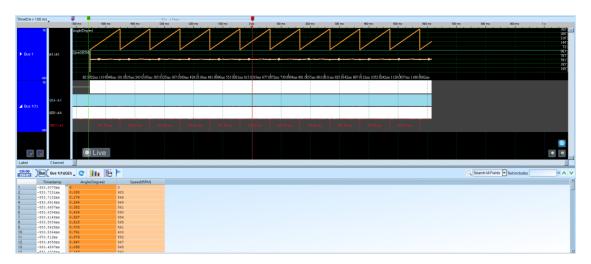
Pulse/Rotation: Set the number of lines of the encoder, the default is 400 lines.

**Start 0 degree at Rising Edge:** Sets the rising edge of the INDX signal to an angle of 0 degrees; the default is for the falling edge to be at an angle of 0 degrees. Enabled when checked.

0

**Draw Curve:** Whether draw the angle/speed curve. Enabled when checked.







# QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

### Settings

🗮 QI Par	rameter Settings	×
Setting		
	QI Channel	A0 Advanced Decode
Color		
	Preamble	▼ Start
_	Head	Parity
	Message	▼ Stop
	CheckSum	<b></b>
Range		
<b></b>	Decode Range	
<b>*</b> *	From	То
	Buffer Head 👻	Buffer Tail 👻
ODefa	ault	✓OK XCancel

**QI Channel:** Show the selected channel.

Advance Decode: show detail message decode



	-							
Time/Div= 20 ms	927.02 ms	957.62 ms 977.62 ms 1.01 s	1.00 s 1.06 s	1.07 s 1.09 s	1.11.6 1.0.6	1.15 s 1.17 s	1.18 5 1.21 5	1.23 s
	\$17.52 mg	Write write write a start	1,005 1,005	1.075		Line Lize		1.200
● ▲ COMM1 CE 0	QI-40 .30.63 mi	Pang Sin Ma Ch — Pang Sin Ma Ma Ma Ma Ma	Me Ge — ?ee Be	lé lé lé lé lé lé Cr	Pressible	Ber Me Ca	Preside De De Ce	
<b>D</b> \$. <b>D</b> \$	OLive							• •
Label Chan	nnel •							
0100 3030								
CH-00 Bus COM	M1(QI) 🗸 😋 🚺 🛃 🖹						Q Search All Fields Text includes	× ^ \
Timestamp	Header(h)	Message(h)	CheckSum(h)	Error				
8 517.37ms								
	Signal Strength (01)	75	74	E1104				
9 967.652ma	Signal Strength (01)	75 6B						
9 967.652ma 0 997.652ma		75 6B Minor Version (0)	74					
9 967.652ma 0 997.652ma 1 997.652ma	Signal Strength (01)	75 68 Mimor Version (0) Major Version (1)	74					
9 967.652ma 0 997.652ma 1 997.652ma 2 997.652ma	Signal Strength (01)	75 6B Minor Version (0) Major Version (1) Manufacturer Code (00 10)	74					
9 967.652ma 0 997.652ma 1 997.652ma 2 997.652ma 3 997.652ma	Signal Strength (01)	75 6B Nimor Version (0) Manufacturer Code (00 10) Besic Device Identifier (00 6A E0 4A)	74 63					
9 967.652ma 0 997.652ma 1 997.652ma 2 997.652ma 3 997.652ma 4 997.652ma	Sigmal Strength (01) Identification (71)	75 68 Minor Version (0) Major Version (1) Maudacturer Code (00 10) Basic Device Identifier (00 6A E0 6A) Ext (0)	74					
9 967.652ma 0 997.652ma 1 997.652ma 3 997.652ma 3 997.652ma 4 997.652ma 5 1.061525a	Signal Strength (01)	75 68 Ninor Version (0) Namifacturer Code (00 10) Basic Device Sensitier (00 4Å 20 4Å) Ext (0) Haximun Power (0Å)	74 63					
9 967.652ma 0 997.652ma 1 997.652ma 2 997.652ma 3 997.652ma 4 997.652ma 5 1.061525a 6 1.061525a	Sigmal Strength (01) Identification (71)	75 68 Hisor Version (0) Hamifacturar Code (00 10) Hamifacturar Code (00 10) The Constitution (00 42 0 44) The Constitution (0) Hatiman Power (14) Power Class (0)	74 63					
9 967.652ma 0 997.652ma 997.652ma 997.652ma 997.652ma 4 997.652ma 4 997.652ma 5 1.061525a 6 1.061525a 7 1.061525a	Sigmal Strength (01) Identification (71)	75 GB (Hard Version (0)) Hinor Version (1) Hamifecturer Code (00 10) Basic Device Destrifer (00 (0Å, 80 (4Å) Ext (0) Haximus Fouwer (0Å) Power (Lass (0) Count (0)	74 63					
9 967.652ms 0 997.652ms 2 997.652ms 2 997.652ms 3 997.652ms 5 1.061525s 6 1.061525s 1 .061525s 8 1.061525s	Sigmal Strength (01) Identification (71)	75 68 Histor Version (1) Meanfacturer Code (10 10) Beanf Dericol Functifier (10 6A E0 4A) Ent (10) Ent (10) Ent (10) Funct (10) F	74 63					
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9 947.652ms 997.652ms 997.652ms 2997.652ms 4997.652ms 997.652ms 51.061825s 51.061825s 81.061825s 91.061825s 01.061825s 91.061825s	Signal Strength (01) Identification (71) Configuration (51)	75 Mayor Version (0) Mayor Version (1) Manufactures Code (00 20) Basic Derice Insettifur (0) GA E0 GA) Ent (0) Formation (0) Formation (0) Frage (0) Frage (0) Manufactures (0) Frage (0) Frage (0) Frage (0)	74 63 81 55					
9         967.652ms           0         997.652ms           1         597.652ms           2         997.652ms           3         597.652ms           4         997.652ms           5         1.061525s           1         1061525s           1         1061525s           1         1061525s           1         1.061525s           1         1.061525s           1         1.061525s           1         1.061525s           1         1.061525s	Signal Strength (01) Identification (71) Configuration (51) Control Error (03)	75 68 Histor Version (1) Mayor Version (2) Mayor Version (2) Basis Device Johnstifier (0) (A E ) (A) Ext (0) Hastims Power (1A) Fower (1A) Fower (1A) Fore (0) Frigg (0) Ext (0) Frigg (0) Ext (0) Frigg (0) Ext (0) Frigg (0) Ext (0) Frigg (0) Ext (0) Frigg (0) Ext (0) E	74 68 81 10					
9 67.652ms 0 997.652ms 1 997.652ms 2 997.652ms 3 997.652ms 4 997.652ms 5 1.061525s 6 1.061525s 9 1.061525s 9 1.061525s 0 1.061525s 2 1.021525s 2 1.221559s	Signal Strength (01) Identification (71) Configuration (51) Control Error (03) Control Error (03)	75 68 Cast Control (1) Main Pression (2) Main Press (2) Marcal Press (2) Marca	74 63 81 10					
9         9         67.652ms           0         997.652ms           1         597.652ms           2         697.652ms           597.652ms         597.652ms           5         1.061525s           1.061525s         1.061525s           1.061525s         1.061525s           1.061525s         1.061525s           1.061525s         1.061525s           1.061525s         1.152146s           1.22259s         1.22259s	Signal Strength (0)) Identification (7)) Configuration (5)) Control Error (03) Control Error (03) Control Error (03)	75 Most Version (8) Most Version (1) Marinetures Cost (0 1) Basic Device Institut (0 4.80 4.0) Results Parce (4) Four Class (8) Cost (8) Kladyo Offent (8) Miadyo Offent (8) Hiddy Offent (8) Hiddy Size (8) 14 Hiddy Size (8) Hiddy Size (8) H	74 63. 81. 88. 10. 10. 10.					
9         9         -87. 652ms           0         897. 652ms           1         997. 652ms           5         997. 652ms           4         997. 652ms           5         1.001525s           1.001525s         1.001525s           9         1.001525s           9         1.001525s           9         1.001525s           1.1001525s           1.1001525s           1.1001525s           1.1001525s           1.12525s           1.12525s           1.12525s           1.12525s           1.12525s           1.12525s           1.12525s           1.12525s           1.1255s           1.1255s           1.1255s           1.1255s           1.1255s	Signal Strength (0) Identification (7) Configuration (5) Control Error (5) Control Error (5) Control Error (5) Control Error (5)	75 68 Hitse Version (0) Major Version (2) Basis Device Identifier (0) (A E) Basis Device Identifier (0) (A E) (A) Ere (0) Prosen Class (0) Freq (0) Hitse (1) Hitse (1	74 63, 81 10 10 10 10 10 10					
9 9 67.652ms 997.652ms 15 997.652ms 2 997.652ms 3 997.652ms 5 97.652ms 5 1.061525s 5 1.061525s 8 1.061525s 9 1.061525s 9 1.061525s 1 .061525s 1 .061525s 1 .061525s 1 .061525s 1 .122559s 3 .1272521s	Signal Strength (0)) Identification (7)) Configuration (5)) Control Error (03) Control Error (03) Control Error (03)	75 Most Version (8) Most Version (1) Marinetures Cost (0 1) Basic Device Institut (0 4.80 4.0) Results Parce (4) Four Class (8) Cost (8) Kladyo Offent (8) Miadyo Offent (8) Hiddy Offent (8) Hiddy Size (8) 14 Hiddy Size (8) Hiddy Size (8) H	74 63. 81. 88. 10. 10. 10.					



# QSPI

QSPI is an enhanced version of SPI, which uses additional data lines to increase throughput in DATA; The data line of QSPI is bidirectional and belongs to parallel transmission

Setti	_											~
CSI QSI	9 Settings											×
Setting								Color				
	Channel								CMD			•
	✓ CS	A0	-	Low Active			•		Address			-
	CLK	A1	\$						Address			
	D0	A2	<b></b>	D4	A	6	*		Data			•
	D1	A3	\$	D5	A	7	-	Range	•			
	D2	A4	* *	D6	A	8	*	<b>5</b>	From		То	
	D3	A5	* *	D7	A	9	-		Buffer Head	Ŧ	Buffer Tail	•
	Mode		CMD+AD	DR	•	MSB	•					
	Significant Bit (D0)		MSB		•							
	Latch Edge		Rising		•							
	Bus Width		4		•							
	Report Column		8		•							
	Image Restorat	ion		Settings								
	User Define For	mat		Settings		0	-					
							(	ODe	efault	<b>√</b> 0К		Cancel

### Channel:

CS: Capture data when CS edge is falling.

CLK: Clock channel.

**D0-D7:** Customizable data channel.

**Mode**: Set the mode of QSPI. It can be set to CMD+ADDR, CMD or DATA, and it can be set to MSB first or LSB first.

Significant Bit(D0): D0 is the MSB or LSB of the data arrangement,

- Take Bus Width = 4 MSB as an example, the Byte combination is D0 D1 D2 D3 D0 D1 D2 D3
- 2. Take Bus Width = 4 LSB as an example, the Byte combination is D3



D2 D1 D0 D3 D2 D1 D0

Latch Edge: Rising/Falling/Both can be selected as the data collection location Bus Width: Optional data 1, 2, 4, 8 lines

**Report Column:** Report presentation mode, 8/16 fields can be selected **Image Restoration:** Save the parsed waveform as a picture for additional reading of the configuration file. Enabled when checked.

**User Defined Format:** User-defined parsing format, which can read additional configure files. Enabled when checked.

\*\* Please note that Image Restoration and User Define Format cannot be enabled at the same time \*\*.

Result	

		37.96 us	38.05 uz	38.15 us		38.25 ui	38.35 us	a 38.45 us	38.55 uz	38.85 uzi	38.75 uz	38.85 ui	38.95 uz	39.26 us	39.15 uz	39.25 uz	39.35 us	39.45 us
۰																		
	00		05	00		05		00	05	00		15 00		05	00		15 00	
CS-A	1	60 m	190 m		60 m	7	190 m	60 ი	190 /	w 6	0 m	190 na	60 ns	190 n:	. [	60 as	190 ne	60 m
JS QSPI	100000	ļĻ		00000				0000.0	000 000000	000000				000 000000	000000			
CLK-I	A.0	80 m			90 m			90 n		в	0 au		80 m			80 au		80 au
D0-A	2																	
GSPI																		
PK. PK		) Live																
				-		-												
( Char	nel I		Þ		_						-					Q Search All F	ields 💌 Text inclus	
Char Bus Bus	QSPI(QSPI) 🖵 🕻	llu P				24 25										Q Search All F	ields 💌 Text includ	
Char Bus Bus Timestamp	QSPI(QSPI) Command	Addres		D1 D2	D3	D4 D5	D6 1	D7 ASC		ormation						Q Search All F	ields 💌 Text Inclus	
Char Bus BUS Timestamp 37.75us	QSPI(QSPI) C Command	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	II Info 4000000.0 4000000.0	00000 FP5						Q Search All F	ields 💌 Text Inclus	
Char Bus BUS	QSPI(QSPI) Command	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0	00000 FP5						Q Search All F	ields 💌 Text inclus	
Char Bus BUS Timestamp 37.75us 38us	Command 05 05 05 05	Addres		D1 D2	D3	D4 D5	D6 1	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0	000000 FPS 000000 FPS 000000 FPS 000000 FPS						Q Search All F	ields 👻 Text includ	
Char Sus Bus Bus Timestamp 37.75us 38us 38.25us 38.5us 38.75us	Command 05 05 05 05 05	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS		_				Q Search All F	ields 💌 Text includ	
Char Char	Command 05 05 05 05 05 05 05 05	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS						Q Search All F	ields 👻 Text includ	
Char Bus Bus Bus Timestamp 37.75us 38.25us 38.25us 38.5us 38.75us	Command 05 05 05 05 05 05 05 05 05 05	Addres 00 00 00 00 00 00 00 00 00 00 00 00 00		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS						Q Search All F	ields 💌 Text includ	
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Char Char	asPI(asPI)         Command           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS						Q Search All F	ields 💌 Text Incluc	
Char Char	asPI(asPI)         Command           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05	Addres 00 00 00 00 00 00 00 00 00 00 00 00 00		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS						C Search All F	ields 💌 Text Incluc	
Char         Char           20         20.0         80.5           Tressen         30.2         80.5           30.2         25.6         30.5           30.2         50.6         39.2           30.3         39.2         50.6           39.2         50.6         39.2           39.2         50.6         39.2           39.2         50.6         39.2           39.2         50.6         39.2           40.2         50.6         50.6	aspi(aspi)         Command           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS 00000 FPS						C Search All F	ields 💌 Text Includ	
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N         Char           005         Data         Bus         Bus           017         75ue         3bus         Bus	aspi(aspi)         Command           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05           05         05	Addres Addres Addres Addres CO		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FFS 00000 FFS						C Search All F	ields 💌 Text Incluc	
Image: Characteristic state         Characteristic state           2000         2000         RUS, RUS, RUS, RUS, State           3010         3010         3010           3011         3010         3010           3012         3010         3010           3013         3010         3010           3014         3010         3010           3015         3010         3010           3016         3010         3010           3017         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010         3010           3010         3010 <td>nel Command 05 05 05 05 05 05 05 05 05 05</td> <td>Addres</td> <td></td> <td>D1 D2</td> <td>D3</td> <td>D4 D5</td> <td>D6 I</td> <td>D7 ASC</td> <td>4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0</td> <td>00000 FFS 00000 FFS</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>Q Search All F</td> <td>ields 💌 Text Incluc</td> <td></td>	nel Command 05 05 05 05 05 05 05 05 05 05	Addres		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FFS 00000 FFS						Q Search All F	ields 💌 Text Incluc	
Image: Characterization         Characterization           37.75ue         26ue           201         Timestamp           37.75ue         26ue           201         25ue           30.51ue         30.51ue           39.51ue         39.75ue           39.75ue         39.75ue           39.75ue         39.75ue           40.25tue         40.25tue           40.25tue         41.85ue           41.25tue         41.5tue	nal Command 05 05 05 05 05 05 05 05 05 05	Addres 00 00 00 00 00 00 00 00 00 00 00 00 00		D1 D2	D3	D4 D5	D6 I	D7 ASC	4000000.4 400000.0 400000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FFS 00000 FFS						Q Search All F	ields 💌 Text Incluc	
All         Char         Char           100         2000         80.5         80.5           17.7         50.0         50.0         80.5           18.0         20.0         50.0         50.0           19.0         20.0         50.0         50.0           19.0         20.0         50.0         50.0           19.0         20.0         50.0         50.0           19.0         20.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0         50.0         50.0         50.0           10.0	nel Command 05 05 05 05 05 05 05 05 05 05	Addres     Addres     Addres     Co     Co		D1 D2	D3	D4 D5	D6 1	D7 ASC	4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0 4000000,0	00000 FFS 00000 FFS						Q Search All F	ields 💌 Text Includ	
Image: Characterization         Characterization           37.75us         38us           38us         38us	nal Command 05 05 05 05 05 05 05 05 05 05	Addres 00 00 00 00 00 00 00 00 00 00 00 00 00		D1 D2	D3	D4 D5	D6 I	ASO	4000000.4 400000.0 400000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0 4000000.0	00000 FFS 00000 FFS						Q Search All F	ields 💌 Text Includ	



### RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

🛤 RC5 Settings		×
Channel		Color
RC5 Channel A0	Option <ul> <li>Extended Mode</li> <li>Isplay without idle in report</li> </ul>	S1 S2
Encoding Method		Toggle 0 🗸
<ul> <li>Mancherster</li> <li>Mancherster with carries</li> </ul>	ier 1 1 0 0	Toggle 1AddressCommand
Range		
From Buffer Head	To Buffer Tail	
	ODefault	✓OK XCancel

### Settings

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

### Option:

1. Extended mode: When the Extended enabled, the S2 will be converted



into seventh bit of the Command. There is an Extend Command on the Waveform Window.

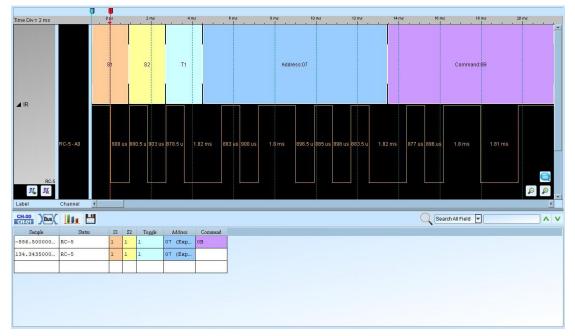
2. Display without idle in report: It will not idle on the Report Window for

the user to observe and analyze data.

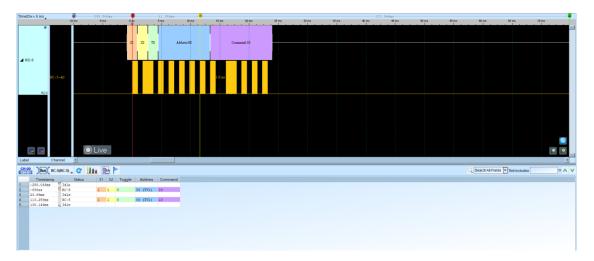
Encoding Method: Mancherster mode and Mancherster with carrier mode.

Result

RC5 without carrier



### RC5 with carrier





## RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

### Settings

🚐 RC6 Settings	×
Channel	Color
RC6 Channel A0 Addr & Cmd Bits 8 Bits Option Display without idle in report	Leader  Start Bit Mode Bits Toggle Bit Control Information
Encoding Method	
<ul> <li>Mancherster</li> <li>Mancherster with carrier</li> </ul>	
Range	
Decode Range	
From To	
Buffer Head 👻 Buffer Tail	▼ ● Default ● OK ★Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and

information in the control label.

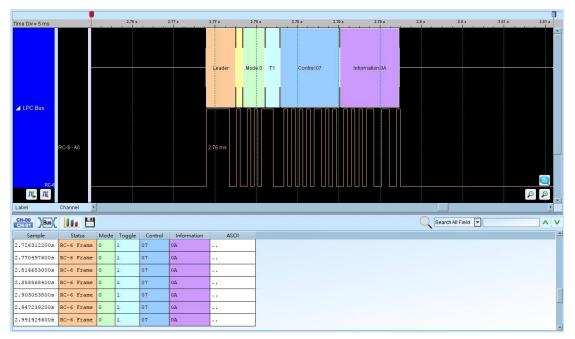


Display without idle in report: Do not display any idle in the Report Window.

Encoding Method: Mancherster mode, Mancherster with carrier mode.

### Result

### **RC6** without carrier



### RC6 with carrier

ime/Div=1	0 ms	2																	
			40.62 s	40.60 s	40.84 s	43.65 s	43.06 s	40.67 s	40.66 s	40.89 s	40.7 s	40.71 s	40.72 s	40.73 #	40.74 s	40.75 s	43.76 s	40.77 s	
🖌 RC-6 de	©			Loader Mod	119 Controls	800F In	formation 9422	Leoder	Mod 10 Co	atel SOOF	Information 040D			Leader Mode T:1	Control 000F	- <u>-</u>	formation.9422		
	RC-6-AO							5.94 me											
15	<b>P</b> <u>U</u>	C	Live																•
Nabel	Channel		) Live																•
Label		•													Q	Search All Fiel	lds 💌 Text include		
Label	Channel	coded(RC-6)	C III		Information	ASCI									Q	Search All Fiel	lds 💌 Text include		
abel	Channel	coded(RC-6) Status RC-6 Frame	C III	control	8422	···\".									Q	Search All Fiel	lds 💌 Text include		
abel 1101	Channel (Bus) RC-6 dev Timestamp 3.526970885s 3.63371538s	Coded(RC-6) Status RC-6 Frame RC-6 Frame	C 1 Mode Toge 6 1 7 0	control 000F 800F	8422 8422	\". \".									۹	Search All Fiel	ids 👻 Text include		•
abel	Channel Bus, RC-6 dev Timestamp 8.526970885s 9.63371538s 9.67697158s	Status RC-6 Frame RC-6 Frame RC-6 Frame	C 1 Mode Tog 6 1 7 0 2 0	000F 800F 800F	8422 8422 040D	···\".									Q	Search All Fiel	ids 💌 Text include		•
abel 11001 13 43 14 43 15 43 16 43	Channel Bus RC-6 der Timestamp 5.526970885s 0.63371538s 0.63371538s 0.67637158s 8.735215855s	Status RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame	C UI Mode Togy 6 1 7 0 2 0 6 1	Control           000F           800F           800F           000F	8422 8422 040D 8422	···\". ····									Q	Search All Fiel	ids 💌 Text include		•
abel 11001 73 43 74 43 75 43 76 43 77 43	Channel Bus RC-6 der Timestamp 8.526970885s 8.63371538s 8.63371538s 8.67697158s 8.735215855s 8.64194035s	status RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame	C 1000 Mode Togy 6 1 7 0 2 0 6 1 7 0	Control           000F           800F           800F           800F           800F           800F           800F	8422 8422 040D 8422 8422	··\". ··\". ··\". ··\".									Q	Search All Fiel	ids 🔻 Text includ		•
3 43 44 43 5 43 6 43 7 43 8 43	Channel Bus RC-6 der Timestamp 5.5269708858 0.633715388 0.676971588 0.676971588 0.676971588 0.676971588 0.676971588 0.676971588 0.676971588 0.676971588 0.641940358 0.605116558	Status RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame	C Mode Togy 6 1 7 0 2 0 6 1 7 0 2 0 2 0	gle Control 000F 800F 800F 800F 800F 800F	8422 8422 040D 8422 8422 8422 040D	··\". ". ".									٩	Search All Fiel	ids 💌 Text include		•
abel 34.00 34.43 54.3	Channel Bus RC-6 der Immestamp 8.5269708058 9.63371538 9.63371538 9.641940358 9.641940358 9.641940358 9.641940358	Status RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame	Mode         Togy           6         1           7         0           2         0           6         1           7         0           2         0           6         1           7         0           2         0           6         1	Control           000F           800F           800F           800F           800F           800F           800F           800F           800F	8422 8422 040D 8422 8422 8422 040D 8422	···\"· ···· ···· ····									Q	Search All Fiel	ids 💌 Text include		•
abel 210210 2100000000	Channel Bus RC-6 dev Timestamp 5.26570855 6.6371555 6.676671555 0.7352156555 0.41940358 0.08116555 0.41940358 0.943400258 0.943400258	Status RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame RC-6 Frame	C Mode Togy 6 1 7 0 2 0 6 1 7 0 7 0 2 0 6 1 7 0 7 0 2 0 6 1 7 0 7 0 2 0 6 1 7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0	Control           000F           800F           800F           800F           800F           800F           800F           800F           800F	8422 8422 040D 8422 8422 8422 040D 8422 8422 8422	····· ···· ···· ···· ····									٩	Search All Fiel	ids 💌 Text include		•
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# **RGB** Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

### Settings

🗮 RGB_IF S	ettings							>	×
Channel									
:									
SCLK	A0 \$	R0	A4	\$	G0	A12	\$ В0	A20 🌲	
DE	A1 \$	R1	A5	\$	G1	A13	B1	A21 🌲	
HSYNC	A2 🌲	R2	A6	\$	G2	A14	🗘 В2	A22 🌲	
VSYNC	A3 🌲	R3	A7	\$	G3	A15	\$ ВЗ	A23 🌲	
		R4	A8	\$	G4	A16	🗘 В4	A24 🌲	
		R5	A9	\$	G5	A17	B5	A25 🌲	
		R6	A10	•	G6	A18	B6	A26 🌲	
		R7	A11	\$	G7	A19	B7	A27 🌲	
Format									
RGB8	388			•	Save	as JPG I	File		
A (Alph	na) F	R (Red)	G (0	Gree	en) l	B (Blue)	L (Lun	ninance)	
0 bits		8 bits	▼ 8 b	its	-	8 bits	▼ 0 bits		
Color									
Color									
		HSY			▼ VSY		▼ DATA	• <b>•</b>	
Range									
De De	ecode Ran	ige							
From					То				
Buffer H	ead			•	Buffer T	ail		•	
					Oefau	It 🗌	<b>√</b> 0К	×Cancel	Ĵ



### Channel

SCLK: The Clock pin.

DE: The Data Enable pin.

**Hsync:** The Horizontal synchronization pin.

**Vsync:** The Vertical synchronization pin.

**R0 – 7, G0 – 7, B0 – 7:** RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of

LA.

### Result

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763 73.	us Bus 1(RGE	Field		D1 (RGB)		D3 (RG8)	D4 (RGB) 13 13 3C	D5 (RG8) 13 13 30	D6 (RG8)	D7 (RG8)		_		_	Q	Search All Fields	Text includes	ax /
763 73. 7764 73. 7765 73.	Bus 1(RGE Timestamp .5631ns .5601ns .569435ns	Field ESYNC La36, D[0:7] La36, D[8:15]	D0 (RGB) 13 13 3C 13 13 3C	13 13 3C 13 13 3C	13 13 3C 1B 12 2C	13 13 3C OE OF 2E	13 13 3C 13 13 3C	13 13 3C OB 16 28	13 13 3C 13 13 3C	13 13 3C OB 0E 26		_		_	Q	Search All Fields	Text includes	IN /
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# RT\_SWI

Realtek Single Wire Interface (SWI) is a communication protocol provided by Realtek. It is an interface designed for data transfer over a single data wire. This interface can help simplify hardware design, reduce wiring complexity, and effectively save space and cost.

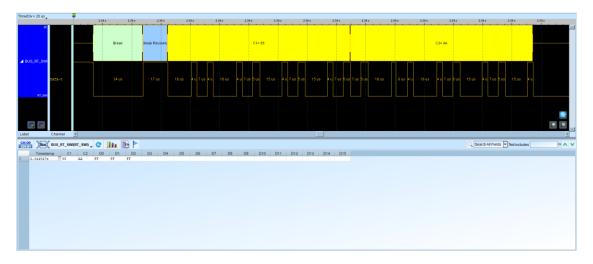
🚢 RT_SWI Settings	×
Parameters	
:	
Channel	
Data	A0
Color	
Break	-
Break Recovery	•
Command	•
Data	•
Range	
Decode Range	
From	То
Buffer Head 👻	Buffer Tail 🔹
Default	✓OK XCancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.



### Result

### Read



#### Write

Time/Dir = 50 us	7.26 s	7.25 #	7.25 x	7.25 x 7.25 x	7.25 x 7.25 x	7.25 x 7.25 x	7.25 s 7.25 s	7.25 # 7.25 # 7.25 #	7.25 x 7.25 x
e)		Break Brea		C1= 12	C2	134	D0= 56	01= 79	D2=AB
DATA-0		34 uş 18 u	6 20 US 20 US 20	us 20 us 20 us	21 us 20 us 21 us 21 us 21 us	1 us 20 us 20 us 21	vs 20 us 21 us 21 u	e 20 us 20 us 20 us 20 us	15 y 16 y 1
Label Channel S C+L00 (Bus_RT_SWIRT) Timestamp C1 1 7,255495 12			D3 D4 D5	D6 D7 D8	D9 D10 D11 0	12 D13 D14 D15		C Search All Field	B Text includes



# SAE J1850

SAE J1850 is an automotive communication protocol used primarily for on-board diagnostics (OBD) and in-vehicle networking. It was widely used in vehicles before CAN (Controller Area Network) became the standard. J1850 allows different electronic control units (ECUs) to communicate within a vehicle.

J1850 Settings					>
arameter		Color			
Channel A0 C Bit Order LSB First  MSB First Invert Waveform Manufacture		SOF DATA EOD NB Range From	Decode Range	IFR EOF IFS BRK	
GM	•	_	er Head 👻	Buffer Tail	-
O PWM	8	us	) VPW		
Active Phase "0"	16	us	Short Pulse	64	us
BitTime	24	us	Long Pulse	128	us
SOF/EOD Time	48	us	SOF/EOD Time	200	us
EOFTime	72	us	EOF Time	280	us
IFSTime	96	us	BRKTime	300	us
Active SOF	32	us	IFSTime	300	us
Active BRK	40	us	ino nine	300	us
BRK to IFS Time	120	us			
			ODefault	<b>√ок</b>	XCancel



**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

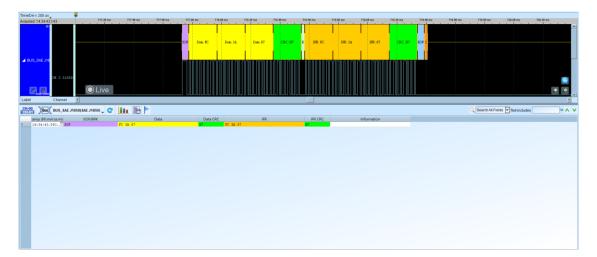
**Bit Order:** Select the transferred bit order. Default is MSB first.

**Invert Waveform:** Invert the waveform for analyzing. Enable while checking. **Manufacture:** Select the Manufacture. Due to different manufacture defined different NB value to indicate enable CRC or not. Please note that, this combo box can only be accessed when the transferred method had been adjusted to VPW. We only support GM and Chrysler now, if user need more manufacture candidate, please contact us.

**Transfer Method:** Select the transferred method. Default is VPW. PWM and VPW has different timing parameters. User can adjust the value manually.

#### **Result:**

#### PWM:



VPW:







### S/PDIF

It is a digital audio interface that can be transmitted using either wire or fiber optics. It is called the Sony/Philips Digital Interconnect Format (also known as Sony Philips Digital InterFace). These two companies are the primary specification developers, and the specification is derived from the AES/EBU professional digital audio interface, with some modifications for use in lower-cost hardware.

### Settings

S/PDIF Settings		×
Setting		
	Block	
		Data Bits
Channel A0	192 (32 ~ 192) frames	16 👻
✓ Auto detect Bit Rate	Bit Order	Parity mode
49.152 (768 kHz) - Mb/s	Aux Data LSB first 👻	Even parity 👻
(384Kb/s~49.152Mb/s)	Audio Data LSB first 💌	
Display the audio waveform		<ul> <li>Playback</li> </ul>
Color		
Preamble	✓ User bit	•
Aux Data	<ul> <li>Channel Status bit</li> </ul>	-
Audio Data	▼ Parity Bit	•
Validity bit	•	
Range		
Decode Range		
From To		
Buffer Head 💌 Buffer Ta	ail 🔹 💿 Default	VOK XCancel

Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.



Num of frame: 192 frames within each block by default, used to analyze each

sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

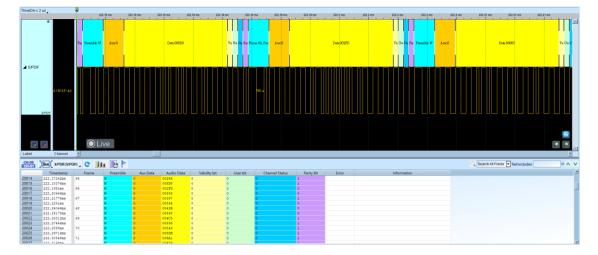
Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

Parity mode: The default is even parity.

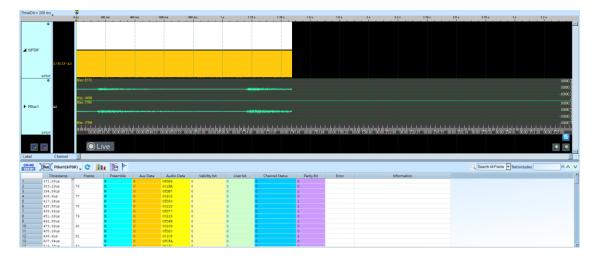
Display the audio waveform: Click to display the audio waveform in the

Waveform Window.



#### Result

Show wave:





# SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for

interfacing with SD (Secure Digital) Flash memory cards.

### Settings

🚞 SDIO,	/SD3.0 Settings					×
Settings	Channel	● SD Mode		Color		
	CLK     A0       CMD     A1       D0     A2       D1     A3       D2     A4       D3     A5	Command     Data     Startup Settings     1-bit Data     4-bit Data     4-bit DDR	SDIO 1/O Block Size Block Size Settings Options Adv. Report 3 Pin Mode No CLK Mode ✔ Auto Phase Correction	Range	Command Response Start Bit Data CRC Status BUSY	
		Startup Settings	Option Adv. Report		From Buffer Head	To Buffer Teil 💌
					Default OK	Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

### SD Mode, analyzed in SPI mode:

Command: Analyze Command.

Data: Analyze Data.

**SDIO I/O Block Size:** Set the block size of CCCR and FBR of SDIO.

SDIO Block Siz	e Setting	×
Card Common Cont	rol Registers (CCC	CR)
Fn0 Block Size	256	bytes
Function Basic Regi	sters (FBR)	
Fn1 Block Size	256	bytes
Fn2 Block Size	256	bytes
Fn3 Block Size	256	bytes
Fn4 Block Size	256	bytes
Fn5 Block Size	256	bytes
Fn6 Block Size	256	bytes
Fn7 Block Size	256	bytes
	OK	Cancel



**Options:** 

- 1. Adv. Report: Show details. Enabled when checked.
- 2. 3 Pin Mode: Analyze the data using CLK, CMD, and D0.
- **3.** No CLK Mode: Analyze the data using CMD line only.
- 4. Auto Phase Correction: Automatically adjusts the phase of measurement.

### SPI Mode, analyzed in SPI mode:

- **1. Detect CRC7:** Detect CRC 7 or not. Enabled when checked.
- 2. Adv. Report: Show details. Enabled when checked.

#### Result

CMD mode

iv= 2 us	2										
	30 x	201 201	30 1 30 1		30 # 30 #	20 x 20 x	30 # 30 #	30 #	20 x	20 #	30 #
		CMI 00h 04h 16h 00h 78h R	1:R 00h 00h 09h 00h <b>69h 🔤</b> C	CME OUN 01h OOh	00h 29h R1 5 00h 00h 09	h 00h 1Fh					
	UTITION AND ADD THE OTHER DATE										
IO-CMD CLR-A0											
				ו וחו							
CHD-A1		935 nz 605 n	1.4 tu 535 n 595 n	1 10 1.14	4 us 1.34 us	670 m					
SDIO/SD3 0											
10.00	OLive										
- · · ·											
Channel											
	D(SDIO/SD3.0) 🗸 😋 🚺								C Search All Fields	Text includes	
Timestamp	D(SDIO/SD3.0) U C IIII	Response	Argument	CRC (h)	Frequency Timing	Information			Q Search All Fields	Text includes	
Timestamp 30.00973642a	Command		00 00 09 00	CRC (h)	15MHz Nor: 2	Information			C Search All Fields	Text includes	
Timestamp 30,00973642# 30,009829915#		Response R1 :RESP13:SEND_STATUS	00 00 09 00 00 04 D6 00	CRC (h)	15MHz Nor: 2 15MHz Nrc: 1354	Information			C Search All Fields	Text includes	
Timestamp 30.00973642a	Command CHD18:READ_MULTIPLE_BLOCK	Response	00 00 09 00 00 04 D6 00 00 00 09 00	CRC (h) 17 78 69 29	15MHz Nor: 2	Information			Q Search All Fields	Text includes	
Timestamp 30.00973642s 30.009829915s 30.009833315s	Command	Response R1 :RESP13:SEND_STATUS	00 00 09 00 00 04 D6 00	CRC (h) 17 78 69 29 17	15MHz Nor: 2 15MHz Nrc: 1354 15MHz Nor: 2	Information			C Search All Fields	Text Includes	
Timestamp 30,00973642s 30,009829915s 30,009833315s 30,00983697s	Command CHD18:READ_MULTIPLE_BLOCK	Response R1 :RESP13:SEND_STATUS R1 :RESP18:READ_NULTIPLE_BL. R1 :RESP13:SEND_STATUS	00 00 09 00 00 04 DE 00 00 01 00 09 00 00 01 00 00 00 04 DE 00	CRC (h) 17 78 69 29 17 78	15MHz Bori 2 15MHz Brci 1354 15MHz Bori 2 15MHz Brci 5 15MHz Brci 5 15MHz Brci 2	Information			C Search All Fields	Text includes	
Timestamp 30.00973642s 30.009829915s 30.009833315s 30.00983697s 30.00983697s 30.00983865s 30.009937265s	Command CMD18:READ_MULTIPLE_BLOCK CMD18:SEND_STATUS CMD18:READ_MULTIPLE_BLOCK	Response R1 :RESPI3:SEND_STATUS R1 :RESPI8:READ_MULTIPLE_BL.	00 00 09 00 00 04 DE 00 00 04 DE 00 00 00 09 00 00 01 00 00 00 04 DE 00 00 00 9 00	CRC (h) 11 78 69 25 11 78 69	15MHz         Nor: 2           15MHz         Nrc: 1354           15MHz         Nrc: 2           15MHz         Nrc: 5           15MHz         Nrc: 12           15MHz         Nrc: 1354           15MHz         Nrc: 2	Information			C Search All Fields	Text includes	
Timestamp 30.00973642s 30.009829915s 30.009833315s 30.0098386597s 30.00983865s 30.009937865s 30.009947265s	Command CMD18:READ_MULTIPLE_BLOCK CMD13:SEND_STATUS	Response R1 :RESF13:SEND_STATUS R3 :RESF18:READ_MULTIPLE_BL. R1 :RESF13:SEND_STATUS R3 :RESF18:READ_MULTIPLE_BL.	00 00 09 00 00 04 DE 00 00 00 09 00 00 01 00 00 00 00 09 00 00 00 09 00 00 00 DE 00 00 00 09 00 00 00 09 00	CRC (h) 17 78 69 25 17 78 69 29	15MM         Nor: 2           15MM         Nrc: 1354           15MM         Nrc: 1354           15MM         Nrc: 5           15MM         Nrc: 1354           15MM         Nrc: 1354           15MM         Nrc: 1354           15MM         Nrc: 1354	Information			C Search All Fields	Text includes	
Timestamp 30.00973642s 30.00923915s 30.00983315s 30.00984037s 30.00994037s 30.00993365s 30.009937265s 30.00994032s 30.00994432s	Command CHD18:READ_HOLTIFLE_BLOCK CHD13:SEND_STATUS CHD18:READ_HOLTIFLE_BLOCK CHD13:SEND_STATUS	Response R1 :RESP13:SEND_STATUS R1 :RESP18:READ_NULTIPLE_BL. R1 :RESP13:SEND_STATUS	00 00 09 00 00 04 D6 00 00 00 09 00 00 00 09 00 00 00 09 00 00 04 D6 00 00 00 09 00 00 00 09 00 00 00 09 00	CRC (h) 17 78 69 29 17 78 69 29 29 29 29 29 17	15MHr Nori 2 15MHr Nori 154 15MHr Nori 254 15MHr Nori 2 15MHr Nori 2 15MHr Nori 1354 15MHr Nori 1354 15MHr Nori 5	Information			C Search All Fields	Text includes	
Timestamp 30.00973642s 30.00929915s 30.00983815s 30.00984037s 30.00984037s 30.00994032s 30.00994052s 30.0099442s 30.0099442s	Command CMD18:READ_MULTIPLE_BLOCK CMD18:SEND_STATUS CMD18:READ_MULTIPLE_BLOCK	Response R1 :RESP1::GEND_STATUS R1 :RESP1::GEND_STATUS R1 :RESP1::SEND_STATUS R1 :RESP1::GEND_NULTP1E_BL R1 :RESP1::SEND_STATUS	00 00 09 00 00 04 D6 00 00 00 00 00 00 00 00 00 00 00 00 00	CRC (h) 17 78 69 29 17 78 69 29 29 29 29 29 27 78	150Hz         Nori 2           150Hz         Nori 1354           150Hz         Nori 2           150Hz         Nori 3           150Hz         Nori 3           150Hz         Nori 3	Information			C Search All Fields	Text includes	
Timestamp 30.00973642 30.00928915s 30.009828915s 30.00983815s 30.00983857 30.00993865s 30.00993865s 30.00994052s 30.00994432s 30.010037115s	Command CHOIS:READ_MOLTPLE_BLOCK CHOIS:READ_MOLTPLE_BLOCK CHOIS:READ_MOLTPLE_BLOCK CHOIS:READ_MOLTPLE_BLOCK	Response R1 :RESF13:SEND_STATUS R3 :RESF18:READ_MULTIPLE_BL. R1 :RESF13:SEND_STATUS R3 :RESF18:READ_MULTIPLE_BL.	00 00 09 00 00 04 DF 00 00 00 09 00 00 00 00 00 00 00 00 00 00 04 DF 00 00 04 DF 00 00 00 09 00 00 00 09 00 00 00 09 00 00 00 00 00	CRC (h) 17 69 29 17 78 69 29 29 29 29 29 17 79 69	15000         Nori 2           15000         Nroi 1354	Information			C Search All Fields	Text Includes	
Timestamp 30.00973642s 30.00923915s 30.00983815s 30.0098365s 30.0098365s 30.009933865s 30.009937855 30.0099442s 30.0099442s 30.010037815s 30.01004447s	Command CHD18:READ_HOLTIFLE_BLOCK CHD13:SEND_STATUS CHD18:READ_HOLTIFLE_BLOCK CHD13:SEND_STATUS	Response R1 HESPIJIED STATUS R1 HESPIJIERAD MULTIPLEJEL R1 HESPIJIERAD MULTIPLEJEL R1 HESPIJIERAD MULTIPLEJEL R1 HESPIJIERAD JULTIPLEJEL	00 00 09 00 00 42 be 00 00 01 90 00 00 01 00 00 00 00 09 00	CRC (h) 17 18 19 29 27 29 29 29 29 29 29 29 29 29 29	SNM:         Nor:         2	Information			Q (Search All Fields	Text includes	
Timestamp 30.00973642s 30.00983315s 30.00983315s 30.009833657s 30.00984037s 30.00994092s 30.00994092s 30.00994092s 30.00994432s 30.00994425s 30.01004427s	Command CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK	Response R1 :RESP1::GEND_STATUS R1 :RESP1::GEND_STATUS R1 :RESP1::SEND_STATUS R1 :RESP1::GEND_NULTP1E_BL R1 :RESP1::SEND_STATUS	00 00 09 00 00 04 05 00 00 04 05 00 00 01 00 05 00 00 04 05 00 00 04 05 00 00 04 05 00 00 04 05 00 00 00 05 00 00 00 00 00 00 00 00 00 00 00 00	CRC (h) 17 73 69 17 17 18 69 69 17 15 19 17 15 19 17 17	15HH:         Nor:         2           15MH:         Nrc:         1354           15MH:         Nrc:         1354           15MH:         Nrc:         1           15MH:         Nrc:         2           15MH:         Nrc:         2           15MH:         Nrc:         2           15MH:         Nrc:         2           15MH:         Nrc:         5           15MH:         Nrc:         5           15MH:         Nrc:         5	Information			C Bearch All Fields	Text Includes	
Timestamp           30.00973642a           30.00923642a           30.00923915a           30.00983315b           30.00984087a           30.010037615a           30.010041215a           30.01004447a           30.0104447a           30.0104447a           30.011766a	Command CHOIS:READ_MOLTPLE_BLOCK CHOIS:READ_MOLTPLE_BLOCK CHOIS:READ_MOLTPLE_BLOCK CHOIS:READ_MOLTPLE_BLOCK	Reports R1 :RES91:SED_STATUS R1 :RES91:READ_MULTIPLE_BL R1 :RES91:SEAD_MULTIPLE_BL R1 :RES91:SEAD_MULTIPLE_BL R1 :RES91:SEAD_MULTIPLE_BL R1 :RES91:SEAD_STATUS R1 :RES91:SEAD_STATUS	00 00 09 00 00 04 05 00 00 00 05 00 00 00 05 00 00 04 05 00 00 04 05 00 00 00 05 00	CRC (h) 12 75 69 29 29 29 29 29 29 29 29 29 29 29 29 29	Linkit         Nort 2	blomation			C Bearch All Fields	Text Includes	
Timestamp 30.009736428 30.009236435 30.00933675 30.00933675 30.0094338 30.0094337 30.0094328 30.00944328 30.00944328 30.00944328 30.00944328 30.019444278 30.01044278 30.011431658	Command CHEDISIERED_MILTIPLE_BLOCK CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS	Response R1 HESPIJIED STATUS R1 HESPIJIERAD MULTIPLEJEL R1 HESPIJIERAD MULTIPLEJEL R1 HESPIJIERAD MULTIPLEJEL R1 HESPIJIERAD JULTIPLEJEL	00 00 09 00 00 04 06 00 00 00 09 00 00 00 09 00 00 04 09 00 00 00 09 00 00 00 00 00 00 00 00 00 00 00 00 00	CRC (h) 17 73 69 29 17 18 29 29 29 29 29 29 29 29 29 29 29 29 29	LAMME         Dict 2           LAMME         Hort 1354           LAMME         Hort 1354           LAMME         Hort 135           LAMME         Hort 5           LAMME         Hort 2	Information			C Bearch All Fields	Text Includes	
Timestamp 30,009736428 30,009236428 30,009338459 30,0093386978 30,0093386978 30,0093386978 30,009340928 30,00944028 30,00944028 30,00944028 30,01044278 30,01044278 30,010442788 30,010442788	Command CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK CHEDISIERAD_MILTIPLE_BLOCK	Reports RI 14229131020_312435 RI 14229131020_312435 RI 14229131020_312435 RI 14229131020_312435 RI 14229131020_31247 RI 14229131020_31247 RI 14229131020_31247 RI 14229131020_31247 RI 14229131020_31247	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	CRC (h) 17 78 69 17 18 17 19 29 29 29 29 29 29 17 19 19 19 29 29 29 20 20 20 20 20 20 20 20 20 20 20 20 20	1988         Hort 2           1988         Hort 3           1988         Hort 3           1988         Hort 5           1988         Hort 1344           1988         Hort 1344           1988         Hort 1344           1988         Hort 2	Information			C Bearch All Fields	Text Includes	
Timestamp           30.00973642           30.00973642           30.00973642           30.009833154           30.00983354           30.009843354           30.009843354           30.009843354           30.009843354           30.009844328           30.009844328           30.019444128           30.019444128           30.019444278           30.01144768           30.01144565           30.01144565           30.01144565           30.01148522a	Command ODI-IFEED_MELTIFEE_LLOOP ODI-IFEED_STATUS ODI-IFEED_STATUS ODI-IFEED_STATUS ODI-IFEED_STATUS ODI-IFEED_STATUS ODI-IFEED_STATUS	Reports R1 :RES91:SED_STATUS R1 :RES91:READ_MULTIPLE_BL R1 :RES91:SEAD_MULTIPLE_BL R1 :RES91:SEAD_MULTIPLE_BL R1 :RES91:SEAD_MULTIPLE_BL R1 :RES91:SEAD_STATUS R1 :RES91:SEAD_STATUS	0         0	CRC (h) IF 773 69 25 17 29 17 29 17 29 17 29 29 17 29 29 29 29 29 29 29 29 29 29	LAMME         Dict 2	Information			C Bearch All Fields	Text Includes	
Timestamp           30.00973642           30.00973642           30.00973642           30.00973642           30.009830567           30.009830567           30.009830567           30.009830567           30.009830765           30.009830765           30.00984027           30.00984027           30.00984126           30.00194417           30.0101421765           30.01145167           30.01145167           30.01145167           30.01145167           30.01145167           30.01145167           30.01145167           30.01145167	Command CHEDISIERED_MILTIPLE_BLOCK CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS CHEDISIERED_STATUS	Reports           R1         HESTRI 1950, 071475           R1         HESTRI 1950, 071475	0         0	CRC (h) 17 73 69 17 18 65 17 75 69 17 75 17 19 17 19 17 19 19 17 19 19 17 19 19 19	1986         Hort 2           1986         Hort 1           1986         Hort 2           1986         Hort 3           1986         Hort 5           1986         Hort 5           1986         Hort 7           1986         Hort 5           1986         Hort 1           1986         Hort 5           1986         Hort 184           1986         Hort 184	Information			C. (Bearch All Fields	Text Includes	
Timestamp 30.0073642a 30.0073642a 30.0073642a 30.0073642a 30.00733657a 30.007433557a 30.007433557a 30.007443557 30.0074512a 30.00544427b 30.0124427b 30.0124427b 30.01244555 30.0124457b 30.01244555 30.0124457b	Command Obility Status Obility Status	Reports RI 14229131020_312435 RI 14229131020_312435 RI 14229131020_312435 RI 14229131020_312435 RI 14229131020_31247 RI 14229131020_31247 RI 14229131020_31247 RI 14229131020_31247 RI 14229131020_31247	0         0	CRC (h) 17 19 29 29 29 29 29 29 29 29 29 29 29 29 29	1986         Horr 2           1986         Horr 1           1986         Horr 2           1986         Horr 3	Information			C. Bearch All Fields	Text Includes	
Timestamp           30.00973642           30.00973642           30.00973642           30.00973642           30.00983726           30.00983726           30.00983726           30.00983726           30.00983726           30.00984726           30.00984726           30.00984726           30.00094427           30.001421765           30.01145165           30.01145165           30.01145165           30.01245155           30.01245155           30.01245155           30.01245155           30.01245155           30.01245155           30.01245155           30.01225156           30.01225156           30.012251575	Command ODI-I-HEAD JAULTIFLE JLLOIF ODI-I-HEAD JAULTIFLE JLLOIF	Response           11 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)	0         0	CRC (h) 12 79 69 29 27 29 29 29 29 29 29 29 29 29 29	15000         Horr 2           15000         Horr 2         1344           15000         Horr 2         140           15000         Horr 2         140           15000         Horr 2         140           15000         Horr 2         140           15000         Horr 1         154           15000         Horr 2         150           15000         Horr 2         150	Information			C. (Bearch All Fields	Text Includes	
Trestamp 30.0073642 30.0073642 30.0073642 30.00833138 30.00833138 30.00843118 30.00843118 30.00843118 30.008431218 30.00844328 30.00844328 30.00344428 30.00146128 30.00146158 30.001458 3	Command Obility Status Collises Jestity Jucci Collises Justity Collises Justity Collises Justity Collises Jestity Collises Jestity Collises Jestity Collises Jestity Collises Jestity Collises Jestity Collises Jestity	Reports           R1         HESTRI 1950, 071475           R1         HESTRI 1950, 071475	0         0         0         0         0         0           0	CRC (h) 14 25 25 25 26 26 27 26 27 27 26 27 27 27 27 27 27 27 27 27 27 27 27 27	1986:         Der: 2           1986:         Der: 154           1986:         Der: 2           1986:         Der: 5           1986:         Der: 5           1986:         Der: 1344           1986:         Der: 2	Information			C. Bearch All Fields	Text Includes	
Timestamp           30.00973642           30.00973642           30.00973642           30.00973642           30.00983785           30.00983785           30.00983785           30.00983785           30.00983785           30.00983785           30.009837255           30.0098437255           30.00094437           30.001481785           30.001481785           30.01148165           30.012481785           30.0124812755           30.012281378           30.012281378           30.012281378           30.012281378	Command Obility Status Obility Status	Response           11 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)           21 (18573) 10502 (15702)	0         0         0         0         0         0           0	CRC (h) 16 27 28 29 29 29 29 29 29 29 29 29 29	15000         Horr 2           15000         Horr 2         1344           15000         Horr 2         140           15000         Horr 2         140           15000         Horr 2         140           15000         Horr 2         140           15000         Horr 1         154           15000         Horr 2         150           15000         Horr 2         150	blomation			C. Bearch All Fields	Text Includes	



### Adv. Report

2 us	<b>P</b>												
	33 #	30 # 30 # 36	30 # 30 #	30 #	20 x	30 #	30 # 30 #	20 x	30 #	30 x	20 #	20 #	* * * *
Θ													
		CMI 00h 04h 16h 00h 78h R1	R 00h 00h 09h 00h 69h CME	00h 01h 00h 001	D 200 0 01 T 1	0h 00h 09h 00h 1							
		Cont dan Dan Dan dan Par		Con one out out		on our own our							
CLK-A0													
						1 1 1							
CND-A1		935 m2 605 m	1.4 us 535 n 595 n	1 10 1.14 10		1.34 10 670 00							
IDIO/SD3 0													
. <i>1</i> 2	OLive												
Channel													
Charmen	<u> </u>												
Bus SDIO-CM	(SDIO/SD3.0) 😋 🛄 💼									C	Search All Field	5 Text includes	0
	o(sDio/sD3.0) 🖵 🧲 🛄 💼					-				C	Search All Field	6 🔻 Text includes	0
Timestamp	Command	Response	Argument		Frequency	Timing	Information			C	Search All Field	5 🐨 Text includes	D4
Timestamp 195n#			00 01 00 00		Frequency 15MBs	Timing	Information			C	Search All Field	6 💌 Text includes 🛛	D.
Timestamp 195n# 195n#	Command	Response	00 01 00 00 RCA: 0001h	29 1	LSMHz		Information			C	Search All Field	8 💌 Text includes 🛛	Ex.
Timestamp 195ns 195ns 3.595us	Command		00 01 00 00 RCA: 0001h 00 00 09 00	29 1	LSMHIE	Timing Nor: 2	Information			C	L Search All Field	8 💌 Text includes 🛛	CX
Timestamp 195ns 195ns 3.595us 3.595us 3.595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 09 00 [31] 00T_0F_RANGE: no er_	29 1	LSMHz		Information			C	Search All Field	5 Text includes	ex.
Timestamp 195ns 195ns 3.595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 09 00 [31] OUT_OF_RANGE: no er [30] ADDRESS_ERROR: no e	29 1	LSMHz		Information			C	Search All Field	s 🛡 Text includes (	
Timestamp 195ns 195ns 3.595us 3.595us 3.595us 3.595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 09 00 [31] 00T_0F_RANGE: no er_	29 1	LSMHz		Information			C	Search All Field	9 Text Includes	0
Timestamp 195ns 195ns 3,595us 3,595us 3,595us 3,595us 3,595us 3,595us 3,595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 09 00 [31] OUT_OR_RANGE: no er. [30] ADDRESS_ERROR: no er. [27] IRASE_PARAM: no err. [26] WP_VIOLATION: no pr. [25] CARD_IS_LOCKED: car.	29 1	LSMHz		Information			C	Search All Field	9 Text Includes	0
Timestamp 195ns 195ns 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 09 00 [31] 00T_0F_RANNE: no er [30] ALDERES_ERROR: no er [21] ERARE_RARN: no er [25] CARD_IS_LOCKED: car. [24] LOCK_UNILCOCK_FAILED:.	29 1	LSMHz		Information			C	Search All Field	8 💌 Text Includes	CX
Timestamp 195ns 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 00 00 [31] 00T_0T_RANGE: no er. [37] REARE PARAMI no err. [26] WP YOUARTION no pr. [26] WP YOUARTION no pr. [26] LOCE_ONLOCK_FAILED: [23] COM_CR_EXBOR: no e.	29 1	LSMHz		Information			C	L Search All Field	8 💌 Text includes [	es
Timestamp 195ns 195ns 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us	Command	Response	00 01 00 00 RCA: 0001h 00 00 00 00 [31] 007_0F_PANDE1 no er. [27] ERANE_PANDE1 no er. [28] KB_VICALTION: no pr. [28] CABS_15_LOURDED: on. [24] LOCE_UNDCOK_FAILED: [23] COM_COK_ERADEN: no . [23] ILLEGAL_COMMANN: no.	29 1	LSMHz		Information			C	L Search All Field	8 💌 Text includes [	EX.
Timestamp 195ns 195ns 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us	Command	Response	00 01:00 00 HEAL 0001h D0 00 00 00 D111 007_0F_RANGE: no er. 127 IEAAE_FARAN: no er. 128 IEAAE_FARAN: no er. 129 IEAAE_FARAN: no er. 129 IEAAE_FARAN: no er. 129 IEAEE_FARAN: no er. 120 IEAEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEE	29 1	LSMHz		Information			C	L Search All Field	0 Text includes [	, ex
Timestemp 1950s 1950s 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us 3.595us	Command	Response	00 01:00 00 EGLA: 0001h 00 00 00 00 131 007_07_MANGES: no err. 137 104AG_TARAN: no err. 136 104D_11AIAO: no err. 136 104D_11AIAO: no err. 135 104D_11AIAO: no err. 131 104D_11AIAO: no err. 132 11LEAAL.006_TAILDI: 132 11LEAAL.006_TAILDI: 133 1006_CFAILDI: no err. 130 1006_CFAILDI: no err. 130 1006_CFAILDI: no err. 130 1006_CFAILDI: no err.	29 1	LSMHz		Information			C	L Search All Field	8 👿 Text Includes [	, sx
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Timestamp           195cs           195cs           3,555tas	Command	Response	00 01.00 00 FCLA: 0001b 00 00 00 00 313 007_07_MANGES: no er. 1001 ACCRESS_EXEGG: no e. 1217 ERALE_PARAM: no err. 128 (ALE_JEANN: no err. 129 (ALE_JEANN: no err. 123) COLE_GTC_SERGG: no e. 123 (ALE_GTC_SERGG: no error 124) EXEGN: no error 124) EXEGN: no error 125 (CL_SEGN: no error 126) EXEGN: no error 126) CSS_OVERBRITE: no e. 155 WF_JEANS_SITE: no p.	29 1	LSMHz		Information			C	k Search All Field	9 Text includes [	5
Timestamp           195cs           195cs           3, 595us           3, 595us	Command	Response	60 01 00 00 ECAL 0001b 10 00 00 00 10 00 1	29 1	LSMHz		Information			C	L Search All Field	9 Text includes	5
Timestamp           195cs           195cs           3,555tas	Command	Response	00         00         00           00         00         00           01         007         07         080           101         007         07         080         00           101         007         07         080         00         00           101         007         07         080         000         00         00         00         000         00         000	29 1	LSMHz		Information			C	L Search All Field	0 Text includes (	
Timestamp           195cs           195cs           3.555us	Conned * 06131808_553193	Response	00 01 00 00 ECAL 00016 00 00 00 00 101 007_07 AANGE: no er. 100 AANGESS_BEAGG: no e. 100 AANGESS_BEAGG: no e. 101 CALGESS CALENCE: no e. 102 CALENCE: CALENCE: no e. 102 CALENCE: CALENCE: no e. 102 CALENCE: NO ENCOMENT 103		I SHRE		Information			C	L Gearch All Field	9 Text includes	, cs
Timestamp           195cs           195cs           3.555us           3.555us	Command	Response	0010000           0010000           0010000           0010000           0010000           00100000           00100000000           0010000000000000000000000000000000000		I SHRE	Nori 2	Information			C	L (Bearch All Field	5 Text includes (	a (
Timestamp           195cs           195cs           3.555us	Conned * 06131808_553193	Response	00         00         00           00         00         00           00         00         00           00         00         00           01         000         00           01         000         00           01         000         00           01         000         00           01         000         00           01         000         00           01         000         00           01         000         00           01         000         00           01         000         000           01         000         000           01         000         000           01         000         000           010         000         000           010         000         000           010         000         000           010         000         000		L SMHz	Nori 2	Information			C	L (Bearch All Field	s Text includes	)0 

No CLK mode:



: Analyses-mailed : BFW\* X / III Logic Analyses-SDIO\_LA.BFW\* X / III Logic Analyses-SDIO\_LA.BFW\* X



			0.5 ms 0.5 ms	9.5 ms 9.5 ms 9.5	ns 0.5ms 0.5ms	9.5 ms 9.5 ms	9.5 ms
200 ns . 💀 . 497ms 🖲			64 84	0.5 ms 0.5 ms 0.5	ns 95ms 85ms	9.5 ms 9.5 ms	9.5 ms
200 ns 309. 499m 9	9.5 ms 9.5 ms 9.5 ms	9.5 ms 9.5 ms 9.5 ms					
0.20.10.002		antere instruction in the instruction of the		nteretereteriteriteriteriteriteri			
	and a main and a second						
CLK-B4							
CMD-B21							
CHD+821	97.34 ns						
SDIO Date0-85							
Data1-86	122.72 ns						
Data2-819				2.28 us			
	<u>──</u>	1					
Date3-820	52 n						
	β2 n						
Data3-820 DDISD3 0							Ĭ
				228us			
Chanel K				2.26 us			
Chanel K				2.26 m		elds Ted ir	ndutes
Channel	In The Parameter of Parameter o	Argument / Data Block 1 (4)	Data Block 2 (h)	2.21 to Data Block 1 (h)	Cata Block 4.00	CRC (h) Fr	nduses [ requency Timing
Channel	ommand Response			Data Block 3 (h)	Data Block 4 (h)		
Color Channell Channe	D(31:0)	10 00 EF FF 65 00 00 0C	00 FE 00 00 00 00 00 00	Data Block 3 (h) 08 00 00 00 00 00 44 00	Data Block 4 (h)	CRC (h) Fr	
Contained Channel Dem (BUSS, SORO(SORO), () Dem (BUSS, SORO(SORO), () Dem (BUSS), BUSS, () Dem (BUSS), () Dem (BUSS), BUSS, () Dem (BUSS), () Dem (BUSS)	D[31:0] D[63:32]	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00	00 FE 00 00 00 00 00 00 00 00 00 00 00 00 00	Data Block 3 (h) 01 00 00 00 00 00 00 00 00 00 00 00 00 00	Data Block 4 (h)	CRC (h) Fr	
Channel 3 Channel 3 Channel 3 Channel 6 Channel 6 Control 110 Control 110 Cont	D[31:0] D[43:33] D[95:64]	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00 00 00 00 00 00	00 FE 00 00 00 00 00 00	Data Block 3 (h) 08 00 00 00 00 00 44 00	Data Block 4 (h)	CRC (h) Fr	
Channel Channe	D[31:0] D[63:32]	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00	00 FE 00 00 00 00 00 00 00 00 00 00 00 00 00	Data Block 3 (h)           01 00 00 00 00 00 00 00 00           01 00 00 00 00 00 00 00 00	Data Block 4 (h) 00 00 00 00 BB SC D8 28 00 00 00 00 00 00 00 00 00 00 00 00 00	CRC (h) Fr	
Channel J Channel J 2007 (1925-1916) (1927-1917) (1927	D(31:0) D(43:32) D(43:32) D(55:64) D(127:96)	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00 00 00 00 00 00	00 FE 00 00 00 00 00 00 00 00 00 00 00 00 00	Data Block 3 (h) 01 00 00 00 00 00 64 00 01 00 00 00 00 00 00 64 00 00 00 00 00 00 00 00 00 00 00 00 00	Data Block 4 (h) 00 00 00 00 08 50 D8 28 00 00 00 00 00 00 00 00 00 00 00 00 00	CRC (h) Fr	
Control Channell Control Contr	mmand Response D(31:0) D(43:32) D(43:32) D(55:42) D(127:82) D(155:128) D(151:160)	10 00 EF FF 65 00 00 0C 00	00         FE         00<	Date Block 3 (b)           01 00 00 00 00 00 00 00 00 00 00 00 00 0	Data Block 4 (h)           00 00 00 00 08 85 CD 8 28           00 00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00	CRC (h) Fr	
Control Channel Channel Control Contro	D[\$1:0]         D[\$1:0]           D[\$4:0]         D[\$5:6]           D[\$5:6]         D[\$7:6]           D[\$5:6]         D[\$157:8]	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00 00 00 00 00 00	00         FE         00<		Data Block 4 (h)           00 00 00 00 BB 5C B2 28           00 00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00	CRC (h) Fr	
Control Channel Channel Control Contro	mmand Response  D[31:0]  D[43:33]  D[45:4]  D[37:40]  D[39:140]  D[39:120]  D	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00 00 00 00 00 00	00         FE         00<		Data Block 4 (h)           00 00 00 00 08 50 20 28           00 00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00	CRC (h) Fr	
Channel	mmand Response  D[31:0]  D[43:33]  D[45:4]  D[37:40]  D[39:140]  D[39:120]  D	10 00 EF FF 65 00 00 0C 00 00 00 00 00 00 00 00 00 00 00 00 00	00         FE         00<		Data Block 4 (h)           00 00 00 00 08 50 20 28           00 00 00 00 00 00 00 00 00           00 00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00 00           00 00 00 00 00 00	CRC (h) Fr	



### Command + Data mode:

Div= 50 ns	3. 499ms 9.5 ms	9.5 ms 9.5 m	ns 9.5 ms	9.5 ms	9.5 ma	9.5 ma	9.5 ms 9.5	ns 9.5 ms	9.5 ms 9.5 ms	9.5 ms 9.5 ms	9.5 ms	9.5 ms
ed: 10:20:18.092												
•												
US_SDIO(1 821,84		CMD53:ID_RV Data:21h	Data:00h Da	ata:01h Data:0	00h CRC:36h	R5:Resp	53 Data:00h Data:00h	Data:10h Data:00h	CRC:2Dh			
SDIO/SD3.0						1						
•												
							10h 00 EFIFFh 65 001 00	0 00 100 FEF 00 00100F 001 001 0	C 00 944 IQ0 90C 00 IQ0 IQ0 98C IC	0 001 001 001 BB 9C D8 281 001 0	100 100 100 100 100 100 100 100 100 100	001301 001001001
CLK-B4												
						000000000						
CMD-B21												
US_SDIO Date0-85												
Data1-B6												
Data2-B19	9											
									122.720ns)			
Data3-B20	0											
SDIO/SD3.0				_		_						
r 07												
1. N												,•
	×											
	x											
Channel	_										1 111 1	
Channel	_						1			iearch All Fields	Text includes	
Channel	ed Report 🚽 🚺 👔									earch All Fields		
Channel	ed Report	BUS_SDIO(1)	BUS_SDIO(1) S	S_SDIO_JS_SDIO(	BUS_SDIO(1) US_SD	BUS_SDIO	BUS_SDIO Aroument / Data Block 1 (b)	BUS_SDIO Data Block 2 (b)	BUS SDIO	Eearch All Fields	BUS SDIO BUS SD	IO BUS_SDI
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument C	CRC (h) Frequency	Timing omma	C BUS_SDIO Response	BUS_SDIO Argument / Data Block 1 (h)	BUS_SDIO Data Block 2 (h)		earch All Fields		IO BUS_SDI
Channel Bus Customize amp (hhmm.ss.ms 10:20:18.112. 10:20:18.112.	ed Report	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency	Timing omma Irc: 18004 Icr: 1	n Response	BUS_SDIO Argument / Data Block 1 (h)	BUS_SDIO Data Block 2 (h)	BUS SDIO	Eearch All Fields	BUS SDIO BUS SD	IO BUS_SD
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	D[31:0]	Argument / Data Block 1 (h)	BUS SDIO Data Block 2 (h) 00 F7 00 00 00 00 00 00	BUS SDIO	Bearch All Fields BUS_SDIO Data Block 4 (h)	BUS SDIO BUS SD	IO BUS_SDI
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	D[31:0] D[63:32]	Argument / Data Block 1 (h)	BU5_SDIC Data Block 2 (h) 00 F7 00 00 00 00 00 00	BUS SDIO	Elearch All Fields BUS_SDIO Data Block 4 (h)	BUS SDIO BUS SD	IO BUS_SD
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	D[31:0] D[63:32] D[95:64]	Argument / Data Block 1 (h)	BUS_SDIO Data Biock 2 (h) 00 F7 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO Data Block 3 (h)	Earch All Fields BUS_SDIO Data Block 4 (h) 0 00 00 00 BB SC DS 28 00 00 00 00 BB SC DS 28 00 00 00 00 00 00 00	BUS SDIO BUS SD	IO BUS_SD
Channel XBax Customize amp (hhmmas.ms 10:20:10.112 10:20:10.112 10:20:10.112 10:20:10.112	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	D[31:0] D[63:32] D[95:64] D[127:96]	Argument / Data Block 1 (h)	BUS_SDIO Data Block 2 (h) 00 F7 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO Data Block 3 (h)	Earch All Fields BUS_SDIO Data Block 4 (h) 00 00 00 00 00 BB SC DS 25 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS SDIO BUS SD	IO BUS_SDI
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	D[31:0] D[63:32] D[95:64] D[127:96] D[159:128]	Argument / Data Block 1 (h)	BUS_SDIO Data Biode 2 (h) 04 87 04 00 00 00 00 00 00 06 00 00 00 00 00 00 00 00 06 00 00 00 00 00 00 00 06 00 00 00 00 00 00 00 06 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO Data Block 3 (h)	Earch All Fields BUS_SDIO Data Blick4 (h) 00 00 00 00 8B sc Ds 28 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS SDIO BUS SD	IO BUS_SD
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	D[31:0] D[63:32] D[95:64] D[127:96]	Argument / Data Block 1 (h)	BUS_SDIO Data Bick 2 (h) 00 F7 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO Data Block 3 (h)	Earch All Fields BUS_SDIO Data Block 4 (h) 00 00 00 00 08 B 4C Ds 28 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS SDIO BUS SD	IO BUS_SDR
amp (hkmmss.ms 10:2016.112 10:2016.112 10:2016.112 10:2016.112 10:2016.112 10:2016.112 10:2016.112 10:2016.112 10:2016.112	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	n Response D[31:0) D[63:32] D[95:64] D[127:96] D[159:128] D[159:128] D[191:160] D[223:192]	Argument / Data Block 1 (h)	BUS_SCHO Data Bio(4.2 (h) 00 F7 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO Data Block 3 (h) 00 00 00 00 00 00 00 00 00 00 00 00 00	Earch All Fields BUS_SDIO Data Block 4 (h) 00 00 00 00 BB SC DS 25 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO BUS_SD CRC (h) Frequen	IO BUS_SDK
Channel	ed Report JUS	BUS_SDIO(1) Response	Argument 0	CRC (h) Frequency 36 197MHz 8	Timing omma Irc: 18004 Icr: 1	n Response D[31:0) D[63:32] D[95:64] D[127:96] D[159:128] D[159:128] D[191:160] D[223:192]	Argument / Data Block 1 (h)	Data Block 2 (h)           00         F7         00	BUS_SDIO           Data Block 3 (h)           02 00 00 00 00 00 00 00 00 00 00 00 00 0	earch All Fields BUS_SDIO Data Block4 (th) 00 00 00 00 88 50 82 50 00 00 00 00 00 00 00 00 00 00 00 00 00	BUS_SDIO BUS_SD CRC (h) Frequen	

SPI mode:





# SDQ

SDQ (Serial Data Quality) interface is an interface standard designed to improve the quality of data transmission, primarily in digital signal processing and communication systems. The SDQ interface is designed to improve data accuracy, reduce miscoding and interference, and ensure signal quality during high-speed data transmission.

### Settings

苎 SDQ Se	ttings				×
Parameter	5		Color		
1					
Channe			CMD		•
SDQ	A0	<b>.</b>	DATA		•
			Reset		•
Model	BQ2024	·	Presence		•
Display	Byte	•	CRC		•
			CRC Error		•
Range					
	ecode Range				
From	То				
Buffer H	lead 👻 Buffer Ta	ail 🔻	ODefault	♦ОК	Cancel

**Channel:** Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Model: Set the IC model number. Currently supports BQ2024, BQ2025,

BQ2026.

**Display:** The result of waveform resolution is displayed in Bit or Byte format.



### Result

e/Div= 20 us		2																-16.302															
uired: 17:39:43.1	138		-10.4		-10.46 #		-10.4	6.5	-10	45.8	- 10	40 5	-10.46	*	-10.461		-10.46 s		-10.46 5		-10.46 #		10.46 s		46 5	-10.4	6	-10.4	6 A	-10.4	M 8	-13.46 s	
• Bit					2	0	1	D	1	1	1	D		0	ŭ	0	ò	0	0	0	0		0	0	0	0	0	0	0	0		D	1
SDQ	SDQ+0		14 10	7.5	a 9 a 71		8.5 m	7 m 8	85 1	85 10	850	u 7 m	16 📾	7 10	3 u 7 us	7 m 8	u 7 w S	3 w 7 m	7 83 8	10 7 tos	7 w	15.5 m	7 us	7 us	7.5 m 8 1	7.5 m	7 10	7 vs	7 m	7 m	15.5 w	7.5 w 1	85 10
er Byte								с	74									00								O	10						A2
spo	3DQ-0						8.5 m		854	85 w					3 <b>u</b> 7 us																		8 u 8.5 us
*	Channel		O Liv	9																													
Here Desk			11.			_	_																			QSea	irch All Fii	nids		Te:	xt includes		EX /
		Cmd(h)								Da	ta(h)								4	SCII													
17:39:40			3	00 01	FD																	_											
17:39:48			7	10 00	00 00 0	0 00 0	66																										
17:39:40			1	10																													
17:39:48			11		01 80 8	8 64 (	C1 24 3	EF 45 0	5									d.ş.E.															
17:39:48			1	B3																													
		78	21				35 31 1	59 30 4	A 46 37	43 30 4	1							23651Y0J	7C8A														
17:39:40				57 00	OB OB O	c											W																
17:39:48	8.977																q																
17:39:48	8.977	72	1	71																													
17:39:48 17:39:48 17:39:48	8.977 8.979 8.979	73	1 5	80 00	C0 00 0	7																											
17:39:48 17:39:48 17:39:48 17:39:48 17:39:49	8.977 8.979 8.979 9.004	73 74	3	80 00	FD																												
17:39:48 17:39:48 17:39:48 17:39:49 17:39:49 17:39:49	8.977 8.979 8.979 9.004 9.005	73 74 75	3 7	80 00 00 01 10 00			66										t																
17:39:48 17:39:48 17:39:48 17:39:49 17:39:49 17:39:49 17:39:49	8.977 8.979 9.979 9.004 9.005 9.007	73 74 75 72	3	80 00 00 01 10 00 71	ED 00 00 (	0 00 0	66																										
17:39:48 17:39:48 17:39:48 17:39:49 17:39:49 17:39:49 17:39:49 17:39:49	8.977 8.979 9.979 9.004 9.005 9.007 9.007	73 74 75 72 73	3 7	80 00 00 01 10 00 71 80 00	ED 00 00 0	0 00 0	66										t																
17:39:48 17:39:48 17:39:48 17:39:49 17:39:49 17:39:49 17:39:49	8.977 8.979 9.004 9.005 9.007 9.007 9.009	73 74 75 72 73 74	3 7	80 00 00 01 10 00 71 80 00 00 01	FD 00 00 0	10 00 1											f q																



## SDR SDRAM

SDRAM (Synchronous Dynamic Random Access Memory) is a synchronous dynamic random access memory. Its characteristic is that it can synchronize the clock pulse of the memory with the host. Because it can only transmit data at the Rising edge, SDRAM can also be called SDR SDRAM (Single Data Rate SDRAM).

SDRAM is different from the DDR SDRAM structure used in current computers. DDR (Double Data Rate) actually refers to DDR SDRAM (Double Data Rate SDRAM), which means that Rising/Falling edge can transmit data.

Due to the large number of channels required and the high signal speed, this decode is only available on LA3000+, LA4000+ or BusFinder models.

In addition, this decode only supports SDR SDRAM analysis, not DDR SDRAM.

Decode Range				
			O A10	Address Data
BA1 A11	A12 A24 🌲	<ul> <li>3 clocks</li> <li>2 clocks</li> </ul>	O Bank Address	SELF
BA0 A10 \$	A11 A23 🜲	Non	O Data	PALL
Bank Address	A10 A22 🌲	#CAS Latency	O Address	MRS
DQM3 A9	A9 A21 🌲	Start Up	Command	CBR_AREF
DQM2 A8	A8 A20 🜲	✓ Parsing include Address and D	ta Decode display in waveform area	ACT PRE
DQM1 A7	A7 A19 \$	DQ7 B0 2 DQ15 B8	DQ23 B16  DQ31 B24  ↓	WRITE /A
	A6 A18 \$	DQ6 A31 CQ14 B7	♦ DQ22 B15 € DQ30 B23 €	READ / A
x4 -	A5 A17 \$	DQ5 A30 DQ13 B6	➡ DQ21 B13 ➡ DQ29 B22 ➡	BST
DQM	A3 A15 -	DQ3 A28 DQ11 B4	➡ DQ19 B12 ➡ DQ27 B20 ➡ ➡ DQ20 B13 ➡ DQ28 B21 ➡	NOP
#RAS A2 \$	A2 A14 \$	DQ2 A27 C DQ10 B3		DESL
#CS A1	A1 A13 🗘	DQ1 A26 C DQ9 B2	♣ DQ17 B10 ♣ DQ25 B18 ♣	
CLK A0	A0 A12 🗘	DQ0 A25 CQ8 B1	DQ16 B9 ↓ DQ24 B17 ↓	
CKE A5	x12 -		x32 💌	
#CAS A3	Address	Data		

### Settings



### Channel: Set the channel number of logic analyzer

Parsing include Address and Data:

When this item is not checked:

Only for simple analysis of SDRAM Command, just connect #CAS, CKE, #CS,

#RAS, the 6 channels of #WE, A10 can be analyzed. In this way, the number of

wiring can be reduced, but because it cannot knowing the status of

Address, Data, etc., is only suitable for primary analysis. Please see Figure

1 below for the analysis results.

When checked:

Including all SDRAM pins for a complete analysis, the analysis results are shown in Figure 2 below

### Startup:

#CAS Latency:

Set the delay time for SDRAM read operation

### Decode display in waveform area

Because there are many states to be displayed by SDRAM, they cannot be displayed all at once in the waveform area.

Therefore, it is necessary to select the item to be viewed in the waveform area. If there are many items to be viewed at the same time, you can add multiple groups of the same SDRAM decoding, then set different decoding and display modes of the waveform area respectively. As shown in Figure 2 below, the left side multiple groups of channels have been added to distinguish the display.



### Result

Uncheck the Parsing include Address and Data option (Figure 1)



### Check the Parsing include Address and Data option (Figure 2)

		<b>*</b>																				
cquired: 18:47:28.049			6.08 ur	0.1 sa	6.12	ur	6.14 km	6.16 ur	6.10 ur		200	6.21 um	6.23 ur	6.26 u	6.2		6.29 ur	6.01 ur	6.33 ur		1.24 ur	6.3
BUS_SDR SDRAM	5 824,820,816,81	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	READ	REA
SOR SORA	#										1											+
BUS_SDR SDRAM(1)	824,820,816,81	Col: 044	Cal.: 0A5	Col: 0A6	Col:0A7	Col:048	Col.:0A9	CoL:DAA	Col.: 0AB	Col: OAC	Col: OAD	Col: OAE	Col: OAF	Col:080	Col: 0B1	Col: 082	Col: 0B3	CoL: 0B4	Col: 0B5	Col:086	Col: 087	08
SDR SDRAI																						
٩	*																					Т
BUS_SDR SDRAM(2)	824,820,816,81	FFFF0SD9	Dets: FFFF05D9	FFFF05D9	Data: FFFF05D9	FFFF05D9	Date: FFFF05D9	FFFRiSD9	Date: FFFF05D9	FFFF05D9	Dets: FFFF05D9	FFFF05D9	Date: FFFF05D9	FFFF05D9	Date: FFFF05D9	FFFF05D9	Dem: FFFF05D9	FFFF03D9	Data: FFFF05D9	FFFF05D9	Date: FFFF05D	99 <b>717</b>
SOR SORA																						1.
SUK SUKA	<u>,                                     </u>																					
BUS_SDR SDRAM(3)	824,820,816,81	BA:0	BA:0	BA:0	BA:0	BA:0	BA:0	BAID	BA:0	BA:0	BA:0	BA:0	BA 0	BA:0	BA:0	BA:0	BA:0	BA:0	BA: 0	BA:0	BA:0	8
BOS_SUR SURVM(3)	824,820,816,81	DN. 0	DA U	DA.U	DA.U	DA.U	DA U	DA U	<b>DN</b> U	DA: U	DA U	DA U	DA U	DA.V	DK.U	DA.U	00.0	DA U	DA.U	- DA. U		1
SOR SORA	4																				<u> </u>	4
	·																					
BUS_SDR SDRAM(4)	B24,B20,B16,B1	A10:0	A10: 0	£10:0	A10:0	A10:0	A10:0	A10:0	A10:0	A10:0	A10:0	#10:0	A10: 0	A10:0	A10:0	A10:0	A10:0	A10:0	A10:0	A10: 0	A10:0	Å1
SOR SORAI																				1		
15, 15	1	C	Live																		<u>,</u>	1
ibel	Channel					-															_	-
3000			10					_		_		_		_	_	_		0				
HLOO BUS_SU	DR SDRAM(4)(SDR S	DRAM) 🛫	C III															QSearch	All Fields 👻 Te	ext includes		]∝,
tamp (hh:mm:s	ss.ms Device		Comm			DR-32b(h)	Row A		Column AD	DR(h)	Bank ADDR		A10	Dat		ASCII		QSearch	All Fields 👻 Te	ext includes		) × .
tamp (hh:mms) 6 18:47:28.04	ss.ms Device	Read	Comm (READ)		000400&3	1	Row Al	0	0A3	DR(h)	Bank ADDR	NO_PRECES	ARGE (0)	FF FF 05 DS				QSearch	All Fields 💌 Te	ext includes		]∝,
amp (hh:mms 6 18:47:28.04 7 18:47:28.04	ss.ms Device 9 SDRAM32B 9 SDRAM32B	Read Read	Comm (READ) (READ)		000400A3 000400A4		Row Al	0	0A3 0A4	DR(h)	Bank ADDR	NO_PRECES	ARGE (0) ARGE (0)	FF FF 05 DS				Q Search	All Fields 💌 Te	ext includes		]∝.
tamp (hh:mms 6 18:47:28.04 7 18:47:28.04 8 18:47:28.04	ss.ms Device 19 SDRAM32B 19 SDRAM32B 19 SDRAM32B	Read Read Read	(READ) (READ) (READ)		000400A3 000400A4 000400A5		Row Al	0 0	0A3 0A4 0A5	DR(h) 0 0	Bank ADDR	NO_PRECES NO_PRECES	ARGE (0) ARGE (0) ARGE (0)	FF FF 05 DE FF FF 05 DE FF FF 05 DE	-			Q Search	All Fields 💌 Te	ext includes		.∝
tamp (hh:mms 6 18:47:28.04 7 18:47:28.04 8 18:47:28.04 9 18:47:28.04	SS.ms         Device           99         SDRAM32B           99         SDRAM32B           99         SDRAM32B           99         SDRAM32B           99         SDRAM32B	Read Read Read Read	Comm (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A5	5	Row Al		083 084 085 086	DR(h) 0 0	Bank ADDR	NO_PRECH NO_PRECH NO_PRECH NO_PRECH	ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 DS FF FF 05 DS FF FF 05 DS FF FF 05 DS				QSearch	All Fields 💌 Te	ext includes		
iamp (hh:mms) 18:47:28.04 19:47:28.04 10:47:28.04 10:47:28.04 10:47:28.04 0 10:47:28.04	SSRMS         Device           19         SDRAM32B           19         SDRAM32B           19         SDRAM32B           19         SDRAM32B           19         SDRAM32B           19         SDRAM32B	Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A6 000400A7		Row A0		083 084 085 086 087	DR(h) 0 0 0 0	Bank ADDR	NO_PRECH NO_PRECH NO_PRECH NO_PRECH NO_PRECH	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 D3 FF FF 05 D3 FF FF 05 D3 FF FF 05 D3 FF FF 05 D3				Q Search	All Fields 💌 Te	ext includes		
tamp (hh:mms 6 18:47:28.04 7 18:47:28.04 8 18:47:28.04 9 18:47:28.04 0 18:47:28.04 1 18:47:28.04 1 18:47:28.04	ss.ms         Device           19         SDRAM32B	Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ)		00040083 00040084 00040085 00040086 00040086 00040087		Row Al		083 084 085 086 087 088	DR(h) 0 0 0 0 0 0	Bank ADDR	NO_PRECHI NO_PRECHI NO_PRECHI NO_PRECHI NO_PRECHI NO_PRECHI	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 D3 FF FF 05 D3				Q Search	All Fields 💌 Te	ext includes		
iamp (hh.mm.) 16 15:47:28.04/ 17 15:47:28.04/ 18 15:47:28.04/ 19 15:47:28.04/ 0 18:47:28.04/ 1 15:47:28.04/ 2 15:47:28.04/ 2	SURAN328         Device           19         SURAN328	Read Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ) (READ)		00040033 00040034 00040035 00040036 00040036 00040036 00040038		Row Al		083 084 085 086 087 088 089	DR(h) 0 0 0 0 0 0 0 0	Bank ADDR	NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 D1 FF FF 05 D1 FF FF 05 D1 FF FF 05 D2 FF FF 05 D1 FF FF 05 D2 FF FF 05 D2 FF FF 05 D2				Q Search	All Fields 💌 Te	ext includes		
amp (h):mms 16:47:28.04 17:18:47:28.04 18:47:28.04 10:19:17:28.04 10:19:17:28.04 10:19:17:28.04 11:19:47:28.04 12:19:47:28.04 13:19:47:28.04 13:19:47:28.04 13:19:47:28.04 14:19:28.04 14:19:28.04 15:1	ss.ms         Device           19         SDRAM32B	Read Read Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A6 000400A7 000400A8 000400A8 000400A9	5 5 7 8	Row At		083 084 085 086 087 088 089 089	DR(h) 0 0 0 0 0 0 0 0	Bank ADDR	NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA NO_PRECHA	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 D FF FF 05 D		· · · · · · · · · · · · · · · · · · ·		Q Search	All Fields 💌 Te	ext includes		
amp (hh:mms) 26 10:47:28.043 27 10:47:28.049 29 10:47:28.049 29 10:47:28.049 10:47:28.049 11:10:47:28.049 12:10:47:28.049 13:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 14:10:47:28.049 15:10:47:100000000000000000000000000000000	ss.ms         Device           19         SDRAM32B	Read Read Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A6 000400A6 000400A6 000400A8 000400A8 000400A8	5 7 8	Row AL		08.3 03.4 08.5 08.6 08.7 08.9 08.9 08.9 08.8 08.8	DR(h) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Bank ADDR	NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF         FF         O5         D5           FF         FF         05         D1           FF         FF         05         D2           FF         FF         05         D1           FF         FF         05         D2           FF         FF         05         D3           FF         FF         05         D3           FF         FF         05         D3           FF         FF         05         D3           FF         FF         05         D3				C Search	All Fields 💌 Te	ext includes		
amp (h):mms 26 18:47:28.043 27 18:47:28.049 29 18:47:28.049 29 18:47:28.049 10:47:28.049 11 18:47:28.049 12 18:47:28.049 13 18:47:28.049 14 18:47:28.049 15 18:47:28.049 19:47:28.049 18:47:28.049 19:47:47:47.049 19:47:47.	SS.ms         Device           19         SDRAH32B	Read Read Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A6 000400A6 000400A8 000400A8 000400A9 000400A8 000400A8		Row A		083 084 085 086 087 088 089 089 088 085 085	DR(h) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Bank ADDR	NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 D5 FF FF 05 D1 FF FF 05 D1 FF FF 05 D5 FF FF 05 D5				C Search	All Fields 👻 Te	ext includes		
amp (hh.mm. 06 10:47:20.04 07 10:47:20.04 09 10:47:20.04 10 10:47:20.04 11 10:47:20.04 12 10:47:20.04 13 10:47:20.04 14 10:47:20.04 15 10:47:20.04 16 10:47:20.04 16 10:47:20.04 17 10:47:20.04 18 10:47:20.04 19 10:47:20.04 10 10:47:47:20.04 10 10:47:20.04 10 10:47:20.04 10 10:47:20.04	SS.ms         Device           19         SDRAM32B           19         SDRAM32B	Read Read Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A5 000400A5 000400A6 000400A8 000400A8 000400A8 000400A8		Row A		083 084 085 086 086 085 088 088 088 088 088 088 088 088	DR(h) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Bank ADDR	NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS NO_PRECESS	ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0) ARGE (0)	FF FF 05 D FF FF 05 D				C Search	All Fields 💌 Te	ext includes [		
2010 2010 2010 2010 2010 2010 2010 2010	SS.ms         Device           19         SDRAM32B	Read Read Read Read Read Read Read Read	Comm (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ) (READ)		000400A3 000400A4 000400A5 000400A6 000400A6 000400A8 000400A8 000400A9 000400A8 000400A8	8 5 7 8 8 7 9 8 7 9 8 7 9 8 7 9 8 7 9 8 7 9 8 9 8	Row A		083 084 085 086 087 088 089 089 088 085 085	DR(h) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Bank ADDR	NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED NO_PRECED	ABGE (0) ABGE (0)	FF FF 05 D5 FF FF 05 D1 FF FF 05 D1 FF FF 05 D5 FF FF 05 D5				C Search	All Fields 💌 Te	ext includes		



# SENT

The SENT (Single Edge Nibble Transmission) protocol is a communication protocol used in the field of automotive electronics, especially for data transmission between sensors and control units (ECUs) in the vehicle's internal electronic system. The SENT protocol is widely used in high-performance in-vehicle sensors such as wheel speedometers, position sensors, etc. It enables efficient data transfer with limited bandwidth and guarantees high-precision data transfer.

### Settings

🛤 SENT Settings					×
Channel			Color		
Configuration C SENT Data A		<b>*</b>	Sync Width		•
Range			S/C		•
			ID		•
Decode Range			CRC		•
From	То		Data		•
Buffer Head 🔹	Buffer Tail	•	Pause		•
Startup					
Clock Tick	3 us	▼ To	olerance	20%	•
# of Nibbles	6	▼ P	olarity	Idle High	•
SENT Version	2010/2016	▼ P	ause	OFF	•
Message	Fast Channel	• C	RC	Recommended	•
			ODefault	✓OK XCan	cel

**Channel:** Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.



**Startup:** Sets the startup setting for SENT before analysis.

### Result





# Serial Flash

Serial flash (SPI Flash) 25, 35, etc. series use SPI/QPI/OPI protocol as their data transfer communication method. Serial flash bus analysis provides users with the ability to view commands and input/output bus messages at the same time when viewing signals, saving users the time of analyzing waveforms using the SPI bus.

### Settings

🗯 Seria	I Flash (25 Series) S	Settings							×
Settings									
	CS#	CH 0	÷	SCLK	CH 1	-	Manufacture		
	SI/SIO0	CH 2	\$	SO/SIO1	CH 3	-	ESMT(EON	) 🔻	
	WP#/SIO2	CH 4	-	Hold#/SIO3	CH 5	-	Device EN25Q32A	(B)	
	SIO4	CH 6	\$	SIO5	CH 7	-	EN25F32 EN25Q16		
	SIO6	CH 8	\$	SIO7	CH 9	\$	EN25F16 EN25S80		
	DQS	CH 10	\$				EN25Q80A EN25F80A EN25QH25 EN25QH25	56	
The flas	sh Startup mode			Decode option	1		EN25F05 EN25(L)F1	0	
Sta	artup in QPI mode			Decode S	SI Only		EN25S10		-
Sta	artup in 4-Byte ADD	OR. mode		Decode S	Single Mode	Only	tSHSL>= 10 n	s	
Sta	artup in PEM mode	è		When Comma			tCLQV >= 6.25	ins	
🗌 Du	immy Cycles	2 Clk 📼		Decode S		ecode SO	10247 0.20		
Wr	ap Around	8 B 👻		Reduced R	Report				
	E bit set			Always in F					
	artup in Octal mod			STR	0				
	○ STR ● D1 curity Field	IR			Read Status				
00	curity r reru			Read data	on the risin	g edge of C	LK		
Range	Decode Rang	e							
<b>20</b>	From			То					
<b>i</b> i	Buffer Head	Ŧ		Buffer Tail	Ŧ				
[	Default						<b>√</b> 0K		×Cancel

**CS#:** Chip Select of transfer signal.

**SCLK:** Clock of transfer signal.

**SIO0-SIO7:** Data pin of transfer signal.



**Manufacturer:** The main purpose of this function is to select the correct Flash model, tCLQV and tSHSL for command parsing. If no exact model is found, the user can also select a model that is compatible with the command format.

The Flash Startup Mode: Since the Serial Flash can switch the operation mode with commands, the Logic Analyzer does not know the current operation mode of the actual Serial Flash when it captures the waveforms. Therefore, the user should be informed if necessary. When the user selects a Flash model that does not support mode switching, the relevant option will be disabled and cannot be set.

**QPI Mode:** Refers to Quad Peripheral Interface Mode or Quad SPI Mode.

**4-Byte Mode:** Refers to the 4-Byte Address Mode.

**PEM Mode:** Refers to the Performance Enhancement Mode.

**Dummy Cycles:** Some Read instructions wait for Dummy cycles, and the number of cycles they wait for can be preset.

Wrap Around: The value of Wrap around can be preset.

**QE bit:** QE bit in the status register, which can be used for QPI mode enable/disable control.

Startup in Octal Mode: Refers to the OPI mode.

**Security Field:** We provide Flash with AES encryption and decryption function, please contact us if user need to use it.

**Decode SI Only:** When checked, the program will use Single mode to analyze the waveforms in 3-line mode. These 3 lines are CS# / SCLK / SI.

**Decode Single Mode Only:** When this option is selected, the program will use Single mode to analyze the waveform in 4-line mode. These 4 lines are CS / Clock / SI / SO. In this case, the program will ignore the command to switch to



multi-line mode. If unchecked, the program will analyze the waveform in 4-wire or 6-wire mode according to the selected Flash model.

When Command Unknown: Decoded for SO or SI only.

**Always in PEM Mode:** When checked, the analyzer will maintain the PEM mode regardless of the command setting, and you can choose to maintain in STR or DTR mode.

**Reduce Read Status(05h):** When checked, the Read Status (05h) command that repeats the unchanged data will be combined into a single command when generating an analysis report, and the number of repetitions will be displayed, thus reducing the number of reports and making it easier to view.

As you can see from the example below, the Read status data = 01 is repeated 1817 times.

(01)Write Status Register	00	02	 ×1
(05)Read Status Register-1	01		Repeat: CMD 1817 Times, DAT
(05)Read Status Register-1	00		
(35)Read Status Register-2	02		×1
(06)Write Enable			<b>v</b> 1

**Read data on the rising edge of CLK:** For SDR Read Data mode, if the Clock signal Duty is not stable enough and the Latch Data out cannot be correct after setting tCLQV value, the Latch bit can be set to Next rising edge.

Result

Using SPI Mode Serial Flash Decoding Situation



lime Div = 500 ns	-38.87 us -38.16 u		35.44 us	-34.73 us		-34.01 u	\$	-33.3	t us	-32	.69 us		-31.87 us -31.16	8 us -30.46 us	-29.73 us
		(03)READ	Addr:00	Addr.01 Av	ddr:8F	DO:DO		):00	DO:00	D0		DO:00	DO:00		
	CS≇-A0					4									
MXIC-1606E	SCLK-A1														
	SI00 - A2	145 ns	880 n		220 n						) us				
Serial Flash	ISIO1 - A3		880 n	s											<b>(</b> )
Label	Channel														•
													Search All Fie		^
Sample	Command (h)	Addr	ess(h)	PEM(h)	DO	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information	
		Contraction and			00	0.0									
41.8400000	(03)normal read	00018B			00	00	00		00	00		_			
41.8400000 36.0650000	(03)normal read (90)read electronic manufacturer & d.	00018B				00			00	00					
41.8400000 36.0650000 18.0150000		00018B			00	00	00		00	00					
-41.8400000 -36.0650000 -18.0150000 -12.6000000	(90)read electronic manufacturer & d.	00018B 00018F			00	00 00	00 0B		00	00					
-41.8400000 -36.0650000 -18.0150000 -12.6000000 -8.44000000 -2.12500000	(90)read electronic manufacturer & d. (9F)read identification	00018B 00018F			00 00 40	00 00 20	00 0B 10	00		00			····· 0 .		

			13.08 ms	33.09 ms	33.1 ms	33.11 ms		33.12 ms		33.13 ms		33.14 ms	3	13.15 ms 33.16	ms 33.17 m	33.18
		(6B)FRQO	Addr:00	Addr:00	Addr:00	DMY:00				(6B)FR	100	Addr:00	Addr:0	10 Addr.20	DMY:00	
c	:S#-A19															
s	CLK-A18								2 u							
▲ Winbond-SFI: S	100 - A20	2 u 2 u						u 2iu 3		s2 u				13.01		4 us
8	IO1 - A21						6 us	2 u					45.51 us			3 us
s	102 - A22						6 us	2 u					40.51 us	6	3 jus	2 u 2 u
S Serial Flash	103 - A23						16.57	7 us						55.51 us		(
									10							a a
ıı, ıı,	Chennel															
Label C	Channel	4												Q Search All Fie	Id 🔽	
abel C		<u>"</u>	aead (h)		Åddress(h)	PEM(h)	D0	D1	D2	D3	D4	D5 D	5 D7	Search All Fie ASCII (D0-D7)	ild 🔽	
abel C CH-00 Bus Timestamp	llin E	<u>"</u>		*	Address(h) 000000	PEM(h)	D0 41	D1 43	1.50		D4 45 2		5 D7			
Label C CH-00 Bus Timestamp 33.067080000ms	(6B) Quad	L. Comm	st Read			PEM(h)		1	55	54		0 53		ASCII(D0-D7)		
Label C CH-00 Bus ( Timestamp 33.067080000ms 33.124580000ms	(6B) Quad	Comm Comm	st Read st Read	READ	000000	PEM(h)	41	43	55 61	54 64	45 2	0 53 0 72	50	ASCII(D0-D7) ACUTE SP		
CH-00         CH-00 <th< td=""><td>(6B) Quad (6B) Quad (EB) Quad</td><td>Comm Comm 1 Output Fas</td><td>st Read st Read utput FASI</td><td></td><td>000000</td><td></td><td>41 51</td><td>43 75</td><td>55 61 55</td><td>54 64 54</td><td>45 2 20 5</td><td>0 53 0 72 0 53</td><td>50 6F</td><td>ASCII(D0-D7) ACUTE SP Quad Pro</td><td></td><td></td></th<>	(6B) Quad (6B) Quad (EB) Quad	Comm Comm 1 Output Fas	st Read st Read utput FASI		000000		41 51	43 75	55 61 55	54 64 54	45 2 20 5	0 53 0 72 0 53	50 6F	ASCII(D0-D7) ACUTE SP Quad Pro		
Label CC CH-00 DBus C Timestamp 33.067080000ms 33.124580000ms 33.182080000ms 33.219580000ms	(6B) Quad (6B) Quad (6B) Quad (EB) Quad	Comm Comm Contput Fai Contput Fai Contput Fai Contput / Or	st Read st Read atput FASI atput FASI	READ	000000 000020 000000	00(reset)	41 51 41	43 75 43	55 61 55 61	54 64 54	45 2 20 5 45 2	0 53 0 72 0 53	50 6F 50	ASCH(D0-D7) ACUTE SP Quad Pro ACUTE SP		
Label C CH-00 CH201 DBus	(6B) Quad (6B) Quad (EB) Quad (EB) Quad (EB) Quad	Comm i Output Fas i Output Fas i Input / Oi i Input / Oi	st Read st Read atput FASI atput FASI	READ	000000 000020 000000 000020	00 (reset) 00 (reset)	41 51 41 51	43 75 43 75	55 61 55 61 55	54 64 54 64	45 2 20 5 45 2	0 53 0 72 0 53	50 6F 50	ASCH(D0-D7) ACUTE SP Quad Pro ACUTE SP Quad Pro Quad Pro		

Using QPI Mode Serial Flash Decoding Scenario

Serial Flash data Comparison : Compare the Serial Flash data by the

waveform files.

**Method:** Create a file by text editor and save it as SFCmp.cfg in order to

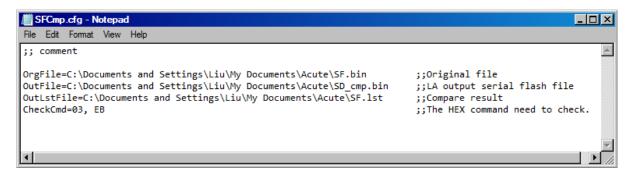
compare with the real Serial Flash waveform to find the bug, the default path is

"My Documents\Acute"



🕌 Acute	_ 🗆 🗵
G Documents Acute	<b>2</b>
🕘 Organize 🔻 🔜 Views 👻	(?)
Name 🔺 🔹 Date modified 💌 Type 💌 Size 💌 Tags 💌	
SFCmp.cfg	
1 item	

SFCmp.cfg information:



**OrgFile=File\_Path:** Key in the file path of the original Serial Flash data file

(.bin).

**OutFile=File\_Path:** Key in the file path of the Serial Flash output file.

OutLstFile=File\_Path: Key in the file path of the comparison result. The file

name will has extension ".lst".

CheckCmd=Serial Flash command: Key in the command in Hex that are

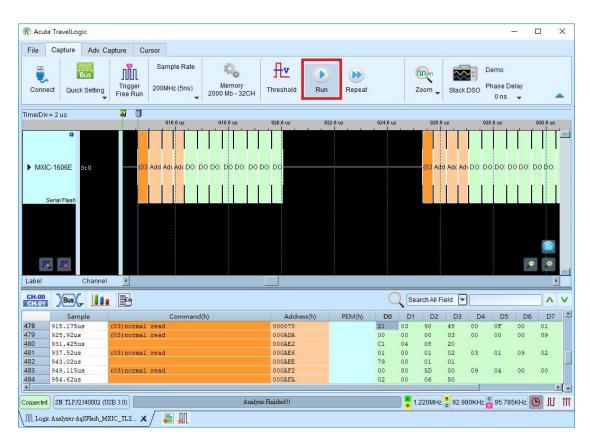
separated by commas.

Save the OrgFile to the OrgFile file path.



🕌 Acute	
G Documents Acute	
🕘 Organize 🔻 🔜 Views 👻	•
Name 🔺 🔹 Date modified 💌 Type 💌 Size 💌 Tags 💌	
SF.bin SFCmp.cfg	
2 items	

Run the Serial Flash Bus Decode to capture the Serial Flash signal.



If the OutFile does not exit, it will copy the OrgFile to the OutFile and write the data to it according to the CheckCmd.



### Compare result:

Acute	_ 🗆 ×
Search	2
Organize 🔻 📷 Views 🔻	0
Name 🔺 🕨 Date modified 🔽 Type 🗣 Size 👻 Tags 👻	
SF.bin SF.Ist SF_cmp.bin SFCmp.cfg	
4 items	

The OutLstFile:

SF.Ist - Notepad	- O ×
File Edit Format View Help	
OrgFile=C:\Documents and Settings\Liu\My Documents\Acute\2Mbit_origin.bin OutFile=C:\Documents and Settings\Liu\My Documents\Acute\2Mbit_origin_cmp.b:	in
00001321 00001399: E2 E0	
00001321 000013A1: 52 50	
0000143C 00001461: 73 71 0000143C 0000148F: D3 D1	
0000143C 00001499: C3 C1	
0000143C 000014BB: E3 E1	
000014D5 000014DB: F3 F1	
0000159C 000015C8: F3 F1 0000159C 000015E2: 32 30	
0000159C 000015E6: 42 40	
<u> </u>	

The first column is the compared address from OrgFile, the second column is

the different address from OutFile.



## Serial PSRAM

Serial PSRAM is a special form of PSRAM (Pseudostatic RAM) that uses a serial interface to communicate with a microprocessor or other system.PSRAM is a type of memory that is intermediate between Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). It has the advantages of high density of DRAM, but similar to SRAM, it offers relatively simple operation and simplifies memory control to some extent.

### Settings

苎 Serial PSRAM	1 Settings			×
Parameter				Color
:				
Channel				CMD 🗸
Bus Width	8		-	Address 🗸
CS	A0 🌲	DQS1	A2 🌲	Data 🗨
CLK	A1 🗘	DQS2	A19 🌲	Range
D0	A3 🌲	D8	A11 🌲	Decode Range
D1	A4 🌲	D9	A12	From To
D2	A5 🌲	D10	A13 🌲	Buffer Head
D3	A6 🗘	D11	A14	
D4	A7 🌲	D12	A15 🌲	
D5	A8 🌲	D13	A16 🌲	
D6	A9 🗘	D14	A17 🌲	
D7	A10 🗘	D15	A18 🌲	
Latch Edge	SDR	•		
DQS Delay	0	🌲 Sa	ample Points	
Latency	Settin	igs		
				ODefault



Bus Width: Set the width of the bus to 8 or 16.

Latch Edge: Choose using SDR or DDR to latch data.

**DQS Delay:** Set the DQS delay time in units of sampling points.

**Latency:** Details Specifies the amount of time that a particular piece of data will be delayed.

# 

### Result



# Serial IRQ

Serial IRQ/Data is a communication protocol composed of two lines, PCI-Clock and IRQSER, used to transmit interrupt status. An IRQSER cycle essentially consists of three parts: Start, IRQ/Data, and Stop Frame. The operating modes are divided into Continuous mode and Quiet mode. In Continuous mode, the source of the Start Frame is not restricted, but in Quiet mode, only the Host can generate the Start Frame signal.

### Settings

Serialized IRQ Setting	×
Channel	Color
CLOCK A0 Repeat format Advance Show Repeat Frame	Start Frame Stop Frame Assert Frame Dessert Frame
Range	
From       To         Buffer Head       Buffer Tail	✓OK XCancel

### CLOCK: PCI Clock channel

**IRQSER;** IRQSER channel

Normal: Not show repeat frame

High Active: Enables the user to adjust the numeric judgment conditions.



Enabled when checked.

### Hide Repeat Frame (default)

CH-00 CH-01		(Serialized IRC	a) 🗸 😋 🚺 🚺																			
	Timestamp	No	Mode	0 1	SMI	3	4	5 6	7	8	9	10	11	12	13	14	15	IOCHCK	INTA	INTB	INTC	INTD
1	-47.535us	1		A										Α								
2	259.155us	137	Continue mode	A				A						A								
3	313.28us	161	Continue mode	A										Α								
4	532.03us	258	Continue mode	A				A						A								
5	550.075us	266	Continue mode	A										A								
6	1.14091ms	528	Continue mode	A				A						A								
7	1.195035ms	552	Continue mode	A										Α								
8	1.416035ms	650	Continue mode	A				A						A								
9	1.429575ms	656	Continue mode	A										A								
10	2.01815ms	917	Continue mode	A				A						A								
11	2.07003ms	940	Continue mode	A										Α								
12	2.28878ms	1037	Continue mode	A				A						A								
13	2.304555ms	1044	Continue mode	A										A								
14	2.895395ms	1306	Continue mode	A				A						A								
15	2.94953ms	1330	Continue mode	A										Α								
16	3.170535ms	1428	Continue mode	A				A						Α								
17	3.184055ms	1434	Continue mode	A										A								
18	3.774895ms	1696	Continue mode	A				A						Α								
19	3.82903ms	1720	Continue mode	A										A								
20	4.050035ms	1818	Continue mode	A				A						Α								
21	4.06355ms	1824	Continue mode	A										A								
22	4.654395ms	2086	Continue mode	A				A						Α								
23	4.704025ms	2108	Continue mode	A										A								
24	4.92277ms	2205	Continue mode	A				A						Α								
25	4.93854ms	2212	Continue mode	A										A								
26	5.52939ms	2474	Continue mode	A				A						A								

### Show repeat frame

CH-00 CH-01		erialized IRQ)	. C 📗 🗄																			
	Timestamp	No	Mode	0 1	SMI	3	4	5 6	7	8	9	10	11 1	12	13	14	15	IOCHCK	INTA	INTB	INTC	INTD
1	-47.535us	° 1		A									A									
2	-45.275us	2	Continue mode	A									A									
3	-43.02us	3	Continue mode	A									A									
4	-40.76us	4	Continue mode	A									A									
5	-38.51us	5	Continue mode	A									A									
6	-36.255us	6	Continue mode	A									A									
7	-34.005us	7	Continue mode	A									A									
8	-31.755us	8	Continue mode	A									A									
9	-29.505us	9	Continue mode	A									A									
10	-27.25us	10	Continue mode	A									A									
11	-24.995us	11	Continue mode	A									A									
12	-22.74us	12	Continue mode	A									A									
13	-20.48us	13	Continue mode	A									A									
14	-18.22us	14	Continue mode	A									A									
15	-15.96us	15	Continue mode	A									A									
16	-13.7us	16	Continue mode	A									A									
17	-11.445us	17	Continue mode	A									A									
18	-9.19us	18	Continue mode	A									A									
19	-6.935us	19	Continue mode	A									A									
20	-4.685us	20	Continue mode	A									A									
21	-2.43us	21	Continue mode	A									A									
22	-180ns	* 22	Continue mode	A									A									
23	2.07us	23	Continue mode	A									A									
24	4.325us	24	Continue mode	A									A									
25	6.58us	25	Continue mode	A									A									
26	8.835us	26	Continue mode	A									A									



Advance: Spread all IRQ/Data in a frame on different lines.

CH-00 CH-01	Bus SERIRQ(Ser	rialized IRQ) 🚽 😋 📗		
	Timestamp	IRQ/Data Frame	Signal Sampled	# of clocks past Start
1	-47.38us	1	IRQ0	2
2	-47.29us	2	IRQ1	5
3	-47.2us	3	SMI#	8
4	-47.11us	4	IRQ3	11
5	-47.02us	5	IRQ4	14
6	-46.93us	6	IRQ5	17
7	-46.84us	7	IRQ6	20
8	-46.75us	8	IRQ7	23
9	-46.66us	9	IRQ8	26
10	-46.57us	10	IRQ9	29
11	-46.48us	11	IRQ10	32
12	-46.39us	12	IRQ11	35
13	-46.3us	13	IRQ12	38
14	-46.21us	14	IRQ13	41
15	-46 12110	15	TPO14	44



### Result

Normal mode (Hide Repeat Frame)

NDir=100 ns	<b>₽</b> -14	4.2ns→7	14.07 md	14.37 ma	14.37 ms	14.37 m	is 14.37 ms	14.37	ms 14	.07 ma	14.37 ms	14.37 ms	14.37 ms	14.37 ms	14.37 m	d 14.%	7 864	14.37 ms	14.37 ms
0	-						· · · · · · · · · · · · · · · · · · ·	· · · · · · · ·					1					· · · · ·	· · · · · · · · · · · · · · · · · · ·
	Stor	Start		IRQ0	IRQ1-A	SMI#	IRQ3	IRQ4	IRQ5	IRQ6-A	IRQ7	IRQS	IRQ9	IRQ18	IRQ11	IRQ12-A	IRQ13	IRQ14	IRQ15 D
SERIRO A2 CI	38-42																		
	JL																		
43.77	R0-A3				30 ns					25.10						25 m			
Serialzed IRD																			
<b>15 1</b>		OLive																	ې فر
iel Char	nnel I																		
Bus SER	IRQ(Serialized)	IRQ) 🗸 😋 🚺 👔	54 Þ													Q Sear	ch All Fields	Text includes	EX.
Timestamp		Mode	0 1	SMI 3	4 5 6	7 8	9 10 11 12	13 14	15 IOCHCK	INITA	INTE INTC	INTO							
-47.535us	1 1		à	3111 3	4 5 6		à 10 11 11	10 14	15 TOTOTON										
259.155us	137	Continue mode	λ		A		λ												
313.28us	161	Continue mode	à																
532.03us	258						Å												
		Continue mode	à		A		Å												
550.075us	266	Continue mode	À				λ λ												
1.14091ms	266 528	Continue mode Continue mode	A A A		A A		A A A												
1.14091ms 1.195035ms	266 528 552	Continue mode Continue mode Continue mode	À		A		2 2 2 2 2 2 2 2												
1.14091ms	266 528 552 650	Continue mode Continue mode	A A A A				2 2 2 2 2 2 2 2												
1.14091ms 1.195035mp 1.416035ms 1.429575ms 2.01815ms	266 528 552 650 656 917	Continue mode Continue mode Continue mode Continue mode	2 2 2 2		A		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.195035ms 1.416035ms 1.429575ms 2.01015ms 2.07003ms	266 528 552 650 656 917 940	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.195035ms 1.416035ms 1.429575ms 2.01015ms 2.07003ms 2.28078ms	266 528 552 650 656 917 940 1037	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		A A		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.195035ms 1.416035ms 1.429575ms 2.01015ms 2.07003ms 2.28075ms 2.304555ms	266 528 552 650 656 917 940 1037 1044	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode	***		а А А А		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.195035ms 1.416035ms 1.429575ms 2.01015ms 2.07003ms 2.20877ms 2.304555ms 2.304555ms	266 528 552 650 656 917 940 1037 1044 1306	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.195035ms 1.416035ms 1.429575ms 2.01015ms 2.07003ms 2.28075ms 2.304555ms 2.995395ms 2.94953ms	266 528 552 650 656 917 940 1037 1044 1306 1330	Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2 2		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.49503ms 1.416035ms 1.425575ms 2.01015ms 2.020703ms 2.0207ms 2.095395ms 2.94953ms 3.170535ms	266 528 552 650 656 917 940 1037 1044 1306 1330 1428	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		а А А А		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2												
1.14091ms 1.495035ms 1.429575ms 2.010135ms 2.010135ms 2.010135ms 2.00703ms 2.00755ms 2.995395ms 3.04555ms 3.170535ms 3.170535ms 3.77455ms	266 528 552 650 656 917 540 1037 1044 1306 1330 1428 1434 1696	Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2 2		۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵												
1.14091ms 1.495035ms 1.425575ms 2.01015ms 2.00155ms 2.304555ms 2.94953ms 3.126055ms 3.126055ms 3.126055ms 3.126055ms 3.2203ms	266 528 552 650 656 917 940 1037 1044 1306 1330 1428 1434 1434 1434 1696 1720	Costinue mode Continue mode	* * * * * * * * * * *		2 2 2 2 2 2 2 2		۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵												
1.14091ms 1.195035ms 1.426035ms 1.425575ms 2.01035ms 2.00030ms 2.28071ms 2.38055ms 2.95355ms 2.94555ms 3.194555ms 3.774595ms 3.774595ms 3.22903ms	266 528 552 650 656 917 940 1037 1044 1306 1330 1439 1434 1494 1720 1018	Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2 2 2 2 2		۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵												
1.14051ms 1.195035ms 1.426535ms 1.425575ms 2.01015ms 2.007003ms 2.20071ms 2.304555ms 2.953595ms 2.953595ms 3.10555ms 3.120555ms 3.24953ms 3.24953ms 4.05055ms 3.2555ms 4.060035ms 4.06505ms 4.065055ms 4.06505ms 4	246 528 552 650 656 917 540 1037 1044 1306 1330 1428 1434 1496 1720 1018 1824	Continue mode Continue mode	, , , , , , , , , , , , , , , , , , ,		2 2 2 2 2 2 2 2		۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵												
1.14051ms 1.416035ms 1.416035ms 1.425575ms 2.01035ms 2.207003ms 2.207077ms 2.20707ms 2.209535ms 3.10055ms 3.10055ms 3.10055ms 3.2903ms 3.2203ms	266 528 552 650 656 917 940 1037 1044 1306 1330 1439 1434 1494 1720 1018	Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2 2 2 2 2 2		۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵۵												

Normal mode(Show repeat frame)

Div=100 ns		14.2ns	14.22 ma 14	.37 ma	14.37 ma	14.37 ma	14.57 ma	14.37 mi	14.37 ma	54.37 ma	14.37 ma	14.37 ma	14.37 ma	14.37 ma	14.37 ma	14.37 m	a 14.37 ma	14.37 ma
0			-	1 1		· · · · · · ·		· · · · · · · · ·	1	r	r	1	r • • • • • •			· · · · ·	· · · · ·	· · · · · · · · ·
		Sho;	Shot		IRQ0	IRQ1-A	SMI# IR	IRQ4	IRQ5	IRQ6-A	IRQ7	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12-A	IRQ13	IRQ14 IRQ15
				i Ta Ta	a de la seconda de													
IRIRQ A	42 CLE-A2																	
	N3 IRQ-A3					30 ns				25 na						25 nz		
Seraized IRQ																		
<b>K N</b>		$\bigcirc$	Live															
		$\overline{\mathbf{O}}$																<i>a</i> -
c	Channel	•																
Lacar.		_		<b>b</b>														
Bus s	SERIRQ(Seria	lized IRQ)	C 🛄 🖻													Q Search	All Fields 🔻 Text in	ncludes e
	estamp	No.	Mode	0 1	SMI	3 4 5 6	5 7 8 9	10 11 12	13 14 15 IC	CHCK INTA	INTB IN	TC INTD						
-47.535				A				A										
-45.275			Continue mode Continue mode	A				A										
-40.76u																		
-38.51u			Continue mode	Â				A										
			Continue mode Continue mode	Å				A A										
-36.255	15 5 5119 6			A A A				A A A										
-34.005	25 5 5128 6 5128 7		Continue mode Continue mode Continue mode	A A A				A A A										
-34.005	as 5 Sus 6 Sus 7 Sus 8		Continue mode Continue mode Continue mode Continue mode	2 2 2 2 2 2 2				А А А А										
-34.005 -31.755 -29.505	25 5 5us 6 5us 7 5us 8 5us 8 5us 9		Continue mode Continue mode Continue mode Continue mode Continue mode	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2				А А А А А										
-34.005 -31.755 -29.505 -27.25u	25 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	0	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode					А А А А А А										
-34.005 -31.755 -29.505 -27.25u -24.995	25 5 50.8 6 50.8 7 50.8 8 50.8 9 8 50.8 9 8 28 1 50.5 1	0	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode					А А А А А А										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u	25         5           5028         6           5028         7           5028         7           5028         8           5028         10           5028         11           5028         12           28         12           29         12	0	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode					А А А А А А А										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.48u	25 5 508 6 508 7 505 8 508 % 9 28 1 505 1 29 1 28 1 29 1	0 1 2 3	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode															
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.48u -10.22u	15         15           5118         6           5118         7           5118         7           5118         7           5118         7           5118         7           5118         7           5118         7           5118         7           5118         7           5118         11           5118         11           12         12           13         12           14         12	0 1 2 3 4	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode					2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.48u -10.22u -15.96u	25         5           5128         6           5128         7           5128         7           5128         7           5128         8           5128         19           28         11           28         12           28         12           28         12           28         12           29         12	0 1 2 3 4 5	Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode Continue mode					) 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.46u -10.22u -15.94u -13.7us	15         15           5128         6           5128         7           5128         7           5128         7           5128         10           528         11           5128         12           128         12           139         12           149         12           15         12           16         12           17         12           18         12           19         12	0 1 2 3 4 5 6	Continue mode Continue mode					2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.48u -18.22u -15.94u -13.7us -11.445	25         5           5128         6           5128         7           5128         8           5128         9           28         11           28         12           28         12           28         12           28         12           29         12           29         12           5         12           5         12           5         12           5         12	0 1 2 3 4 5 6 7	Continue mode Continue mode	*******				2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.250 -24.995 -22.740 -20.480 -18.220 -15.960 -13.708 -11.495 -9.1908	25         5           51.8         6           51.8         7           51.8         7           51.8         7           51.8         7           51.8         7           52.8         10           50.8         11           50.8         12           28         12           28         12           29         12           5         12           5         12           5         12           5         12           5         12	0 1 2 3 4 5 6 7 8	Continue mode Continue mode	* * * * * * * * * * * * * * * * * * * *				2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.45u -15.94u -15.94u -13.7us -11.445 -5.15us -6.935u	25         5           5128         6           5128         7           5128         8           5128         8           28         11           5128         12           28         12           29         12           29         12           29         12           29         12           29         12           20         12           20         12           20         12	0 1 2 3 4 5 6 7 9 9	Continue mode Continue mode	*******				2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.40u -15.94u -15.94u -13.7us -11.445 -9.19u3 -6.953u -4.655u	25         5           Sus         6           Sus         7           Sus         8           Sus         1	0 1 2 3 4 5 6 7 8 9 9 0	Continue mode Continue mode	* * * * * * * * * * * * * * * * * * * *				) 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.955 -22.74u -20.45u -10.22u -15.94u -13.7us -11.445 -9.19us -4.635u -4.635u -2.43us	25         25         5           Stas         6         7           Stas         7         5           Stas         7         5           Stas         10         8           As         11         12           As         12         12           As         2         12	0 1 2 3 4 5 6 6 7 8 9 9 0	Continue mode Continue mode	* * 2 * * * * * * * * * * * * * * * * *				) 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										
-34.005 -31.755 -29.505 -27.25u -24.995 -22.74u -20.46u -10.22u -15.94u -13.7us -11.445 -9.19u3 -6.955u -4.655u	25         S           Sus         6           Sus         7           Sus         7           Sus         10           Sus         11           Sus         12           Las         12           Las         12           Sus         12      S	0 1 2 3 4 5 6 7 9 0 1 2	Continue mode Continue mode	***************************************				) 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2										

## Advance mode

e/Div= 100 ns		2-14.2ns-	14.37 ma 1	37 ma 1	32 ma	14.37 ma	14.37 ma	14.27 mi	14.27 ma	14.37 ma	14.37 ma	14.37 ma	14.37 ma	14.27 ma	14.37 m	r 14	37 ma	14.37 ma	14.37 ma
0		510	Stat	IRQ	IRQ1-J	SMI#	IR	QJ IRQ4	IRQ5	IRQ6-A	IRQ7	IRQ8	IRQ9	IRQ10	IRQ11	IRQ12-A	IRQ13	IRQ14	IRQ15
IERIRQ	A2 CLK-A2	ΠΠΓ			İ			<b>T</b> AİSTR											
			нппп																
Serialized IRQ	A3 IRQ-A3				30 ns					25 nd						25 na			
PK 11			Live																<u>ب</u>
el	Channel	*		- C			-												
00 3/5-3/	r	informed attracts	C 🛄 🖻	b.												O Search	All Elabor	Text includes	EX
Bus	E SEMINCI(Ser	sanzed incu) +	C III E													C Dearch		- International and a	
T	Timestamp		ita Frame	Signal Sampled		t of clocks past St	art									C Dealer		- Inter includes	
-47.	Timestamp . 38us		ita Frame IRQO	Signal Sampled	2	f of clocks past St	art									C Council		- HEALINGUISES	
-47. -47.	Timestamp . 38us . 29us		ta Frame IRQC IRQI	Signal Sampled	2 5 8	f of clocks past St	art									C CONTRACT			
-47. -47. -47.	Timestamp . 38us		ita Frame IRQO	Signal Sampled	2 5 8 11	t of clocks past St	art									C Dialo		- Jew monores	
-47. -47. -47. -47. -47. -47.	Timestamp .38us .29us .2us .11us .02us		ta Frame IRQC IRQI SHI IRQC IRQC	Signal Sampled	2 5 0 11 14	t of clocks past St	art									C UNION		- Jew monores	
-47. -47. -47. -47. -47. -47. -46.	Timestamp .38us .29us .2us .11us .02us .93us		IRQU IRQU IRQU IRQU IRQU IRQU IRQU IRQU	Signal Sampled	2 8 11 14 17	F of clocks past St	art									C. Uvarda			
-47. -47. -47. -47. -47. -47. -46. -46.	Timestamp .38us .29us .2us .11us .02us .93us .84us		ta Frame IROC IRQ1 SMI4 IROS IRQ4 IRQ2 IRQ2 IRQ2	Signal Sampled	2 5 0 11 14 17 20	t of clocks past St	art									C Utato			
T -47. -47. -47. -47. -47. -46. -46. -46.	Timestamp .38us .29us .2us .11us .02us .93us .93us .84us .75us		ta Frame IRQU SMI4 IRQ2 IRQ4 IRQ5 IRQ5 IRQ5 IRQ5 IRQ5	Signal Sampled	2 5 0 11 14 17 20 23	f of clocks past St	art												
T -47. -47. -47. -47. -46. -46. -46. -46.	Timestamp .38us .29us .11us .02us .93us .84us .75us .66us	IRQ/Da 1 2 3 4 5 6 7 8 9	ta Frame IBOC IRQJ SHI4 IRQS IRQ4 IRQ5 IRQ5 IRQ5 IRQ5 IRQ5 IRQ5 IRQ5 IRQ5	Signal Sampled	2 5 8 11 14 17 20 23 26	t of clocks past St	art												
T -47. -47. -47. -47. -46. -46. -46. -46. -46. -46.	Timestamp .38us .29us .2us .11us .02us .93us .93us .84us .75us		ta Frame IRQU SMI4 IRQ2 IRQ4 IRQ5 IRQ5 IRQ5 IRQ5 IRQ5	Signal Sampled	2 5 0 11 14 17 20 23	t of clocks past St	art												
-47. -47. -47. -47. -46. -46. -46. -46. -46. -46. -46. -46	Simestamp           .38us           .29us           .2us           .1us           .02us           .63us           .84us           .75us           .66us           .57us           .44us           .39us	IRQ/De 1 2 3 4 5 6 7 8 9 10 11 12	ta Frame IRO( IRO) IRO IRO IRO IRO IRO IRO IRO IRO IRO IRO	Signal Sampled	2 5 8 11 14 17 20 23 26 29 32 35	* of clocks past St	art												
- 47. - 47. - 47. - 47. - 47. - 46. - 46.	Timestamp           .38us           .29us           .2us           .11us           .62us           .93us           .64us           .75us           .64us           .39us           .39us           .39us	IRQ/De 1 2 3 4 5 6 7 8 9 10 11 12 13	ta Frame IRO( IRO) 3814 IROS IROS IROS IROS IROS IROS IROS IROS	Signal Sampled	2 5 8 11 14 17 20 23 26 29 32 35 38	f of clocks past St	art												
-47. -47. -47. -47. -46. -46. -46. -46. -46. -46. -46. -46	Situs           .38us           .29us           .2us           .1lus           .02us           .93us           .64us           .75us           .64us           .37us           .48us           .39us           .24us           .29us           .29us           .29us           .29us           .29us           .29us           .29us	IRQ/De 1 2 3 4 5 6 7 8 9 10 11 12 13 14	ta Frame IRO( IRO) IRO( IRO( IRO( IRO( IRO( IRO( IRO( IRO) IRO( IRO( IRO( IRO( IRO( IRO( IRO( IRO(	Signal Sampled	2 5 8 11 14 20 23 26 29 32 35 38 41	t of clocks past St	art												
- 47. - 47. - 47. - 47. - 46. - 46.	Timestamp           .38us           .29us           .2us           .1lus           .02us           .93us           .84us           .75us           .66us           .37us           .44us           .39us           .12us           .39us           .12us           .21us           .12us	IRQ/De 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	ta Frame IRO( IRO) IRO) IRO( IRO) IRO( IRO) IRO) IRO) IRO( IRO) IRO) IRO) IRO( IRO) IRO) IRO( IRO) IRO) IRO) IRO) IRO( IRO) IRO) IRO) IRO) IRO) IRO) IRO) IRO)	Signal Sampled	2 5 0 11 14 17 20 23 26 29 32 35 30 41 44	t of clocks past St	art												
-47. -47. -47. -47. -46. -46. -46. -46. -46. -46. -46. -46	Simestamp           .30us           .29us           .2us           .02us           .93us           .84us           .75us           .66us           .87us           .39us           .3us           .3yus           .3yus           .3yus           .3us           .1us           .1us           .3us           .1us           .2us           .2us           .2us           .2us           .2us           .2us	IRQ/De 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	ta frame 1900 98/11 1902 1904 1904 1904 1904 1904 1904 1904 1904	Signal Sampled	2 5 0 11 14 14 20 23 26 29 32 35 38 41 41 44 47	F of clocks past St	art									a long			
-47. -47. -47. -46. -46. -46. -46. -46. -46. -46. -46	Timestamp           .30us           .29us           .2us           .1us           .02us           .04us           .75us           .66us           .67us           .48us           .39us           .3us           .3us           .21us           .12us           .025us           .635us	IRQ/De 1 2 3 4 5 5 6 7 8 9 10 11 12 13 14 15 16 17	ta Frame IRQ IRQ IRQ IRQ IRQ IRQ IRQ IRQ IRQ IRQ	Signal Sampled	2 5 11 14 17 20 23 26 29 32 35 36 41 44 47 50	t of clocks pest St	art									a lana			
1 -67, -47, -47, -46, -46, -46, -46, -46, -46, -46, -46	Timestamp .30us .29us .2us .11us .02us .64us .64us .64us .75us .64us .77us .64us .97us .21us .21us .21us .21us .21us .21us .64us .84us	IRQ/De 1 2 3 4 5 5 6 7 7 8 9 10 11 12 13 14 15 16 17 10 17 10 17 10 10 10 10 10 10 10 10 10 10	ta Frame ISO() 98(4) ISO() 180(4) ISO(2) ISO	Signal Sampled	2 5 11 14 17 20 23 26 29 32 35 38 41 44 47 50 53	t of clocks past St	art									C Lanna			
1 - 67. - 47. - 47. - 46. - 46	Timestamp 30us 29us 20us 20us 40us 40us 40us 40us 40us 40us 30us 20us 20us 20us 20us 40us 30us 4	IRQ/D# 1 2 3 4 5 6 7 7 8 9 9 10 11 12 13 14 15 16 17 18 19 19	ta Frame IRQ 1804 1802 1804 1805 1806 1806 1806 1806 1806 1806 1806 1806	Signal Sampled	2 5 11 14 17 20 22 26 29 32 35 38 41 44 47 50 53 56	f of clocks past St	art									C Lanna			
1 -67, -47, -47, -46, -46, -46, -46, -46, -46, -46, -46	Timestamp .30us .20us .20us .20us .20us .20us .30us .50us .60us .57us .60us .57us .60us .30us .30us .21us .21us .22us .30us .22us .30us .22us .30us .22us .30us .30us .22us .30us .30us .30us .22us .30us .30us .30us .30us .22us .30us .22us .30us .30us .30us .40us .30us .30us .40us .30us .40us .30us .40us .30us .40us .30us .40us .30us .40us .40us .30us .40us	IRQ/De 1 2 3 4 5 5 6 7 7 8 9 9 10 11 12 13 14 15 16 17 18 19 20	ta Frame 2800 3814 2802 2804 2804 2804 2804 2804 2804 280	Signal Sampled	2 5 0 11 24 27 20 23 29 32 35 38 41 44 47 50 53 55 59	t of clocks pert St	art									C Lanna			
1 -67. -67. -67. -67. -66. -66. -66. -66.	Timestamp .30us .20us .20us .20us .20us .20us .30us .50us .60us .57us .60us .57us .60us .30us .30us .21us .21us .22us .30us .22us .30us .22us .30us .22us .30us .30us .22us .30us .30us .30us .22us .30us .30us .30us .30us .22us .30us .22us .30us .30us .30us .40us .30us .30us .40us .30us .40us .30us .40us .30us .40us .30us .40us .30us .40us .40us .30us .40us	IRQ/D# 1 2 3 4 5 6 7 7 8 9 9 10 11 12 13 14 15 16 17 18 19 19	ta Frame IRQ 1804 1802 1804 1805 1806 1806 1806 1806 1806 1806 1806 1806	Signal Sampled	2 5 11 14 17 20 22 26 29 32 35 38 41 44 47 50 53 56	t of clocks peet St	art									C Lana			



# SGPIO

SGPIO (Serial General Purpose Input Output Serial) is a general-purpose

input/output that can be controlled by the user.

## Settings

SGPIO Settings		×
	Startup Settings	
	Mode:	3-bit Driver 👻
:#	Byte per column:	16-bits 👻
	Packets Starts From:	Low
Channel	Load Latch On:	Rising
Clock A0	SGPMO Latch On:	Falling -
Load A1 🌲	SGPMI Latch On:	Rising -
✓ DO A2 🜲	Display:	DataOut 👻
✓ DI 🛛 🗍	Significant Bit:	LSB 👻
Color Load / Start DO DI	Range Decode Range From Buffer Head	e To • Buffer Tail •
	Opefault	✓OK Cancel

**Channel:** Set the channel number of each signal on the object to be tested that is connected to the Logic Analyzer. These are Clock, Load, Data Out, and Data In. User can choose to have only Data Out, Data In, or both.

## Startup Settings:

Mode:



- 1. 3-Bit Driver:
- 2. User Defined Data, the following settings are valid only when the mode is switched to this item:

Byte per Column: Sets the Data-Size.

Packets Starts From: Set the Packet to start from Low or High.

Load Latch On: Latch data on rising or falling edge of Load Pin.

SGPMO Latch On: Latch data on rising or falling edge of SGPMO Pin.

**SGPMI Latch On:** Latch data on rising or falling edge of SGPMI Pin.

#### Result:

ne/Div=2us		9										032.724										
			190.61 us	-100.61 us	-106.61 va		61 us - 11	12.61 us	-100.61 us	-170.61 us	-176	Alus	-174.61 us	-172.61 us	170.01 us	-168.61 u	-100	61 us	-164.81 us	-162.61 us	-193.6	itus
	•	DO: 2	DO: 3	DO: 7	DO: 0	known DO:	3 DO:6	DO:1	DO: 2	DO:3	DO: 7	D0:0	mknown	DO: 3	0:6 DO:1	DO: 2	DO: 3	DO:7	DO: 0	unkaowa	DO: 3	DO: 6 DO
PBus1	C1k-40						ШЛ						Ш									
	Load-Al						560 n			9.04 10				555 a			9.04 ws				555 x	
sor	D0-A2	<b>"</b>	0 nx 530 n	1.48 m	1.54 m 570 n	960 xs 1	05 m 1.52 v	0 1.52 08		985 nz 535 n	1.48 us	1.55 m - R	3 m 953	ns 1.06 as	1.51 m 1.52	•	985 as 535 x	1.48 vs	1.55 us - 86	5 n 955	ns 1.06 m	1.51 w
	0	DE: 3	D1:0	Dt:0	DI:2 w	aknown DI:	1 DE:4	D1:7	D1: 3	DE: D	D1:0	D1:2	antoon	D1:1 1	12:4 DE:7	DE 3	DE: 0	DI: 0	D1: 2	minown	DI: 1	DI: 4 DI
	C1k-40		ΠΠ	innn				NNN				İNN				ŃN	NN	ÌNN			nnn	
IUS_SGPIC	Load-Al						560 n													Π		
107	DI-A3				600 n 730 nr							600 n 730 n							595 n 735 m	1.56 m		
<b>1</b> 5. <b>1</b> 5		OL	ive																			
el .	Channel																					
81 )Bu	BUS_SGP	10(SGP10) 🖵 😋	lin.															Q Sear	th All Fields	Text in	cludes	EX /
Т	imestamp	Device	r Specific	Vender Specifi	c(IDn.1) V	ender Specific	:(IDn.2)															
		Device 2		Activity	Loc																	
	.535us	Device 3		Activity		ate																
	.035us	Device 4		No Activity	No loc																	
	.535us	Device 5		No Activity	No loc																	
	.46us	Device 6 Device 0		No Activity Activity	Loc No loc																	
	.9648	Device 1	^	No Activity	No loc																	
	.46us	Device 2		Activity	Loc																	
	.96us	Device 3		Activity	Loc																	
	4648	Device 4		No Activity	No loc																	
	.96us	Device 5		No Activity	No loc																	
	.46us	Device 6		No Activity	Loc																	
	.00548	Device 0	3	Activity	No loc																	
7 -173																						



# Smart Card (ISO7816)

Smart Card is a communication protocol based on ISO 7816 specification, generally used in IC card or IC chip card, different IC chips have different functions and applications. It is mainly used for identification, recording and encoding/decoding.

### Settings

苎 Sma	art Card Settings				×
Settings	Channel	AO	Color	Start Data	<b>•</b>
	Data Baud Rate	A1	•	Parity End Error	
	ETU MSB First	32 (ETU range 1~2048)	Range		
	Invert Bits			From Buffer Head - Default	To Buffer Tail - DK Cancel

## Channel

CLK: Clock of transfer signal.

Data: Data of transfer signal.

ETU(Elementary Time Unit): The number of Clocks in each Bit.



#### Result





## SMBus

The full name System Management Bus (SMBus) is derived from I<sup>2</sup>C bus, which is a bus consisting of two signals. SMBus was defined by Intel in 1995, and contains Clock, Data, and commands based on Philips' I<sup>2</sup>C serial bus protocol. The clock frequency ranges from 10KHz to 100KHz.

## Settings

📇 SMBus	s Ver. 3.1 Settings				×
Settings			Color		
:	SMBCLK A0	Startup		Command Address	· ·
	SMBDATA A1			Write / Read Start / Stop / Sr ACK / NACK	
	8-bit addressing (Include R/W in	ı Address)		PEC / Word / Byte Count Data / Content	· · ·
	MCTP	SBS (Smart Battery System)		Word Address	· · · · · · · · · · · · · · · · · · ·
	SPD (Serial Presence Detect) Clock Stretching	DDR4	Range		
	Timeout Check 35000	us	- <b>1</b>	Decode Range	
	✔ Ignore Glitch			From	То
	Filter pulse with < 2	sample points		Buffer Head	▼ Buffer Tail ▼
				Defa	ult OK Cancel

#### Channel:

**SMBCLK:** Clock of transfer signal.

**SMBDATA:** Data of transfer signal.

Startup: PEC analysis. Enabled when checked.

8-bit addressing (Include R/W in Address): Displays the 8-bit width address

(7-bit width address plus 1-bit Rd/Wr). Enabled when checked.

**Device**, by default, the report window displays the SMBus analysis result.

Enabled when checked:



- 1. MCTP: Display MCTP analysis result in report area.
- **2. Show SBS:** The report window displays the Smart Battery System analysis, which shows the status of the battery and information such as voltage, current, or manufacturer information.
- 3. Show SPD(Serial Presence Detect): The report window displays the EEPROM analysis content, which shows the configuration information of memory modules (DDR3, DDR2, DDR, SPD SDRAM), such as the number of P-Banks, voltage, the number of row addresses/column addresses, the bit-widths, and the timing of each major operation (e.g., CL, tRCD, tRP, tRAS, etc.).

**Clock Stretching:** Set the time for Clock Stretching. Enabled when checked.

**Ignore Glitch:** Ignore noise caused by slow transitions when analyzing.

Enabled when checked.

#### Result

SMBus

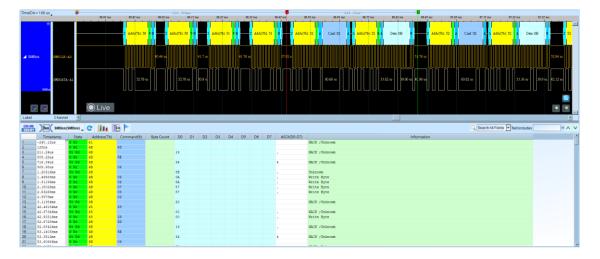
ime/Div=100 us	55.87 ma	55.97 ma	239, 354a.s 66.97 ms 66.17 ms	66.27 ms 66	1.37 ms 58.47 ms	60.57 ms 50.57 ms	49.20us 60.27 ms 60.87 ms	58.97 ma 5	7.07 ms 67.17 ms 67.27 ms	67.37 mi
0		S &6dz(7b): 50	N S Adds(7b): 50 V N	8 Addar(7h): 51 9 15	S Addar(7b): 51 N	8 Adder(7b): 52 A Coud: 02	8.31 A66:(7b):52 R.8 Deta:08	88	& Cmd: 02 & 12 Adds(76): 52 A	Data: 0B
d SMBus SKBCLK-A0			40.44 m	.7 w				51.78		52.94 ==
SHEDATA-A1		52.78 w	52.78 m 3	39 w		60.66 us	53.62 m 99.86	w 40.96 w	60.82 va	s 39.9 w 42.12 w
abel Channel	OLive									
	Bus) , C								Q Search All Fields Text inclu	des 🔍 🗛
	State Address(7b)		Byte Count D0 D1	D2 D3 D4 D5	D6 D7 ACCW	D0-D7)		Information		
	Rz 48	06	0A	02 03 04 03		Write Byte				
	Wz 50					NACK ; Unknown				
	Wz 50					NACK /Unknown				
56.22164ms S	Wz 51					NACK ; Unknown				
	Wr 51 Wr 52	02				NACK ; Unknown				
	Rd 52	~	08			NACK ; Unknown				
	Wr 52	02				,				
	Rd 52		08			NACK /Unknown				
57,43896ng S	Wr 52	02								
57.65036ms Sr	Rd 52		08			NACK /Unknown				
57.65036ms 51 57.90758ms 51	Rd 52 Wz 52	80								
57.65036ms 51 57.90758ms 51 58.11906ms 51	Rd 52 Rz 52 Rd 52		0B 49		I	NACK /Unknown				
57.65036ms Sr 57.90758ms Sr 50.11906ms Sr 50.37762ms S	r Rd 52 We 52 r Rd 52 We 52	80 81	49			BACK /Unknown				
57,65036ms Sr 57,90758ms Sr 58,11906ms Sr 58,37762ms Sr 58,509ms Sr	Rd         52           Wr         52           Rd         52           Wr         52           Rd         52				I M					
S7.65034ms         Sr           S7.90758ms         S           S5.11904ms         S           S0.3776ms         S           S0.509ms         S           S0.4354ms         S           S0.90358ms         S	r Rd 52 We 52 r Rd 52 We 52	81	49			BACK /Unknown				
3         57.65034ms         58           4         57.90750ms         51           5         50.11904ms         51           5         50.37742ms         51           7         50.509ms         52           8         50.4354ms         52           9         59.0545ms         52           5         50.31252ms         52	Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52	81	49 4D 53		M S	NGACH ; Unknown NGACH ; Unknown NGACH ; Unknown				
57.65034ms         57.9075ms         50.1504ms         50.1504ms         50.1504ms         50.505ms         50.505ms	Rd         52           RE         52           Rd         52	01 02 03	49 4D		м	HACK ;Unknown				
57,6503(ms 57 57,90750ms 5 58,1199(ms 0 58,0199(ms 0 58,04354ms 57 59,0445ms 57 59,0445ms 57 59,0445ms 57 59,0445ms 57 59,0445ms 57 59,72275ms 51	Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52           Rd         52	81 82	49 4D 53		M S	NGACH ; Unknown NGACH ; Unknown NGACH ; Unknown				



Show SBS (Smart Battery System)

= 100 us	*	55.87 ms 55.97 ms	239,354as 66,07 ms 56,17	ns 66.27 ms	56.37 ms	58.47 ma	55.57 ms	447, 20us 66.67 ms	56.77 ms	66.87 ms	58.97 ms	47.07 ms	67.17 ms	67.27 ms	67.37 mg
		55.97 mg 55.97 mg	00.17 ms 00.17	nd 00.27 ms	56.37 m3	58.47 md	00.07 md	511 70.00	50.77 ms	66.87 ms	66.97 ms	67.07 ms	67.17 md	67.27 HS	67.37 md
e		3 <mark>8//8/(76): 50</mark>	N 3 Adde(7b): 50 9 8	NSAddu(74):51	x	): 51 N	S A44c(7b):52 A	Caul: 02 & 3 & 6	Ma(7b): 52 R A	Data: 0B	3 <u>&amp;ddu(7b): 1</u>	2 A Cmd:02	A-31 Adda	76): 52 A	Data: 0B
as SHECLK-	<b>L</b> 0		40.44 mi	41.7 us	41.76 ==	37. <b>9</b> 2 o					51.78 m				52.9
SMEDATA	-61	52.78 w	52.78 w	90.9 w					53.62	1 uu 99.86 uu	4C.96 m	60.82 w		53.36	m 19.9 m 42.1
Channe		Live													
	4														
												Q	Search All Field	Is 💌 Text inclu	ides
Bus SMBus	SMBus) _ C Address(7b)	Function		Content		Unit	Duration	Info	mation			Q	Search All Field	is 💌 Text inclu	ides
Bus SMBus( Timestamp -240.12us	SMBus) C Address(7b)	Function	_	Content			127636 us	Info	ormation			Q	Search All Field	ls 💌 Text inclu	sdes
Timestamp -240.12us 120ns	SMBus) C Address(7b) 30 25	Function Undefined Cmd(5D)	19	Content			127636 us 127396 us	Info	mation			Q	Search All Field	Is 💌 Text inclu	ides
Bus SMBus Timestamp -240.12us 120ns 505.22us	SMBus) _ C Address(7b) 30 25 25	Function Undefined Cmd(SD) Undefined Cmd(SE)	34	Content			127636 us 127396 us 126891 us	Info	mation			Q	Search All Field	Is 💌 Text inclu	Ides
Timestamp           -240.12us         *           120ns         \$           505.22us         \$           989.98us         *	SMBus) C Address(7b) 30 25 25 25	Function Undefined Cmd(5D) Undefined Cmd(5E) Undefined Cmd(06)	34 88	Content			127636 us 127396 us 126891 us 126406 us	Info	rmation			Q	Search All Field	Is 💌 Text inclu	Ides
Bus:         SMBus(           Timestamp         -240.12us         120ms           120ms         505.22us         999.99us         1.46503ms	SMBus) _ C Address(7b) 30 25 25 25 25 25 25	Function Undefined Cmd(SD) Undefined Cmd(SE) Undefined Cmd(06) Undefined Cmd(06)	34 88 0A	Content			127636 us 127396 us 126891 us 126406 us 125930 us	Info	emation			Q	Search All Field	Is 💌 Text inclu	ides
Busk         SMBusk           Timestamp         -240.12us         120ns           120ns         505.22us         969.90us         1.46500ns           1.46500ns         1.81196ns         1.81196ns	SMBus) _ C Address(7b) 30 25 25 25 25 25 25 25	Function Undefined Cmd(5D) Undefined Cmd(5E) Undefined Cmd(06) Undefined Cmd(06) Undefined Cmd(06)	34 68 6A 8A	Content			127636 us 127396 us 126891 us 126406 us 125930 us 125584 us	Info	ormation			Q	Search All Field	15 💌 Text inclu	ides
XBusx         SMBus(           Timestamp         -240.12us         #           120ns         505.22us         #           505.22us         999.99us         1.4650ms           1.46150ms         2.18026ms         #	SMBus) C Address(7b) 30 25 25 25 25 25 25 25 25	Function Undefined Cmd(SD) Undefined Cmd(SE) Undefined Cmd(06) Undefined Cmd(06) Undefined Cmd(07) Undefined Cmd(07)	34 88 0A 83 87	Content			127636 us 127396 us 126891 us 126406 us 125930 us 125584 us 125216 us	Info	rmation			Q	Search All Field	is 💌 Text inclu	ides
Disc         SMBus(           Timestamp         -240.12us         *           120ns         505.22us         *           99.96us         1.4650tms         1.9119-8ms           1.8119-8ms         2.18026ms         2.53268ms	SMBus) C Address(7b) 30 25 25 25 25 25 25 25 25 25	Function Dodefined Cmd(5D) Dodefined Cmd(5E) Dodefined Cmd(6E) Dodefined Cmd(06) Dodefined Cmd(07) Dodefined Cmd(07) Dodefined Cmd(07)	34 88 0A 83 87 87	Content			127636 us 127396 us 126951 us 126406 us 125930 us 125584 us 125516 us 124263 us	Info	mation			Q	Search All Field	Is 💌 Text inclu	ides
Encode         SMBus           Timestamp         -240.12us         6           120ns         505.22us         99.99us         1.46500ms           1.46500ms         1.81194ms         2.18026ms         2.53260ms           2.853260ms         2.85726ms         3.85726ms         3.85726ms	SMBus) C Address(7b) 30 25 25 25 25 25 25 25 25 25 25 25	Function Obdefined Chd(SD) Obdefined Chd(SD) Obdefined Chd(SE) Obdefined Chd(O4) Obdefined Chd(O4) Obdefined Chd(O2) Obdefined Chd(O2) Obdefined Chd(O2)	34 88 0A 83 87 87 20	Content			127636 us 127396 us 126891 us 126406 us 125594 us 125594 us 125216 us 12483 us 12489 us	Info	emation			Q	Search All Field	IS 💌 Text inclu	ides
Busk         SMBusk           Timestamp         -240.12us           120ns         505.22us           969.90us         1.46500ms           1.46500ms         2.18026ms           2.18026ms         2.3226ms           2.42.46194ms         2.4948ms	SMBus) C Address(7b) Address(7b) 30 25 25 25 25 25 25 25 25 25 25	Function Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10) Undefined Cnd(10)	34 68 0A 82 87 87 20 00	Content			127636 us 127396 us 126891 us 126806 us 125504 us 125584 us 125584 us 1258216 us 124896 us 124498 us	Info	mation			Q	Search All Field	IS 🛡 Text inclu	ides
Euc. SMBus/ Timestamp -240.12us 989.90us 1.46500ms 1.81196ms 2.18026ms 2.83206ms 2.83206ms 2.8370ms 42.46194ms 42.46194ms	SMBus) Address(7b) 30 25 25 25 25 25 25 25 2	Function Undefined Cha(SD) Undefined Cha(SE) Undefined Cha(SE) Undefined Cha(OE) Undefined Cha(OE) Undefined Cha(OE) Undefined Cha(OE) Undefined Cha(OE) Undefined Cha(OE) Undefined Cha(OE) Undefined Cha(OE)	34 88 0A 87 87 20 00 00	Content			127636 us 127396 us 126851 us 126851 us 126860 us 125504 us 125524 us 125216 us 124863 us 84934 us 84934 us	Info	rmation			Q	Search All Field	IS 💌 Text inclu	ides
Eux SMBus/ SMBus/ S05.22us 999.90us 1.4650tns 1.61196tns 2.5326tns 2.5326tns 2.5326tns 42.46194tns 42.45316tns 52.6728tns	SMBus) C Address(7b) Address(7b) 30 25 25 25 25 25 25 25 25 25 25	Function Undefined Cha(16D) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E)	34 88 8A 87 67 20 00 00 19	Content			127636 us 127394 us 126896 us 126896 us 125930 us 125524 us 125524 us 125216 us 124893 us 124893 us 124893 us 84934 us 84463 us 74723 us	Info	mation			Q	Search All Field	IS V Text inclu	ides
Constants           12000         SMB0esi           12000         SM00esi           12000         S000           12000         S000           12000         S000           1.46500ms         1.46500ms           1.81196ms         2.18020es           2.53260ms         2.8970ms           42.46194ms         42.33316ms           52.47294ms         53.14030ms	SMBus) C Address(7b) 30 25 25 25 25 25 25 25 25 25 25	Function Observations Observation Observat	34 88 83 87 87 20 00 00 19 34	Content			127636 us 127396 us 126851 us 126851 us 126806 us 125524 us 125216 us 12683 us 124498 us 84934 us 84944 us 84945 us 74723 us 74225 us	info	emation			Q	Search All Field	is Text inclu	ides
Euc.         SMBust           Timestamp         -240.12as           120ns         505.22as           999.90us         1.4650ms           1.4650ms         1.81196ms           2.53265ms         2.6970ms           42.45194ms         55.267ms           53.4070ms         53.4031ms           53.4031ms         53.4031ms	SMBus) C Address(7b) 30 25 25 25 25 25 25 25 25 22 25 25	Function Undefined Cha(16D) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(15E) Undefined Cha(15E) Undefined Cha(15E)	34 88 0A 87 20 00 00 19 34 28	Content			127636 US 127594 US 126891 US 126406 US 125500 US 125504 US 125516 US 124663 US 124663 US 74723 US 74256 US 74256 US	info	ormation			Q	Search All Field	is 💌 Text inclu	ides
Dimestamp           -240.12xs         120ns           505.22xs         120ns           120ns         505.22xs           10156ms         1.46502ms           1.01156ms         2.18026ms           2.18026ms         2.18778ms           42.46134ms         52.67294ms           52.47394ms         53.4038ms           53.4038ms         53.4038ms	Address(7b) 30 25 25 25 25 25 25 25 25 25 25 25 25 25	Function Observations Observation Observat	34 88 83 87 87 20 00 00 19 34	Content			127636 UB 127394 UB 126891 UB 126891 UB 126891 UB 126804 UB 125524 UB 125524 UB 125524 UB 124458 UB 04954 UB 74225 UB 74225 UB 73709 UB 73221 UB	Info	emation			Q	Search All Field	is 🛡 Text inclu	ides
Disc.         SMBbs/           Timestamp         -240.12us           120ns         505.22us           969.90us         1.4650ms           1.81196ms         2.18026ms           2.83260ms         2.83260ms           2.8376ms         5.3260ms           3.40316ms         53.4603ms           53.4603ms         53.4603ms           55.9456ms         55.9456ms	SMBus) C Address(7b) 30 25 25 25 25 25 25 25 25 25 25	Function Undefined Cha(16D) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(15E) Undefined Cha(15E) Undefined Cha(15E)	34 88 0A 87 20 00 00 19 34 28	Content			127636 UB 127394 UB 126891 UB 126891 UB 126890 UB 125840 UB 125840 UB 12584 UB 124463 UB 124463 UB 124463 UB 124463 UB 12468	info	rmation			Q	Search All Field	is 💌 Text inclu	rdes [
Date         SMBus(           Timestamp         -240.12us           120ns         505.22us           505.22us         506.22us           1.01156as         1.01156as           2.18026ms         2.0570ms           42.45316ms         52.47294ms           53.4606ms         53.4606ms           55.9456ms         55.9456ms           56.07376ms         55.9456ms	Address(Tb) 30 25 25 25 25 25 25 25 25 25 25	Function Undefined Cha(16D) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(15E) Undefined Cha(15E) Undefined Cha(15E)	34 88 0A 87 20 00 00 19 34 28	Content			127536 us 127396 us 126891 us 126891 us 126894 us 125810 us 125824 us 125824 us 12483 us 12483 us 74256 us 74256 us 74256 us 73759 us 73251 us 71462 us 71462 us	Info	mation				Search All Field	15 💌 Text Inclu	ides
Disc.         SMBDisc.           Timestamp         -240.12us           120m         505.22us           505.22us         969.90us           1.46500ms         1.01196ms           2.180260ms         2.53260ms           2.6370ms         42.45316ms           35.4603ms         35.4603ms           55.9456ms         55.9456ms           56.07736ms         56.07736ms           56.077378ms         56.077378ms	Address(Tb) 30 Address(Tb) 30 25 25 25 25 25 25 25 25 25 25	Function Undefined Cha(16D) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(15E) Undefined Cha(15E) Undefined Cha(15E)	34 88 0A 87 20 00 00 19 34 28	Content			127636 US 127394 US 126891 US 126891 US 126891 US 125504 US 125514 US 125514 US 124643 US 124643 US 124643 US 12465 US 74723 US 74725 US 7322 US 7322 US 7322 US 7321 US 7321 US 7321 US 7321 US	Info	rmation			٩	Search All Field	is 💌 Text inclu	:des [
Jean         SMBus(           Trmestamp         -240.12us           120na         100.20us           105.22us         999.90us           1.61196ans         1.01196ans           2.180208ms         2.85206ans           2.85718ms         42.463194ans           42.463194ans         52.87294ans           53.14038ms         55.94354ans           55.94354ans         55.94354ans           56.02734ms         56.26604ans           56.36604ans         7.87244ans	SMBus) C C C C C C C C C C C C C C C C C C C	Function District Cos(10) Constrant Cos(16) Constrant Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16) District Cos(16)	34 68 0A, 87 87 20 00 00 19 34 8A, 0A	Content			127536 Um 127396 Um 126891 Um 126891 Um 126894 Um 125830 Um 125834 Um 125824 Um 126894 Um 124498 Um	into	smation			Q	Search All Field	15 💌 Text inclu	idea
2600 SMBbs/ Timestanp -240.12as 120na 969.69us 1.4650ms 1.81196ms 2.18026ms 2.18026ms 2.18026ms 2.18026ms 2.18026ms 2.18026ms 2.18026ms 2.18026ms 2.18026ms 3.14035ms 5.14035ms	Address(Tb) 30 25 25 25 25 25 25 25 25 25 25	Function Undefined Cha(16D) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(16E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(12E) Undefined Cha(15E) Undefined Cha(15E) Undefined Cha(15E)	34 88 0A 87 20 00 00 19 34 28	Content			127636 US 127394 US 126891 US 126891 US 126891 US 125504 US 125514 US 125514 US 124643 US 124643 US 124643 US 12465 US 74723 US 74725 US 7322 US 7322 US 7322 US 7321 US 7321 US 7321 US 7321 US	into	smation			٩	Search All Field	15 💌 Text Inclu	udes

Show SPD (Serial Presence Detect)





# SMI

SMI (Serial Microprocessor Interface) was developed by BDNC and consists of

a Clock and Data.

## Settings

🗮 SMI Se	ettings		×
Settings			
<b>:</b>			
CLK		Data	
A0	\$	A1	\$
Color			
	Color Settings		
	Attn		•
	Sel / Desel		•
	R/W		-
	Address		•
	Data		-
	Attn desel		•
Range			
<b>R</b>	Decode Range	•	
From		То	
Buffer	Head 👻	Buffer Tail	•
	Default	<b>√</b> 0К	XCancel

## Channel:

**CLK:** Clock of transfer signal.

Data: Data of transfer signal.



### Result





## SPI

The Serial Peripheral Interface Bus (SPI) is a 4-wire synchronous sequential data protocol for portable device platform systems. Serial peripheral interfaces are generally 4-wire, and can sometimes be 3-wire or 2-wire.

## Settings

🗯 SPI	Settings	×
Setting		
	Туре	3 Wire-SPI
	3 Wire-SPI 🔹	Chip Select Channel (CS) CH 0
		Data Channel (SDA) CH 2
	Clock Channel(SCK)	Chip Select Edge Data Edge Active Low
	Bit Order MSB First 👻	SDI(Write)-Latency-SDO(Read)
	Word Size 8 bit (4~40)	Write Length 0 Latency 2
	Data valid from SCK 0 💌 S/R Clk	Read Length 32776 (Bits)
	Report	
	<ul> <li>Show Idle state in report window</li> <li>Reduce report</li> </ul>	
	Show data in report (Column) 16 💌	
Color	SDI/SDA/Write Channel	
	SDO/Read Channel	
Range	Decode Range	
<b>5</b>	From To	
	Buffer Head 👻 Buffer Tai	I ▼
	Default	✓OK ★Cancel

**Type:** Select the SPI type, the default is 3-wire-SPI, which is included:

## 4 Wire-SPI dialog box →CS, SCK, SDI, SDO

User can set the trigger edge of CS, SDI and SDO respectively, the default

setting of CS is Active Low, and the default setting of SDI/SDO is Active High,



because the SDI and SDO data will be displayed at the same time. User can

select the last data to be displayed in the display data channel as SDI only,

SDO only or both, and the default is Both.

4 Wire-SPI	
Chip Select Channel (CS)	CH 0
Data Channel (SDI)	CH 2
Data Channel (SDO)	CH 1
Chip Select Edge	Active Low 👻
SDI Edge	Rising -
SDO Edge	Rising -
Show Data Channel	Both 👻

## 3 Wire-SPI dialog box → CS, SCK, SDA

In 3-wire Slave select mode, only 1 data channel (either SDI or SDO) is required. User can set the triggering edge of CS and Data respectively, the default setting of CS is Active Low, and the default setting of Data is Active High, for general application, the data channel is a single line and unidirectional way to transfer data.



Wire-SPI	
Chip Select Channel (CS)	CH 0 🗢
Data Channel (SDA)	CH 2
Chip Select Edge Active Low 👻	Data Edge Rising 💌
SDI(Write)-Latency-SDO	(Read)
Write Length	Latency 2
Read Length 32776	(Bits)
ACS	

We also provide a one-line bidirectional transmission mode. As shown in the

#### figure below

✓ SDI(Write)-Lat	ency-SDO(Read	)
Write Length	0	Latency 2
Read Length	32776	(Bits)
ACS SCK SDAX		Read

User only need to check "SDI(Write)-Waiting-SDO(Read)", then user can set the bit number of bidirectional transmission. Let's take Master as our point of view, the write length is the number of bits that Master puts into the data channel, the minimum is 1. The number of bits that wait for Slave to process is the minimum is 0. Then the data is collected according to the read length, the minimum is 1. The maximum value of these 3 parameters is 65535.

## 3 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDI, SDO



Since CS is not used, user has to set the Idle time of SCK as the frame separating time. In 3-wire without Slave select mode, user need to set the channel where SDI/SDO is located and its trigger edge to Active High. In the 3-wire non-slave select mode, user need to set the channel where SDI/SDO is located, and set the trigger edge of SDI/SDO to Active High, and set the time to wait for Clock Idle to separate the frames. The SDI and SDO data will appear at the same time. User can select the last data to be displayed in SDI only, SDO only or both in the display data channel, and the default is Both.

o mile of itomased omp cered	/
Data Channel (SDI)	CH 0
Data Channel (SDO)	CH 2
SDI Edge	Rising -
SDO Edge	Rising
Frame guard time	0 ns
Show Data Channel	Both -
SCK	

3 Wire-SPI(Unused Chip Select)

## 2 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDA

Since CS is not used, user has to set the Idle time of SCK as the frame separating time. In 2-wire without Slave select mode, user need to set the channel where the data is located and its trigger edge to Active High. The trigger edge of the data channel and the trigger edge of the data channel should be set to Active High, and set the time to wait for the Clock Idle as the Frame Separation. In general application, the data channel is a single line and



unidirectional way to transfer the data.

2 Wire-SPI(Unused	Chip Select)
Data Channel (S	(DA) CH 0
Data Edge	Rising 💌
SDI(Write)-La	atency-SDO(Read)
Write Length	0 Latency 2
Read Length	(Bits)
Frame guard tin SCK SDA	

If Slave select is not used, and the time between frames is not 0, the application example is as follows. The signals are only CLK, DATA, Frame is separated by 6 us, and the data trigger edge is Rising. it can be seen that if the Clock pause interval is more than 6 us, it will be recognized as Idle.

CLK 🛛 🗸	TUUU						
DATA 2 X							
SPI 2,0 X↓b	0	D Idle	AA	Idle 84	Idle 00	Idle	00 Idle



SPI Settings	×
Setting	2 Wire-SPI(Unused Chip Select)
2 Wire-SPI(Unused Chip Select)	Data Channel (SDA) CH 0 🗢 Data Edge Rising 🗸
Clock Channel(SCK) CH 1	SDI(Write)-Latency-SDO(Read) Write Length 0 Latency 2
Bit Order MSB First ▼ Word Size 8 bit \$(4~40)	Read Length 32776 (Bits)
Data valid from SCK 0 - S/R Clk	Frame guard time 0 ns
Report	
<ul> <li>✓ Show Idle state in report window</li> <li>Reduce report</li> </ul>	
Show data in report (Column) 16 👻	
Color SDI/SDA/Write Channel	
From To	
Buffer Head 💌	ail 🔹
Opefault	✓OK XCancel

When Slave select is not used, and the Frame separation time is 0, it can be another kind of continuous data analysis, as shown in the following figure. The signal is only CLK, DATA, and the time between frames is 0, the data trigger is in Falling.

CLK D		
DATA 1 X		
SPI-2 wire 1.0 XJb	BAFB 70	J22 3A3A



spi	Settings	×
Setting	I	
	Туре	2 Wire-SPI(Unused Chip Select)
	2 Wire-SPI(Unused Chip Select) 👻	Data Channel (SDA) CH 0
		Data Edge Rising 👻
	Clock Channel(SCK) CH 1	SDI(Write)-Latency-SDO(Read)
		Write Length 0 Latency 2
	Bit Order MSB First 👻	Read Length 32776 (Bits)
	Word Size 8 bit (4~40) Data valid from SCK 0 - S/R Clk	Frame guard time 0 ns
	Report	
	<ul> <li>✓ Show Idle state in report window</li> <li>□ Reduce report</li> </ul>	SCK
	Show data in report (Column) 16 👻	
Color	SDI/SDAWrite Channel	
•	SDO/Read Channel	
Range	Decode Range	
	From To	
<b> </b>		
	Buffer Head 👻 Buffer Ta	il 👻
	Default	✓OK ★Cancel

**Bit Order:** You can configure the SPI data interpretation as either MSB first or LSB first. The default setting is LSB first.

**Word Size:** You can set the data word size in bits. During SPI analysis, this value will define the number of bits for each data word. The minimum value is 4, and the maximum value is 40. The default value is 8.

#### Report:

Show Idle state in report window: In SPI applications, there may be intervals with the Idle State between each data capture. To make data review easier, you can configure the report window to hide the Idle State. By default, the Idle State is shown.



**Reduce report:** You can configure consecutive SPI data to be displayed in the report window in a format ranging from 1 to 16 columns. The default setting is 16 columns, and the ASCII-encoded results can be viewed on the far right side of the report window.

**Data Valid from SCK:** In certain devices using SPI transmission, there is a delay between the data output and the valid data, which does not align with the clock's edge. To accommodate such devices, you can configure the "Data Valid from SCK" to delay this time. You can input the delay time in terms of the sampling rate, with a range of 0-3. By default, there is no delay. If set to 1, with a sampling rate of 200 MHz, the actual delay time will be 5 ns.

#### Result

me/Div=1us		<b>N</b>				948.5										698.095us					3
		-515	-4 ed		-3 u	s 	-2	us 	1	us 0	gs	1us 2us	3 65	415	6u3		7 us	 805	Pes	10 u	s 11 us
•										05 01					05 00					05 00	
											1 × 1										
	05-80									555 au	80 10	3.77 u									
A SPI-DataIn															0.0					10	
	SDA-A2																				
										1000					CONTRACTOR OF						
3	3CK-#1									425 as											
																				A ROWLINGS	
											00				00 37					00 3F	
											1 – I										
	CS-80																				
SPI-DataOut																					
	3DA-#3																				
	3CK-#1									425 m	0000										
50	JUN-ML											4070									
		<b>A</b>																			
<b>P</b> 5. <b>P</b> 5		OLive																			
abel (	Channel	T											_								5
				_	_	_	_	_	_		_				_		_		-	_	
HLOO BUS	SPI-DataOut	(SPI) 🗸 😋 🛄																Cearch All Fi	elds 💌 Text	includes	EX 🔨
Times		Status(8 bits data)	DO	D1	D2	D3	D4	D5	D6	D7 ASC	II(D0-D7)	Information									
-7.465us		ile	00									Duration: 6.555 us									
-910ms		ita ile	00									Duration: 445 ns									
-205ms	7 Da	ite ita	00	00								Durgerout eeo no									
350n#		ile	~~	~~								Duration: 4.075 us									
4.42508		ita	00	38						- ?											
4,980#		lle										Duration: 4.370 us									
9,350#		ica	00	38						-7											
9.905us		ile										Duration: 4.520 us									
14.425us		ita	00	37						.7											
14.98us	Id	ile										Duration: 4.445 us									
19.425us		ita	00	38						.?											
19.90us	Id	ile										Duration: 4.445 us									
24 42514		**	00	27						2											



# **SPI NAND**

The SPI NAND Flash Memory series uses the SPI/QPI transmission protocol for data communication. The SPI NAND bus analysis allows users to view both command and input/output bus information simultaneously, saving time when using the SPI bus analysis waveform.

## Settings

	ttings			×
Parameter Settir	ngs			
<b>:</b>				
CS#	A0	SCK	A1 🌲	Micron 💌
SI/SO0	A2	\$0 / \$01	A3 🌲	MT29FXG01AAADD
WP/SO2	A4	HOLD#/SO3	A5 🗘	
Refer to #	Hold Status			
Start up readi	ng mode	Continuous R	ead 👻	
Command de	eselect time		—— 100 ns	
		n SCK rise edge		
Clock LOW to	output valid	•	15 ns	
Show Cal	culated Phys	ical Address From F	age Address	
Show all r	epeated Get	/Set Feature Data		
Color	epeated Get	/Set Feature Data		
	epeated Get	/Set Feature Data		
	epeated Get	/Set Feature Data		
	epeated Get	/Set Feature Data	Dummy	
Color	epeated Get		Dummy Data In	
Color Op Code	epeated Get	•		
Color Op Code Address	epeated Get	•		
Color Op Code Address Data Out Range	epeated Get	•		
Color Op Code Address Data Out Range		•		



**CS#:** Chip Select of transfered singal.

**SCLK:** Clock of transferred signal.

**SIO0 – SIO3:** Data pins for data transfer.

**Start up reading mode:** Enables selection of the read state during initial analysis.

**Command deselect time:** Adjustable hold time for determining CS# inactivity during analysis.

**Clock LOW to output valid** : Adjustable setting for determining the actual data position during analysis.

**Refer to #Hold Status:** Decode based on the state of the #Hold pin. Enabled when checked.

Latch IC output data on SCK rise edge: Latch Data on the rising edge of SCK for analysis. Enabled when checked.

Show Calculated Physical Address From Page Address: Display the full address. Enabled when checked.

**Show all repeated Get/Set Feature Data:** Fully display repeated Get or Set Feature data. Enabled when checked.

		3.03 ma		2.401			4.919as 3.83 ma					4.60 ma	4.83 ma	6.03 ma			43 ma	6.83 ma	5.83 mi		
		3.03 ma	0.23 ma	3,401	na :	1.63 ma	3.83 ma	4.03 ma	4.23 r	na 4	40 ma	4.63 ma	4.83 ma	6.02 ma	6.23 m		40 ma	6.63 ma	5.03 mi	6.03 ma	
AO																					
A1		161.14 ==	161.14 w	161.22 w	161.14 us	161.14 w	161.24 w	161.14 w	161.14 us	161.22 18	161.34 m	161.24 us	161.14 us	161.22 us	161.14 uz	161.14 📾	161.24 w	161.14 w	161 14 us	161.22 w	
AZ																					
A3		161.56 m	161.56 m	161.66 m	161.56 m	161.54 w	16) 64 w	161.56 m	161.56 w	161.66 m	161.56 m	161.69 m	161.56 m	161.65 m	161.56 ==	161.54 m	161.64 m	161.56 m	161 36 w	161.66 va	
• 1 A0 , A0	A3,A: 03	60	ω	ω	03	03	03	0.3	ω	03	ω	ω	ω	O2	ω	ω	0.3	ω	<u>(</u> 13	03	0.3
		Live																			۰
Chann	el I	Live																			
Chann	el 🔹	<u>III.</u> E								_							Q	Search All Field	is 💌 Text inclu	des	
Channer Channe	el I SPI NAND) 🖉 😋	Op Code		Address	Dummy	D0	D1 D2	D3	D4 D5	D6	D7						Q	Search All Field	IS 💌 Text inclu	des	•
Bus Bus 1 Timestamp 2.30838ms	el 🔹	Op Code			Dummy	03	D1 D2	D3	D4 D5	D6	D7			Memo .120 ns (Repe			۹	Search All Field	is 💌 Text inclu	des	
Channel Bus Bus 1 Timestamp 2.30838ms 4.59392ms	el • SPI NAND) • C GET FEATURE (OF	Op Code			Dummy		D1 D2	D3	D4 D5	D6	D7						Q	Search All Field	is 💌 Text inclus	des	
Chann Bust, Bus 1 Timestamp 2.30838ms 4.59392ms 4.60828ms	el SPI NAND) C GET FEATURE (OF WRITE ENABLE (O	Op Code	co	)	Dummy	03	D1 D2	D3	D4 D5	Dő	D7						Q	Search All Field	Is 💌 Text inclus	des	•
Chann Chann	el  SPI NAND)  C GET FEATURE (OF KRITE ENABLE (O BLOCK ERASE (DE	Op Code F) 061		00080	Dummy	03 00	D1 D2	D3	D4 D5	Dő	D7		Duration: 2	.120 ms (Repe	at: 14 Time:	»)	٩	Search All Field	Is 💌 Text inclu	des	
Chann Channel Chane	el SPI NAND) C GET FEATURE (OF WRITE ENABLE (O	Op Code F) 061	co	00080	Dummy	03	D1 D2	D3	D4 D5	D6	D7		Duration: 2		at: 14 Time:	»)	Q	Search All Field	is 🔽 Text inclus	des [	•
Chann Channel	el  SPI NAND) C GET FEATURE (OF WRITE ENABLE (O BLOCK ERASE (DE "" GET FEATURE (OF	Op Code F) D() F)		00080	Dummy	03 00	D1 D2	D3	D4 D5	D6	D7		Duration: 2	.120 ms (Repe	at: 14 Time:	»)	Q	Search All Field	is 💌 Text inclu	des	•
Chane C. JBus, Bus 1 Timestamp 2.30838ms 4.60932ms 4.60972ms 4.61432ms 6.93906ms 6.93906ms	el  SPI NAND) C GET FEATURE (OF BLOCK ERASE (D) GET FEATURE (OF WRITE ENABLE (O KRITE ENABLE (O	Op Code () () () () () () () () () ()	00	00080	Dummy	03	D1 D2	D3	D4 D5	D6	D7		Duration: 2	.120 ms (Repe	at: 14 Time:	»)	Q	Search All Field	IS 💌 Text inclu	des	
Chane Chane Constant Co	el  SPI NAND) C GET FEATURE (OF MELICK ERABLE (O BELICK ERASE (DE WRITE ENABLE (O BLOCK FRASE (DE BLOCK FRASE	Op Code () () () () () () () () () ()		00080	Dummy	03 00 03 00	D1 D2	D3	D4 D5	D6	D7		Duration: 2 Duration: 2	.120 ms (Repe	eat: 14 Time:	9)	٩	Search All Field	is 💌 Text inclus	des [	
Chane Chane Constant Co	el  SPI NAND) C GET FEATURE (OF BLOCK ERASE (D) GET FEATURE (OF WRITE ENABLE (O KRITE ENABLE (O	Op Code () () () () () () () () () ()	00	00080	Dummy	03 00 03 00 03	D1 D2	D3	D4 D5	D6	D7		Duration: 2 Duration: 2	.120 ms (Repe	eat: 14 Time:	9)	Q	Search All Field	is 🛡 Text inclui	des	
Chane Ch	el · · · · · · · · · · · · · · · · · · ·	Cop Code F) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def) Def Def Def Def Def Def Def Def		00080	Dummy	03 00 03 00	D1 D2	D3	D4 D5	D6	D7		Duration: 2 Duration: 2	.120 ms (Repe	eat: 14 Time:	9)	۵	Search All Field	is 💌 Text inclus	des	
Chane Ch	el 4 SPI NAND) C GET FEATURE (OF HEITE ENALE (O ELOCK ERASE (D ELOCK ERASE (D ELOCK ERASE (D ELOCK ERASE (D ELOCK ERASE (D ELOCK ERASE (D HEITE ENALE (OF HEITE ENALE (OF	Dp Code D) D(1)	00 00 00	) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) ) )	Dummy	03 00 03 00 03	D1 D2	DJ	D4 D5	D6	D7		Duration: 2 Duration: 2	.120 ms (Repe	eat: 14 Time:	9)	۹	Search All Field	is 👿 Text inclu	des	
Chane Ch	el · · · · · · · · · · · · · · · · · · ·	Op Code () () () () () () () () () ()	00 00 00	00080	Dummy	03 00 03 00 03	D1 D2	D3	D4 D5	D6	D7 .		Duration: 2 Duration: 2 Duration: 2	.120 ms (Repe	eat: 14 Time: eat: 14 Time: eat: 14 Time:	n) n)	<u>(</u>	Search All Field	is 💌 Text inclu	des	•

#### Result

The report will delete the repeated value while Op Code = Get Feature (0F).



And mark its duration time °



# SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals: Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame Synchronous (FS). The SSI protocol supports either the Normal or Network mode that is independent of whether the transmitter and the receiver are synchronous or asynchronous.

## Settings

🔤 SSI Settings	×
Channel	
Select Channel Mode	
SCK A0 FS A1 DATA A2 Network	
Line Of Data	
Transmit      Receive	
Merge continuous unknown	
Color	
11 Hex	-
22 Hex	-
33 Hex	-
44 Hex	-
Range	
Decode Range	
From To	
Buffer Head 👻 Buffer Tail	•
ODefault ✔OK ¥Cance	el 🚽



Select Channel: Assign the signal pins of the Device Under Test (DUT) to the

corresponding channel numbers of the logic analyzer

Mode: Normal or Network.

Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

### Result

Click **OK** to run SSI decode and see the result on the Report Window below.

/Div= 200 us		341.27 ma		0.01.00														
		341.37 Ha	341.67 ma	341.77 ma	341.97 ma	242.17 ma	342.37 ma	342.67 ms	342.77 ma	342.97 ma	343.17 ma	343.37 ma		0.47 ma	343.77 ma	540.97 ma	344.17 ma	344.37 ms
•	75 00 1	00 B6 I	99 <b>00</b> 98	00 75 0	0 00 86	D9 <b>00</b> 98	08 75	00 00 56	D9 00	98 <b>00</b> 1	5 00 00	<b>E6</b> D9	00	98 00	75 00	00 BS	D9 00 9B	00 75 00 00
<b>3CK-A</b>	ω																	
F3-A1	4					389.95 vs		29.95 w										
DATA-	-A2 160 us		р9.95 ш	90 w	160 ==	руу 55 м []	»•	160 w	79.95 m	90 w	160 ==		79.94 w	90 00	160	•	N9.95 m	90 us 160 us
		Live																
100 100		Live																
el Chann		Live																
													_			Q Search Al	I Fields 💌 Text inc	
Bus SI(S	nel I		D1	D2	D3	D4	DS	Dé	D7	ASCI	;					Q Search A	I Fields 👻 Text inc	
Bus SSI(S: Timestamp	nel I				D3	D4	D5	D6	D7							Q Search Al	I Fields 💌 Text inc	
Bus SSI(S	nel I		D1 00 D9	D2 00 00	D3 98	00	D5	D6	D7	ASCII U						Q Search Al	I Fields 💌 Text inc	
Bus SSI(S: Timestamp 55.005us	nel I		00	00			DS	D6	D7	u						Q Search Al	I Fields Text inc	
Bus SSI(S) Timestamp 55.005us 294.955us	nel I	75 86 75 86	00 D9 00 D9	00			DS	D6	D7	u						Q Search Al	I Fields 💌 Text inc	
Bus         SSI(5)           Timestamp         55.005us           294.955us         694.905us           934.86us         1.33401ms	nel I	D0	00 D9 00 D9 00	00 00 00 00 00	98 98	00	D5	D6	D7	u u						C Search Al	I Fields 💌 Text inc	
55.005us 294.555us 694.505us 934.64us 1.33401ms 1.57476ms	nel I	D0 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9	00 00 00 00 00 00 00 00 00	98	00	D5	D6	D7	u u u						Q Search Al	I Fields 💌 Text inc	
55.005us 294.955us 694.955us 694.955us 934.64us 1.57476us 1.974715us	nel I	75 86 75 86	00 D9 00 D9 00 D9 00 D9 00	00 00 00 00 00 00 00	98 98 98	00 00 00	DS	D6	D7	u u u u u						Search Al	I Fields 💌 Text inc	
Bus \$51(52 Timestamp 55.005us 294.955us 934.86us 1.33401ms 1.57476ms 1.57476ms 2.214665ms	nel I	D0 75 86 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9	00 00 00 00 00 00 00 00	98 98	00	DS	D6	D7	U U U U U						Q Search Al	I Fields 👻 Text Inc	
Dimestamp           55.005us           294.955us           934.864us           1.33401ms           1.97476ms           2.24665ms           2.24665ms	nel I	D0 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9 00	00 00 00 00 00 00 00 00 00	98 98 98 98	00 00 00 00	DS	Dő	D7	U U U U U U U U						Search Al	I Fields 💌 Text Inc	
Bus         S SI(5)           Timestamp         55.005ua           254.505ua         654.505ua           934.640a         1.33401ma           1.57476ma         2.214655ma           2.214655ma         2.614457ma	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9 00 D9	00 00 00 00 00 00 00 00 00 00	98 98 98	00 00 00	DS	Dé	D7	U U U U U U U U						Q Search Al	I Fields 💌 Text Inc	
Bux         SSI(5)           Timestamp         5.005ue           294.395us         694.905us           934.85us         1.33401ms           1.57476ms         2.24465ms           2.24465ms         2.64415ms           2.65457ms         3.24452ms	nel I	D0 75 86 75 86 75 86 75 86 86 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00	00 00 00 00 00 00 00 00 00 00 00 00	98 98 98 98 98	00 00 00 00 00 00 00 00 00 00 00 00 00	DS	D6	D7	U U U U U U U U			_			Q Search Al	i Fields 💌 Text Inc	
Busy         Ssi(S)           Timestamp         5,005ar           95,005ar         94.8%           1,33401ms         1,33401ms           1,944.7415as         2,24465as           2,644615as         2,6447ms           3,2442ms         3,2442ms	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9	00 00 00 00 00 00 00 00 00 00 00 00 00	98 98 98 98	00 00 00 00	D5	Dő	D7	U U U U U U U U						C Search Al	I Fields 💽 Text inc	
State         State           1         Weak         SSI(S)           254.955us         254.955us         254.955us           264.955us         264.955us         264.955us           264.955us         264.955us         264.955us           27.9747bm         1.57476m         1.974715ms           2.224665ms         2.614615ms         2.65457ms           3.25452ms         3.45452ms         3.45447ms	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 00 D9 00 00 D9 00 00 00 00 00 00 00 00 00 0	00 00 00 00 00 00 00 00 00 00 00 00 00	55 58 58 58 55 58 58		DS	Dő	D7	U U U U U U U U						Search Al	I Fields 💌 Text Inc	
Year         SSI(5)           Timestamp         51.0050#           55.0050#         54.050#           694.850#         1.33401m           1.33401m         1.57476m           1.57476m         2.24465m           2.624652m         3.26452m           3.694427m         3.694427m           3.694427m         4.13477m	nel I	D0 75 84 75 84 75 86 75 86 75 86 75 86 75 86 75 86 75 86	00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 00 D9 00 00 00 00 00 00 00 00 00 0	00 00 00 00 00 00 00 00 00 00 00 00 00	98 98 98 98 98	00 00 00 00 00 00 00 00 00 00 00 00 00	DS	D6	D7	U U U U U U U U						C Search Al	I Fields 🛡 Text Inc	
Year         SSI(S)           Timestamp         55.0054ap           254.955as         694.955as           944.955as         694.955as           944.954as         694.955as           944.954as         694.955as           94.9745as         1.57476as           1.57476as         2.24465ms           2.65457ms         3.25452ms           3.69442ms         3.69442ms           4.19475as         4.54422ms           4.53422ms         4.53422ms	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86	00 D9 D9 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 00 D9 00 00 D9 00	00 00 00 00 00 00 00 00 00 00 00 00 00	95 98 98 98 98 95 98 98 98	00 00 00 00 00 00 00	DS	Dé	D7	U U U U U U U U						Q Search Al	I Fields 💌 Text Inc	
Bit         Deal         SSI(5)           Timestamp         55,0054#         294,9554#           294,9554#         694,9554#         694,9554#           944,854#         1,55476#         2,24457#           1,57476#         2,214650#         2,214657#           2,214657#         3,25492#         3,45447#           3,45442#         3,45442#         3,45442#           3,654425#         4,274275#         4,274275#	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 86	00 D9 D9 D9 D9 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9 00 D9	00 00 00 00 00 00 00 00 00 00 00 00 00	55 58 58 58 55 58 58		DS	D6	D7	U U U U U U U U						C Search Al	I Fields 🛡 Text Inc	
201 201 201 201 201 201 201 201	nel I	D0 75 84 75 84 75 86 75 86 75 86 75 86 75 86 75 86 75 86	00 D9 D9 D9 D9 D9 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00	95 98 98 98 95 98 98 98 98 98	00 00 00 00 00 00 00 00 00	DS	Dé	70	U U U U U U U U						C Search A	i Fields 👻 Text Inc	
00 C1 Vent (55155 00 C1 Vent (5515 00 C1	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 86 86	00 D9 D9 D9 D9 D9 D9 D9 D9 D9 D9 D9 D9 D9	00 00 00 00 00 00 00 00 00 00 00 00 00	95 98 98 98 98 95 98 98 98	00 00 00 00 00 00 00	DS	D6	70	U U U U U U U U						Q Search A	I Fields 💌 Text Inc	
001 011 011 011 011 011 011 011	nel I	D0 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 75 86 86	00 D9 D9 D9 D9 D9 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 00 D9 00 00 D9 00 00 D9 00 00 D9 00 00 00 00 00 00 00 00 00 00 00 00 00	00 00 00 00 00 00 00 00 00 00 00 00 00	95 98 98 98 95 98 98 98 98 98	00 00 00 00 00 00 00 00 00	DS	D6	07	U U U U U U U U						C Search A	i Fields 🔽 fait inc	



# ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

### Settings

🔤 ST7669 Ver. 1.3a Settings			×
Parameter		Color	
:=/			
Туре	8-bit Serial Interface	<b>•</b>	
Channel			)
Chip Select Channel (/CS) Clock Channel (SCL) Serial Data Input (MPU SI) Serial Data Input (LCD SI) A0	A0 A1 A2 A0 A3	D/C D/C Com Data	
Range			
From To Buffer Head To	Tail 👻		
	0	Default VOK	Cancel

#### Type, selectable options:

- 1. 8-bit Serial Interface
- 2. 8-bit Serial Interface + LCD SI
- 3. 9-bit Serial Interface
- 4. 9-bit Serial Interface + LCD SI

Chip Select Channel (/CS): CS for ST7669 data transmission.

Clock Channel (SCL): Clock for ST7669 data transmission.



Serial Data Input (MPU SI): MPU Data Input for ST7669 data transmission.Serial Data Input (LCD SI): LCD Data Input for ST7669 data transmission.A0 for ST7669 data transmission.

	Chip Seler	90 92 s	16.52 s 16.52 s	94.92 s	95.92 s		96.92 #	96.82 s	95.92.4	95.92 s	95.92 s	96.92 #	96.92 s	96.92 s	95.92.8	95.92 s
	Chip Selec	X07 05														
	Chip Selec					21	AFOR (23)	03	NOP	05				21	APON (23)	03
	Chip Selec															
317669 51																
	5C1-A1		1													
213	NPU SI-A2	6 = 4 = 9.99 =				4 m 7.99 m 1	6 m 6 m 6 m 11.	99 m 4 m1 m	9.9	»				 	w 6 w 6 w 6	m 11.99 m 4 m
5	LCD SI-AO			28.04 w								28.04 10				
\$17665																
<b>15 16</b>		OLive														
0	Channel															
Bus s	ST7669(ST766	9. C 🛄 📑	Þ										Q	Search All Fields	Text includes	EX.
	estamp	Data / Command	Data / Para	meter												
96.9216		mand	NOP													
96.9216	634295s Da 730325s Da		05													
96.9217	748326 00	mand	APON (23)													
	766315# Da		03													
96.9217		mand	NOP													
96.9218			05													
96.9218			21													
	916335# Co		APON (23)													
96.9219			03													
4 96.9219		mand	NOP													
5 96.9219 6 96.9220			05													
	066368 Da		21 NDOF (28)													

### Result



# SVI2

The SVI2 (Serial VID Interface 2.0) bus is a communication protocol used by AMD for power management control data transmission, typically applied in voltage control. SVI2 bus analysis allows users to view transmitted signal packets, reducing the time needed for waveform interpretation. It operates with a voltage range of 1V to 1.8V and a maximum frequency of 20MHz. The interface consists of three signal channels: SVC, SVD, and SVT. When measuring signals, it is important to set the trigger level between 0.6V and 0.9V to ensure stable signal triggering.

## Settings

SVI2 Rev 1.07 Settings		×
Channel Analysis Mode SVI2.x SVI1.x SVC A0	Color Start / Stop TFN VDD1 Load Line Slope Trim VDD2 Offset Trim	
SVD A1 SVT A2 Display SVD • SVT	VDDNB VDDNB VDV1 VDDNB VDDNB VDDNB VDDNB VDD1 Voltage / Current VDD2 Voltage / Current VD2 Voltag	
Range Decode Range From To Buffer Head To Buffer Tail	ODefaultOK€Cancel	

## Analysis Mode:

SVI2.x / SVI1.x: Select SVI2 / SVI decoding.

#### Channel:

**SVC:** Clock for transferred signal.

**SVD:** Data for transferred signal.



**SVT:** Telemetry Data Line for SVI2 data transmission. Only effective when the analysis mode is set to SVI2.x.

**Display:** Display SVD or SVT decoding results in the waveform area. The SVT option is only effective when the analysis mode is set to SVI2.x.

### Result

ne/Div= 200	ins ,			51 m	-17	1	-17.1 x	-17.1 #	-17.1 #	-17.1		-17.5 a	-17.1 a	-17.1 x	-17.1 #	-17.1 #	-12.1 x	-17.1 #	-17.1 #	-17.1 #	-17.1 #
		-		1																	
	A.0				_					لالالالا					450 m						
						# 110 mm		50 m 100 m	: 50 m 100 m	50 m <sup>50</sup> m 100 m	ar 150 m	100 -	= 100 as 50 as 10								
	A2															65 ns 50 ns 85					
	1																				
SVT(1)	A2:A0															Shet 1	,				
	21/2																				
	0																				
SVD(1)	A2:A0				Sta	t Coo	usteat; 18	0 1 C:0	A 1	VID: 2C	Δ.	1 0	3 1	E P							
								- i (													
	5V12									-											
																					_
15 1			OLiv	/e																	۰
Del	Channel	×	() Liv	/e																	
					•													Q	Search All Fields	Text include	95
	Channel Bus SVI2(1)(SV Timestamp	- /12) _ C		Ð		VID	TFN	Load Line Sk	ope Trim	Offset Tr	im \$	SVT1 SVT0	VDD1 Volt	VDD1 C	ury .	VDD2 Volt	VDD2 C			Text include	•5
90 -	Bus SVI2(1)(SV Timestamp 17.100667675a	1 //2) _ C		Ð	ISI1_L							SVT1 SVT0	VDD1 Volt	VDD1 C	urr	VDD2 Volt	VDD2 C	urr		irmation	
590 -	Bus SVI2(1)(S) Timestamp 17.108667675a 17.108249065a	12) _ C DIR V 570 0		Ð	ISI1_L	VID 75007 (20)		Load Line Sk					VDD1 Volt	VDD1 C		VDD2 Volt	VDD2 C	urr Tis	Info ne between Cmd	irmation	
690 - 691 - 692 -	Bus SVI2(1)(SV Timestamp 17.108667675s 17.108249065s 17.10824723s	1 //2) _ C		Ð	ISI1_L							ovti svto	VDD1 Volt	VDD1 C	urr	VDD2 Volt	VDD2 C	Umr Tin Vot	Info me between Cmd IF Complete	ermation and VOIF: 50.0:	50 us
590 - 591 - 592 - 593 -	Bus SVI2(1)(57 Timestamp 17.100667675s 17.100249065s 17.10024723s 17.10024723s			Ð	ISII_L	7500V (2C)		Initial LL 5	lope (3) Ini	tial Offset	-25 mV (		VDD1 Volt	VDD1 C		VDD2 Volt	VDD2 C	Umr Tin Vot	Info ne between Cmd	ermation and VOIF: 50.0:	50 us
690 - 691 - 692 - 693 - 694 -	Bus SVI2(1)(57 Timestamp 17.100667675s 17.100249065e 17.10024723s 17.10024723s	A2) C DIR V SVD 0 SVT 1		1	ISII_L			Initial LL 5		tial Offset	-25 mV (		VDD1 Volt	VDD1 C		VDD2 Volt	VDD2 C	Urr Tin VO: Tin	Info me between Cmd - IF Complete me between Cmd -	ermation and VOIF: 50.0:	50 us
590 - 591 - 593 - 594 - 595 -	SVI2(1)(SV Timestamp 17.1066676758 17.106249258 17.106247238 17.106247238 17.107913788	A2) C DIR V SVD 0 SVI SVI 1 SVI 1		1	ISII_L	7500V (2C)		Initial LL 5	lope (3) Ini	tial Offset	-25 mV (	0	VDD1 Volt	VDD1 C		VDD2 Volt	VDD2 C	Uurr Tin VO: Tin VO:	Info me between Cmd IF Complete	and VOTF: 50.03	50 us 5 us
690 - 691 - 692 - 693 - 694 - 695 - 695 - 696 - 697 -	Timestamp 17.108667675a 17.108249068a 17.10824723a 17.107913778a 17.107962235a 17.107862235a 17.10786235a	AI2) CIR V DIR V SVD 0 SVT SVT SVT SVT SVT 1		1	USI1_L	7500V (2C)	0	Initial LL 5	lope (3) Ins	tial Offset	-25 xV ( 1 (set (2)	0	VDD1 Volt	VDD1 C	urr I	VDD2 Volt	VDD2 C	Vot Tis Vot Tis	Info me between Cmd IF Complete me between Cmd IF Complete me between Cmd	and VOTF: 50.03	50 us 5 us
590 - 591 - 592 - 593 - 595 - 595 - 595 - 596 - 597 - 598 -	University of the second secon	DIR V     SVD 0     SVD 1     SVD 1     SVD 1     SVD 1     SVD 1     SVT		PSI0_L	USI1_L	7500V (2C) 1250V (66)	0	Initial LL 5	lope (3) Ins	tial Offset	-25 xV ( 1 (set (2)	0	VDD1 Volt	VDD1 C	urr	VDD2 Volt	VDD2 C	Vor Tis Vo: Tis Vo: Vo: Vo: Vo:	Info me between Cmd - IF Complete me between Cmd - IF Complete me between Cmd - IF Complete	and VOTF: 50.0	50 us 5 us 45 us
690	Timestamp 17.108667675a 17.102490656 17.10247238 17.10247238 17.107913786 17.10766235a 17.10766138 17.107660156	DIR V SVD 0 SVD 0 SVT 1 SVT 1 SVT 1 SVT 1	2 DD1 VDD2 1 1 . 0	2 PSIO_L 2	ISI1_L 1.2 0 0.5	7500V (2C) 1250V (66) 1250V (66)	0	Initial LL 5 Initial LL 5 Initial LL 5	lope (3) Ind lope (3) Use	s Initial Offset	-25 mV (] fact (2) fact (2)	0	VDD1 Volt	VDD1 C	JIT	VDD2 Volt	VD02 C	Vor Tis Vo: Tis Vo: Vo: Vo: Vo:	Info me between Cmd IF Complete me between Cmd IF Complete me between Cmd	and VOTF: 50.0	50 us 5 us 45 us
690 - 691 - 692 - 693 - 694 - 695 - 696 - 696 - 698 - 698 - 699 - 700 -	Timestamp 17.102667675a 17.102490656 17.10247238 17.10247238 17.10762235a 17.10766135a 17.107660115a 17.1077600115a	A(2)     C     DIR V     SVD     SVD	2 DD1 VDD2 1 1 . 0	PSI0_L	ISI1_L 1.2 0 0.5	7500V (2C) 1250V (66)	0	Initial LL 5	lope (3) Ind lope (3) Use	s Initial Offset	-25 mV (] fact (2) fact (2)	0	VDD1 Volt	VDD1 C	ut	VDD2 Volt	VDD2 C	Uurr Tin Voi Tin Voi Tin Voi Tin	Info me between Cmd IF Complete me between Cmd IF Complete me between Cmd IF Complete me between Cmd	and VOTF: 50.0	50 us 5 us 45 us
H-00         0           690         -           691         -           692         -           693         -           694         -           695         -           696         -           697         -           698         -           699         -           700         -           7701         -	Timestamp 17.108667675a 17.102490656 17.10247238 17.10247238 17.107913786 17.10766235a 17.10766138 17.107660156	A(2)     C     DIR V     SVD     SVD	2 DD1 VDD2 1 1 . 0	2 PSIO_L 2	ISI1_L 1.2 0 0.5	7500V (2C) 1250V (66) 1250V (66)	0	Initial LL 5 Initial LL 5 Initial LL 5	lope (3) Ind lope (3) Use	s Initial Offset	-25 mV (] fact (2) fact (2)	0	VDD1 Volt	VDD1 C	urr	VDD2 Volt	VDD2 C	Uurr Tis Voo Tis Voo Tis Voo Tis Voo Tis Voo Tis Voo	Info me between Cmd - IF Complete me between Cmd - IF Complete me between Cmd - IF Complete	ermation and VOTF: 50.0: and VOTF: 0.33: and VOTF: 50.0 and VOTF: 0.31:	50 us 5 us 45 us 5 us



# SWD

SWD (Serial Wire Debug) is a test protocol defined by ARM, consisting of two signal lines: SWDIO and SWDCLK. It serves as a debug access protocol for CoreSight<sup>™</sup> Debug Access Port and is an alternative to JTAG when there are pin count limitations.

## Settings

Parameter Settings Channel Setting SWDIO A1 SWDI	SWD Parameter Settings		×
SWDIO       A1         SWDIO       A1         SWDCLK       A0         Enable Glitch Filter       JTAG-AP         AP Select Reg Startup       MEM-AP         Bank 0       Show AP Reg bit assignments         MEM AP Startup       MEM AP Startup	arameter Settings		
SWDIO       A1         SWDIO       A1         SWDCLK       A0         Enable Glitch Filter       JTAG-AP         AP Select Reg Startup       MEM-AP         Bank 0       Show AP Reg bit assignments         MEM AP Startup       MEM AP Startup			
SWDIO       A1       Image: Construct of the construction	Channel Setting	Show DP Reg bit assignments	Filter Setting
SWDCLK A0       Image: Other       Im	SWDIO A1	AP Setting	Register Display List
SWDCLK A0       Image: Construction of the con		Other	
AP Select Reg Startup OMEM-AP I DP - CTRL/STAT Register			
□     Bank 0     ●     MEM AP Startup       ■     MEM AP Startup			
Bank 0 MEM AP Startup	AP Select Reg Startup		
memory otartap	Bank 0		✓ DP - WCR Register
CtrlSel 0	CtrlSel 0		DP - SELECT Register
Endian Big  DP - RESEND Register		Endian Big 👻	✓ DP - RESEND Register
Bit Order TAR Auto-Inc Off  DP - ROUTESEL Register	Bit Order	TAR Auto-Inc Off 👻	✓ DP - ROUTESEL Register
● LSB First Access Size 32 Bits ▼ DP - RDBUFF Register	<ul> <li>LSB First</li> </ul>	Access Size 32 Bits 👻	✓ DP - RDBUFF Register
O MSB First	O MSB First		d An Percented
Ap - Reserved			
Color Range	Color	Ra	nge
Decode Range			Decode Range
Start Park From To	Start		r 1
Buffer Head Tail			Buffer Head 👻 Buffer Tail 👻
RnW • ACK •	RnW	ACK	
Addr Data	Addr	Data 🗾	
Stop   Parity	Stop	Parity	
☐Default ✔OK ¥Cance			ODefault ✔OK ★Cancel

SWDIO: I/O data.

SWDCLK: Clock.



-AP Select Reg Startup												
Bank = 0		Time		Sele	ect	RnW	Address	(h)	ACK	Data		
	9	-0.0003	ms	AP		Write	0		OK	23 00	00	52
CtrlSel = 0	÷											
-												
- AP Select Reg Startup												
Bank = 0		ime	Sel	ect	RnW	Address	(h)		ACK	Data		
		.0003 ms	AP		Write	Bank 0	Register	0 (0)	OK	23 00	00	52
CtrlSel = 0												

Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

Select	RnW	Address (h)	ACK	Data	
DP	Write	SELECT Register (8)	OK	00 00 00 00	
				APSEL [31:24]	00
				APBANKSEL [7:4]	0
				CTRLSEL [0]	0

AP Setting: You can select between MEM-AP and JTAG-AP for AP Register

decoding. If the user selects Other, the AP data will only display as Bank X

Register X without further interpretation.

**JTAG-AP:** Show the JTAG AP decode.

**MEM-AP:** Show the MEM AP decode.

Other: Show Bank X Register X.

Other	Time	Select	RnW	Address (h)	ACK	Data
C JTAG-AP	-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	OK	23 00 00 52
C MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	Bank 0 Register 1 (4)	OK	00 00 02 68
O Other	Time	Select	RnW	Address (h)	ACK	Data
• JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	ок	23 00 00 52
C MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	PSEL Register (4)	OK	00 00 02 68
O Other	Time	Select	RnW	Address (h)	ACK	Data
○ JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
• MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
S PIEPFAF	2.9998 ms	AP	Write	TAR Register (4)	OK	00 00 02 68

Show AP Reg bit assignments: Display the AP register information if

JTAG-AP or MEM-AP checked.



MEM-AP	Select	RnW	Address (h)		ACK	Data	
Show AP Reg bit assignments	AP	Read	BASE Register	(8)	OK	00 00 00 00	
						BASEADDR [31:12]	EOOFF
						Format [1]	1
						Entry present [0]	1

MEM AP Startup: When selecting MEM-AP, the contents of MEM-AP can be

initialized. During data capture, if a corresponding register address is

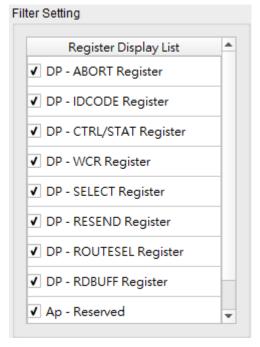
encountered, the data will be updated according to the bus content. Enabling

the Endian checkbox activates the display of data along with the corresponding

read/write addresses.

۰.	IEM-AP		AP	Read	DRW Register	(C)	OK	00 00 00 0D	TAR Address = E000EFF0
	Show AP Reg bit as	ssignments						Big-Endian	
	MEM AP Startup -							000D Access to E000EFF0	
	🔽 Endian	Big 💌						0000 Access to E000EFF2	
	,		AP	Read	DRW Register	(C)	OK	00 00 00 E0	TAR Address = E000EFF2
	TAR Auto-Inc	Single 💌						Big-Endian	
	Access Size	16 Bits 💌						00E0 Access to E000EFF2	
	1							0000 Access to E000EFF4	

Filter Setting: Filter the unwanted Registers.





### Result





# SWIM

SWIM is the single wire interface module of STM8 8-bit MCUs family. While the CPU is running, the SWIM allows a non-intrusive read/write accesses to be performed on-the-fly to the RAM and peripheral registers, for debug purposes.

## Settings

📇 SWIM Settings	×
Parameter	Color
	Reset v pulse (1Khz)
Channel	pulse (2Khz)
Swim pin A1	Header  Command  Data
Display format Byte 👻	Parity Error 🗾
✓ Detail Report	NACK 🗾
Range Decode Range	
From	
Buffer Head	▼ Buffer Tail ▼
Def	ault VOK XCancel

Swim pin: set the Swim Channel.

Rst pin: set the Reset Channel.

Display format: the display method of waveform decode (Byte, Bit).

Detail Report: show the detail information of SWIM decode.



## Result

## Normal

NDiv=20 us	*	3.40 s		1.43 s		3.43 5		3,43			3.4D s		01	3.43 s	3.43		3.43 s	3.40 s		0.4D s		2.40 s	3.4		0.40 s		3.43 5		40 s
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· ·																													
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Chane Bus Swim Timestamp Dpa	nel I		8 🕨	1 A2	DO	D1	D2 [	)3 D4	4 D5	Dő	P	arity Erro	2			In	formation							(	CSearch A	J Fields	Text inclu	ides	
Channel Bus swime Timestamp Opa Opa	nel (SWIM) Command		8 🕨	I A2	DO	D1	D2 [	03 D4	4 D5	Dő	P	arity Erro = NACK /	z No ACK			In	formation							(	L Search A	I Fields	Text inclu	ides	
Chan Bus swam Timestamp Ops 0ps 3.369791435s	nel (SWIM) Command	Len(Dec)	A0 A1			D1	D2 D	03 D4	4 D5	D6	P	arity Erro = NACK /	e So Ack			In	formation							(	L Search A	I Fields	Text inclu	ides	
Chan Bux swam Dps 0ps 3.369751435s 3.399621335s	nel (SWIM) Command SR5T (0) WOTF (2)	Len(Dec)	A0 A1	80	AO	D1	D2 0	03 D4	4 D5	Dő	P	arity Erro = NACK /	z Bo ACK			In	formation							(	Cearch A	Il Fields	Text inclu	ides	
Chane Chane Constant Co	nel ( (SWIM) C Command SRST(0) WOTF(2) WOTF(2)	Len(Dec)	A0 A1	80	A0 08	D1	D2 [	23 D4	4 D5	Dő	P	arity Erro = NACK /	s Bo ACK			In	formation							(	C Search A	Il Fields	Text inclu	ides	
Chann Channel Chane	nel ( A(SWIM) Command SRST(0) WOTF(2) WOTF(2)	Len(Dec)	A0 A1 00 77 00 77 00 77 00 50	80 99 62	A0 08 56	D1	D2 D	D3 D4	4 D5	D6	P	arity Erro = NACK /	s Bo ACK			Ir	formation							(	C Search A	I Fields 💽	Text inclu	ides	
Chane Dps Ops 0,369751435s 3,369751435s 3,399621335s 3,420269343s 3,42029343s 3,42152833s	A(SWIM) Command SRST (0) WOTF (2) WOTF (2) WOTF (2) WOTF (2)	Len(Dec)	A0 A1 00 77 00 77 00 77 00 50	80	A0 08 56 AE	D1	D2 0	D3 D4	4 D5	D6	P	arity Erro = NACK /	s Bo ACK			In	formation							(	Search A	JI Fields 💽	Text inclu	ides	
Chane	nel (  KSWIM)  Command  SRST(0)  WOTF(2)  WOTF(2)	Len(Dec)	A0 A1 A0 77 00 77 00 77 00 50 00 50	80 99 62 62	A0 08 56 AE 01 CD	FE	D2 0			D6 CC		arity Erro = NACK /	s So ACK			In	formation		-					(	L Search A	Il Fields 💽	Text inclu	ides	
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Channel Switch Timestamp Ops 098 098 098 098 098 098 098 098 098 098	rel (SWIM) Command Command SRST (0) WOTF (2) WOTF (2) WOTF (2) WOTF (2)	Len(Dec)	A0 A 00 72 00 72 00 72 00 50 00 50 00 50	80 99 62 62 58	A0 08 56 AE 01 CD 80 68	FE SO CC	BC 43	A 26 4 52	03	CC A6 02	91 00 87	arity Erro = DACK /	e Bo ACK			In	formation							(	Search A	JI Fields 💽	Text inclu	ides	
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## **Detail Report**

Div= 20 us	~	3.43 s	3.		3.43 5	3.43 s	37	3.40 s 3.43 s 3.43 s 3.43 s 3.43 s 3.43 s 3.43 s 3.43 s 3.43 s	i 0.40 s 0.40 s
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Buck swill Timestamp Ops Ops 3.369791435s 3.399621335s 3.420663s	Annel Command Command SSST(0) WOTT(2)	Len(Dec)	A0 A1	80 A0		2 D3 D4 (	DS D6 D	bifumation bifumation set of the	AN Fands Thet Includes
Timestamp Ops Ops 3.36979.1435s 3.36979.1435s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.4200603s 3.4200603s	Annel Command SKST(0) WOTF(2)	Len(Dec) 1 01	A0 A1	59 08		2 D3 D4 (	DS D6 C	biomedion biomedia biomedion biomedion biomedione bio	•
Bus         swii           Timestamp         Ops           Ops         3.369791435s           3.399021335s         3.399021335s           3.399021335s         3.399021335s           3.399021335s         3.399021335s           3.399021335s         3.399021335s           3.399021335s         3.399021335s           3.399021335s         3.400603s           3.4200603s         3.4200603s           3.4200603s         3.4200603s           3.4200603s         3.4200403s	Annet  Annessee Annes	Len(Dec)	A0 A1	50 A0 59 08 62 56		2 03 04 0	DS D6 C	bifumation bifumation starts register information (2000) HIGK / SD ACK MERK / SD ACK MERK / SD ACK MERK / SD AC	AN Tracks Dat Includes o
Timestamp Ops Ops 3.36979.1435s 3.36979.1435s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.39962.1335s 3.4200603s 3.4200603s	Annel Command SRST(0) WOTF(2) WOTF(2) WOTF(2)	Len(Dec) 1 01	A0 A1	59 08		2 D3 D4 (	D5 D6 C	bifumation bifumation starts register information (2000) HIGK / SD ACK MERK / SD ACK MERK / SD ACK MERK / SD AC	AN Faces Test includes a



# SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

## Settings

🚢 SWP :	Settings		×
Channel			
1	S1 S2 Data Link Layer:	A0	
Color			
	SOF / EOF Payload CRC16		
Range			
From Buffer	Decode Range To r Head 💌 E	Buffer Tail 🔹	
	Default	OK XCancel	

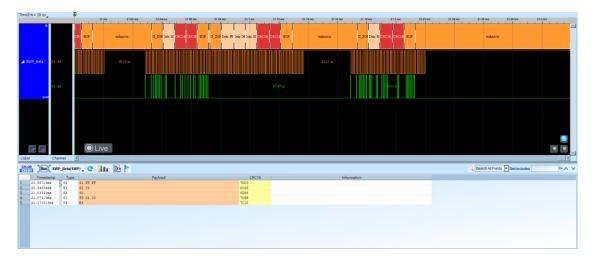
- **S1**: I/O data.
- **S2**: I/O data in current domain and it need convert to voltage domain.

Data Link Layer: Supported MAC and LLC layers



## Result

## MAC



## LLC

e/Div= 20 us	2	21 ms 21,02 ms 21,04 ms 21,06 ms 21,08 ms	21.1ms 21.12ms	21.14 ms 21.10 ms 21.10 ms	21.2 ms 21.22 ms 21.2	4me 21.26 me 21.29 me 21.31	ma
0	CR	BOF waknown 22,009 Jan. 65 CRC16 (2001) 809 11,000 Day. F9	Dete: 04 Dete: 00 CRC16_CRC16_BDF	mikaowa 12,000 Den: B CRC1	6.CRC16 BOF	minova	
SWP_Beta \$1	ы м	28.50 m		72.13 m			
32 - J	u				i63 u		
<b>B</b> \$ <b>B</b> \$		OLive					•
	nnel !						
Bus SW	P_Beta(SWP	. C 🛄 🖻 🏲				Q Search All Fields Text Includes	EX 🔨
Timestamp	Type	Payload	CRC16	Information			
20.88719ms		61 FF FF	7DC8				
20.88719ms		ACT LPDU					
20.88719ms		INR(0): Contains the ACT_INFORMATION info					
20.00719ms	5 C	ACT_SYNC(001): 0xffff					
20.94634ms 20.94634ms	51	<2 01 ACT LPD0	6066				
20.94634ms		FR(0): The UICC shall not repeat the last ACT frame					
20.94634ms		ACT_POWER_MODE(010): Full power(01)					
		60	8056				
		ACT LPDU					
21.03343ms							
21.03343ms 21.03343ms							
21.03343ms 21.03343ms 21.03343ms 21.03343ms		ACL LPDO INE(0): Contains the ACT_INFORMATION info ACT_READY(000) from UICC					
21.03343ms 21.03343ms 21.03343ms		INR(0): Contains the ACT_INFORMATION info	7098				



# TDM

TDM Audio (Time Division Multiplexing Audio) is a method for transmitting multiple audio channels over a single data line (or a pair of data lines) by dividing the transmission content into multiple time slots. This technique is widely used in digital audio systems to efficiently manage and transmit multiple audio streams, particularly in professional audio, consumer electronics, and automotive applications.

## Settings

🚐 TDM Settings	×
Channel	Mode Select
Clock(SCK) A0 C Word Select(WS) A1 C Data(SD) A2 C	Slot Width Mode
Audio Settings	Range
Slot bits16 bit(s)Audio bits:16 bit(s)Audio bits:16 bit(s)Channel Count2Latch EdgeFallingEnable PulseHighData Offset0 bit(s)LSB FirstSave as CSV file	From To   Buffer Head Buffer Tail   Sound Reduction(Max Ch. = 8)     Display the audio waveform   Save as WAV file   Align common sampling rate   Playback     Image: All image: Save as in the same interval of the s
	○Default ✓OK ★Cancel



Channel: The signal pins of the Device Under Test (DUT) are assigned to the

channel numbers of the logic analyzer.

**Option:** Adjust the detailed settings of the audio signal.

**Slot bits:** Data width of an audio channel.

Audio bits: Valid bits in the slot bits.

Channel Count: Number of audio channels (e.g., 2, 4, 8)

Latch Edge: Choose which clock edge to latch data (Rising or Falling)

**Start Pulse:** Set the polarity of the active pulse (High or Low)

Data Offset: Bit offset before starting data capture

**LSB First:** Check this if the data is transmitted with LSB first

Save as CSV file: Save the decoded result as a .CSV file

Mode: Set the data arrangement format. The following formats are currently

supported:

Slot Width Mode	
Slot Width Mode	
Bit Width Mode(Left Align)	
Bit Width Mode(Right Align)	
Bit Width Mode(Middle Align)	
I2S Mode(Standard)	
I2S Mode(Left Align)	
I2S Mode(Right Align)	

Sound Reduction: Set whether to save, replay, or visualize the audio

waveform based on the analysis results after decoding. Enabled when selected.

- Display the audio waveform
- Enable meet full scale
- Save as WAV file
- Align common sampling rate
- Playback: Choose to play all, 5 seconds, or 3 seconds



# Result

ime/Div= 10 us	۰,	-	32.5	, 4	3 44	12.3 ci	02.3 us	72	1.3 wi	82.3 ur	92.5 us 192	605.035us	2.3 44 122.5	ius 192.3	us 142	.3 us 152.3 u	ai 112.3 va	172.0 us	182.3 us	
1	•	CH2	coh da	II.CIN	CH2:41h	CH1:41h	CE	2.C1h	CHICZA	CH2:42h	CH1:42h	CH2 C2h	CB1.C3h	CH2:43h	CH1:43h	CH2.C3h	CB1.C4h	CH2:44h	CE1:44h	CH2:C4),
BUS_TDM	5CK-0																			
	WS-1										19.		193			9.57 m	19.4			
	DATA-2		6	45 us	6.47 w	6.45 m	4 100 6.4	17 10: 3.921	m 5.2 m	5.2 m	52 w	52 m	250 52m 26m	5.2 w	5.03 5.	25 w 5.2 w 5.4	·	3.98 us 3.9 u	3.67 m	3.89 m
T	TOM .		O Live																	
Label	Channe																			•
CH-00 )Bu	US BUS_T	el 💽 DM(TDM) 🖕	C III															Il Fields 💌 Text in	cludes	
EH-00 Bu	us BUS_T	H I			D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15	D16		formation	Il Fields 💌 Text in	cludes	× •
H-00 Bu	us BUS_T	н <u>.</u> DM(TDM) _ D1	C 111		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 👻 Text in	cludes	×
H.00 )Bu Tim -60ns 18.730	us BUS_T	DM(TDM)	C		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15			formation	Il Fields 💌 Text in	cludes	× ~
H-00 Bu	us BUS_T	DM(TDM) D1 CH1: 40 CH1: C1 CH1: 41	C 11 D2 CH2: C0 CH2: 41 CH2: C1		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 💌 Text in	cludes	×
-60ns 18.730 39.530 60.330 81.130	us BUS_T nestamp Us Us Us	DM(TDM) U D1 CH1: 40 CH1: C1 CH1: 41 CH1: C2	C D2 D2 CH2: C0 CH2: 41 CH2: C1 CH2: 42		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 💌 Text in	cludes	<u>~</u> ^
CH-00 (Bu -60ns 18.730 60.330 81.130 101.93	nestamp US US US US US US US	DM(TDM) U D1 CH1: 40 CH1: C1 CH1: 41 CH1: C2 CH1: 42	C D2 CH2: C0 CH2: C1 CH2: C1 CH2: C1 CH2: C2		D4	D5	D6	D7	DS	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 💌 Text in	cludes	<u>.</u> ~ ∧
-60ns 18.73u 39.53u 60.33u 81.13u 101.93 122.73	nestamp US US US US US SUS	DM(TDM) U D1 CH1: 40 CH1: 41 CH1: 41 CH1: 62 CH1: 42 CH1: 63	CH2: C0 CH2: C1 CH2: C1 CH2: 41 CH2: C2 CH2: 42 CH2: C2 CH2: 43		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 🖤 Text in	cludes	×
CH.00 XBu -60ns 18.73u 39.53u 60.33u 81.13u 101.93 122.73 143.53	BUS_T nestamp US US US US SUS SUS SUS	CH1: 40 CH1: 40 CH1: C1 CH1: 41 CH1: C2 CH1: 42 CH1: C3 CH1: C3 CH1: 43	C D2 CH2: C0 CH2: C1 CH2: C1 CH2: C2 CH2: C2 CH2: C3 CH2: C3		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 🛡 Text in	cludes	
CH.00 XBu -60ns 18.730 39.530 60.330 81.130 101.93 122.73 143.53 164.33	US US US US US US SUS SUS SUS	CH1: 40 CH1: 40 CH1: C1 CH1: 41 CH1: C2 CH1: C3 CH1: C3 CH1: C4	C D2 CH2: C0 CH2: C1 CH2: C1 CH2: C2 CH2: C2 CH2: C3 CH2: C3 CH2: C4		D4	D5	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields Text in	cludes	<u>×</u> ⊇∝ ∧
-60ns -60ns 18.73u 39.53u 60.33u 81.13u 101.93 122.73 164.33 0 185.13	BUS_T nestamp US US US SUS SUS SUS SUS SUS	DM(TDM) D1 CH1: 40 CH1: C1 CH1: C1 CH1: C2 CH1: C2 CH1: C3 CH1: C3 CH1: C3 CH1: C4 CH1: C4 CH1: C5	CH2: C0 CH2: 41 CH2: C1 CH2: C1 CH2: C2 CH2: C2 CH2: C3 CH2: C3 CH2: C3 CH2: C4 CH2: C		D4	DS	D6	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields Text in	cludes	<u>×</u>
-60ns 18.73u 60.33u 60.33u 81.13u 101.99 143.53 164.33 0 185.13 1 205.93 2 226.73	US BUS_TI nestamp 123 125 125 125 125 125 125 125 125 125 125	CH1 40 CH1: 40 CH1: 40 CH1: 41 CH1: 42 CH1: 42 CH1: 42 CH1: 43 CH1: 43 CH1: 44 CH1: 45	CH2: CD2 CH2: C0 CH2: C1 CH2: C1 CH2: C1 CH2: C2 CH2: C2 CH2: C3 CH2: C4 CH2: C4 CH2: C4 CH2: C4 CH2: C4 CH2: C4 CH2: C4 CH2: C4		D4	D5	D6	D7	Dê	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 💌 Text in	Cludes	<u>×</u>
CH.00 XBU -60ns 10.730 23,530 60.330 101.99 122.73 143.55 164.33 0 185.13 1 205.99 2 226.73 3 247.53	US BUS_TI nestamp 10 13 14 14 15 15 15 15 15 15 15 15 15 15	H         I           DM(TDM)         D1           D1         CH1: 40           CH1: 40         CH1: 41           CH1: 41         CH1: 42           CH1: 42         CH1: 43           CH1: 43         CH1: 44           CH1: 45         CH1: 45	C D2 CH2: C0 CH2: 41 CH2: 41 CH2: 42 CH2: 42 CH2: 43 CH2: C3 CH2: 44 CH2: C4 CH2: C4 CH2: C4 CH2: C4 CH2: C4 CH2: C4		D4	D5	D6	D7	Dê	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields Text in	cludes	× •
CH.00         Xee           -#0ns         18-73           18-73         39.53           101.93         12.73           101.93         124.73           101.93         124.73           101.93         124.73           101.93         124.73           101.93         124.73           120.73         124.73           120.73         226.73           247.53         247.53           4         246.33	BUS_TI nestamp 11 12 12 12 12 12 12 12 12 12	H 1 DM(TDM) D D1 CH1: 40 CH1: C1 CH1: 41 CH1: 42 CH1: 42 CH1: 42 CH1: 42 CH1: 42 CH1: 42 CH1: 42 CH1: 44 CH1: 44 CH1: 45 CH1: 46	C D2 CH2: 41 CH2: 41 CH2: 42 CH2: 42 CH2: 42 CH2: 43 CH2: 43 CH2: 44 CH2: 46 CH2: 46 C		D4	D5	D6	D7	D8	D9	D10 D11	D12	D1â D	14 D15		Sample Rate: 40.	formation	Il Fields Text in	cludes	× •
Image: system         Image: system           1         -Cons           2         16.73u           4         60.33u           5         81.13u           5         101.93           7         122.73           8         143.53           9         164.33           10         15.13           12         226.73           13         247.52           14         269.93           15         259.13	US BUS_T nestamp 10 10 10 10 10 10 10 10 10 10	H         I           DM(TDM)         D1           D1         CH1: C1           CH1: C1         CH1: C1           CH1: C1         CH1: C2           CH1: C2         CH1: C4           CH1: C4         CH1: C4	C D2 CH2: 41 CH2: 41 CH2: 42 CH2: 42 CH2: 43 CH2: 44 CH2: 44 CH2: 45 CH2: 45 CH2: 46 CH2: 47		D4	D5	Dé	D7	De	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields Text in	cludes	<u>∢</u>
CHOO         Tem           -Cons         2           18.733         460.330           59.5334         60.330           60.10.99         7           7         122.79           11         205.93           12         226.73           13         235.93           14         264.33           15         259.13           16         209.83	US BUS_T nestamp 11 12 12 12 12 12 12 12 12 12	H 1 DM(TDM) D1 CH1: 40 CH1: 40 CH1: C1 CH1: 41 CH1: 42 CH1: 42 CH1: 43 CH1: 43 CH1: 44 CH1: C5 CH1: 45 CH1: 45 CH1: 45 CH1: 46 CH1: 47	C D2 CH2: C0 CH2: 41 CH2: C1 CH2: C2 CH2: C2 CH2: C3 CH2: C3 CH2: C4 CH2: C4 CH2: C3 CH2: C4 CH2: C5 CH2: C6 CH2: C6 CH2: C6 CH2: C6 CH2: C7 CH2: C7		D4	DS	Dé	D7	D8	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	Il Fields 👻 Text in	cludes	* ^ *
CHOOL         Tem           1         -COAS           2         18,73u           3         95,53u           4         60,33u           5         81,13u           5         81,13u           7         122,73           3         143,55           9         143,55           9         144,55           10         125,131           12         226,733           13         247,553           14         264,035           15         289,13           16         05,92           7         30,77	Image: Second	H 4 DM(TDM) CH1: 40 CH1: 40 CH1: C1 CH1: C1 CH1: C2 CH1: C2 CH1: C3 CH1: C3 CH1: C3 CH1: C4 CH1: C3 CH1: C4 CH1: C4 CH1: C4 CH1: C3 CH1: C4 CH1: C4	C D2 CH2: C0 CH2: C1 CH2: C1 CH2: C1 CH2: C2 CH2: C3 CH2: C3 CH2: C4 CH2: C		D4	DS	Dé	D7	Da	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	II Fields 💌 Text in	cludes	∝ ∧
CHOO         Tem           -Cons         2           18.733         460.330           59.5334         60.330           60.10.99         7           7         122.79           11         205.93           12         226.73           13         235.93           14         264.33           15         259.13           16         209.83	Image: state	H 1 DM(TDM) D1 CH1: 40 CH1: 40 CH1: C1 CH1: 41 CH1: 42 CH1: 42 CH1: 43 CH1: 43 CH1: 44 CH1: C5 CH1: 45 CH1: 45 CH1: 45 CH1: 46 CH1: 47	C D2 CH2: C0 CH2: 41 CH2: C1 CH2: C2 CH2: C2 CH2: C3 CH2: C3 CH2: C4 CH2: C4 CH2: C3 CH2: C4 CH2: C5 CH2: C6 CH2: C6 CH2: C6 CH2: C6 CH2: C7 CH2: C7		D4	D5	Dé	D7	De	D9	D10 D11	D12	D13 D	14 D15		Sample Rate: 40.	formation	II Fields 🛡 Text in	cludes	× ~



# UART(RS-232, RS485)

It is a serial data communication interface standard established by the Electronic Industries Alliance (EIA) in the United States. In the RS-232 and RS-485 standards, characters are transmitted sequentially as a series of bits in a serial manner. The advantages of this method include fewer transmission lines, simpler wiring, and longer transmission distances. Since RS-485 uses differential signaling, the signal must be converted into a logic signal before measurement. The logic analyzer (LA) cannot directly measure differential signals.

## Settings

UART Set	ttings				×
Paramet	er Channel Tx CH 1 Rx CH 1	• •		Waveform Area Settings Show Scale Decode Tx	
	Format Auto Detect Baud Rate 115200 Parity None V	Polarity Idle high V Data Bits 8 V	Stop Bits 1 ×	Report Area Settings         Idle, Break Line Wrap         Show ASCII Only         Report Size         16         Line Wrap (<= 8Bits)	
	MSB First	Invert Bits	Show S/P	Range From To Buffer Head V Buffer Tail V Default OK Cancel	

# Channel:

**Tx:** Assign the Tx signal pin to the corresponding channel number of the logic analyzer.

**Rx:** Assign the Rx signal pin to the corresponding channel number of the logic analyzer. Enabled when selected.



**Auto:** Automatically detect the settings for the following options. Enabled when selected.

Baud Rate: The data transmission speed, measured in bits per second

(bps). The supported range is 110 to 2M bps.

**Polarity:** Includes Idle High and Idle Low formats.

Parity: Includes N - None Parity (No parity bit), O - Odd Parity, and E -

Even Parity.

Data Bits: Can be set between 4 to 16 bits.

**Stop Bits:** Can be set to 1, 1.5, 2, 2.5, 3, 3.5, 4, or 4.5 bits.

**MSB First:** When selected, the Most Significant Bit (MSB) comes after the Start Bit. When not selected, the Least Significant Bit (LSB) is used.

Invert Bits: Reverses High and Low levels. Enabled when selected.

**Show S/P:** Displays Start and Stop in the waveform area. Enabled when selected.

## Waveform Area Settings:

**Decode:** Select whether to display the Rx or Tx decoding results in the waveform area. The Rx option is only effective when the Rx channel is enabled.

**Show Scale:** Displays the scale in the waveform area. Enabled when selected.

# Report Area Settings, enabled when selected:

**Idle, Break Line Wrap:** When the bus Idle/Break, the report is displayed on a new line.

Show ASCII Only: Show only ASCII reports.

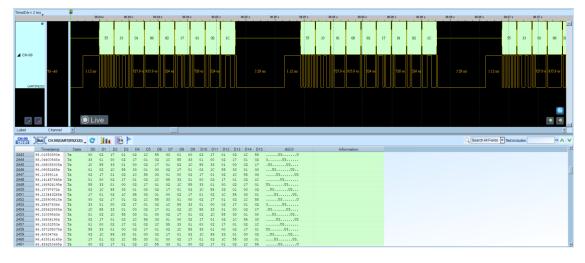
**Report Size:** Sets the number of Data fields in the report area. Can be set to 16 or 32.

**Line Wrap Data:** Allows setting two values as the primary order for decoding, making it easier to view analysis results.



## Result

# Normal Data Analysis Displaying



# Enable Line Wrap Data Analysis Displaying

me/Div= 2	ms "	*	95	04 s	95	.04 s	95.	14 s	95.	04 s	95.05 s		95.05 s	95.05 s	95.05 s	95	.05 s	95.	.06 s	95	06 s	95.00	) s	96.06 s	96.06 s	96.07	5	06.07 s	
d CH-00	69 Tx-A0 85225		1.12 ===	55	33	01	00	524	17	01 728 w	02	1C	J 29 m	1.12 m	55	33	01 727.9 a	00 935.9 m	02 524 w	17	01 728 w	02 524 m	1C	3 29 m	•	55 1.12 mu	33	01 727.9 u	00 22 935.9 m
	14	(	🛈 Liv	/e																									
abel	Channel	×					_											_		_			_	(	Q Search All I	Fields 💌 Text	includes		• • •
abel	Bus CH-00(UAF	< T(R\$232)) State	- C D0	D1	D2 D	3 D4		D6 C	7 D8	D9 D1	10 D11	D12 D	13 D14 D15	ASCII				mation						(	Q Search All I	Fields 💌 Text	includes		• •
abel	Bus CH-00(UAF	tt(RS232)) State Tx	C C	D1 33 0	D2 D	3 D4 02	17 0	D6 D	7 D8	D9 D1	10 D11	D12 D	1	13		Seud rete			-1					(	Q Search All I	Fields 💌 Text	includes		
abel 24.00	Bus CH-00(UAF	Tr (RS232)) State	- C D0 55 55	D1 33 0 33 0	D2 D	3 D4 02 02	17 0 17 0	D6 D 1 02 1 02	7 D8	D9 D1	10 D11	D12 D		73		Seud rete			-1					(	Q Search All I	Fields 💌 Text	includes		• • •
abel H-00 HE01	Bus CH-00(UAF Timestamp 5ns 13.77319ns 17.54638ns	T(RS232)) State Tx Tx Tx Tx	C D0 55 55 55	D1 33 ( 33 ( 33 (	D2 D2 01 00 01 00 01 00	3 D4 02 02 02	17 0 17 0 17 0	D6 D 1 02 1 02	7 D8 1C 1C 1C	D9 D1	10 D11	D12 D		13 73 13		Seud rete			-1	ľ				(	Q Search All I	Fields 💌 Text	includes		
abel	Bus CH-00(UAF Timestamp 5ns 13.77319ns 17.54630ns 11.319565ns	T(RS232)) State Tx Tx Tx Tx Tx	- C D0 55 55 55 55 55	D1 33 ( 33 ( 33 ( 33 (	D2 D2 01 00 01 00 01 00 01 00	3 D4 02 02 02 02 02	17 0 17 0 17 0 17 0	D6 C 1 02 1 02 1 02 1 02	7 D8 1C 1C 1C	D9 D1	10 D11	D12 D		13 73 13		Baud rate			-1					(	C Search All I	Fields 💌 Text	includes		
ibel	Bus CH-00(UAF Timestamp 31.3.77319ms 27.54630ms 11.319565ms 35.092755ms	K State Tx Tx Tx Tx Tx Tx Tx Tx	- C D0 55 55 55 55 55 55	D1 33 ( 33 ( 33 ( 33 ( 33 (	D2 D1 01 00 01 00 01 00 01 00 01 00	3 D4 02 02 02 02 02 02 02	17 0 17 0 17 0 17 0 17 0 17 0	D6 C 1 02 1 02 1 02 1 02 1 02	7 D8 10 10 10 10 10	D9 D1	10 D11	D12 D		73 73 73 73		Baud rate			-1	ſ				C	Q Search All I	ields 💌 Text	includes		
bel	Bus CH-00(UAF Timestamp ins 13.77319ms 27.54638ms 11.319565ms 50.92755ms 18.08594ms	K State Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx	D0 55 55 55 55 55 55	D1 33 ( 33 ( 33 ( 33 ( 33 ( 33 ( 33 ( 33	D2 D 01 00 01 00 01 00 01 00 01 00 01 00	3 D4 02 02 02 02 02 02 02 02	17 0 17 0 17 0 17 0 17 0 17 0 17 0	D6 C 1 02 1 02 1 02 1 02 1 02 1 02	7 D8 10 10 10 10 10 10 10	D9 D1	10 D11	D12 D		13 13 13 13 13 13 13		Baud rate			-1	ſ				(	Search All I	Fields 🛡 Text	includes _		● ● ●
bel	Bus CH-00(UAF Timestamp 13.77319ms 27.54630ms 13.319565ms 55.092755ms 56.86594ms 22.63913ms	State Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx	D0 55 55 55 55 55 55 55 55	D1 33 33 33 33 33 33 33 33 33	D2         D1           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00	3 D4 02 02 02 02 02 02 02 02 02 02	17 0 17 0 17 0 17 0 17 0 17 0	D6 D 1 02 1 02 1 02 1 02 1 02 1 02 1 02	7 D8 10 10 10 10 10 10 10 10	D9 D1	10 D11	D12 D		73 73 73 73 73 73		Baud rate			-1	ĺ				(	C Search All I	Fields 💌 Text	includes _		≥ ⊃ ∝ /
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bel	Bus CH-00(UAF Timestamp 5.ns 12.77319ms 12.54630ms 12.39565ms 13.9565ms 10.66594ms 12.63913ms 64.412315ms 10.185505ms	State Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx	D0 55 55 55 55 55 55 55 55 55 55 55	D1 33 33 33 33 33 33 33 33 33 33 33 33	D2 D3 01 00 01 00 01 00 01 00 01 00 01 00 01 00 01 00 01 00	3 D4 02 02 02 02 02 02 02 02 02 02 02 02 02	17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0	D6 D 1 02 1 02	7 D8 10 10 10 10 10 10 10 10 10	D9 D1	10 D11	D12 D		73 73 73 73 73 73 73 73 73		Beud rate			-1					(	Search All I	Fields Text	Includes		● ● ●
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	Bus CH-00UAF Timestamp 13. 77319ms 13. 77319ms 13. 315650ms 15. 052755ms 15. 052755ms 15. 052755ms 12. 63913ms 16. 412313ms 10. 1855050ms 123. 95065ms 13. 33108ms	K State Tx Tx Tx Tx Tx Tx Tx Tx Tx Tx	C D0 55 55 55 55 55 55 55 55 55 55 55 55 55	D1 33 33 33 33 33 33 33 33 33 3	D2         D1         00           01         00         01         00           01         00         01         00           01         00         01         00           01         00         01         00           01         00         01         00           01         00         01         00           01         00         01         00           01         00         01         00           01         00         01         00	3 D4 02 02 02 02 02 02 02 02 02 02 02 02 02	17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0           17         0	D6 D 1 02 1 02	7 D8 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	D9 D1	10 D11	D12 D		23 23		Seud rate			-1					C	Search All I	Tields 🛡 Text	includes		
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	Ex. CH-00UAF Timestamp 5.05 13.77319ma 13.319645ms 13.319645ms 13.319645ms 13.319645ms 13.019645ms 13.019545ms 12.63913ms 14.412315ms 10.1855050ms 123.95045ms 13.7.7316tma 151.505065ms 145.272355ms	x Tr Tr Tr Tr Tr Tr Tr Tr Tr Tr Tr Tr Tr Tr T	C D0 55 55 55 55 55 55 55 55 55 55 55 55 55	D1 33 33 33 33 33 33 33 33 33 3	D2         D1           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00	3 D4 02 02 02 02 02 02 02 02 02 02 02 02 02	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	D6 D 1 02 1 02	7 D8 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	D9 D1	10 D11	D12 D		23		Baud rate			-1					C	Search All 1	Tields 💌 Text	Includes		
	CH-00(UAF Timestamp 13.77319ms 13.77319ms 13.377319ms 13.375458ms 13.315655ms 13.85565ms 13.85565ms 13.23.95065ms 13.773185ms 13.773185ms 13.773185ms 13.773185ms 13.773185ms 13.773185ms 13.773185ms 13.23.55065ms 13.25.55065ms 1	x           State           Tx           Tx	D0 55 55 55 55 55 55 55 55 55 5	D1 33 0 33 0 33 0 33 0 33 0 33 0 33 0 33	D2         D1           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00	3 D4 02 02 02 02 02 02 02 02 02 02 02 02 02	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	D6 D 1 02 1 02	7 D8 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	D9 D1	10 D11	D12 D		23 23		Beud rate			-1					¢	Search All 1	Tields Text	Includes		
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bel	CH-00UAF Timestampo Time 1 13.77318ma 13.77318ma 13.19565ms 13.19565ms 13.19565ms 13.05595ms 12.69594ms 12.69594ms 12.595059ms 13.7.7318ma 15.1.55505ms 13.7.7318ma 15.1.555050ms 15.1.5550505ms 15.1.5550505ms 15.1.5550505ms 15.1.20251ma	x           State           Tx           Tx	D0 55 55 55 55 55 55 55 55 55 5	D1 33 0 33 0 33 0 33 0 33 0 33 0 33 0 33	D2         D1           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00           01         00	3 D4 02 02 02 02 02 02 02 02 02 02 02 02 02	17         0           17         0	D6         D           1         02	7 D8 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	D9 D1	10 D11	D12 D		23 23		Beud rete			-1					C	Search All 1	Tields 💌 Text	includes		
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# UFCS

UFCS(Universal Fast Charging Specification) formulate integrated fast charging standards for mobile terminals to solve the problem of incompatibility between fast charging and create a fast, safe and compatible charging environment for end users. The power supply port of UFCS adopts USB Type-A charging port, and the signal transmission is based on USB D+/D-.



🚨 UFC	S Settings					×
Settings			Color			
	Channel			Tx		•
	Tx	A0 🗘		Rx		•
	Rx	A1 🗘				
	Waveform Decode	Tx •	Range			
				From	То	
				Buffer Head 🛛 👻	Buffer Tail	•
				Default OK	Cancel	

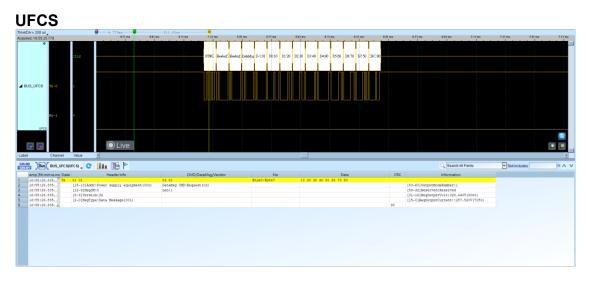
**Channel:** Set the Tx/Rx channel of UFCS.

# Waveform Decode: Tx/ Rx.

(Multiple sets of waveform area decoding cannot be displayed on a single decoder. If you need to view multiple sets at the same time, please add an additional set of decoders.)



### Result





# ULPI

UTMI + Low Pin Interface. ULPI is the Low Pin version of UTMI. UTMI (USB2.0 Transceiver Macrocell Interface) is a protocol for USB controller and USB PHY communication. Compared with ULPI, UTMI has more control signals and supports 8bit / 16bit data interface.

Parameter:	
🛤 ULPI Settings	×
Parameter	Color
Channel	TURN
CLK A0	TxCMD
DIR A1	TxData 🗸
STP A2	RxCMD
NXT A3	RxData 🗸
D0 A4 2 Quick Setting	Range
D1 A5	Decode Range
D2 A6	From To
D3 A7	Buffer Head 👻 Buffer Tail 👻
D4 A8	
D5 A9 🌲	
D6 A10 🌲	
D7 A11 🜲	
Decode ULPI -	ODefault ✔OK ★Cancel

**Channel setting:** Set the ULPI channel. And you can use Quick Setting to quickly set the data pin.

**Decode:** Set the decoding method of ULPI, optional ULPI / USB (analog timing).



#### Result





## USB

red: 16:13:31.380			8.45 ns 159.46 ns	178.46 nd 198.46 nd	496.729x.c 218.46 ns 238.46 ns	259.45 ns 278	46 nd 298.46 nd	318.46 nd	138.46 ns 358.46 ns 370	.46 ns
CLR-6		SYNC	HD_DATA0: 4 00	04 3A	CRC16:0001	EOP				
	6 ns 8 ns 10 ns 8 ns 10 ns	8 m 6 m 10 m 8 r	2 8m 10m 8m 6m	8 m 10 m 6 m 12 m	8 m 6 m 10 m 8 m 8 m	10 m 8 m 6 m 8 m				
DIR-0 STP-1			18 🐋							
S17-1 MOT-11		66 m								
00-10	18 m									
D1-9 D2-0	20 xt									
p3-7			62 10	······			114 as			
<b>D4-5</b>			60 as		3 26	64 20				
D5-4 D6-3	18 m				30 ns		ê xe	12 xx 6 ns 10 ns 6	0 m 8 m	
D7-2					50 m					
	OLive									
R R Channel	Live									• •
	P0. C 🛄 🖻 🏲							Q Search All Fields	Text includes	× ^
tamp (hh.mm:ss.ms 16:13:31.385 DATA0:	PID D0 D1 D2	D3 D4 D5	D6 D7 D8	D9 D10 D11 0	D12 D13 D14 D15	CRC CRC16: 0001	Informat	ion		



# UNI/O

UNI/O is a communication protocol developed by Microchip, primarily used in EEPROM applications. It was designed to meet the growing demand for fewer I/O pins in miniaturized embedded systems, while also providing a low-cost and easy-to-use single-wire bus solution. UNI/O utilizes Manchester Encoding and supports data transmission rates ranging from 10Kbps to 100Kbps

### Settings

🛤 UNI/O Settings	×
Parameter	Color
Channel	
SCIO AO	
Device Address	Start Header 🗸 🗸
8 Bits      12 Bits	MAK / NoMAK
Tolerance	SAK / NoSAK
Input Edge Jitter Tolerance	Unknown
10%	Device Address 🗾 👻
Output Edge Jitter Tolerance	Command 🗸
25% -	Address 🗸
Report Setting	Data 🔹
8 columns 👻	Hold
	Standby Pulse 🗾
Range	
Decode Range	
From To	
Buffer Head 👻 Buffer Tail 💌	
	ODefault ✔OK ★Cancel



Channel: Show the selected channels (SCIO CH0).

Device Address: Set data bits for the device address.

**Tolerance:** Set the Input / Output Edge Jitter Tolerance, ±10% / ±25% default.

**Report Setting:** To show the data by 8 or 16 columns in the Report Window.



#### Result



# USB PD

USB PD (Power Delivery) 2.0/3.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 240W, and the users can charge the device by supporting USB Type-C connector, current version is Revision 3.1, Version 1.0.

## Settings

🚾 USB PD Settings	×
Channel	Color
	User can assign color for specific pattern.
Configuration Channel	Preamble SOP/EOP
CC1 A0 🗘 CC2 A1 🗘	Header   Extended Header
	Data Object(s) CRC
VDM	
Acute USB PD VDM v1.01 All the number is HEX mode Format = VDM Header + VDO(s) Maximum VDM size is 32 (e.g. VDM 1 ~ VDM 32) Support Header Structured VDM only (SVID / Comm Each Vendor-defined command has a correspond	mand Items) Iing VDO(s), e.g. 10.DISCOVER_BUTTONS command
	Default Reload Edit in text editor
Range	Display Settings
Decode Range    From  To    Buffer Head   Buffer Tail	<ul> <li>Detail Report</li> <li>Show 5b value in waveform window</li> </ul>
	ODefault ✔OK ★Cancel

Channel: Set Configuration Channel (CC) CC1 & CC2.



**VDM:** Use the vendor defined message function when checked; users could

define the SVID/Command of the Structured VDM by Edit/Refresh.

Content of the configure file as the following:

Acute USB PD VDM v1.01 Acute USB PD VDM v1.01 All the number is HEX mode Format = VDM Header + VDO(s) Maximum VDM size is 32 (e.g. VDM 1 ~ VDM 32) Support Header Structured VDM only (SVID / Command Items) Each Vendor-defined command has a corresponding VDO(s), e.g. 10,DISCOVER\_BUTTONS command and VDO 1 ##VDM 1 ##VDM 1 ##eader #Header #Header #Header #VD0 4 \*VD0 2; #WD0 2; #WD0 2 ##VDM 1 ##VDM 1 ##VDM 2 ##VDM 2 ##VDM 2 ##VDM 2 ##VDM 2 ##VDM 2 ##VDM 2 ##VDM 2 #WD0 2 VDO<0; I.Power chassis button #VD0 2 #WD0 2 #VD0 2 \*VD0 2 \*VD0 2 \*VD0 1 VDO<0; I.C.Vendor-defined message Bits<1:05,8087,Intel Vendor-defined message Bits<31:155,8087,Intel Vendor-defined message Bits<31:55,8087,Intel Vendor-defined message VDO<0; I.Yendor-defined function ON \*VD0 1 VDOM (Vendor defined message)

Maximum quantity: 32 (##VDM1 ~ ##VDM32)

The ##XXX at the beginning of each column is a keyword and don't use it at

other position in the file. Each VDM is composed of a header and its

corresponding VDO (VDM Object), and the header is the first Data Object of

VDM; the rest is VDO(s), which is the response message according to the

Command.

The header part uses the keyword #Header to include the definition of SVID /

Command:



SVID (Standard/Vendor ID):

Bits<31:16>,8087,Intel Vendor-defined message

When the value of Header bit 31 ~ bit 16 is 8087h, the Intel Vendor-defined

message is displayed.

Command:

Bits<4:0>,10,DISCOVER\_BUTTONS

When the value of Header bit  $4 \sim$  bit 0 is 10h, it's command is

DISCOVER\_BUTTONS.

Show 5b value in waveform window: Show 5b value in the waveform.

**Details Report:** Show the details of bit parsing for the Data Obj(s) frame.

Show 5b value in waveform window: Show 4b or 5b value in the waveform.

#### Result

/Div= 100 us	2	4.17 s	4.17 5 4	17 s 4.17 s	4.17 s	4.17 5		4.17 s	4.17 s	4.17 s	4.17 s	4.17 s 4.17 s 4.17 s 4.17 s	4.17 s	4.17 5
•		1		1 1 1 1 1 1 1 1	111	-	· 'T				· · · ·			1.1.1
			Presonh	5 DOP 5	enter (0566) CF	RC (02142	(A51) E	DC		Preschie	208	0441 CRC (AFD6A8AZ) BC		
D CC1-AL				nannenern		mm		64.65 u	mmmn		ITTTT			
D CL-A								64.65 0	с 					
CC2-A0														
USB PD	•													
USB PD														
		1.5.0												_
P. P	$\odot$	Live												<b>.</b>
Chann														
n Onalli,														
	68 PD) 🖵 🚺	L. 🖻				_						🔍 Search All Fie	Ids 💌 Text includes	
Bus PD(US)	88 PD) C I			Port Data/Power Role	Cable Plug	Rev.	Msg ID	Obj(s) Cnt	Extended	Extended Msg Hdr(h)		Data Obj(s)(h)	Ids Text Includes	D
Bus PD(US Timestamp 3.679755065a				Port Data/Power Role	Cable Plug	Rev.	Msg ID	Obj(s) Cnt	Extended		0013C12C ;	Data Obj(s)(h) Fixed supply:Voltage(12.00V);Max.Current(3.00A)	lds 👻 Text includes	P
Bus PD(US) Timestamp 3.679755065s 3.679691025s	SOP_Sequence	Header(h)	Message Type	-	Cable Plug	Rev.	Msg ID	Obj(s) Cnt	Extended		0013C12C ; 001640E1 ;	Data Obj(s)(h) Fixed supply:Voltage (12.007) ;Max.Current (3.00A) Fixed supply:Voltage (20.007) ;Max.Current (2.25A)	Ids Text Includes	p
Bus PD(US) Timestamp 3.679755065s 3.679950025s 3.629626695s				Port Data/Power Role DEP (SRC->SNK) / SRC	Cable Plug	Rev.	Msg ID	Obj(s) Cnt	Extended		0013C12C ; 001640E1 ; 0A11912C ;	Data Obj(0)(b) Fixed supply:Voltage(12.007);Max.Current(3.00A) Fixed supply:Voltage(20.007);Max.Current(2.25A) Fixed supply:Voltage(5.007);Fixe.Current(3.00A)	Ids Text Includes	
Bus PD(US) Timestamp 3.679755065 3.679950258 3.8296246958 3.8296246958 3.829628828	SOP_Sequence	Header(h)	Message Type	-	Cable Plug	Rev.	Msg ID	Obj(s) Cnt	Extended		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ;	Data Obj(d)(h) Fixed supply:Voltage(12.00%) Max.Current(3.00Å) Fixed supply:Voltage(20.00%) Max.Current(3.25Å) Fixed supply:Voltage(5.00%) Max.Current(3.00Å) Fixed supply:Voltage(12.00%) Max.Current(3.00Å)	ids Text includes	
Bus PD(US) Timestamp 3.679755065s 3.679651025s 3.62962862s 3.6296982s 3.6296982s	SOP_Sequence	Header(h)	Message Type Source Capabilities	DFP (SRC->SNR) /SRC	Cable Plug	Rev.	Msg ID	Obj(s) Cnt	Extended		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ;	Data Obj(0) Fixed supply:Voltage(12.007) Nax.Current(3.00A) Fixed supply:Voltage(30.007) Nax.Current(3.00A) Fixed supply:Voltage(3.007) Nax.Current(3.00A) Fixed supply:Voltage(32.007) Nax.Current(3.00A) Fixed supply:Voltage(32.007) Nax.Current(3.25A)	ids 💌 Text includes	
Bus         PD(US)           Timestamp         3.679755065s           3.679755065s         3.6296902s           3.02969002s         3.02969002s           3.0300481s         3.97977106s	SOP_Sequence	Header(h)	Message Type	-	Cable Plug	Rev. 2.0 2.0	Msg ID 0	Obj(s) Cnt 3 3	Extended N		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ;	Data Obj0/b) Fixed supply/Voltage(12.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00)	ids Text includes	
Timestamp           3.679755065s         3.67981025s           3.02962665s         3.0296962s           3.0303481s         3.9977108s           3.9977108s         3.960043195s	SOP_Sequence	Header(h)	Message Type Source Capabilities	DFP (SRC->SNR) /SRC	Cable Plug	Rev. 2.0 2.0	Msg ID 0	Obj(s) Cnt 3 3	Extended N		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0A11912C ;	Data Obj000 Fixed supply/V01tage(12.007) /Har.Current(3.00A) Fixed supply/V01tage(2.007) /Har.Current(3.00A) Fixed supply/V01tage(3.007) /Har.Current(3.00A) Fixed supply/V01tage(3.007) /Har.Current(3.10A) Fixed supply/V01tage(3.007) /Har.Current(3.00A)	ids 💌 Text includes	
Dusc         PD(US)           1:mestamp         3.679755065s           3.679851025s         3.029624695s           3.02962692a         3.0300401s           3.99977106s         3.90043195s           3.90043195s         3.900192a	SOP_Sequence SOP SOP	Header(h) 3161 3161	Message Type Source Capabilities Source Capabilities	DFP (SRC->SNR) / SRC DFP (SRC->SNR) / SRC	Cable Plug	2.0 2.0	Msg ID	Obj(s) Cnt 3 3	Extended 3		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0A11912C ;	Data Obj0/b) Fixed supply/Voltage(12.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00) Fixed supply/Voltage(20.07) /Har.Current(3.00)	ids 💌 Text Includes	•
Timestamp           3.679755065s           3.62962602s           3.8296262s           3.800481s           3.990043185s           3.9001782s           3.9001785s           3.9001785s	SOP_Sequence	Header(h) 3161 3161	Message Type Source Capabilities Source Capabilities GoodCRC	DFP (SRC->SHK) / SRC DFP (SRC->SHK) / SRC UFP (SNC->SRC) / SHK	Cable Plug	2.0 2.0 2.0	Msg ID 0	Obj(s) Crrt 3 3	Extended 3		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 0013C12C ; 0013C12C ;	Data Objojsh Tanet supply:Vitage (12.007) fear.Current (3.03) Tanet supply:Vitage (12.007) fear.Current (3.23)		a 
0011 Description of the second	SOP_Sequence SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042	Message Type Source Capabilities Source Capabilities GoodCRC Request	DFP (SRC->SNR) / SRC DFP (SRC->SNR) / SRC UFP (SNR->SRC) / SRC UFP (SNR->SRC) / SNR UFP (SNR->SRC) / SNR	Cable Plug	2.0 2.0 2.0 2.0	Msg ID 0 0	Obj(s) Crvt 3 3 0 1	Extended S S S S		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 0013C12C ; 0013C12C ;	Data Obj000 Fixed supply/V01tage(12.007) /Har.Current(3.00A) Fixed supply/V01tage(2.007) /Har.Current(3.00A) Fixed supply/V01tage(3.007) /Har.Current(3.00A) Fixed supply/V01tage(3.007) /Har.Current(3.10A) Fixed supply/V01tage(3.007) /Har.Current(3.00A)		a 
Timestamp           3.679753005s         3.679851025s           3.629659025         3.029659025           3.029659025         3.029659025           3.97971108s         3.900043185s           3.900171282         3.900171285           3.91649055s         3.91449055s	SOP_Sequence SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161	Message Type Source Capabilities Source Capabilities GoodCRC Request GoodCC	DFP (3RC->SNR) / SRC DFP (3RC->SNR) / SRC UFP (3NK->SRC) / SNR UFP (3NK->SRC) / SNR UFF (3NK->SRC) / SNR	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0	Misg ID 0 0 0 0	Obj(s) Cmt 3 3 0 1 0	Extended 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 0013C12C ; 0013C12C ;	Data Objojsh Tanet supply:Vitage (12.007) fear.Current (3.03) Tanet supply:Vitage (12.007) fear.Current (3.23)		
Buck         PD(US)           Treestamp         3.479750249           3.479750249         3.22959224           3.22959224         3.30024818           3.96071708         3.96071708           3.96071708         3.96071708           3.96071708         3.96017708           3.96071708         3.96017708           3.96071708         3.96017708           3.96071708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017788         3.96017788           3.96017788         3.96017788           3.96017788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.96017888           3.9601788	SOP_Sequence SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363	Message Type Source Capabilities Source Capabilities GoodCRC Request GoodCRC Accept	DFP (SRC->SNR) / SRC DFP (SRC->SNR) / SRC UFP (SNR->SNR) / SRC UFP (SNR->SNR) / SNR UFF (SNR->SNR) / SNR DFF (SRC->SNR) / SNR	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0	Msg ID 0 0 0 0 0 0 1	Obj(s) Cnt 3 3 1 0 0 0	Extended 3 3 3 3 3 3 3 3 3 3 3 3 3		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 0013C12C ; 0013C12C ;	Data Objojsh Tanet supply:Vitage (12.007) fear.Current (3.03) Tanet supply:Vitage (12.007) fear.Current (3.23)		
Year         PD(US)           Timestamp         0.479750658           3.479750658         3.479510258           3.429624628         3.429624628           3.429624628         3.429624628           3.429624628         3.49961258           3.429624628         3.49971468           3.499614285         3.49971368           3.990173558         3.990173558           3.9914430558         3.992442235           3.9942442355         3.994242355           3.994242355         3.994242355	SOP_Sequence SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161	Message Type Source Capabilities Source Capabilities GoodCRC Request GoodCRC Accept GoodCRC	DFP (3RC->58R) / 5RC DFP (3RC->58R) / 5RC UFP (5RC->58C) / 58R UFP (3RK->58C) / 58R UFF (3RC->68R) / 58R DFP (3RC->58R) / 5RC UFF (3RC->58R) / 5RC	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	Msg ID 0 0 0 0 0 0 0 1 1 2	Obj(s) Cnt 3 3 0 1 0 0 0 0 0	Extended B B B B B B B B B B B B B B B B B B		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 0013C12C ; 0013C12C ;	Data Objojsh Tanet supply:Vitage (12.007) fear.Current (3.03) Tanet supply:Vitage (12.007) fear.Current (3.23)		) =
Buck         PD(US)           Treestamp         3.479750249           3.479750249         3.22959224           3.22959224         3.30024818           3.96071708         3.96071708           3.96071708         3.96071708           3.96071708         3.96017708           3.96071708         3.96017708           3.96071708         3.96017708           3.96071708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017708         3.96017708           3.96017788         3.96017788           3.96017788         3.96017788           3.96017788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.9601788           3.9601788         3.96017888           3.9601788	SOP_Sequence SOP SOP SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363 0241	Message Type Source Capabilities Source Capabilities GoodCRC Request GoodCRC Accept	DFP (SRC->SNR) / SRC DFP (SRC->SNR) / SRC UFP (SNR->SNR) / SRC UFP (SNR->SNR) / SNR UFF (SNR->SNR) / SNR DFF (SRC->SNR) / SNR	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	Msg ID 0 0 0 0 0 1 1 2 2	Obj(s) Cnt 3 3 0 1 0 0 0 0 0 0	Extended S S S S S S S S S		0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 001640E1 ; 0A11912C ; 0013C12C ; 0013C12C ; 0013C12C ;	Data Objojsh Tanet supply:Vitage (12.007) fear.Current (3.03) Tanet supply:Vitage (12.007) fear.Current (3.23)		•
Year         POUS           1.75753065         2.75753065           2.75753065         2.75951025           3.12962405         3.2305405           3.12962405         3.2305412           3.800013255         3.80013255           3.98014223         3.98013255           3.98144005         3.98144005           3.98144005         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225           3.98144225         3.98144225	SOP_Sequence SOP SOP SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363 0241 0566	Message Type Source Capabilities Source Capabilities GoodCRC Arcept GoodCRC S_JRT	DFP (SRC->SNC) / SRC DFP (SRC->SNC) / SRC UFP (SNC->SRC) / SRC UFP (SNC->SRC) / SNC UFP (SRC->SNC) / SNC DFF (SRC->SNC) / SNC UFP (SRC->SNC) / SNC UFP (SRC->SNC) / SNC	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	0 0 0 0 0 1 1 2	Obj(s) Cnt 3 3 0 1 0 0 0 0 0 0 1	Extended 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		0013C12C 7 001440E1 7 0013C12C 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7	Data Objojsh Tanet supply:Vitage (12.007) fear.Current (3.03) Tanet supply:Vitage (12.007) fear.Current (3.23)	nt(2.258)	
Timestamp           0.479755065           0.479755065           0.479755065           0.479755065           0.479755065           0.479755065           0.28964025           0.28956426           0.38004185           0.980173555           0.980473555           0.98146255           0.98146255           0.982446255           0.982446255           0.982416225           0.98242648           0.982617668           0.982617668           0.982617668           0.982617668           0.982617668 <td>SOP SOP SOP SOP SOP SOP SOP SOP SOP SOP</td> <td>Header(h) 3161 3161 0041 1042 0161 0363 0241 0566 0441</td> <td>Message Type Source Capabilities Source Capabilities GoodCRC Regards GoodCRC Accept GoodCRC FS_BDY GoodCRC</td> <td>DFP (SRC-&gt;SRC) / SRC DFP (SRC-&gt;SRC) / SRC UFP (SRC-&gt;SRC) / SRC UFP (SRC-&gt;SRC) / SRC UFP (SRC-&gt;SRC) / SRC DFP (SRC-&gt;SRC) / SRC DFP (SRC-&gt;SRC) / SRC DFP (SRC-&gt;SRC) / SRC</td> <td>Cable Plug</td> <td>2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0</td> <td>0 0 0 0 0 1 1 2</td> <td>Obj(t) Crrt 3 3 0 1 0 0 0 0 0 0 0</td> <td>Extended y y y y y y y y y y y y y y y</td> <td></td> <td>0013C12C 7 001440E1 7 0013C12C 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7</td> <td>These supply "No.14 per (12.07) (the Company of the /td> <td>nt(2.258)</td> <td></td>	SOP SOP SOP SOP SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363 0241 0566 0441	Message Type Source Capabilities Source Capabilities GoodCRC Regards GoodCRC Accept GoodCRC FS_BDY GoodCRC	DFP (SRC->SRC) / SRC DFP (SRC->SRC) / SRC UFP (SRC->SRC) / SRC UFP (SRC->SRC) / SRC UFP (SRC->SRC) / SRC DFP (SRC->SRC) / SRC DFP (SRC->SRC) / SRC DFP (SRC->SRC) / SRC	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	0 0 0 0 0 1 1 2	Obj(t) Crrt 3 3 0 1 0 0 0 0 0 0 0	Extended y y y y y y y y y y y y y y y		0013C12C 7 001440E1 7 0013C12C 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7	These supply "No.14 per (12.07) (the Company of the	nt(2.258)	
Poil         Poil           1         757530659           2         757530659           3         25256229           3         25255225           3         25255225           3         25255225           3         25255225           3         25017228           3         9601732555           3         9814490255           3         980213559           3         982442255           3         980213559           4         1751317629           4         17513038	SOP_Sequence SOP SOP SOP SOP SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363 0241 0366 0241 0366 0441 176F	Message Type Source Capabilities Source Capabilities GoodCRC Arcept GoodCRC S_BAT GoodCRC Vendor Defined(VCM)	DFF (SRC->508) / SRC DFF (SRC->508) / SRC	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	0 0 0 0 0 1 1 2	Objit) Cnt 3 3 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Extended 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3		0013C12C 7 001440E1 7 0A11912C 7 0013C12C 7 001440E1 7 0013C12C 7 001440E1 7 330384E1 7	These supply "No.14 per (12.07) (the Company of the	nt (2.25%)	2)
Description         POCUS           Trenstamp         3. 479550458           3. 479550458         3. 4294246959           3. 4294246959         3. 4294246959           3. 4394244959         3. 4390424395           3. 4394244959         3. 439042439           3. 4394244959         3. 439042439           3. 4394244329         3. 490173559           3. 4924442259         3. 492442239           3. 4442039         3. 492442239           3. 4175117689         4.17511768           4.175121768         4.17751238	SOP_Sequence SOP SOP SOP SOP SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363 0241 0566 0441 1766 0441	Message Type Source Capabilities Source Capabilities GoodCRC Request GoodCRC Accept GoodCRC PS_BDY GoodCRC Vendor Defined(VCN) GoodCRC	DFF (SRC->888) / SRC DFF (SRC->888) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	0 0 0 0 0 1 1 2	Objis) Cnt 3 3 0 1 0 0 0 0 0 0 0 0 0 3	Extended N N N N N N N N N N N N N N N N N N		0013C12C 7 001440E1 7 0013C12C 7 0013C12C 7 00140E1 7 0013C12C 7 00140E1 7 0013C12C 7 001440E1 7 330384E1 7	Deer Chylyddi Traed wegalyrfol Loey (2010) (Mac Current (L. 2010) Traed wegalyrfol Loey (2010) (Mac Current (L. 2010) Traed wegalyrfol Loey (2010) (Mac Current (L. 2010) Traed megalyrfol Loey (2010) (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010) (Mac Current (Mac Current (L. 2010) (Mac Current (L. 2010	nt (2.25%)	2)
Band         POCUS           1.4797550458         1.4797550458           1.4797550458         1.4797550458           1.4798510458         1.42942445           1.239569428         1.30004818           1.390711088         1.98017355           1.98017355         1.98017355           1.98017355         1.98014258           1.980173556         1.984142258           1.980123556         1.174521435           4.17521436         4.17521436	SOP_Sequence SOP SOP SOP SOP SOP SOP SOP SOP SOP SOP	Header(h) 3161 3161 0041 1042 0161 0363 0241 0566 0441 1766 0441	Message Type Source Capabilities Source Capabilities GoodCRC Request GoodCRC Accept GoodCRC PS_BDY GoodCRC Vendor Defined(VCN) GoodCRC	DFF (SRC->888) / SRC DFF (SRC->888) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC UTT (SRC->881) / SRC	Cable Plug	2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0 2.0	0 0 0 0 0 1 1 2	Obj(s) Cnt 3 3 0 1 0 0 0 0 0 0 0 1 0 0 3	Extended N N N N N N N N N N N N N N N N N N		0013C12C ; 001400E1 ; 0013C12C ; 0013C12C ; 0013C12C ; 001400E1 ; 0013C12C ; 001440E1 ; 330304E1 ; 330304E1 ; FF008002 ; FF008002 ;	Date Objects Tead regular/1012/escillation (International Control (	nt (2.25%)	2)

## Accessories:

https://www.acute.com.tw/en/product/detail142



# USB1.1

USB (Universal Serial Bus), known as the "Universal Serial Bus", was initially developed by seven companies: Intel, Microsoft, National Semiconductor, Compaq, Northern Telecom, NEC, and AT&T. The development of USB began in 1994, with version 1.0, followed by version 1.1 in 1998, and later USB 2.0 in 2000. The data transfer speed evolved from 12 Mbps in USB 1.1 to 480 Mbps in USB 2.0.

In the USB protocol, communication between the host and device is primarily established through two differential signal lines, D+ and D-.

Setting	Color
Channel	
D-  A1 + D+ A0 +	
USB 1.1 Setting	Sync 🗸
Auto Detect O Low speed O Full speed	Packet ID
Decode USB standard request & discriptor	Frame No. / Address / Endpoint/ Data
Report Setting	CRC5/CRC16
Mark PID SOF -	EOP
Show Data 8 Columns -	Transfer Direction
	Туре
SOF DATA1	Recipient -
	bRequest 🗸
OUT STALL	wValue 🔹
DATA0 PRE	windex 👻
	wLength -
Show scale in the waveform	Descriptor 🗸
Range	
Decode Range	
From To	
Buffer Head 🔹 Buffer Tail 👻	ODefault ✔OK ★Cancel

# Settings



**D+:** D+ line for USB 1.1 data transmission.

**D-:** D- line for USB 1.1 data transmission.

**USB1.1 Settings:** Configure the USB 1.1 signal as Low-Speed or Full-Speed,

and determine whether to decode USB standard requests and descriptors.

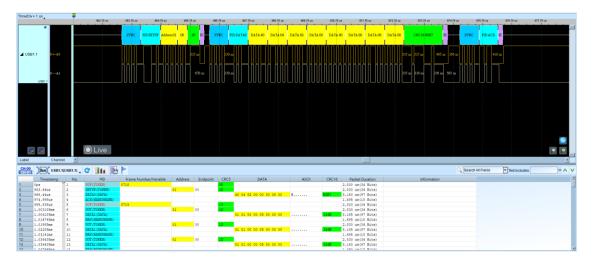
**Mark PID**: Allows marking selected PID types with specific colors in the report window.

**Show Data:** Sets the data display in the report window to 8 columns or 16 columns.

PID Filter: Allows hiding specific data from display.

Show Scale in Waveform: Displays scale markings on the waveform.

Result.





# **USB4/TBT3 SB**

USB4 can simultaneously transmit DisplayPort video and PCIE signals through Intel Tunneled technology, and also support PD (Power Delivery) fast charging technology.

USB4 is backward compatible with USB 2.0 and USB 3.2 Gen1/Gen2 and supports Thunderbolt 3/4. The sideband channel (SB) was originally defined as a channel for video protocol communication after entering the Alt-Mode (Alternate Mode) in USB 3.2 (for example: DP Alt-Mode transmits AUX signals through the Sideband channel...etc.). In the USB4 specification, new features of Sideband channel are added to confirm whether the USB4 interface is connected, start and close the channel, initialize the channel, and enter or leave the sleep mode. Thunderbolt Alt-Mode will be enabled when connecting to the device via Thunderbolt 3.

	Channel Settings		>	<
	endmiter betangs			`
Settings	: Channel		Color	
ō	Sideband TX AO	Waveform Area	Data Link Escape (DLE)	
		TX     ORX	Lane State Event (LSE) / ELSE 🗾 🗸 🗸	J
			Complement LSE(CLSE) / ECLSE 📃 🗸	
	Options		Start Transaction (STX) - AT	
	Show Scale	Version • USB4 1.0	Start Transaction (STX) - RT	)
	Detail Report	<ul> <li>USB4 2.0</li> <li>TBT3</li> </ul>	Data Symbols / Link Parameters 🖉 🗸 🗸	
			LCRC/HCRC -	
Range	From	То	End of Transaction (ETX) Symbol	
	Buffer Head 💌	Buffer Tail 👻	No Meaning Byte 🗸 🗸 🗸	
			Default Cancel OK	

# 0-441-0-0-0

## a. Channel:

Sideband TX: Show the selected channel.



**Sideband RX:** It is checked by default, and the dual-channel analysis mode can be enabled by checking Sideband RX.

**Data Convert:** TX is checked by default, and the TX/RX channel can be selected for analysis in the data convert field.

**Show on Report:** TX and RX is checked by default. Choose which channel to display in the report area, and both channels can be displayed at the same time.

b. Others:

**Version:** USB4 2.0 is checked by default, and different versions can be selected for USB4/TBT3 SB signal analysis.

Show scale on data convert: The default is off. Show the scale on data convert field.

**Show data detail on report:** The default is off. If checked, additional data information will show on report as shown below.

Channel	Transaction Type	Reg	Len	WnR	Data Symbols / Link Parameters payload(H)
BTX	RT Addressed	vendor specific (15h)	35	Read	
BRX	AT Command	Link Configuration(0Ch)	3	Read	
BTX	AT Response	Link Configuration(OCh)	3	Read	03 F3 03
					Byte0 [0]Enabling Decision (Lane 0): 1
					<pre>[1]Enabling Decision (Lane 1): 1</pre>
					[2]Asymmetric Decision (Tx): 0
					[3]Asymmetric Decision (Rx): 0
					Byte1 [0]Enabling Request (Lane 0): 1
					[1]Enabling Request (Lane 1): 1
					[4]Bonding Support: 1
					[5]Gen 3 Support: 1
					[6]RS-FEC Request (Gen 2): 1
					[7]RS-FEC Request (Gen 3): 1
					Byte2 [0]USB4 Sideband Channel Support: 1
					[1]TBT3-Compatible Speeds Support: 1
					[2]Gen 4 Support: 0
					[3]Asymmetric Support 3 Tx: 0
					<pre>[4]Asymmetric Support 3 Rx: 0</pre>
					[5]Request Asymmetric Tx: 0

# 2. Result:



iv= 50 us	.0.0	7 s 6.67 s	0.07 s 0.07	7 s 0.67 s	6.87 s 6.87 s	6.67 s 6.67 s	5.67 s 6.67 s 6.67	s 8.87 s	6.67 s 6.07 s	0.67 s
•							* * * * * * * * *			
						FE 40 0D 0	00 00 00 00 AA 19 <mark>FE</mark> 40			
M/TBT3 SI BUTK-AO										
SBR0C-AL	4									
84/1813 58				U LUL						
•										
					04 24 87 <mark>78</mark> 40					
1 3813(-40	٥									
7111X-A1										
SBR0C-A1	1									
1584/1813 58										
1584 TBT3 58	OLiv	e								
SB4TBT3 SB Channel	el I									
Channel	OLiv							٩	Search All Fields 🕐 Text Includes	
Channel	el J USB4/TBT3 SB) C Channel Tra	III P P	Reg	Len	Wisk	Payload(h)			Information	
Channel Bus Bus 1(U: Timestamp 6.670205315s	USB4/TBT3 SB) C Channel Tra SBTX LT Resu	IIII P	Reg	Len				CII C(E)LSE / CRC		
Channel Channel Bus Bus 1(U: Timestamp 6. 6702053155 6. 6715040055	USB4/TBT3 SB) C Channel Tra SBX LT Resy SBX RT Adda	Insection Type	Reg	Len	VinR 10 04 00 00 00				Information	
Channel Channel Bus Bus 1(U) Timestamp 6.670203315s 6.6712069s 6.67335664s	USB4/TBT3 SB) C Channel Tr SB2X RI Addi SB2X RI Addi SB2X RI Res SB2X RI Res	IIII P P	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04			CII C(E)LSE / CRC	Information	p
Channel Channel Bus Bus 1(U Timestamp 6.470205315s 6.471320405s 6.47133564s 6.47333564s 6.47333564s	el I USB4/TB13 SB) C Channel Tra SB7X KI Asig SB7X KI Asig SB7X KI Asig SB7X KI Asig SB7X KI Asig	intaction Type are reserd ronse resed	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04 0D 04 00 00 80 80			CII C(E)LSE / CRC SD 24 07 AA 19 24 07 CA 79	Information	
Channel Channel Bas Bus Bus 1(U Imestamp 6.670203315s 6.671304005s 6.6733664s 6.6733664s 6.6733664s	el s USB4/TBT3 S8) C Channel Trr S87X RT Addr S87X RT Rest S87X RT Rest S87X RT Rest S87X RT Rest S87X RT Rest S87X RT Rest	IIII P P	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04 0D 04 00 00 00 00 0D 04			C(E)LSE / CRC 50 24 67 AA 19 24 67 CA 79 24 67	Information	
Channel Channel Channel Channel Channel Constants Consta	Channel Tra SBXX RI Addi SBXX RI Addi	IIII P P	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04 0D 04 00 00 80 80 0D 04 0D 04 00 00 81 81			C(E)LSE / CRC           SD           24 87           24 87           CA 79           24 67           CA 29	Information	p
Channel Channel Des Bus (U Timestamp 6.670203315s 6.67130645 6.67336645 6.673356645 6.673356645 6.673356645 6.673356645	USB4/TB13 58) C Channel Tra SB07 LT Res SB07 RT Addi SB77 RT Addi SB77 RT Addi SB77 RT Addi SB77 RT Addi SB77 RT Addi SB77 RT Addi	maction Type are eased onse eased onse eased onse eased onse eased	Reg	Len	00 04 00 04 00 00 00 00 00 04 00 04 00 00 80 80 00 04 00 04 00 00 81 81 00 04		** ** ** ** **	CIEUSE / CRC 50 24 87 34 87 24 87 24 87 24 87 24 87 03 29 24 87	Information	p
Channel Channe	el ( USB4/TBT3 S8) C Channel Tr SBX AT Adds SBX AT Adds	insction Type ased onse eased onse eased onse eased onse eased onse eased onse eased	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04 0D 04 00 00 80 80 0D 04 0D 04 00 00 81 81 0D 04 0D 04 00 00 81 81			C(E)LSE/CRC SD 24.87 34.19 24.67 CA.19 24.67 03.29 24.67 03.29 04.29	Information	p
Channel Channel Bas Bus 1(U Timestamp 6.6702053155 6.6712069 6.67335664 6.6712069 6.67335664 6.673531955 6.674249455 6.675513055 6.675513055	USB4TBT3 S8) C Channel Tr BOTX C T Resp STX C T Addr STX C T Addr	insection Type are eased onse eased onse eased onse eased onse eased onse eased onse eased	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04 0D 04 00 00 80 80 0D 04 0D 04 00 00 81 81 0D 04 0D 04 00 00 81 81 0D 04		** ** ** ** ** ** **	C(E)LSE / CRC           55           24           87           24.97           24.97           24.97           24.97           24.97           24.97           24.97           24.97           24.97           24.97           24.97           24.97	Information	
Channel Channel Bac Bac Bus 10/ Tmestamp 6. 47203315 6. 471320495 6. 473354645 6. 4735713658 6. 4735713658 6. 4735713658	el ( USB4/TBT3 S8) C Channel Tr SBX AT Adds SBX AT Adds	the sed     tops     tops	Reg	Len	0D 04 0D 04 00 00 00 00 0D 04 0D 04 00 00 80 80 0D 04 0D 04 00 00 81 81 0D 04 0D 04 00 00 81 81			C(E)LSE/CRC SD 24.87 34.19 24.67 CA.19 24.67 03.29 24.67 03.29 04.29	Information	



# Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic entry system.

Settings	
🚐 Wiegand Settings	×
Channel	
:	
Data 0 A0	
Data 1 A1	
Color	
Data Parity -	
Range	
Decode Range	
From To	
Buffer Head 💌 Buffer Tail 💌	
ODefault ✔OK ★Cance	el 🛛

Data 0: Wiegand data 0 •

Data 1: Wiegand data 1 °

Result	:																
Time/Div=10 ms	2	-30 ms	0.5 s -20 ms		0.05	10 ms	20 ms		40 ms	60 ms	60 ms	70 ms	10 m/	90 ms	100 ms	110 ms	
•	-40 ms	-38 ms	-20 ms	-10 ms	· · · ·	10 ms	20 ms	30 ms	40 md	00 m3	00 ms	70 ms	10 nd	90 ms	100 ms	110 ms	120 ms
· · ·					Pi 34	95	04	88									
					n - 1	1 T	1 T										
																	- 8
d Bus 1 Date 0-	-1.0				3.32 m												
Data 1-	-A1				3.33 m 3.34 n	18.31 m	6.76 xu: 3.34 x	n 4.45 mi									
Wiegand																	
15, 16	O Live																• •
Label Channe		_															
	Megand) 🖵 🚺													Q Seat	ch All Fields 💌 Te	vt includes	× ^ V
		03 D4 D5	D6 D7	Even parity	Odd parity	Information								-			
	4 95 04 88	13 04 05		: OK	0: OK	information											
2 204.58238ms 3	4 95 04 88		1	: 080	0: 000												
3 13.74065962s 3 4 16.912640465#	4 95 04 88		· · · ·	: OK	0: OK	unknown											



# Chapter 2 Bus Trigger

# **Bus Trigger**

## Introduction of trigger

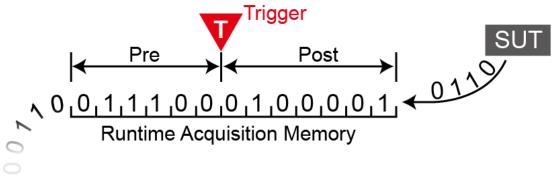
Trigger function is to utilize the logic analyzer's hardware circuitry to check whether the signal to be tested meets the trigger conditions within a limited period of time by using parallel processing techniques, and then carry out the signal acquisition work. Ideal logic analyzer trigger function, in addition to the basic must be accurate, but also as much as possible can be varied. The hardware of logic analyzer takes the signal acquisition function and then performs the signal acquisition work.

The hardware of logic analyzer take the parallel processing technology to check the signal.

## **Trigger Mode**

1. Pre-Trigger

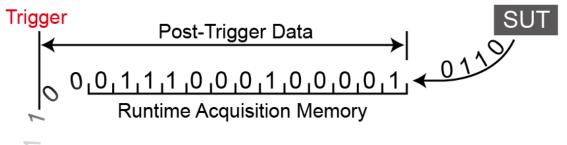
In certain applications, when the user wants to capture signals before the trigger point, the Pre-Trigger function must be enabled. After pressing the 'Start Capture' button, the logic analyzer will wait until the data fills the memory from the beginning of the buffer to the trigger cursor before allowing the trigger circuit to start operating (it starts operating, not issuing the trigger signal). Therefore, before the logic analyzer has filled the data between the buffer and the trigger cursor, any signal that meets the trigger condition will not cause the trigger circuit to issue a trigger signal.



2. Post-Trigger



This is the most basic triggering method. After pressing the 'Start Capture' button, the logic analyzer will wait for the trigger to occur and then start capturing data from the position specified by the trigger cursor. Once the memory is fully filled with data, the capture will stop.



3. Delay-Trigger

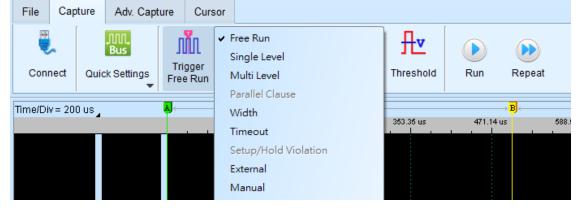
In certain applications, when the user wants to capture signals after the trigger point and with a delay, the trigger delay function can be used to set the desired delay time. After the signal capture is successful, the trigger cursor will stop at the position where the data capture started.

4. Pass Count

Pass Count represents the number of times the set trigger parameters should be ignored. Under normal conditions, Pass Count is set to 0, which means data capture will start as soon as the trigger parameters are met. If set to N times, it means the trigger parameters must be met N+1 times before data capture begins. The maximum value of Pass Count will be automatically adjusted based on the specific model.

5. Choose to Trigger

Click on 'Trigger' in the toolbar and select the desired condition to use.



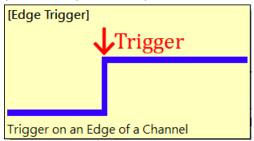


# Parallel Clause Trigger

M Parallel Clause Trigger Setting	IS		
Trigger Sample            • Edge Trigger • 10th Edge Trigger • Channel Value • Bus Value on Signal Edge • Edges Too Close • Edges Too Far Apart • Edge Followed by Bus • Edge Followed by Bus • Pulse Volth Time	¥ ⊿State 0	Description IF CH-00 • Edge Rising * * AND CH-01 • = 0h Occur • 1 time(s) ÷ Start Timer 0 AND Reset Timer 0 THEN Stop Timer 1 Stop Waveform Store Auto (Goto Next) • ELSE IF Anything • * THEN Goto State 2 •	Available Resources: State x 14 Condition Resource x 62 Channel Event: Slot A x 13 Slot B x 16 Slot C x 16 Slot C x 16 Slot D x 16 Timer/Counter 0 Condition Mode Timer Counter Value V 100.00 ns V Timer/Counter 1 Condition
My Setting1  Wy Setting2	∡State 1	Add Else If      Add Else Description	Mode       Timer       Counter         Value       >       100.00       ns         Timer/Counter 2 Condition       Mode       Timer       Counter         Value       >       100.00       ns       >         Timer/Counter 3 Condition       Mode       Timer       Counter         Value       >       100.00       ns       >         Value       >       100.00       ns       >
H Save Current Settings	+ Add State		✓ OK X Cancel

Parallel Clause Trigger feature provides 16 States, 64 Condition Resources and 4 Timer/Counter conditions(1) to help user locate the target waveform, it is also available to set State branch control flow for each IF Clause and decide whether to store waveform or not.

 Trigger Sample: Provides several Trigger Samples for user's reference, users may also combine multiple trigger samples together for more complex trigger condition. Holding mouse cursor on each Sample for a while will pop up the sample description with schematic picture.





2. Trigger condition settings:

*	Description	0	
	IF	CH-00 Edge Rising 💌 🗰	+
	B	AND V CH-01 V = V Oh *	Ο,
	U	Occur 🔽 1 time(s) 🌻	
		Start Timer 0 AND Reset Timer 0 Stop Timer 1	V
<b>.</b>		Stop Waveform Store	_ =
⊿State 0		🕹 Auto (Goto Next)	-
0	ELSE IF	Anything 💌 🗱	+ ~ ~
	THEN		4
		Goto State 2	-
	🕂 Add Else	lf 🕂 Add Else 5	
*	Description		
	IF	CH-00 🔽 = 🔽 Oh	+
			9,
<b>⊿</b> State 1		Present > ▼ 150.000 😧 us ▼	
	THEN		_⊻
		Value (Set Triggered)	<u>'</u>
	🛉 Add Else	If 🛉 Add Else	
Add State	6		
-	$\mathbf{\nabla}$		

- State button: Click to switch between Text Read Only mode and Edit mode.
- ② State description: Click to edit a short user description for the State, maximum input text length is 80 characters.
- ③ IF Clause: Setup trigger conditions for Label selected in waveform area, and it is also available to setup AND/OR logic combination for multiple IF conditions.
  - Channel Logic/Edge/Pattern compare: Specify value or edge condition for each channel label, it is also available to input X as don't care value for the comparison. Input value ended with h for hexadecimal value; input value ended with b for binary value; input value not ended with b or h for decimal value.



Bus_[A7:A0] 🗨 =	ABh 🗱	
AND Bus_[A7:A0]	▼ = ▼ 10101011b	×
AND Bus_[A7:A0]	▼ = ▼ 171	×
AND Bus_[A7:A0]	▼ = ▼ XBh	×
AND Bus_[A7:A0]	▼ = ▼ AXh	×

- ii. Timer/Counter condition check: Check Timer/Counter conditions, condition will be set as True if the Timer/Counter value is matched, otherwise the condition is be set as False.
- Occur and Present time check: Additional Occur times check or Present time check when the all conditions are set to True in the IF Clause.

iv. Control buttons

Add new condition: Click to add new AND/OR IF condition, the new IF condition will consume 1 Condition Resource.

Advanced control button, including:

Get Value From: Set IF condition value by all Label value from selected Cursor position in the waveform area.

Copy: Copy all IF conditions of current IF Clause.

Paste: Paste the copied IF conditions into current IF Clause.

④ THEN Branch: Select the Branch or Trigger control flow when the IF

Clause is matched (2). When select Auto, the Branch or Trigger control will be determined by current State order in the setting, the Action will be set as Trigger if current State is the last State in the setting; the Action will be set as Goto Next State if current State is NOT the last State in the setting.

THEN		
	🔻 Auto (Set Triggered)	-
Add Else	Auto (Set Triggered)     Goto Next	
	<ul> <li>Set Triggered</li> <li>Goto State 0</li> <li>Goto State 1</li> <li>Goto State 2</li> <li>Goto State 3</li> <li>Goto State 4</li> <li>Goto State 5</li> <li>Goto State 6</li> </ul>	•



Additional Then action: Setup Timer/Counter Start/Stop/Reset actions or Waveform Store Suspend/Resume for each IF Clause when condition matched.

⑤ Add new ELSE IF / ELSE Clause: Click to add new ELSE IF / ELSE Clause, each clause condition will be checked from top to bottom, and perform the specified Action and Branch if the clause condition is matched. New clause conditions will consume Condition Resources. ELSE Clause condition will be set as "Anything" and Branch to current State by default if the user didn't assign ELSE Clause.

- 6 Add new State: Click to add new State Clause, the new State Clause will consume both State and Condition Resources.
- 3. Available Resources and Timer/Counter settings: Display remain available

resource number and Timer/Counter settings.

Timer / Counter: Parallel Clause trigger provides 4 independent Timer/Counter resources, each resource could be selected to work in Timer or Counter mode. The minimum Timer interval is 12 Sample clock intervals (i.e. 60ns when working in 200MHz sampling mode), and the maximum Timer interval is 0x3FFFFFF (i.e. 5s when working in 200MHz sampling mode). The minimum Counter value is 1, and the maximum Counter value is 0x3FFFFFFF.

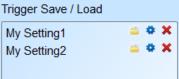
4. Triger Save/Load: Users may save their current trigger settings with

maximum 20 characters description, or load previous saved trigger settings

from the list, the saved settings will be stored into Working Directory with file

name PClauseUserSetting.aqr. Copy and share the .aqr file in order to

share the settings to other user.



Load selected Trigger settings, it's also available to select to overwrite current Trigger settings, or select + to append the selected settings to the end of current Trigger settings.

Edit the display name for the selected Trigger settings.

X Delete the selected Trigger settings.



- (1) Timer / Counter features are provided in 300MHz, 250MHz, 200MHz and below sampling rate mode only.
- (2) If these not valid trigger setting, system will be hold and the status bar will display "Wait for Trigger", and must press Stop Capture manually in order to retrieve the waveform.

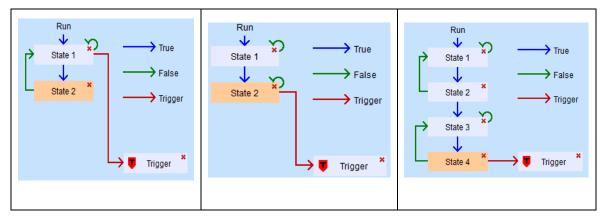
# **Clause Trigger**

The Clause trigger settings dialog box is as below.

M Serial Flas	h / SPI NAND F	ash Trigger Settings			? ×	<
Channel		Clause Trigger				
CS#	A0 🌲	Run 2		State 3 3 Timer Condition		
SCLK	A1 🗘	rr State 1	> True	Logic OR O Logic AND     AND Timer 1 >= 5ns		
SI/SIO0	A2 🌲	T1 T2		Event 1 OR Single Mode Command		
SO/SIO1	A3 🗘	State 2 - *		Single Mode		
WP#/SIO2		State 2 - X		8 cycles If the condition is true, then		
Hold#/SIO		State 3		Reset Counter 1		
SIO4	A6 \$	L	Trigger *	Address      Reset Counter 2      Start Timer 1 from reset		
SIO5	A7 🗘		- inggei	8b 16b 24b 32b = XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX		
SIO6	A8 \$		🛉 State x 5	Dummy cycles		
SIO7	A9 \$		Counter x 2	0 Dummy cycle(s)		
DQS	A10 🌲		Counter x 2	Data		
CS# Glitch Tr	rigger			Fix Offset 0  Dyte(s)		
None	-					
Width	< 10ns					
	-		-			
✓ tSHSL>=	5ns		Timer 1	<< Advanced Setting		
tCLQV >= 8.7	7E0po		Timer 2			
IULUV >= 8.7						
O Defau	lt			V OK X Cancel		

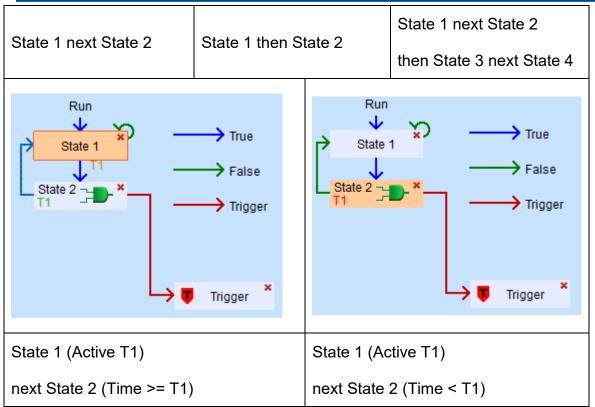
#### 1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.



## 2. Flow chart





A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:

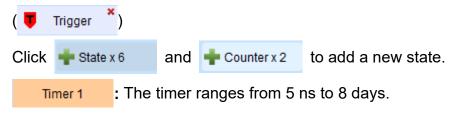
Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.

Double click any state, the state will branch to itself if it is false.

Click the state button and trigger button ( **Trigger** \*): triggere when the state conditions is satisfied.

Delete any state by clicking the cross sign on the state.

Clear the links to the trigger button by clicking on the trigger button





### 3. State settings

This area displays the detailed trigger conditions for each level in the triggering process on the left:

The State 1 text in the upper left indicates the currently displayed state number.

● Logic OR ○ Logic AND User can set the logic operation rules between events.

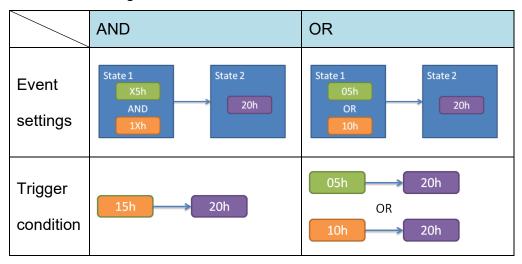
Event 1 🗶 Event 2 🗶 Event 3 🗶 🚽 OR User can switch/view the

number of combinations of OR/AND conditions currently in this hierarchy.

Choose + OR / + AND tab to add up to 8 OR/AND triggers.

The center parameter setting area varies according to the selected trigger type. The input values support 2 /10/16 progress, binary code (followed by b, such as 01000001b), decimal code (followed by no b, such as 65), hexadecimal code (followed by h, such as 41h).

The relationship between events and triggering signals within each level can be seen in the following table:



## 4. Timer and Counter settings

Press Advanced Setting >> button to edit the timer/counter reset settings of

the state.



Timer Co	ondition							
	D Timer 1 D Timer 2	<		ns ns				
If the cor	ndition is tru	e, then						
✓ Re	set Counter	r 1						
✓ Re	▼ Reset Counter 2							
✓ Start Timer 1 from reset								
✓ State	art Timer 2 fr	rom reset						

The following table describes the state button icons:

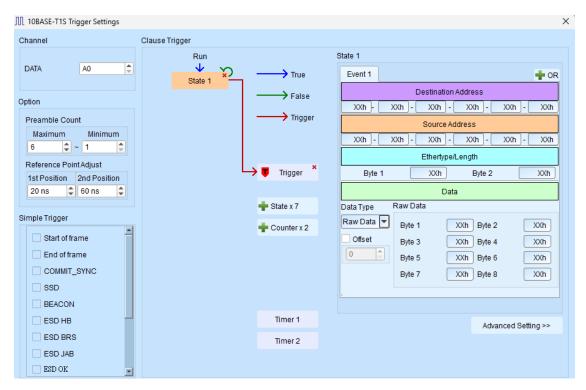
	Run State 1 T1	Run State 1	Run State 1 C2 T2	Run State 1* T1 T2* C1 C2 T1 T2
		State 1	State 1	State 1
Conditions	State 1	And	And	And
		timer > T1	timer < T1	T2 < timer <t1< td=""></t1<>
satisfied	Start T1	x	Start T2	Start T1 and T2
condition		^	Reset C2	Reset C1 and C2



# 10BASE-T1S Trigger

## **Trigger Parameter Settings**

Click on the "10BASE-T1S Trigger Settings" in the toolbar, and the following window will appear.



# Travel Bus series

			/
Channel          10 BASE-T1S Port         LAPort         DATA         0         Coption         Preamble Count         Maximum         Maximum         Minimum         6         ~ 1         Reference PointAdjust         1st Position         20 ns         60 ns         Simple Trigger         Start of frame         End of frame         COMMIT_SYNC         SSD	Clause Trigger Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1  Event 1  Destination Address XXh - XXh
BEACON		Timer 1	Advanced Setting >>
ESD BRS ESD JAB ESD OK		Timer 2	. Second douing .



Since TravelBus has specially designed channels for 10BASE-T1, the 10BASE-T1S trigger settings in the TravelBus software will include additional channel source options.

- 1. Channel: Configure the Data channel.
- 2. Option

Preamble Count: Set the number of Preamble bits.

**Reference Point Adjust:** Adjusts the reference point for logic level determination.

- 3. Simple Trigger: Configure the trigger packet.
- 4. Clause Trigger: Please refer to the Parallel Clause Trigger description for details.
- 5. State: This section displays the detailed trigger conditions within each level of the trigger process on the left. Users can specify values for Destination Address, Source Address, Ethertype/Length, or Data, or leave 'X' as a wildcard for any value.



# **BiSS-C Trigger**

# BiSS-C Trigger Parameter Settings

Click on the "BiSS-C Trigger Settings" in the toolbar, and the following window

will appear.			
M BiSS-C Trigger Settings			×
Channel	Clause Trigger		
MA A0 C SLO A1 C Option Serial data length 12 Type of data CDM V	Run State 1	→ True → False → Trigger → Trigger *	State 1
Simple Trigger Start of frame Stop of frame		<ul> <li>State x 7</li> <li>Counter x 2</li> </ul>	Bypass 0 byte(s) Data Data Size 0 V
Error Trigger			
CRC6 Error		Timer 1 Timer 2	Advanced Setting >>
O Default			V OK X Cancel

1. Channel: Select channels.

#### 2. Option:

- I. Serial data length: Set SCD packet length, the default is 12 bits, 255 bits is the maximum.
- II. Type of data: Select the CDM or CDS packet.
- 3. Simple Trigger: Specific trigger function of BiSS-C.
- 4. Error Trigger:

CRC6 Error/CRC4 Error: Trigger CRC6 or CRC4 error of BiSS-C.

- 5. Clause Trigger: Please reference Clause Trigger chapter.
- 6. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the CTS, Commands, IDL and Data fields, default value is XX means "don't care".



X

# **CAN Trigger**

# **CAN Trigger Settings**

Click CAN Trigger in the toolbar and will show the dialog as the following  $\,^\circ$ 

M CAN Trigger Settings

Channel	Clause Trigger		
	Run V State 1	→ True → False	State 1 Event 1 Trigger On 11 Bits ID
Data Rate		> Trigger	ID XXXh Data
CAN FD  ISO-CRC O Non ISO-CRC Data Phase		→ 🛡 Trigger ×	Data Position Offset       Data Offset
5M bps Sample Point [80%]		<ul> <li>State x 7</li> <li>Counter x 2</li> </ul>	Byte 3 XXh Byte 4 XXh Byte 5 XXh Byte 6 XXh
Start of frame End of frame Data frame Remote frame			Byte 7 XXh Byte 8 XXh
Error frame Overload frame		Timer 1	Advanced Setting >>
ACK Error CRC Error		Timer 2	

# Travel Bus series

M CAN Trigger Settings				×
Channel	Clause Trigger			
CAN Port LAPort CAN L 0	Run State 1	→ True → False → Trigger	ID	+ OR its ID VXXh
500K v bps CAN FD			Data Data Position Offset	
<ul> <li>ISO-CRC</li> <li>Non ISO-CRC</li> <li>Data Phase</li> </ul>	L.	→ ▼ Trigger ×	Data Offset 0 Byte 1 XXh	byte(s) Byte 2 XXh
5M bps Sample Point [80%]		<ul> <li>State x 3</li> <li>Counter x 2</li> </ul>	Byte 3 XXh Byte 5 XXh	Byte 4 XXh Byte 6 XXh
Simple Trigger		-	Byte 7 XXh	Byte 8 XXh
Start of frame End of frame Data frame Remote frame				
Error frame		Timer 1		Advanced Setting >>
Overload frame		Timer 2		Auvanceu Setting >>
CRC Error				



Since TravelBus has specially designed channels for CAN, the CAN trigger settings in the TravelBus software will include additional channel source options.

- 1. **Channel:** Configure the CAN interface (supported only on TravelBus B series models) or set to LA channels.
- 2. Data Rate: CAN data rate. Users could type the data rate if no data rate is available.
- 3. Simple Trigger: Specific trigger function of CAN.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; there are 11 Bits ID, 29 Bits ID, Data, 11 Bits ID + Data and 29 Bits ID + Data selections in the Trigger On; selecting one of them and typing the trigger values in the ID or Data fields, default value is XX means "don't care".



# DALI2 Trigger

## **DALI Trigger Settings**

Click DALI Trigger in the toolbar and will show the dialog as the following.

👖 DALI Trigger Settings					×
Channel	Clause Trigger				
DALI 0  Data Rate Data Rate Data Rate Data Rate Simple Trigger C Start of frame End of frame		True Trigger Trigger State x 7 Counter x 2	State 1  Event 1  102  Short Address Address byte  Short Address = 0  Data byte  0_OFF  Data (8 bits)  Address byte Data 01	Custome Arc power	]
		Timer 1 Timer 2		Advanced Setting ≻	>
Default			<b>√</b> 0	K 🗙 Canc	el

- 1. Channel: Select channels.
- 2. Simple Trigger: Trigger specific of DALI.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- State: Show the details of trigger condition in every state as left side; selecting the trigger type of DALI (102, 103), command type (short address, group address, broadcast, response, special command), or custom cmd.



# **DPAux Ch Trigger**

M DP Aux Trigger Settings				×
Channel	Clause Trigger			
DP_Aux A0 Data Rate Data Rate Sorple Trigger SOF(Source) EOF(Source) SOF(Sink) EOF(Sink) No Reply	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1	
		Timer 1	Advanced Setting >>	
		Timer 2		

#### **Travel Bus series**

M DP_AuxCh Trigger Settings		×
Channel	Clause Trigger	
DP_AUX Port LA Port DP_Aux 0	Run     State 1 $\checkmark$ $\rightarrow$ $\checkmark$ $\rightarrow$ $\rightarrow$ $False$ $\rightarrow$ $Trigger$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$	+ OR
1000     KHz       Simple Trigger       SOF(Source)       EOF(Source)       SOF(Sink)       EOF(Sink)       EOF(Sink)       No Reply	► Trigger ×	XX XX XX XX XX
	Timer 1 Advanced	Setting >>
	Timer 2	
Default	✓ ОК	× Cancel



Since TravelBus has specially designed channels for DP Aux, the DP Aux trigger settings in the TravelBus software will include additional channel source options.

- 1. Channel: Configure the DP Aux channel
- 2. Data Rate: Configure the DP Aux data rate
- 3. Simple Trigger: Triggers on common basic packets. Enabled when selected.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: This section displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the packet as Request or Reply, fine-tune Command settings, or specify trigger values for the Data packet content. Alternatively, 'X' can be used as a wildcard to represent any value.



# eSPI Trigger

### eSPI Trigger Settings

Click eSPI Trigger in the toolbar and will show the dialog as the following.

👖 eSPI Trigger	Settings						?	×
Channel		Clause Trigger						
CS#	A0 🌲	Run		State 1				
SCLK	A1 🌲	1 × ×	> True			Logic	OR 🔾 Logic	AND
I/O 0	A2 🌲	State 1	<b>N</b> -1	Event 1				OR
I/O 1	A3 🌲		> False	Command	Any Command ()	XXh)		-
I/O 2	A4 🌲		> Trigger	Response	Any Response ()	(Xh)		•
I/O 3	A5 🗘			Data Dir	Command	O Res	ponse	_
Alert	A6 🗘			Data Offset	Any Ofs	[ D		□0+
Start up setting	ns				mmand PCode		sponse sponse	
			└── <b>T</b> rigger ``		XXh		XXh	
Single Mode			-					
Alert From I/	<u> </u>		🛉 State x 7					
CRC Check	Enable 🔻		🕂 Counter x 2					
Trigger on								
Format E	rror							
OPCode	Error							
Respons	e Error							
Status Er	ror							
CRC Erro	or		Timer 1			Adv	anced Setting	>>
			Timer 2					
tCLQV 15ns								
Default						🗸 ОК	🗙 Car	ncel

- 1. Channel: Select channels.
- 2. Startup settings: Set the initial parameters of eSPI.
- 3. Trigger on: Trigger specific error of eSPI.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- State: Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Response fields, default value is 00h.
  - I. **Data Dir:** Trigger the data in the Command or Response.

Timestamp	OpCode/Response	CycType	Tag	LEN	Address	DO	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
-0.00000245 S	GET CONFIGURATION(21)			_	0010									_		5.5	
0.00000086 5	ACCEPT(08)					13	11	00	00						0305	95	
0.000003 S	SET_CONFIGURATION (22)			_	0010	01	11	00	00							25	-
0.000005935 S	ACCEPT(08)														030F	98	
0.000008455 5	GET_STATUS(25)															FB	
0.000009365 5	ACCEPT(08)														030F	98	
0.001601195 5	GET_CONFIGURATION(21)				0010											58	
0.001602795 S	ACCEPT(08)					13	11	00	00						0302	95	
0.001606635 S	SET_CONFIGURATION (22)				0010	01	11	00	00							25	
0.001609575 S	ACCEPT(08)														030F	98	



II. Data Offset: Trigger the data from start of data frame without any offset. For example, setting D0 13h will check the first byte of data frame. With any offset, the siganl would be triggered by the byte pattern. For instance, setting D0+ XXh D1+ 11h, and the byte pattern of XXh and 11h will be triggered regardless of the position of the data.



# HIDoverl2C Trigger

## HIDoverI2C Trigger Settings

Click HIDoverI2C Trigger in the toolbar and will show the dialog as the

### following.

III HIDoverl2C Trigger Setti	ngs			×
Channel	Clause Trigger			
SCL A0 SDA A1 Simple Trigger Start of frame Repeat Start Stop of frame ACK NACK	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1	+ OR
		Timer 1		
		Timer 2	Advanced Settin	ig >>

#### **Travel Bus series**



👖 HIDoverl2C Trigger Setti	ngs		×
Channel	Clause Trigger		State 1
<ul> <li>○ I2C Port</li> <li>● LAPort</li> <li>SCL</li> <li>0 \$</li> <li>SDA</li> <li>1 \$</li> </ul>	State 1	→ True → False → Trigger	Event 1 OR Address Mode 7-BitAddressing
Simple Trigger Start of frame Repeat Start Stop of frame ACK NACK		Trigger *	Value R/W ACK XXh ••• •• •• Data
		Timer 1	Advanced Setting >>
		Timer 2	

Since TravelBus has specially designed channels for I2C, the HID Over I2C settings in the TravelBus software will include additional channel source options.

- Channel: Available only on TravelBus B series models, or set to LA channels.
- 2. Simple Trigger: Configure I2C Specific Frame Trigger.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: This section displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values in the Value, R/W, ACK, and Data fields, or use 'X' as a wildcard for any value.

The Data field can be set to HID descriptor as a trigger condition. When the trigger item is set to descriptor, the R/W field will automatically switch to Read mode.



# HyperBus Trigger

## HyperBus Trigger Settings

Click HyperBus Trigger in the toolbar and will show the dialog as the following.

M HyperBus Trigger Settings				×
Channel	Clause Trigger			
			State 1 Event 1	🛉 OR
CLK A1	State 1	→ True → False	Command/Address Bit	
RWDS1 A12	•		CA0[47:40] XX CA1[31:24] XX	CA0[39:32] XX CA1[23:16] XX
○ x8 ● x16 Settings			CA2[15:8] XX	CA2[7:0] XX
Quick Setup     User Defined	L,	🛡 Trigger 🗙	Data	edOffset
D0 (LSB) A4		🛉 State x 7	Any Offset O Fix	edOffset 0
RWDS2 A13	•	Counter x 2	XX XX	
Invert R WDS			4 5	6 7
Mode Hyper Flash				
Latency 7 CMD/Write CLK Delay = Ons				
		Timer 1		Advanced Setting >>
Read CLK/R WDS Delay = Ons		Timer 2		
Reau CLAAR WDS Deny = 015				
Simple Trigger				
Start of Frame				
<ul> <li>Default</li> </ul>			✓ OK	X Cancel

#### 1. Channel:

- I. CS、CLK、RWDS1、RWDS2: Configure HyperBus Channel.
- II. Using CLK to latch Read Data: Uses CLK to latch Read Data. Enabled when selected.
- III. DATA:
  - **x8 x16:** Configure the Data Bus Width.
  - Quick Setup 

     User Defined: Users can either use the Quick
     Setup function to batch-configure DATA channels or manually
     define each DATA bit channel.
  - **Settings:** Configure the Data Arrangement format.
- **IV.** Invert CLK: Reverses the CLK signal. Enabled when selected.
- Invert RWDS respectively: Independently inverts the RWDS1 & RWDS2 signals. Enabled when selected.
- **2. Mode:** Can be set to HyperFlash or HyperRAM.



- **3.** Latency: Sets the number of Sample Points for latency.
- CMD/Write CLK Delay 
   Read CLK/RWDS Delay: Configures the delay time for commands, write clock, read clock, and RWDS.
- 5. Clause Trigger: Please reference Parallel Clause Trigger chapter.
- 6. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values in the Command/Address Bit and Data fields, or use 'X' as a wildcard for any value.



 $\times$ 

# I<sup>2</sup>C Trigger

## I2C Trigger Settings

Click I2C Trigger in the toolbar and will show the dialog as the following.  $\rm I2C \, Trigger \, Settings$ 

Channel	Clause Trigger		
	Run	:	State 1
SCK A0	State 1	> True	Event 1 + OR
SDA A1		$\longrightarrow$ False	Address
		> Trigger	Mode 7-BitAddressing
			Value R/W ACK
Timing Violation			
🗌 Clock Stretching 🔹	L	→ 🛡 Trigger *	Data
Simple Trigger			Any Offset     Fixed Offset     Byte(s)
Start of frame		🖶 State x 7	Value 💻
Repeat Start		🕂 Counter x 2	XXh 🔽
Stop of frame			XXh 🔽
ACK			XXh 🔽
NACK			XXh 🔽
		Timer 1	Advanced Setting >>
		Timer 2	

#### **Travel Bus series**

M I2C Trigger Settings			×
Channel	Clause Trigger		
<ul> <li>I2C Port</li> <li>LA Port</li> <li>SCK</li> <li>SDA</li> <li>SDA</li> <li>Timing Violation</li> <li>Clock Stretching</li> <li>Simple Trigger</li> <li>Start of frame</li> <li>Repeat Start</li> <li>Stop of frame</li> <li>ACK</li> <li>NACK</li> </ul>	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1  Event 1 Address Mode 7-Bit Addressing Value R/W ACK XXh ACK ACK ACK ACK ACK ACK ACK ACK ACK ACK
		Timer 1	Advanced Setting >>
		Timer 2	



## Since TravelBus has specially designed channels for I2C, the I2C settings in the TravelBus software will include additional channel source options.

- 1. **Channel:** Configure the I2C interface (supported only on TravelBus B series models) or set to LA channels.
- 2. Simple Trigger: Configure I2C specific frame trigger.
- **3. Timing Violation:** Trigger based on timing condition violations.

JUL Timing Violation Settings		×
Timing Violation (Unit: ns / Range: 5 ns ~ 286.7 us)		
tSU;STA 800 tSU;DAT 50 tSU;STO 800	tLOW	800
tHD;STA 800 tHD;DAT 50 tBUF 2500	thigh	300
SDA	1 1 1	
O Default	✓ OK	X Cancel

4. Clock Stretching: Triggers on Clock Stretching events. Enabled when

selected.						
		×				
Clock Stretching Settings						
Clock stretching						
Timeout check (Range: 0 n	Timeout check (Range: 0 ns ~ 67 ms)					
Violation check						
Default	🗸 ОК	X Cancel				

- 5. Clause Trigger: Please reference Parallel Clause Trigger chapter.
- 6. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can specify trigger values for Value, R/W, ACK, and Data fields or use 'X' as a wildcard for any value.
  - I. The Data field allows up to 4 Bytes to be set. Unused fields should be



filled with XXh to indicate any value. Additionally, users can click the equal sign ("=") next to the set value to modify the trigger condition to "not equal to" the specified value.

- **II.** The input field can contain the required trigger Data or 'X' to represent any value. When entering values:
  - Hexadecimal values should end with 'h'.
  - Binary values should end with 'b'.
  - Decimal values do not require a suffix.
- **III.** Trigger Data Offset (Offset):
  - i. Any Offset: Triggers when valid **Data** that meets the set conditions appears anywhere in the **Data** field, regardless of offset.
  - ii. Fixed Offset: Triggers only when valid Data that meets the set conditions appears at the specified offset.



# I<sup>2</sup>S Trigger

## **I2S Trigger Settings**

Click I2S Trigger in the toolbar and will show the dialog as the following.

I2S Trigg	ger Sett	ings						×
Channel								
SCK	A0	-	WS	A1	\$	SD	A2	\$
Data Bits	8						-	Bits
Method	Data M	latch					-	]
Data Trigg	jer							
Channe	el	Bo	th	⊖ Lef	t	O F	Right	
Pattern	Unit	Va	lue	⊖ Volt	tage	0.0	IB	
Pattern	=							-
	00h							
Duration	n (# of f	rames)	1					
O De	fault			♥ 0	к		Cance	el

- Channel: Select Serial clock (SCK), word select (WS) and serial data (SD).
- 2. Data Bits: 1-32 bits, normally it is 8, 12, 16, 24 or 32.

### 3. Method:

Data Match : Trigger when the conditions matched.

Rising Edge : Trigger when it is a rising edge between two patterns.

Falling Edge : Trigger when it is a falling edge between two patterns.

Glitch : Trigger when there is a glitch.

- Mute : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X < +P.
- Clip : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of  $-P < X \cup +P > X$ .

Timing Violation : Provide 6 trigger conditions and this function will be enabled at 200 MHz sampling rate.

4. Data Trigger: Select Both, Left, Right channel and pattern unit.



# LIN Trigger

## LIN Trigger Settings

Click LIN Trigger in the toolbar and will show the dialog as the following.

🕕 LIN Trigger Settings					×
Channel	Clause Trigger				
CH A0	Run		State 1		
Data Rate	State 1	> True	Event 1		🛉 OR
9600 <b>y</b> bps		> False			
LIN 1.3		> Trigger			
Simple Trigger			ID XXh	Parity	Xh
Start of frame			Data Length	4	<b></b>
End of frame		🗲 📕 Trigger 🗡	Data		
Data frame			Byte 1 X	CXh Byte 2	XXh
Wake up frame		🛖 State x 7	Byte 3 X	CXh Byte 4	XXh
Sync frame		+ Counter x 2	Byte 5 X	CXh Byte 6	XXh
Error Trigger			Byte 7 X	CXh Byte 8	XXh
Sync error					
Parity error					
Stop bit error					
Checksum error		Timer 1			
Checksum mode				Advar	nced Setting >>
Classic Enhanced		Timer 2			
O Default				✓ ок	X Cancel
Delault				V UK	<ul> <li>Cancel</li> </ul>

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of LIN.
- 3. Error Trigger: Trigger specific error of LIN.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ID, Parity, Data Length and Data fields, default value is XX means "don't care". When select the LIN 2.2, Data Length field will be enabled.



# LPC Trigger

## LPC Trigger Settings

Click LPC Trigger in the toolbar and will show the dialog as the following.

肌 LPC Trigger	Settings					×
Channel		Clause Trigger				
LFRAME# / LAD[0] / LAD[1] /	A0 (*) A1 (*) A2 (*) A3 (*) A4 (*)	Run State 1	← True ← False ← Trigger	State 1 Event 1 Cycle Type Clk#	Start of Frame	+ OR
LAD[3] AUX Clock Edge Rising Edge Error Trigger START En CT/DIR E ADDR. E (Bus Mas	A5 + A6 + Fror Fror Fror Ster)		Trigger * State x 7 Counter x 2	START 1	XXXXb	
Channel (DMA)	r		Timer 1 Timer 2		Adva	anced Setting >>
MSize Err						
Default					♥ ОК	🗙 Cancel

- 1. Channel: Select LPC channels.
- 2. Clock Edge: Select Rising/Falling clock edge.
- 3. Error Trigger: Trigger specific error of LPC.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side;

typing or selecting the trigger values in the Cycle Type and its parameters,

default value is XX means "don't care". Switch  $=/\neq/>/\leq$  by click = button.

	Data Offset
	Fix Offset 0+
Data offset setting:	



# **MDIO Trigger**

## **MDIO Trigger Settings**

Click MDIO Trigger in the toolbar and will show the dialog as the following.

JUL MDIO Irigger Settings						^
Channel	Clause Trigger					
MDC A0	Run		State 1			
MDIO A1	State 1	> True	Event 1			🛉 OR
Clock Latch on		> False	ST	Any		-
Clock Latch on		> Trigger	OP	Any		•
Rising Edge 🔽				=		•
Preamble			PHYADR (P)	P=		XXh
32 🗘 bit(s)		→ <b>T</b> rigger *				
		• •	REGADR (R)	) = R=	XXh	
Simple Trigger		🛉 State x 7	DATA			
Start of frame		Counter x 2	DAIA		XXXXh	
Stop of frame						
TAError						
		Timer 1				1.0-1-1-1
		Timer 2			Advance	d Setting >>
		initial 2				
Default					ок	X Cancel

- **1.** Channel: Select MDC / MDIO channels.
- 2. Preamble: Select the length of preamble.
- **3. Simple Trigger:** Specific trigger function of MDIO.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ST, OP, PHYADR, REGADR and DATA fields, default value is XX means "don't care".

PHYADR(P) / REGADR(R) fields provided the range function:

=	,
=	
!=	
>=	
<=	
In Range	
Not In Range	



## MII / RMII / GMII / RGMII Trigger

**BusFinder/LA:** Click MII / RMII / GMII / RGMII Trigger in the toolbar and will show the dialog as the following.

MII/RMII/GMII/RGMII Trigger Sett	ings	:
Standard Settings	Clause Trigger	
Type MII 💌	Run	State 1
Clk Latch Rising	State 1	Event 1 + OR
RMII Cik Normal	> False	Destination Address
	> Trigger	Byte 1 XXh Byte 2 XXh Byte 3 XXh
Channel TX RX	,	Byte 4 XXh Byte 5 XXh Byte 6 XXh
		Source Address
EN A5 2 DV A17 2		Byte 1 XXh Byte 2 XXh Byte 3 XXh
ER A6 🗘 ER A18 🗘	🛏 🤍 Trigger	Byte 4 XXh Byte 5 XXh Byte 6 XXh
COL A7 🗘	State x 5	Ethertype/Length TX/RX
		Byte 1 XXh Byte 2 XXh TX ORX
Data Settings: 🌼	🛉 Counter x 2	Data
Phase Delay = 0 sample(s)		Byte 1 XXh Byte 2 XXh
		Byte 3 XXh Byte 4 XXh Byte 5 XXh Byte 6 XXh
Simple Trigger		Byte 7 XXh Byte 8 XXh
Start of frame		
End of frame	Timer 1	Advanced Setting >>
Format Error	Timer 2	
Frame Error		
CRC Error		

**Travel Logic/MSO:** Click MII / RMII / RGMII Trigger in the toolbar and will show the dialog as the following.

MII/RMII/RGMII Trigger Settings	
Standard Settings	Clause Trigger
Type MII  Clk Latch Rising	Run State 1 State 1 State 1 Fvent 1 Fvent 1 Fvent 1 Fvent 1
RMII Cik Normal	False Destination Address
Channel	Byte 1         XXh         Byte 2         XXh         Byte 3         XXh           Byte 4         XXh         Byte 5         XXh         Byte 6         XXh
TX RX	Source Address
EN 5 0V 15 0	Byte 1 XXh Byte 2 XXh Byte 3 XXh Byte 4 XXh Byte 5 XXh Byte 6 XXh
ER 6 COL 7	Ethertype/Length TX/RX
	State x 7 Byte 1 XXh Byte 2 XXh TX O RX
Data Settings:	Counter x 2 Data
Phase Delay = 0 sample(s) Simple Trigger	Byte 1 XXh Byte 2 XXh Offset Byte 3 XXh Byte 4 XXh 0  Byte 5 XXh Byte 6 XXh Byte 7 XXh Byte 8 XXh
Start of frame	
Format Error	Timer 1 Advanced Setting >>
Frame Error	Timer 2
CRC Error	



#### 1. Standard Settings:

- Type: Sets the decoding category. GMII measurement is not supported on TravelLogic and MSO, except for BusFinder/LA models. Additionally, to enable RGMII, the sampling rate must be set to 1 GHz or higher.
- II. **Clk Latch:** Configures whether data is latched on the rising or falling edge of the CLK signal.
- III. RMII CIk: Sets the CLK mode for RMII, applicable only when the measurement category is set to RMII.

#### 2. Channel:

- I. **TX:** Configures the TX channel, excluding the Data channel.
- **II. RX:** Configures the RX channel, excluding the Data channel.
- **III.** Data Setting: Assigns channels for TX Data and RX Data.
- 3. Phases Delay: Configures the Phase Delay, measured in sample points.
- **4. Simple Trigger:** Provides basic trigger conditions, such as Start of Frame and End of Frame. Enabled when selected.
- 5. Clause Trigger: Please reference Parallel Clause Trigger chapter.
- 6. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values for Destination Address, Source Address, or use "X" as a wildcard for any value.



# MiniLED Trigger

### MiniLED Trigger Settings

Click MiniLED Trigger in the toolbar and will show the dialog as the following.  $$$M$ MiniLED Trigger Settings $$\times$$ 

Channel	Clause Trigger		
Channel DCLK 0  LE 1  Data 2  DCLK Rate 20 MHz Option (GCLK) Magnification	Clause Trigger Run State 1	→ True → False → Trigger → Trigger *	State 1  Event 1  Command (LE high)  DCLK edge count  Data (LE low)  Word size  Vord size  XX  XX  XX  XX  XX  XX  XX  XX  XX
Latch data       Rising       DDR mode		Counter x 2	4-7 XX XX XX XX XX 8-11 XX XX XX XX 12-15 XX XX XX XX XX
		Timer 1	Advanced Setting >>
Delay           0         \$ sample		Timer 2	
Default			V OK X Cancel

- **1. Channel:** Configures the channels for DCLK, LE, and Data.
- 2. DCLK Rate: Sets the speed of DCLK.
- 3. Option (GCLK):
  - I. Magnification: Sets the simulation CLK multiplier relative to DCLK.
  - **II.** Latch Data: Determines whether Data is latched on the rising or falling edge.
    - **DDR mode:** Enables DDR mode when selected.
  - **III. Delay:** Configures the delay time, measured in sample points.
- 4. Clause Trigger: Please reference Parallel Clause Trigger chapter.
- 5. State: Displays the detailed trigger conditions within each level of the trigger process on the left. In the Command field, enter the DCLK edge count value, while in the Data field, enter a specific trigger value or use 'X' as a wildcard for any value.



# MIPI I3C Trigger

#### **MIPI I3C Trigger Settings**

Channel	Clause Trigger			
	Run	St	ate 1	
SCK A0	State 1 X	→ True	Event 1	
SDA A1		→ False	Address Value R/W	ACK
		→ Trigger	XXh	<b>• •</b>
Timing Violation			Common Command Code /	Transition Bit
Simple Trigger			XXh	▼▼
Start of frame Repeat Start Stop of frame	L , u	Trigger *	Data	) Fixed Offset
Error Trigger	💠 St	tate x 7	0 🗘 E	Byte(s)
SDR	🛨 C	ounter x 2	XXh -	
TE0			XXh -	
TE1			XXh	
TE2			XXh	
TE3 TE4				
TE5				
DDR	1	Timer 1		Advanced Setting >>
CRC Parity	1	Timer 2		
Preamble Read DDR NACK				

#### **Travel Bus series**

∭ I3C Trigger Settings			×
Channel	Clause Trigger		
<ul> <li>I2C Port</li> <li>LAPort</li> <li>SCK</li> <li>D</li> <li>SDA</li> <li>Timing Violation</li> <li>Simple Trigger</li> <li>Start of frame</li> </ul>	Run State 1	→ True → False → Trigger	State 1
Repeat Start Stop of frame		+ State x 7	Any Offset     Fixed Offset     Byte(s)
SDR TE0 TE1 TE2 TE3 TE4 TE5		Counter x 2	XXh      ▼       XXh      ▼       XXh      ▼       XXh      ▼
DDR		Timer 1	Advanced Setting >>
CRC Parity Preamble Read DDR NACK		Timer 2	



Channel: Configure the I3C channel using either I2C Port or LA Port.

Simple Trigger: Set triggers for I3C Start, Repeat Start, or Stop events.

State: Categorized into Address, Common Command Code (CCC), and Data.

For the Data parameter, two offset options are available:

Any Offset (default): Triggers when the first detected I3C data matches the specified value.

Fixed Offset: Specifies both the I3C data value and its exact position (offset).

An offset of 0 triggers on the first data byte, with the offset unit in bytes.

Since some I3C CCCs contain specially formatted data, the following describes their specific trigger settings:

- 1. Triggering on RSTDAA (06h) / ENTDAA (07h) data
  - a. Event 1 CCC is set to RSTDAA (06h) / ENTDAA (07h).

I3C Trigger Settings					×
Channel	Clause Trigger				
L2C Port     LAPort     SCK     0     CAPort     SDA     1     CAPORT     SDA     Timing Violation     Simple Trigger     Start of frame     Repeat Start     Stop of frame  Error Trigger  SDR     TE0     TE1     TE2     TE3     TE4     TE5	Run State 1	True False Trigger Trigger * State x 6 Counter x 2	Address Value	Write 💌	Bit
DDR		Timer 1		Advanc	ed Setting >>
CRC Parity Preamble Read DDR NACK		Timer 2			
O Default				✔ ОК	× Cancel

b. Event 2: When selecting ENTDAA, the entered data width must be 9 bits and is fixed to Fixed Offset.



Ⅲ I3C Trigger Settings			>
Channel	Clause Trigger		
I2C Port     LAPort     SCK     0     0     0     SDA     1     0     Timing Violation  Simple Trigger     Start of frame     Repeat Start	Run State 1	→ True → False → Trigger → Trigger *	State 1
Stop of frame		🕂 State x 6	0 🗘 Unit(s) 🗹 ENTDAA
SDR TE0 TE1 TE2 TE3 TE4 TE5		Counter x 2	101h
DDR		Timer 1	Advanced Setting >>
CRC Parity Preamble Read DDR NACK		Timer 2	
Default			V OK X Cancel

2. Triggering on EHTHDR0 (20h) / EHTHDR1 (21h) / EHTHDR2 (22h) HDR

Data: The data format consists of a 16-bit payload.

IIC Trigger Settings					>
Channel	Clause Trigger				
O I2C Port ● LAPort SCK 0 ↔ SDA 1 ↔ Timing Violation Simple Trigger ■ Start of frame ■ Repeat Start Stop of frame	Run State 1 *	True True False Trigger Trigger	State 1  Event 1  Address Value RA  TEh Wr Common Command Cr  20h EHTHDR0(Broad HDR Data  Any Ofset	ite 💽 ode / Transition dcast) O Fixed	Bit -
Error Trigger SDR TE0 TE1 TE2 TE3 TE3 TE4 TE5		<ul> <li>State x 7</li> <li>Counter x 2</li> </ul>	Preamble Payloa		Nord(s)
DDR CRC Parity Preamble Read DDR NACK		Timer 1 Timer 2		Advance	ed Setting >>
<ul> <li>Default</li> </ul>				🗸 ок	X Cancel



# **MIPI RFFE Trigger**

### **MIPI RFFE Trigger Settings**

Click MIPI RFFE Trigger in the toolbar and will show the dialog as the following. MIPI RFFE Trigger Settings  $\times$ 

Channel	Clause Trigger				
Channel SCLK 0 SDATA 1 Error Trigger Start of frame Bus Park Cycle Parity Error Frame Error	Run State 1	→ True → False → Trigger Trigger * State x 7 Counter x 2	State 1  Event 1  Any_Command  SA/ MID  Xh High X  Any Offset  Fixed Offset  Byte 1 XXh  Byte 3 XXh  Byte 5 XXh  Byte 7 XXh	Data  Data  Data  byte(s)  Byte 2  Byte 4  Byte 6	CR
		Timer 1		Advan	ced Setting >>
		Timer 2		Advan	iced Setting >>
<ul> <li>Default</li> </ul>				✓ ОК	X Cancel

- 1. Channel: Configure the channels for SCLK and SDATA.
- 2. Error Trigger: Provides basic trigger conditions, such as Start of Frame and End of Frame. Enabled when selected.
- 3. Clause Trigger: Please reference Parallel Clause Trigger chapter.
- 4. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the Command type, enter a specific Address trigger value, or specify a Data trigger value, with the option to use 'X' as a wildcard for any value.



# **MIPI SPMI Trigger**

### **MIPI SPMI Trigger Settings**

Click MIPI SPMI Trigger in the toolbar and will show the dialog as the following.

MIPI SPMI Trigger Settings					×
Channel	Clause Trigger				
SCLK A0	Run	:	State 1		
SDATA A1	State 1 ×	> True	Event 1		🕂 OR
Arbitration OFF		> False	Device Address	X	h
Trigger On		> Trigger	Command	XX	(h
SSC			Data Address	XXX	CXh
Bus Timeout			Data		
No Resp. Frame		→ <b>▼</b> Trigger *	XXh XX	h XXh	XXh
Error Trigger		/ Ingger	XXh XX	h XXh	XXh
CMD Frame Format		💠 State x 7	XXh XX	h XXh	XXh
CMD Parity		-	XXh XX	h XXh	XXh
Data Addr. Parity		+ Counter x 2			
Data Frame Parity					
Bus Park / Bus Handover					
Non ACK Aribitration Format					
Bus Timeout		Timer 1		Advar	nced Setting >>
0		Timer 2		Advar	lood ootang '
O Default				🛩 ОК	X Cancel

- 1. Channel: Configure the channels for SCLK and SDATA.
- 2. Arbitration OFF: Disables Arbitration. Enabled when selected.
- **3. Trigger On:** Configure specific special trigger conditions. Enabled when selected.
- **4. Error Trigger:** Provides basic trigger conditions, such as CMD Frame Format and CMD Parity. Enabled when selected.
- 5. Bus Timeout: Set the timeout duration.
- 6. Clause Trigger: Please reference Parallel Clause Trigger chapter.
- 7. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the Command type, enter a specific Address trigger value, or specify a Data trigger value, with the option to use 'X' as a wildcard for any value.



# ModBus Trigger

### ModBus Trigger Settings

Click ModBus Trigger in the toolbar and will show the dialog as the following.

Channel Clause Trigger Run State 1	
Idle High   Tx   A0   Rx   A1   Baud Rate   9600   bps   Option   + State x 3   + Counter x 2	Pak
Parity Error Timer 1 Advanced Setting 2	>>
Break/Idle frame Timer 2	

### Travel Bus series

Channel Clau	use Trigger			
O UART Port				
LAPort Idle High Tx 0 Rx 1 Rx 1 Parity None Parity None Mode ASCII Simple Trigger Start of frame		True False Trigger Trigger State x 3	State 1	OR
End of frame		Timer 1	L	
Parity Error		inner i	Advar	nced Setting >>
Break/Idle frame		Timer 2		



Since TravelBus has specially designed channels for UART, the ModBus settings in the TravelBus software will include additional channel source options.

#### Channel

UART Port / LA Port : Select ModBus channels.

#### **Baud Rate**

Select the baud rate and providing the manual input if no appropriate selection.

#### Option

Parity: Provide None/Odd/Even selections, none parity defaulted.

Mode: Provide ASCII/RTU mode, ASCII mode defaulted.

Support the 8-N-1 protocol under RTU mode, 8-N-2 protocol defaulted.

Parity	None	-
Mode	RTU	-
	N-8-1	

#### Simple Trigger:

Provide Start of frame, End of frame, Parity Error, Break/Idle frame triggers .

#### State:

Provide ASCII/HEX input mode by ASCII/RTU mode.

ASCII

RTU

State 1	State 1
Event 1	Event 1 + OR
O Rx Tx	O Rx Tx
Bypass 0 🗘 Data(s) after Break	Bypass 0 🗘 Data(s) after Break
Data (ASCII)	Data (Hex)
:1103	Data Size 2



# NAND Flash Trigger

### NAND Flash Trigger Settings

Click NAND Flash Trigger in the toolbar and will show the dialog as the

following.						
M NAND Flash Trigg	er Settings					×
Channel		8	Clause Trigger			
CLE	A8 A9	¢	Run	> True	State 1	R
RE# (W/R#) WE# (CLK)	A10 A11	¢	State 1	> False	Command	
CE# ✓ R/B#	A12 A13	÷		> Trigger	Address	
DQS     Invert RE# (W/F     Invert DQS	A14 (#)	\$		→ <b>T</b> rigger ×	3-Byte Row Addr.     Condition     Address =	-
DATA x8 Quick Setup User Defined	○ x16	ö		<ul> <li>State x 7</li> <li>Counter x 2</li> </ul>	Column/Feature XXXXh	
DQ0 (LSB)	A0	-			Data Offset	
Startup Mode					1st         2nd         3rd         4th           XXh         XXh         XXh         XXh	
tREA>= 20ns	tDQSQ >= 500	)ps		Timer 1	Advanced Setting >>	
Cmds. accept d	uring busy	•		Timer 2		
Busy time check		\$				
Default					V OK X Can	cel

- 1. Channel: Select CLE, ALE, RE, WE, CE, R/B, DQS channels.
- 2. DATA: Select x8 or x16 bits
  - Quick Setup: Only set DQ0(LSB), others will be set automatically.
     (e.g. LSB = B4, MSB = B11; LSB = B7, MSB = B14)

#### II. User Defined:

∭ I/O Cha	nnel Se	ttin	gs		×
1/00	B4	+	I/C	08	B12 🌲
I/O1	B5	\$	I/C	9	B13 🌲
I/O2	B6	•	I/C	010	B14 🌲
I/O3	B7	\$	I/C	D11	B15 🌻
I/O4	B8	\$	I/C	012	B16 🌻
I/O5	B9	÷	I/C	013	B17 🌲
I/O6	B10	\$	I/C	014	B18 🗘
1/07	B11	\$	I/C	015	B19 🗘
<ul> <li>Default</li> </ul>				✓ OK	X Cancel



#### 3. Startup Mode: Set DDR mode.

### 4. **tREA / tDQSQ:** Set tREA at SDR mode and tDQSQ at DDR mode.

#### tREA:

Time/Div:	7.5 ns			<b>P</b>	Ą								
Acquired:	11:47:26.693		-105 ns	97.5 ns	-90 ns	-82.5 ns	-75 ns	-67.5 ns	-60 ns	-52.5 ns	-45 ns	-37.5 ns	-30
		Idle		DO: 0	0		I	DO	00		1		DO:
	5 I/OO						Ï						
	6 I/O1												
	7 I/O2												
	8 I/O3												
	9 I/O4												
L	10 I/O5												
NAND Flash	<sup>ח</sup> 11 I/O6												
	12 I/O7												
	0 CLE												
	3 ALE					1	-						
	4 RE		10n		22.5n		7.5n		22.5n		12.	5ր	
	2 WE												
	1 (E1												
N	and Flark 13 R/B1												
Data Bus	125				00	)			) At	BĂ	49		

#### tDQSQ:

		Idle		DO: OE	I	DO: 48		DO: E5	Ī	DO: C3	DO: (
	O DQO							30n			15n
	1 DQ1		17.5n			27.5n				32.5n	
	2 DQ2		17.5n		12.5n		17.5	in _		27.5n	
	3 DQ3			32.5n						57.5n	
	4 DQ4										
	5 DQ5						17.5	in _		27.5n	
IAND Flash	6 DQ6									92.5n	
	7 DQ7								47.5	n	
	8 CLE										
	9 ALE										
	13 W/R		1	.2.5n		17.5n		12.5n		17.5n	12.5n
	12 CLK										
	14 CE1										
	10 R/B1										
Nand Fl-	, 15 DQS 📘		15n		15n		15n		15n		15n

5. Commands accepted during busy: Set NAND commands still could be triggered during busy state, default is 70h/FFh/78h/7Bh.

M Busy Command Setting	S	×
Commands		
1 70h	5 XXh	
2 FFh	6 XXh	
3 78h	7 XXh	
4 7Bh	8 XXh	
<ul> <li>Default</li> </ul>	VOK X Cance	al
Doradit		



## Trigger 70h during busy state:

cquired: 1	5:35:22.352	-100 ns			100 ns	200 ns	300	ns 	400 ns	500 ns	600 ns	
		Busy	R	EAD STAT	r. RĖG.(70)							Busy
	7 1/00								1			
	8 I/O1											
	9 I/O2								1			
	10 I/O3								1			
	11 I/O4											
	12 I/O5								1			
NAND Flash	13 I/O6											
	14 I/O7								1			
	0 CLE											
	1 ALE								1		1	
	5 RE											
	2 WE											
	6 (E1											
Nan	4 R/B1								1		1 I	
									1		1	
Data Bus	147									70		

6. Busy time check: Triggers when timing >= tBusy, providing 6 tBusy to check.

∭ Busy T	ime Settings	5				×
tBusy1	tBusy2	tBusy3	tBusy4	tBusy5	tBusy6	
tBusy (F	ange: 0.1us-	250ms)				
>= [2	250000					us
Comma	nd					
		1 XXh				
		2 XXh				
		3 XXh				
		4 XXh				
Default					✓ ОК Х	Cancel

#### Trigger the tBusy >= 25 us after NAND command (10h)

	Tdl	e PAGE PRO	G. #2(10)				Busy
	7 I/O0 8 I/O1						
	9 1/02			-		 	
	10 I/O3 📃					 	
	11 I/04						
NAND Flash	12 I/05 13 I/06			_			
	14 I/07						
	1 ALE				_		
	2 WE					 	
	6 CE1						
NandFla	🔥 4 R/B1		<u> </u>	->=25 us -			
Data Bus	147					10	



- 7. Clause Trigger: Please reference Clause Trigger chapter.
- 8. State: Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Address and Data fields, default value is XX means "don't care".



# **PMBus Trigger**

## **PMBus Trigger Settings**

Click PMBus Trigger in the toolbar and will show the dialog as the following.

M PMBus Trigger Settings			×
Channel	Clause Trigger		
PMBCLK A0 PMBDAT A1 PMBDAT A1 Clock Stretching Simple Trigger Start of frame Repeat Start Stop of frame ACK NACK Check PEC Group Command None Group CMD	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1  Event 1  Address(7b)   XXh  Command   XXh  Data  Any Offset  Fixed Offset  Byte(s)  XXh   XXh   XXh   XXh   XXh   XXh     XXh     XXh      XXh     XXh      XXh
<ul> <li>None Group CMD</li> </ul>		Timer 1	Advanced Setting >>
		Timer 2	

## Travel Bus series

M PMBus Trigger Settings	-		×
Channel	Clause Trigger		
<ul> <li>I2C Port</li> <li>LA Port</li> <li>PMBCLK</li> <li>PMBDAT</li> <li>Clock Stretching</li> <li>Simple Trigger</li> <li>Start of frame</li> <li>Repeat Start</li> <li>Stop of frame</li> <li>ACK</li> <li>NACK</li> <li>Check PEC</li> <li>Group Command</li> <li>None Group CMD</li> </ul>	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1  Event 1  Address(7b)  XXh  Command  Extended  Extended  XXh  Data  Any Offset  Fixed Offset  Byte(s)  XXh    XXh
		Timer 1	Advanced Setting >>
		Timer 2	



Since TravelBus has specially designed channels for I2C, the PMBus settings in the TravelBus software will include additional channel source options.

- 1. Channel: Configure the I2C interface or LA channel.
- 2. Simple Trigger: Set PMBus-specific frame trigger.
- 3. Check PEC: Configure the trigger for Packet Error Checking (PEC).
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values for Address, Command, and Data, or use 'X' as a wildcard for any value.

**I.** The Data field allows up to 4 Bytes to be set. Unused fields should be filled with XXh to indicate any value.

**II.** The input field can contain the required trigger Data or 'X' as a wildcard.

- Hexadecimal values should end with 'h'.
- **Binary** values should end with 'b'.
- **Decimal** values do not require a suffix.

#### III. Data Offset Triggering:

- Any Offset: Triggers when valid Data that meets the set conditions appears anywhere in the Data field, regardless of offset.
- **Fixed Offset:** Triggers only when valid Data that meets the set conditions appears at the specified offset.



# **ProfiBus Trigger**

## **ProfiBus Trigger Settings**

Click ProfiBus Trigger in the toolbar and will show the dialog as the following.

ProfiBus Trigger Settings	;				×
Channel	Clause Trigger				
CH A0 Option Start bit is Low Data Rate 9600 bps	Run State 1	→ True → False → Trigger	State 1 Event 1 Start Delimiter (SD) DA XXtr FC XXtr EDH 16t	FCS	OR     XXh     XXh     XXh     XXh
Simple Trigger Start of frame End of frame Chksum Error SD Error ED Error LE Error		<ul> <li>State x 7</li> <li>Counter x 2</li> </ul>			
DA/SA Error Parity Error Parity Setting		Timer 1		Advan	ced Setting >>
Even		Timer 2			
<ul> <li>Default</li> </ul>				✔ ОК	X Cancel

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of ProfiBus.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SD packet and its fields, default value is XX means "don't care".



# SD/eMMC Trigger

### **SD/eMMC Trigger Settings**

Click **SD/eMMC** Trigger in the toolbar and will show the dialog as the

following •

∭ SD/eMMC Trigger Sett	ings				×
	ings Clause Trigger Run State 1	→ True → False → Trigger	State 1 Event 1 Command Any Command DATA0 = ST Comma X X XXh Stuff Bits[31: XXh Stuff Bits[23: XXh	and (Descrip	onse User Defined
✓ CMD Gap Time 10 ms tODLY Settings Host -> Device 0ps Device -> Host 5ns		♣ State x 7 ♣ Counter x 2	Stuff Bits[23: XXh Stuff Bits[15: XXh Stuff Bits[7:1 XXh CRC XXh	8]	
<ul> <li>DATA Settings</li> <li>Error Check Settings</li> </ul>					
O Default				✓ OK	× Cancel

1. Channel: select CLK, CMD as the trigger channel

AUX can be used for checking power state before running CRC error check, disabled by default.

2. Protocol: select SD or eMMC trigger

Protocol			
I SD O eM	MC		
<ul> <li>CMD Only</li> <li>CMD + RESP</li> </ul>			
Command	Response	Argument	CRC
CMD18:READ_MULTIPLE_BLOCK		000A 8000h	17h
	R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h
CMD12:STOP_TRANSMISSION		0000 0000h	30h
	R1b:CMD12:STOP_TRANSMISSION	0000 0B00h	3Fh

- 3. CMD Gap time: delay trigger between the two CMDs.
- **4. tODLY Settings:** set the phase delay time such that the device can latch valid command and response.



5. Error Check Settings: CRC7 error, CRC16 error, Timeout trigger are parallel structure with the Clause Trigger

Ι.	CRC	Error	Trigger:
----	-----	-------	----------

CRC Error Trigger	Timeout Trigger
Trigger on CMD	) (CRC7) error
Trigger on DATA	A (CRC16) error
Read CMD list fo	or CRC check
Cmd 17	✓ Cmd 18 ✓ Cmd 46 ✓ Cmd 53
Write CMD list fo	r CRC check
Cmd 24	<ul> <li>▼ Cmd 25</li> <li>▼ Cmd 47</li> <li>▼ Cmd 54</li> </ul>

- Trigger on CMD (CRC7) error: Check the CRC7 error on Command line.
- Trigger on DATA (CRC16) error: Check the CRC16 error on DATA lines.
- II. Timeout Trigger: provide 4 statements as following



C Error Trigger	Timeout Trigger	
Enable Timeout I		
Trigger on Data	meout after CMD/DATA	
CMD	CMD RESP. Time	
DAT	Time Data Data	
Trigger when w		
IIIgger when w		
<ul> <li>Trigger on Data</li> </ul>	DLE timeout before CRC status	
0145		
CMD	Time	
DAT	Data CRC Status	
Trigger when w	CRC Status time > 5 ms	
0 T		
Ingger on Bus	imeout after CRC Status	
CMD		
	Time	
DAT	Data CRC Status Busy	
Trigger when B	y time > 5 ms	
) Trigger on Bus	meout After CMD	
O Trigger on Bus	imeout After CMD	
CMD	CMD RESP.	
CMD DAT	CMD RESP. Busy Time	
CMD	CMD RESP. Busy Time	

- Trigger on Data timeout after CMD/DATA
- Trigger on Data IDLE timeout before CRC ststus
- Trigger on Busy timeout after CRC ststus
- Trigger on Busy timeout after CMD
- 6. Clause trigger settings: Please reference Clause Trigger chapter
- 7. Trigger settings



Event 1	🛉 OR
Command (	) Response
Any Command	-
DATA0 = X 0	1 User Defined
S T Command	(Description)
X X XXh	
Stuff Bits[31:24]	
XXh	
Stuff Bits[23:16]	]
XXh	
Stuff Bits[15:8]	]
XXh	
Stuff Bits[7:0]	J I
XXh	
CRC	
XXh 1	

#### SD/eMMC analysis result

Command Response		Argument (h)	CRC7 (h)	Frequency	
CMD23:SET_BLOCK_COUNT		00 00 08	BF	166MHz	
	R1 :CMD23:SET BLOCK COUNT	00 00 09 00	1D	166MHz	
CMD18:READ_MULTIPLE_BLOCK		00 00 1D 20	09	166MHz	
	R1 :CMD18:READ_MULTIPLE_BLOCK	00 00 09 00	D3	166MHz	
CMD23:SET_BLOCK_COUNT		00 00 00 08	BF	166MHz	
	R1 :CMD23:SET_BLOCK_COUNT	00 00 09 00	1D	166MHz	
CMD18:READ_MULTIPLE_BLOCK		00 00 1C 70	ES	166MHz	

#### Parameter :

DATA0 =  $X \ 0 \ 1$  : use Data0 to judge the R1 and R1b.

Input trigger value, input 'X' means don't care.

Append 'h' for HEX, 'b' for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

User Defined add the command reserved:

Command	Description	-
Cmd 1	Click To Edit	
Cmd 5	Click To Edit	
Cmd 14	Click To Edit	
Cmd 21	Click To Edit	
Cmd 22	Click To Edit	
Cmd 26	Click To Edit	
Cmd 31	Click To Edit	
Cmd 34	Click To Edit	•



# SD/eMMC Data Trigger

#### SD/eMMC Data Trigger Settings

Click **SD/eMMC Data** Trigger in the toolbar and will show the dialog as the following •

∭ SD/eMMC Data Trigger Setti	ngs	×
Protocol Select	Data Trigger Error Trigger	
SD O eMMC	✓ Start Data Trigger after READ command (CMD17/18)	
	Data Address XXh XXh XXh XXh	
Probe Select	✓ Start Data Trigger after WRITE command (CMD24/25)	
LA Probe	Data Address XXh XXh XXh XXh	
	🗌 Start Data Trigger after 🛛 CMD 0 - GO_IDLE_STATE 🌞 as Read 🔽 command	
DATA Settings	CMD Command Response	
O 8-bit Data	DAT	
4-bit Data	Pattern P - P - P - P - P - P - P - P - P - P	
O 1-bit Data		1
DDR Mode		
HS 400 (MMC)	Data Trigger Pattern	
Data Length (Byte)	Trigger when pattern(s) match	
512 💌	Pattern Size	
	BYTE 00 - 03 XXh XXh XXh XXh XXh	
	BYTE 04 - 07 XXh XXh XXh XXh XXh	
tODLY Settings	BYTE 08 - 11 XXh XXh XXh XXh XXh	
Host -> Device 0ps	BYTE 12 - 15 XXh XXh XXh XXh XXh	
Device -> Host 500ps		
Default	✓ OK X Cance	

- 1. **Protocol:** select SD or eMMC trigger
- 2. Probe Select: select CLK, CMD and AUX as the trigger channel.
- 3. Data Settings: select current bus width, byte, SDR, DDR of the test object
- **4. tODLY Settings:** set the phase delay time such that the device can latch valid command and response.
- 5. Data Trigger: set the patterns of data trigger.
- 6. Timeout Trigger: set the condition of idle time to trigger.



🔟 SD/eMMC Data Trigger Setting	gs	×
Protocol Select	Data Trigger Timeout Trigger	
SD O eMMC	Enable Timeout Trigger	
Probe Select LA Probe	<ul></ul>	
DATA Settings 8-bit Data 4-bit Data 1-bit Data DDR Mode HS 400 (MMC) Data Length (Byte) 512	O Trigger on Data IDLE timeout before CRC status  CMD DAT Data CRC Status Trigger when wait CRC Status time > 5 ms ▼  O Trigger on Busy timeout after CRC Status	
tODLY Settings Host -> Device Ops	CMD       Time         DAT       Data       CRC Status       Busy         Trigger when Busy time > 5       ms >         The trigger function will be turned on only after receiving the following command	
Device -> Host 500ps	Cmd 17 Cmd 18 Cmd 24 Cmd 25	
<ul> <li>Default</li> </ul>	✓ OK X Cancel	5



## SENT Trigger

### SENT Trigger Settings

Click SENT Trigger in the toolbar and will show the dialog as the following.

M SENT Trigger Settings		×
Channel	Clause Trigger	
SENT A0 Startup Clock Tick 3 us # of Nibbles 6 Version 2010/2016 SENT Pause OFF CRC Recom Message Fast Simple Trigger Start of Fast Start of Short Start of Enhanced Error Trigger	Run State 1 False Trigger Trigger State x 7 Counter x 2	State 1  Event 1  Slow Channel  Message ID Xh Data XXh Fast Channel  S & C Xh  # of Nibbles to Trigger 0  Nibble(s)  # #1~4 Xh Xh Xh Xh #5~8 Xh Xh Xh Xh Xh
Error Trigger Sync Pulse Error Pulse Period Error Enhanc. CRC Error Short CRC Error Fast CRC Error	Timer 1 Timer 2	Advanced Setting >>
<ul> <li>Default</li> </ul>		V OK X Cancel

- **1. Channel:** Configure the SENT channel.
- 2. Startup: Set the Startup conditions.
- **3. Simple Trigger:** Configure SENT-specific frame trigger. Enabled when selected.
- **4. Error Trigger:** Configure SENT-specific error trigger. Enabled when selected.
- 5. Clause Trigger: Please reference Clause Trigger chapter.
- 6. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the Slow Channel Message ID or Data (available only when the Message setting in Startup is set to Short or Enhanced) or specify details in the Fast Channel (available only when the Message setting in Startup is set to Fast).



### Serial Flash / SPI NAND Trigger

#### Serial Flash / SPI NAND Flash Trigger Settings

Click Serial Flash Trigger in the toolbar and will show the dialog as the

following.

∭ Serial Flash	h / SPI N	AND Flash Trigger Setting	gs			?	×
Channel		Clause Trigger					
CS#	0 🌲	Run		State 1			
SCLK	1 🗘	State 1	> True		Logic	OR O Logic	
	2 🗘		→ False	Event 1	▼ Co		OR
	3 🌲		> Trigger	Single Mode Single Mode		mmand	
	4 🗘			8 cycles	<b>XXh</b>	AND XXh	
Hold#/SIO3							
	6 ‡ 7 ‡		→ <b>▼</b> Trigger *		A	ddress	
	8 ‡			16b 24b 3		XXh	
	9 🗘		🛨 State x 7		Dum	imy cycles	
	10 🗘		+ Counter x 2		0	Dummy cyc	le(s)
CS# Glitch Tric	ager		-			Data	
None					Fix Offs	et 0 🗘 by	te(s)
Width < 1	I0ns			O In Out	E XXh	XXh XXh >	(Xh
✓ tSHSL >= 5	5ns		Timer 1		A		
			Timer 2		Adv	anced Settin	g >>
tCLQV >= 8.75	50ns		hindr 2				
<ul> <li>Default</li> </ul>					✓ OK	× Car	ncel

- 1. Channel: Select channels.
- 2. CS# Glitch Trigger: Trigger the glitch on CS# channel.
- 3. tSHSL / tCLQV: Set tSHSL / tCLQV.

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- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Command, Address and Data fields, default value is XX means "don't care".

Provided the Single / Dual / Quad / Octal mode.

Single Mode	
Single Mode	
Dual Mode	
Quad Mode	
Octal Mode	



## SMBus Trigger

### **SMBus Trigger Settings**

Click SMBus Trigger in the toolbar and will show the dialog as the following. MBus Trigger Settings

M SMBus Trigger Settings			×
Channel	Clause Trigger		
SMBCLK A0 SMBDAT A1 Protocols Select SMBus Clock Stretching		State x 7	State 1  Event 1  Address(7b)   XXh  Command   XXh  Data  Any Offset  Byte(s)  XXh   XXh
Simple Trigger Start of frame Repeat Start Stop of frame ACK		Counter x 2	XXh V XXh V XXh V
		Timer 1	Advanced Setting >>
Check PEC		Timer 2	

#### Travel Bus series

M SMBus Trigger Settings			×
Channel	Clause Trigger		
<ul> <li>I2C Port</li> <li>LAPort</li> <li>SMBCLK</li> <li>SMBDAT</li> <li>Protocols Select</li> <li>SMBus</li> <li>Clock Stretching</li> <li>Clock Stretching</li> <li>Simple Trigger</li> <li>Start of frame</li> <li>Repeat Start</li> <li>Stop of frame</li> </ul>	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1  Event 1  Address(7b)  Command  Address(7b)  Address(7b)  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  XXh  Address(7b)  Addr
		Timer 1	Advanced Setting >>
Check PEC		Timer 2	Addition of any



Since TravelBus has specially designed channels for I2C, the SMBus settings in the TravelBus software will include additional channel source options.

- 1. **Channel:** Configure the I2C interface (supported only on TravelBus B series models) or set to LA channels.
- 2. Protocols Select: Set the trigger for SMBus, SBS, or SPD protocols.
- 3. Simple Trigger: Configure SMBus-specific frame trigger.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values for Address, Command, and Data, or use 'X' as a wildcard for any value. The Command field will display different command formats based on the Protocols Select setting.

**I.** The Data field allows up to 4 Bytes to be set. Unused fields should be filled with XXh to indicate any value.

**II.** The input field can contain the required trigger Data or 'X' as a wildcard.

- **Hexadecimal** values should end with **'h'**.
- **Binary** values should end with 'b'.
- **Decimal** values do not require a suffix.
- III. Data Offset Triggering:
  - Any Offset: Triggers when valid Data that meets the set conditions appears anywhere in the Data field, regardless of offset.
  - **Fixed Offset:** Triggers only when valid Data that meets the set conditions appears at the specified offset.



## **SPI Trigger**

### **SPI Trigger Settings**

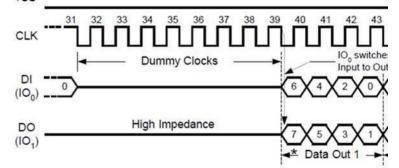
Click SPI Trigg	er in the toolbar	and will show	the dialog a	s the tollo	wing.
👭 SPI Trigger Setting	gs				×
Channel	Clause Trigger				
✓ CS 0 🜲	Run		State 1		
Clock 1	State 1	> True	Event 1		🛉 OR
MOSI 2		→ False	Data In		<b>•</b>
MISO 3		> Trigger	Data		
Frame guard time			Any Offset	○ Fixed	Offset
			0	Byte(s)	
	l	→ 🛡 Trigger 🎽	Data 1 🔿	XXh Data 5	XXh
10.00 🖶 us			Data 2 🛛	XXh Data 6	XXh
Option		+ State x 7	Data 3 🛛	XXh Data 7	XXh
Clock latch data on		🖶 Counter x 2	Data 4 🛛 🗙	XXh Data 8	XXh
Rising Edge					
Chip select					
Active Low					
Data output delay					
0 ns					
Word size					
8 v bit(s)					
<ul> <li>Default</li> </ul>				✓ OK	× Cancel

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- Channel: Select the channel. Depending on the mode, two to four 1. channels can be used.
- 2. Frame guard time: When CS is not selected, this value can be set to define the time threshold for recognizing the next Frame.
- **Option:** The Data Output Delay setting specifies how long the Latch Data 3. should be delayed after the transition edge. The default value is 0, with a maximum delay of 75 ns.
- Clause Trigger: Please reference Clause Trigger chapter. 4.
- 5. State: Displays the detailed trigger conditions within each level of the trigger process.
  - Ι. Data In: Triggers based only on the Data In channel.
  - Data Out (Ref. Output Delay): Triggers based only on the Data Out II. channel, applying the Data Output Delay parameter.



III. Dual Data: Treats Data In/Out as a 2-bit dual-channel mode. For example, if the Word Size is set to 8, only 4 clock cycles are required for transmission. The 1st bit of the Data Out pin represents the MSB.



IV. Dual Data(Ref. Output Delay): Functions the same as Dual Data, but applies the Data Output Delay parameter.

Data Field Input Rules:

- The Data field allows up to 8 Bytes. Unused fields should be filled with XXh to indicate any value.
- The input field can contain the required trigger Data or 'X' as a wildcard.
  - Hexadecimal values should end with 'h'.
  - Binary values should end with 'b'.
  - Decimal values do not require a suffix.
- III. Data Offset Triggering

Any Offset: Triggers when valid Data that meets the set conditions

appears anywhere in the Data field, regardless of offset.

Fixed Offset: Triggers only when valid Data that meets the set

conditions appears at the specified offset.



## SVI2 Trigger

### SVI2 Trigger Settings

Click SVI2 Trigger in the toolbar and will show the dialog as the following.

M SVI2 Trigger Settings					×
Channel	Clause Trigger				
	Clause Trigger Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 7</li> <li>Counter x 2</li> </ul>	State 1 Event 1 SVD Packet VDD Kh PSI1 L Xh Load Line Slo Xn SVID = SVT Packet SVT Packet	XXh XXh SVT0 Xh Itage	
SVT Packet Error					
<ul> <li>Default</li> </ul>				✔ ОК	× Cancel

- 1. Channel: Select channels.
- 2. Error Trigger: Trigger specific error of SVI2.
- 3. Clause Trigger: Please reference Clause Trigger chapter.
- 4. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SVD and SVT packet, default value is XX means "don't care".

When check the AUX, the trigger function will refer to the state of AUX (High/Low).



## UART Trigger

### **UART Trigger Settings**

Click UART Trigger in the toolbar and will show the dialog as the following.  $$\mathbbmath{\mathbb{M}}$$  UART Trigger Settings  $$\times$$ 

Channel	Clause Trigger		
Idle High   Tx   A0   Tx   A0   Rx   A1   Baud Rate   9600   9000   9000   9000   9000  <	Run State 1	True False Trigger Trigger * State x 3 Counter x 2	Tx ASCII C Data(s) after Break XXh XXh XXh XXh XXh XXh
End of frame Break/Idle frame		Timer 1	Advanced Setting >>
Parity Error Stop bit Error		Timer 2	Auvanced Setting >>

#### Travel Bus series

UART Trigger Settings				X
Channel	Clause Trigger			
● UART Port         ● LA Port         Idle High         Tx       0         Rx       1         Baud Rate         9600       • bps         Option         Data Bits       8 bits         Stop Bits       1         Parity       None         Simple Trigger         End of frame	Run State 1	<ul> <li>True</li> <li>False</li> <li>Trigger</li> <li>Trigger</li> <li>State x 3</li> <li>Counter x 2</li> </ul>	Hex Value     Bypass     Data (Hex)	
Break/Idle frame		Timer 1		Advanced Setting >>
Parity Error Stop bit Error		Timer 2		

#### Since TravelBus has specially designed channels for UART, the UART



settings in the TravelBus software will include additional channel source options.

- 1. Channel: Configure the UART interface.
- 2. Baud Rate: Set the UART Baud Rate.
- 3. Simple Trigger: Configure UART-specific frame trigger.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Displays the detailed trigger conditions within each level of the trigger process. Users can enter specific trigger values in the Data field or use 'X' as a wildcard for any value. The Data trigger field supports up to 16 Bytes; to specify a trigger data position, Bypass must be selected, and an offset value must be entered.



## USB 1.1 Trigger

### USB 1.1 Trigger Settings

Click USB 1.1 Trigger in the toolbar and will show the dialog as the following.

🕕 USB 1.1 Trigger S	ettings				×
Channel	Clause Trigger				
Dp 0 Dn 1 USB Speed Full Speed Simple Trigger Start of frame End of frame SE0 Bus Idle	Clause Trigger Run State 1	→ True → False → Trigger → Trigger * State x 7 • Counter x 2	State 1 Event 1 PID Any Frame Number XXXh Address (A) = XXh Data XXh XXh XXh XXh XXh XXh XXh XX		XXh XXh
<ul> <li>Idle State</li> <li>Error Trigger</li> <li>PID Error</li> <li>CRC5 Error</li> <li>CRC16 Error</li> <li>EOP Error</li> <li>Bit Stuff Error</li> </ul>			Offset	0 C Byte	e(s)
Default				✓ OK	× Cancel

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of USB 1.1.
- 3. Error Trigger: Trigger specific error of USB 1.1.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the PID, Frame Number, Address and Data Field, default value is XX means "don't care".

Data field provided 4 bytes data to trigger, checking the Fixed Offset and selecting the offset value when want to trigger at the specific position.



## **USB PD Trigger**

### **USB PD 3.0 Trigger Settings**

Click USB PD 3.0 Trigger in the toolbar and will show the dialog as the

#### following.

III USB PD Trigger Settings			×
Channel	Clause Trigger		
CC A0	Run		State 1
Data Rate 300 Kbps Simple Trigger Start of frame End of frame	State 1	True False Trigger	Event 1 OR SOP Sequences Any V Message Header
		🖶 State x 7	
		🖶 Counter x 2	Data Obj(s)
Error Trigger SOP Error EOP Error Chunked bit Error CRC32 Error			Offset 0
CR032 Ellor		Timer 1	Advanced Setting >>
		Timer 2	
Default			V OK X Cancel

- 1. Channel: Select channels.
- 2. Simple Trigger: Specific trigger function of USB PD 3.0.
- 3. Error Trigger: Trigger specific error of USB PD 3.0.
- 4. Clause Trigger: Please reference Clause Trigger chapter.
- 5. State: Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SOP Sequences, Message Header and Data Obj(s), default value is XX means "don't care".
  Provide 0 ~ 7 offset value for Data Obj(s) field.