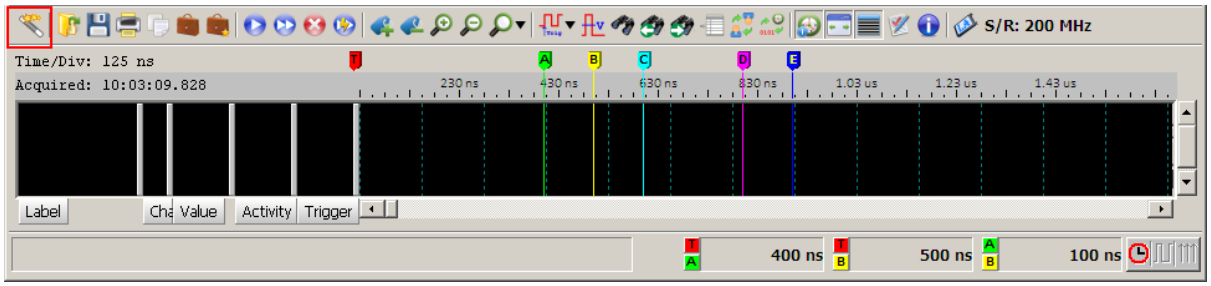
Table of Contents

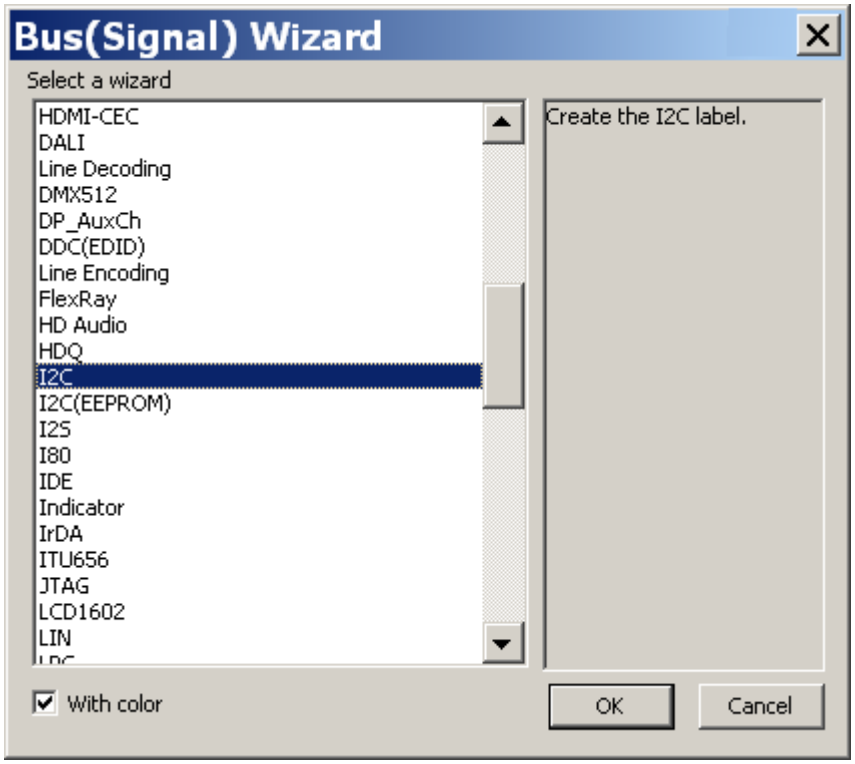
Chapter 1 Bus Decode

Add a Bus Decode:

Method 1:

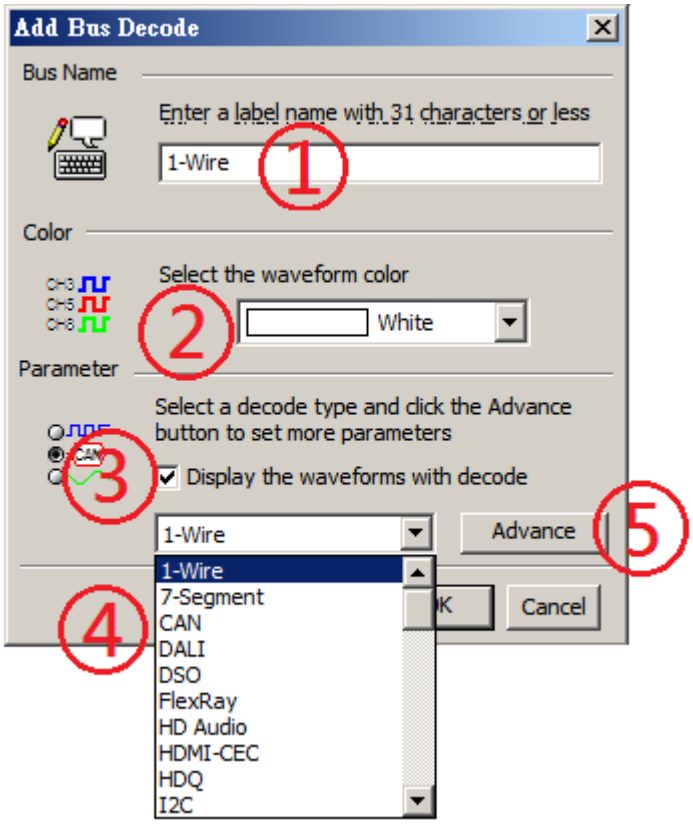
Click the wizard in the menu, and select the bus decode.



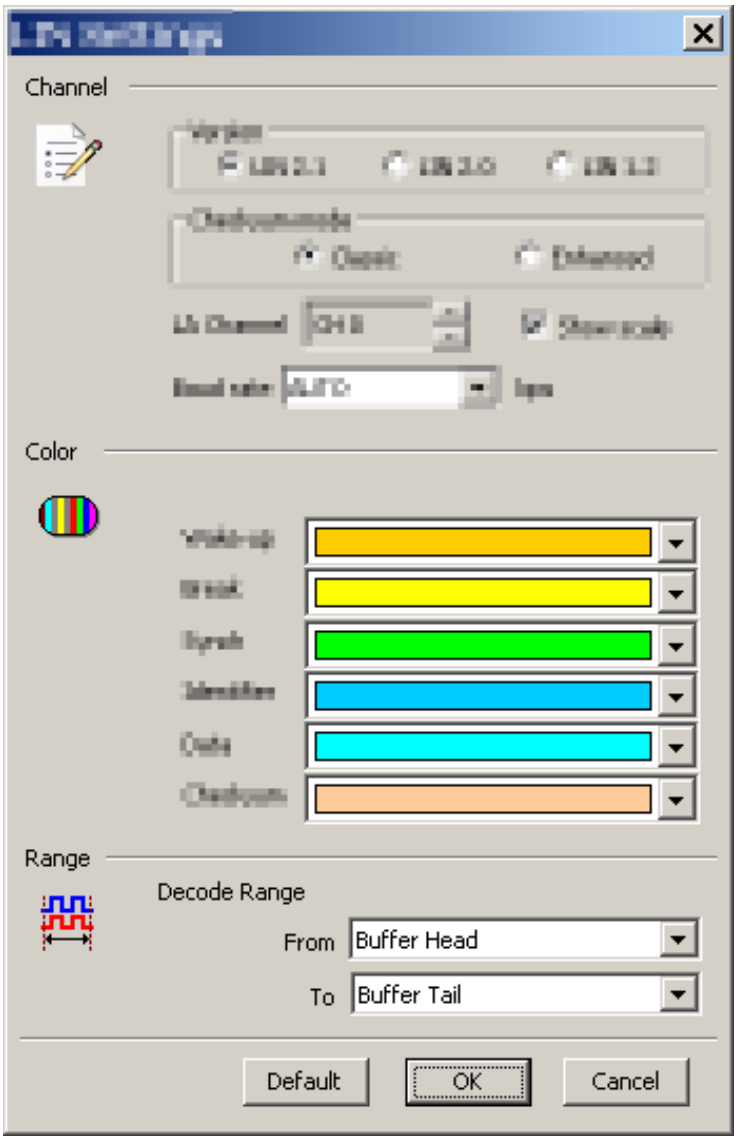


Method 2:

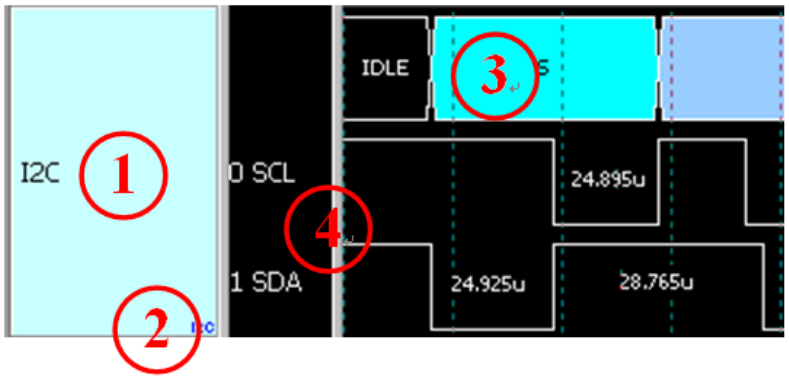
Click Add Bus Decode in the Label menu or right-click the label field to show the dialog box.



1. **Bus Name:** Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
2. **Color:** Set the waveform color.
3. **Display the waveforms with decode**
4. Display the waveforms with its decode together.
5. **Advance:**



Set the decode parameters or press **OK** to use default settings. There are "Channel", "Color", "Range" settings



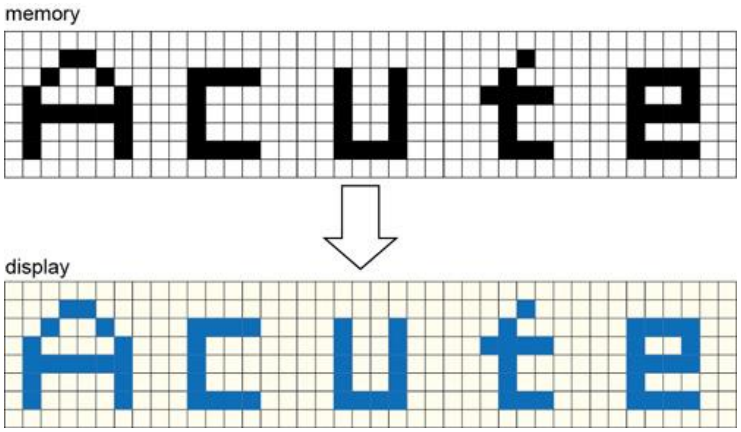
1. **Bus name**
2. **Decode type**
3. **Result**
4. **Channel name & signal**

Specially Bus Decode:

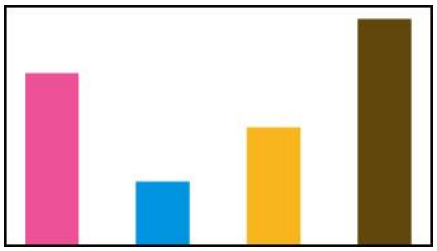
The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode…), image, analog waveform (ADC decode) etc.

In the future, we will extend the original form display to more applications like:

LCD/CMOS image sensor bus decodes:



Statistic or Bar chart:

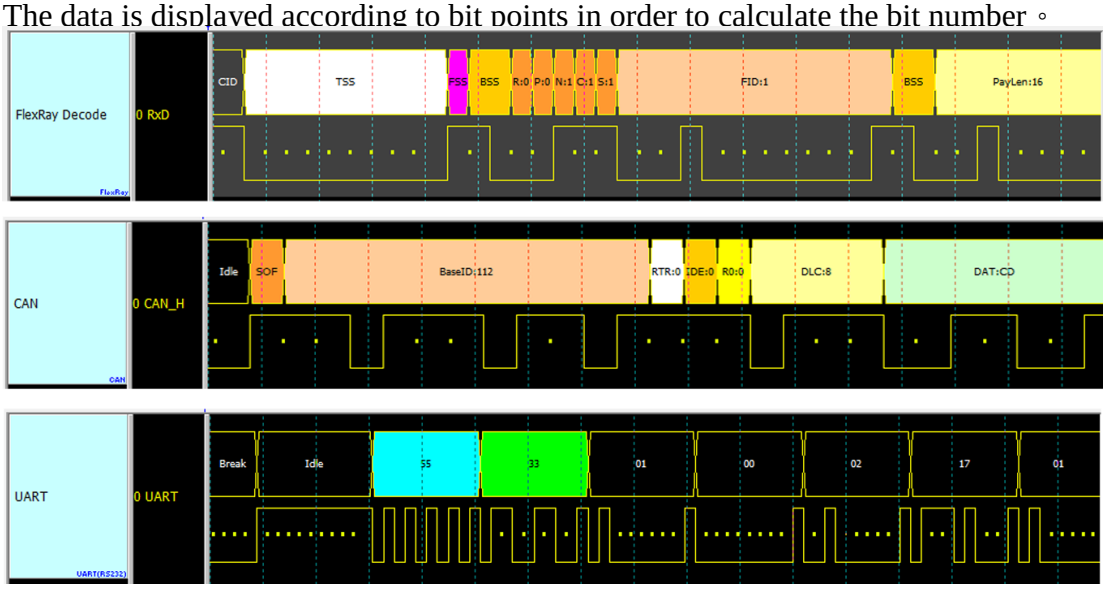


RPM:

The following original data form display for bus decodes are already available in the past.

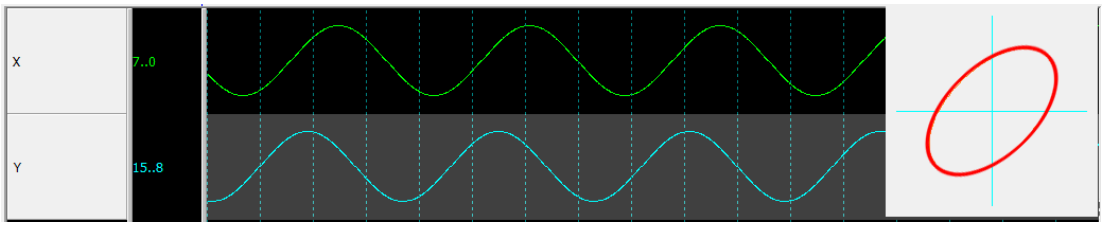
UART/CAN/FlexRay..bus decodes (released in 2009/9, LA Viewer Ver. 2.0):

The data is displayed according to bit points in order to calculate the bit number。



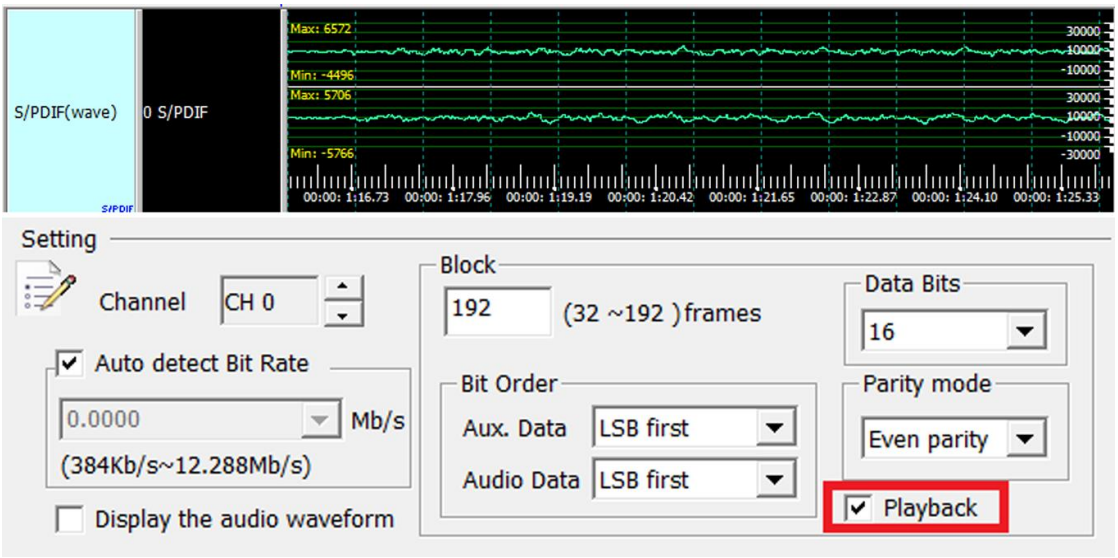
Lissajous analysis (released in 2009/09, LA Viewer Ver.2.0):

Display the signal in graph by X-Y or I-Q data.。



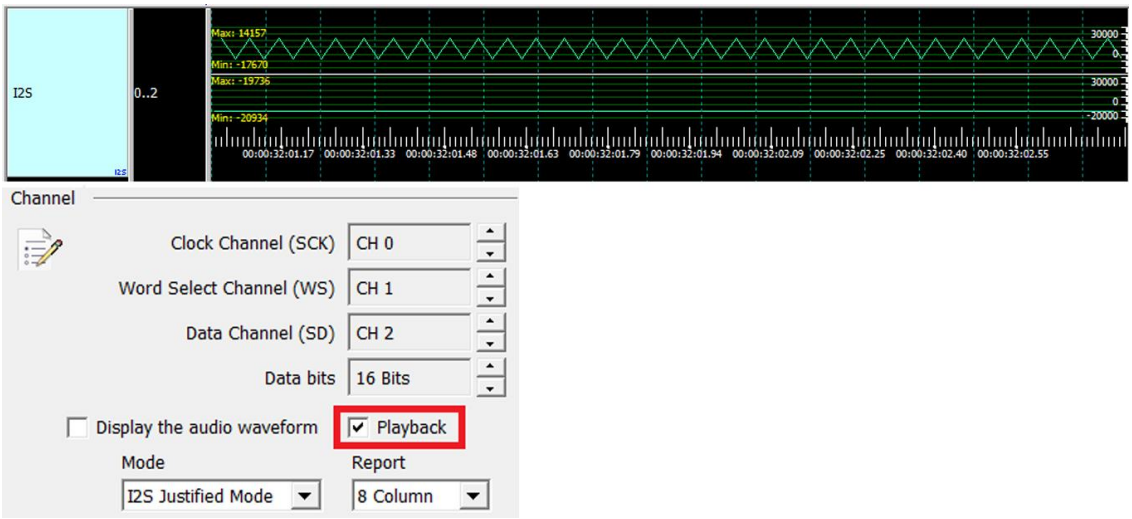
S/PDIF analysis (2010/11, LA Viewer Ver. 2.5):

Display the data in sound waveform。



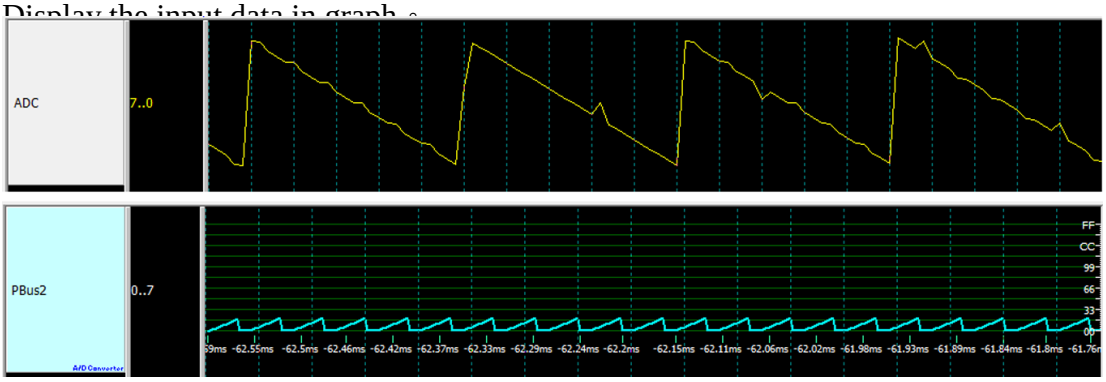
I2S analysis (2011/09, Ver. 2.6.3): 分析 (2011/09, LA Viewer Ver 2.6.3)

Display the data in sound waveform。



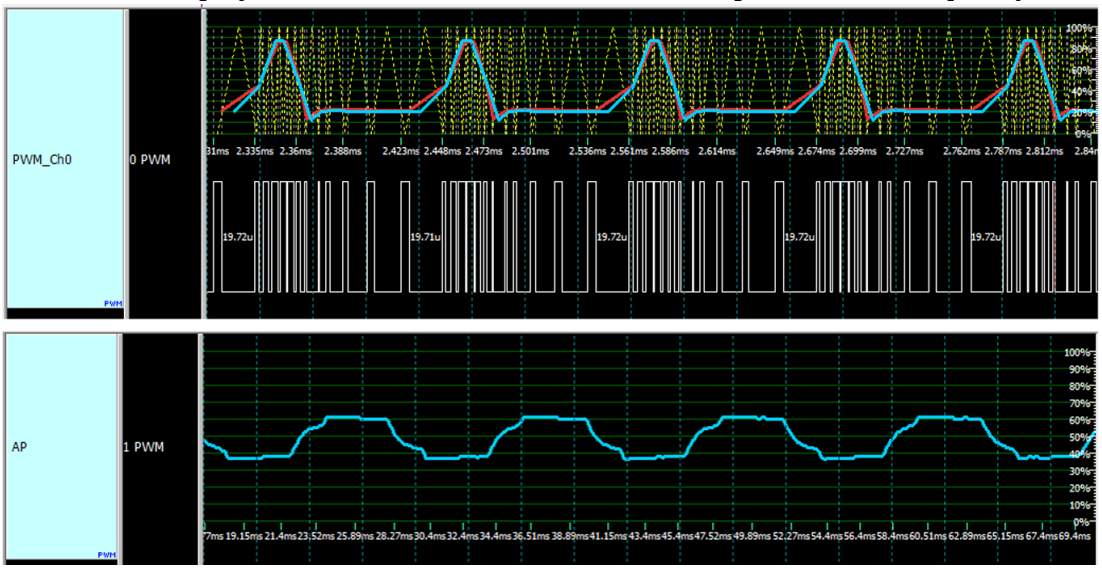
ADC bus decode (2012/08, LA Viewer Ver. 2.7.3):

Display the input data in graph。



PWM analysis (2012/08, LA Viewer Ver. 2.7.3):

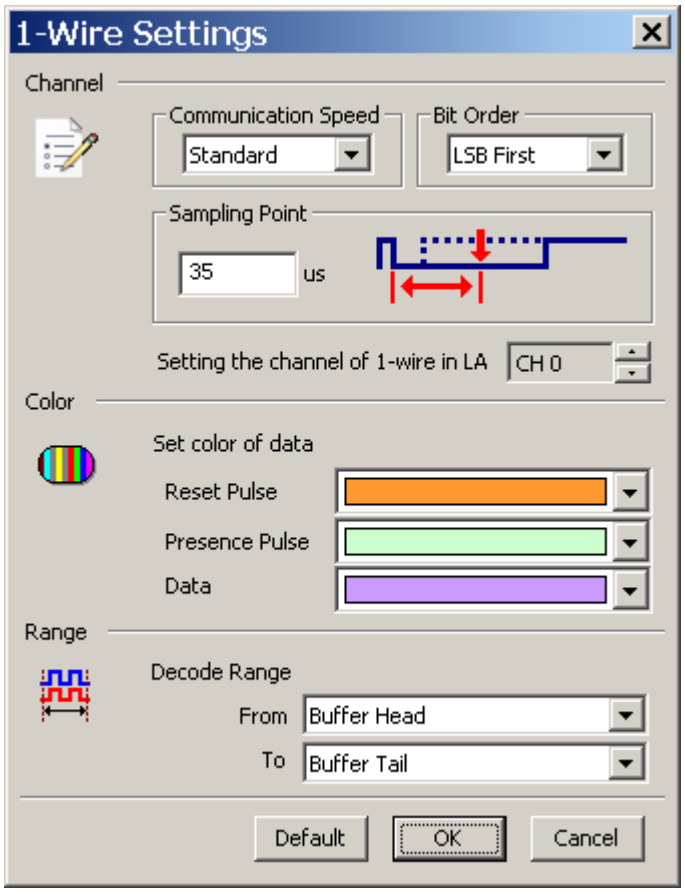
Restore and display the data in the waveform window as percentile or frequency。



1-Wire

The 1-Wire bus has data bits (Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, Read 0) in standard or overdrive speed as the diagram below.

Settings



Communication Speed: Standard or overdrive.

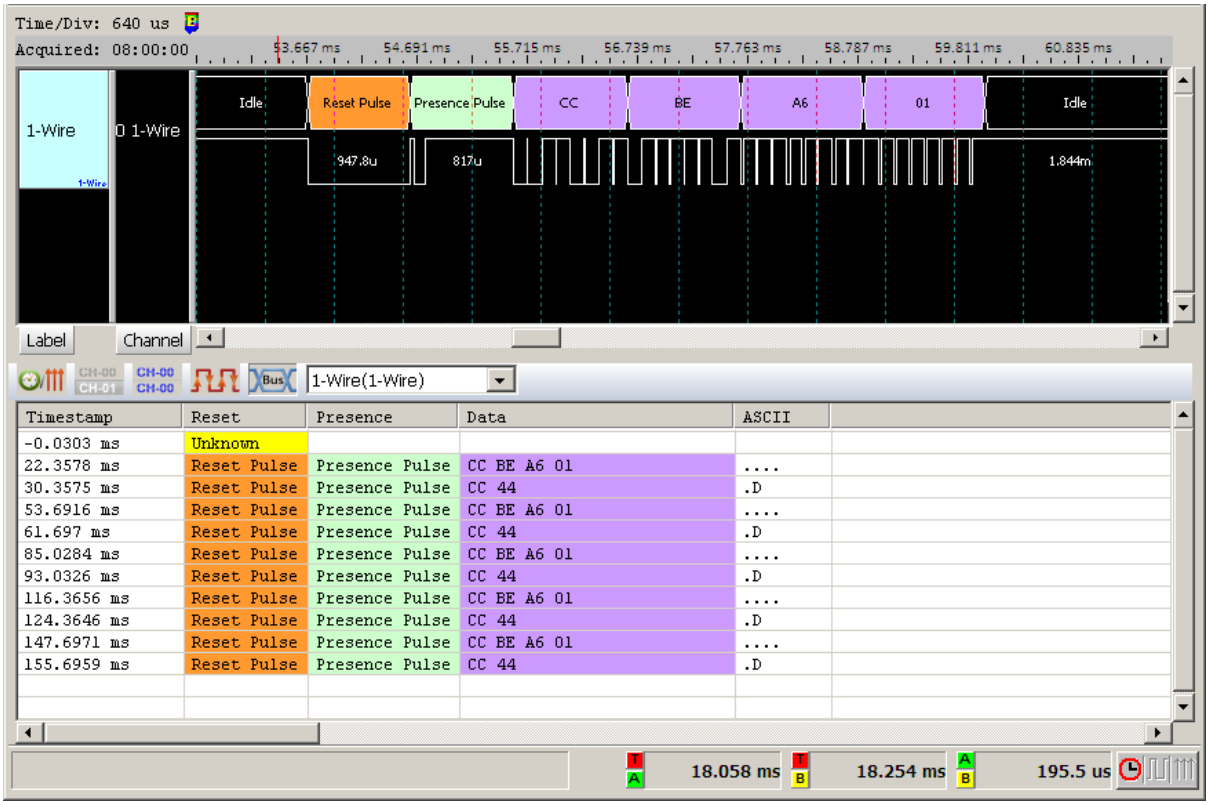
Bit Order: LSB first or MSB first.

Sampling point: Set the sampling point N microseconds (us) after the beginning of each data bit.

Result

Click OK to run the 1-Wire decode and see the result on the Waveform Window

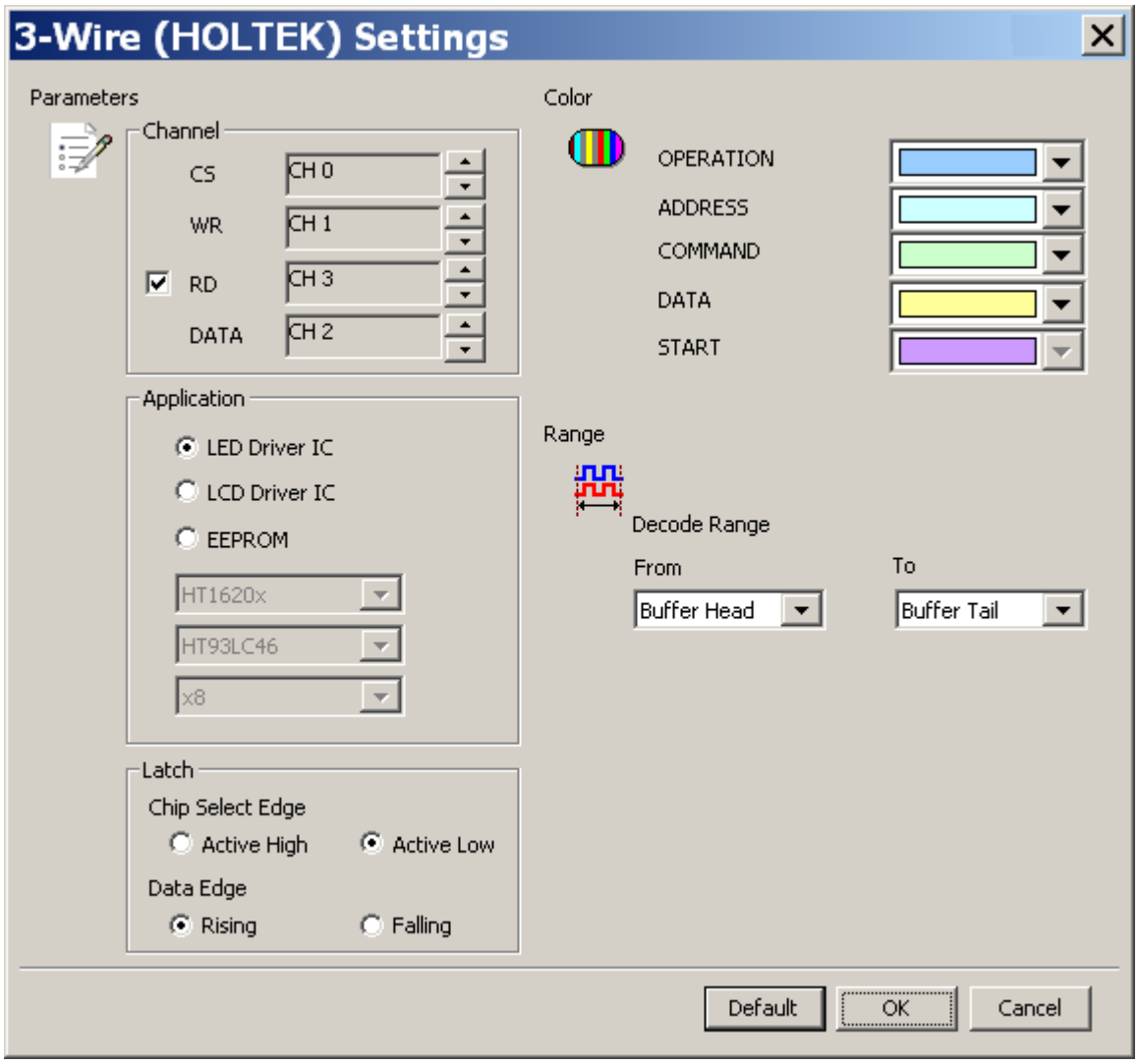
below.



3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

Settings



Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

EEPROM: Select EEPROM application.

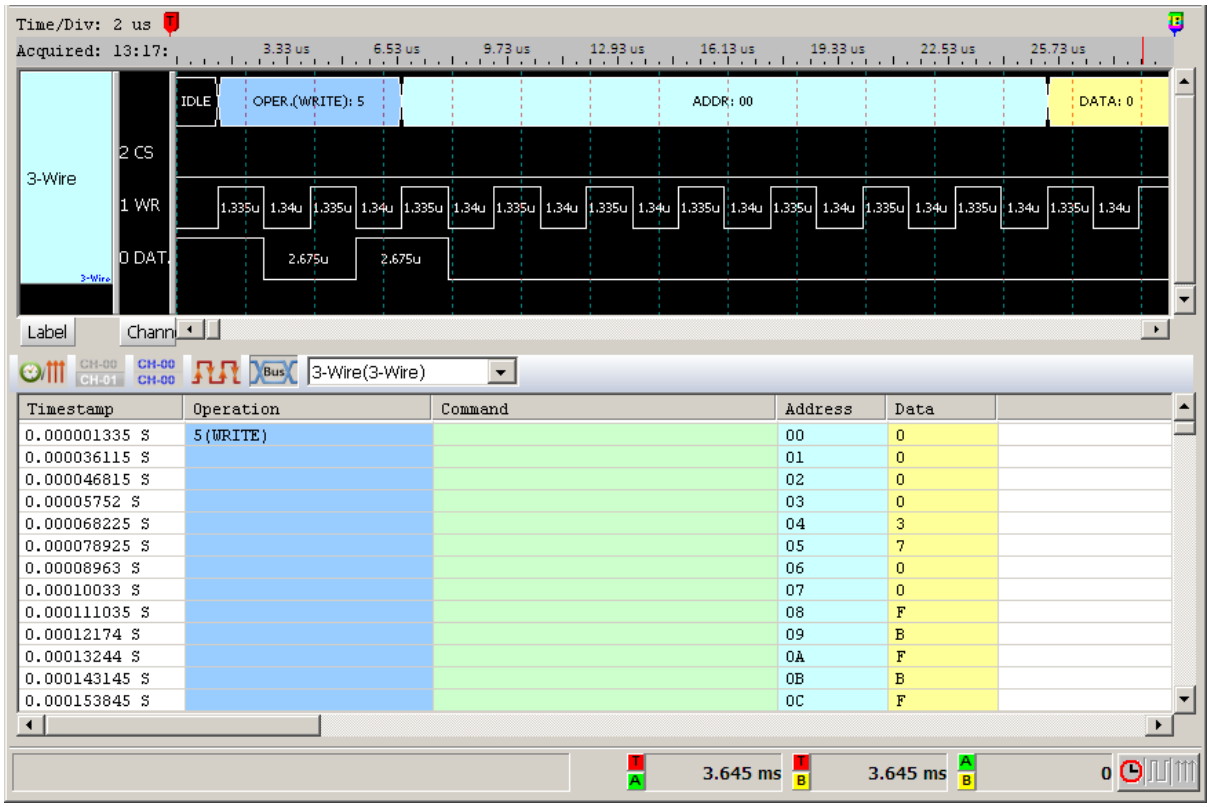
Active High: Select Active High.

Active Low: Select low chip select (CS).

Rising: Select Rising Data Edge.

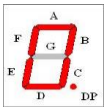
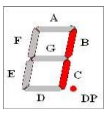
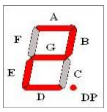
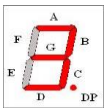
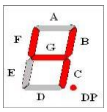
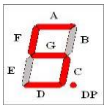
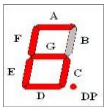
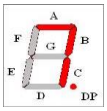
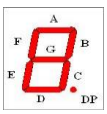
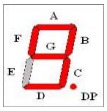
Falling: Select Falling Data Edge.

Result

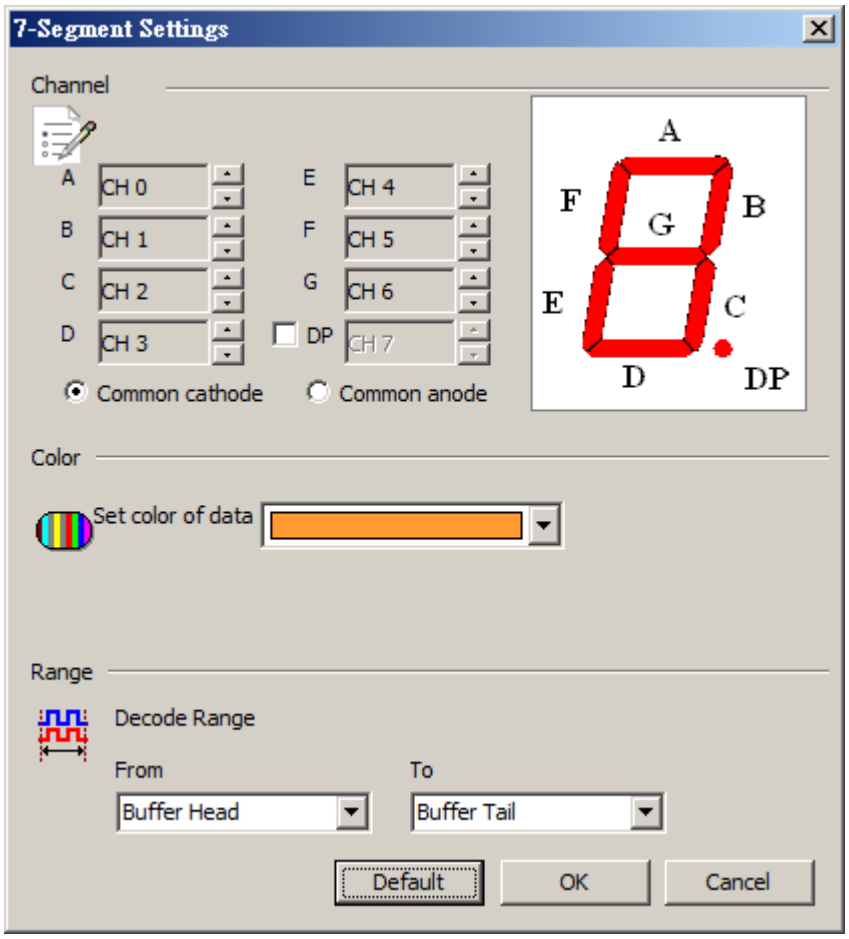


7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit	LED	A	B	C	D	E	F	G
0		**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	OFF
1		OFF	**ON**	**ON**	OFF	OFF	OFF	OFF
2		**ON**	**ON**	OFF	**ON**	**ON**	OFF	**ON**
3		**ON**	**ON**	**ON**	**ON**	OFF	OFF	**ON**
4		OFF	**ON**	**ON**	OFF	OFF	**ON**	**ON**
5		**ON**	OFF	**ON**	**ON**	OFF	**ON**	**ON**
6		**ON**	OFF	**ON**	**ON**	**ON**	**ON**	**ON**
7		**ON**	**ON**	**ON**	OFF	OFF	OFF	OFF
8		**ON**	**ON**	**ON**	**ON**	**ON**	**ON**	**ON**
9		**ON**	**ON**	**ON**	**ON**	OFF	**ON**	**ON**

Settings



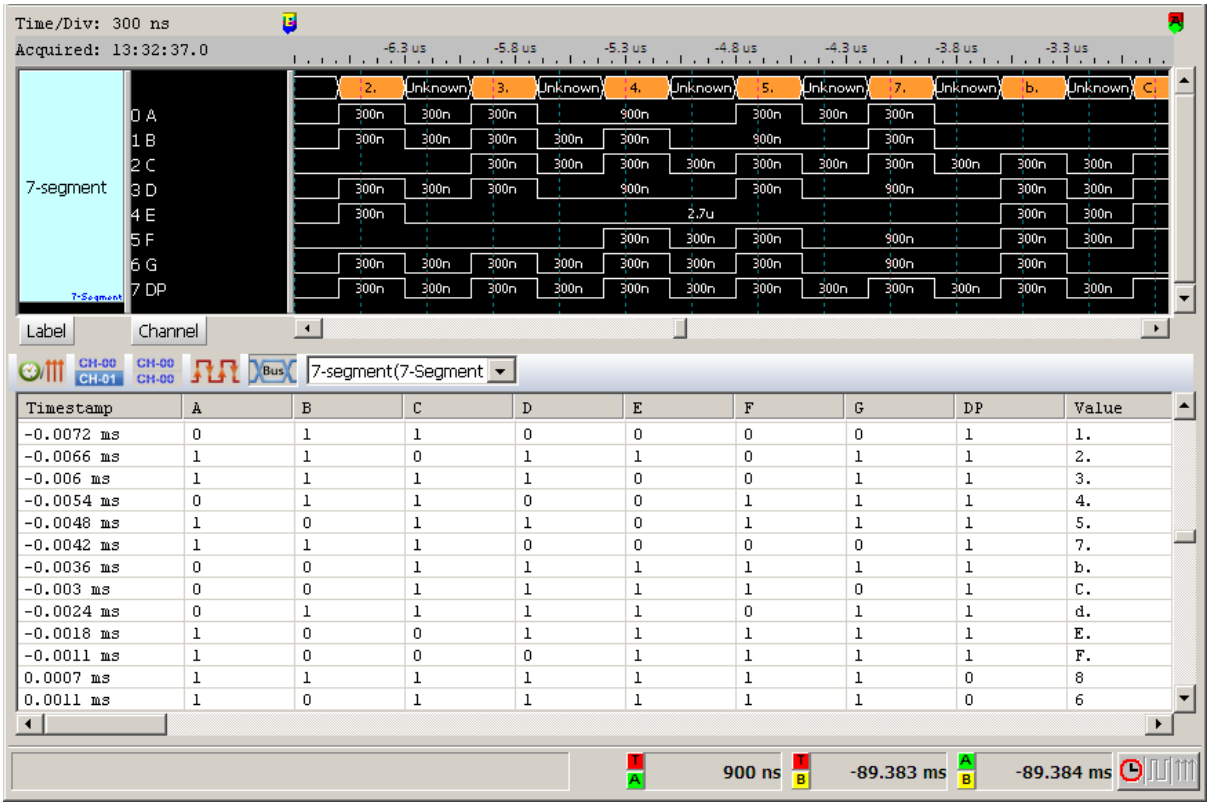
Channel: Show the selected channel (CH 0).

DP: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.

Result

Click **OK** to run the 7 Segment decode and see the result on the Waveform Window below.

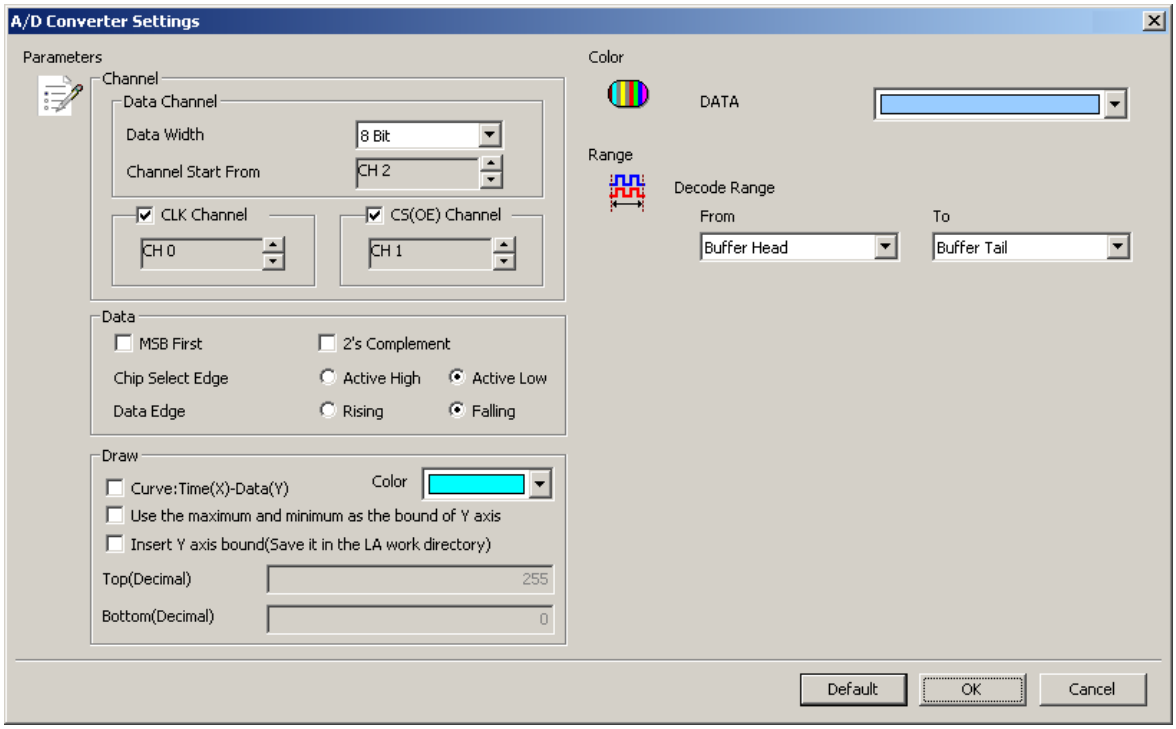


Timestamp	A	B	C	D	E	F	G	DP	Value
-0.0072 ms	0	1	1	0	0	0	0	1	1.
-0.0066 ms	1	1	0	1	1	0	1	1	2.
-0.006 ms	1	1	1	1	0	0	1	1	3.
-0.0054 ms	0	1	1	0	0	1	1	1	4.
-0.0048 ms	1	0	1	1	0	1	1	1	5.
-0.0042 ms	1	1	1	0	0	0	0	1	7.
-0.0036 ms	0	0	1	1	1	1	1	1	b.
-0.003 ms	0	0	1	1	1	1	0	1	C.
-0.0024 ms	0	1	1	1	1	0	1	1	d.
-0.0018 ms	1	0	0	1	1	1	1	1	E.
-0.0011 ms	1	0	0	0	1	1	1	1	F.
0.0007 ms	1	1	1	1	1	1	1	0	8
0.0011 ms	1	0	1	1	1	1	1	0	6

A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

Settings



Data Channel Start From: ADC data channel start from

CLK Channel: ADC clock in channel

CS(OE) Channel: ADC chip select (output enable) channel

Data Width: ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted

2's Complement: Show the 2's complement result.

Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

Curve: Time(X)-Data(Y) Show the diagram in form of time as X axis; data as Y

axis.

Color: Select the curve color

Use the maximum and minimum as the bound of Y axis: Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis.

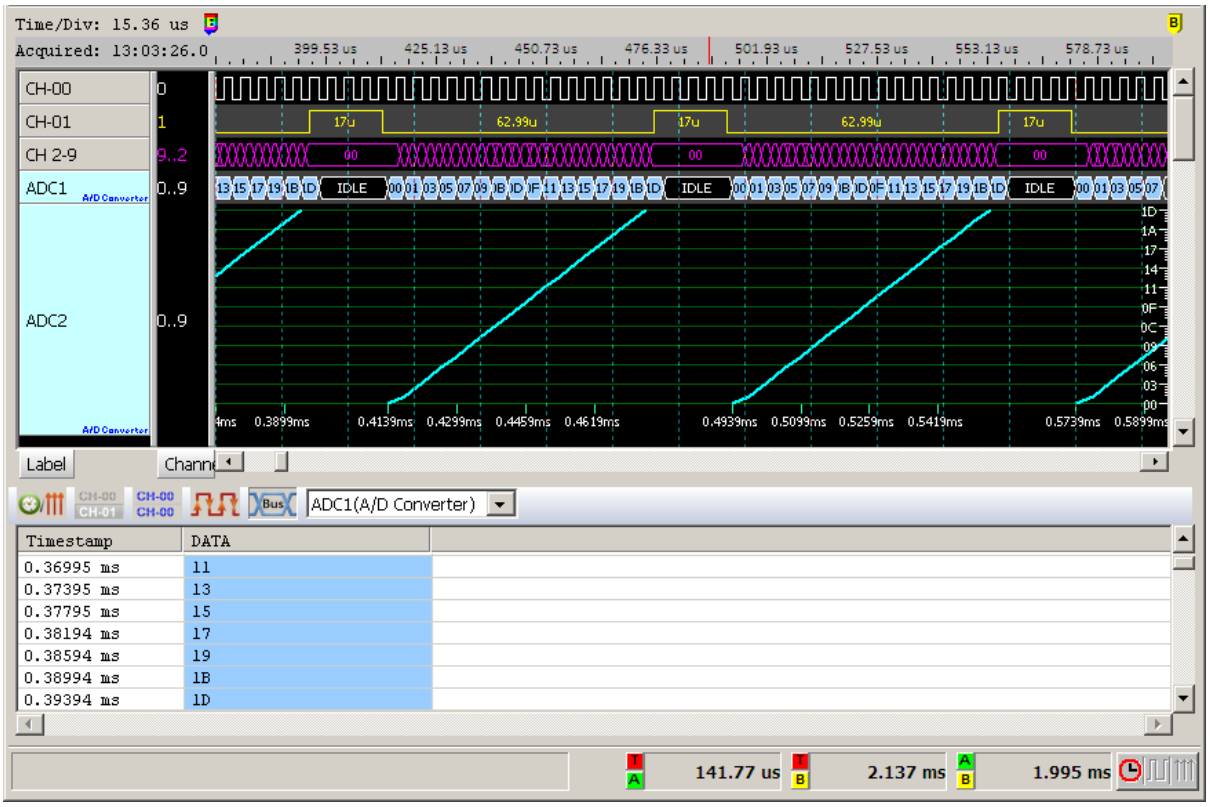
Insert Y axis bound: Set the maximum and minimum bounds of Y axis.

Note: When Insert Y axis boundaries is actived (Save it in the LA file directory), the Top and Bottom values will always be saved as an independent text file named as ADC.txt, different from the waveform file, at file work directory unless a different name is assigned. If you need the specific boundary settings, please save it, so you can reload the settings next time.

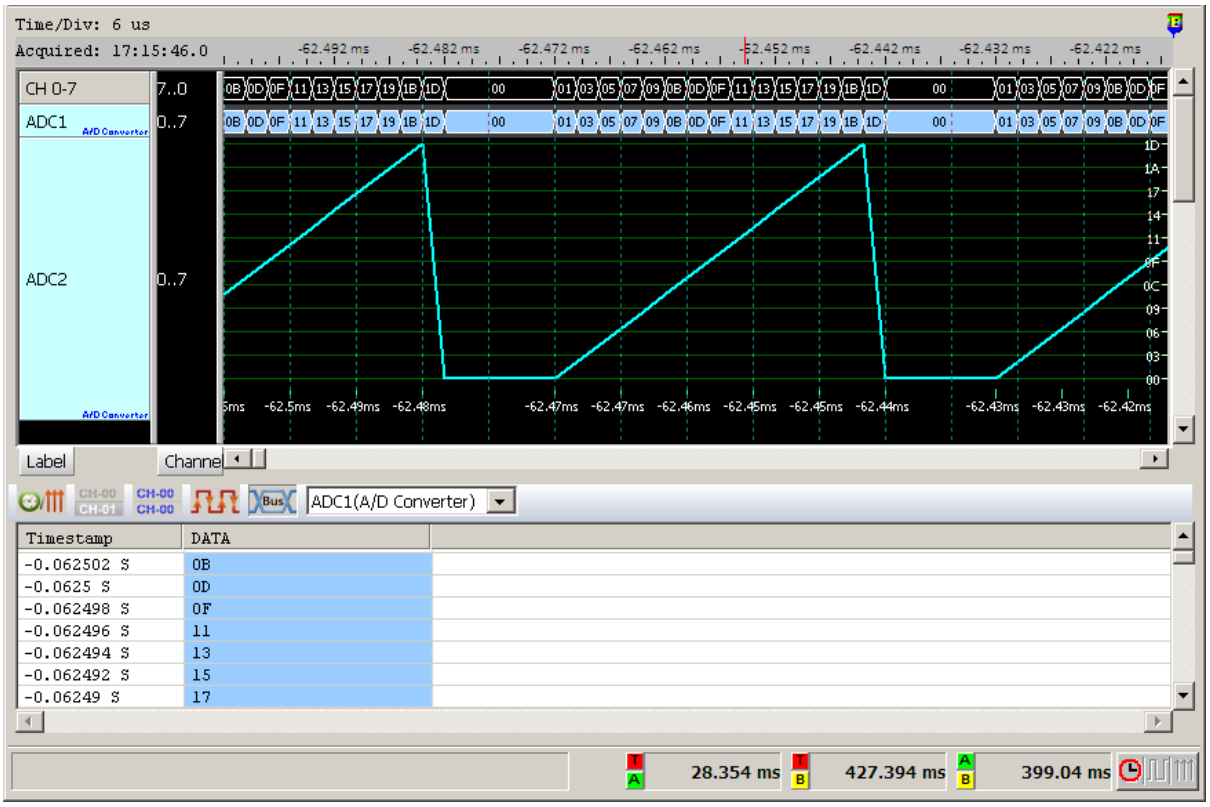
Result

Click **OK** to run the A/D Converter decode and see the result on the Waveform Window below.

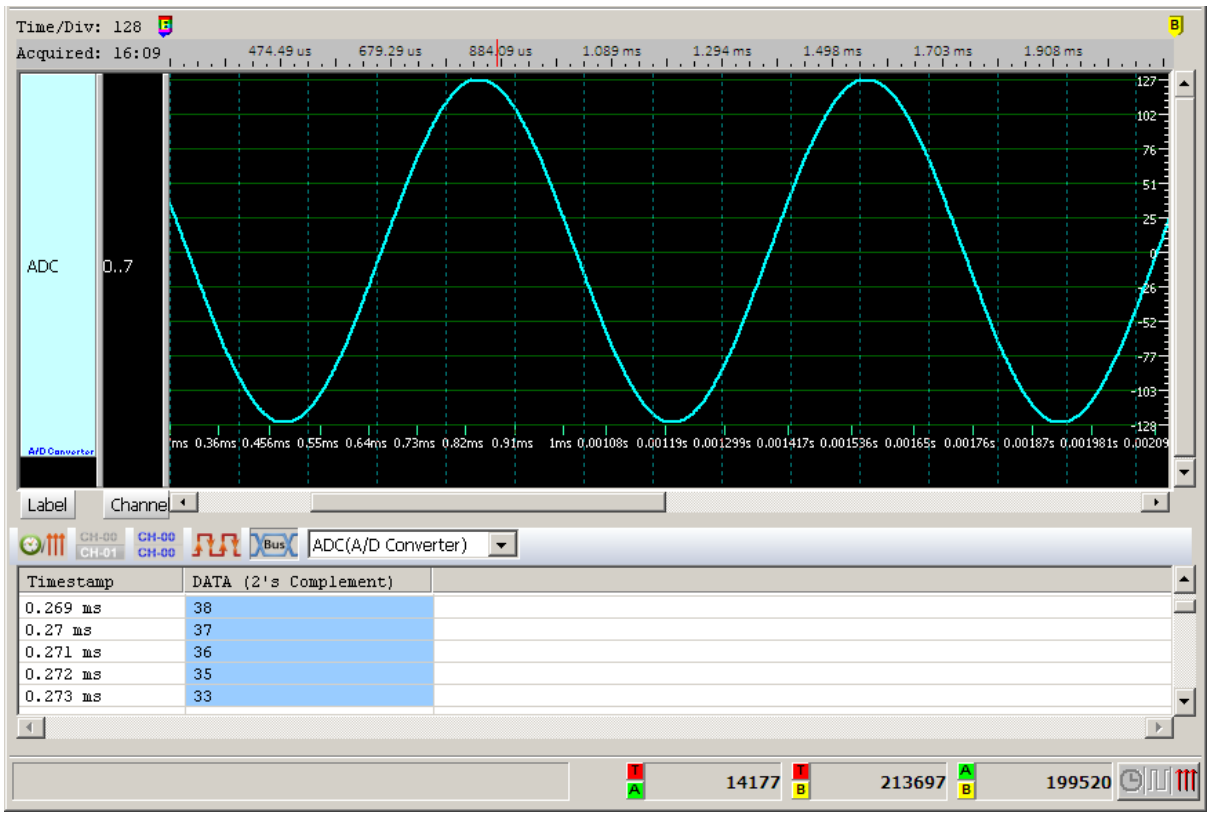
Select 8-bit data, CLK/CS channels:



Select 8-bit data:



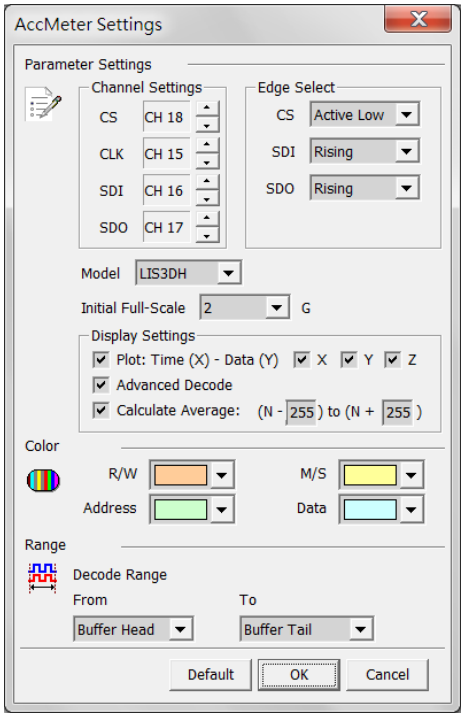
Select 8-bit data, 2’s complement



AcceleroMeter

AcceleroMeter (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

Settings



CS: Chip Select, must specified the active state of the CS pin.

CLK: Clock

SDI: Data Input Pin, must specified the data sampling edge.

SDO: Data Output Pin, must specified the data sampling edge.

Model: The IC model of the target accelerometer.

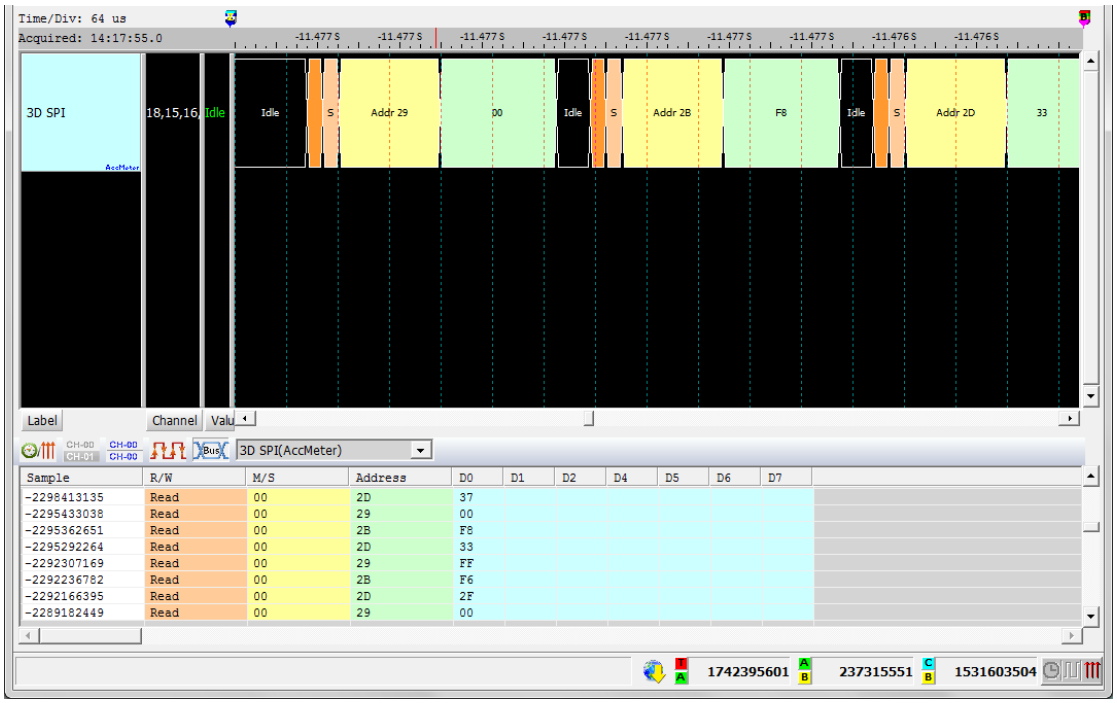
Initial Full-Scale: The default Full-Scale setting.

Plot: Enable/Disable to display the waveform in Time-Value curve.

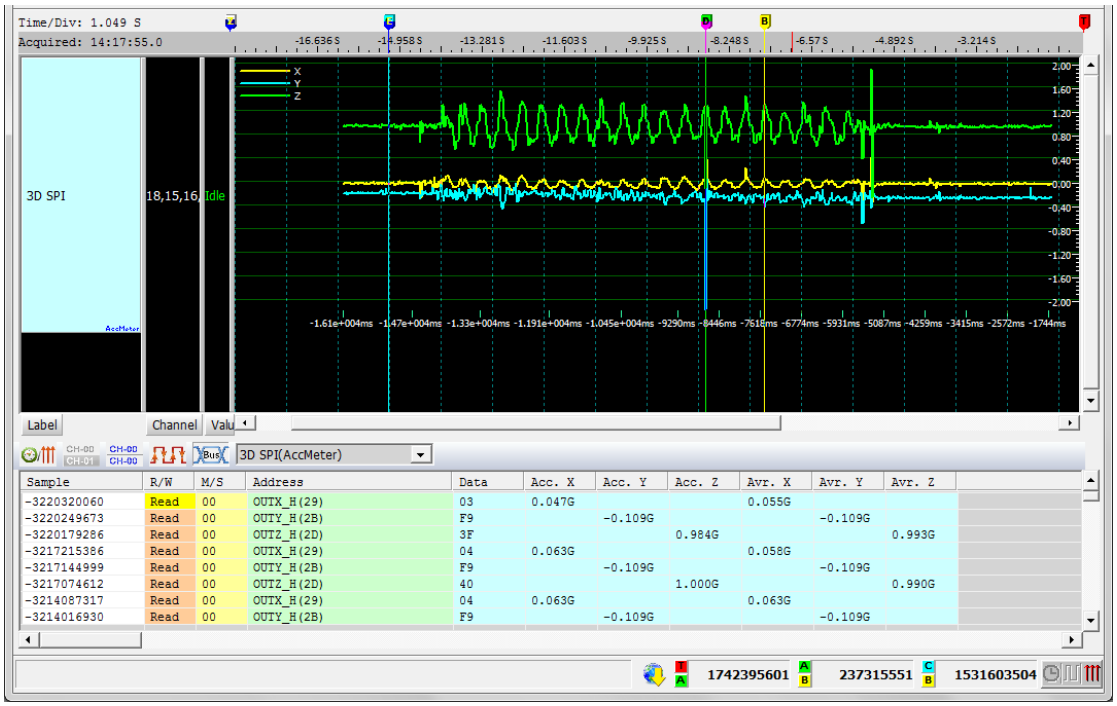
Advanced Decode: Enable/Disable the address, value convert function.

Result

Standard decoder result



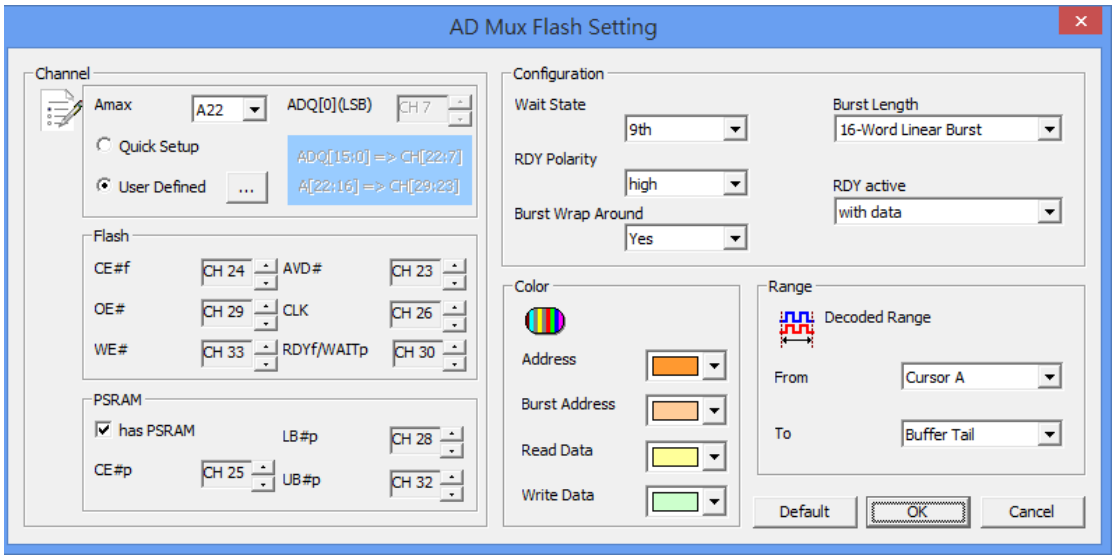
Advanced decode result + Time-Value curve display



AD-Mux Flash

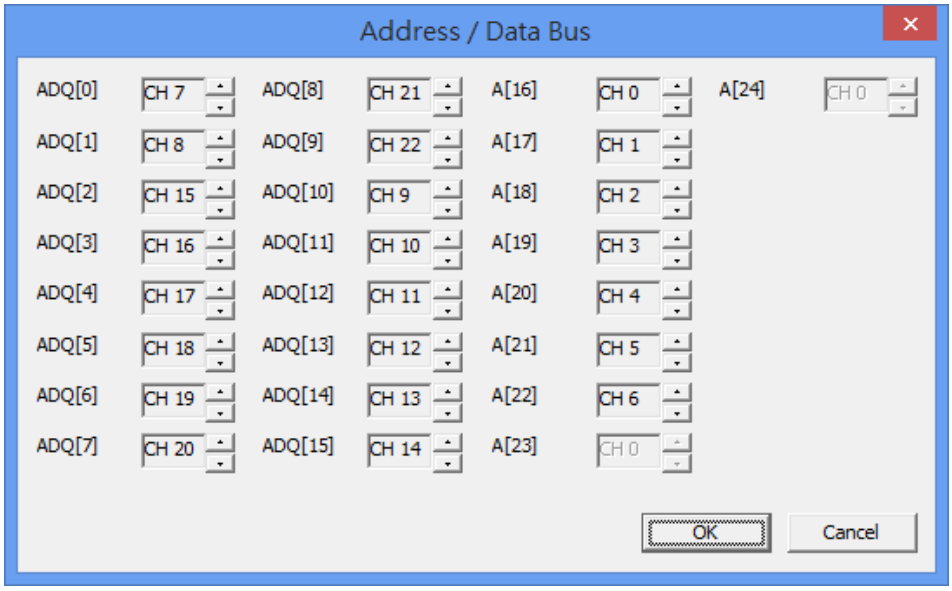
AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

Settings



Amax: Setting the number of address pin.

Quick Setup/User Defined: Only set ADQ[0](LSB) when select the Quick Setup, other channels will be set automatically. When check User Defined and press the button will show the dialog below:



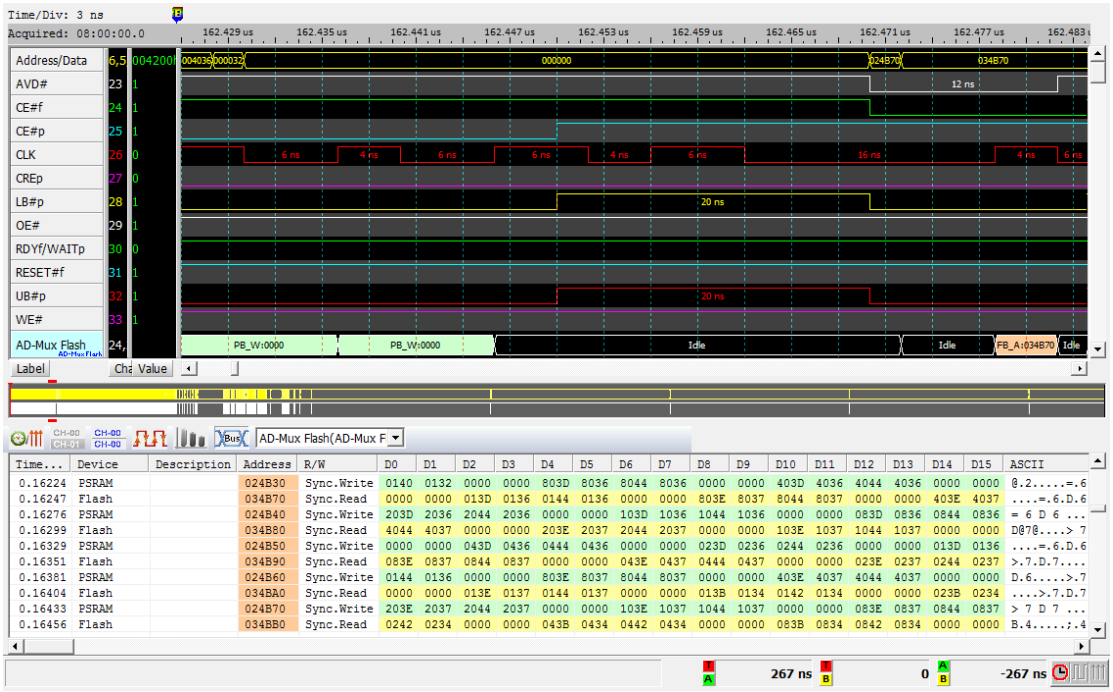
Flash: Control pins of flash.

PSRAM: Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when “has PSRAM” is checked.

Configuration: The default setting of configuration register. User must set here to make a correct analysis.

Result

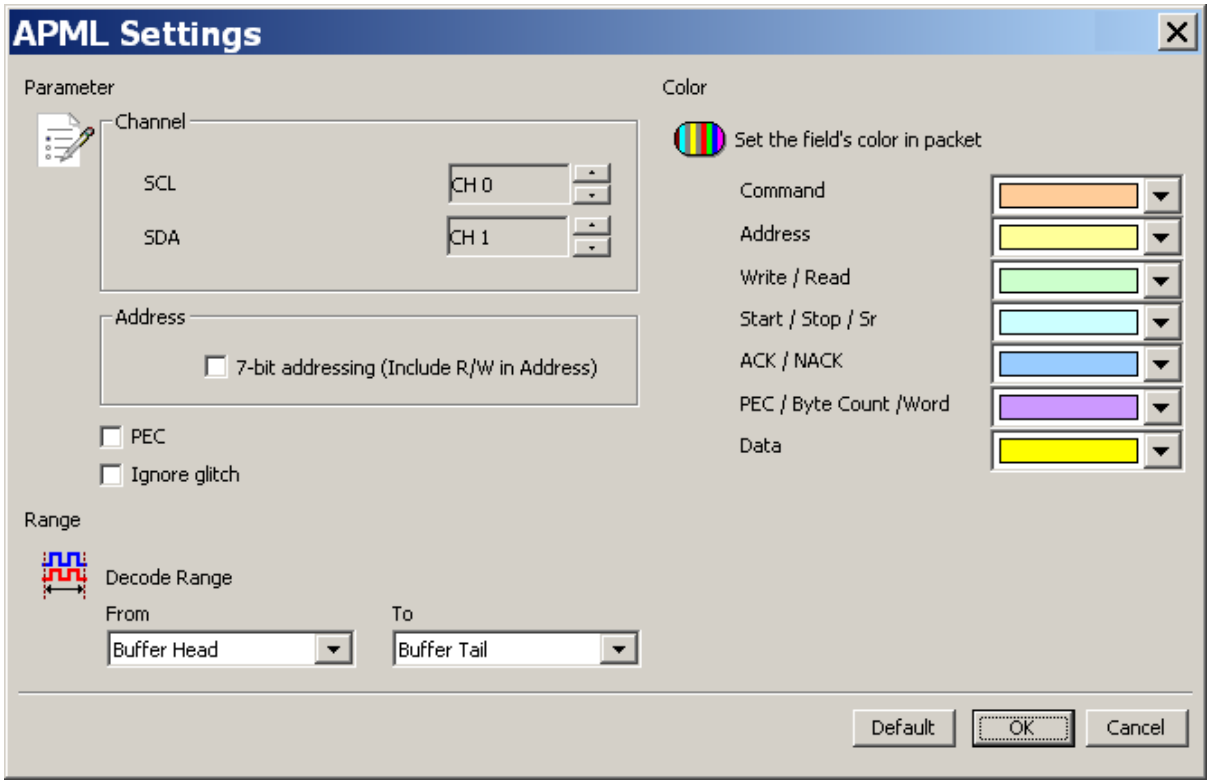
Click OK to run the AD-Mux Flash Decode and see result on the Waveform Windows below.



Advanced Platform Management Link (APML)

APML protocol is established by AMD for it's Opteron CPU platform.

Settings



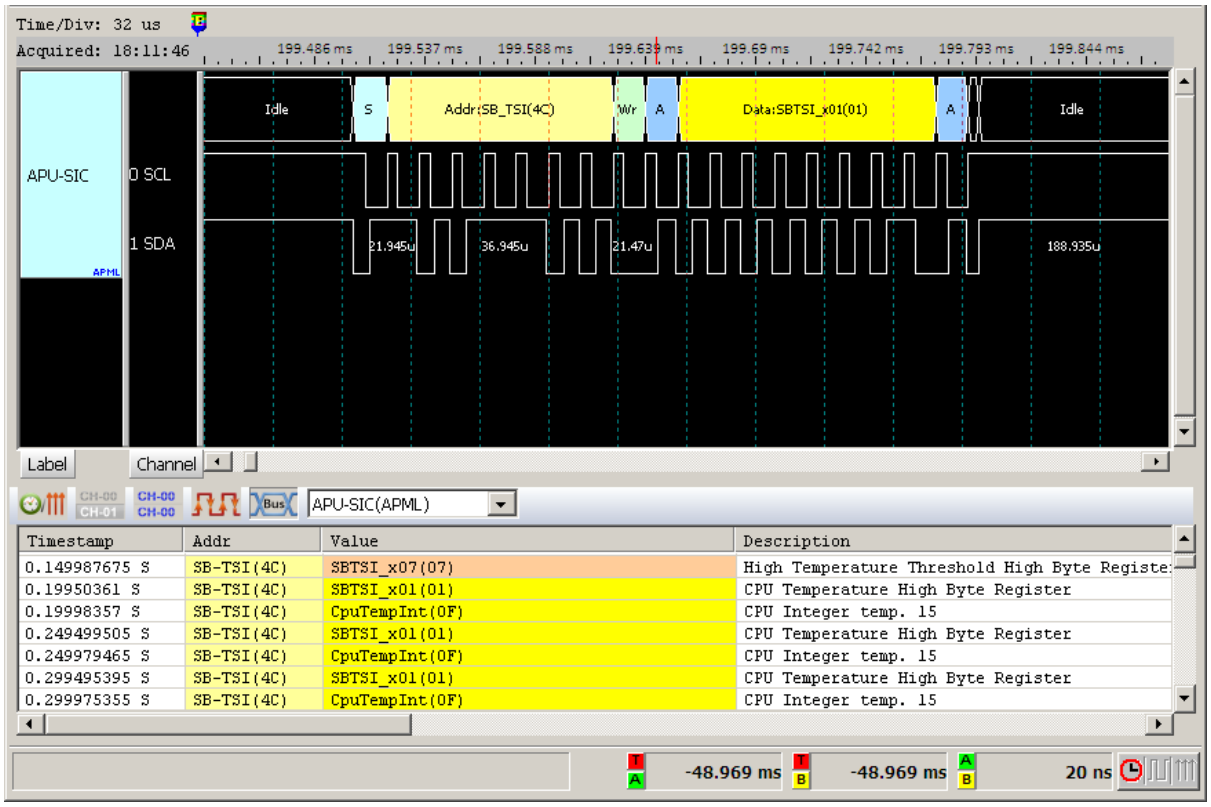
Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

PEC: Packet Error Check.

Ignore glitch: Ignore the glitch when the slow transitions.

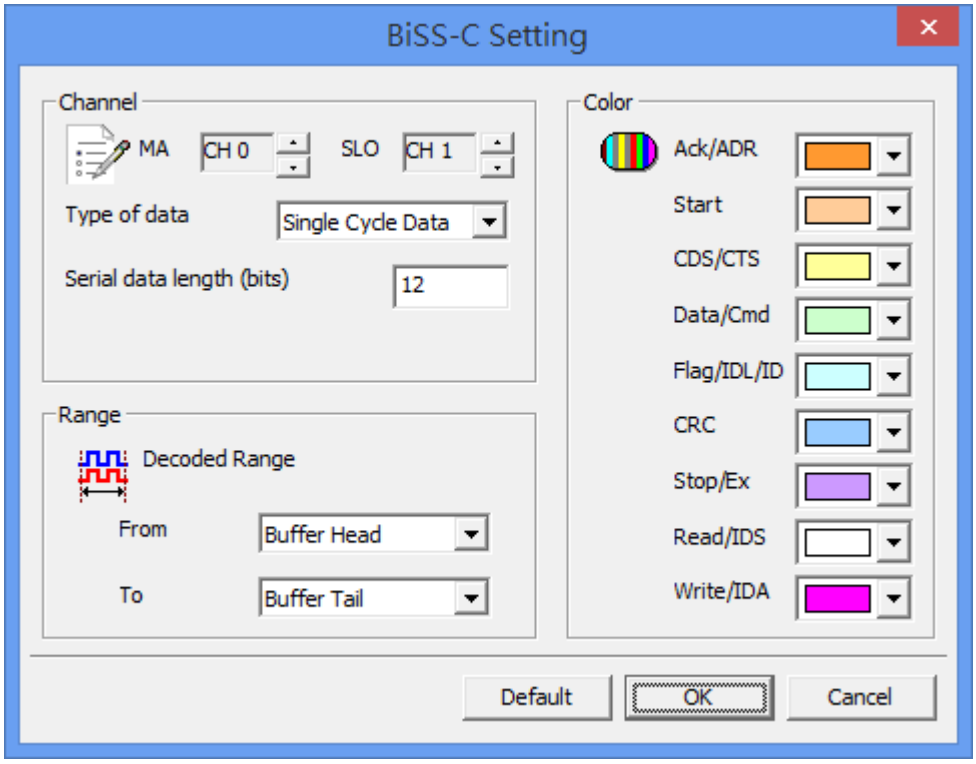
Result



BiSS-C

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings



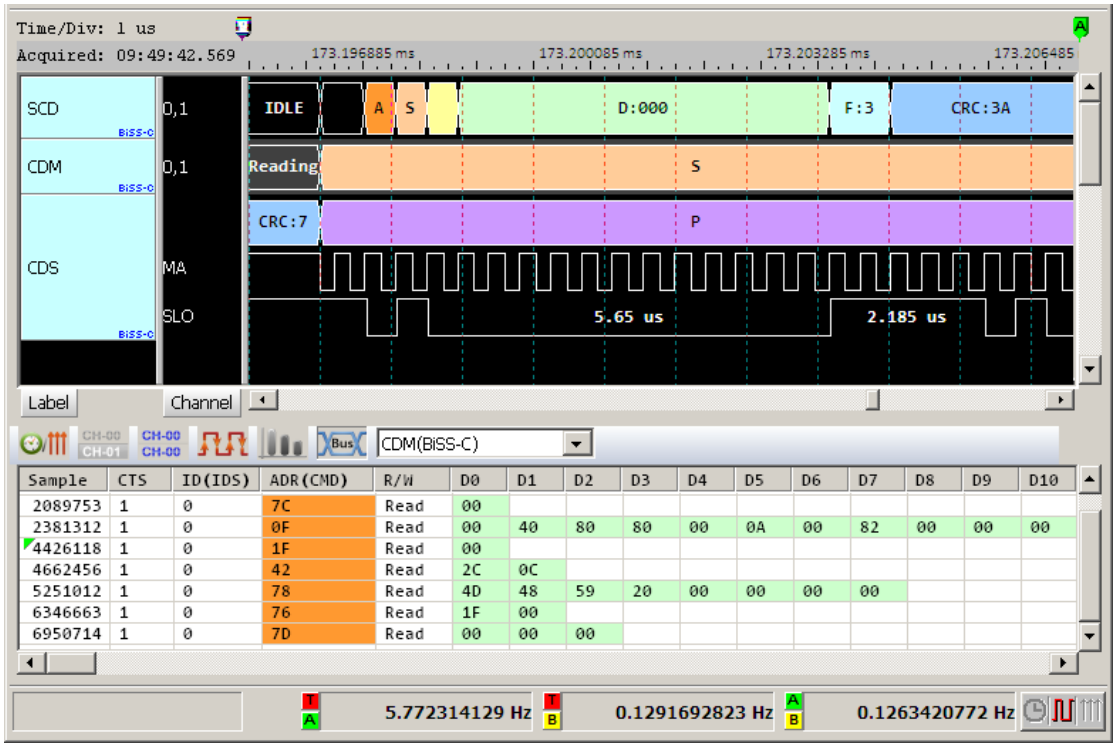
MA/SLO: Setting the channel of MA and SLO.

Type of data: Setting the type you want to decode. It include “Register Data-CDM”, “Register Data-CDS”, “Single Cycle Data”.

Serial data length(bits): Setting the data length when Single Cycle Data mode.

Result

Click OK to run the BiSS-C Decode and see result on the Waveform Windows below.

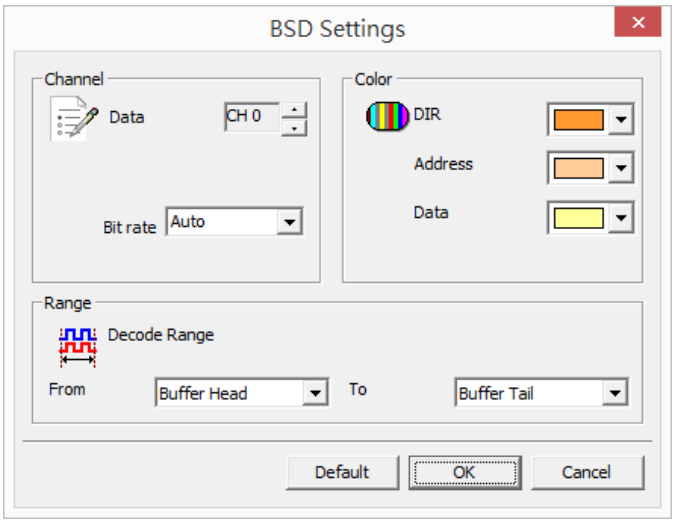


Sample	CTS	ID(IDS)	ADR(CMD)	R/W	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
2089753	1	0	7C	Read	00										
2381312	1	0	0F	Read	00	40	80	80	00	0A	00	82	00	00	00
4426118	1	0	1F	Read	00										
4662456	1	0	42	Read	2C	0C									
5251012	1	0	78	Read	4D	48	59	20	00	00	00	00			
6346663	1	0	76	Read	1F	00									
6950714	1	0	7D	Read	00	00	00								

BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

Settings



Data: The BSD data.

Bit rate: The bit rate of the BSD data

Result

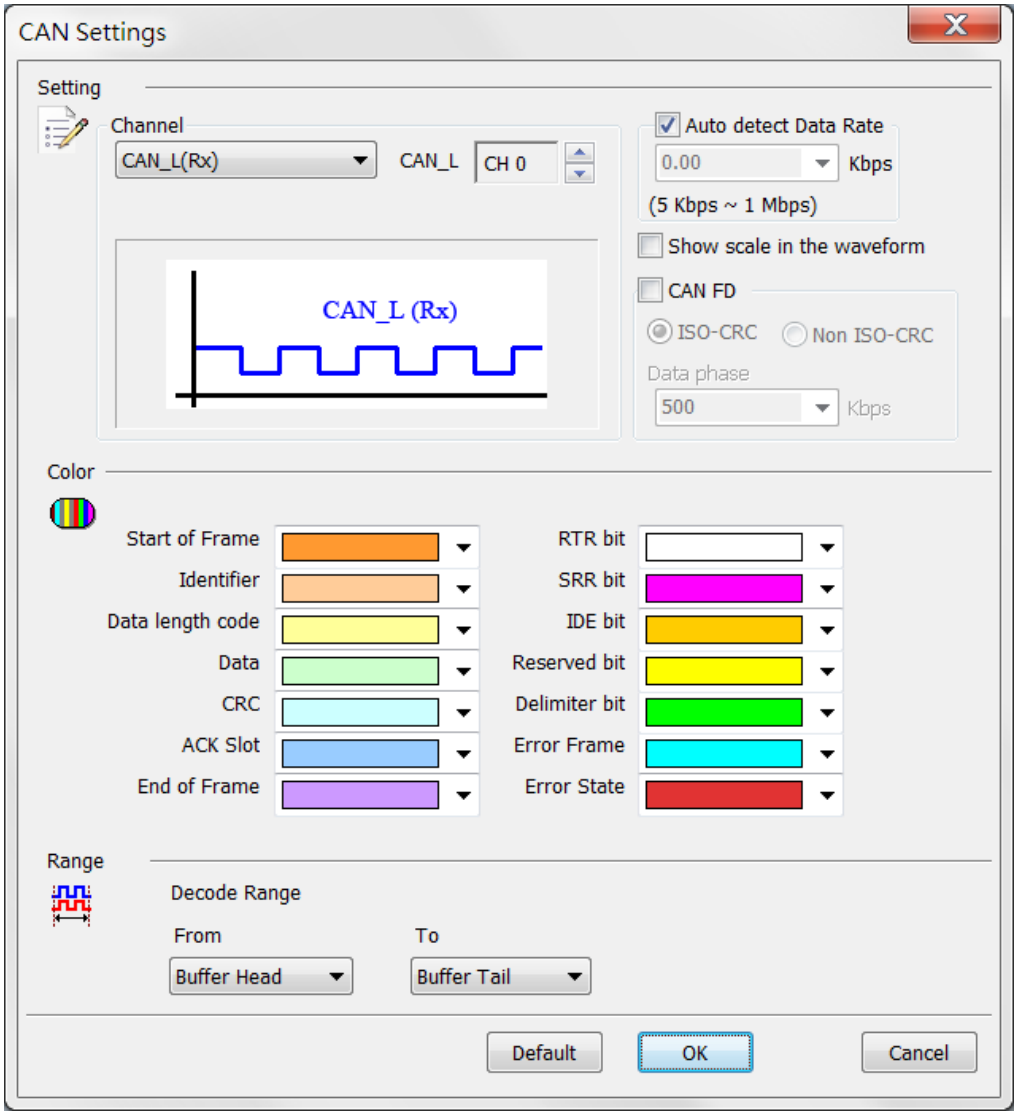
Click OK to run the BSD Decode and see result on the Waveform Windows below.

CAN 2.0B/ CAN FD

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN_H) and CAN Low (CAN_L).

The data rate is flexible in CAN FD (CAN with Flexible Data-Rate). When CAN FD is transferring, it is 64 (bytes/per data) and including CRC17/CRC21.

Settings



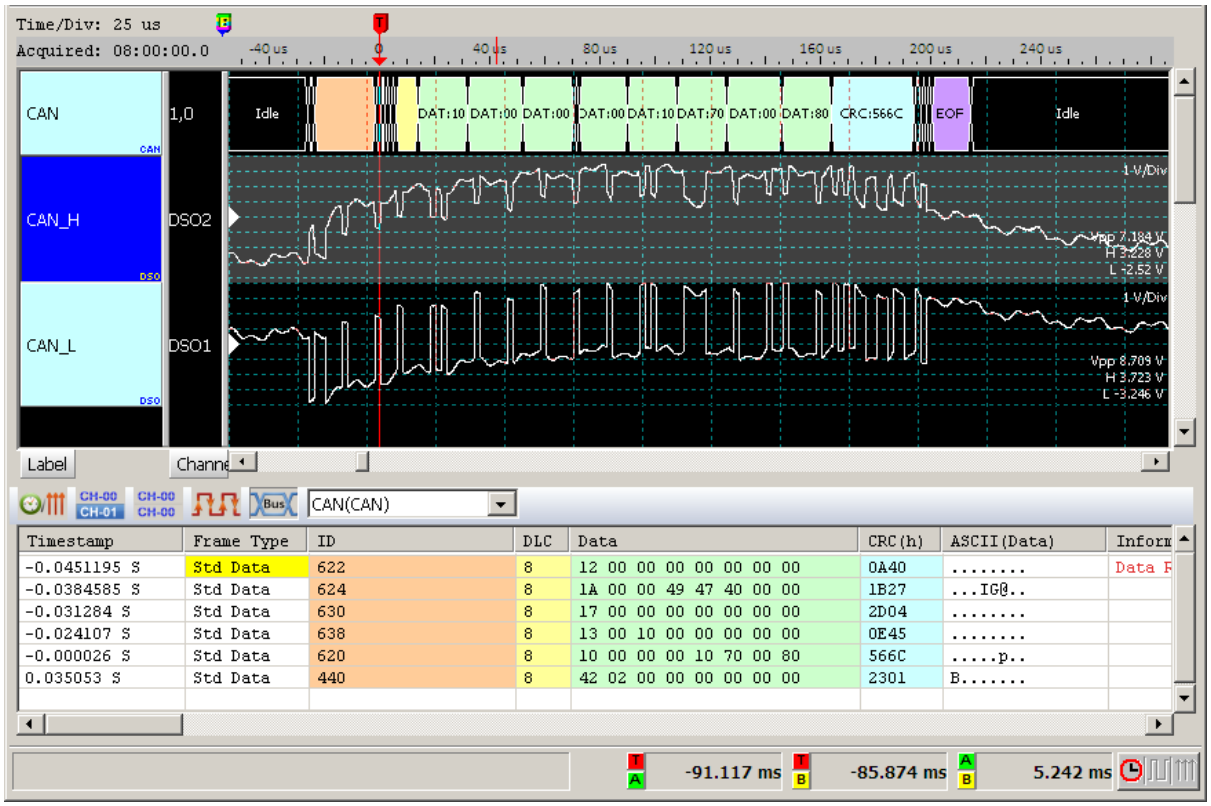
Channel: The differential data from the DSO channel (CAN_H or CAN_L) is shown by default.

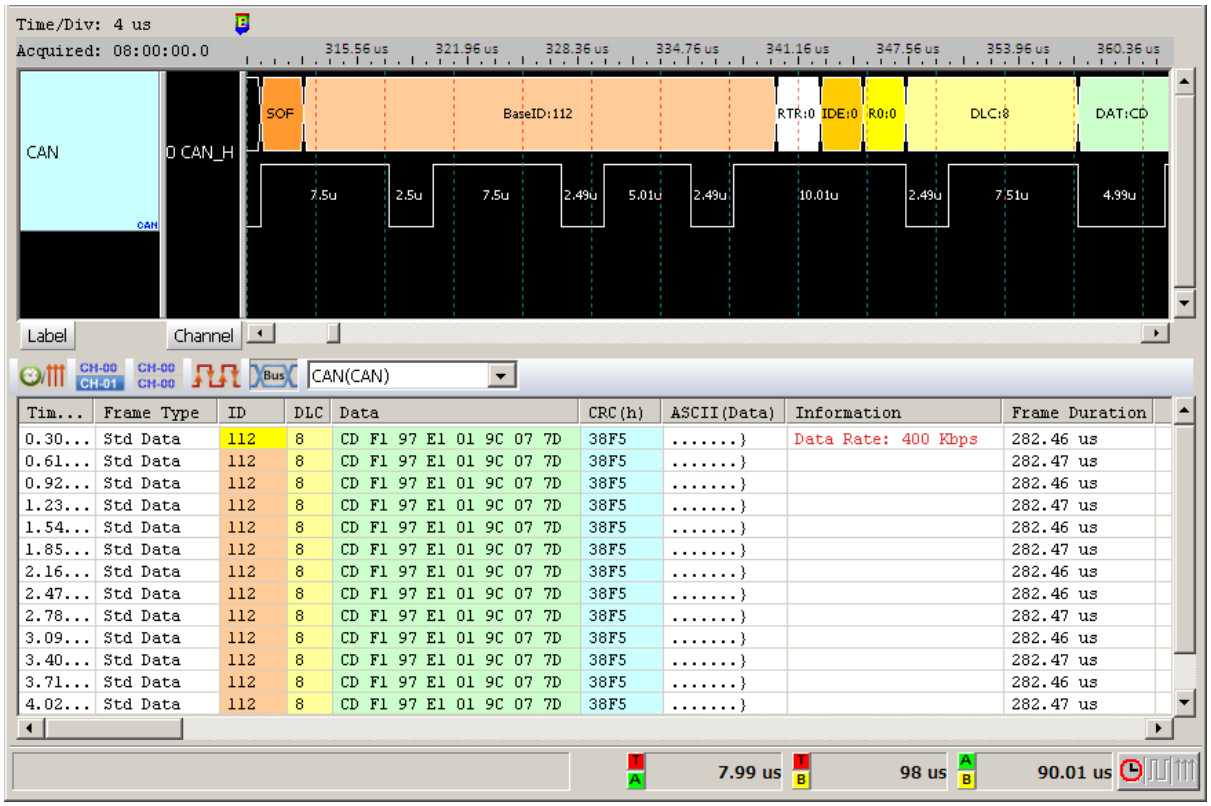
Auto detect Data Rate: Check this option for auto-detecting the CAN bit rate by the LA Viewer; this option will be disabled when enabling CAN FD decode, the maximum input range of the Data rate is from 5Kbps-1Mbps.

Show scale in the waveform: Display the scale in the Waveform Window, this option will be disabled when enabling CAN FD decode.

Result

Click **OK** to run the CAN decode and see the result on the Waveform Window below.



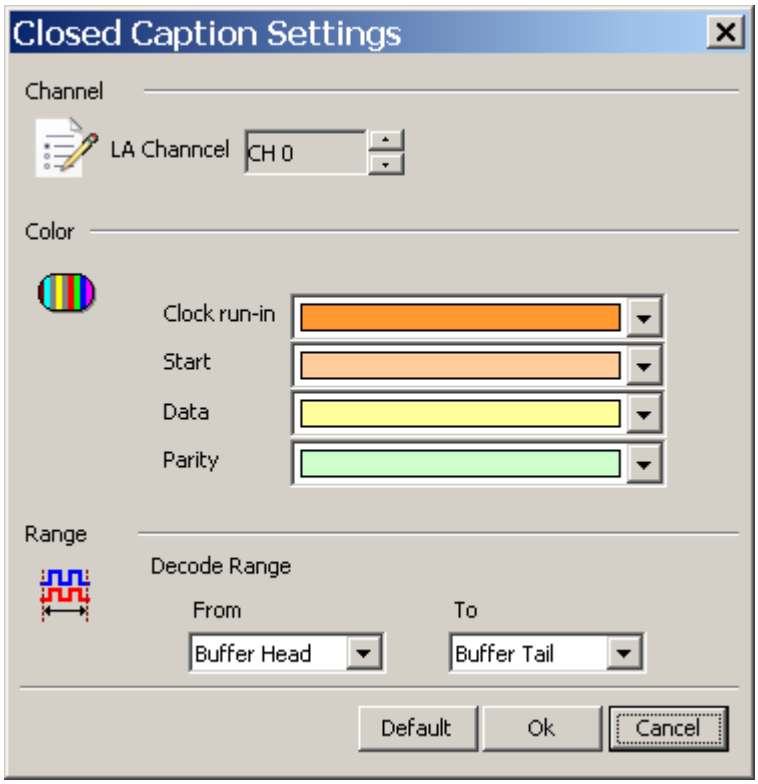


Tim...	Frame Type	ID	DLC	Data	CRC(h)	ASCII(Data)	Information	Frame Duration
0.30...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}	Data Rate: 400 Kbps	282.46 us
0.61...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
0.92...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
1.23...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
1.54...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
1.85...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
2.16...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
2.47...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
2.78...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
3.09...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
3.40...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us
3.71...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.46 us
4.02...	Std Data	112	8	CD F1 97 E1 01 9C 07 7D	38F5	.......}		282.47 us

Closed Caption

Closed captioning is the process of displaying text on a TV or video screen. The text is encoded in the video data stream.

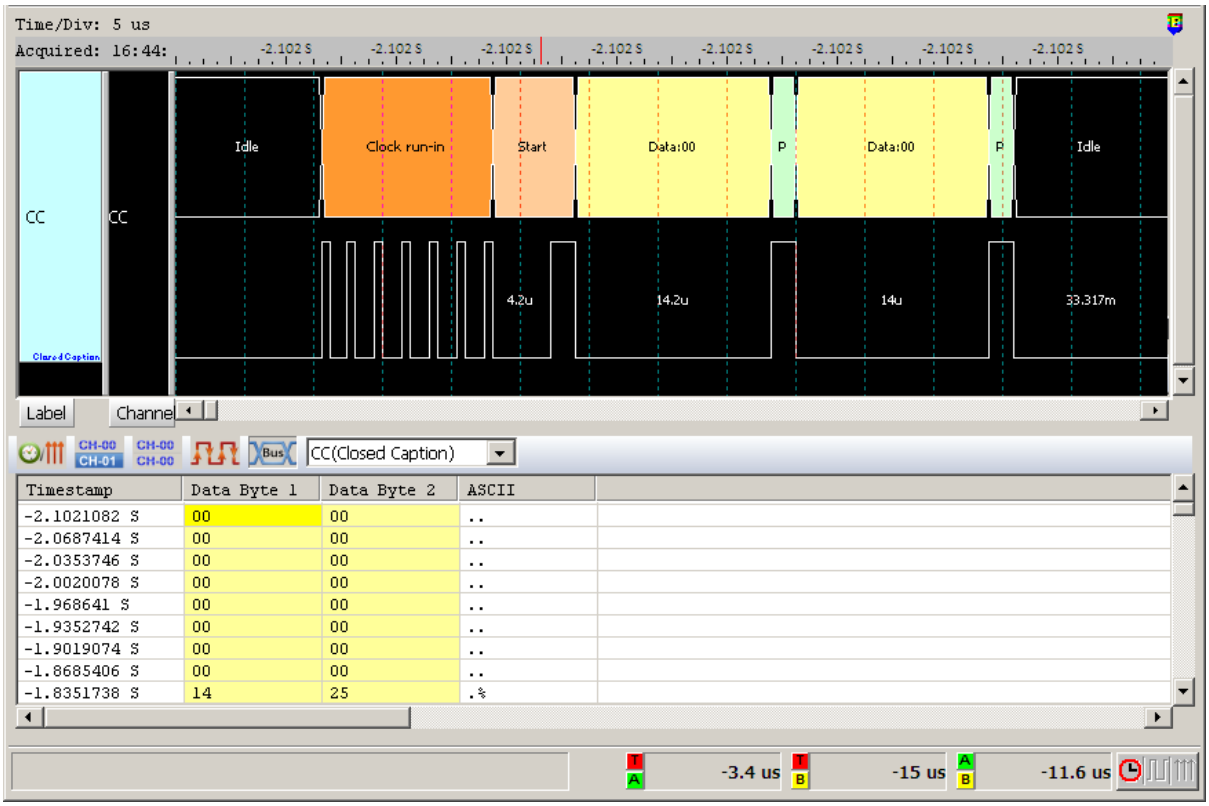
Settings



LA Channel: Show the selected channel (CH0).

Result

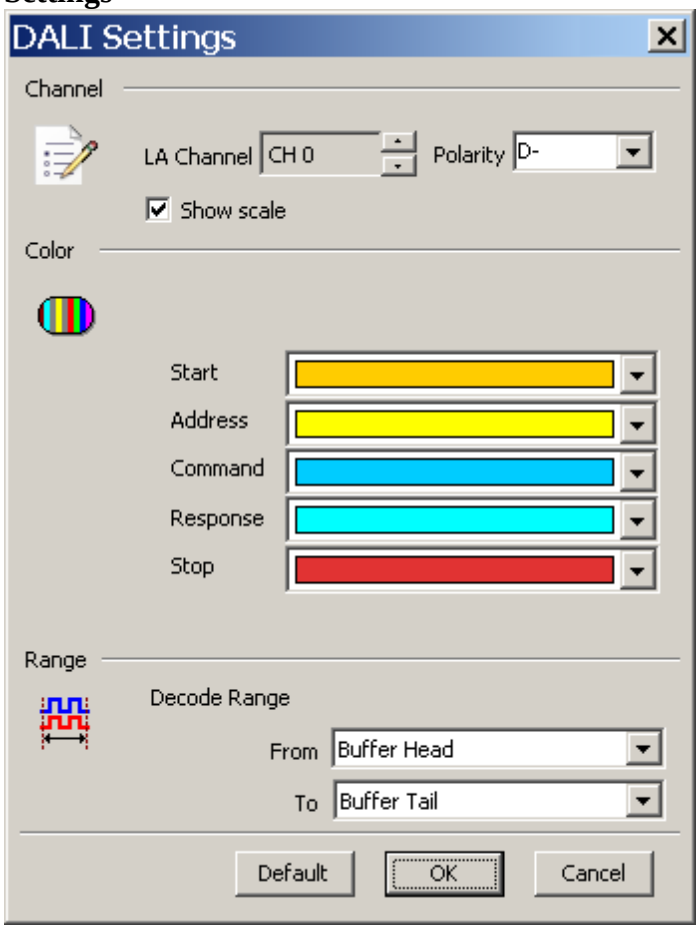
Click OK to run the Closed Caption Decode and see result on the Waveform Window below.



DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings



LA Channel: Show the selected channel (CH0).

Polarity:

D-: Access side of the signal polarity is D-.

D+: Access side of the signal polarity is D+.

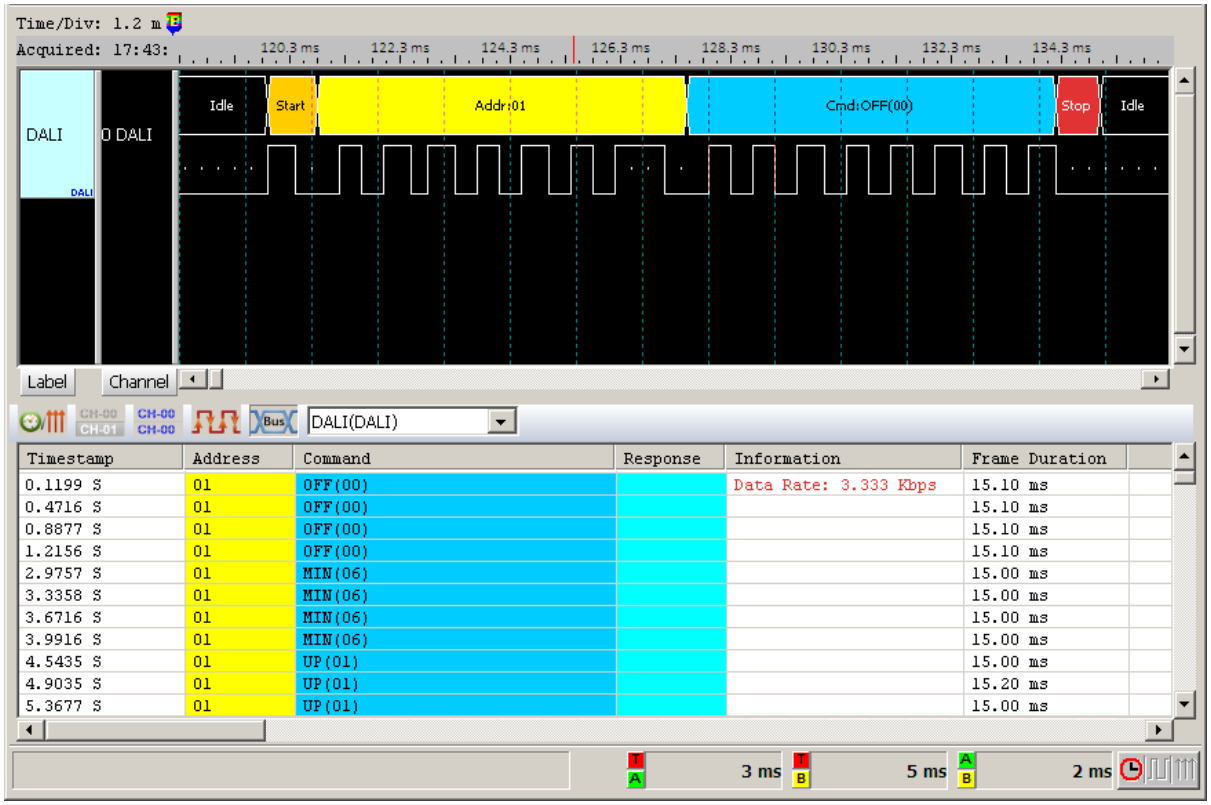
Auto: Automatically detect the polarity of the access end signal.

Show scale: Show Scale on the waveform.

Result

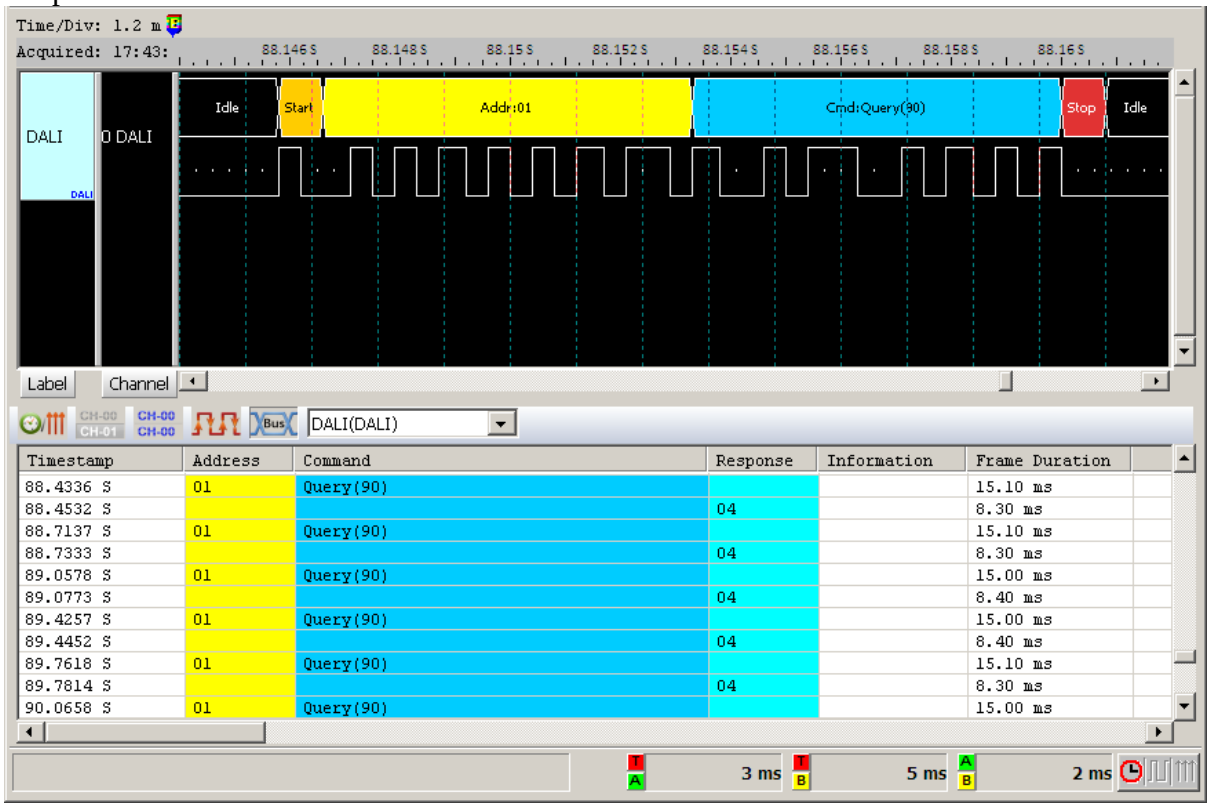
Click OK to run DALI Decode and see result on the Waveform Window below.

Send data



Timestamp	Address	Command	Response	Information	Frame Duration
0.1199 S	01	OFF(00)		Data Rate: 3.333 Kbps	15.10 ms
0.4716 S	01	OFF(00)			15.10 ms
0.8877 S	01	OFF(00)			15.10 ms
1.2156 S	01	OFF(00)			15.10 ms
2.9757 S	01	MIN(06)			15.00 ms
3.3358 S	01	MIN(06)			15.00 ms
3.6716 S	01	MIN(06)			15.00 ms
3.9916 S	01	MIN(06)			15.00 ms
4.5435 S	01	UP(01)			15.00 ms
4.9035 S	01	UP(01)			15.20 ms
5.3677 S	01	UP(01)			15.00 ms

Response data

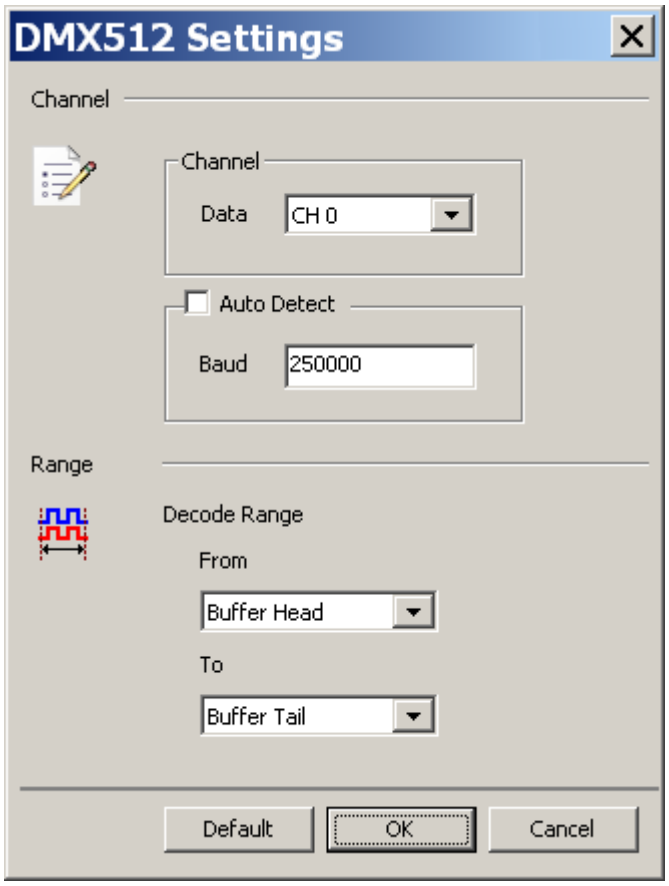


Timestamp	Address	Command	Response	Information	Frame Duration
88.4336 S	01	Query(90)			15.10 ms
88.4532 S			04		8.30 ms
88.7137 S	01	Query(90)			15.10 ms
88.7333 S			04		8.30 ms
89.0578 S	01	Query(90)			15.00 ms
89.0773 S			04		8.40 ms
89.4257 S	01	Query(90)			15.00 ms
89.4452 S			04		8.40 ms
89.7618 S	01	Query(90)			15.10 ms
89.7814 S			04		8.30 ms
90.0658 S	01	Query(90)			15.00 ms

DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings

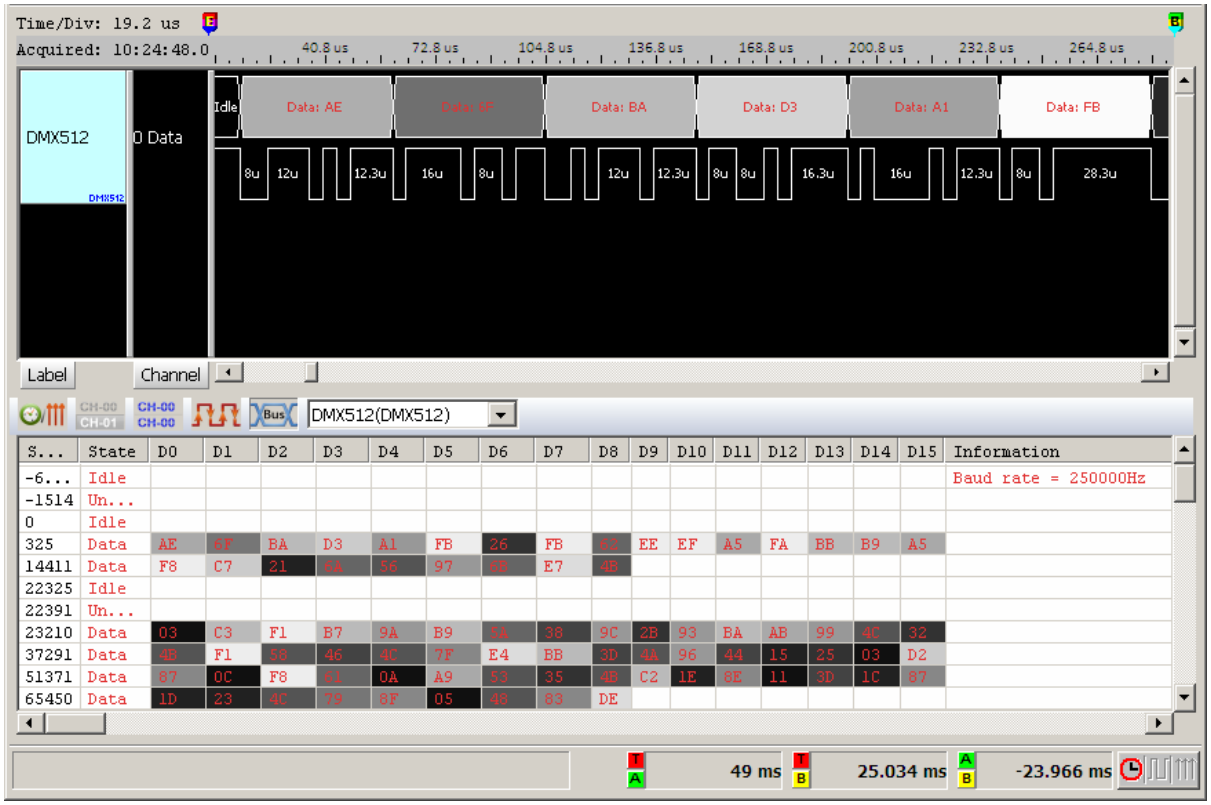


Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

Result

Use grayscale to display the decode results.

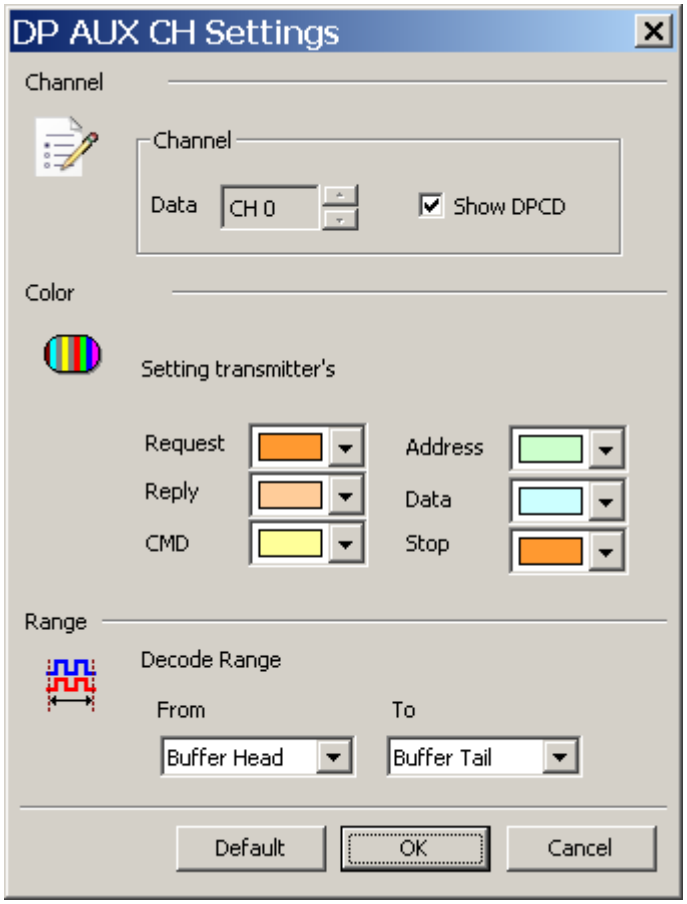


S...	State	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	Information
-6...	Idle																	Baud rate = 250000Hz
-1514	Un...																	
0	Idle																	
325	Data	AE	6F	BA	D3	A1	FB	26	FB	62	EE	EF	A5	FA	BB	B9	A5	
14411	Data	F8	C7	21	6A	56	97	6B	E7	4B								
22325	Idle																	
22391	Un...																	
23210	Data	03	C3	F1	B7	9A	B9	5A	38	9C	2B	93	BA	AB	99	4C	32	
37291	Data	4B	F1	58	46	4C	7F	E4	BB	3D	4A	96	44	15	25	03	D2	
51371	Data	87	0C	F8	61	0A	A9	53	35	4B	C2	1E	8E	11	3D	1C	87	
65450	Data	1D	23	4C	79	8F	05	48	83	DE								

Display Port Auxiliary Channel (DP Aux Ch)

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard.

Settings

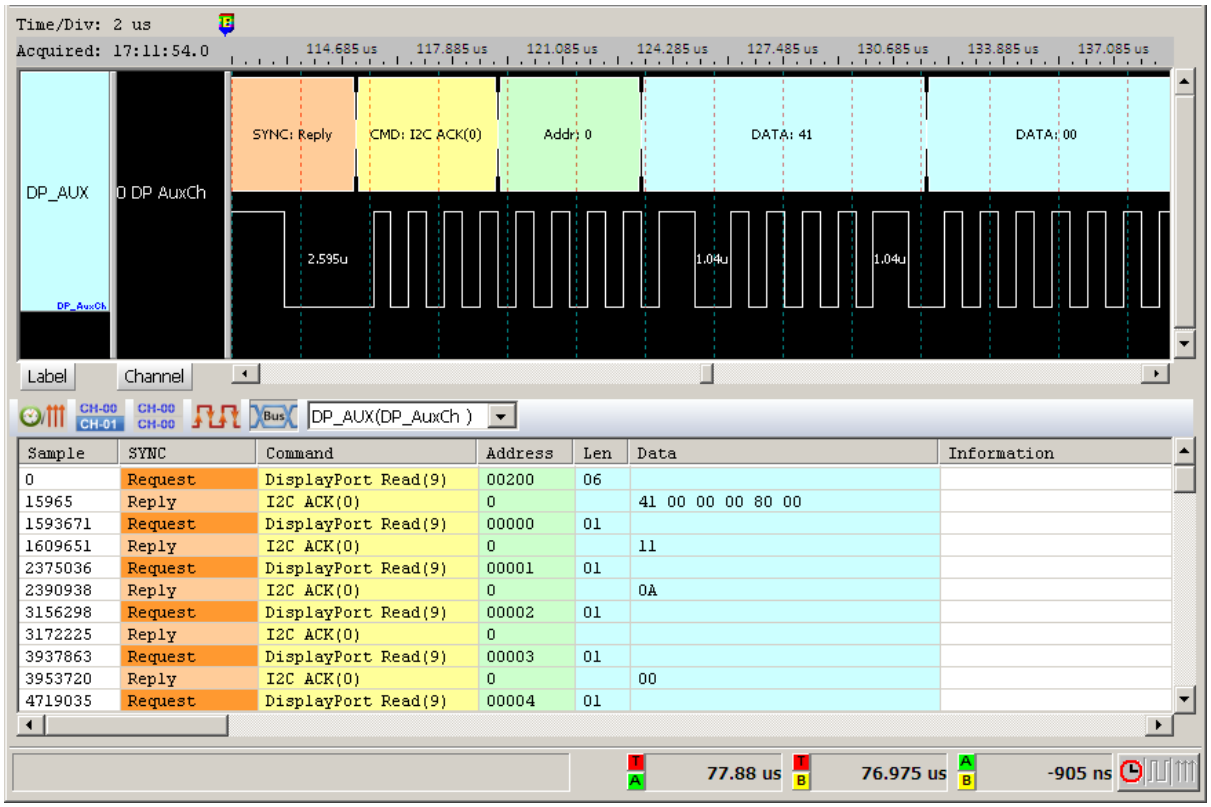


Data: Show the selected channel (CH0).

Show DPCD: Show the Display Port Configuration data.

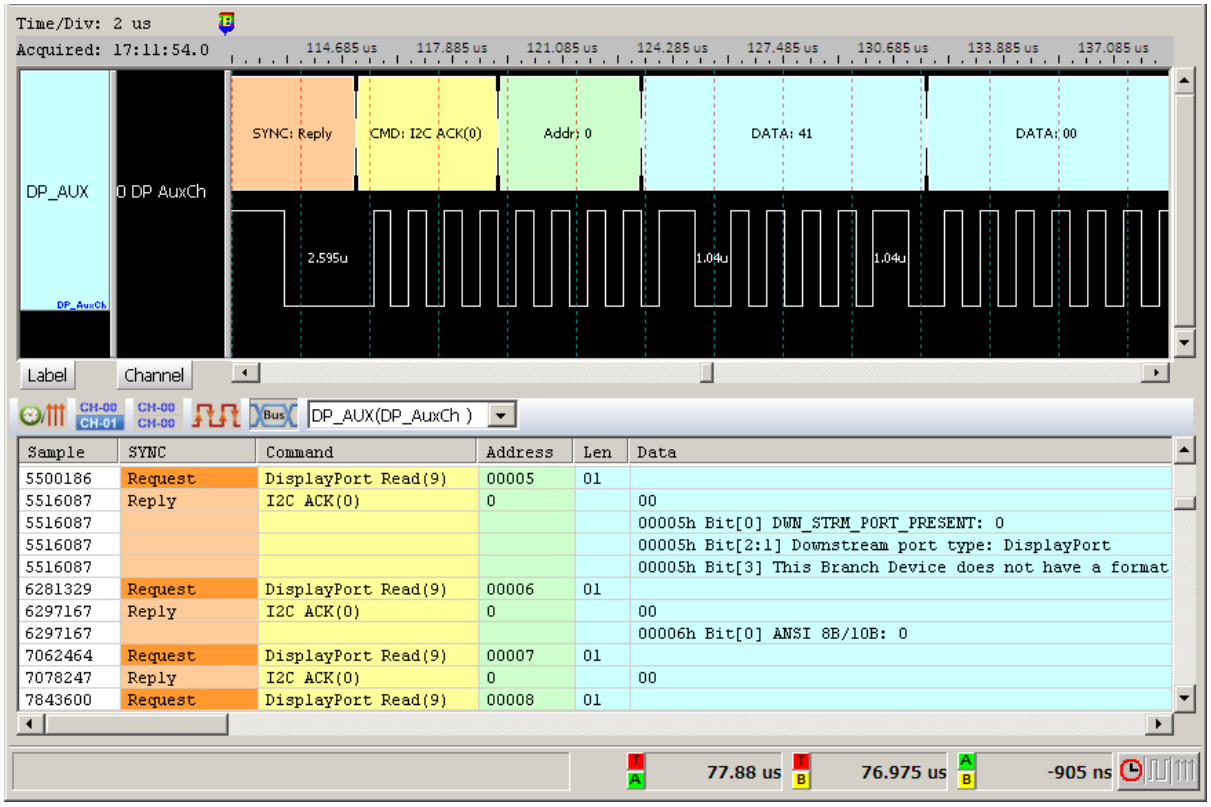
Result

Without the DPCD information



Sample	SYNC	Command	Address	Len	Data	Information
0	Request	DisplayPort Read(9)	00200	06		
15965	Reply	I2C ACK(0)	0		41 00 00 00 80 00	
1593671	Request	DisplayPort Read(9)	00000	01		
1609651	Reply	I2C ACK(0)	0		11	
2375036	Request	DisplayPort Read(9)	00001	01		
2390938	Reply	I2C ACK(0)	0		0A	
3156298	Request	DisplayPort Read(9)	00002	01		
3172225	Reply	I2C ACK(0)	0			
3937863	Request	DisplayPort Read(9)	00003	01		
3953720	Reply	I2C ACK(0)	0		00	
4719035	Request	DisplayPort Read(9)	00004	01		

Show the DPCD information

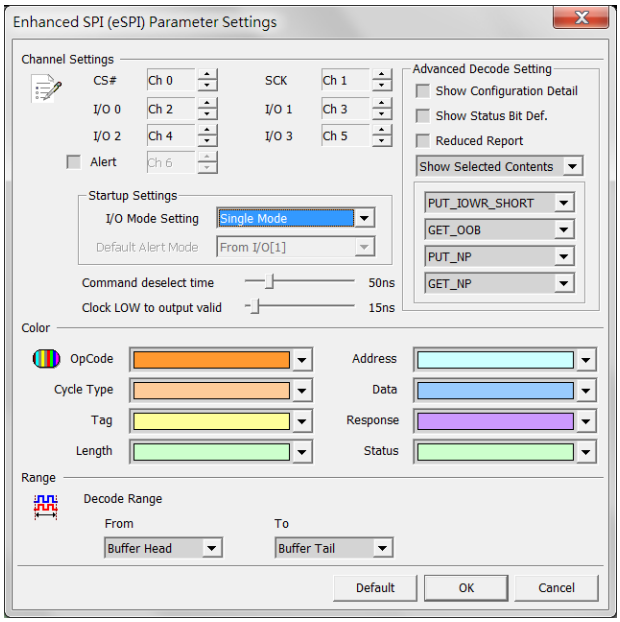


Sample	SYNC	Command	Address	Len	Data
5500186	Request	DisplayPort Read(9)	00005	01	
5516087	Reply	I2C ACK(0)	0		00
5516087					00005h Bit[0] DWN_STRM_PORT_PRESENT: 0
5516087					00005h Bit[2:1] Downstream port type: DisplayPort
5516087					00005h Bit[3] This Branch Device does not have a format
6281329	Request	DisplayPort Read(9)	00006	01	
6297167	Reply	I2C ACK(0)	0		00
6297167					00006h Bit[0] ANSI 8B/10B: 0
7062464	Request	DisplayPort Read(9)	00007	01	
7078247	Reply	I2C ACK(0)	0		00
7843600	Request	DisplayPort Read(9)	00008	01	

Enhanced Serial Peripheral Interface (eSPI)

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings



Channel:

CS#: Chip Select (Active Low)

SCK: Clock

I/O0 – I/O3: Data input / output

Alert: Alert signal (Optional)

Startup Settings:

I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I / O state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

Command deselect time: Set tSHSL, Chip Select# Deassertion Time.

Clock LOW to output valid: Set tCLQV, Output Data Valid Time.

Advanced Decode Setting:

Show Configuration Detail: Show details of SET_CONFIG / GET_CONFIG.

Show Status Bit Def.: Show details of Status.

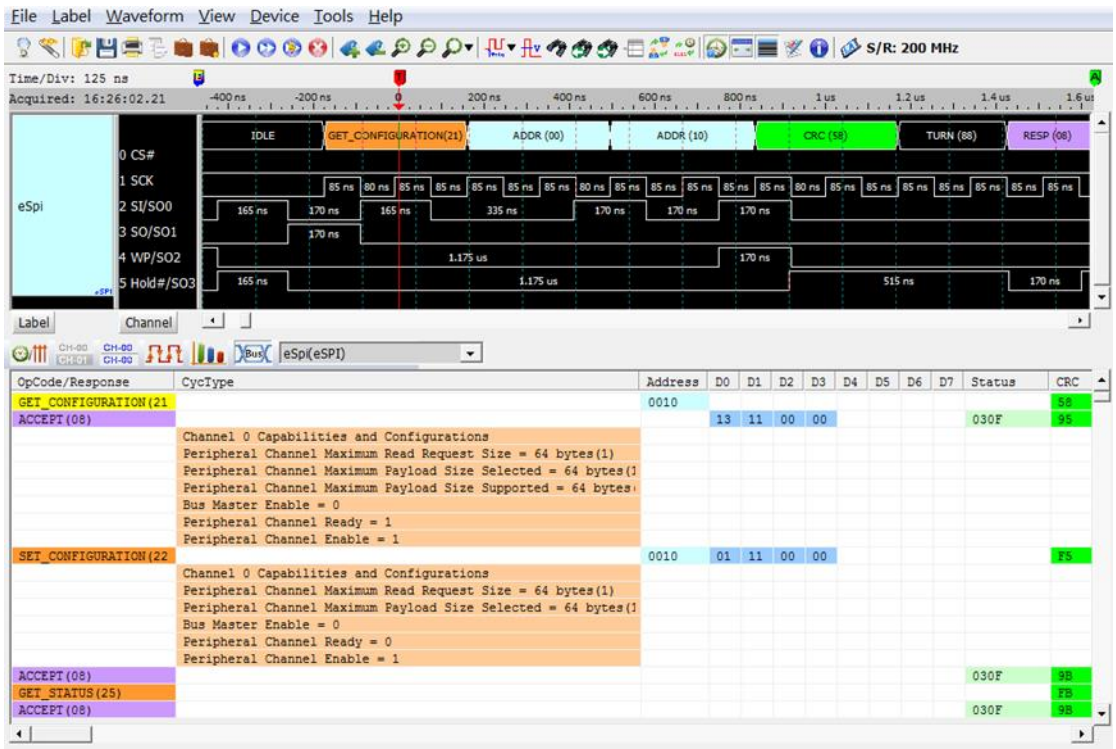
Reduced Report: Reducing the report is easy to check the Command Flow.

Filter Setting: To show or hide the specific OP Code / Cycle Type or Address range in the report.

Note: The setting of Address Filter would be saved as LA\eSPI\eSPIFilterX.bin in the work directory.

Result

Click **OK** to run the eSPI decode and see the result on the Waveform Window below.

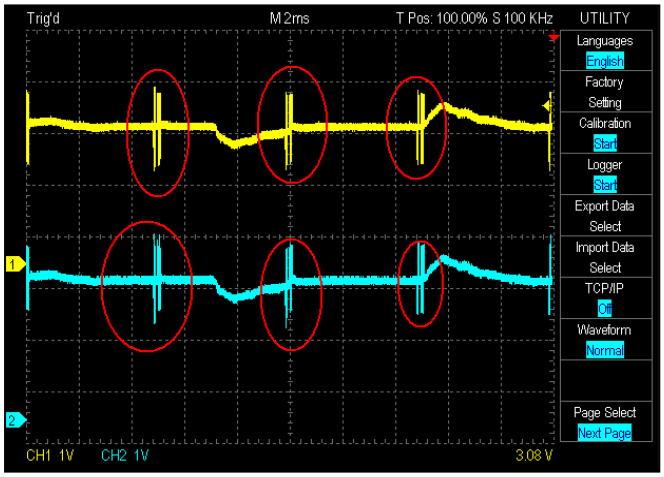


FlexRay

The FlexRay protocol has 2 bits with timing at 10Mbps.

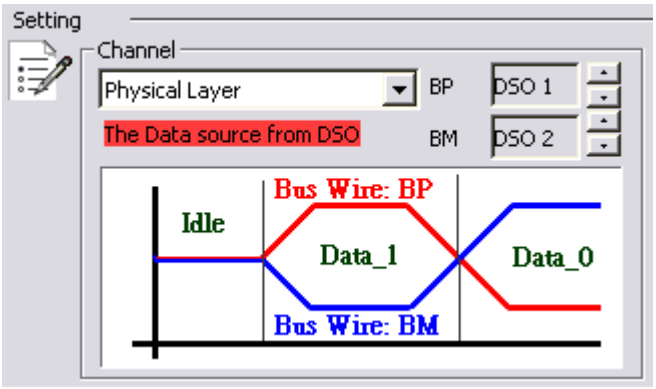
FlexRay signal

Physical Layer: We use the DSO to measure the differential signal at the FlexRay physical layer and get the blue-color BP signal and the yellow-color BM signal as the picture below.



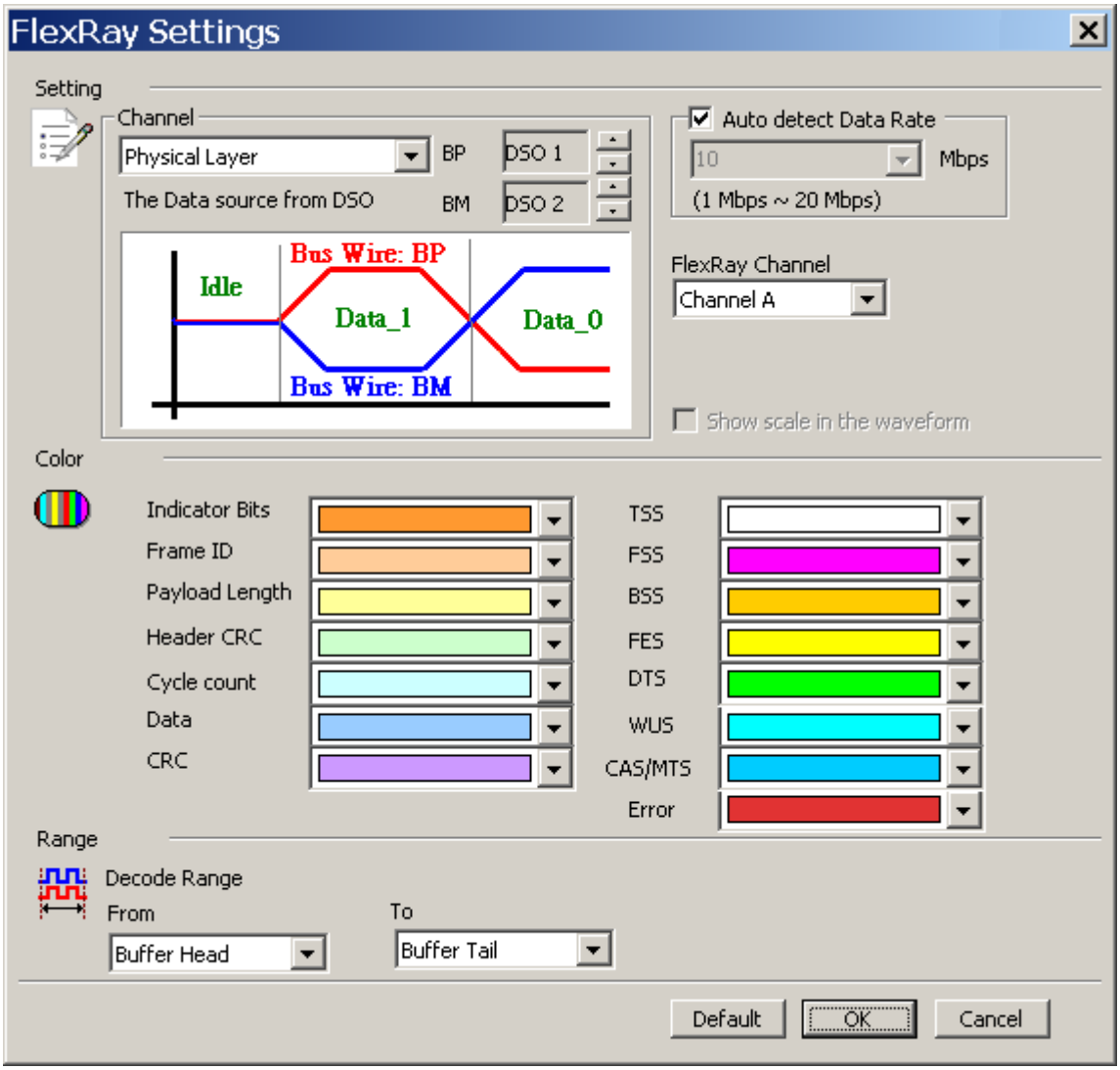
Then, we subtract BP and BM values and get the red-color signal used by the logic analyzer to decode the FlexRay bus as the picture above.

In order to trigger from the logic analyzer, you need to connect the logic analyzer to either the BP or BM pin in the setting dialog on the right.



Communication Data Layer: The FlexRay communication data is either at transmitter (Txd) or receiver (Rxd) of the FlexRay transceiver. You may set the threshold according to the FlexRay transceiver voltage.

Settings



Channel: Display the channel, Physical Layer is the default.

Physical Layer: The signals (BP, BM) are from the DSODSO channels can be Ch1 - Ch6.

Communication Data (TxD): The TxD data is from the TxD and TxEN of the FlexRay transceiver.

Communication Data (RxD): The RxD data is from the RxD and RxEN of the FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.

FlexRay Channel: Channel A or B, for Frame CRC checking.

Errors are:

Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

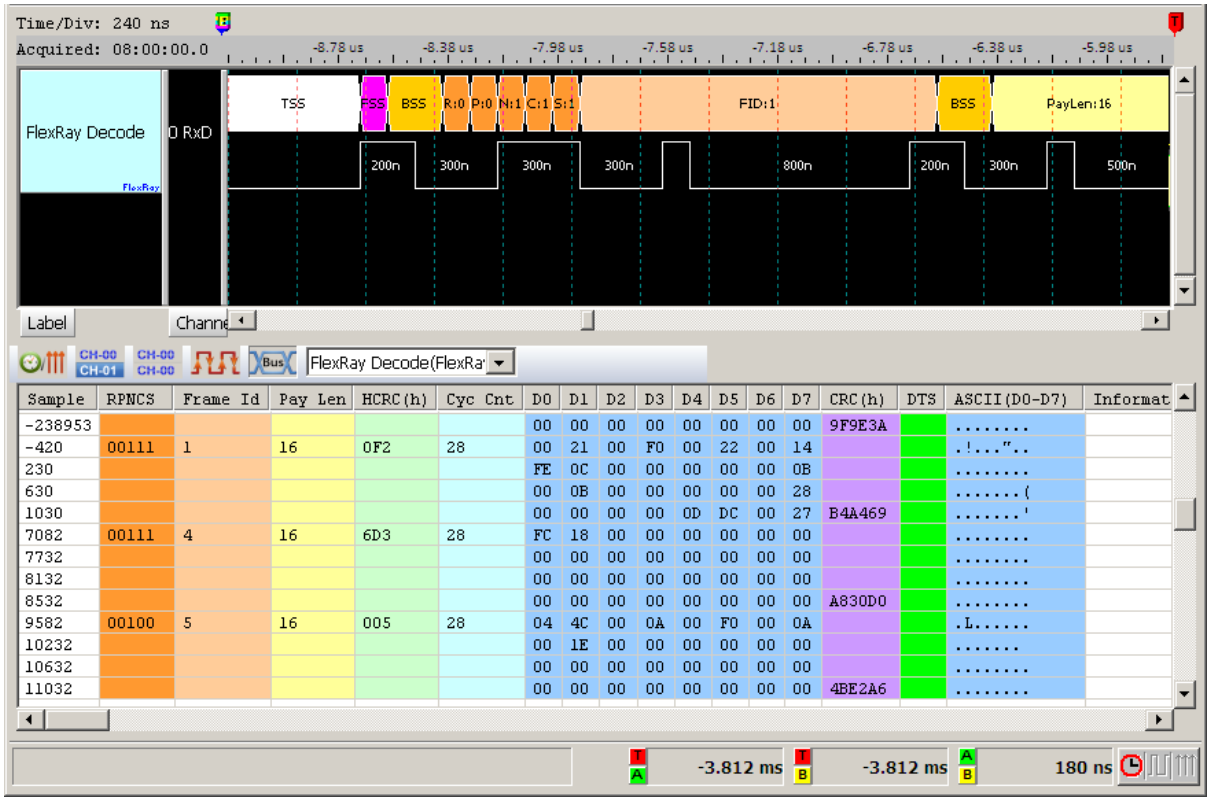
Abbreviations are:

Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol
WUP	Wakeup Pattern
CID	Channel Idle Delimiter

Result

Click **OK** to run the FlexRay decode and see the result on the Waveform Window below.

10Mbps FlexRay Communication Data(RxD)

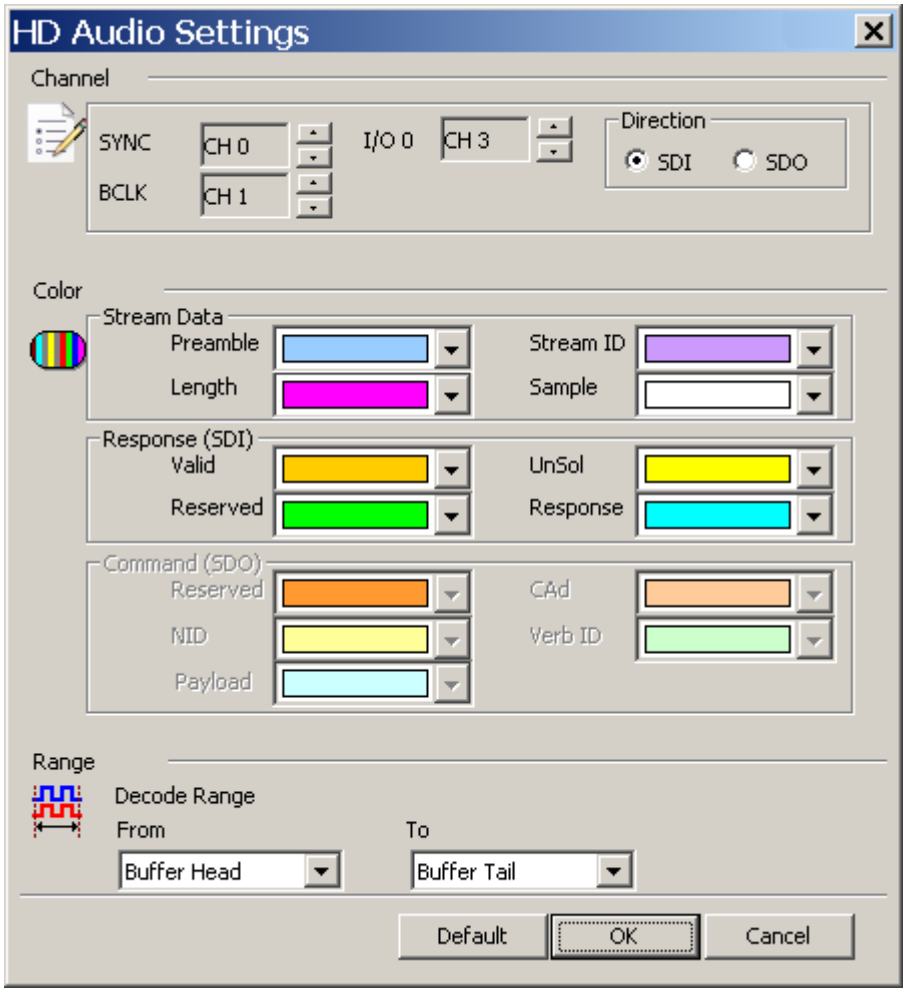


Sample	RPNCS	Frame Id	Pay Len	HCRC(h)	Cyc Cnt	D0	D1	D2	D3	D4	D5	D6	D7	CRC(h)	DTS	ASCII(D0-D7)	Informat
-238953						00	00	00	00	00	00	00	00	9F9E3A		....	
-420	00111	1	16	0F2	28	00	21	00	F0	00	22	00	14			.!.."..	
230						FE	0C	00	00	00	00	00	0B			....	
630						00	0B	00	00	00	00	00	28			.......(	
1030						00	00	00	00	0D	DC	00	27	B4A469		.......'	
7082	00111	4	16	6D3	28	FC	18	00	00	00	00	00	00			....	
7732						00	00	00	00	00	00	00	00			....	
8132						00	00	00	00	00	00	00	00			....	
8532						00	00	00	00	00	00	00	00	A830D0		....	
9582	00100	5	16	005	28	04	4C	00	0A	00	F0	00	0A			.L......	
10232						00	1E	00	00	00	00	00	00			....	
10632						00	00	00	00	00	00	00	00			....	
11032						00	00	00	00	00	00	00	00	4BE2A6		....	

HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

Settings

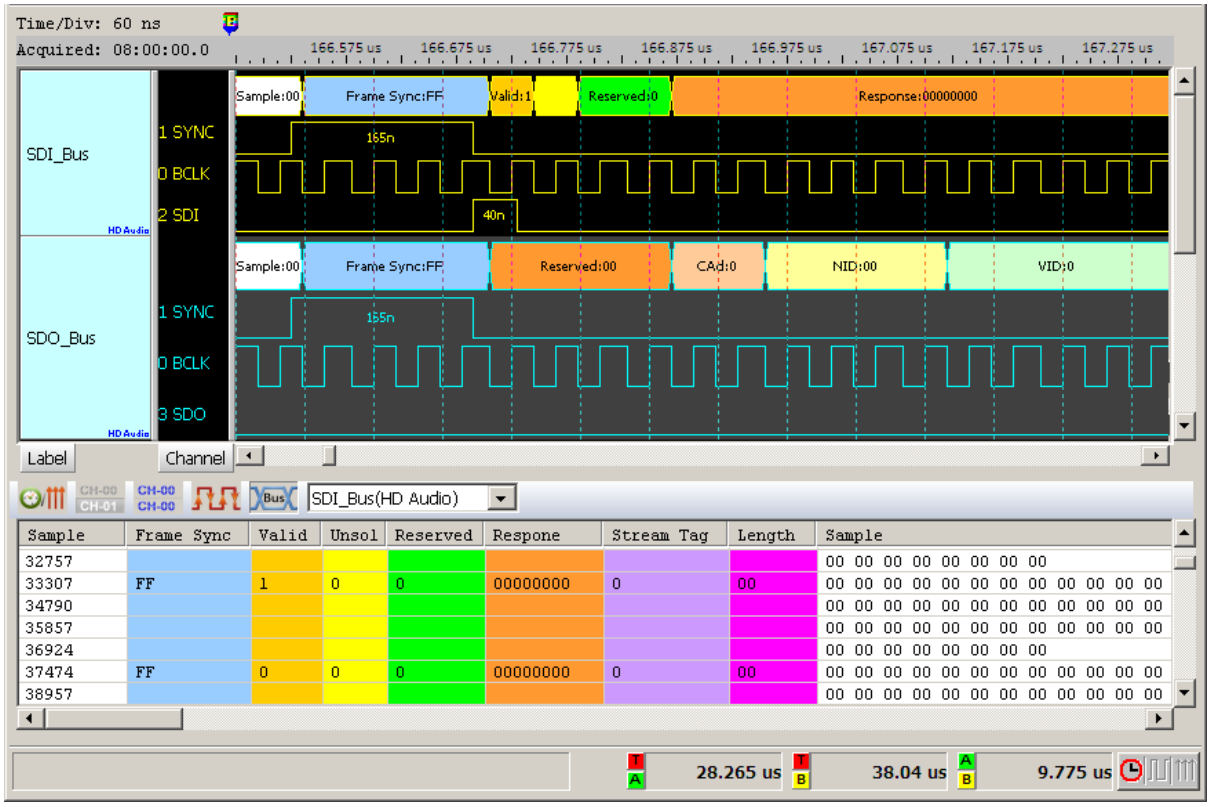


Channel: Show the selected channel (CH 0-CH3).

Direction: Show the data with SDI or SDO decoding.

Result

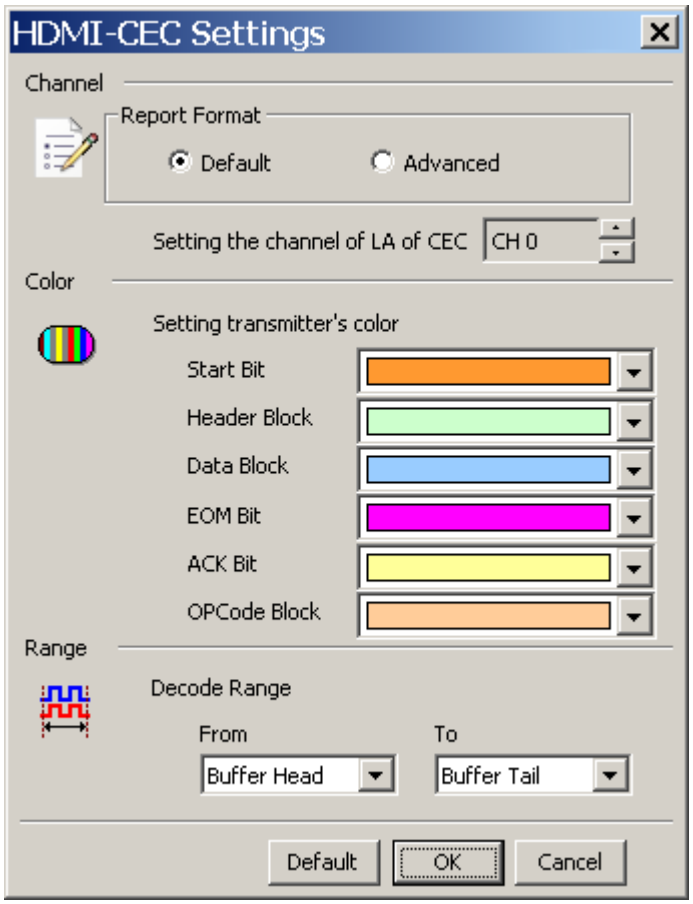
Click **OK** to run the HD Audio decode and see the result on the Waveform Window below.



HDMI-CEC

The HDMI-CEC bus is a one-wire, “party line” that connects up to ten (10) AV devices through standard HDMI cabling. The CEC protocol includes automatic mechanisms for physical address (topology) discovery, (product type based) logical addressing, arbitration, retransmission, broadcasting, and routing control. Message opcodes support both device specific (e.g. set-top-box, DTV, and player) and general features (e.g. for power, signal routing, remote control pass-through, and on-screen display).

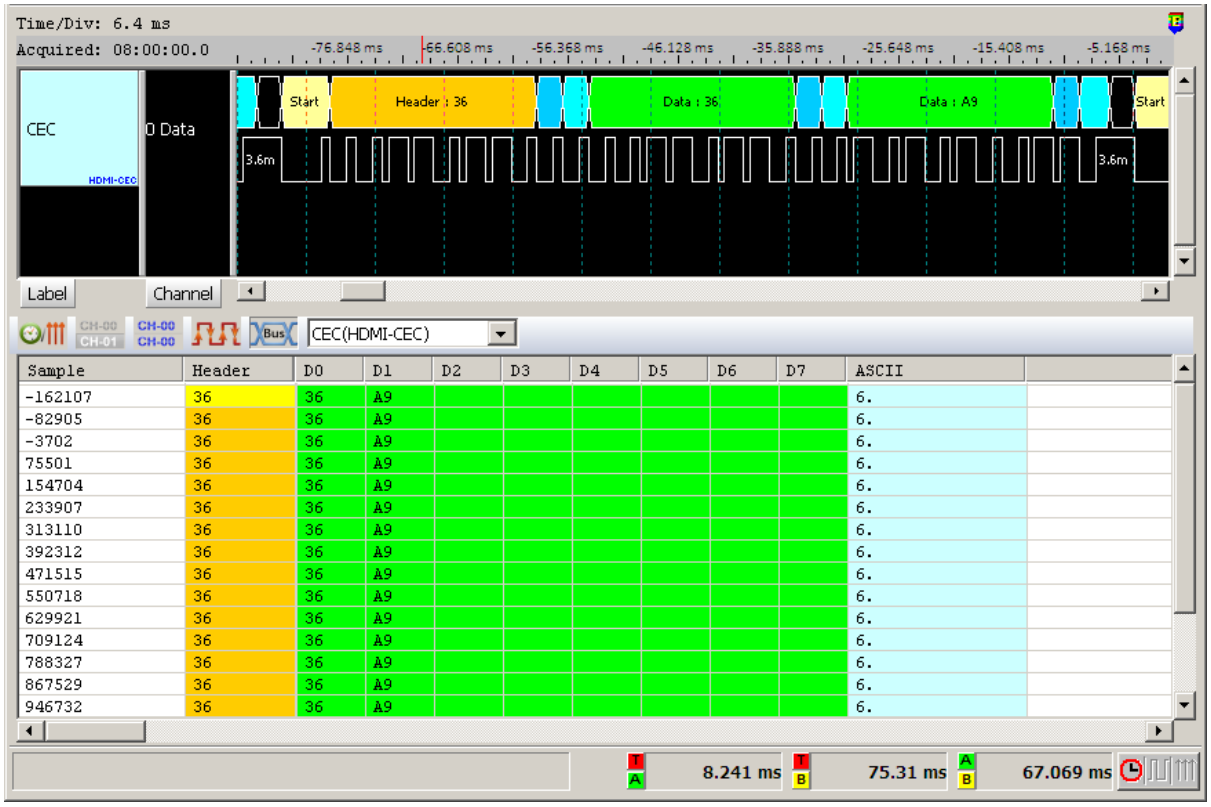
Settings



Latch data: Nominal (1.05 micro seconds) or User Define.

Result

Click **OK** to run the HDMI-CEC decode and see the result on the Waveform Window below.

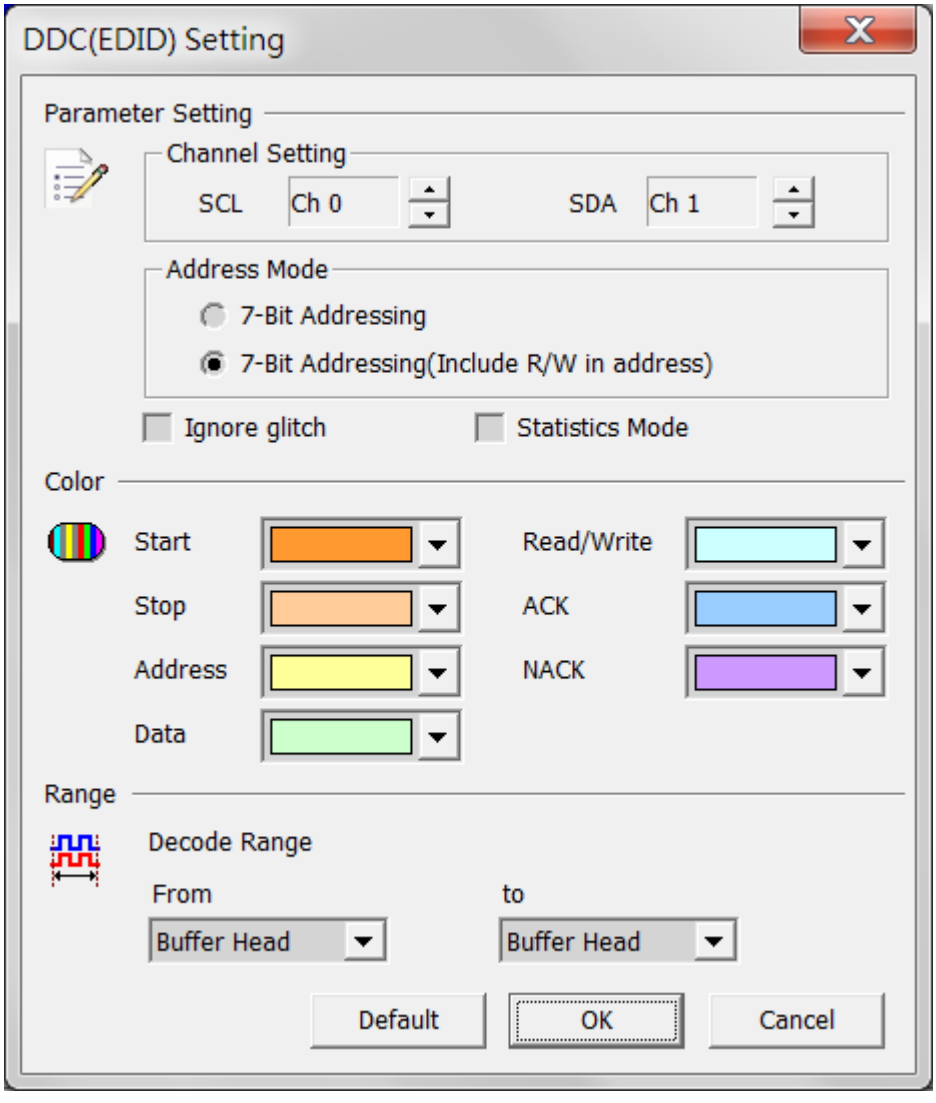


Sample	Header	D0	D1	D2	D3	D4	D5	D6	D7	ASCII
-162107	36	36	A9							6.
-82905	36	36	A9							6.
-3702	36	36	A9							6.
75501	36	36	A9							6.
154704	36	36	A9							6.
233907	36	36	A9							6.
313110	36	36	A9							6.
392312	36	36	A9							6.
471515	36	36	A9							6.
550718	36	36	A9							6.
629921	36	36	A9							6.
709124	36	36	A9							6.
788327	36	36	A9							6.
867529	36	36	A9							6.
946732	36	36	A9							6.

HDMI-DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings



Channel: Display the channels (CH0 and CH1).

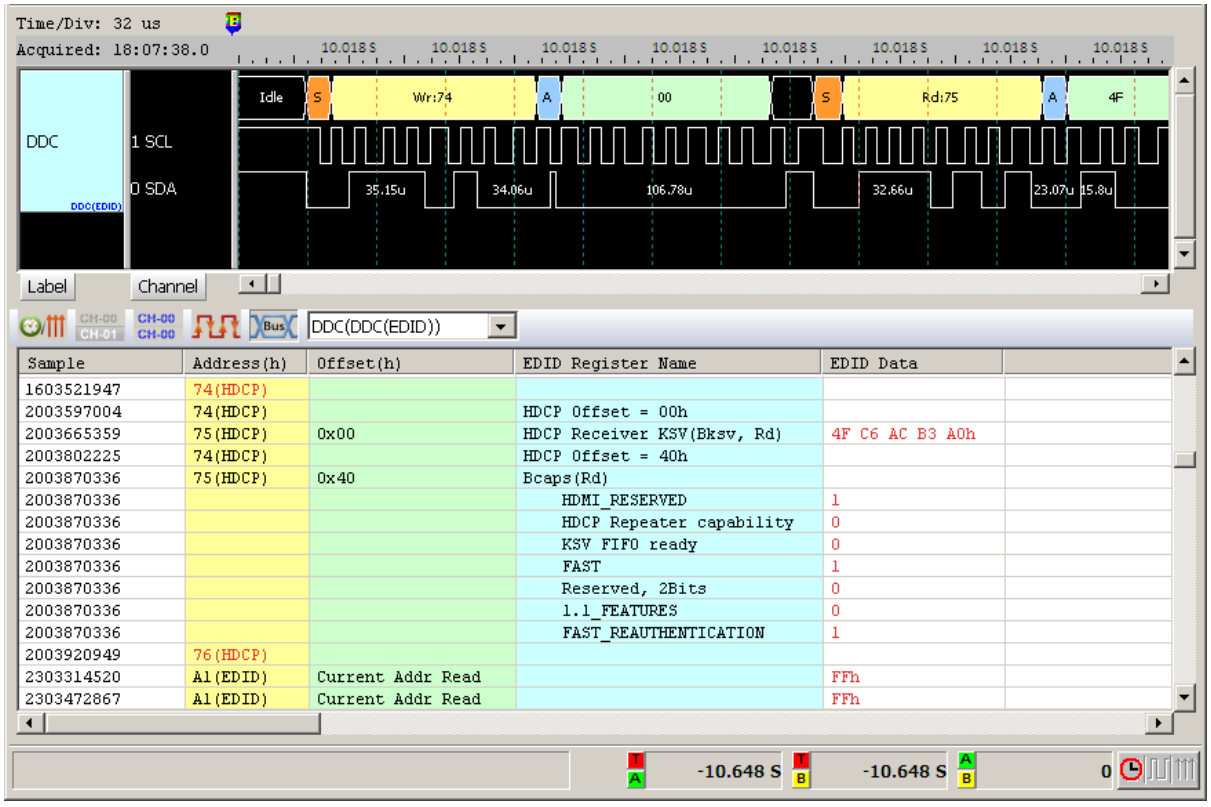
7-bit addressing: Show 7-bit addressing

7-bit addressing(Include R/W in Address): Show 8-bit addressing(include 7-bit addressing and 1-bit Rd/Wr).

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Statistic Mode: Collect all the data frames into one report by register address order.

Result

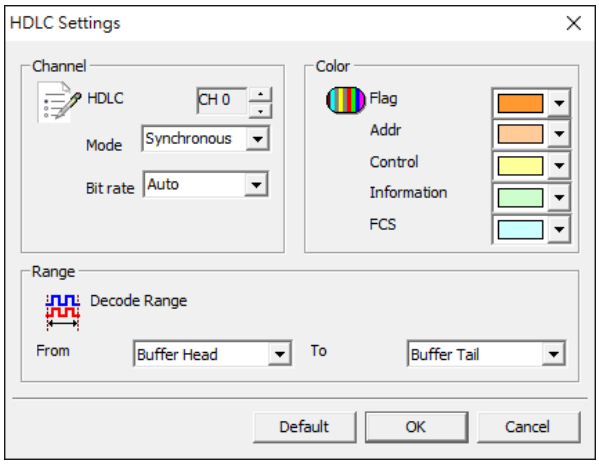


Sample	Address(h)	Offset(h)	EDID Register Name	EDID Data
1603521947	74(HDCP)			
2003597004	74(HDCP)		HDCP Offset = 00h	
2003665359	75(HDCP)	0x00	HDCP Receiver KSV(Bksv, Rd)	4F C6 AC B3 A0h
2003802225	74(HDCP)		HDCP Offset = 40h	
2003870336	75(HDCP)	0x40	Bcaps(Rd)	
2003870336			HDMI_RESERVED	1
2003870336			HDCP Repeater capability	0
2003870336			KSV FIFO ready	0
2003870336			FAST	1
2003870336			Reserved, 2Bits	0
2003870336			1.1_FEATURES	0
2003870336			FAST_REAUTHENTICATION	1
2003920949	76(HDCP)			
2303314520	AI(EDID)	Current Addr Read		FFh
2303472867	AI(EDID)	Current Addr Read		FFh

HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

Settings

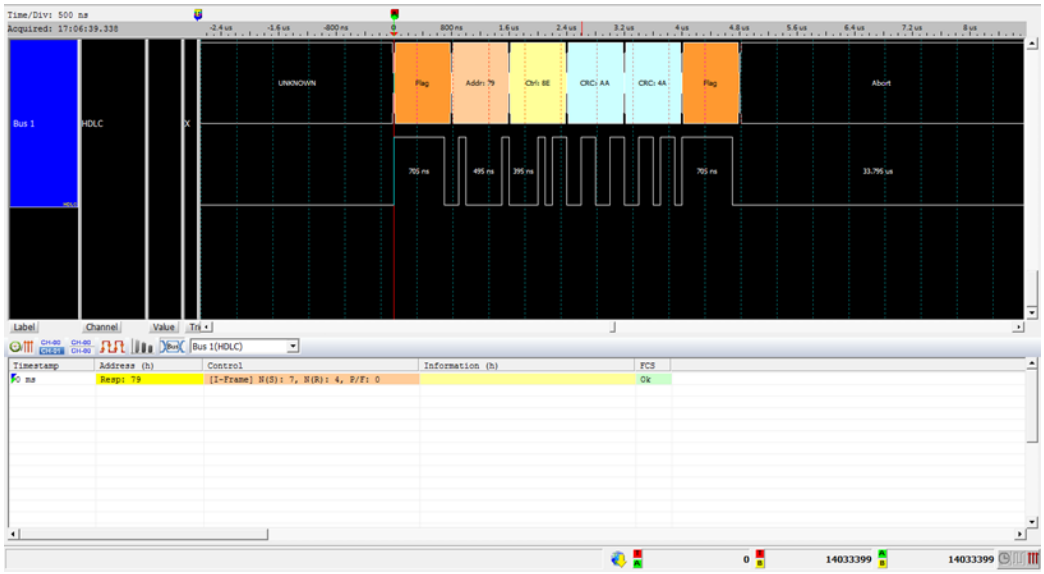


HDLC: Set the channel of the signal.

Mode: Synchronous or Asynchronous mode.

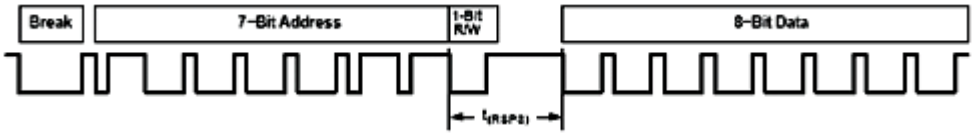
Bit rate: Set the specific data rate or auto detection.

Result

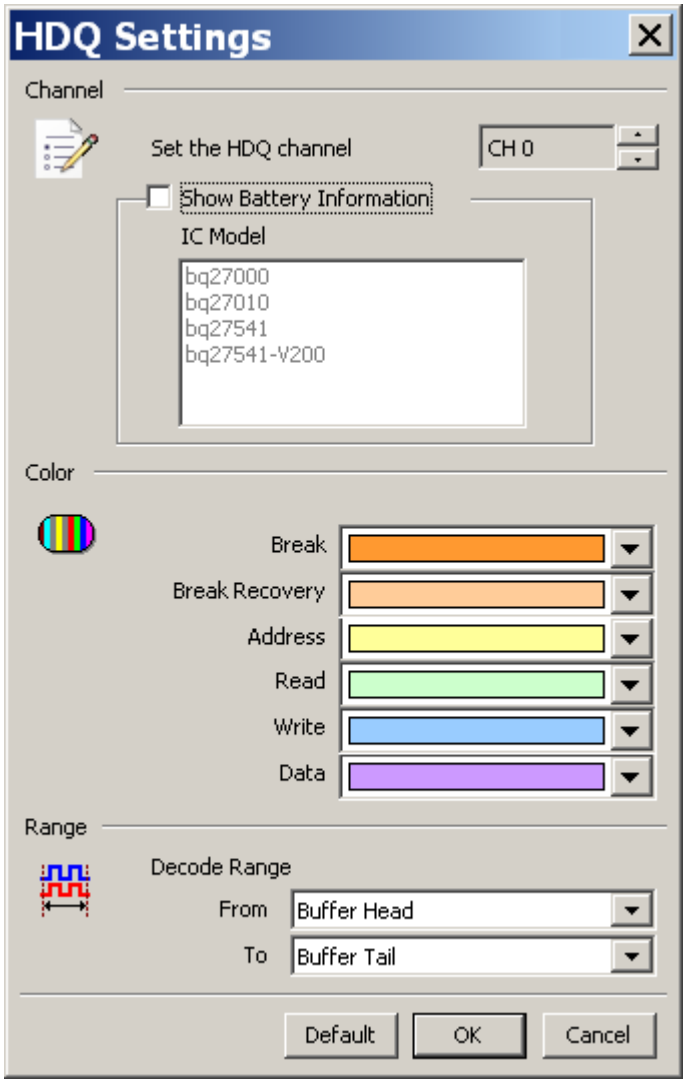


HDQ

The HDQ bus has two kinds of formats: 8 bits or 16 bits signals as the diagram below.



Settings

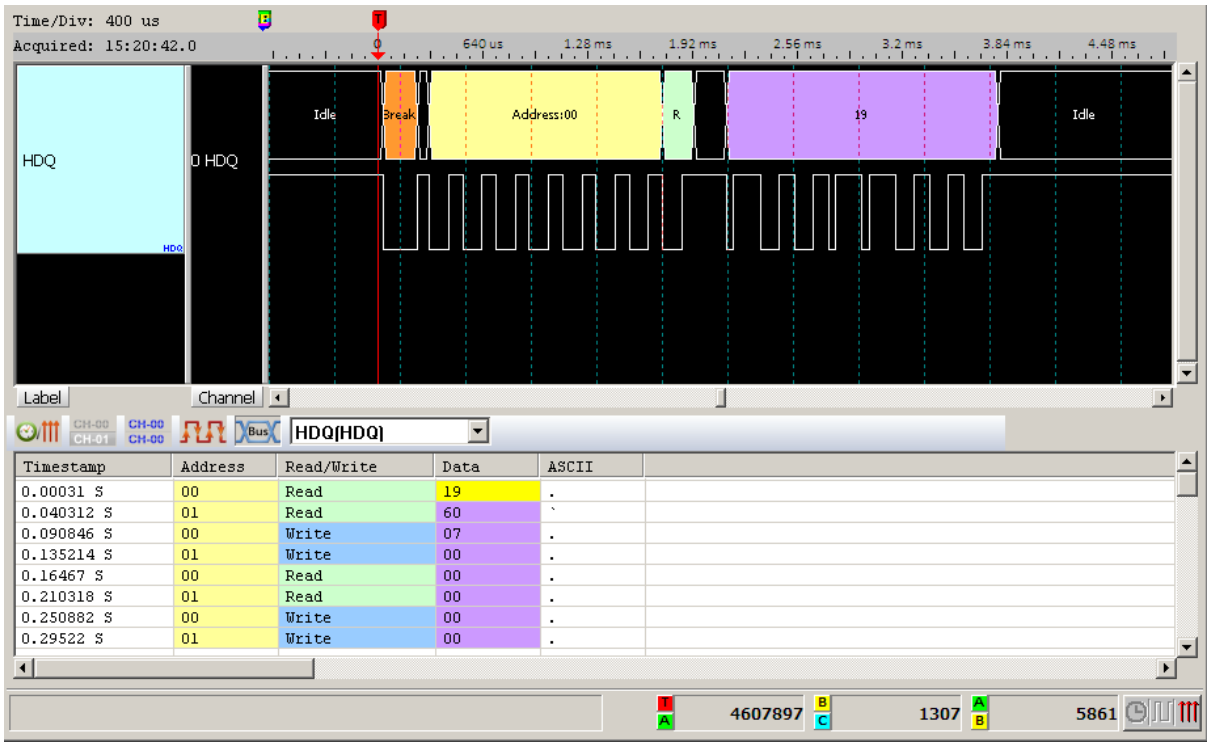


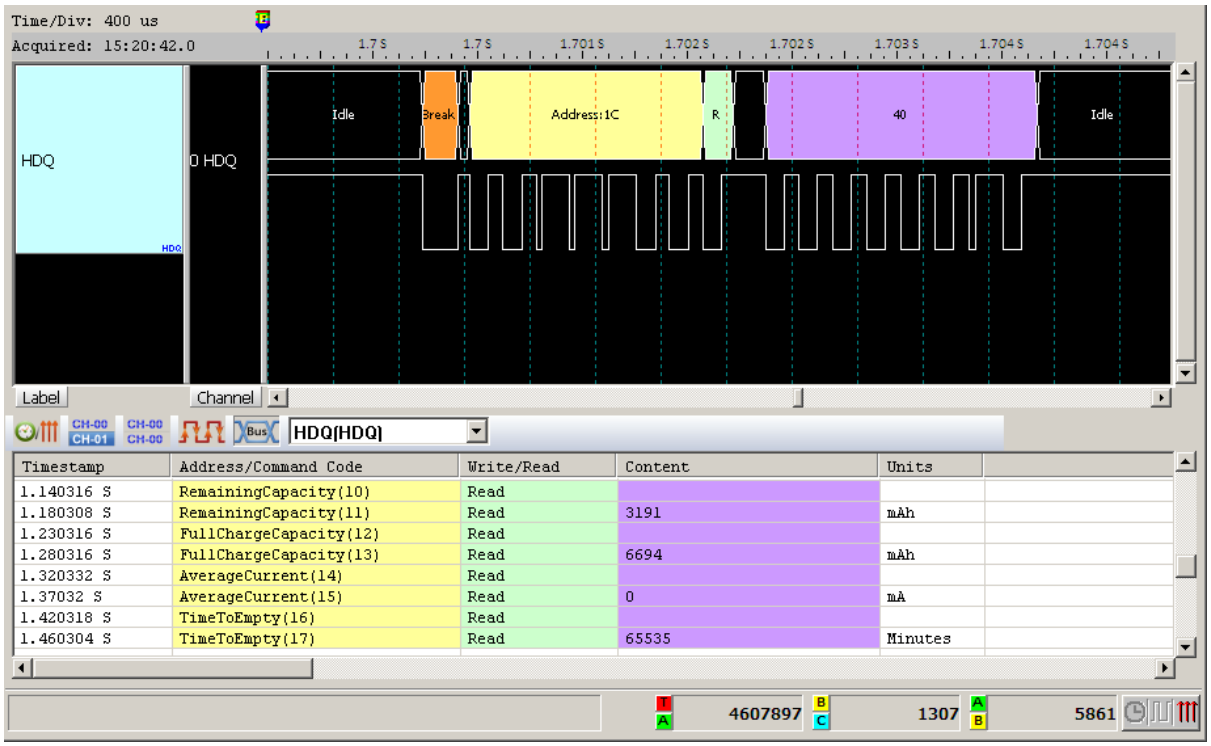
Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.

Result

Click **OK** to run the HDQ decode and see the result on the Waveform Window below.

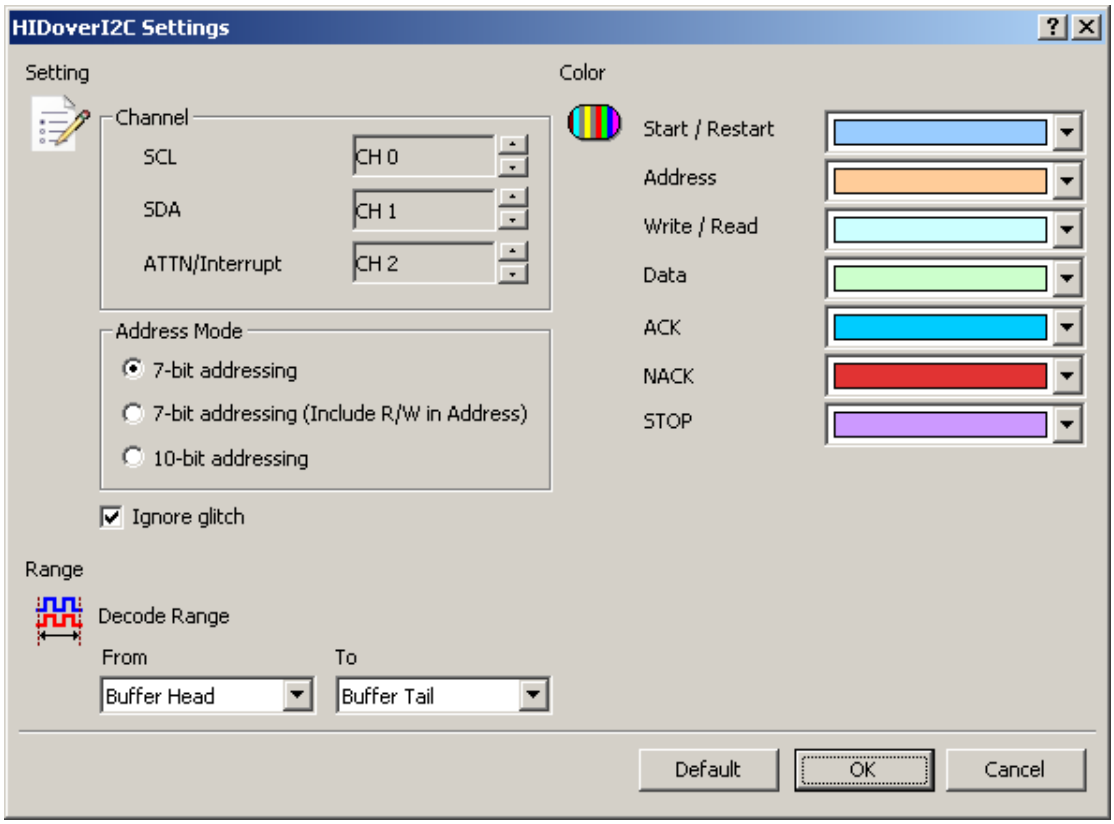




HID Over I²C

HID Over I2C (Human Interface Device Over I2C) protocol is established by Microsoft. It's applied for Windows 8 ARM platform.

Settings



Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

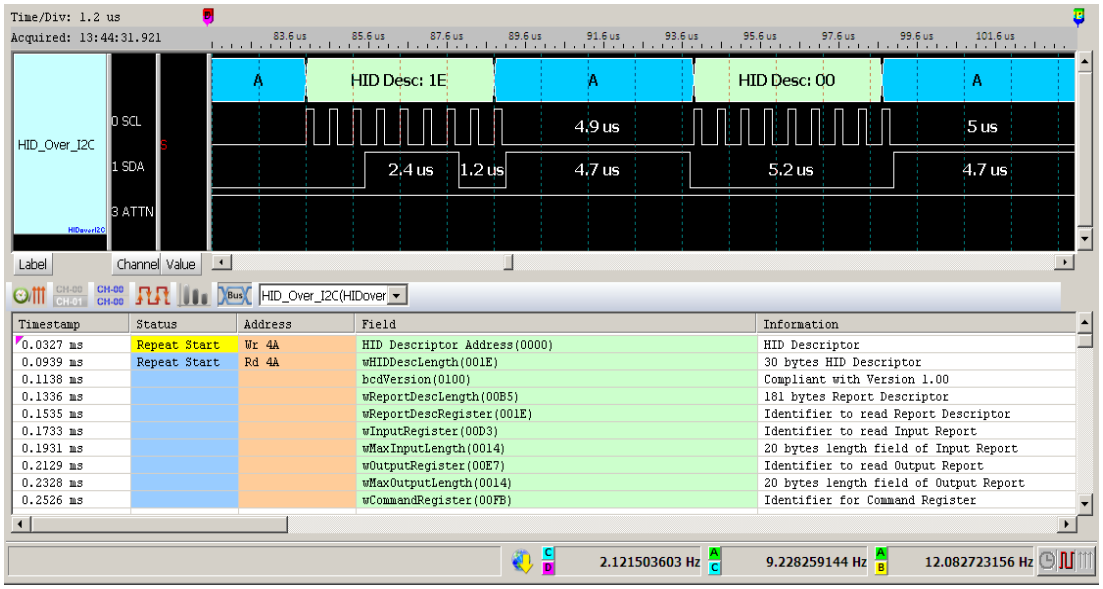
7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

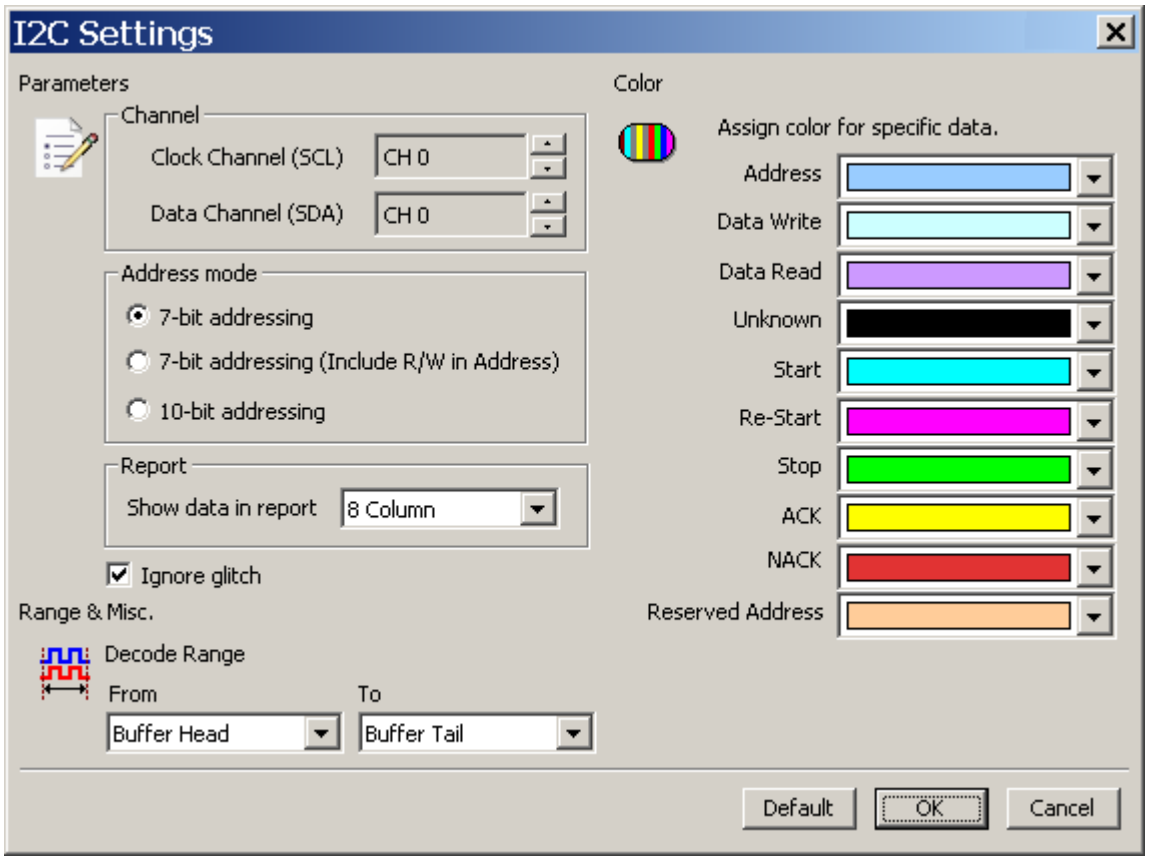
Result



I²C

The Inter-Integrated Circuit (I²C) bus has two data bits: Serial Data (SDA) and Serial Clock (SCL).

Settings



Channel: Display the channels (CH0 and CH1).

Address Mode: Select the 7-bit or 10-bit address.

7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

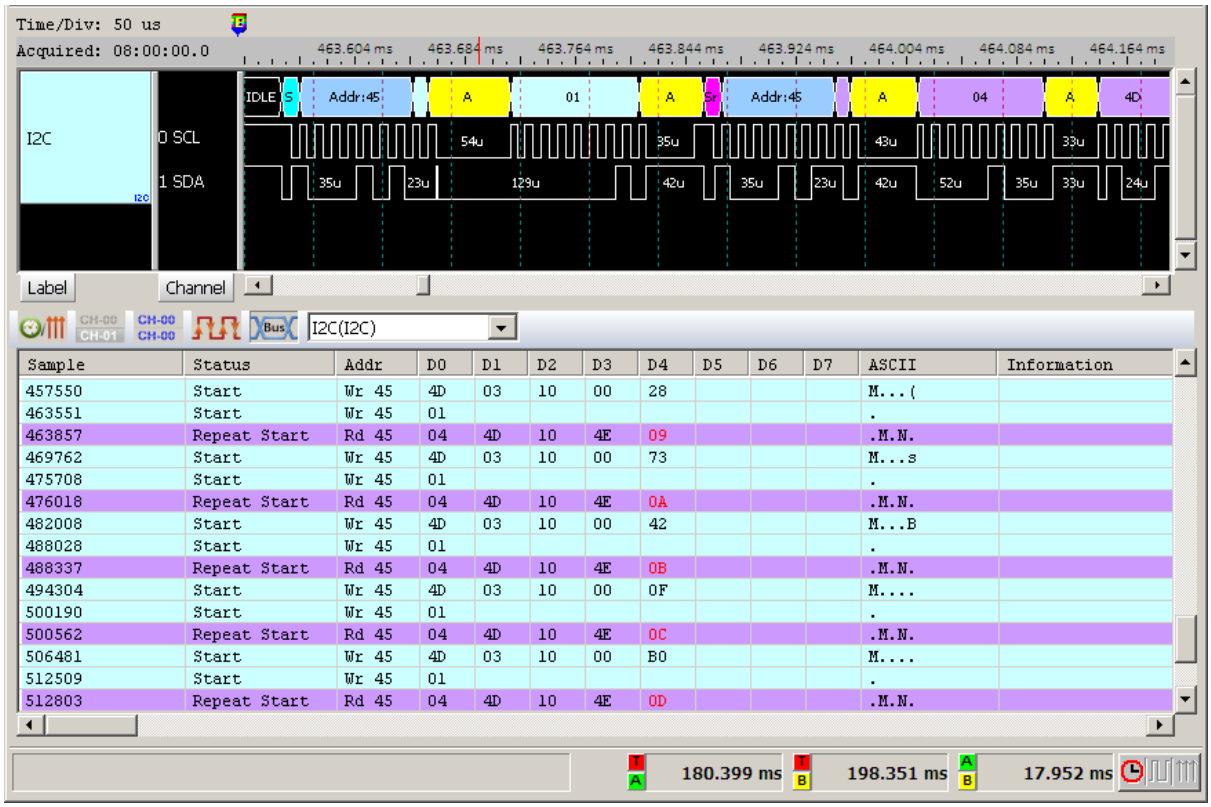
Report: Show either 8 or 16-columns data in the report window.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Result

Click **OK** to run the I^2C decode and see the result on the Waveform Window below.

It shows frequency in the Information field.

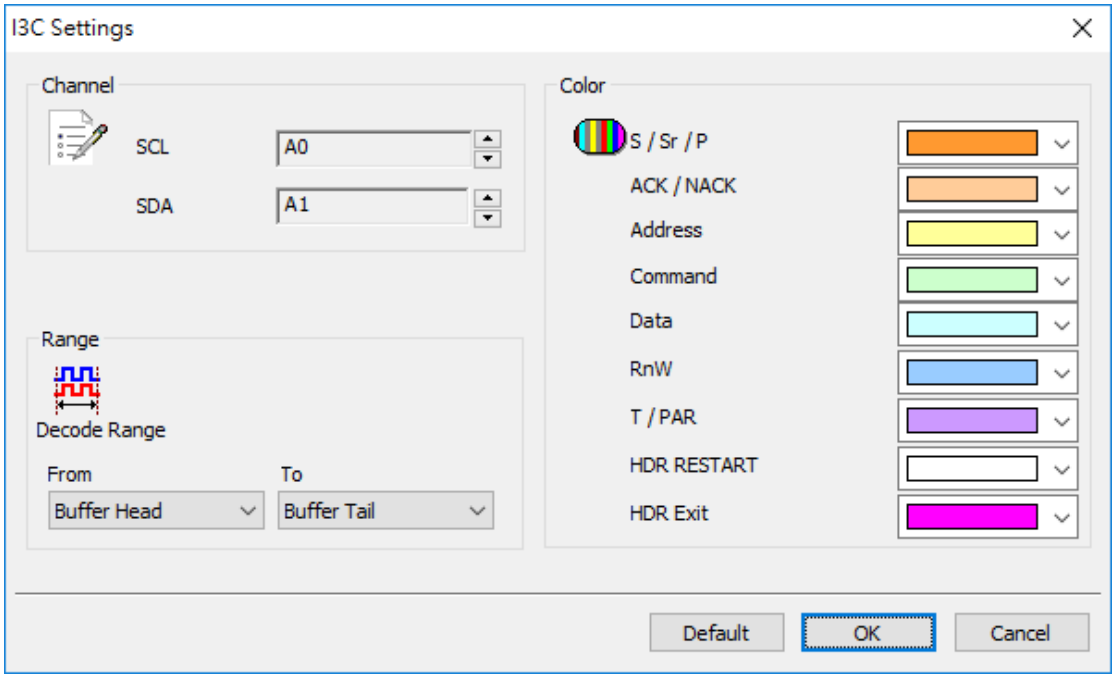


Sample	Status	Addr	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Information
457550	Start	Wr 45	4D	03	10	00	28				M...(	
463551	Start	Wr 45	01								.	
463857	Repeat Start	Rd 45	04	4D	10	4E	09				.M.N.	
469762	Start	Wr 45	4D	03	10	00	73				M...s	
475708	Start	Wr 45	01								.	
476018	Repeat Start	Rd 45	04	4D	10	4E	0A				.M.N.	
482008	Start	Wr 45	4D	03	10	00	42				M...B	
488028	Start	Wr 45	01								.	
488337	Repeat Start	Rd 45	04	4D	10	4E	0B				.M.N.	
494304	Start	Wr 45	4D	03	10	00	0F				M....	
500190	Start	Wr 45	01								.	
500562	Repeat Start	Rd 45	04	4D	10	4E	0C				.M.N.	
506481	Start	Wr 45	4D	03	10	00	B0				M....	
512509	Start	Wr 45	01								.	
512803	Repeat Start	Rd 45	04	4D	10	4E	0D				.M.N.	

I3C

I^{3}C is a bus interface for connecting sensors to an application processor. It is a core sensor integration technology that can combine multiple sensors from different vendors in a device to streamline integration and improve cost efficiencies. It gives developers unprecedented opportunity to craft innovative designs for any mobile product, from smartphones, to wearables, to safety systems in automobiles.

Settings

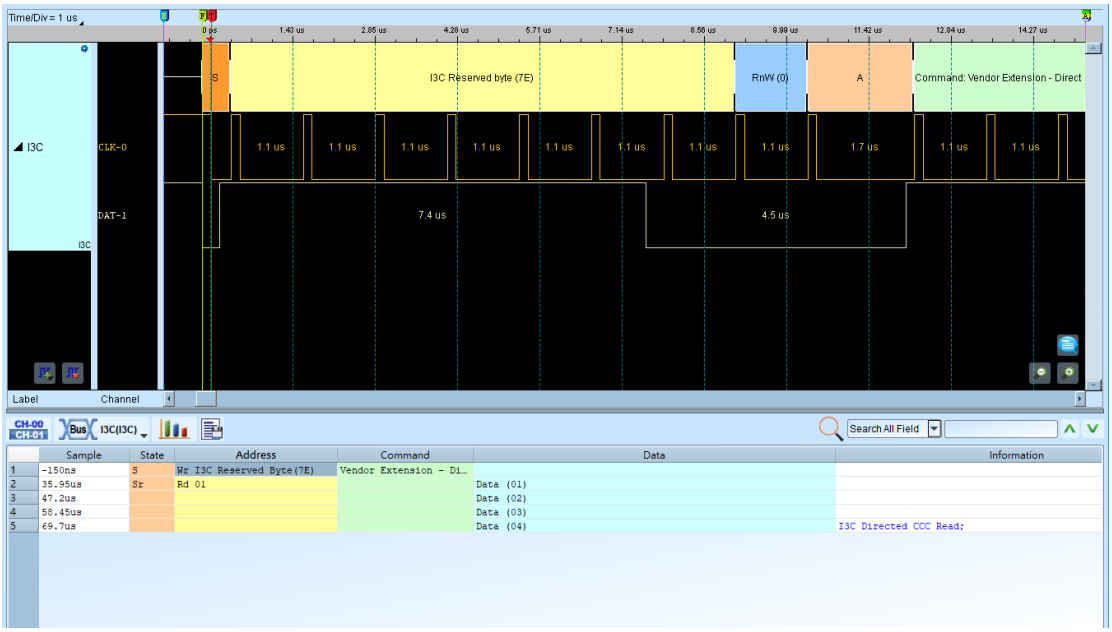


Channel: Display the channels (CH0 and CH1).

Result

Click **OK** to run the I^3C decode and see the result on the Waveform Window below.

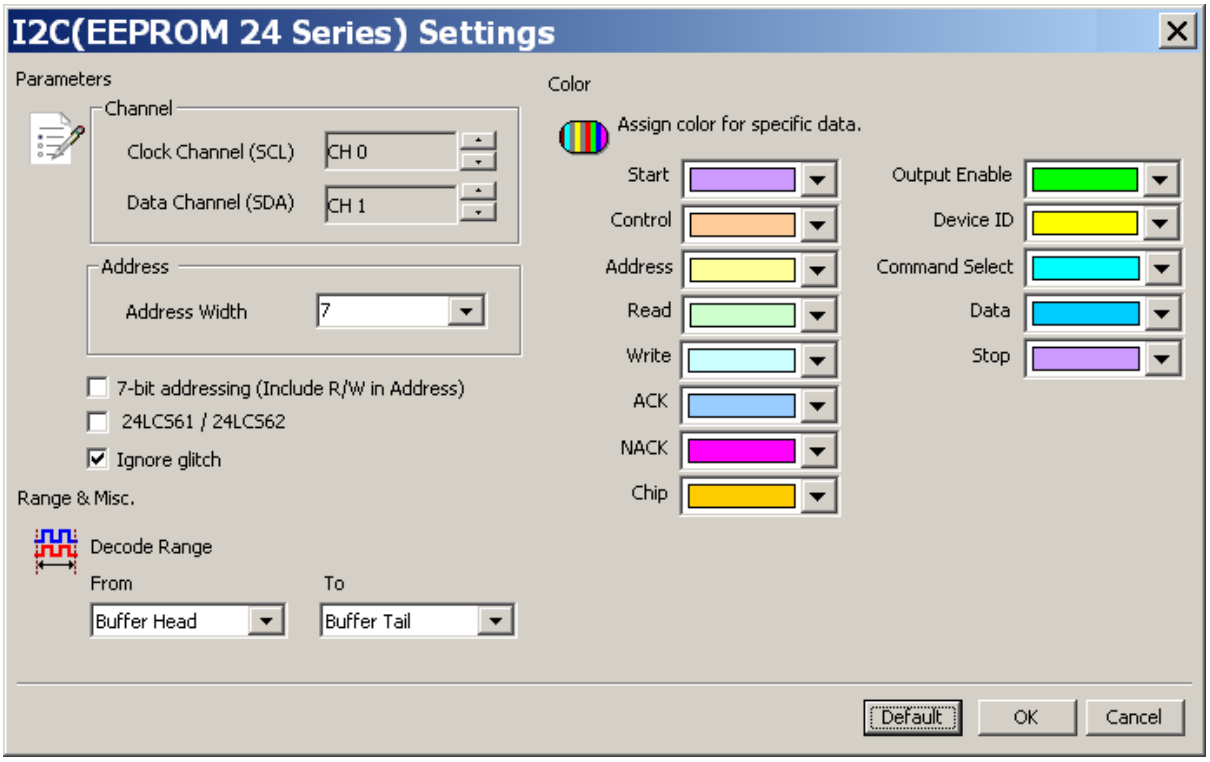
It shows frequency in the Information field.



I²C EEPROM

EEPROM can be erased and reprogrammed (written to) repeatedly through the application of higher than normal electrical voltage generated externally or internally in the case of modern EEPROMs.

Settings



Channel: Display the channels (CH0 and CH1)

Address: The default address width is 7.

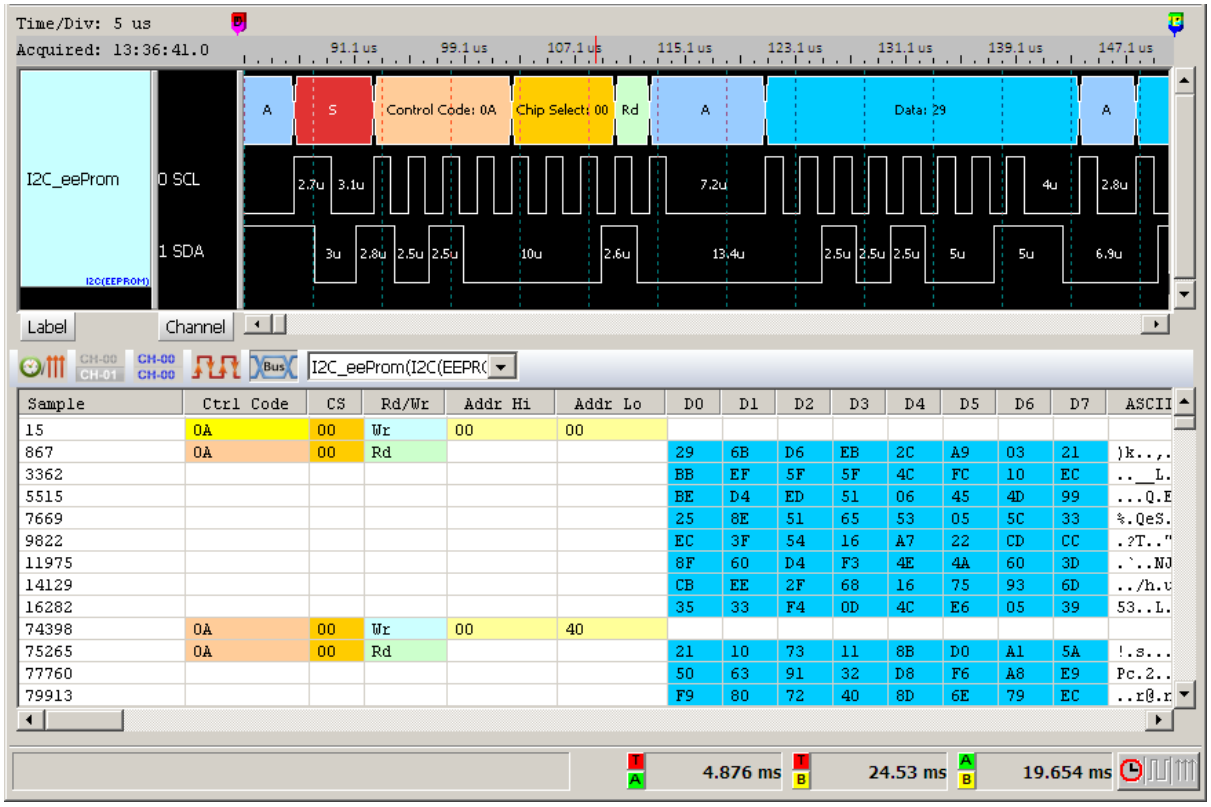
7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

24LCS61/24LCS62: 24LCS61/24LCS62 EEPROM protocol.

Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click OK to run the I²C EEPROM decode and see the result on the Waveform Window below.

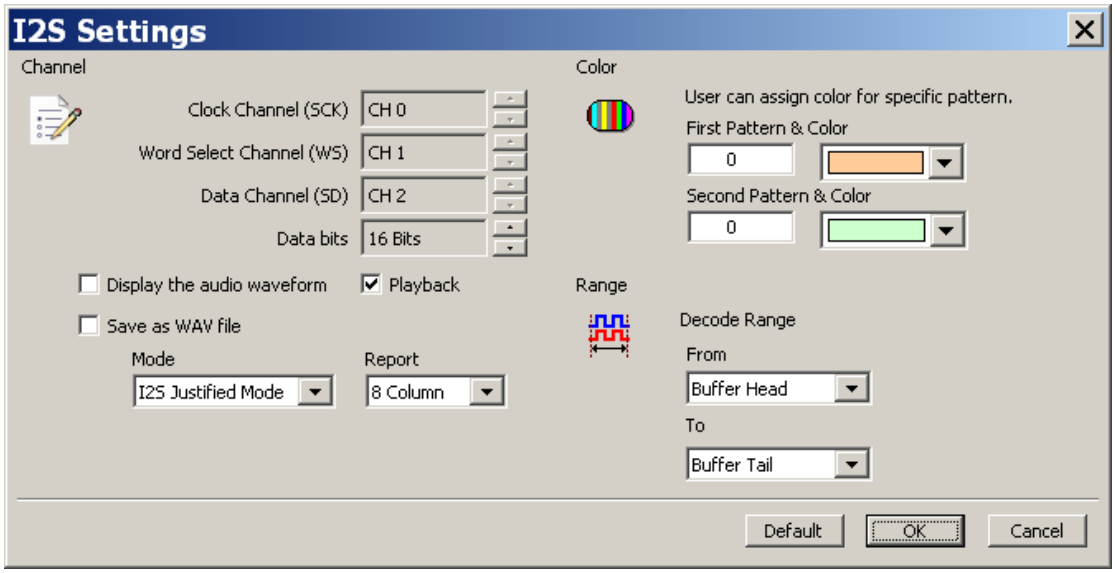


Sample	Ctrl Code	CS	Rd/Wr	Addr Hi	Addr Lo	D0	D1	D2	D3	D4	D5	D6	D7	ASCII
15	0A	00	Wr	00	00									
867	0A	00	Rd			29	6B	D6	EB	2C	A9	03	21	)k..,.
3362						BB	EF	5F	5F	4C	FC	10	EC	.._L.
5515						BE	D4	ED	51	06	45	4D	99	...Q.E
7669						25	8E	51	65	53	05	5C	33	%.QeS.
9822						EC	3F	54	16	A7	22	CD	CC	.?T.."
11975						8F	60	D4	F3	4E	4A	60	3D	.`..NJ
14129						CB	EE	2F	68	16	75	93	6D	../h.u
16282						35	33	F4	0D	4C	E6	05	39	53..L.
74398	0A	00	Wr	00	40									
75265	0A	00	Rd			21	10	73	11	8B	D0	A1	5A	!.s...
77760						50	63	91	32	D8	F6	A8	E9	Pc.2..
79913						F9	80	72	40	8D	6E	79	EC	..r@.r

I^2S

The Inter-Integrated Circuit Sound (I2S) bus has three data bits: Serial Clock (SCK), Word Select Line (WS) and Multiplex Data Line (SD).

Settings



Channel: Show the selected channels (CH0, CH1 and CH2) and set Data bits (16 bits).

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

Playback: Click to display the audio from the speaker..

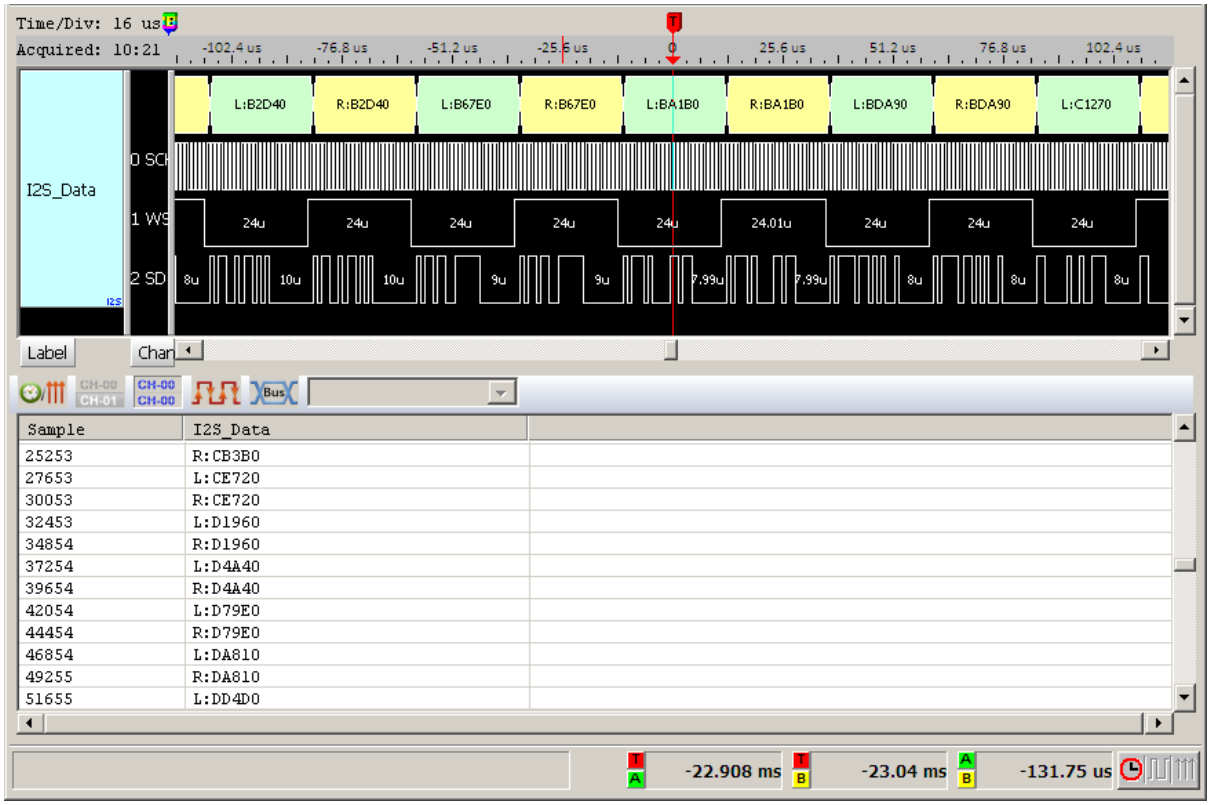
Save as WAV file: Click to save the data to a audio file(.wav) in the work directory.

Mode: I^2S Justified/MSB Justified/LSB Justified/PCM/TDM.

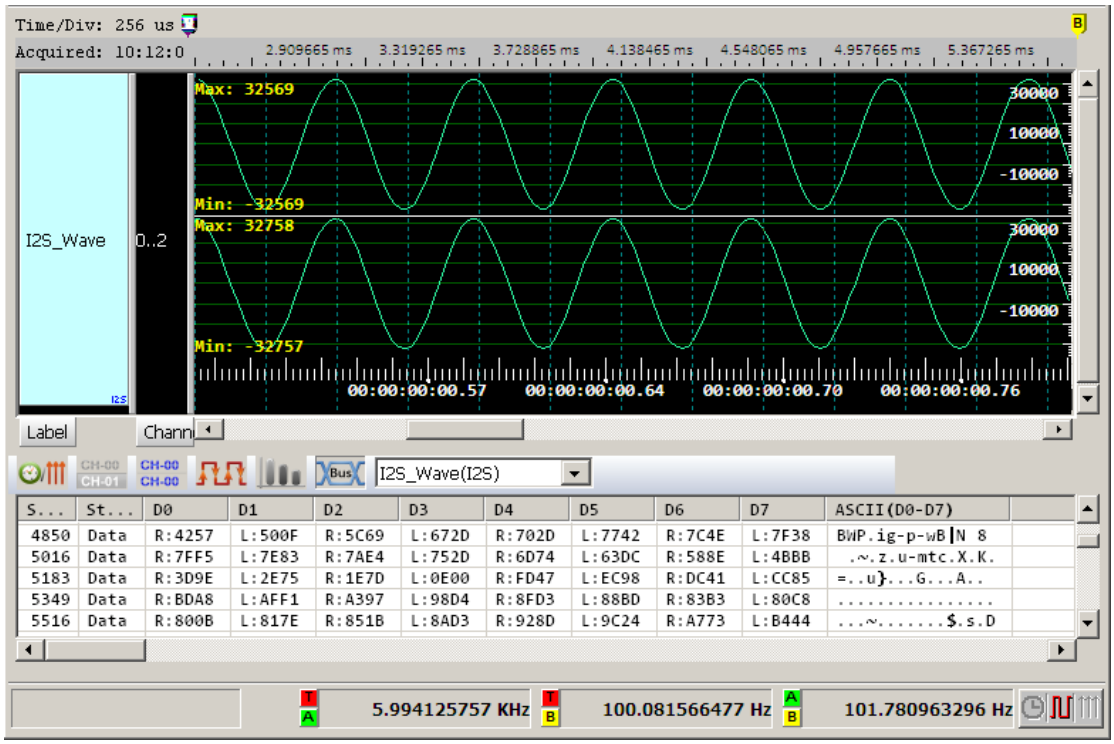
Report: Select the column number.

Result

Click **OK** to run I^2S decode and see the result on the Waveform Window below.



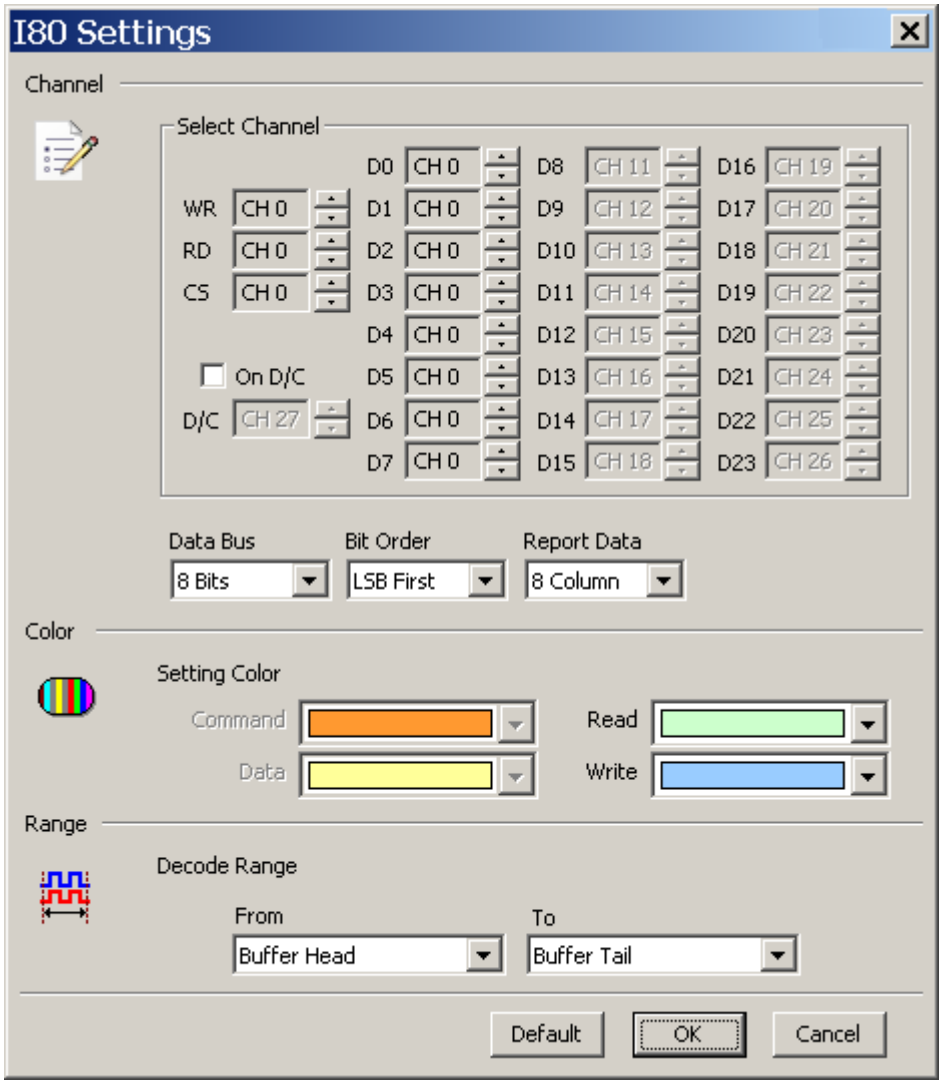
Display the audio waveform



I80

The I80 controls 3 or 4-pins (WR, RD, CS, D/C) data.

Settings



Select Channel: Show the selected channels (WR, RD, CS, D0, D1, D2, D3, D4, D5, D6,…).

On D/C: Use the D/C pin as Command (Low) or Data (High).

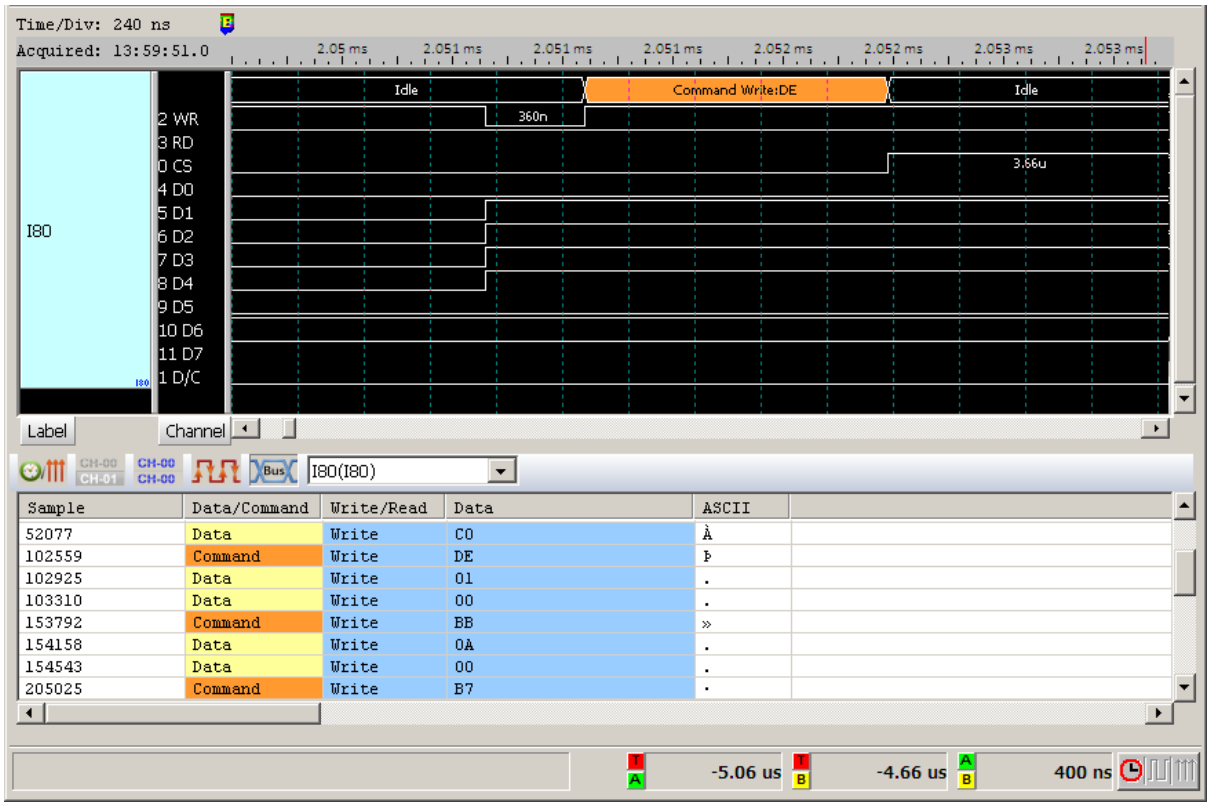
Data Bus: Select 4 Bit, 8 Bit, 12 Bit, 16 Bit, 20 Bit, or 24 Bit.

Bit Order: Select LSB First or MSB First.

Report Data: Select 8 columns or 16 columns.

Result

Click **OK** to run the I80 decode and see the result on the Waveform Window below.



IDE

IDE (Integrated Device Electronics) is a computer hardware bus and has the following data bits:

General Channel (11 pins): DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP, DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-, RESET-, CSEL, IOCS16-.

Register Channel (5 pins): CS(0:1)-, DA(2:0).

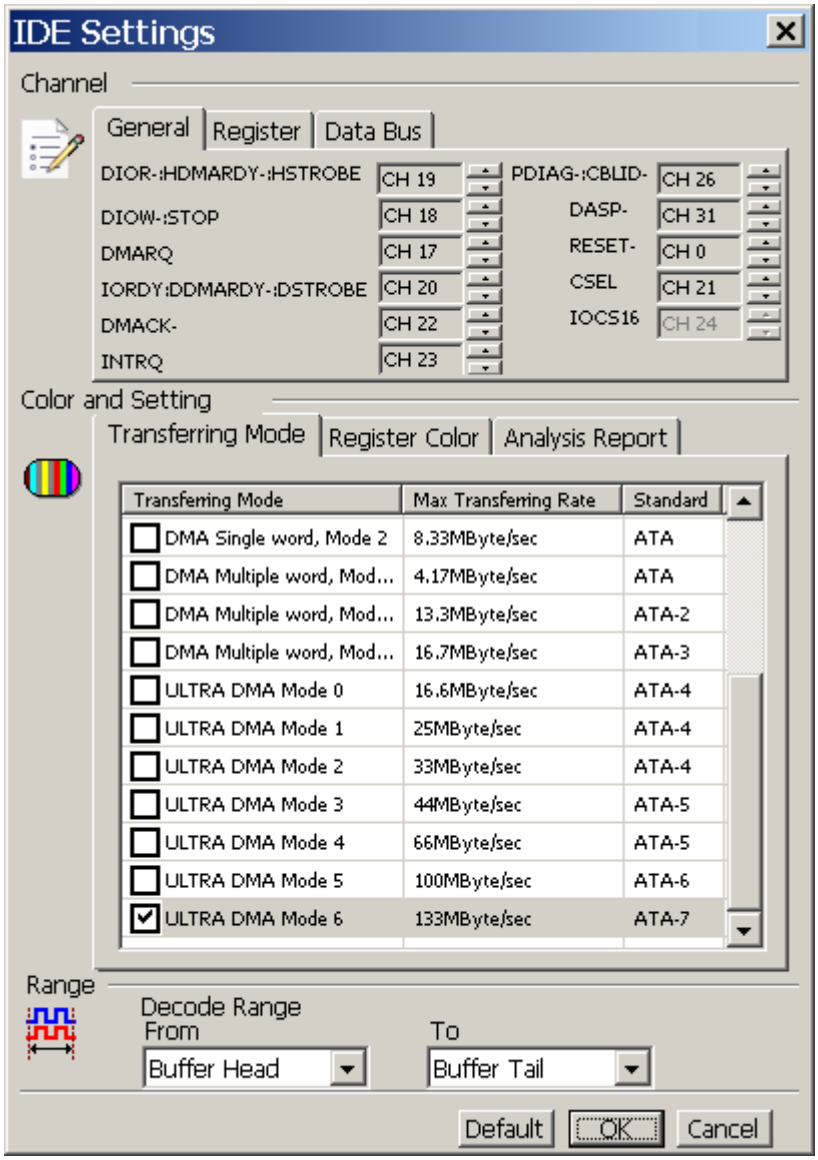
Data Bus (16 pins): DD(15:0)

We recommend that IDE bus of the target system to be connected to the instrument as the following table:

IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4
Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14

Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25	DIOR-:HDMARDY-:HSTROBE	Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMARDY-:DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24
Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		

Settings



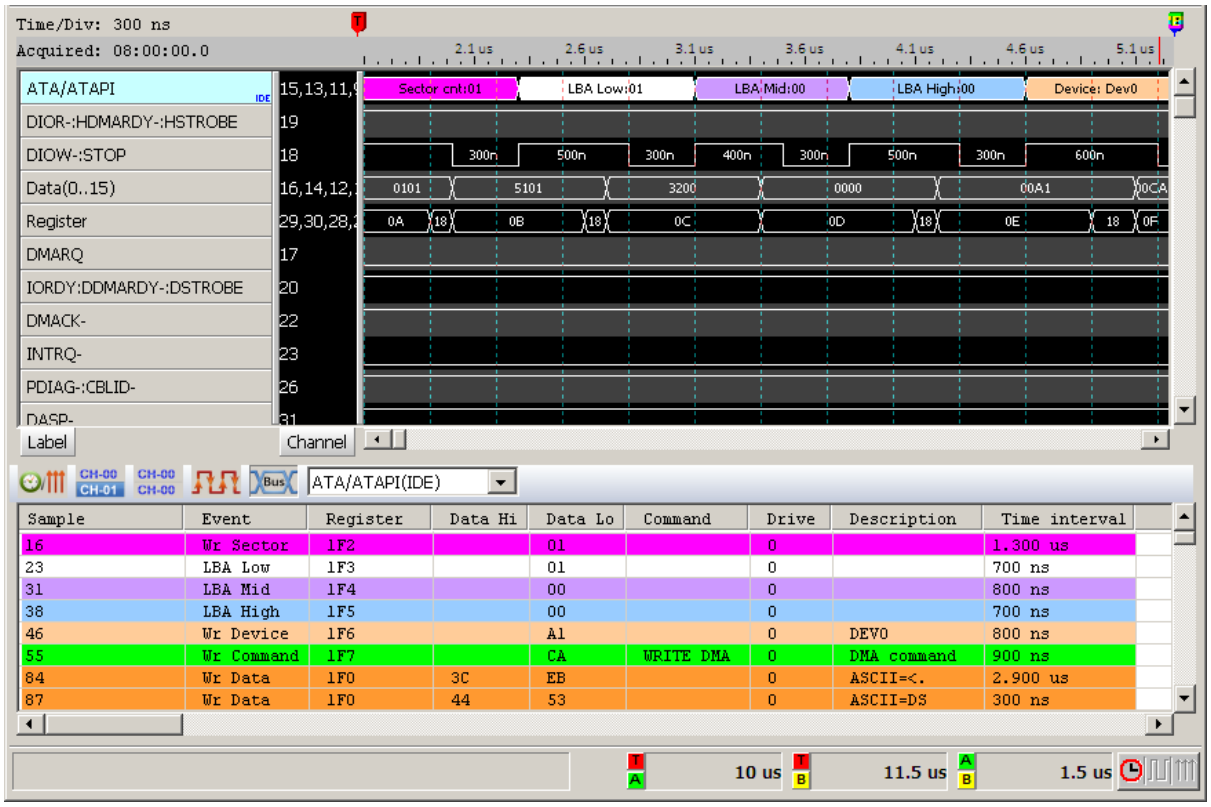
Channel: Set channel number for General, Register, and Data Bus.

Transferring Mode: Select the target system.

Analysis Report: Filter the data in the Report Window.

Result

Click **OK** to run the IDE decode and see the result on the Waveform Window below.

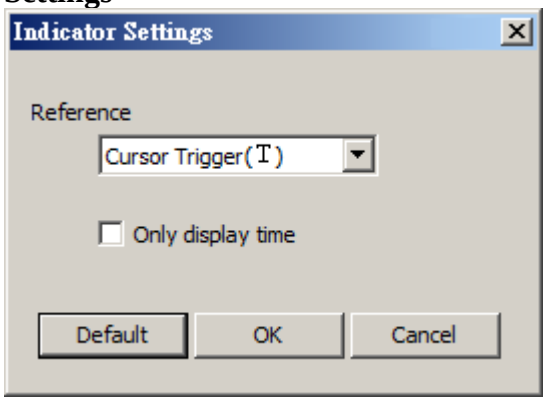


Sample	Event	Register	Data Hi	Data Lo	Command	Drive	Description	Time interval
16	Wr Sector	1F2		01		0		1.300 us
23	LBA Low	1F3		01		0		700 ns
31	LBA Mid	1F4		00		0		800 ns
38	LBA High	1F5		00		0		700 ns
46	Wr Device	1F6		A1		0	DEV0	800 ns
55	Wr Command	1F7		CA	WRITE DMA	0	DMA command	900 ns
84	Wr Data	1F0	3C	EB		0	ASCII=<.	2.900 us
87	Wr Data	1F0	44	53		0	ASCII=DS	300 ns

Indicator

Indicator is to display with the time or clock samples on the Waveform window to be helpful to read the waveform.

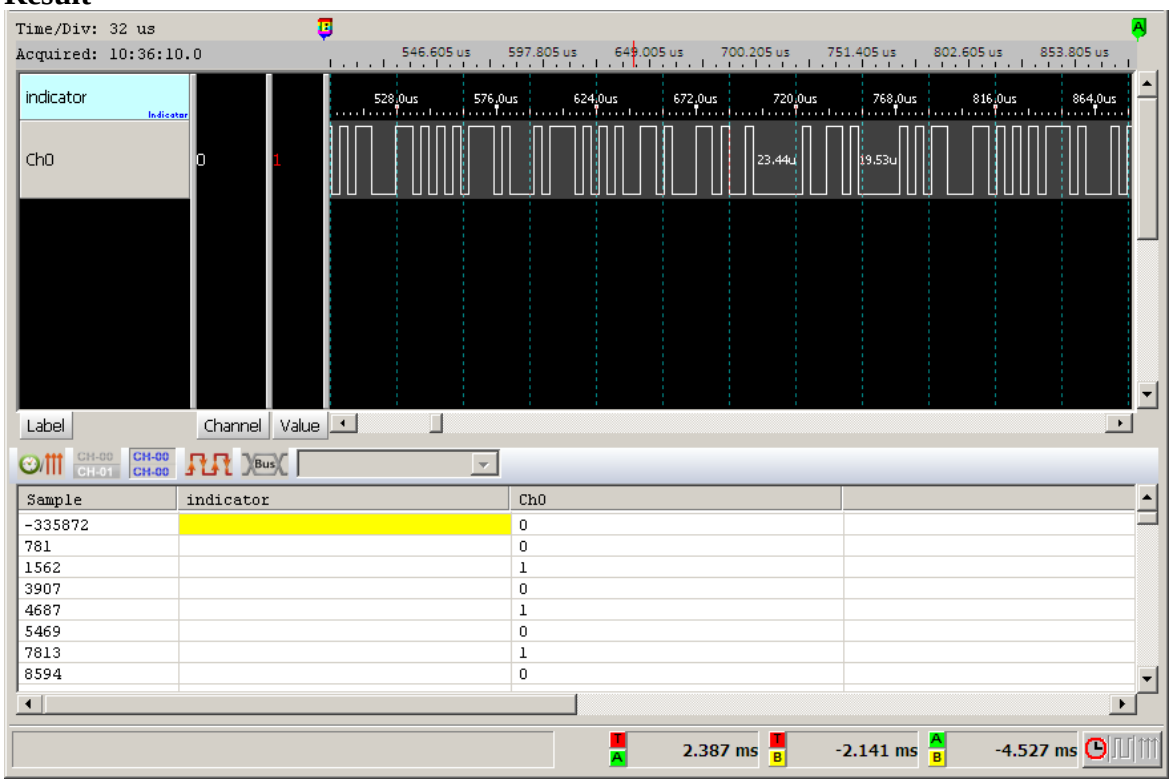
Settings



Reference: Set the reference position (Trigger cursor), time value on the right (left) is positive (negative). Default reference position is the trigger cursor and also shows time or sample rate.

Only display time: to show time only.

Result

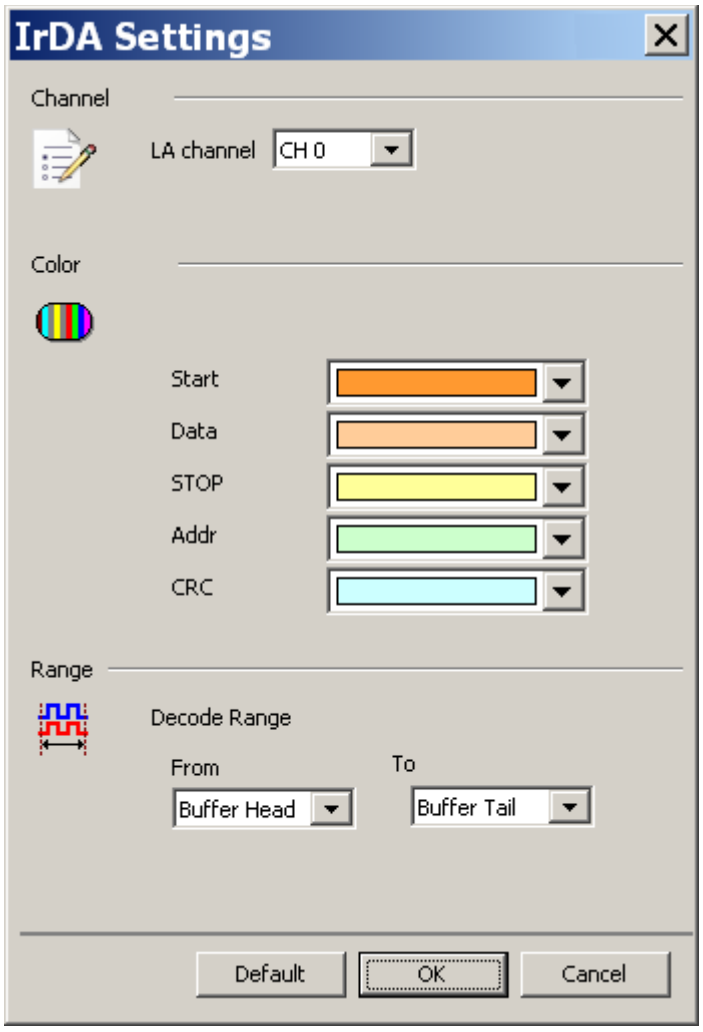


Add two Indicators for two channels with two different cursors as the references to display the result on the Waveform Window below.

IrDA

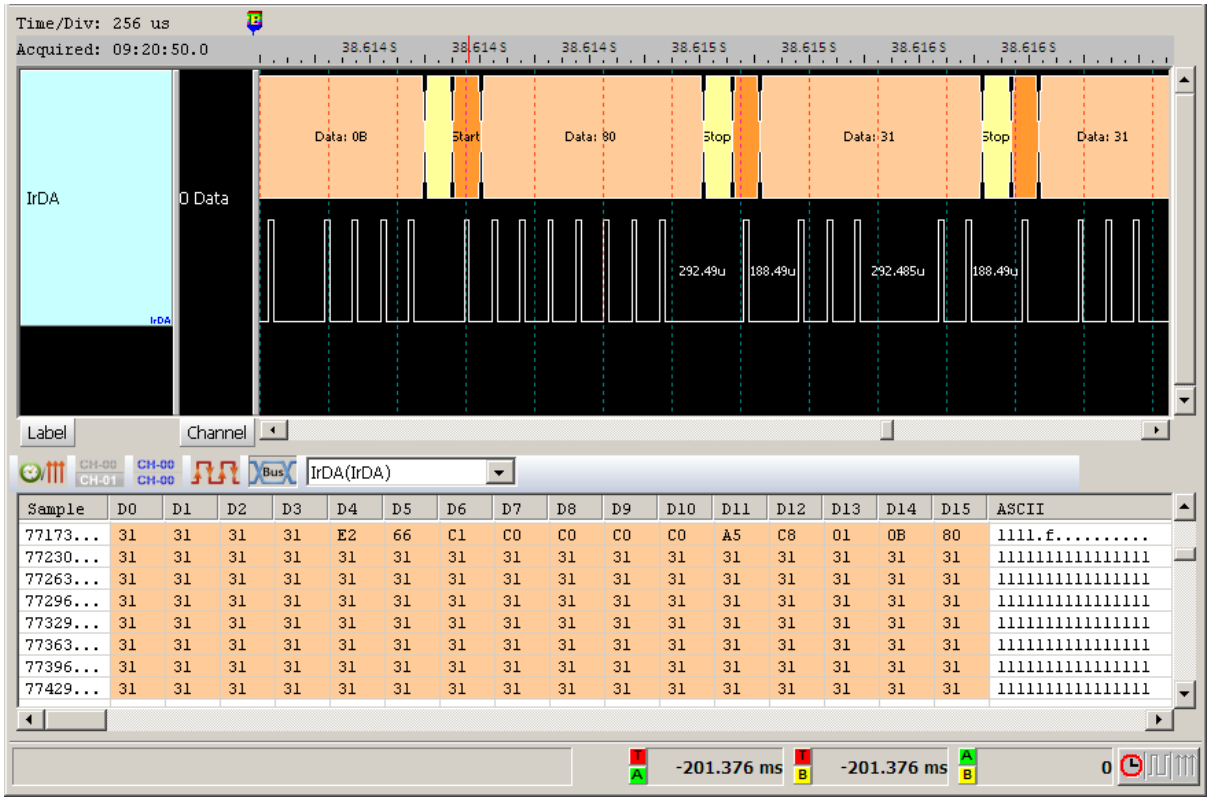
The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

Settings



Channel: Show the selected channel.

Result

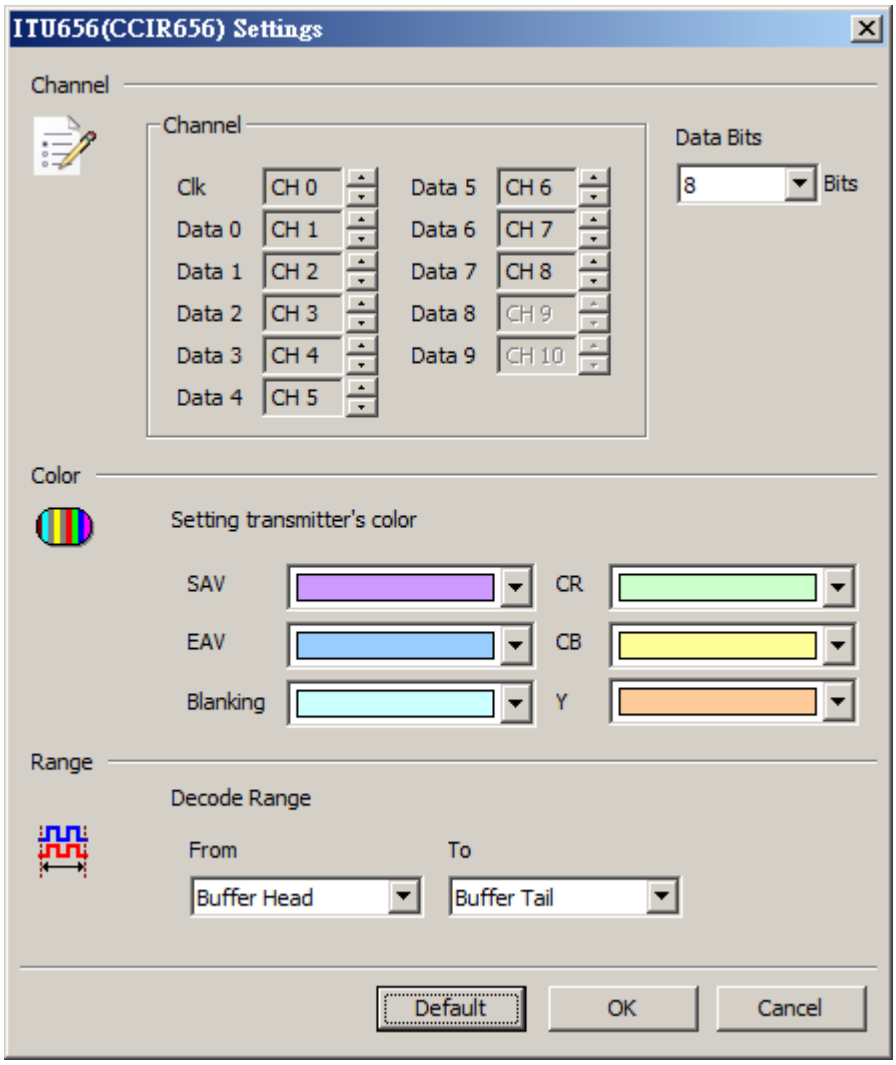


Sample	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	ASCII
77173...	31	31	31	31	E2	66	C1	C0	C0	C0	C0	A5	C8	01	0B	80	llll.f.....
77230...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll
77263...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll
77296...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll
77329...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll
77363...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll
77396...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll
77429...	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	31	lllllllllllllll

ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

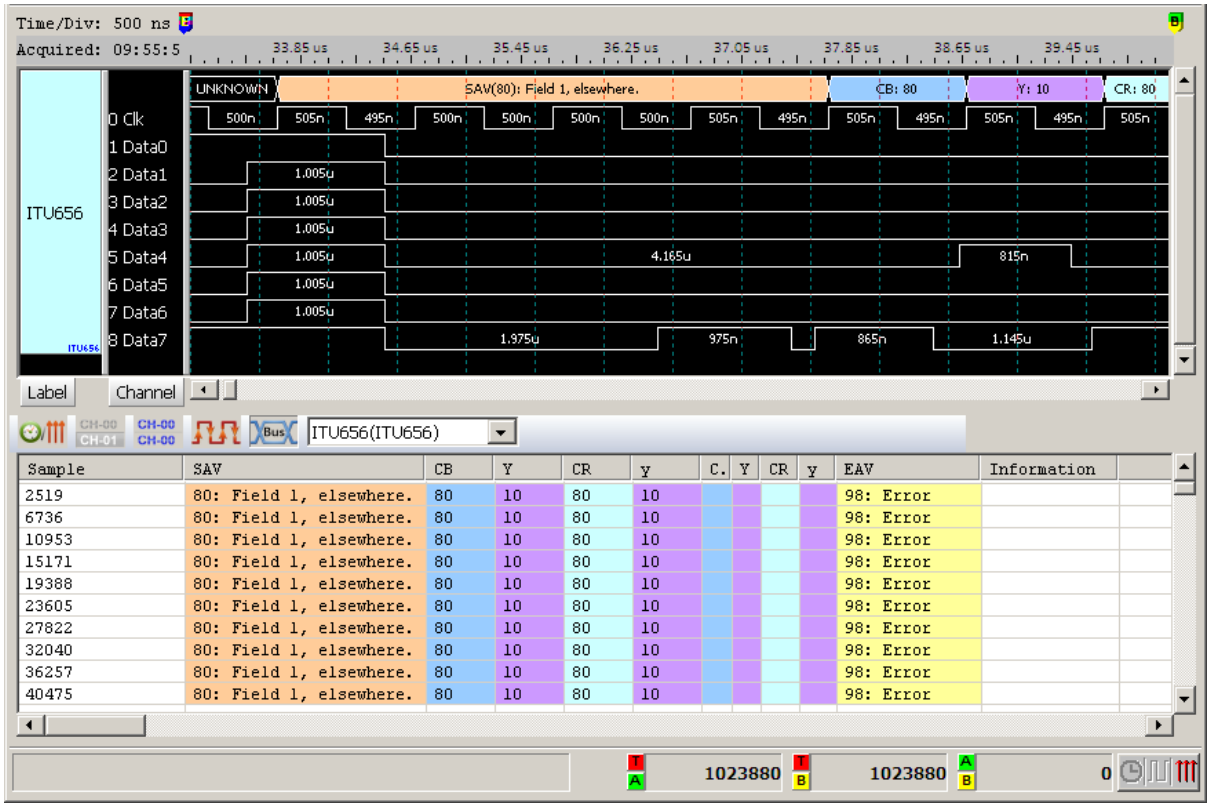
Settings



Channel: Show the selected channel (Clk, Data 0 – Data 9).

Data Bits: Show the number of data bits.

Result



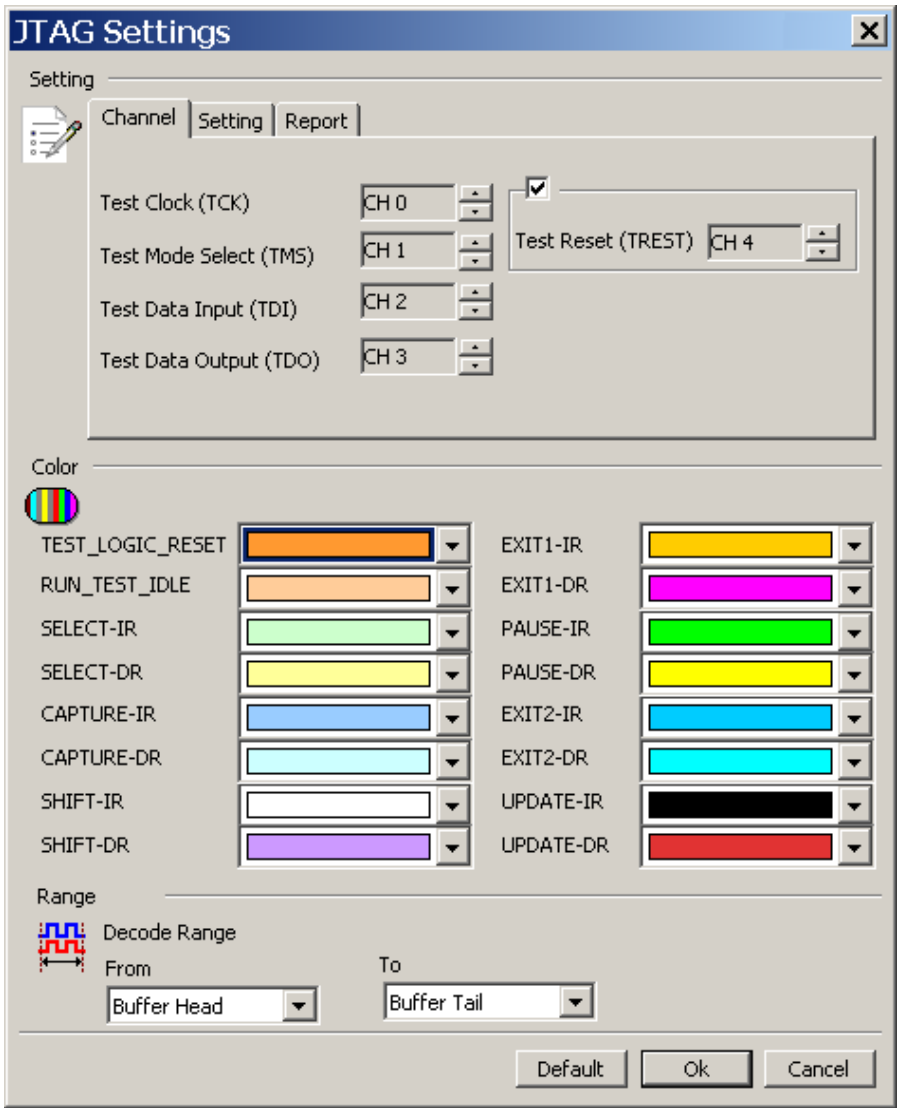
Sample	SAV	CB	Y	CR	y	C.	Y	CR	y	EAV	Information
2519	80: Field 1, elsewhere.	80	10	80	10					98: Error	
6736	80: Field 1, elsewhere.	80	10	80	10					98: Error	
10953	80: Field 1, elsewhere.	80	10	80	10					98: Error	
15171	80: Field 1, elsewhere.	80	10	80	10					98: Error	
19388	80: Field 1, elsewhere.	80	10	80	10					98: Error	
23605	80: Field 1, elsewhere.	80	10	80	10					98: Error	
27822	80: Field 1, elsewhere.	80	10	80	10					98: Error	
32040	80: Field 1, elsewhere.	80	10	80	10					98: Error	
36257	80: Field 1, elsewhere.	80	10	80	10					98: Error	
40475	80: Field 1, elsewhere.	80	10	80	10					98: Error	

JTAG

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan.

A JTAG interface is a special four/five-pins interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met, and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board.

Settings

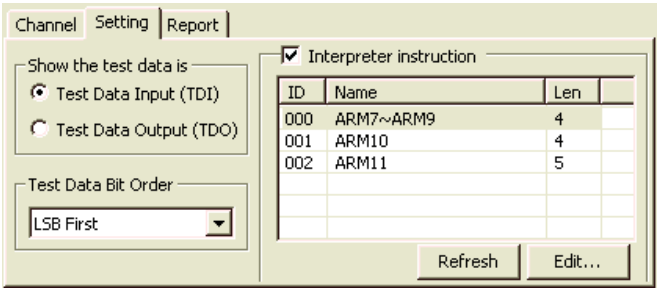


Settings: Includes Channel, Setting, and Report.

Channel: Set the channel number.

Show the test data is: The data is TDI or TDO.

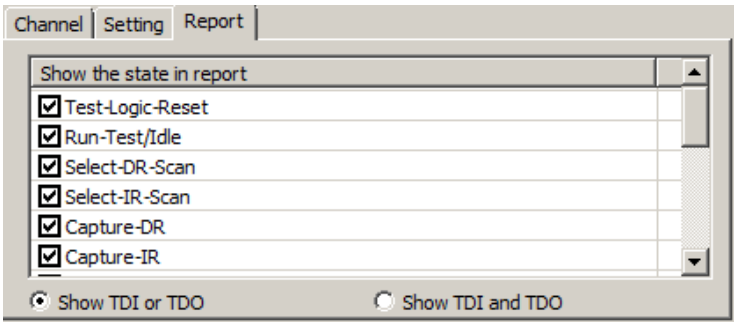
Test Data Bit Order: LSB First or MSB First.



Interpreter instruction: Check the Interpreter Instruction and you will see a list of commands. The JTAG decode will display its updated commands in the Instruction Register, which is the temporary memory buffer for the commands. Click Edit to edit the commands in the Interpreter Instructions; then click Refresh to update the commands in the Interpreter Instructions.

Acute JTAG Instruction table (JtagInst.txt): This file is supported by the JTAG DLL and can be modified if needed. The JTAG Decode also supports the BSDL format. You can load the BSDL file in order to save time on editing commands. If you are interested in more details, please refer to the Acute JTAG Instruction table Syntax Description in the end of the JTAG Decode chapter.

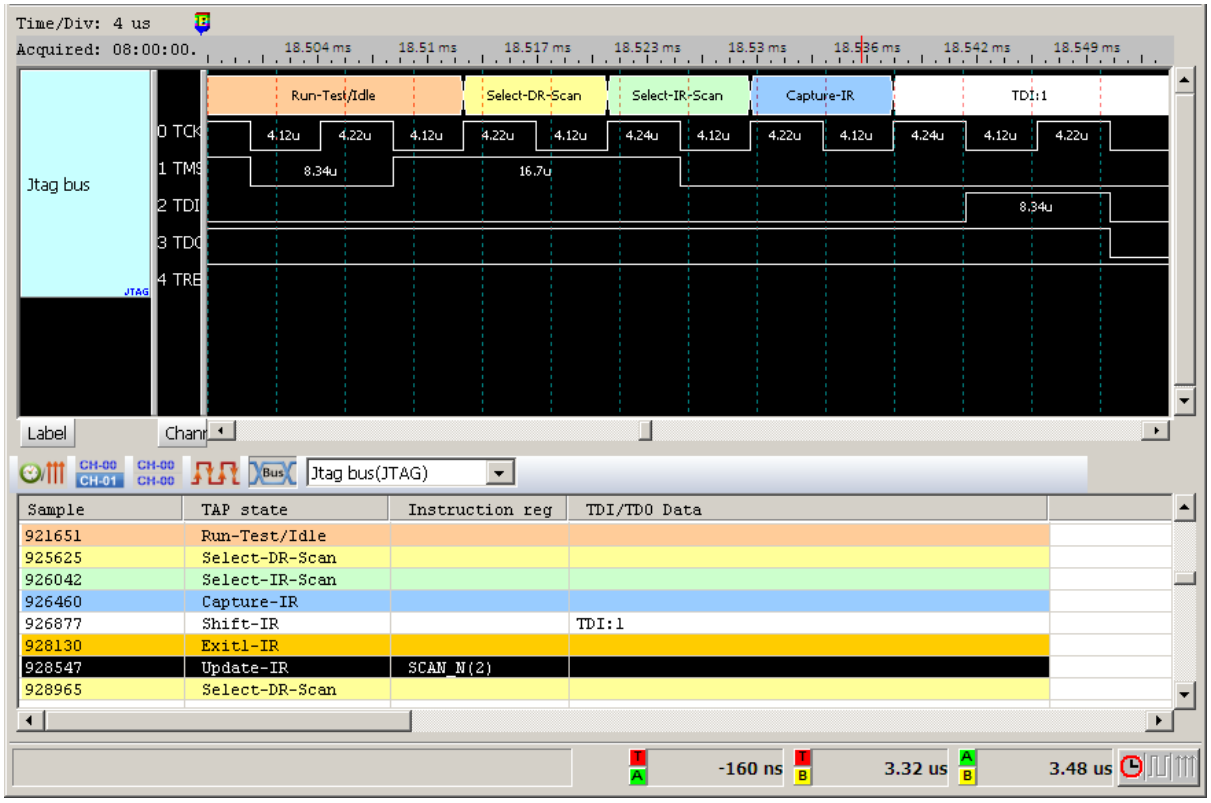
Report: You can filter the data you want to see on the Report Window.



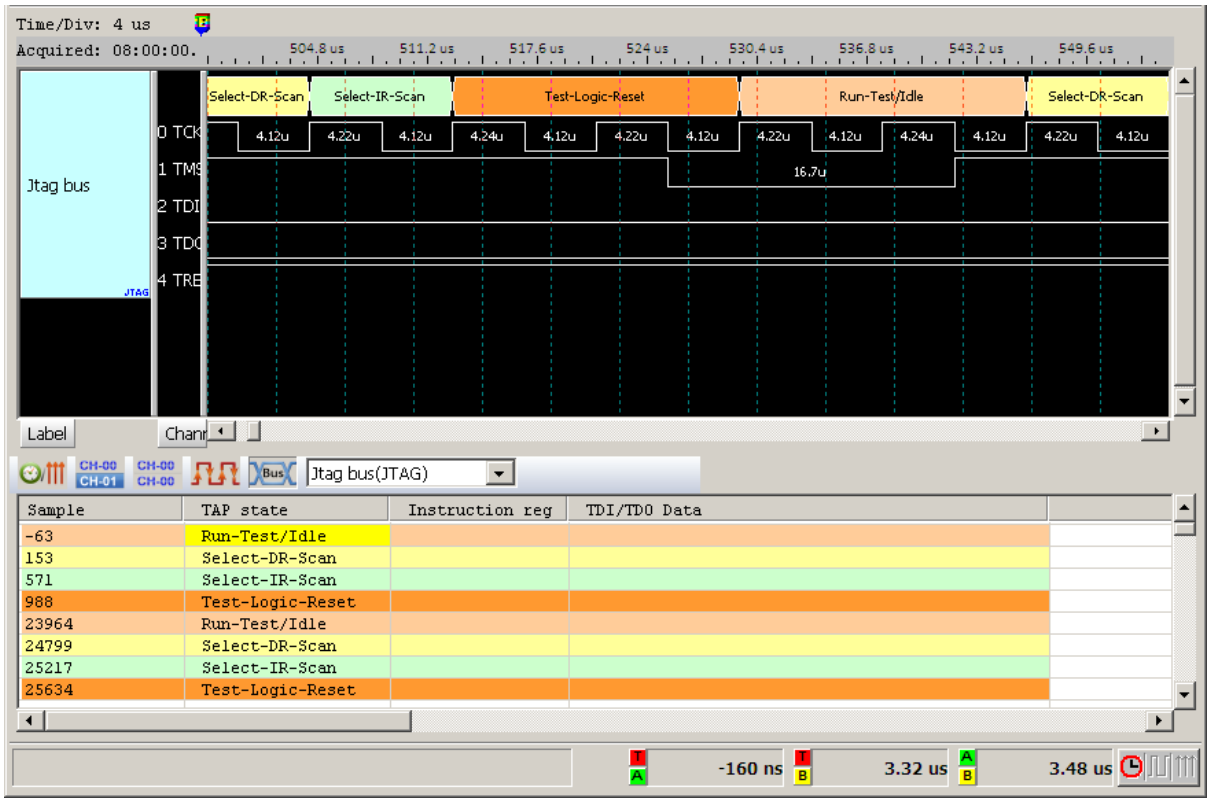
Show TDI or/and TDO

Result

The Altera EPM3256AT144 Programming Schematic JTAG decode on the Waveform Window



The ARM7 Read IDCODE JTAG decode on the Waveform Window



Acute JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

#ID: Command list number; the range is 00 - FF and , MUST be entered in order or will be seen as the end of commands.

#NAME: Command Name, 32 bytes most will be shown in the command list.

#LENGTH: Command length, unit in bits.

#CAPTURE: Command Capture Code, is stored in Instruction Register..

#INST: Command List, listed by Command Code and Command Name or will be seen as the end of commands..

#TRST: Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

#BSDL: Load the BSDL file. Use the BSDL file as step 1-6.

Example:#ID:00

#NAME:ARM7-ARM9

#LENGTH:4

#CAPTURE:1

#INST:0, EXTEST

#INST:2, SCAN_N

#INST:3, SAMPLE/PRELOAD

#INST:4, RESTART

#INST:5, CLAMP

#INST:7, HIGHZ

#INST:9, CLAMPZ

#INST:C, INTEST

#INST:E, IDCODE

#INST:F, BYPASS

#INST:

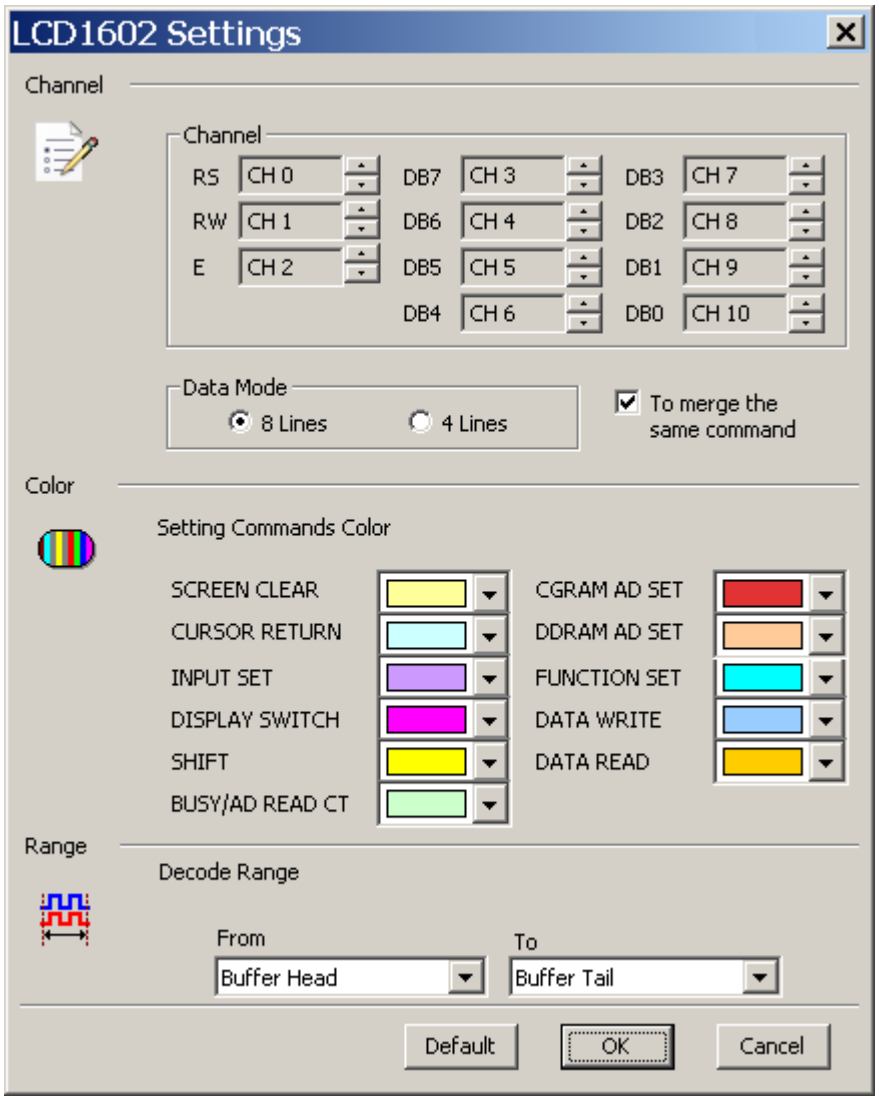
#ID:01

#BSDL:C:\3256at144_1532.bsd

LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits: Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select (E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

Settings



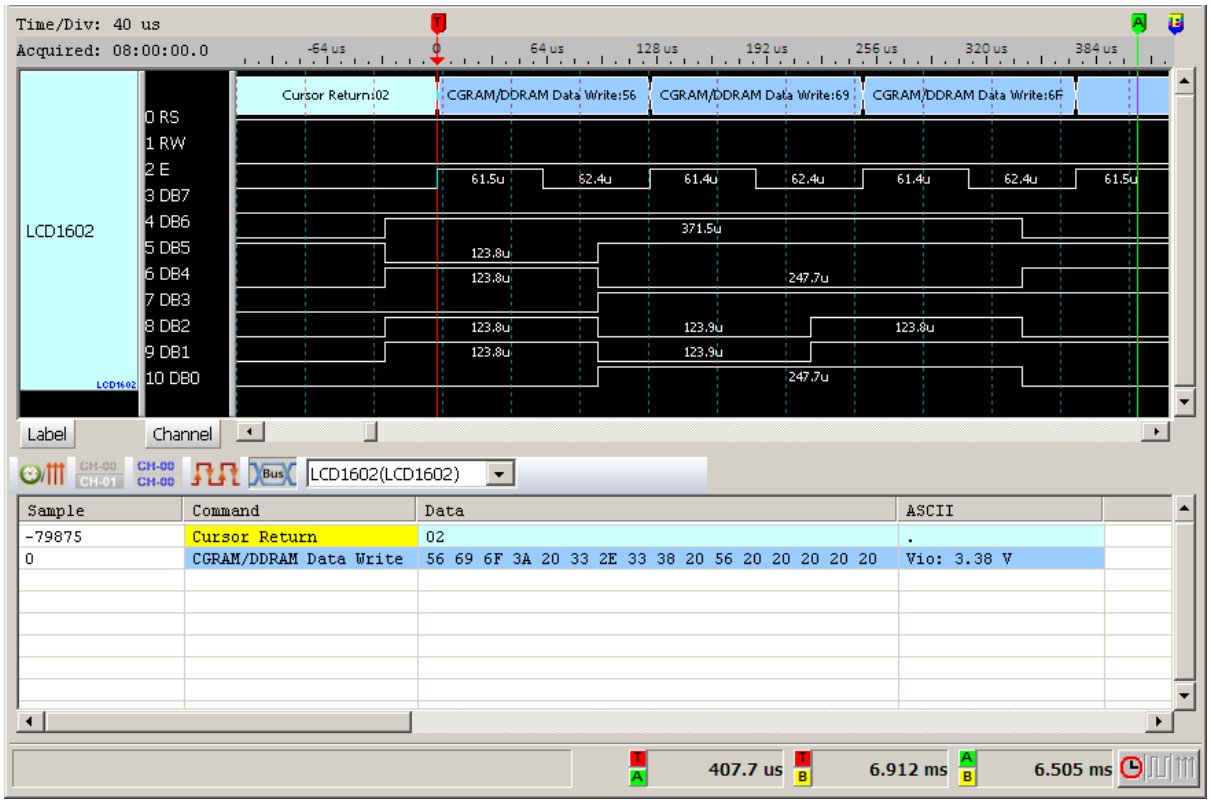
Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.

To merge the same command: Merge data with its command.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window below.



LIN

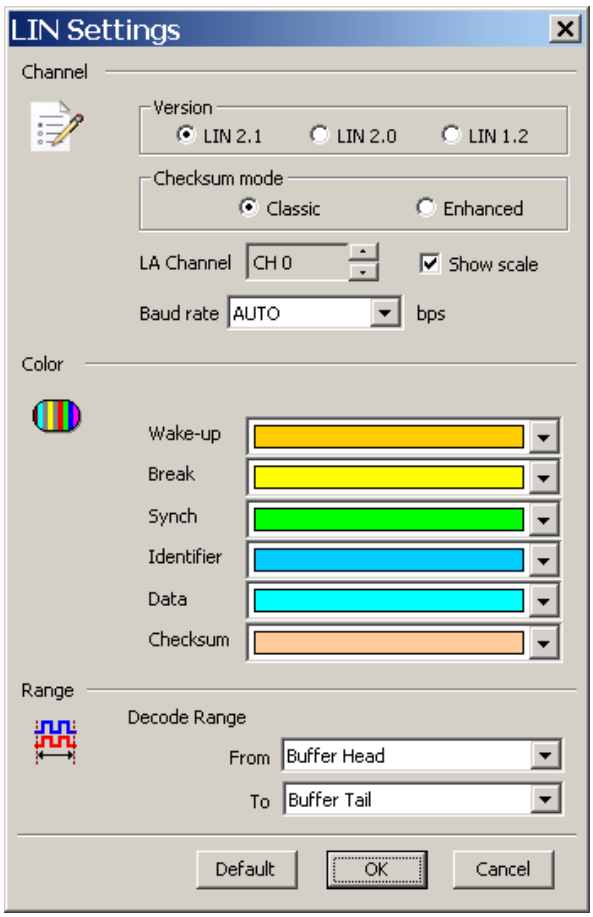
The Local Interconnect Network (LIN) bus (version 2.1) has two message types: Header and Response.

(1) Header contains three data frames: Synchronization Break (Break), Synchronization Field (Sync) and Identifier Field (Identifier).

(2) Response contains two data frames: Data Field (Data) and Checksum Field (Checksum). Checksum contains data and identifier (Enhanced mode), but version 1.3 or below (Classic mode) contains data only.

LIN bus has two states - Sleep mode and Active mode. While data is on the bus, all LIN nodes are in active state; but after a specified timeout, the nodes enter Sleep mode and will be released back to active state by a WAKEUP frame.

Settings



Version: Select LIN version.

Checksum Mode: Select Classic: data only or Enhanced: data and identifier.

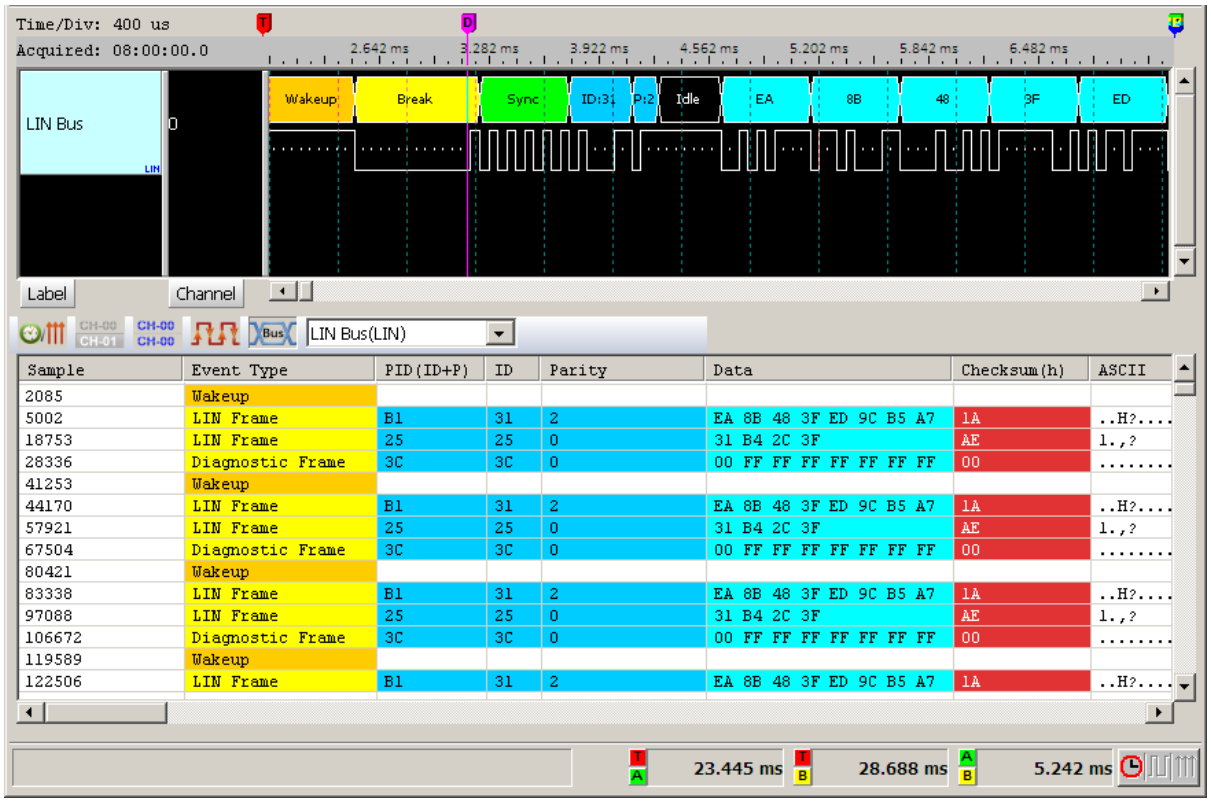
LA Channel: Show the selected channel (CH0 for LIN).

Show Scale: Show scale on the waveform.

Baud rate: Show the selected baud rate.

Result

Click **OK** to run the Lin decode and see the result on the Waveform Window below.



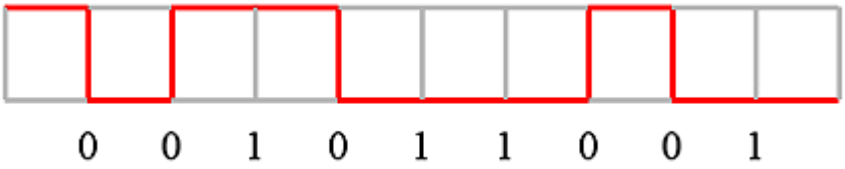
Sample	Event Type	PID(ID+P)	ID	Parity	Data	Checksum(h)	ASCII
2085	Wakeup						
5002	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	..H?....
18753	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?
28336	Diagnostic Frame	3C	3C	0	00 FF FF FF FF FF FF FF	00	....
41253	Wakeup						
44170	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	..H?....
57921	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?
67504	Diagnostic Frame	3C	3C	0	00 FF FF FF FF FF FF FF	00	....
80421	Wakeup						
83338	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	..H?....
97088	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?
106672	Diagnostic Frame	3C	3C	0	00 FF FF FF FF FF FF FF	00	....
119589	Wakeup						
122506	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	..H?....

Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

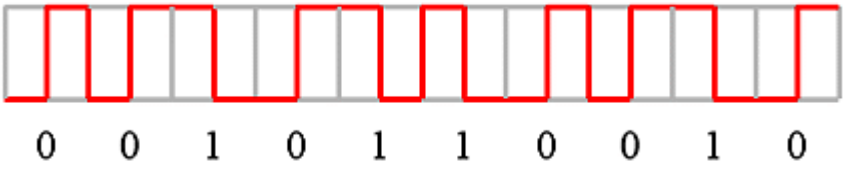
NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.

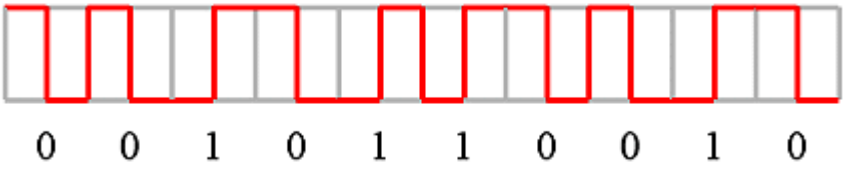


Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

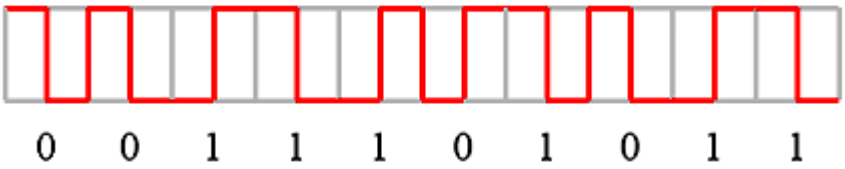
Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.

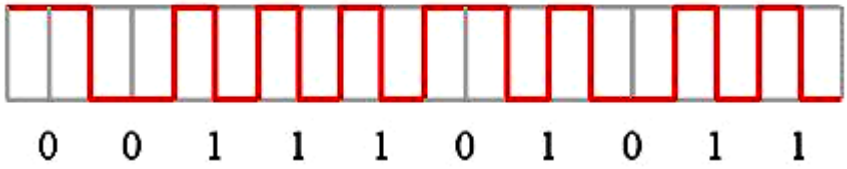


Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult. When

encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.

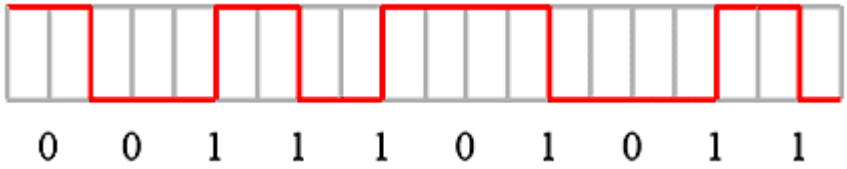


Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

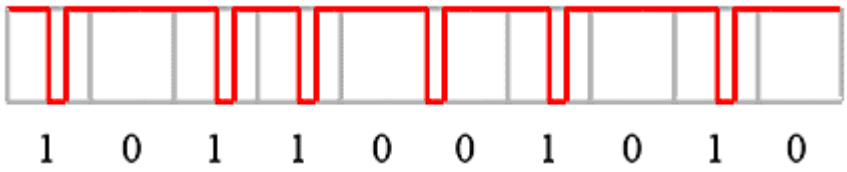
Delay encoding is used primarily for encoding radio signals because

the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.

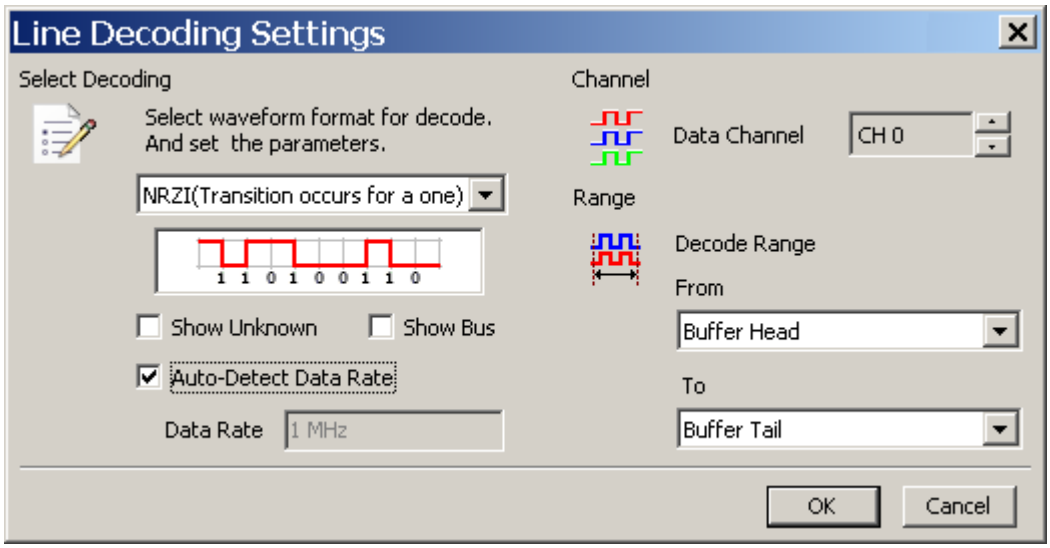


Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits

and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Decoding: Select the line code you want to decode.

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate is not selected.

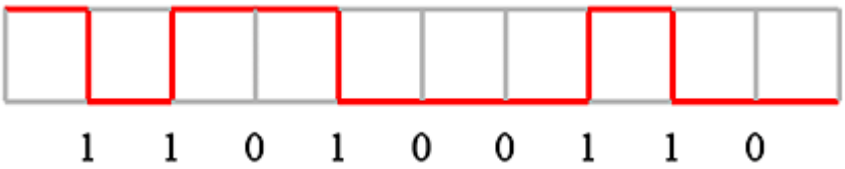
Channel: Show the selected channel (CH 0).

Range: Select the range within the waveform you want to decode.

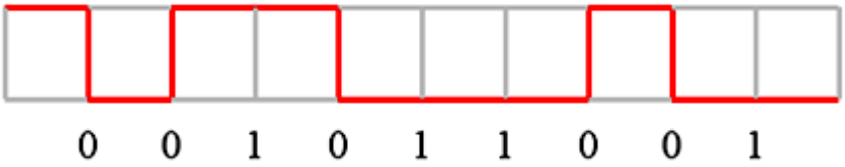
Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

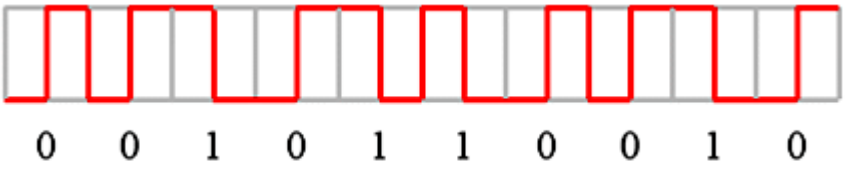


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.

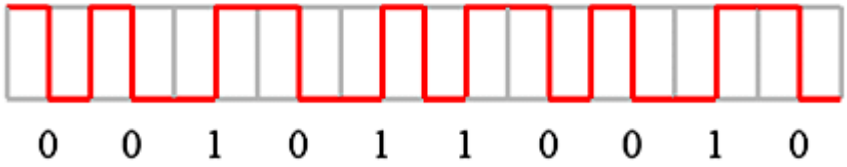


Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



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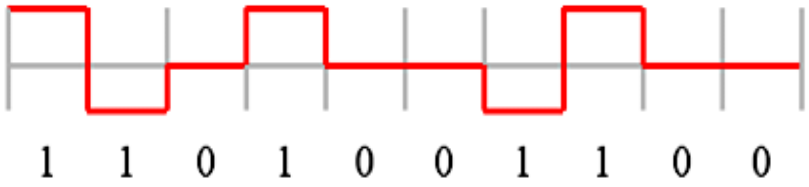
AMI (Alternate Mark Inversion): There are four modes:

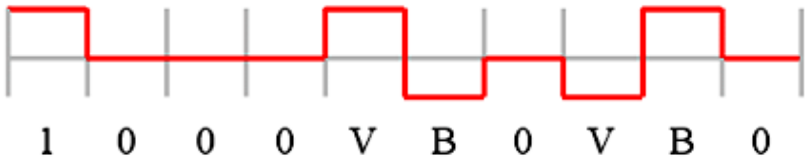
AMI (Standard): AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.



AMI (B8ZS): Bipolar-8-Zero Substitution

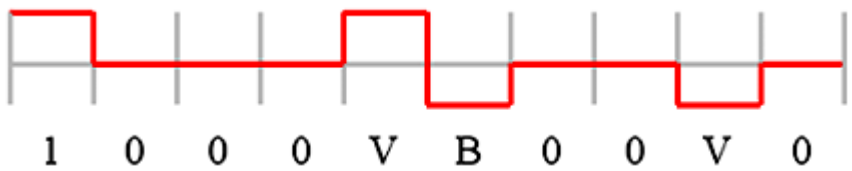
If 1 is +, 00000000 is represented to 000+-0-+

1 is -, 00000000 is represented to 000-+0+-



AMI (HDB3): High Density Bipolar 3

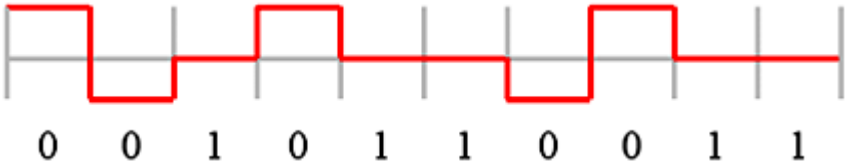
The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.



MLT-3: Multilevel Transmission 3: A 0 means no transition happens, a 1 is

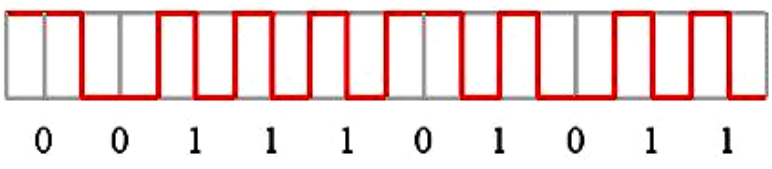
represented by a transition (0, +, 0, -).

Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).



CMI (Coded Mark Inversion): A zero is sent a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].

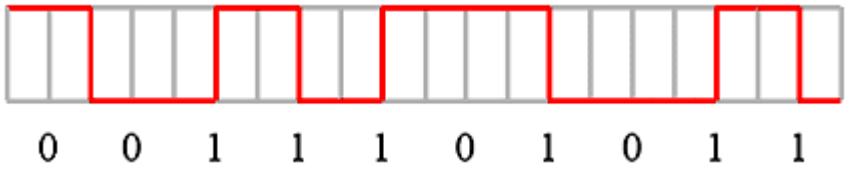
Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.



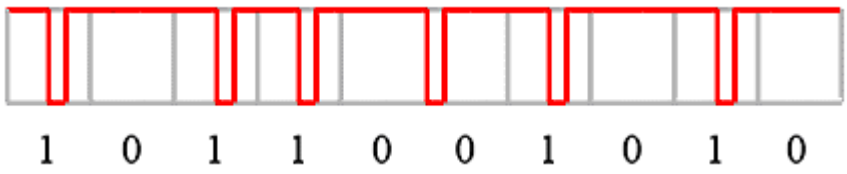
Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

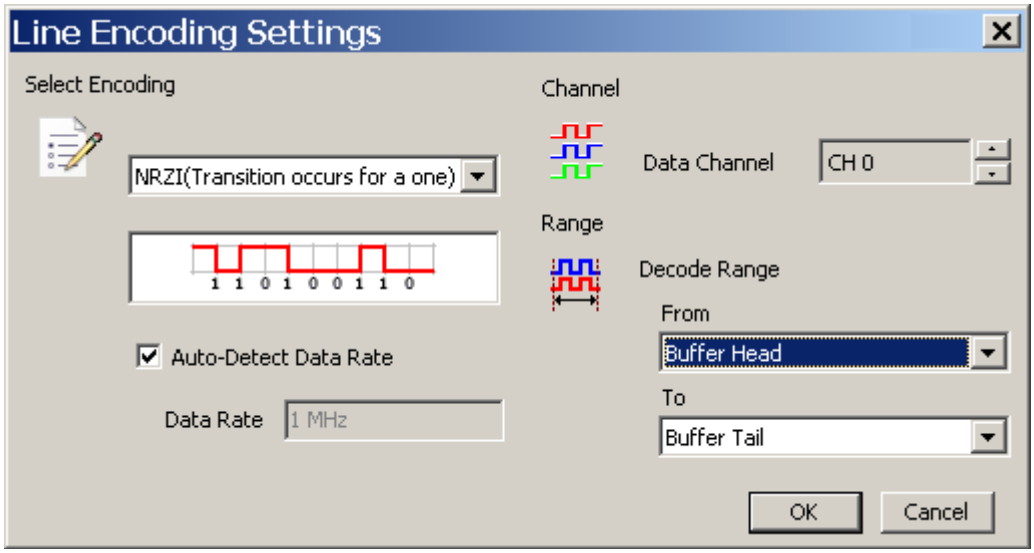
Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Encoding: Select the line code you want to encode.

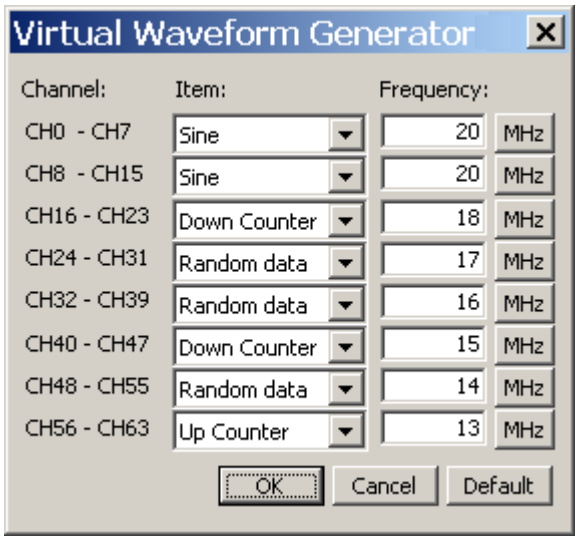
Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate is not selected.

Channel: Show the selected channel (CH 0).

Range: Select the range within the waveforms you want to encode.

Lissajous

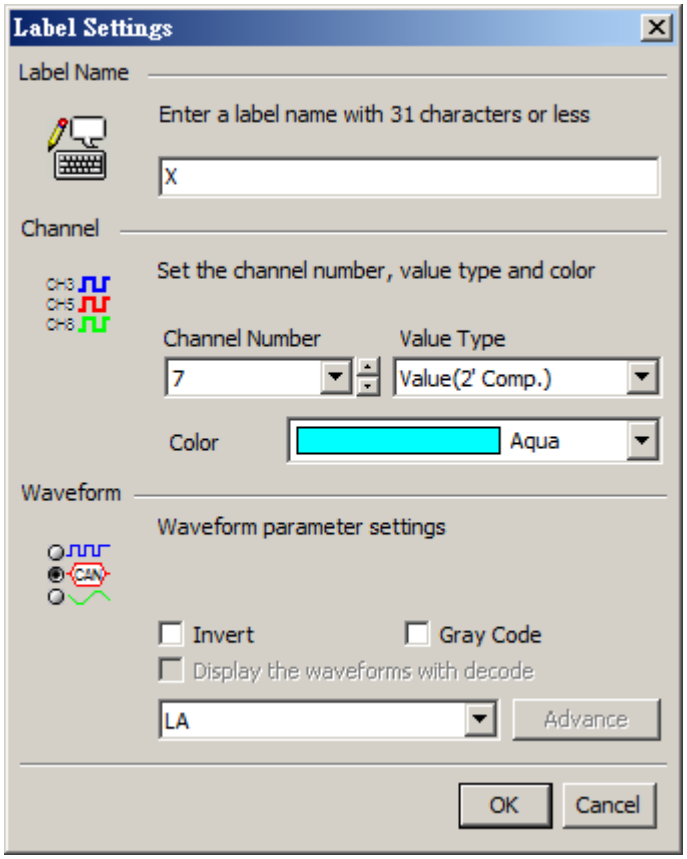
Add a Lissajous decode: The Virtual Waveform Generator, only available when no instrument is connected to your PC, can generate sine waves to form a Lissajous graph. Click Virtual Waveform Generator from the Device menu or click Virtual Waveform Generator button on the Toolbar to show the dialog box below.



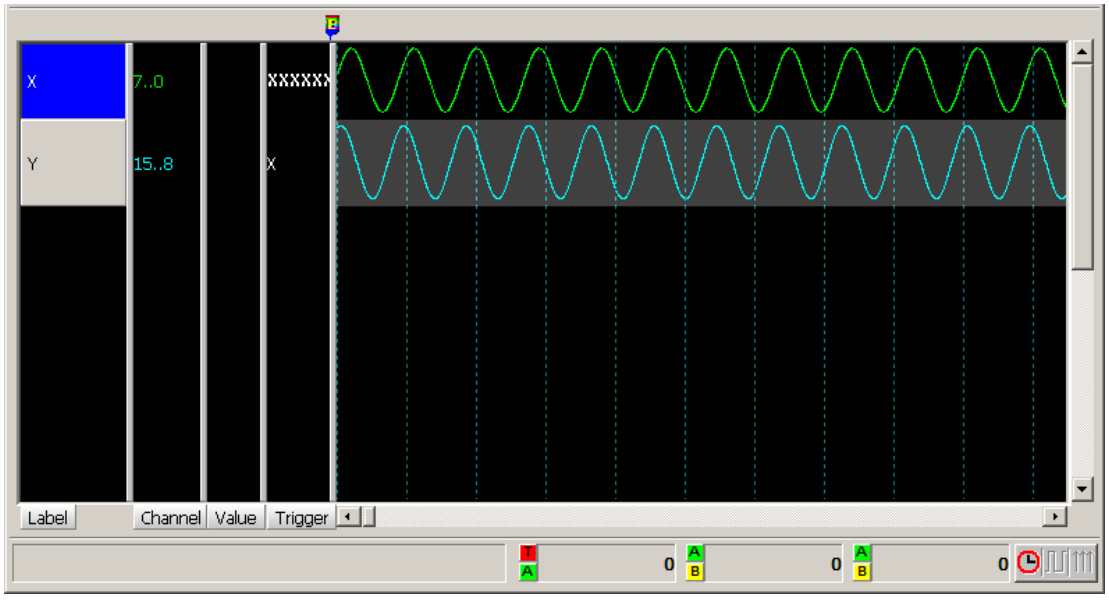
Set parameters like Item (Sine, ..., Up Counter) and Frequency (20MHz, ..., 13MHz).

Note: CH0 and CH8 are the least significant bits (LSB), CH7 and CH15 are the most significant bits (MSB).

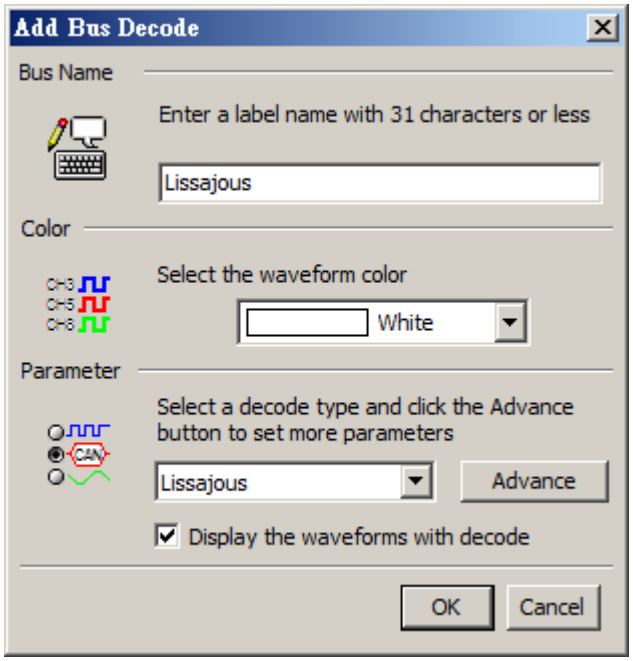
Combine the eight labels (CH0-CH7/CH8-CH17) to form a Sine wave bus and enter a new name (X/Y), then double click on the label name (X/Y) to show the Label Settings dialog box below.



Set more parameters for Sine waves X/Y like Value Type (2' Comp), Color (Aqua) and click OK to generate the sine waves below.

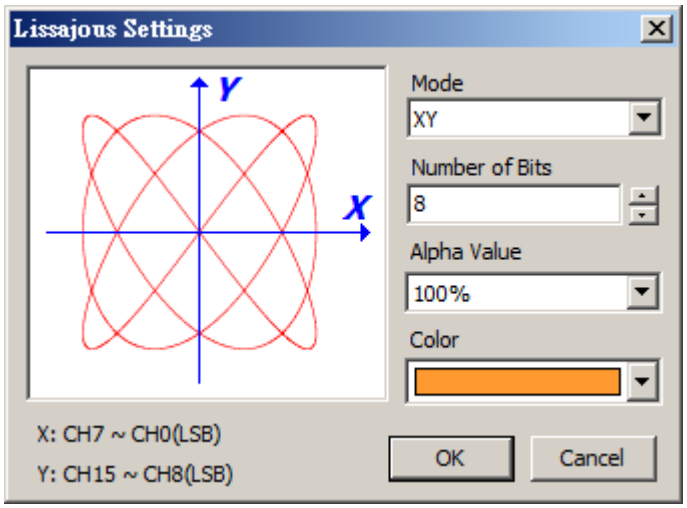


Click Add Bus Decode in the Label menu to show the dialog box below.



Select Lissajous in Parameter and click Advance to show the dialog box below.

Settings



Mode: Set the mode for the axis (XY or IQ).

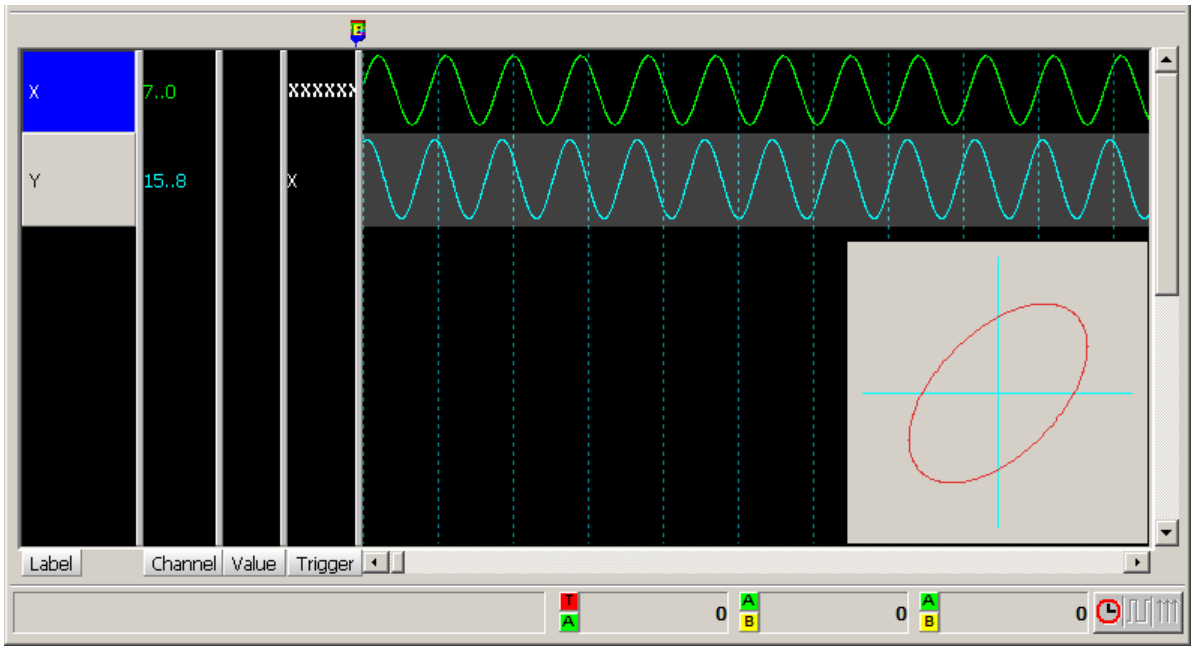
Number of Bits: Set the number of data bits (8).

Alpha Value: The higher, the less transparent for the Lissajous graph on the Waveform Window.

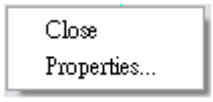
Color: Set the color for the Lissajous graph.

Result

Click **OK** to see the Lissajous graph on the lower-right corner of the Waveform Window.



Right-click the Lissajous graph to show the dialog box below.



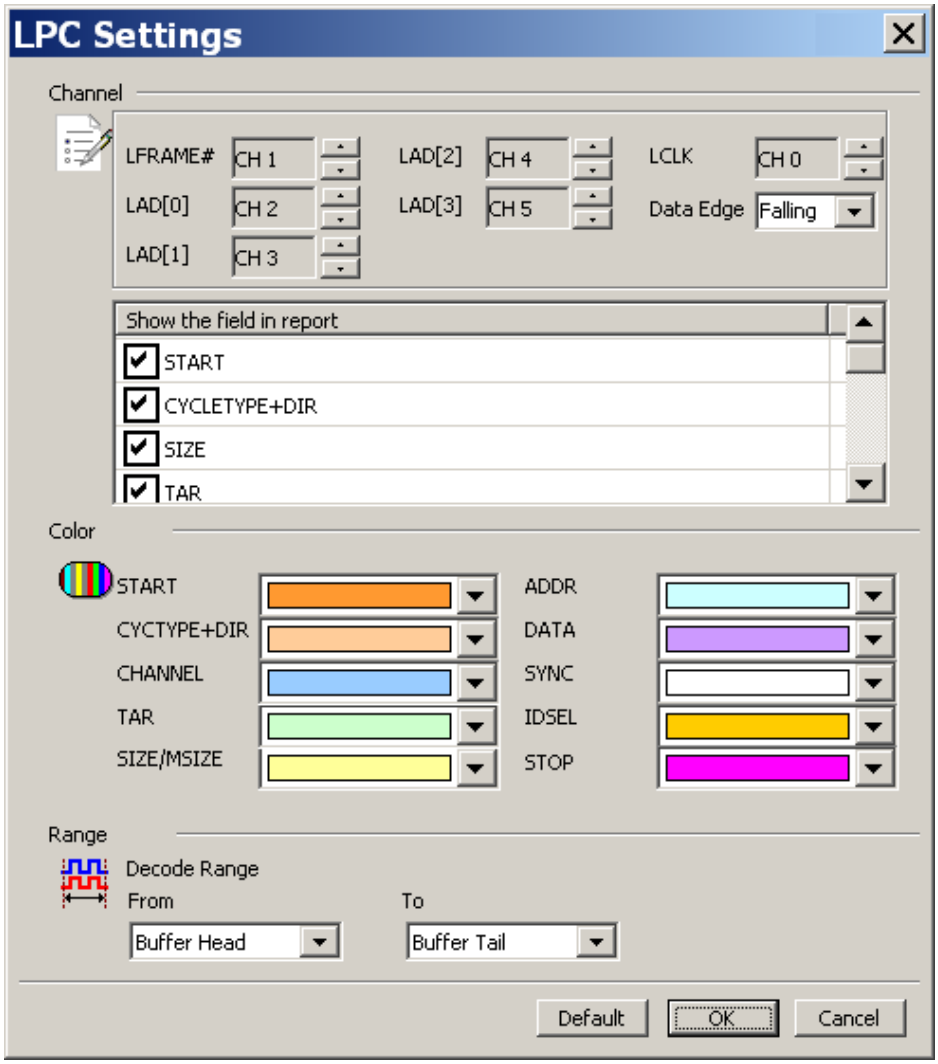
Close: Close the Lissajous graph.

Properties: Return to the Lissajous Settings.

Low Pin Count (LPC)

The LPC bus, for the data transmissions, was developed by Intel to replace the ISA bus.

Settings



Channel: Show the selected channels.

LFRAME#: Frame indicator.

LAD[0-3]: Data bits.

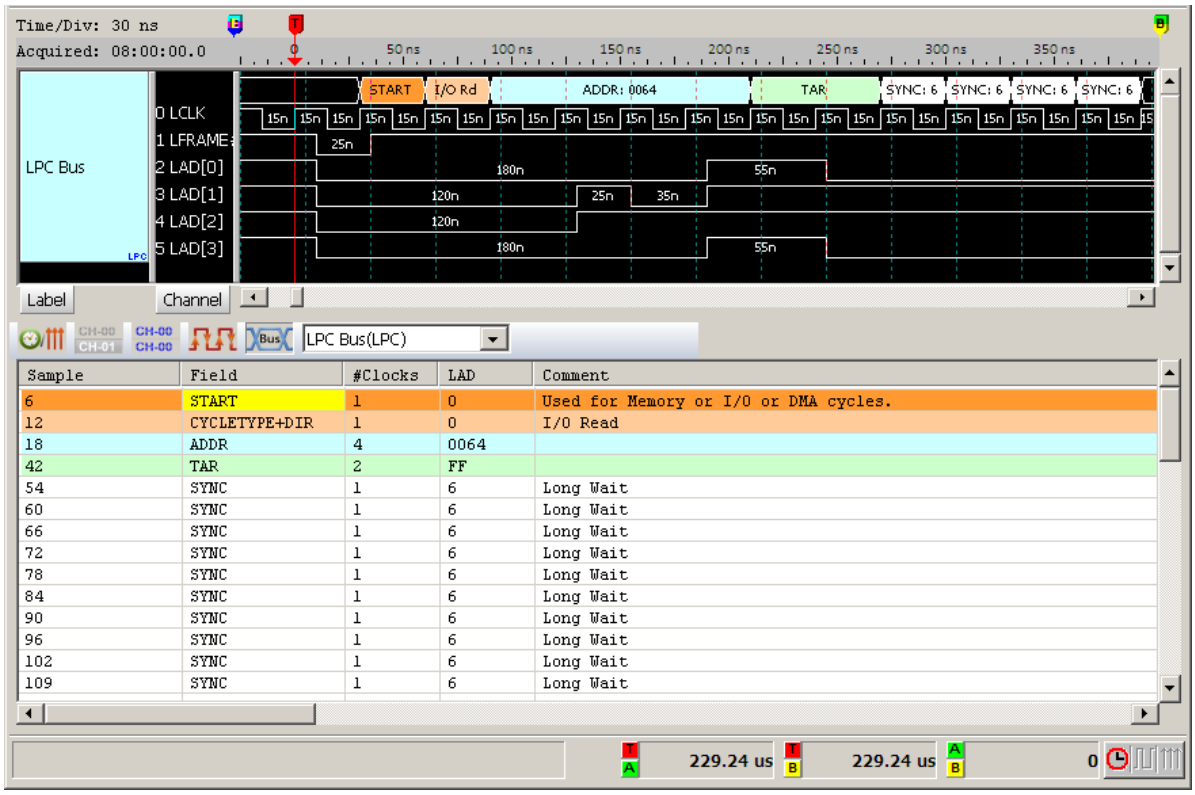
LCLK: Clock.

Filter the data in the report window: You can filter the data in the Report Window.

Result

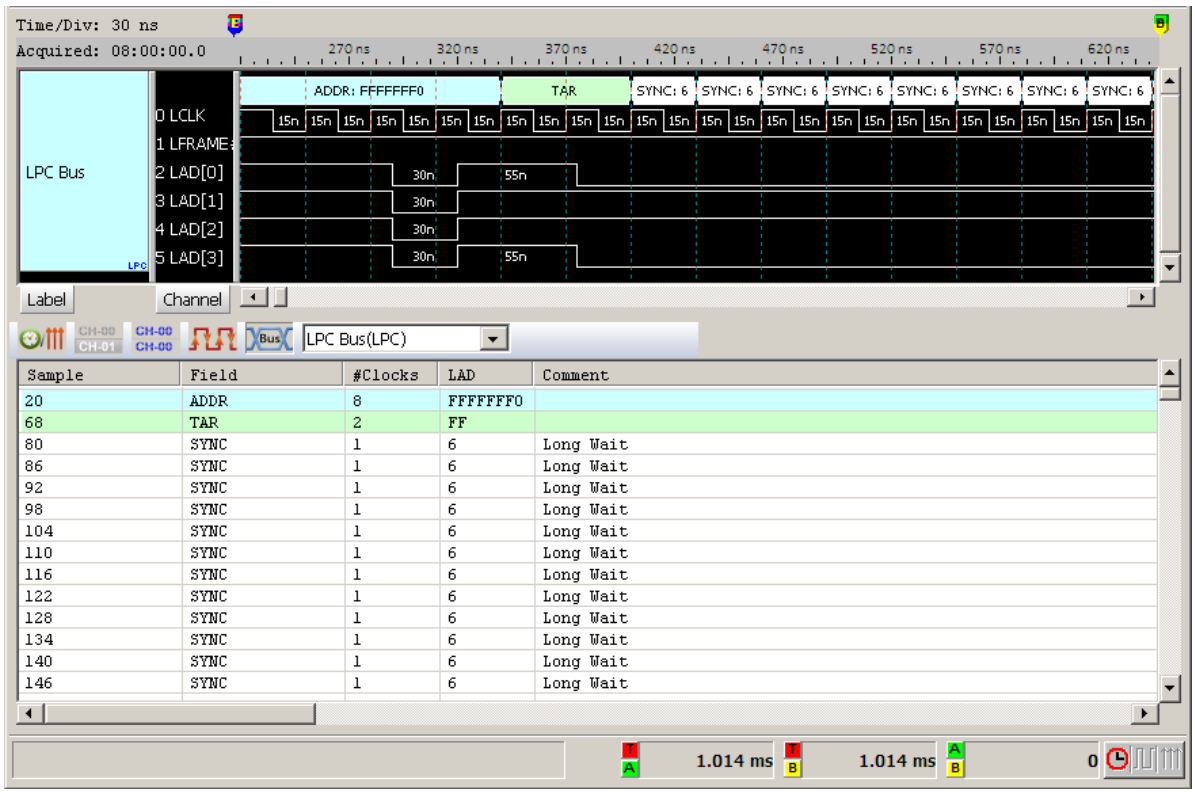
Click **OK** to run the LPC decode and see the result on the Waveform Window below.

I/O Read Cycle.



Sample	Field	#Clocks	LAD	Comment
6	START	1	0	Used for Memory or I/O or DMA cycles.
12	CYCLETYPE+DIR	1	0	I/O Read
18	ADDR	4	0064	
42	TAR	2	FF	
54	SYNC	1	6	Long Wait
60	SYNC	1	6	Long Wait
66	SYNC	1	6	Long Wait
72	SYNC	1	6	Long Wait
78	SYNC	1	6	Long Wait
84	SYNC	1	6	Long Wait
90	SYNC	1	6	Long Wait
96	SYNC	1	6	Long Wait
102	SYNC	1	6	Long Wait
109	SYNC	1	6	Long Wait

Memory Read Cycle

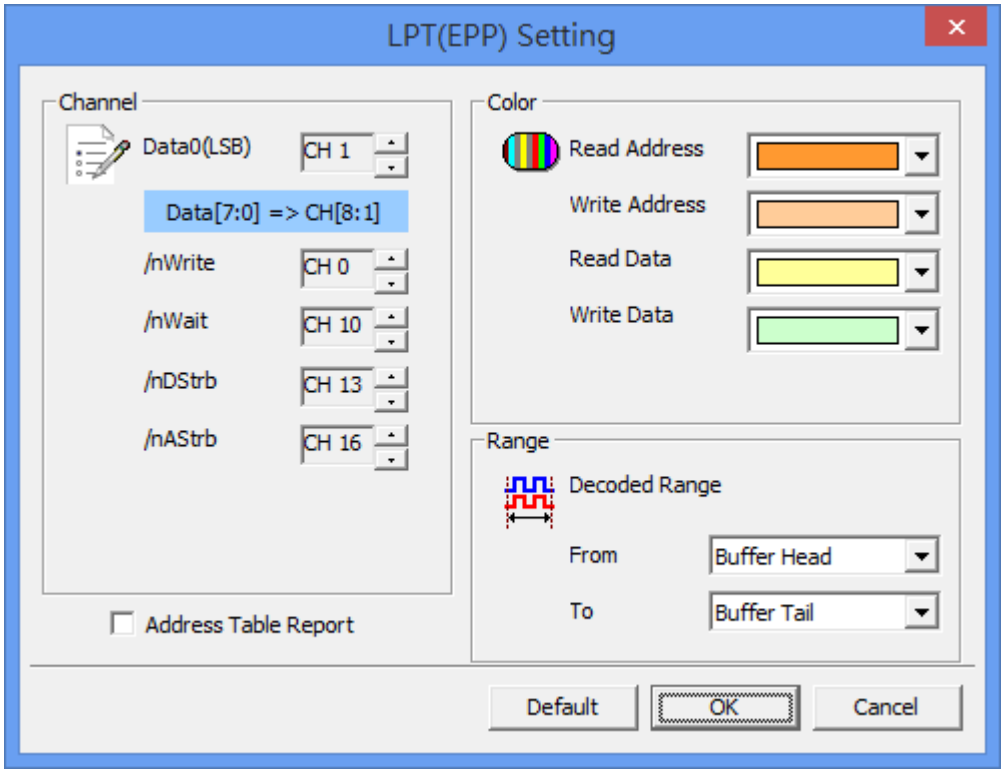


Sample	Field	#Clocks	LAD	Comment
20	ADDR	8	FFFFFFF0	
68	TAR	2	FF	
80	SYNC	1	6	Long Wait
86	SYNC	1	6	Long Wait
92	SYNC	1	6	Long Wait
98	SYNC	1	6	Long Wait
104	SYNC	1	6	Long Wait
110	SYNC	1	6	Long Wait
116	SYNC	1	6	Long Wait
122	SYNC	1	6	Long Wait
128	SYNC	1	6	Long Wait
134	SYNC	1	6	Long Wait
140	SYNC	1	6	Long Wait
146	SYNC	1	6	Long Wait

Line Printer Terminal Port (LPT)

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals. This decode only support EPP Mode.

Settings



Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other channel will be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

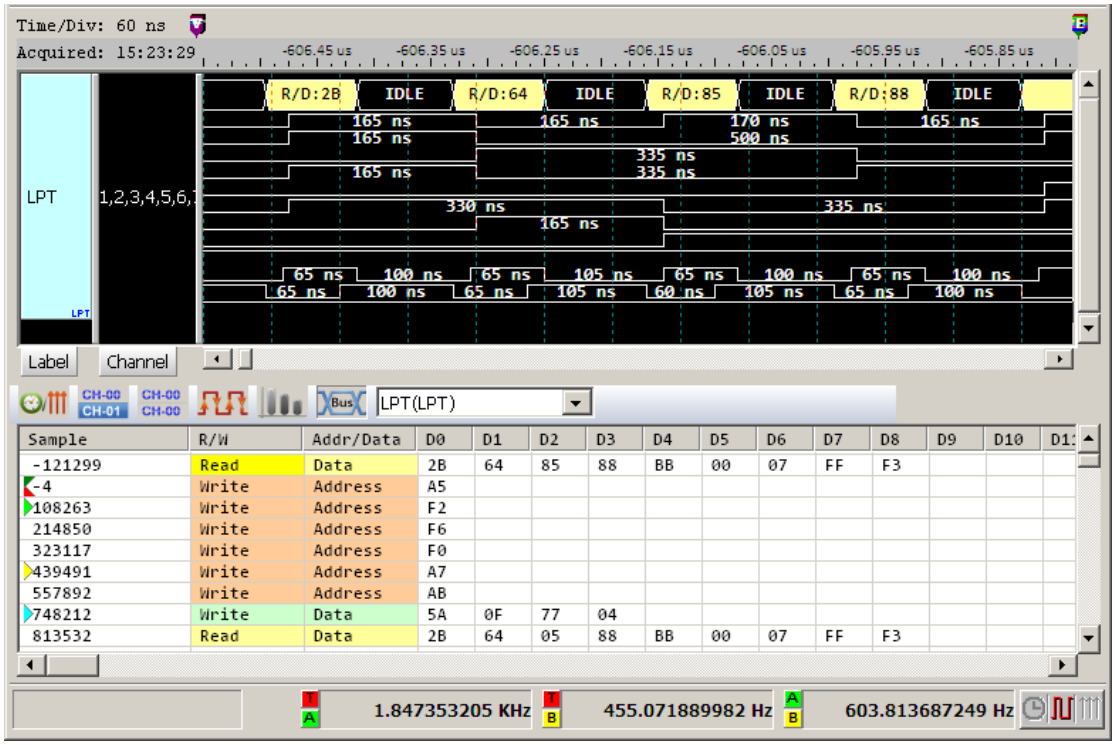
/nAStrb: Indicates the address cycle.

/nInit: Indicates a termination cycle in order to return the interface to the Compatibility mode. User can option to use this channel or not.

/nIntr: This is an interrupt signal. User can option to use this channel or not.

Result

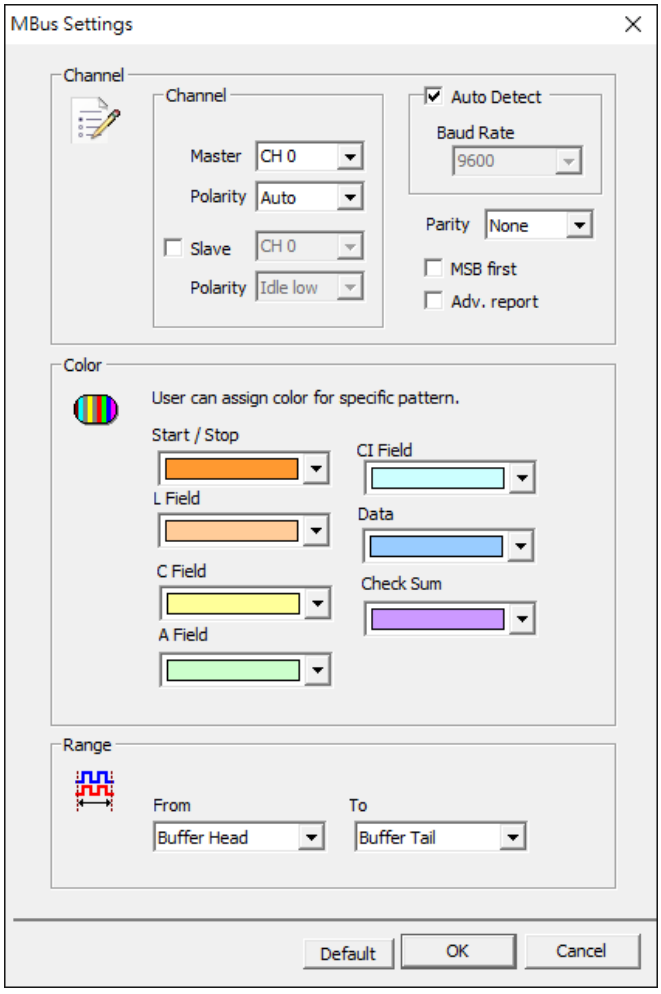
Click OK to run the LPT Decode and see result on the Waveform Windows below.



M-Bus

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

Settings



Channel: Set the channel of the signal and Polarity.

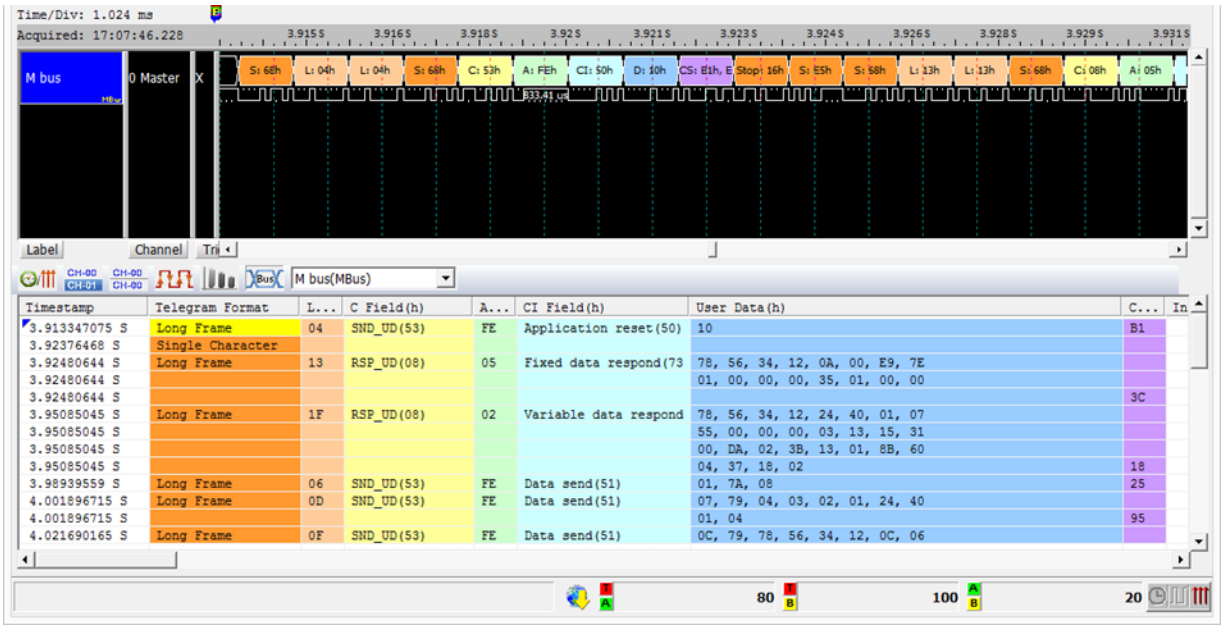
Baud rate: Set the specific data rate or auto detection.

Parity: Error detection.

MSB first: Set MSB format.

Adv. Report: Advanced report.

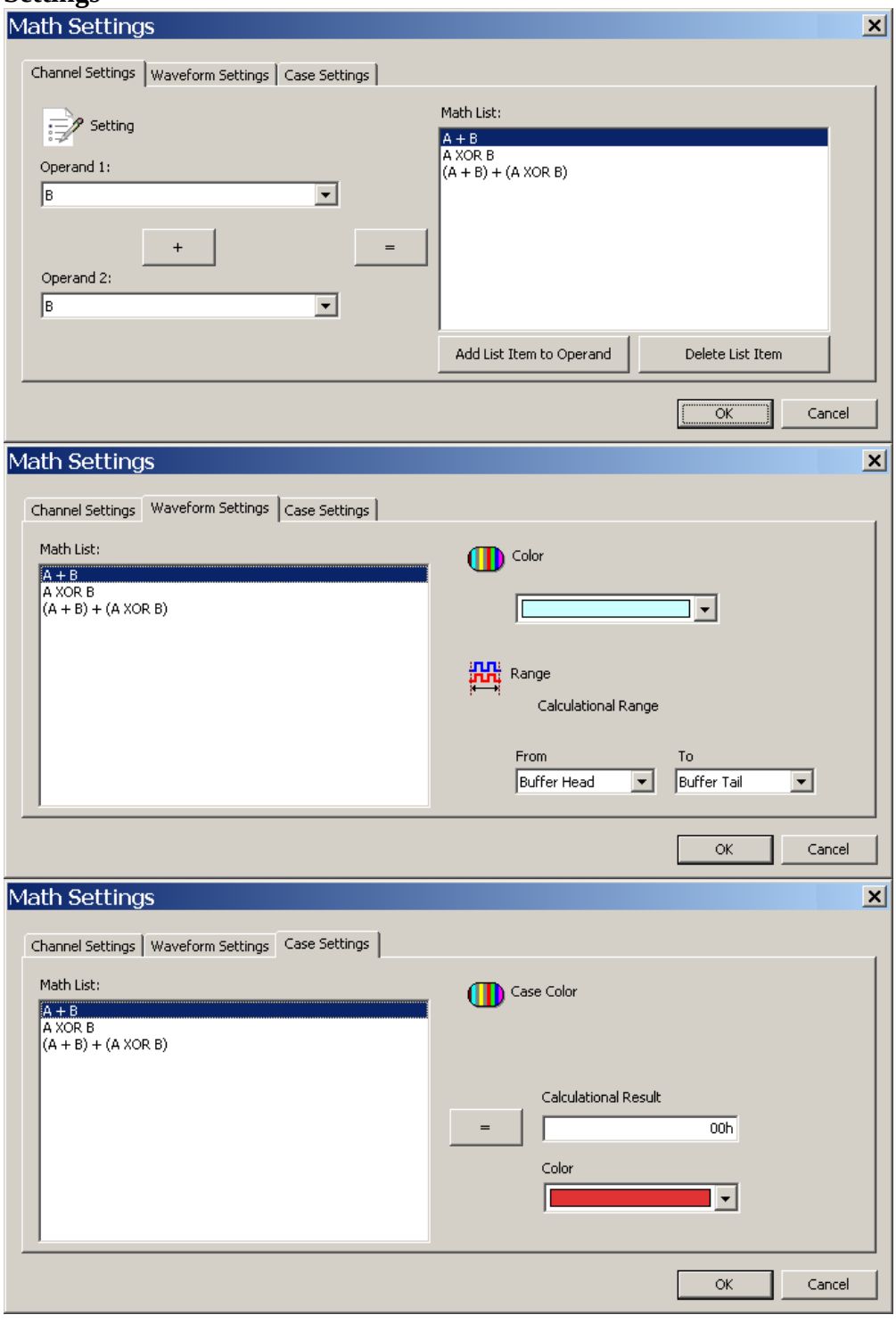
Result



Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR, OR,NAND, NOR, XNOR operation for the channel or combined channels.

Settings



Operand: Select the channel(s) in the waveform window.

"+": Select "+", "-", "X", "/", "AND", "XOR", "OR" , "NAND", "NOR", "XNOR" operator.

"=": Add operation type.

Add List Item to Operand: Add operation type to operand.

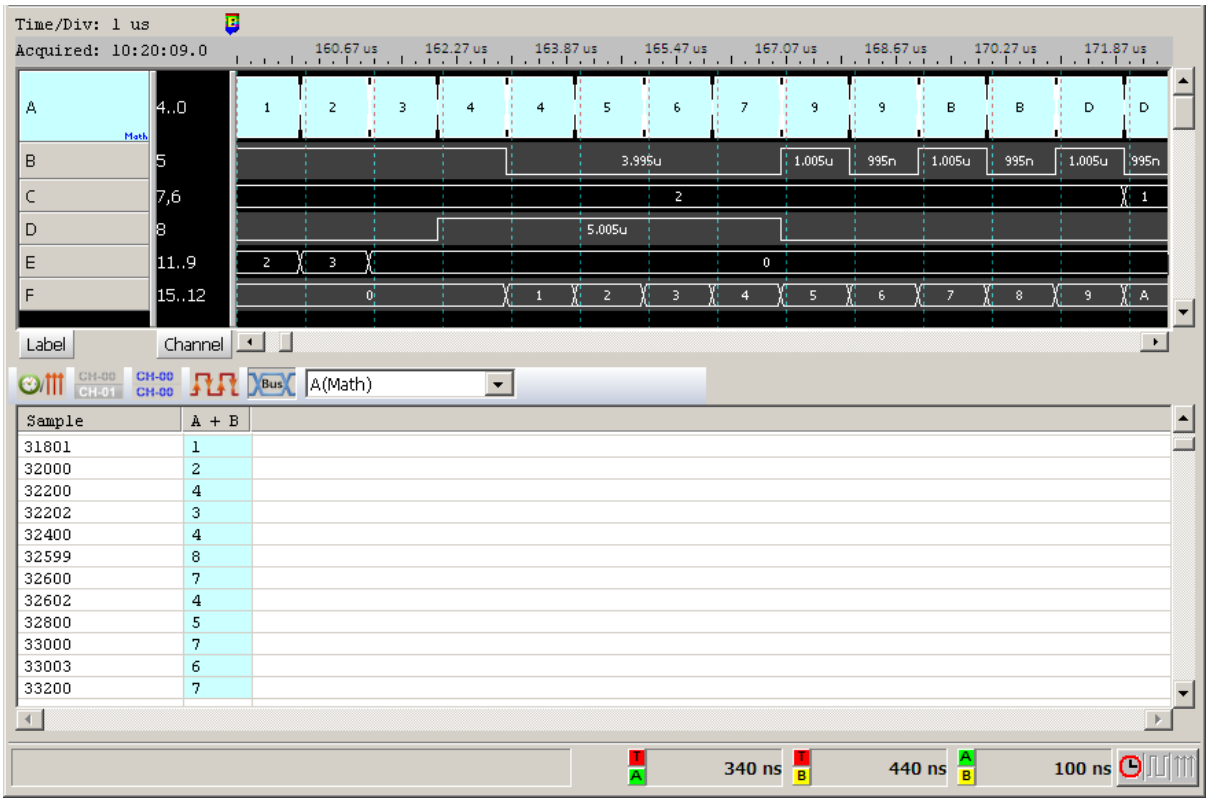
Delete List Item: Delete operation type from the list.

Color: Set the colors for the data bits.

Range: Select the range within the waveform you want to decode.

Case Settings: Select condition and frame color.

Result

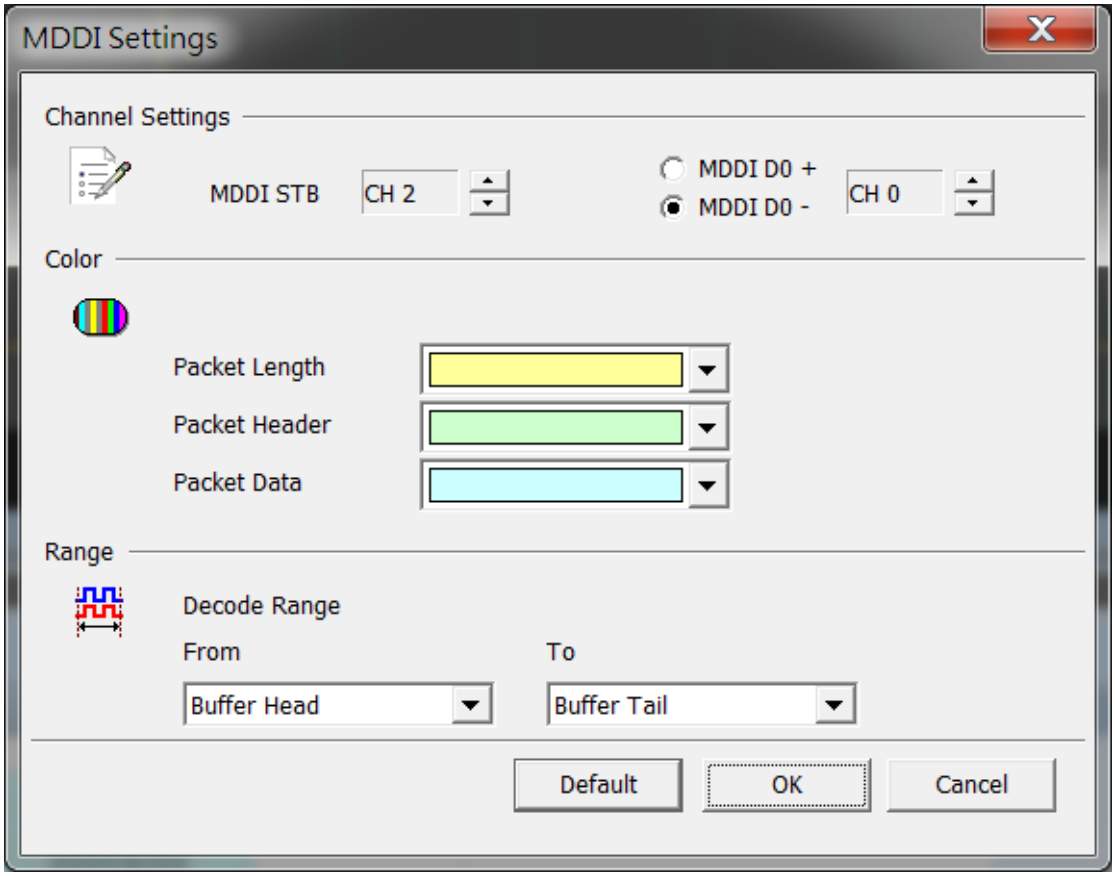


Note: When the Math settings are finished, the settings will always be saved as an independent text file named as AqMath.txt, different from the waveform file, at work directory unless other name assigned. If you need the specific Math settings, please save it, so you can reload the settings next time you open the specific waveform file.

Mobile Display Digital Interface (MDDI)

The Mobile Display Digital Interface (MDDI) is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link for connecting portable computing, communication, and entertainment devices to wearable micro displays. This decoder is based on VESA Mobile Display Digital Interface Standard Version 1.2, only Type I communication is supported in this decoder.

1. MDDI Parameter Settings



Channel Settings

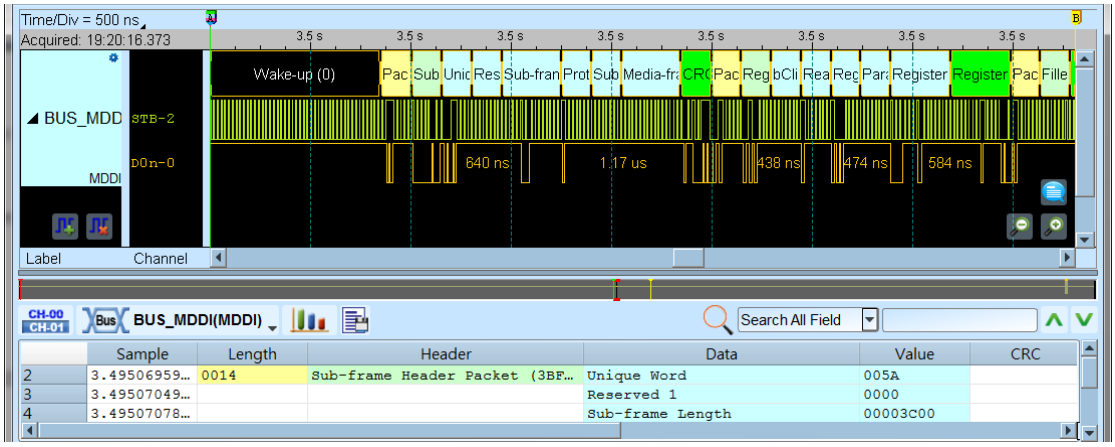
MDDI STB: MDDI Strobe

MDDI D0+/-: MDDI Data 0 +/-

Configure the Channel setup for the decoder, and choose the data source

from Data 0+ or Data 0-.

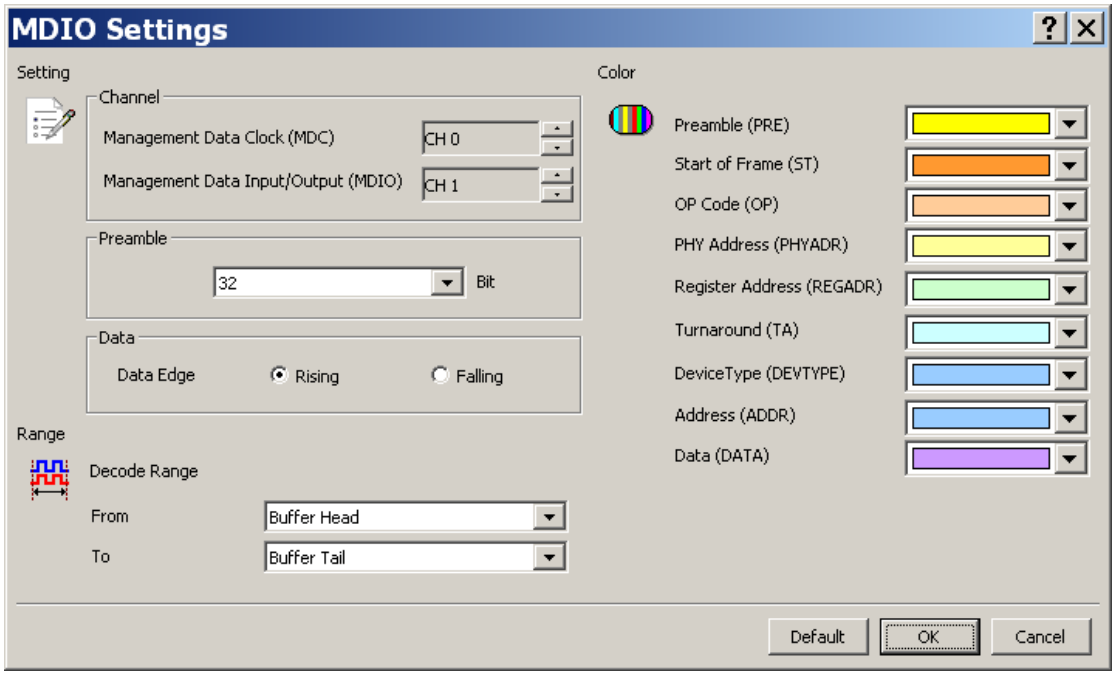
2. Result



MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

Settings



MDC: Clock.

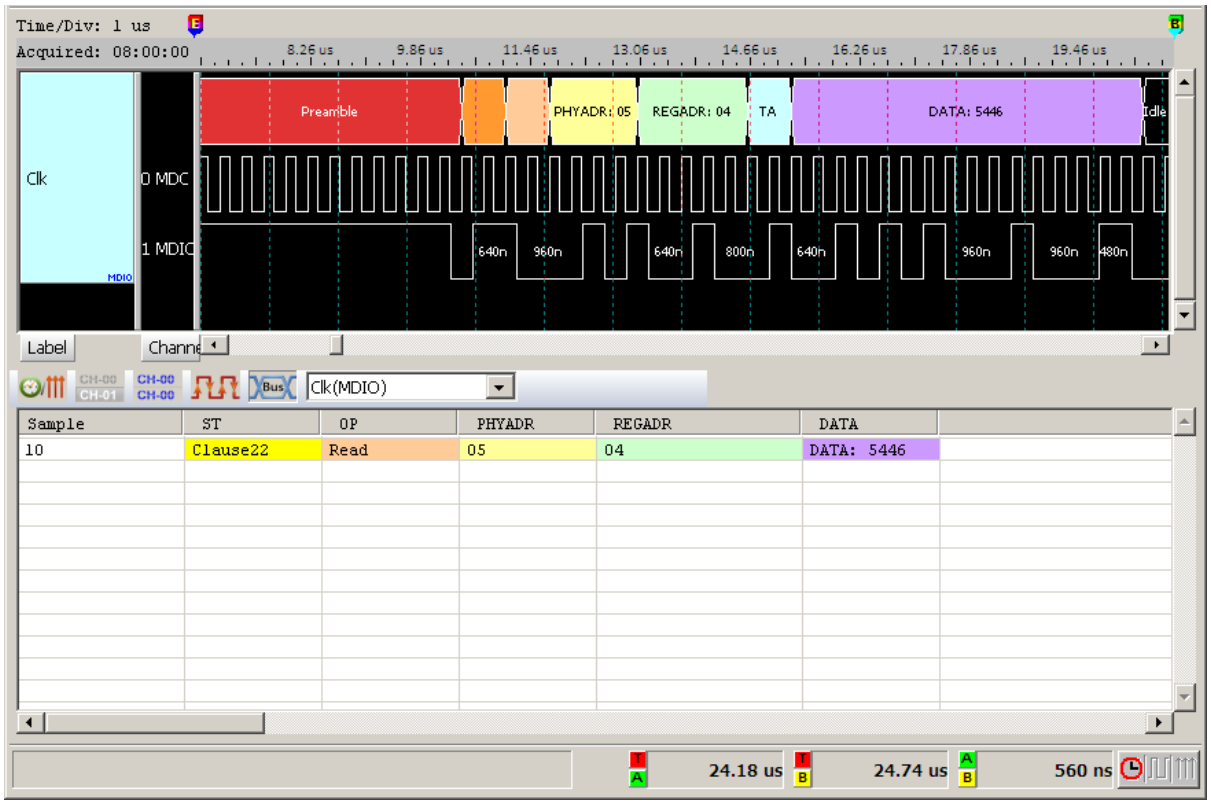
MDIO: Data Input / Output.

Preamble: Set the MDIO preamble width, 32 bit default.

Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising Edge default.

Result

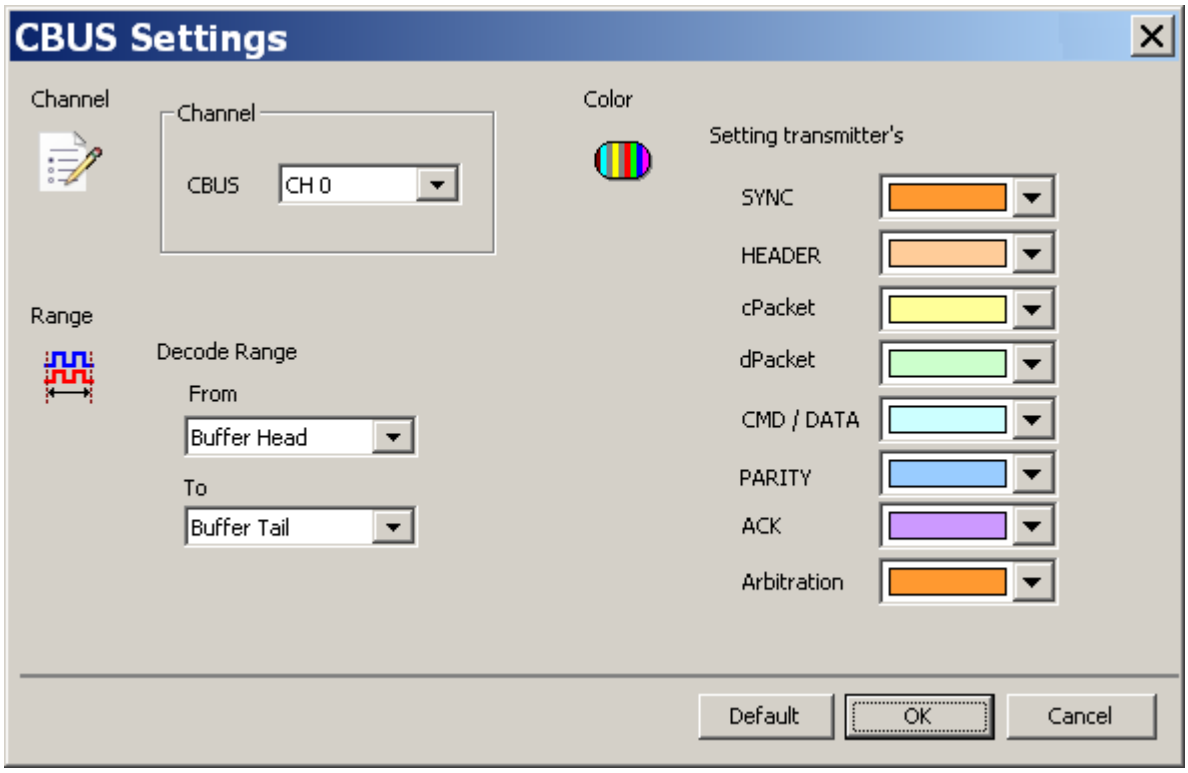
Click **OK** to run the MDIO decode and see the result on the Waveform Window below.



MHL-CBUS

Mobile High-definition Link (MHL) is an HD audio and video interface, Control Bus (CBUS) is used to control it.

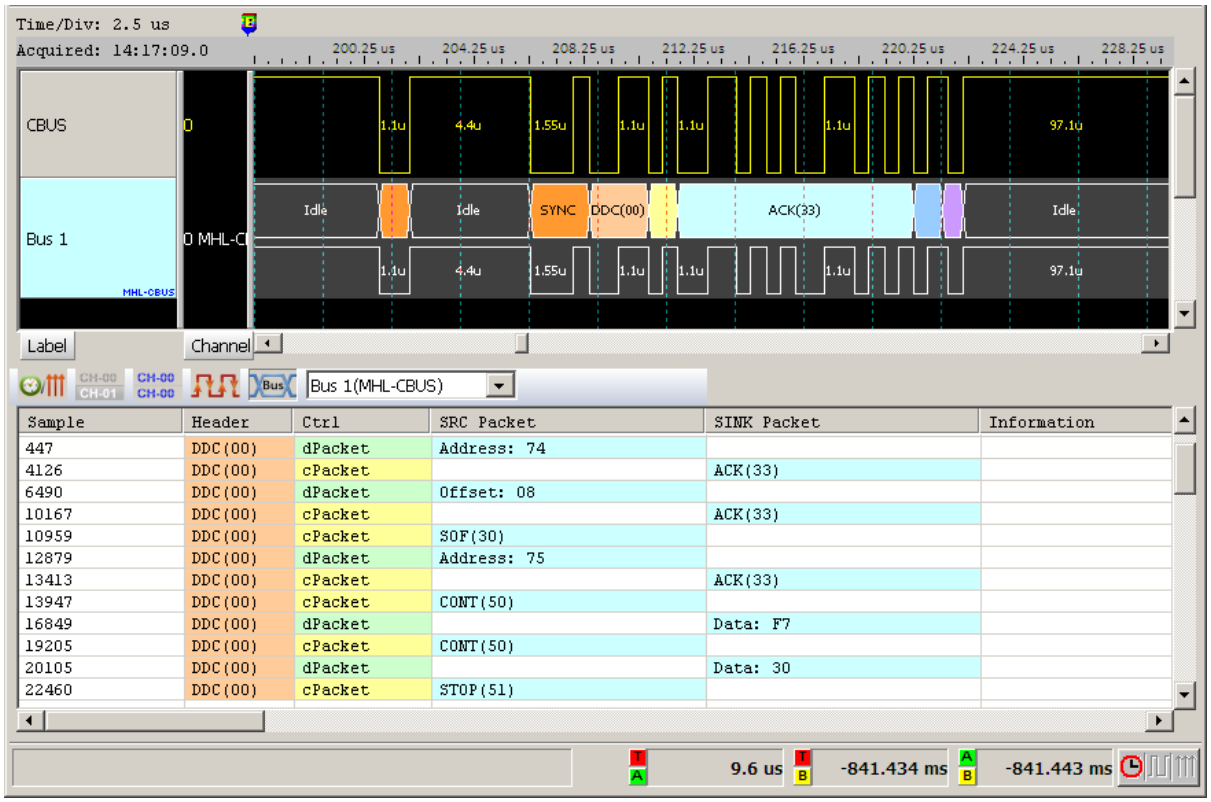
Settings



LA Channel: Show the selected channel (CH0).

Result

Click OK to run the MHL-CBUS Decode and see result on the Waveform Window below.

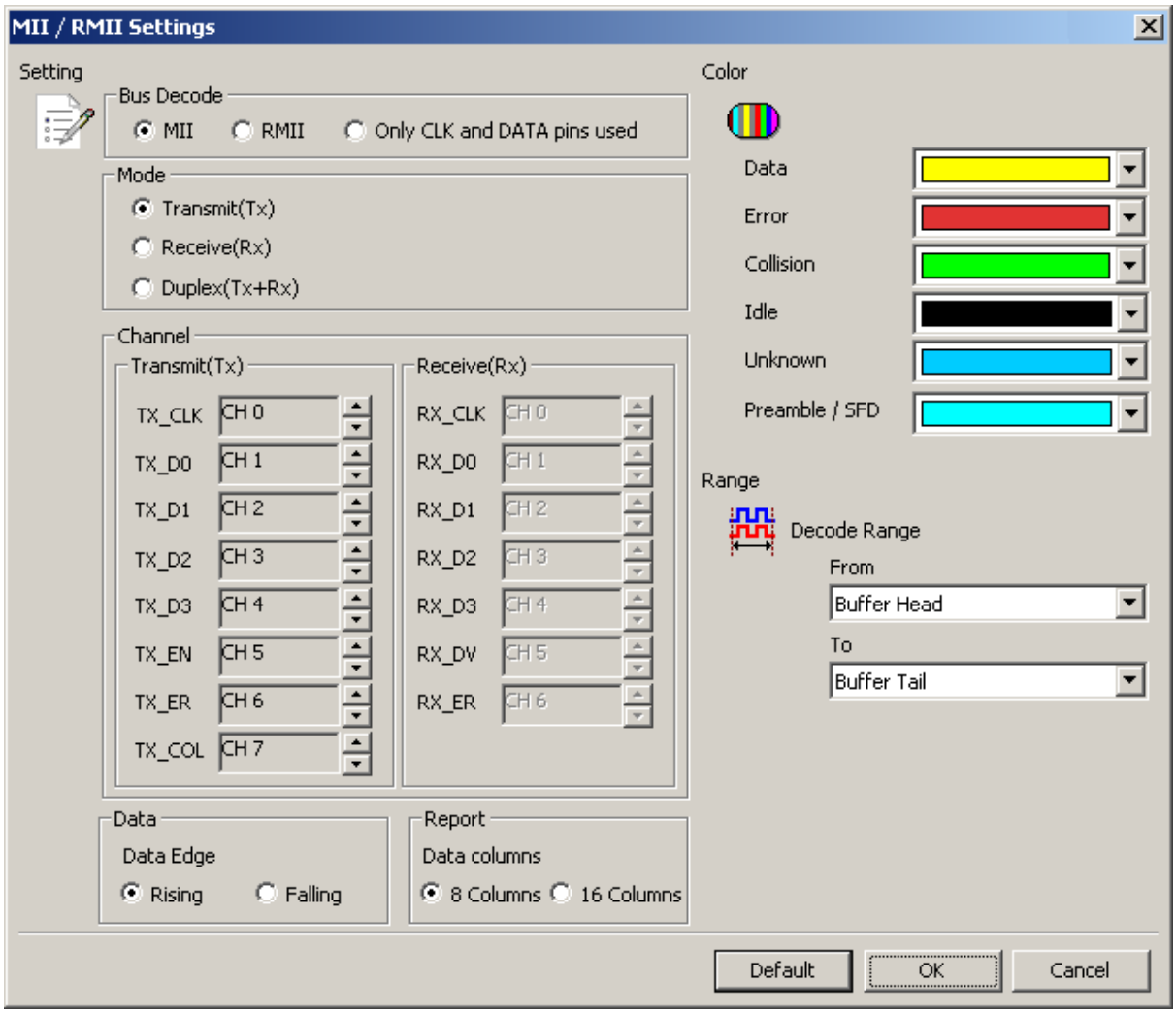


Sample	Header	Ctrl	SRC Packet	SINK Packet	Information
447	DDC(00)	dPacket	Address: 74		
4126	DDC(00)	cPacket		ACK(33)	
6490	DDC(00)	dPacket	Offset: 08		
10167	DDC(00)	cPacket		ACK(33)	
10959	DDC(00)	cPacket	SOF(30)		
12879	DDC(00)	dPacket	Address: 75		
13413	DDC(00)	cPacket		ACK(33)	
13947	DDC(00)	cPacket	CONT(50)		
16849	DDC(00)	dPacket		Data: F7	
19205	DDC(00)	cPacket	CONT(50)		
20105	DDC(00)	dPacket		Data: 30	
22460	DDC(00)	cPacket	STOP(51)		

MII/RMII

MII/RMII (Media Independent Interface/Reduced Media Independent Interface) is a protocol formulated by 802.3u that applied to Fast Ethernet, connecting MAC of Data Link Layer and PHY layer. Its clock frequency is either 25MHz or 2.5MHz (Ethernet); they are TX_CLK and RX_CLK. TX [0:3], RX [0:3] are 4-bit-width bus and TX_EN, RX_EN enable the IN/OUT; TX_ER, RX_ER can detect the errors on the bus; RX_DV inform bus the data received is valid or not; COL can detect the collision on the bus. **Serial Management Interface (SMI), also known as MDIO, is also an important part of MII.**

Settings



MII / RMII: Select the MII / RMII bus decode

GMII / RGMII: Select the GMII / RGMII bus decode

Only CLK and Data pins used(M/G): Select MII / GMII the CLK and Data pins only**.**

Transmit (Tx): Select TX mode

Receive (Rx): Select Rx mode

Duplex (Tx+Rx) : Select duplex mode

Channel: Set the channel number.

Rising: Select rising edge to latch data

Falling: Select falling edge to latch data

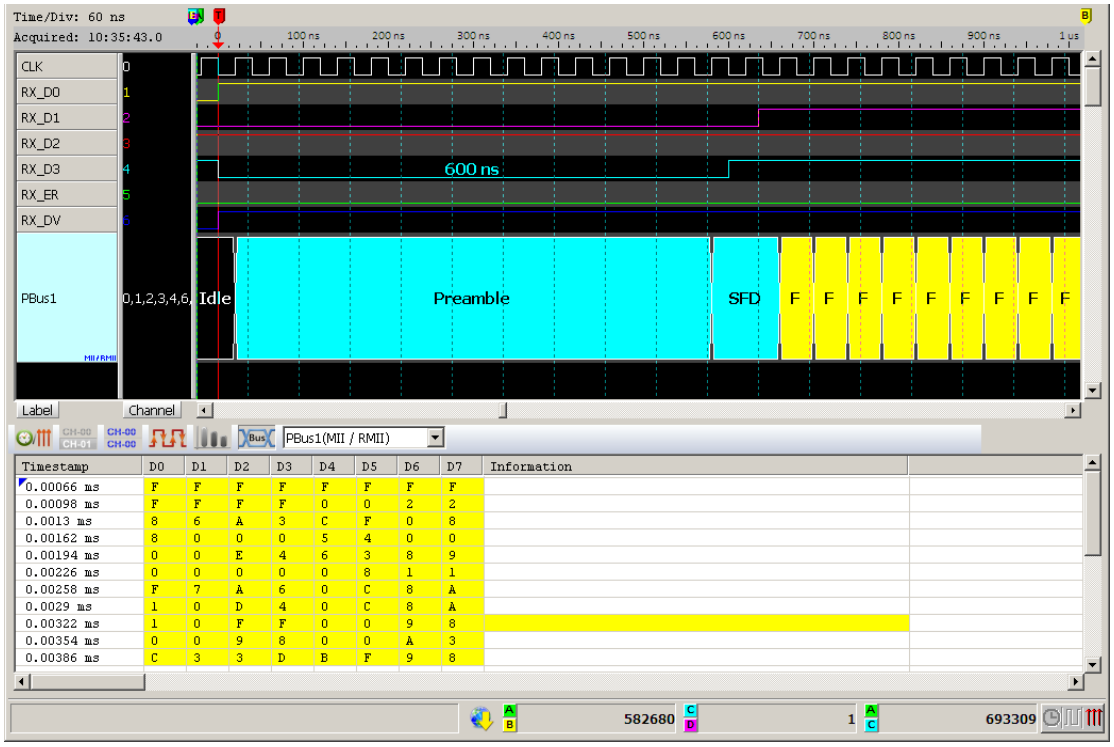
8 columns: show 8 columns data field in the report window

16 columns: show 16 columns data field in the report window

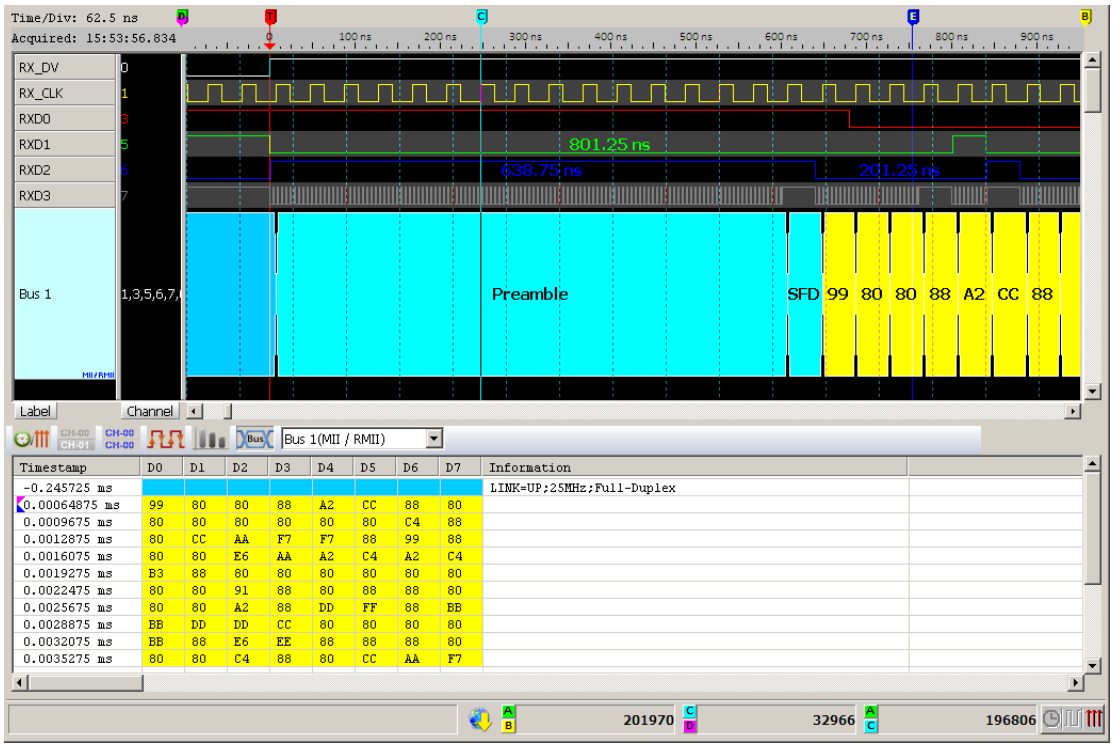
Result

Click **OK** to run the MII/RMII decode and see the result on the Waveform Window below.

MII



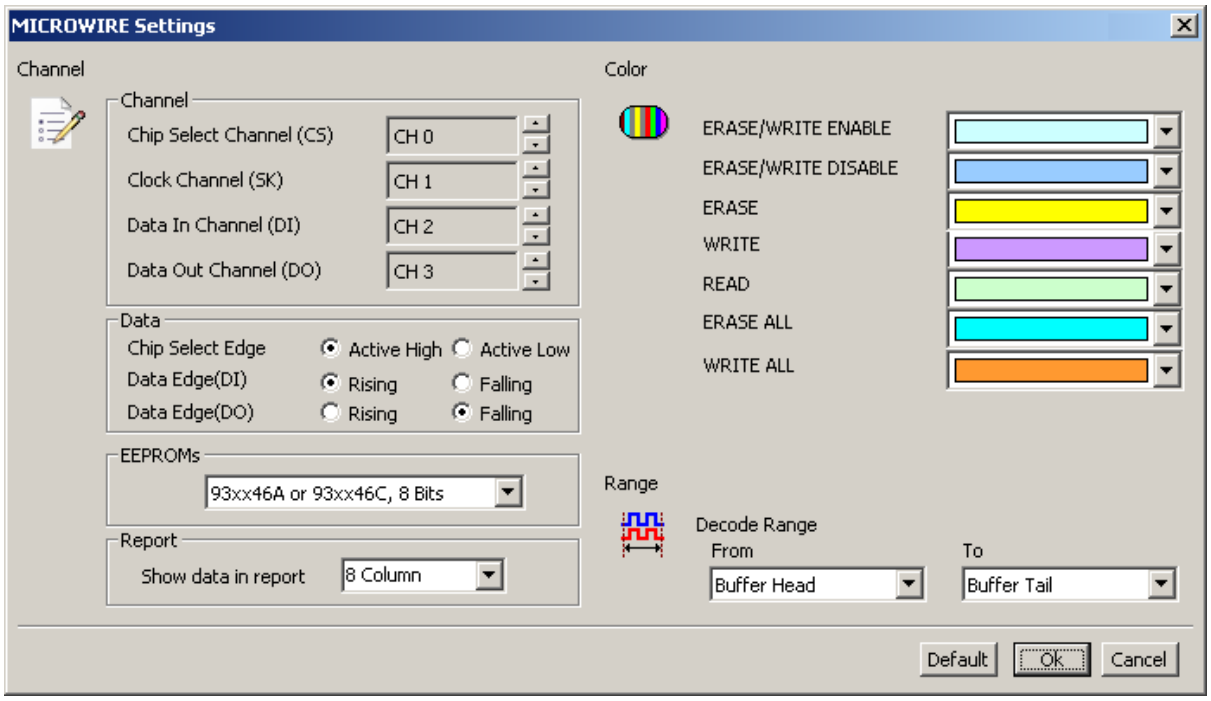
RGMII



Microwire

The Microwire bus has four data bits: Chip Select (CS), Serial Clock (SK), Data Input (DI), and Data Output (DO).

Settings



Channel: Show the selected channels.

Chip Select Edge: Active Low or Active High.

Data Edge: Rising or Falling.

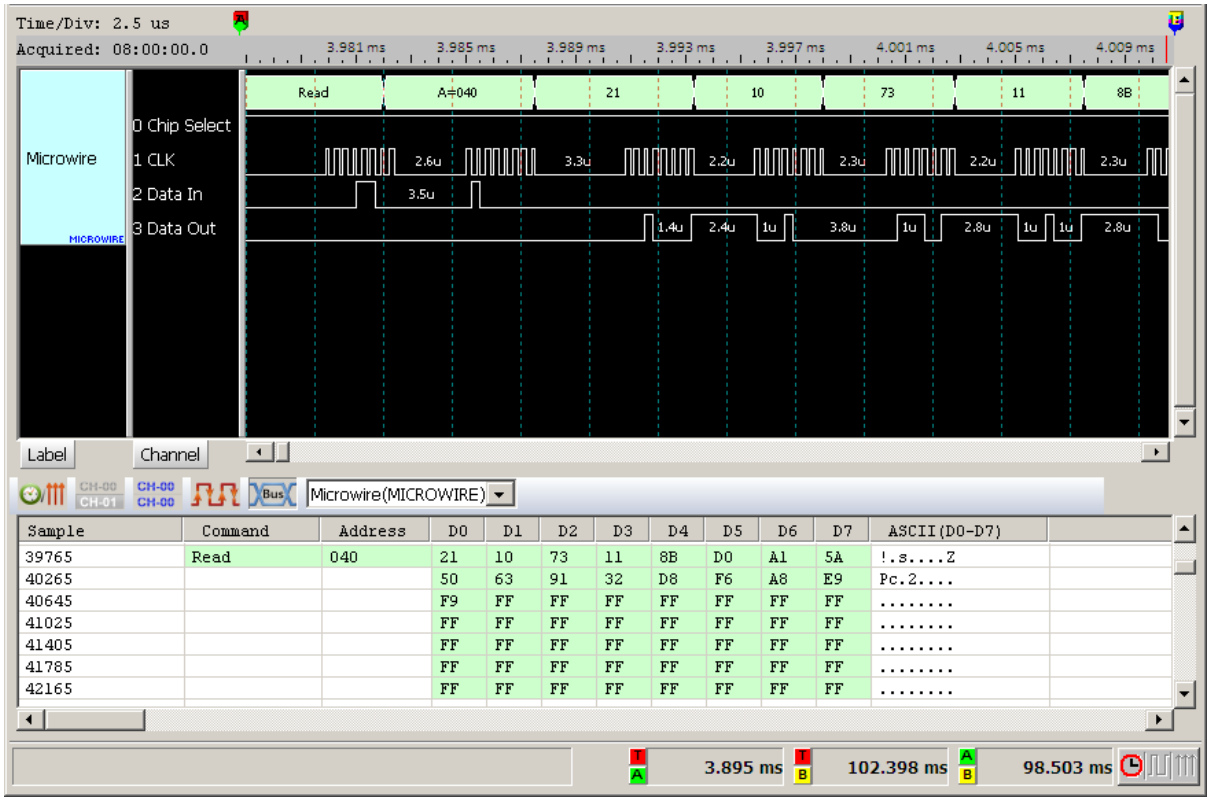
EEPROMs: Select EEPROMs.

Report: Show data in report.

Result

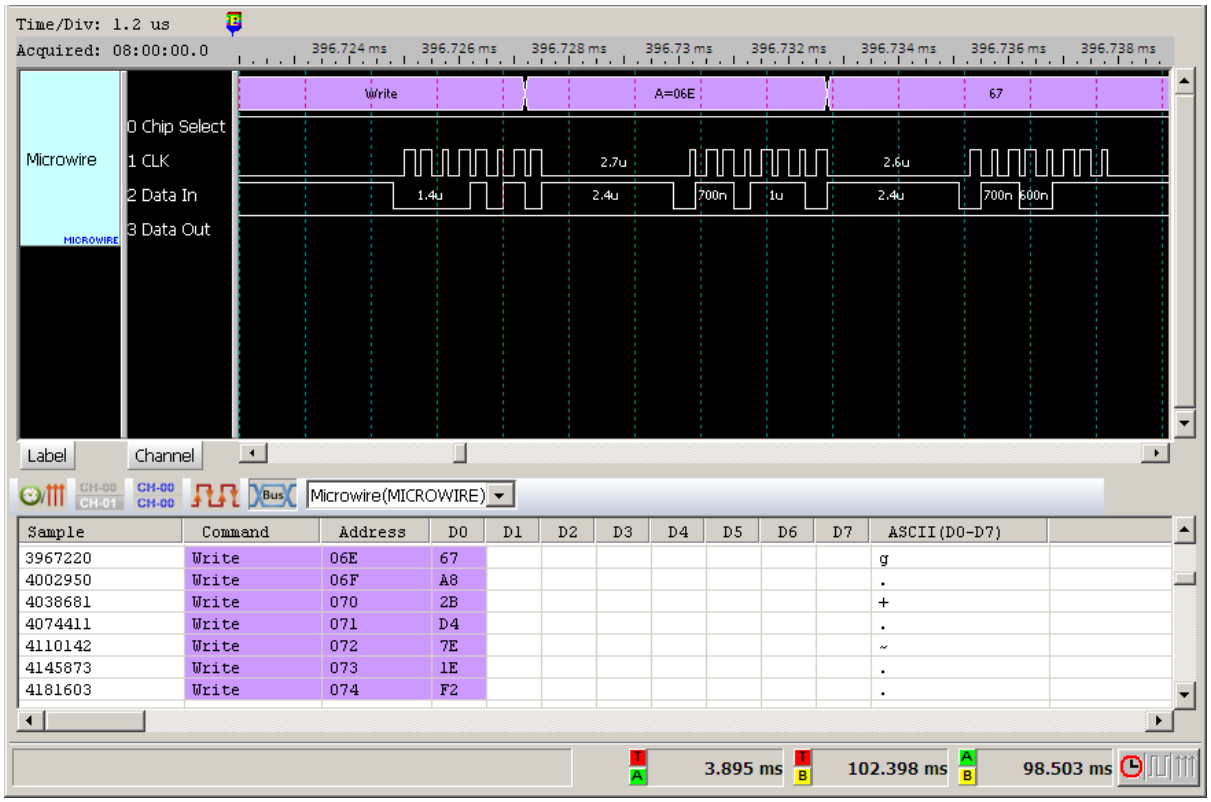
Click **OK** to run the Microwire decode and see the result on the Waveform Window below.

Read



Sample	Command	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
39765	Read	040	21	10	73	11	8B	D0	A1	5A	!.s....Z
40265			50	63	91	32	D8	F6	A8	E9	Pc.2....
40645			F9	FF	FF	FF	FF	FF	FF	FF	....
41025			FF	FF	FF	FF	FF	FF	FF	FF	....
41405			FF	FF	FF	FF	FF	FF	FF	FF	....
41785			FF	FF	FF	FF	FF	FF	FF	FF	....
42165			FF	FF	FF	FF	FF	FF	FF	FF	....

Write

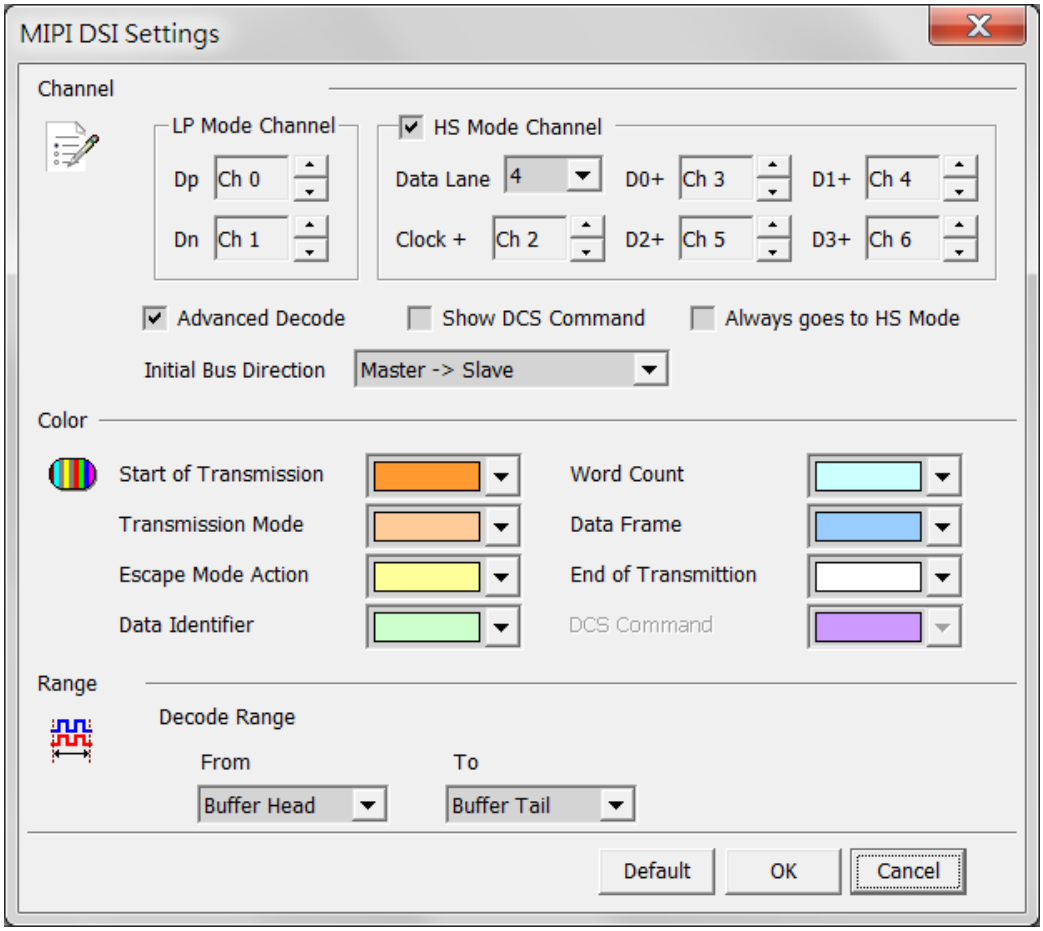


Sample	Command	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)
3967220	Write	06E	67								g
4002950	Write	06F	A8								.
4038681	Write	070	2B								+
4074411	Write	071	D4								.
4110142	Write	072	7E								~
4145873	Write	073	1E								.
4181603	Write	074	F2								.

MIPI DSI

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

Settings



Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines

Advanced Decode: Enable DSI format decode and display.

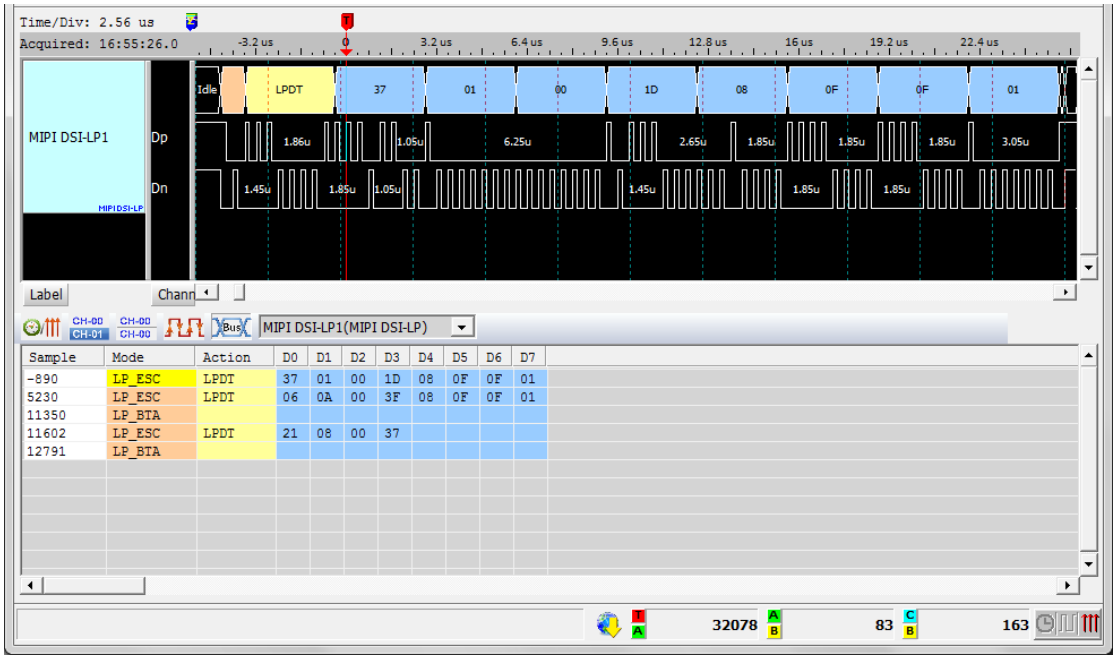
Show DCS Command: Enable DCS Command decode and display.

Always goes to HS Mode: Ignore the Dp and Dn status and decode all the data frame in HS mode

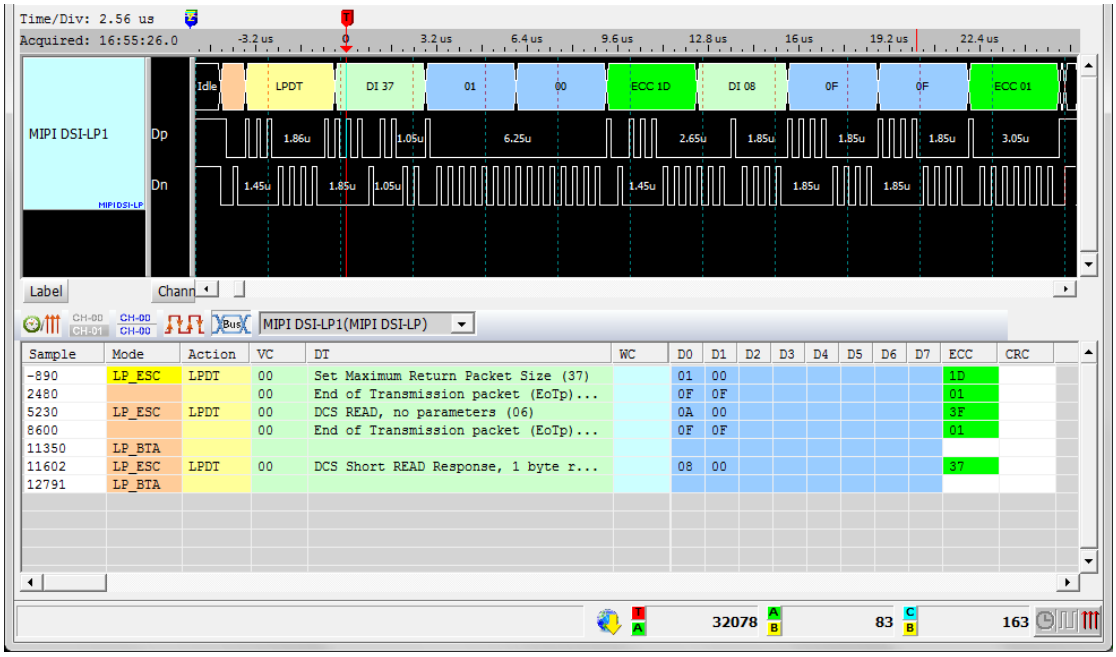
Initial Bus Direction: Select the Initial direction of the bus transmission.

Result

Advanced Decode Disabled:



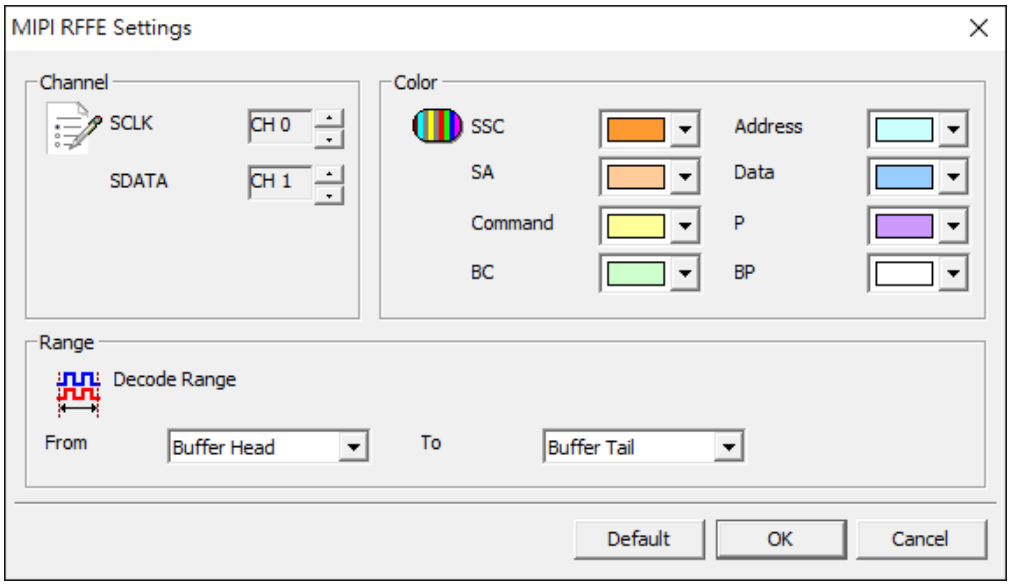
Advanced Decode Enabled:



MIPI RFFE

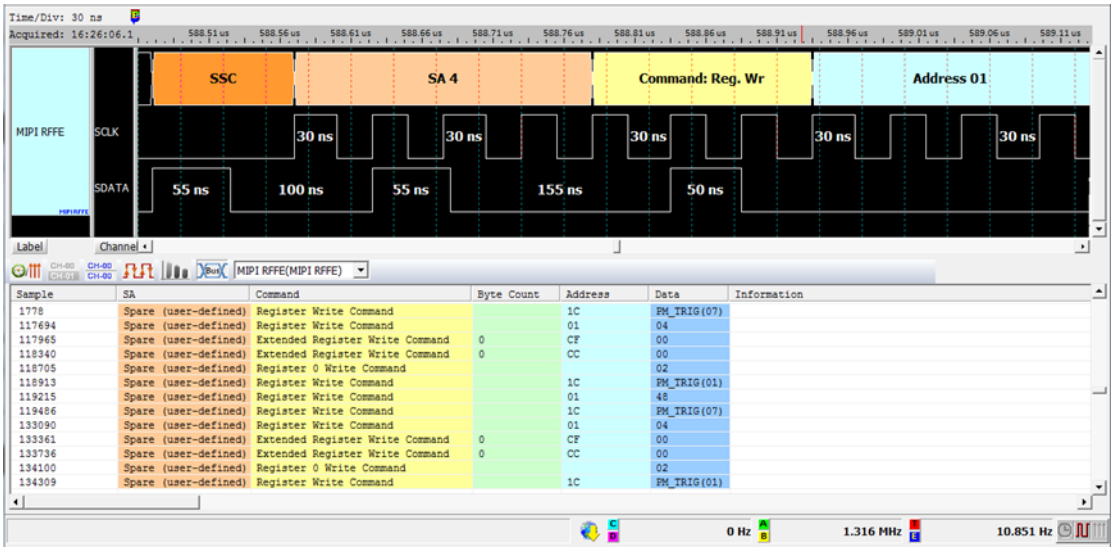
MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

Settings



Channel: Set the channels of SCLK and SDATA.

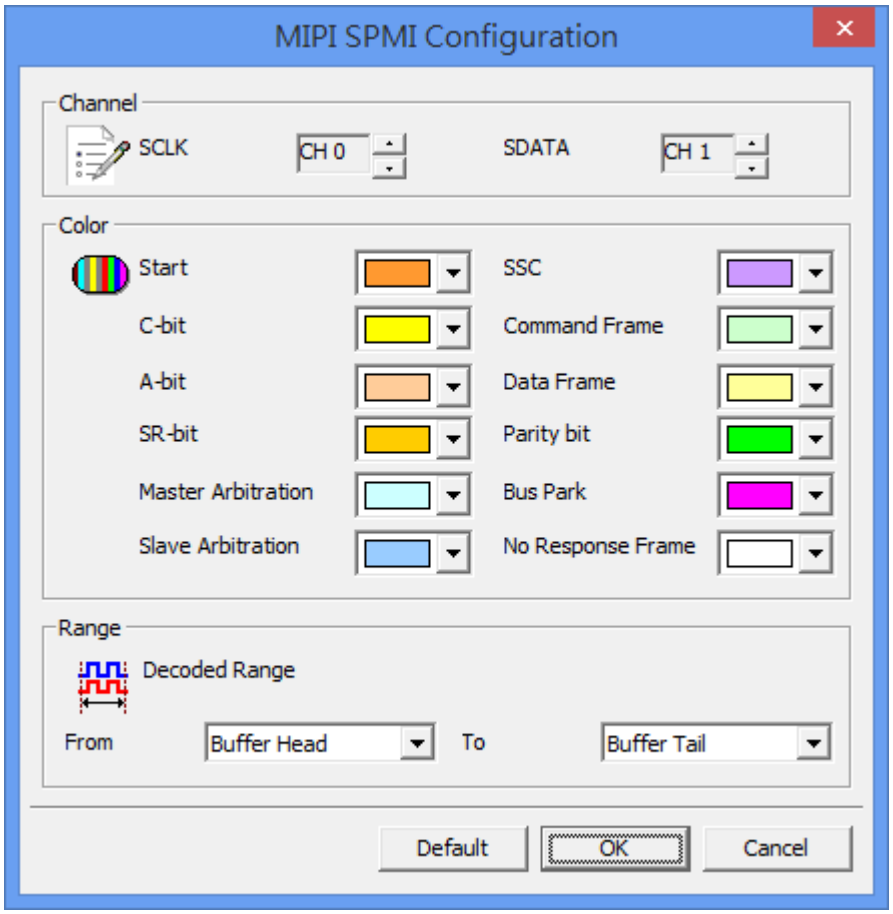
Result



MIPI SPMI

MIPI SPMI(System Power Management Interface) designed by MIPI alliance. SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

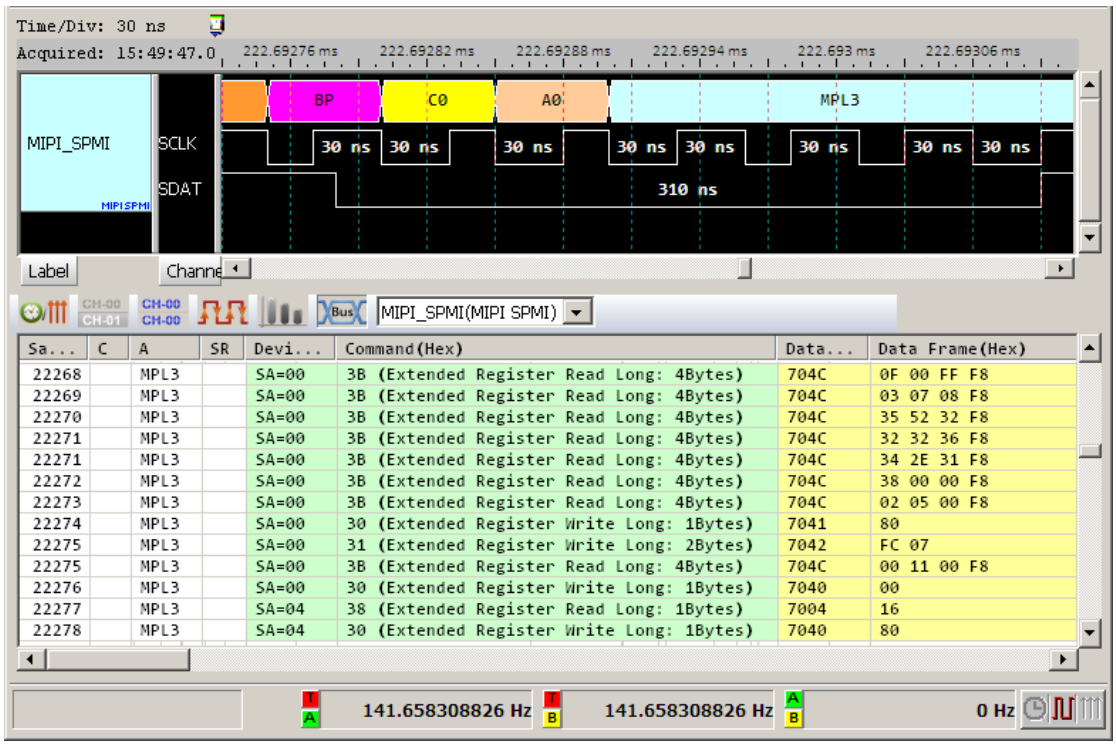
Settings



Channel: Set the channels of SCLK and SDATA.

Result

Click OK to run the MIPI SPMI Decode and see result on the Waveform Windows below.

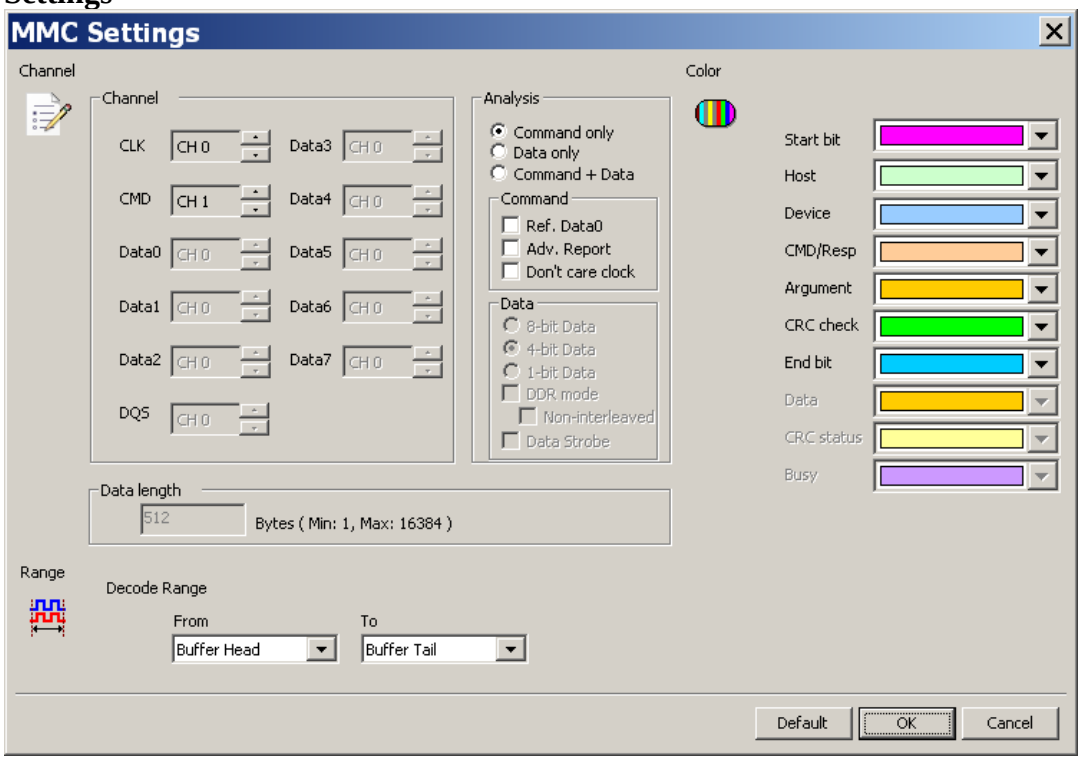


Sa...	C	A	SR	Devi...	Command(Hex)	Data...	Data Frame(Hex)
22268		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	0F 00 FF F8
22269		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	03 07 08 F8
22270		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	35 52 32 F8
22271		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	32 32 36 F8
22271		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	34 2E 31 F8
22272		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	38 00 00 F8
22273		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	02 05 00 F8
22274		MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	7041	80
22275		MPL3		SA=00	31 (Extended Register Write Long: 2Bytes)	7042	FC 07
22275		MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	00 11 00 F8
22276		MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	7040	00
22277		MPL3		SA=04	38 (Extended Register Read Long: 1Bytes)	7004	16
22278		MPL3		SA=04	30 (Extended Register Write Long: 1Bytes)	7040	80

MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC) version 5.0 is a flash memory card standard.

Settings



Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data

Command + Data: Analyze Command and Data in the report window.

Ref. DAT0: To help analyze the R1/R1b of the response.

Adv. Report: To analyze the command argument.

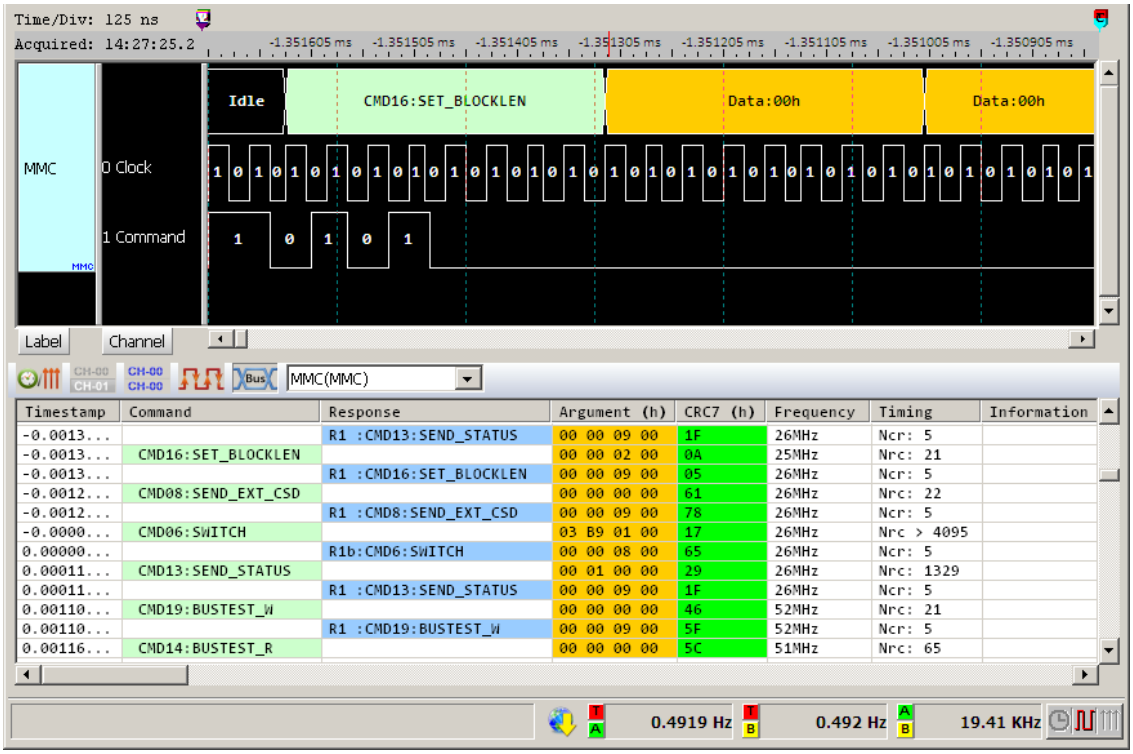
Don't care clock: To decode only depend on the CMD channel without the CLK channel.

Data: 1/4/8 bits or DDR mode, check "DDR mode" and " "Non-interleaved" to analyze data without interleaved. Check "Data Strobe" to analyze data with the DQS channel.

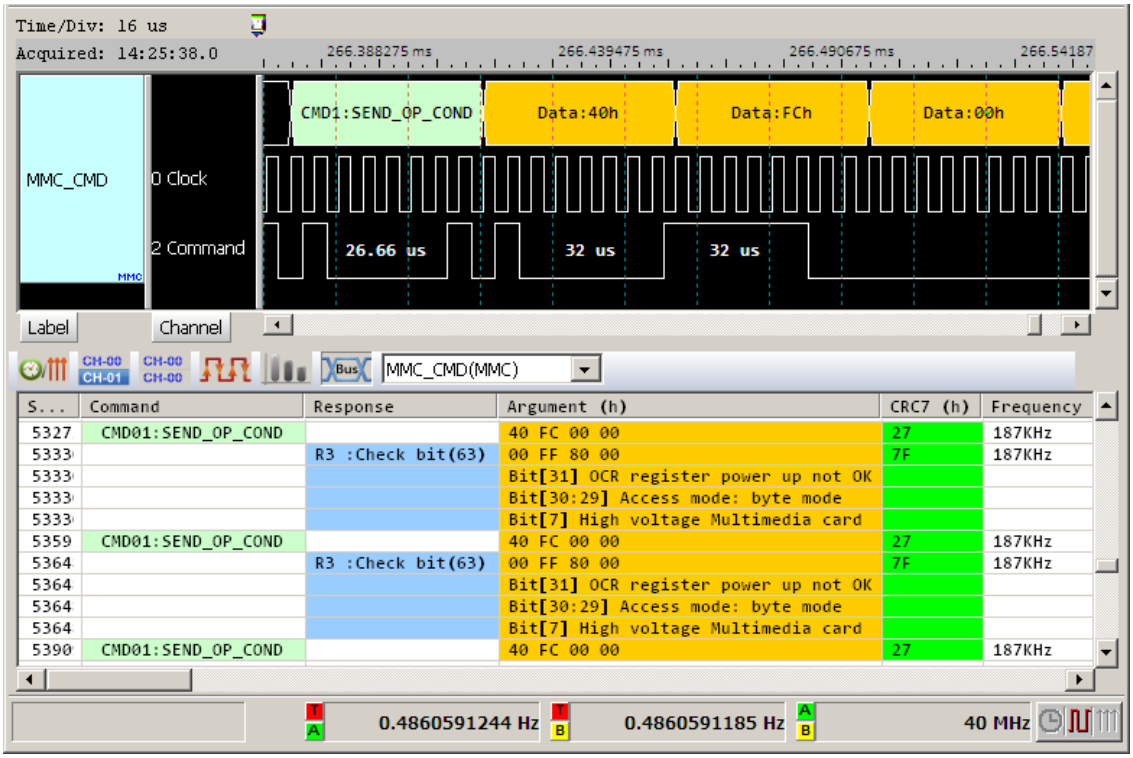
Data length: Set the number of data bits.

Result

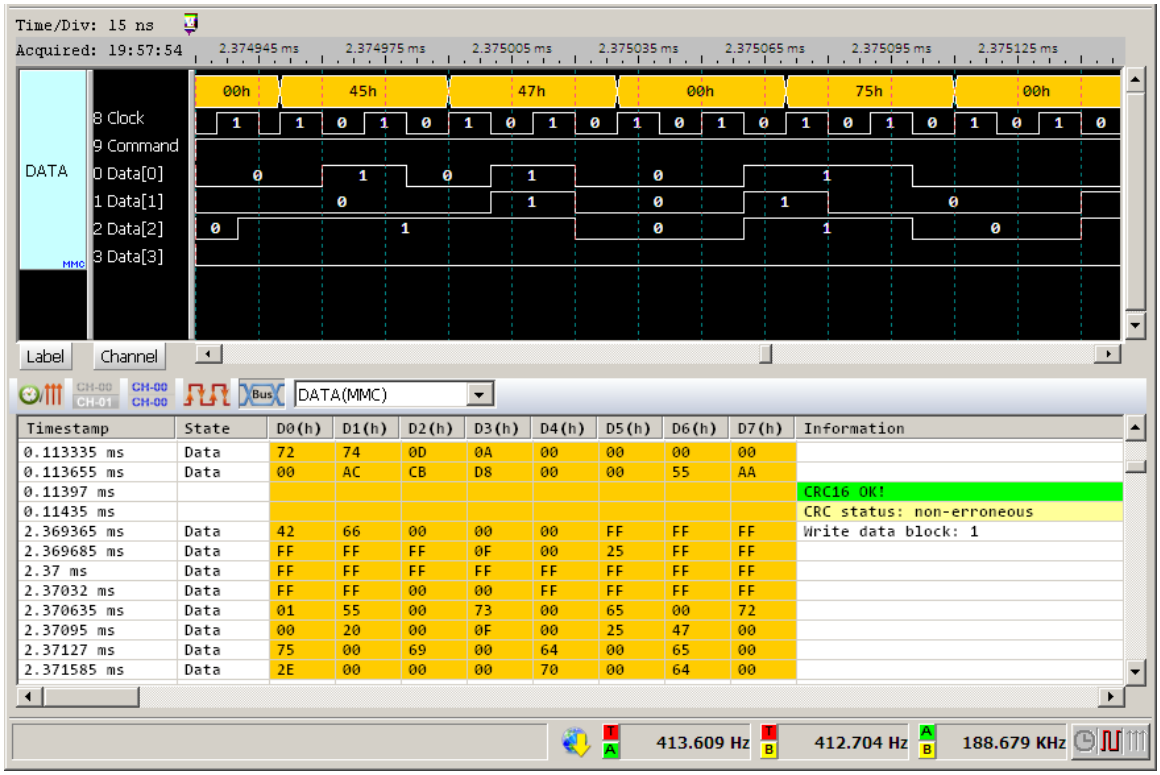
Command:



Adv. Report:



Data:

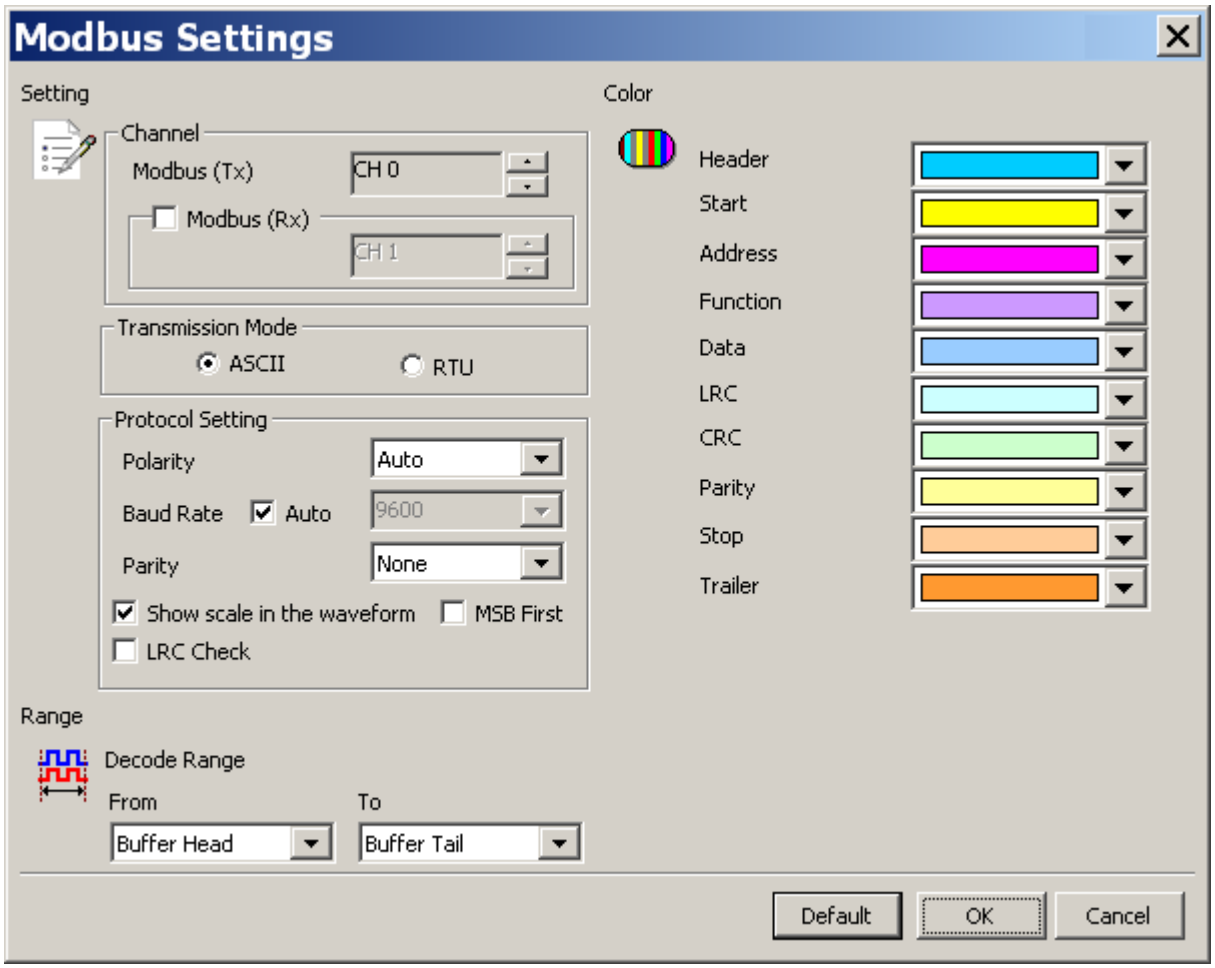


Timestamp	State	D0(h)	D1(h)	D2(h)	D3(h)	D4(h)	D5(h)	D6(h)	D7(h)	Information
0.113335 ms	Data	72	74	0D	0A	00	00	00	00	
0.113655 ms	Data	00	AC	CB	D8	00	00	55	AA	
0.11397 ms										CRC16 OK!
0.11435 ms										CRC status: non-erroneous
2.369365 ms	Data	42	66	00	00	00	FF	FF	FF	Write data block: 1
2.369685 ms	Data	FF	FF	FF	0F	00	25	FF	FF	
2.37 ms	Data	FF	FF	FF	FF	FF	FF	FF	FF	
2.37032 ms	Data	FF	FF	00	00	FF	FF	FF	FF	
2.370635 ms	Data	01	55	00	73	00	65	00	72	
2.37095 ms	Data	00	20	00	0F	00	25	47	00	
2.37127 ms	Data	75	00	69	00	64	00	65	00	
2.371585 ms	Data	2E	00	00	00	70	00	64	00	

ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

Settings



Channel: Modbus (Tx) or Modbus (Rx).

Transmission Mode: ASCII and RTU mode.

Auto: Auto detection idle polarity.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

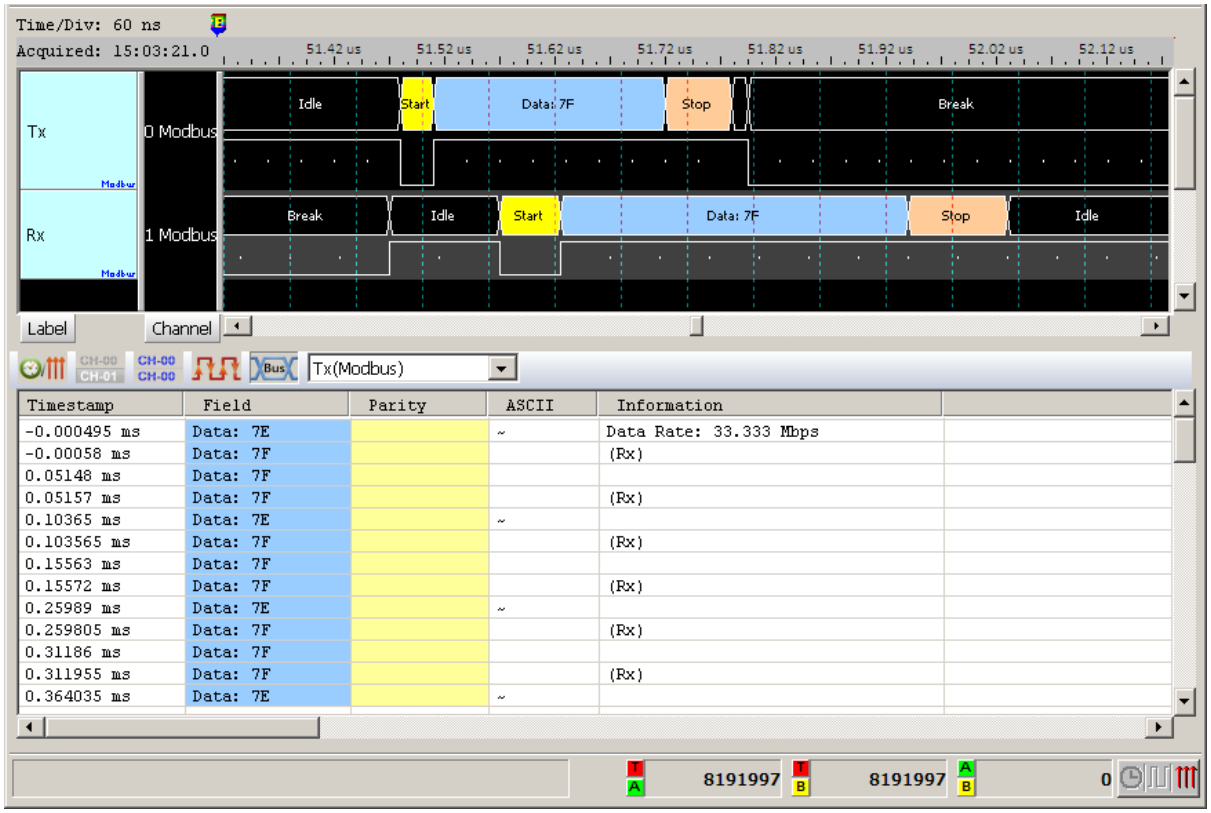
Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Parity: N-None Parity, O-Odd Parity, E-Even Parity.

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Display the waveforms with scales.

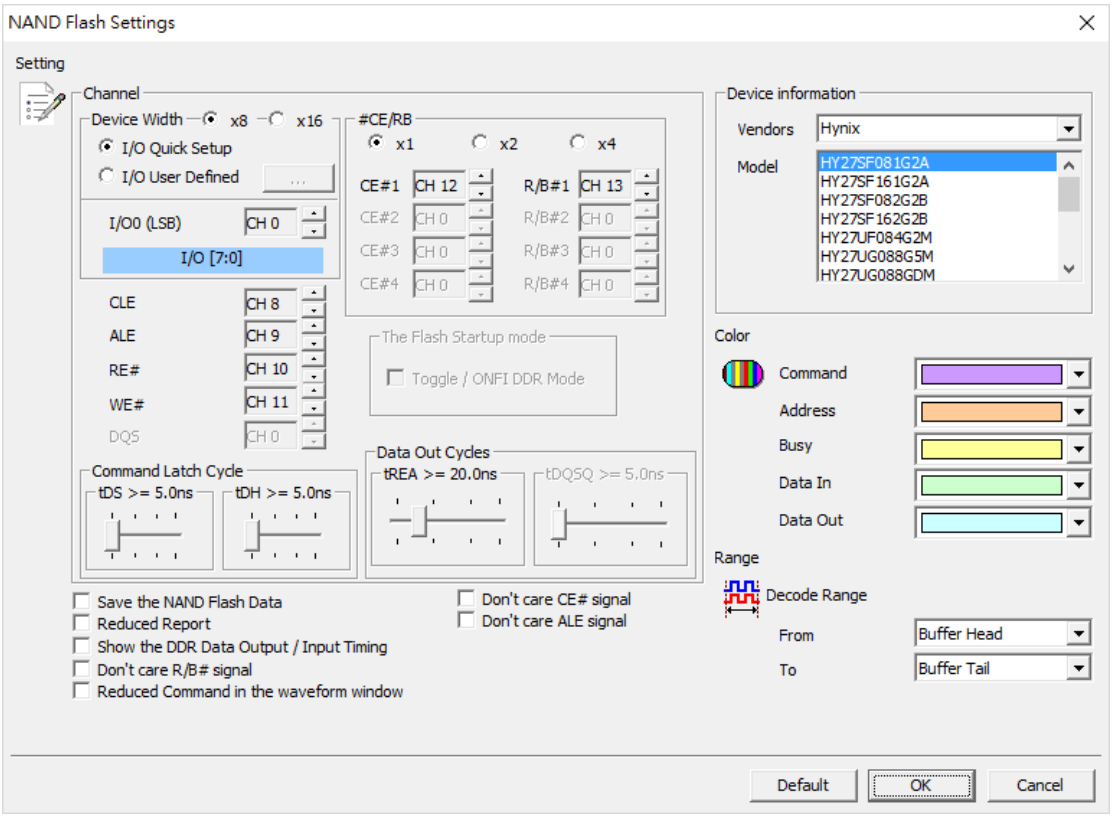
Result



NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB storage devices known as USB flash drives, as well as most memory card formats and solid-state drives available today.

Settings



Channel:

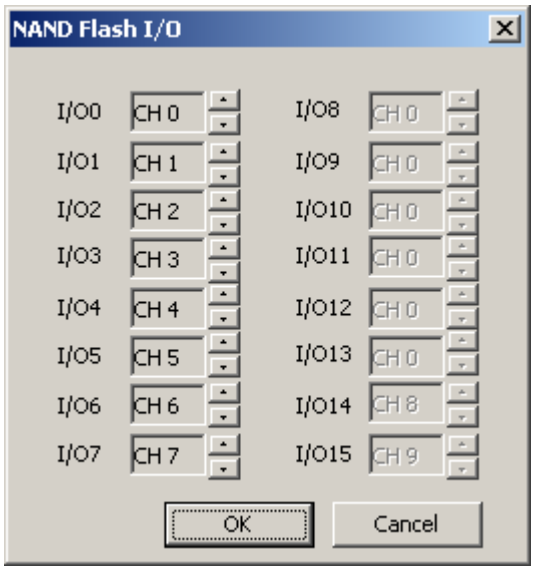
Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel

RE	W/R	Read Enable and Write/Read channel
WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel
CE#	CE#	Chip Enable channel
---	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O Quick Setup, other channels will be set automatically. when check the I/O User Defined and press the button will show the dialog below:



User can set NAND I/O channel by channel.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

tREA / tDQSQ: Set the delay time to access the NAND data under SDR / DDR **Save the NAND Flash Data:** Save the read/write data. Program will save the NAND Flash read/write data as a file when check Save the NAND Flash Data. It will be saved into

the LA work directory.

mode.

Reduced Report: Only show NAND Flash command in the Report window when check it.

Show the DDR Data Output/Input Timing: Only show timing information under DDR mode.

Reduced Command in the waveform window: Only show NAND Command value in the waveform window.

Don't care ALE/RB#/CE# signal: Ignore the signal selected when decode.

Description of file name as following:

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxxh	Row Address
_Colxxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF_DI_Row017821h_Col0000h_CE1_1.bin

NF_DO_Row017821h_Col0000h_CE1_2.bin

NF_DO_Row_Col_CE1_3.bin

Compare the content of file with the one of report.

D0	D1	D2	D3	D4	D5	D6	D7
5A	A6	6F	36	B2	38	B8	B7
06	8A	B7	0B	B1	19	C8	21
7E	CE	58	EF	BD	18	47	7C
5E	DD	9A	E3	A5	E4	02	11
E9	2D	96	14	86	32	CE	F4
53	10	60	79	EA	B6	D6	CE
5A	22	53	A5	F1	9E	DB	58
8A	73	B3	B1	82	19	B9	46
92	25	76	EA	E4	CE	74	A7
1C	E5	20	3D	9F	74	BB	E5
55	54	68	4C	69	86	AC	0F

```
000000  5A A6 6F 36 B2 38 B8 B7  06 8A B7 0B B1 19 C8 21
000010  7E CE 58 EF BD 18 47 7C  5E DD 9A E3 A5 E4 02 11
000020  E9 2D 96 14 86 32 CE F4  53 10 60 79 EA B6 D6 CE
000030  5A 22 53 A5 F1 9E DB 58  8A 73 B3 B1 82 19 B9 46
000040  92 25 76 EA E4 CE 74 A7  1C E5 20 3D 9F 74 BB E5
000050  55 54 68 4C 69 86 AC 0F  F1 A2 47 FA 37 4B 04 0D
```

Device information

Vendors: Select the NAND Flash Vendor. Please refer to the following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a **AqNFCustom.txt** file into the LA work directory when select the **Custom** vendor item and edit NAND Flash Command set.

```
Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , , Y, N, Y, 70
Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10
```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description
Manufacturer	NAND Flash Vendor.
PartNo	NAND Flash IC Model.
#CE/RB	Number of targets, only 1/2/4 acceptable.
X16	8/16 bits device width, only Y/N acceptable.
SyncMode	Only Y/N acceptable, Y: Synchronous data interface supported; N: Not supported.
	Cmd is composed of several parts, it's divided with comma.
	1. Complete command name.

	2. Abbreviation of command.
	Name of first busy time check. Put a space and add a comma if unused.
	Value of first busy time check. Its unit is micro seconds. Put a space and add a comma if unused.
	Name of second busy time check. Put a space and add a comma if unused.
	Value of second busy time check. Its unit is micro mseconds. Put a space and add a comma if unused.
	First flag. It's acceptable command during busy.
	Second flag. It can be inserted by some command or not.
	Third flag. It can insert into some multi plane command or not.
	Command.

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,

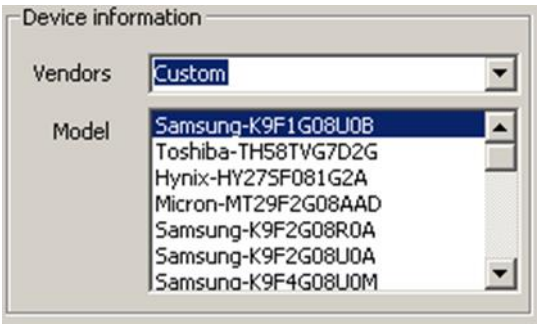
N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

Read Stat. / TPP Prog. : abbreviation of command.

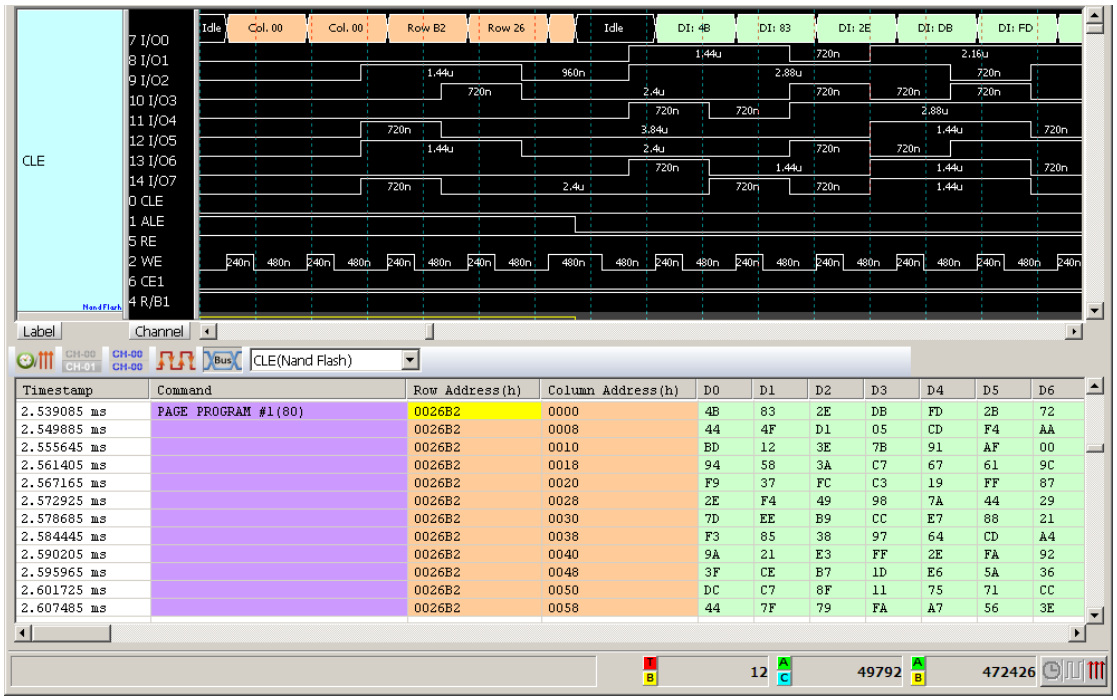
Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is 5000 us. It will show some information when violation of busy time.

3 Flags: 1st flag of "Read Status" is Y means it's acceptable command During busy; 2nd flag of "Two-Plane Page Program" and 3rd flag of "Read Status" means any command between 11h and 81h is prohibited except "Read Status (70h)".

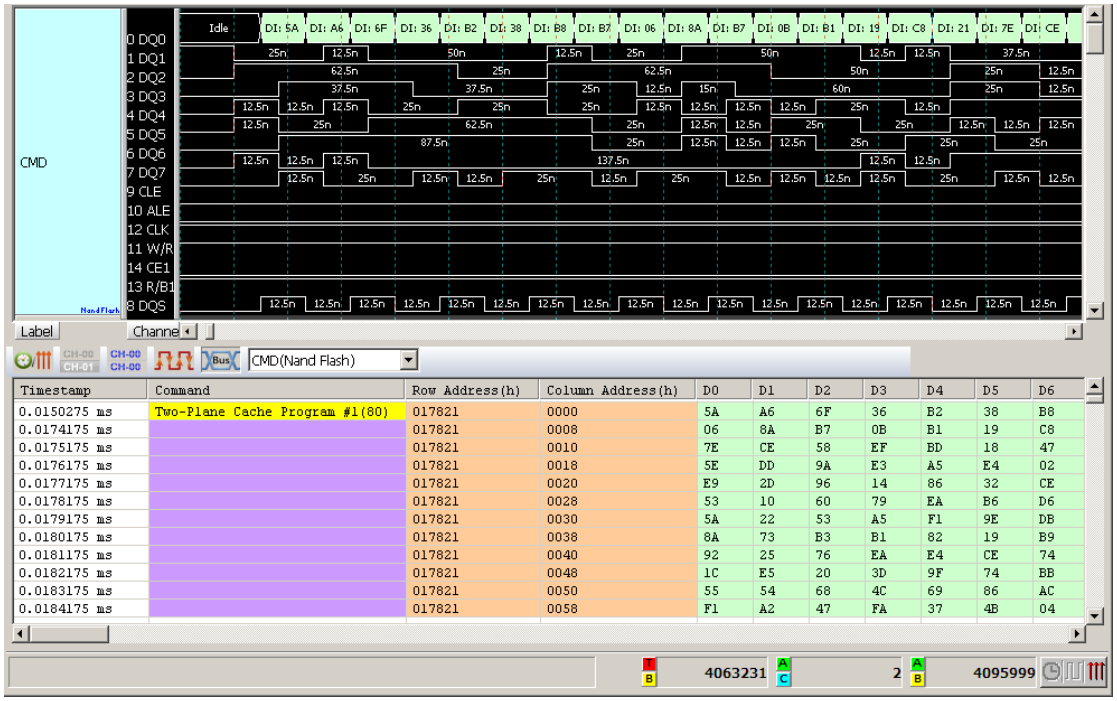


Result

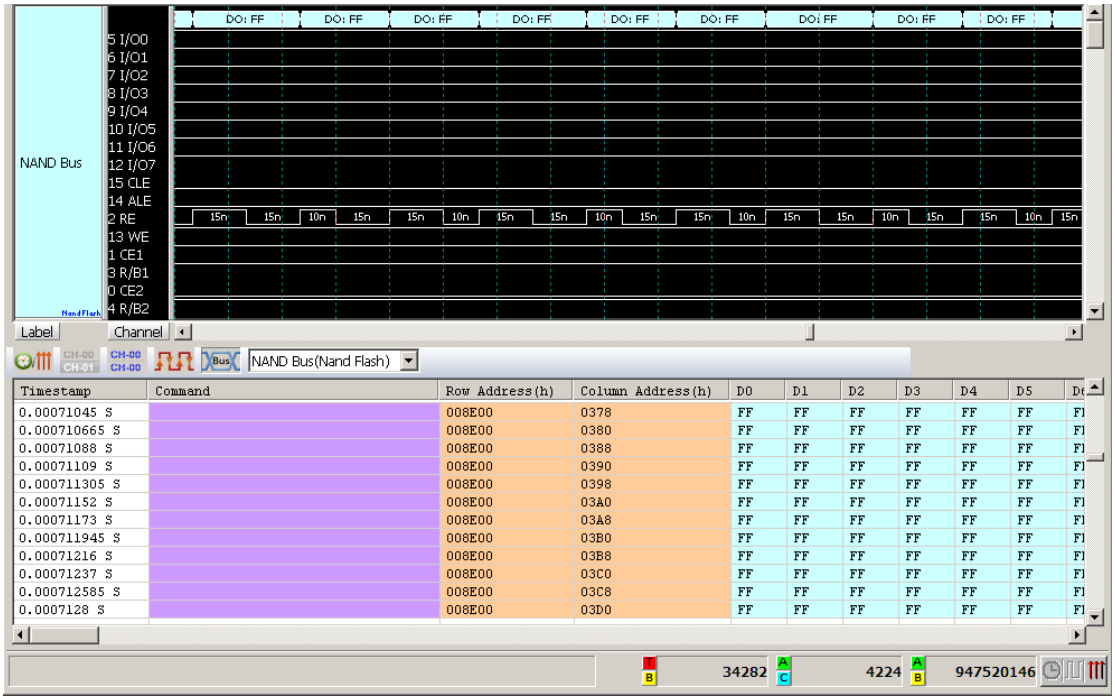
SDR Data In



DDR Data Out



CE x 2 Data Out

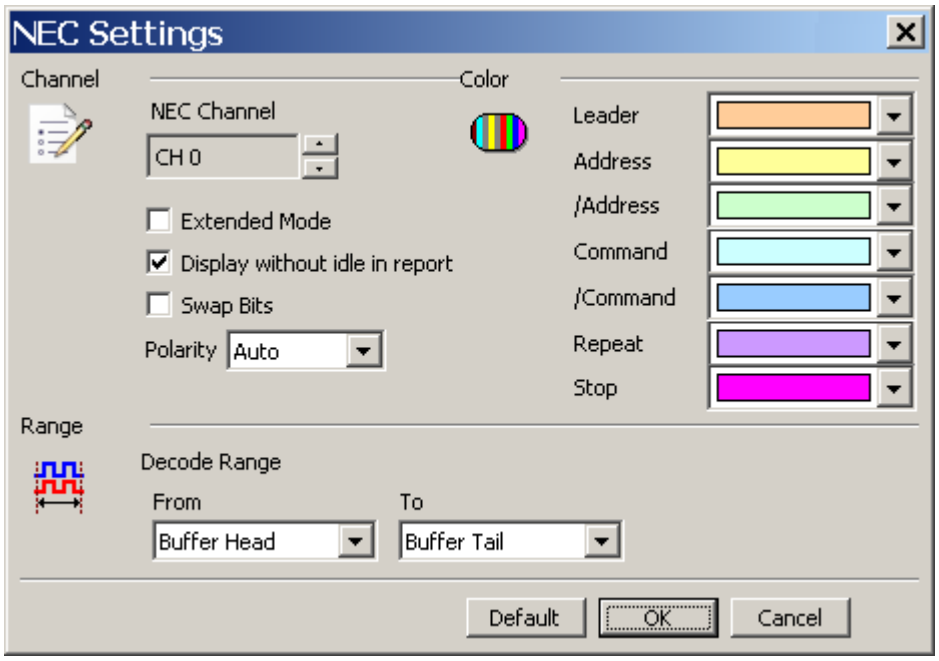


Timestamp	Command	Row Address(h)	Column Address(h)	D0	D1	D2	D3	D4	D5	D6
0.00071045 S		008E00	0378	FF	FF	FF	FF	FF	FF	FF
0.00070665 S		008E00	0380	FF	FF	FF	FF	FF	FF	FF
0.00071088 S		008E00	0388	FF	FF	FF	FF	FF	FF	FF
0.00071109 S		008E00	0390	FF	FF	FF	FF	FF	FF	FF
0.00071305 S		008E00	0398	FF	FF	FF	FF	FF	FF	FF
0.00071152 S		008E00	03A0	FF	FF	FF	FF	FF	FF	FF
0.00071173 S		008E00	03A8	FF	FF	FF	FF	FF	FF	FF
0.00071945 S		008E00	03B0	FF	FF	FF	FF	FF	FF	FF
0.00071216 S		008E00	03B8	FF	FF	FF	FF	FF	FF	FF
0.00071237 S		008E00	03C0	FF	FF	FF	FF	FF	FF	FF
0.00071258 S		008E00	03C8	FF	FF	FF	FF	FF	FF	FF
0.0007128 S		008E00	03D0	FF	FF	FF	FF	FF	FF	FF

NEC IR

It needs only one channel to analysis NEC signals.

Settings



Channel: Display the channel (CH 0).

Extended Mode: It integrates /Address and Address into 16 Bits Address, /Command and Command into 16 Bits Command.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Swap Bits: Switch LSB First to MSB First.

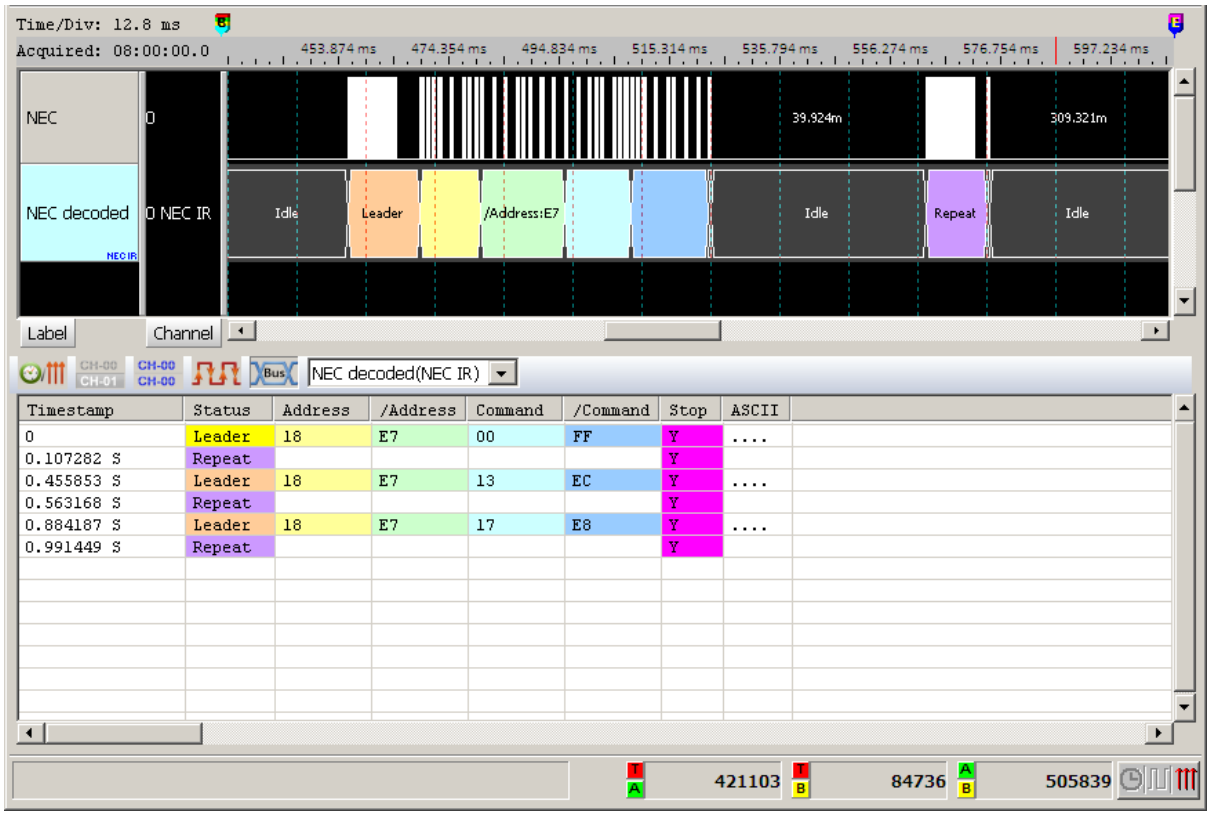
Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Result

Click **OK** to run the NEC IR decode and see the result on the Waveform Window below.

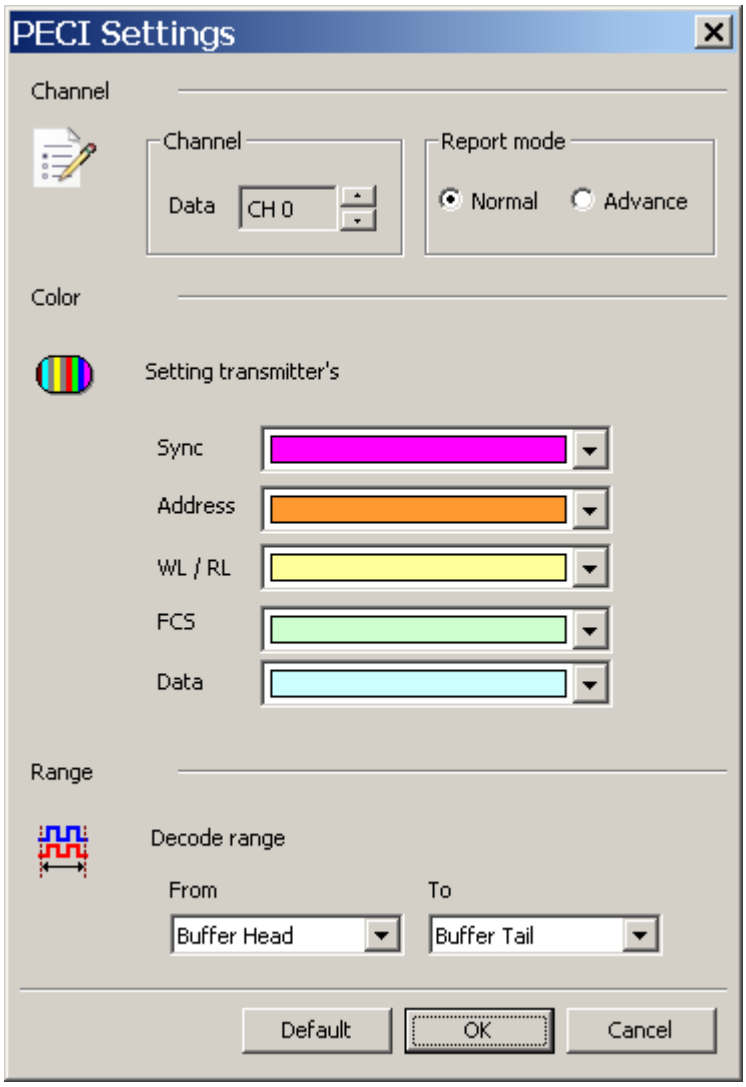


Timestamp	Status	Address	/Address	Command	/Command	Stop	ASCII
0	Leader	18	E7	00	FF	Y	....
0.107282 S	Repeat					Y	
0.455853 S	Leader	18	E7	13	EC	Y	....
0.563168 S	Repeat					Y	
0.884187 S	Leader	18	E7	17	E8	Y	....
0.991449 S	Repeat					Y	

PECI

Platform Environment Control Interface, Platform management include thermal, power and electrical error monitoring.

Settings

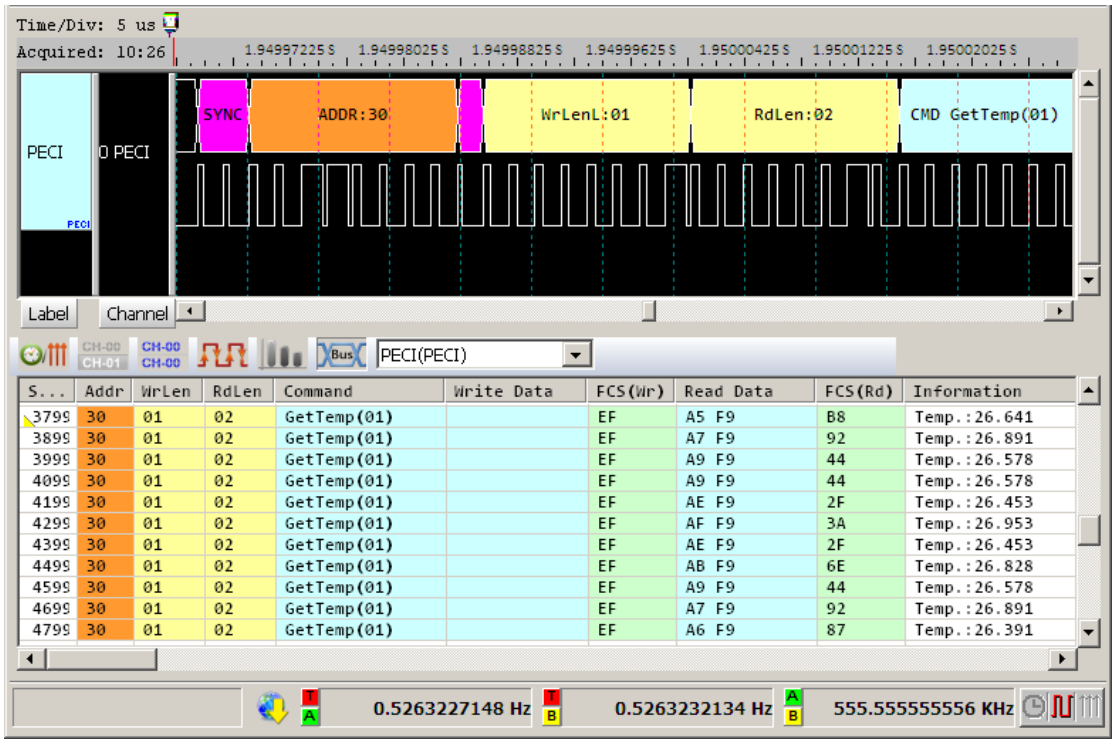


Channel: Show the selected channels.

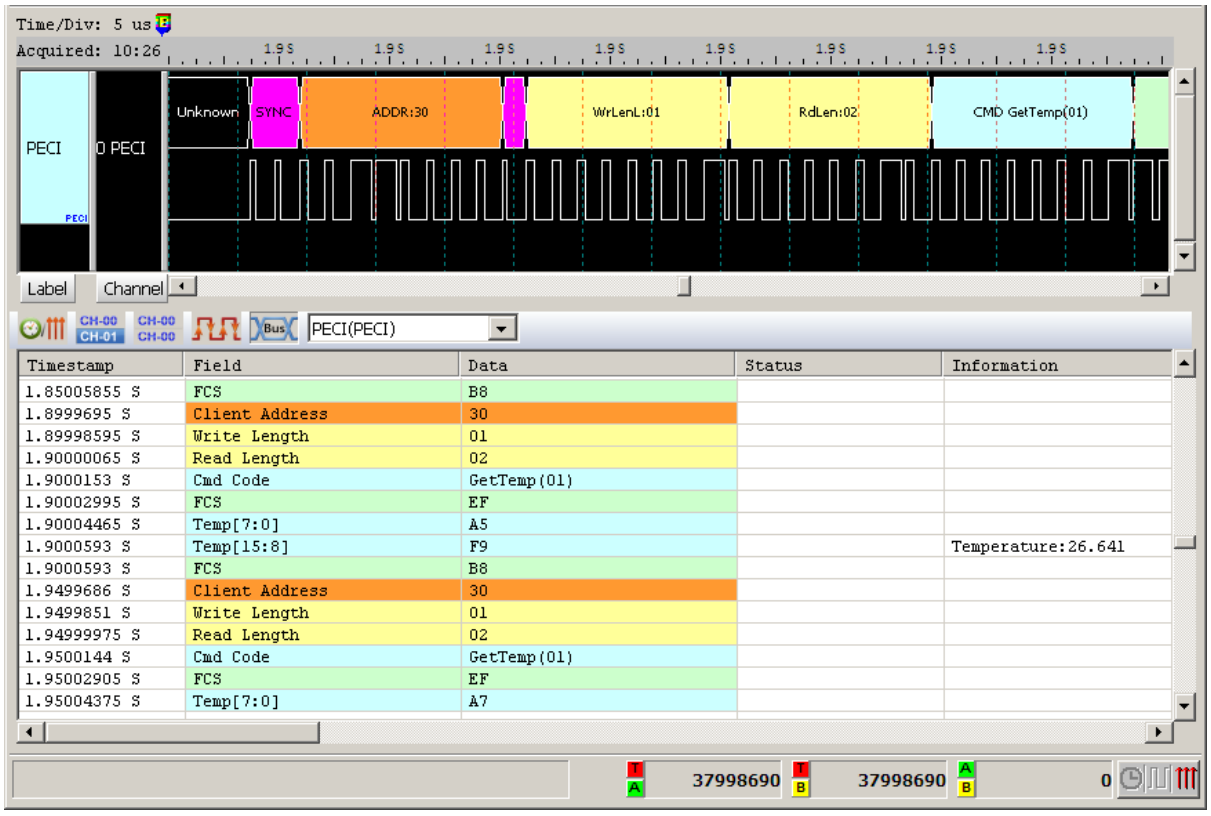
Report mode: Normal or Advance

Result

Normal mode



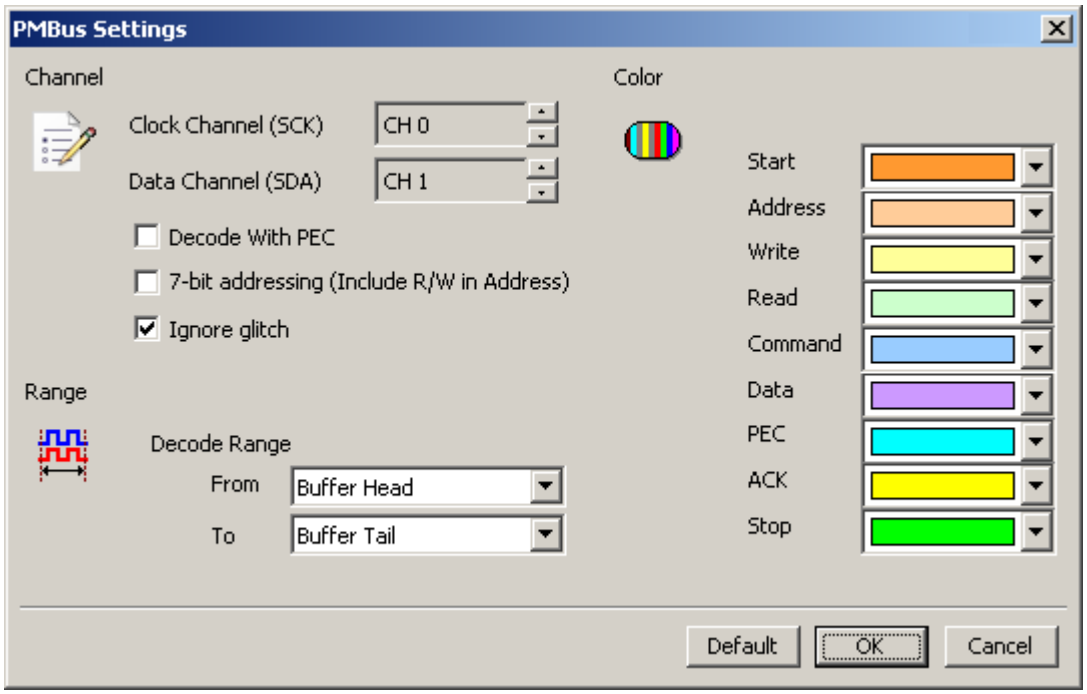
Advance mode



PMBus

The Power Management Bus (“PMBus”) is an open standard protocol that defines a means of communicating with power conversion and other devices.

Settings



Channel: Show the selected channels.

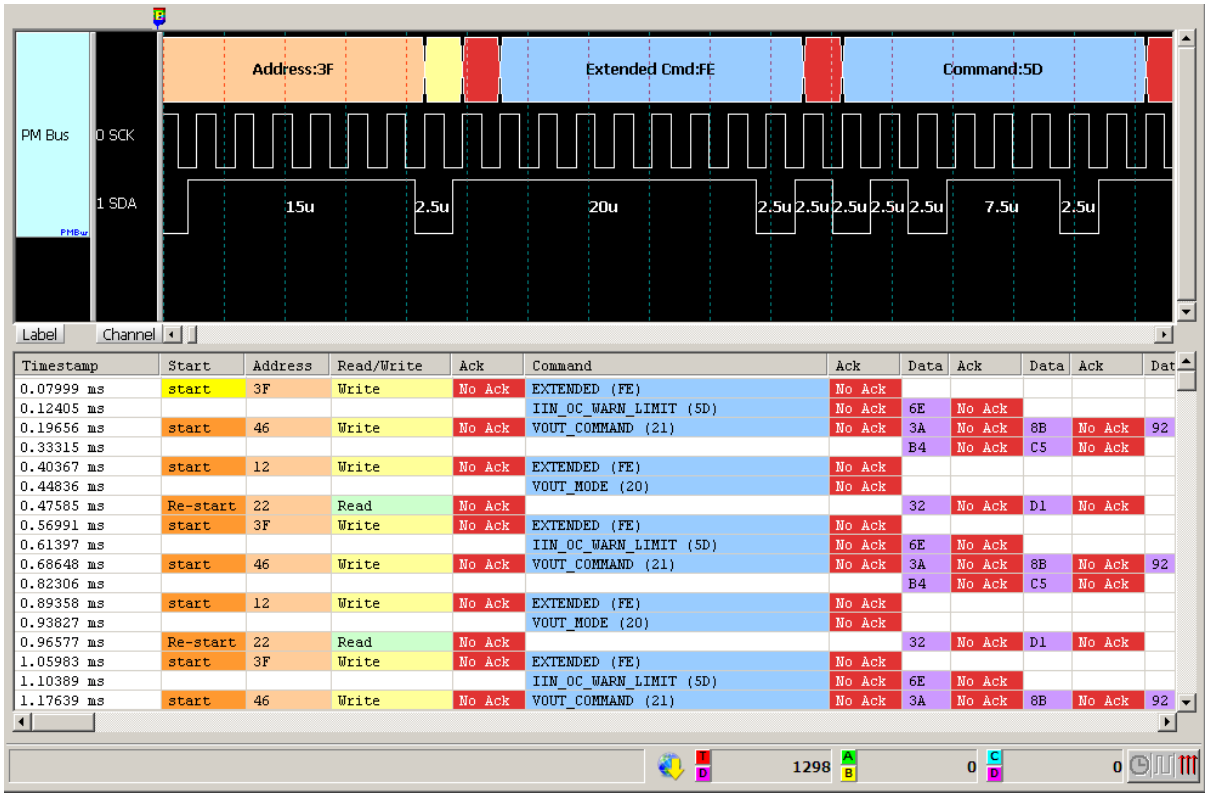
Decode With PEC: Group command protocol with PEC.

7-bit addressing (Include R/W in address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click **OK** to run the PMBus decode and see the result on the Waveform Window below.

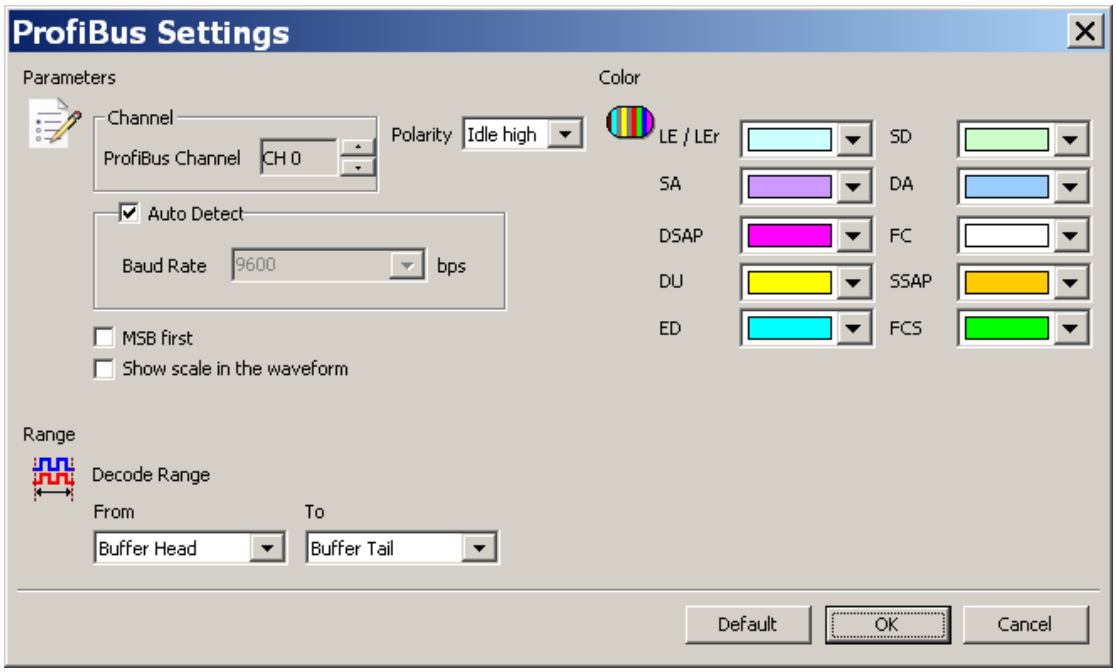


Timestamp	Start	Address	Read/Write	Ack	Command	Ack	Data	Ack	Data	Ack	Dat
0.07999 ms	start	3F	Write	No Ack	EXTENDED (FE)	No Ack					
0.12405 ms					IIN_OC_WARN_LIMIT (5D)	No Ack	6E	No Ack			
0.19656 ms	start	46	Write	No Ack	VOUT_COMMAND (21)	No Ack	3A	No Ack	8B	No Ack	92
0.33315 ms							B4	No Ack	C5	No Ack	
0.40367 ms	start	12	Write	No Ack	EXTENDED (FE)	No Ack					
0.44836 ms					VOUT_MODE (20)	No Ack					
0.47585 ms	Re-start	22	Read	No Ack			32	No Ack	D1	No Ack	
0.56991 ms	start	3F	Write	No Ack	EXTENDED (FE)	No Ack					
0.61397 ms					IIN_OC_WARN_LIMIT (5D)	No Ack	6E	No Ack			
0.68648 ms	start	46	Write	No Ack	VOUT_COMMAND (21)	No Ack	3A	No Ack	8B	No Ack	92
0.82306 ms							B4	No Ack	C5	No Ack	
0.89358 ms	start	12	Write	No Ack	EXTENDED (FE)	No Ack					
0.93827 ms					VOUT_MODE (20)	No Ack					
0.96577 ms	Re-start	22	Read	No Ack			32	No Ack	D1	No Ack	
1.05983 ms	start	3F	Write	No Ack	EXTENDED (FE)	No Ack					
1.10389 ms					IIN_OC_WARN_LIMIT (5D)	No Ack	6E	No Ack			
1.17639 ms	start	46	Write	No Ack	VOUT_COMMAND (21)	No Ack	3A	No Ack	8B	No Ack	92

ProfiBus

ProfiBus (PROcess Field Bus) is implemented by RS485. It includes PROFIBUS DP, PROFIBUS PA and PROFIBUS FMS.

Settings



Channel: Set the ProfiBus Channel

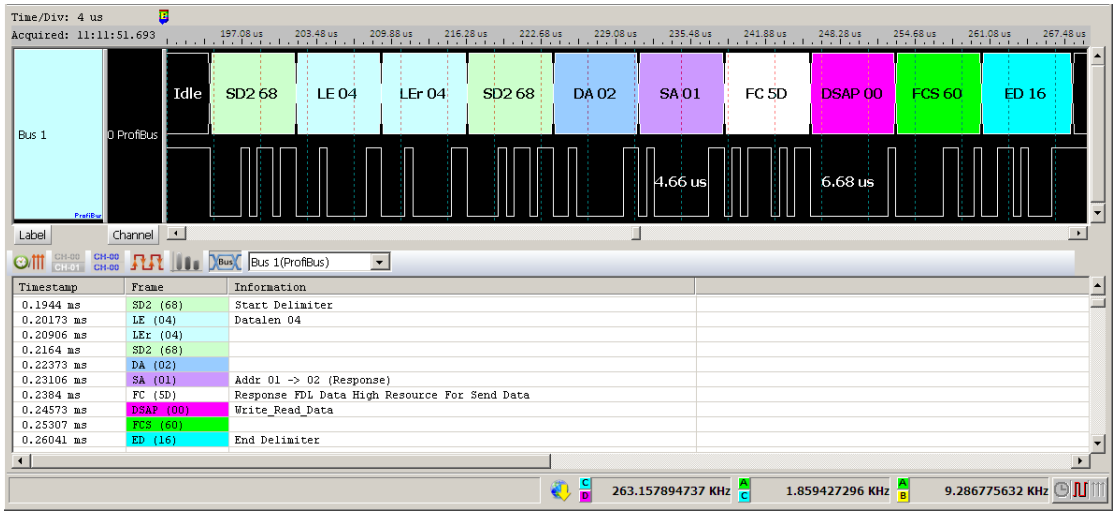
Polarity: Set the polarity Idle high / Idle low

Baud Rate/Auto Detect: Set the baud rate manually or auto detect

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section

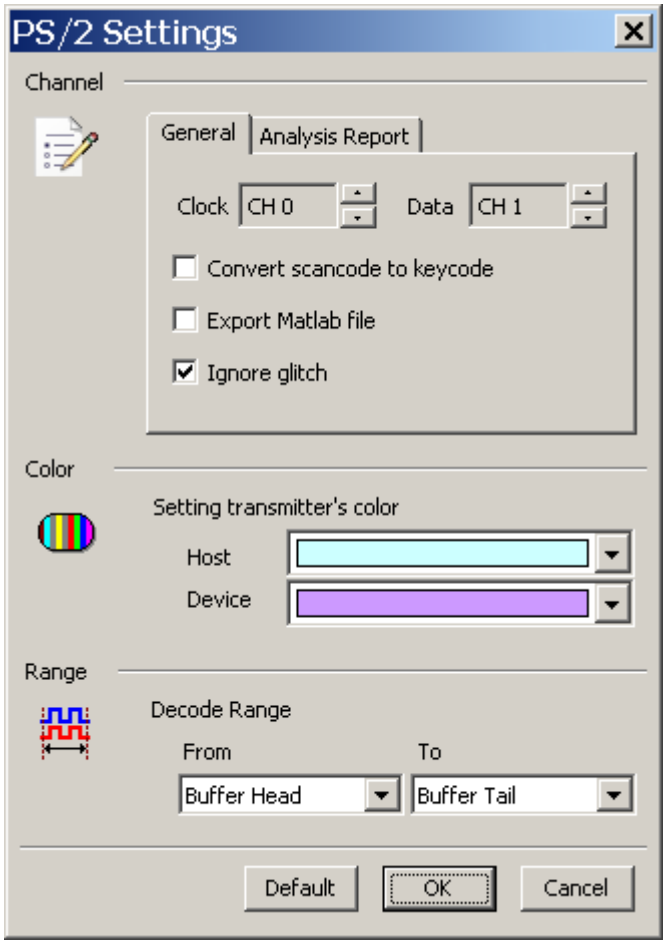
Result



PS/2

The Personal System/2 (PS/2) protocol has 6 data bits, but only the first bit (Data) and the fifth bit (Clock) need to be analyzed.

PS/2 Settings



Channel: Show the selected channels.

Convert scan code to key code: Transform data into keyboard characters.

Export MATLAB file: Export the data with MATLAB format as the following:

Time = [25.78484 25.785985 …]

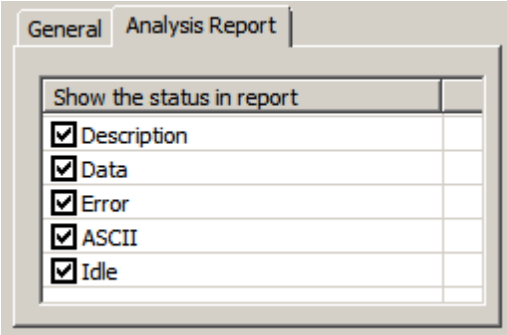
Description = [DH DH …] DH = Device to Host, HD = Host to Device

Data = [58 FA 02 FA C4 …]

The file (PS2_Matlab.m) will be saved at work directory

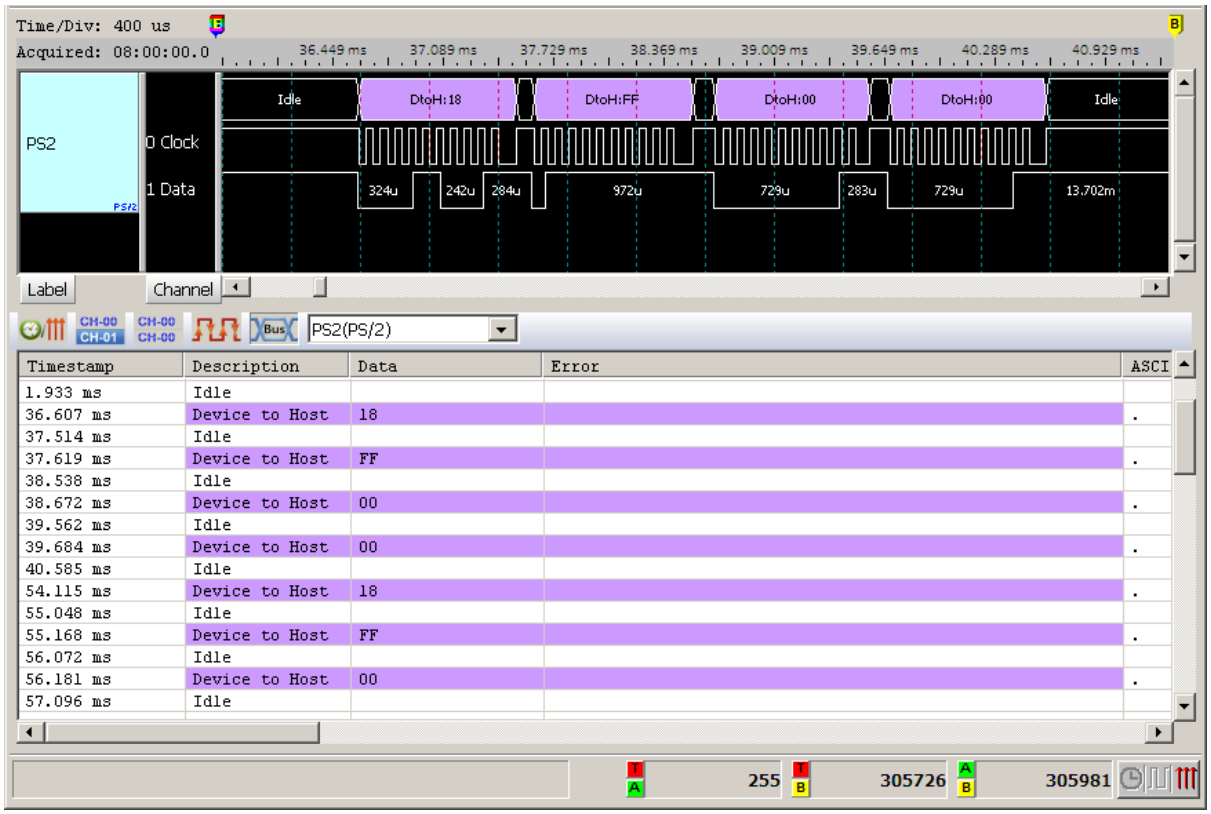
Ignore glitch: Ignore the glitch when the slow transitions.

Analysis Report: Show the selected status in report.



Result

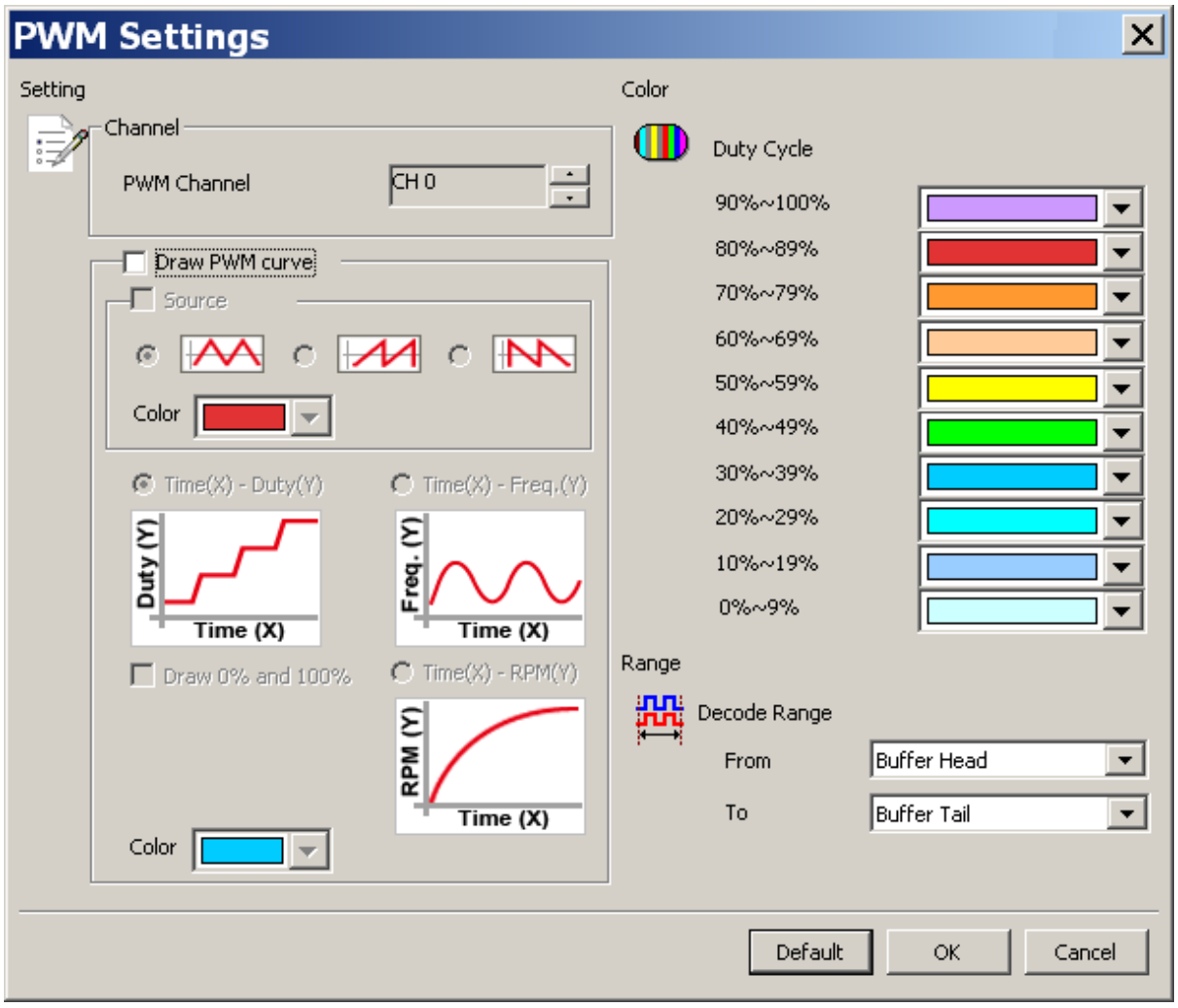
Click **OK** to run the PS/2 decode and see the result on the Waveform Window below.



PWM

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

Settings



Channel: Show the selected channel.

Draw PWM curve:

Source: Show the source waveform of the PWM.

Time(X)-Duty(Y): Show the curve diagram with Time(X) and Duty(Y)

Time(X)-Freq.(Y): Show the curve diagram with Time(X) and Freq.(Y)

Time(X)-RPM(Y): Show the curve diagram with Time(X) and RPM(Y)

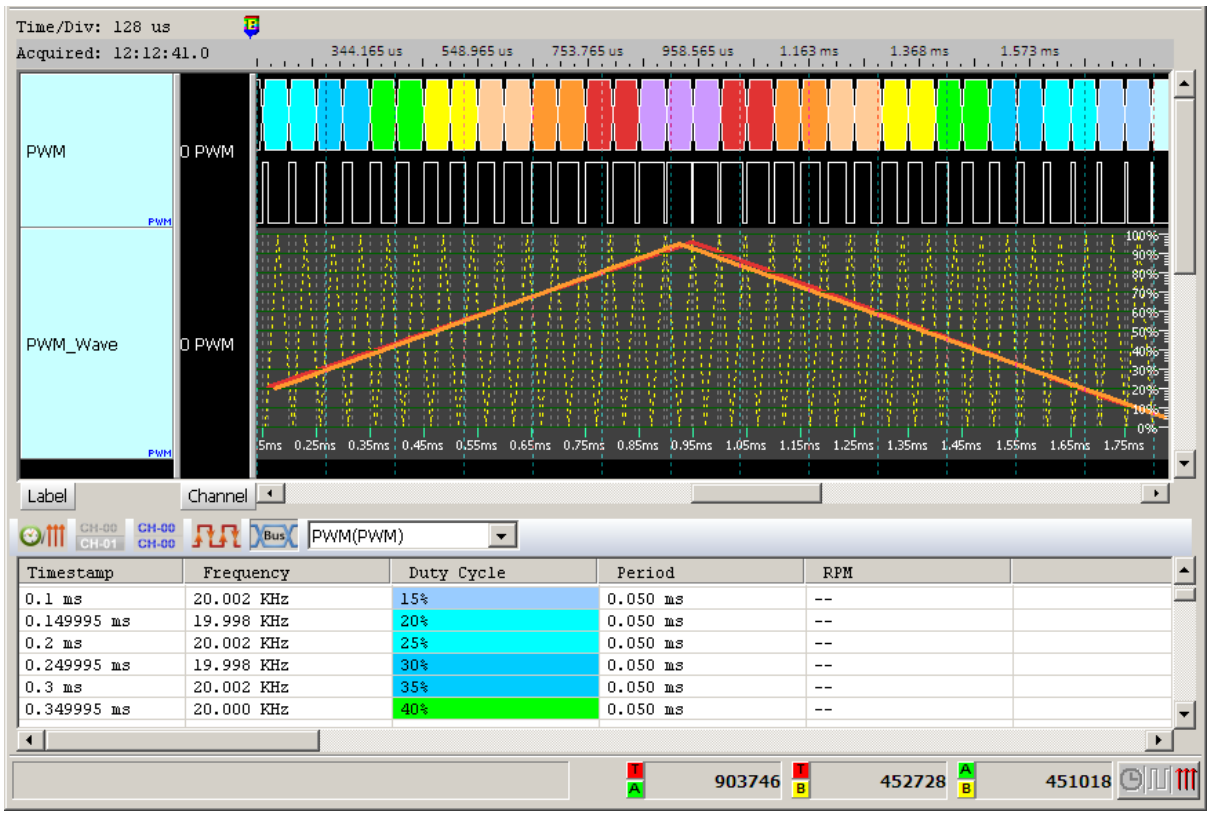
Draw 0% and 100%: When select the Time(X)-Duty(Y) drawing and check Draw 0% and 100%, the program will draw this duty curve of 0% or 100%; it will draw this duty curve of 0% or 100% when uncheck Draw 0% and 100%.

Draw 0 Hz: When select the Time(X)-Freq.(Y) drawing and check the item Draw 0 Hz, will show the Frequency from 0 Hz at Y axis.

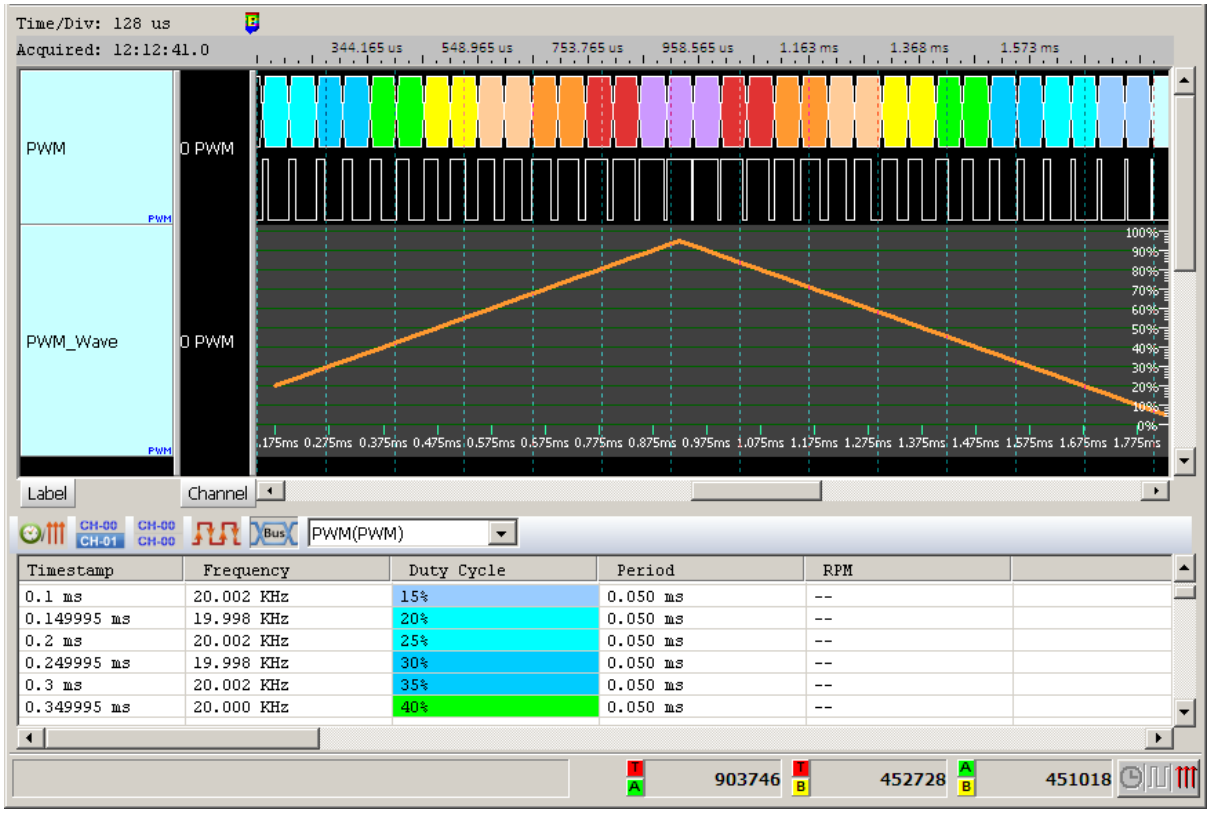
Result

Click **OK** to run the PWM decode and see the result on the Waveform Window below.

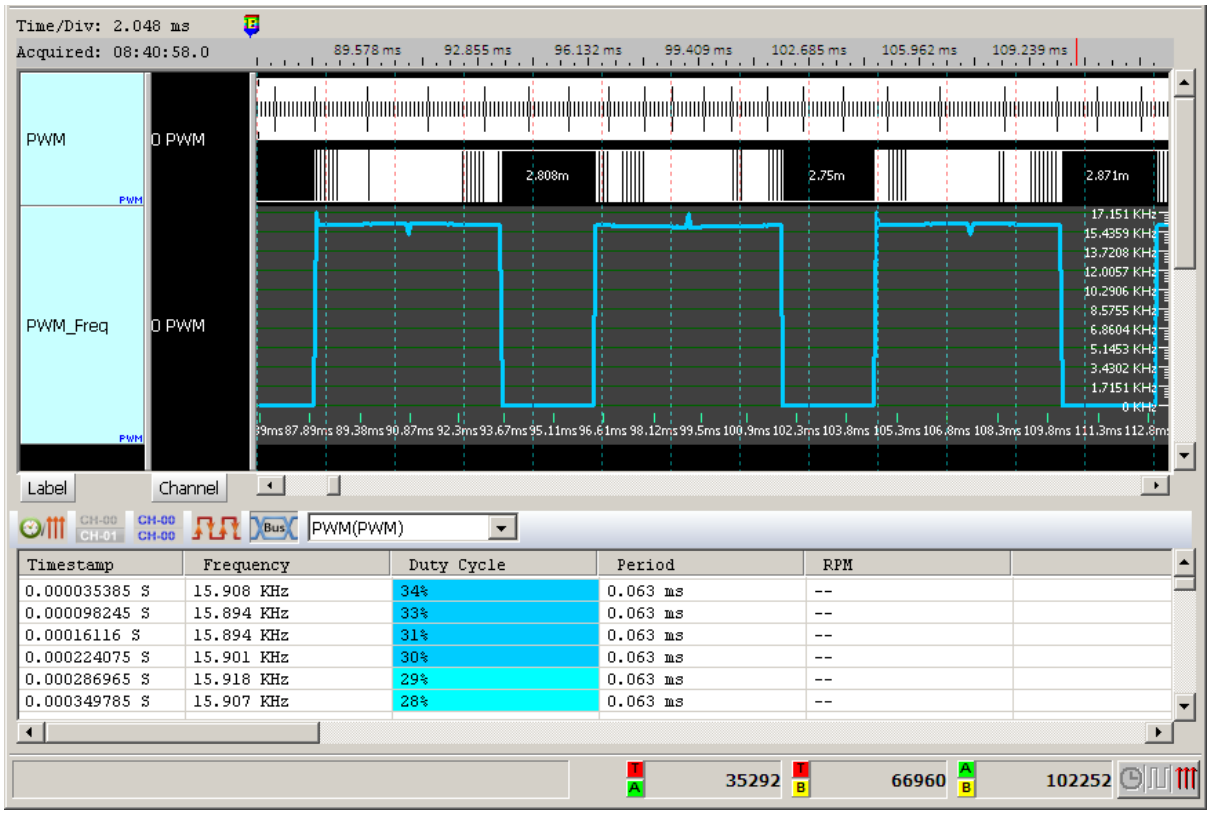
Select “Source”



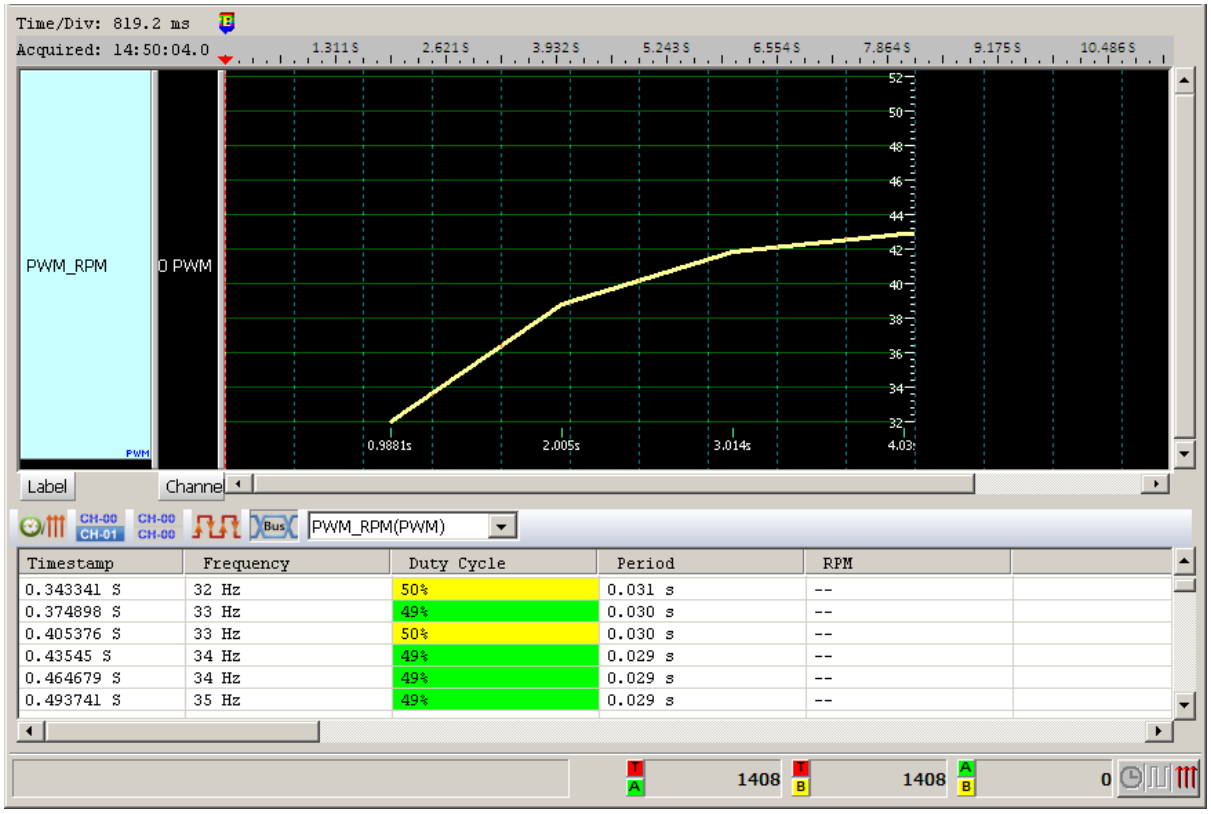
Select Time(X)-Duty(Y)



Select Time(X)-Freq.(Y)



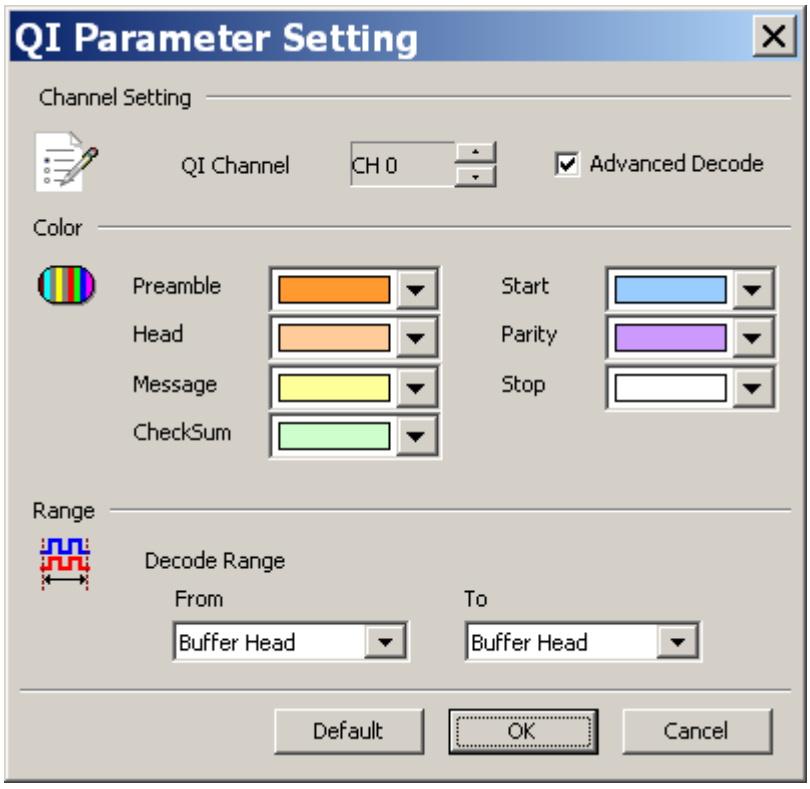
Select Time(X)-RPM(Y)



QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

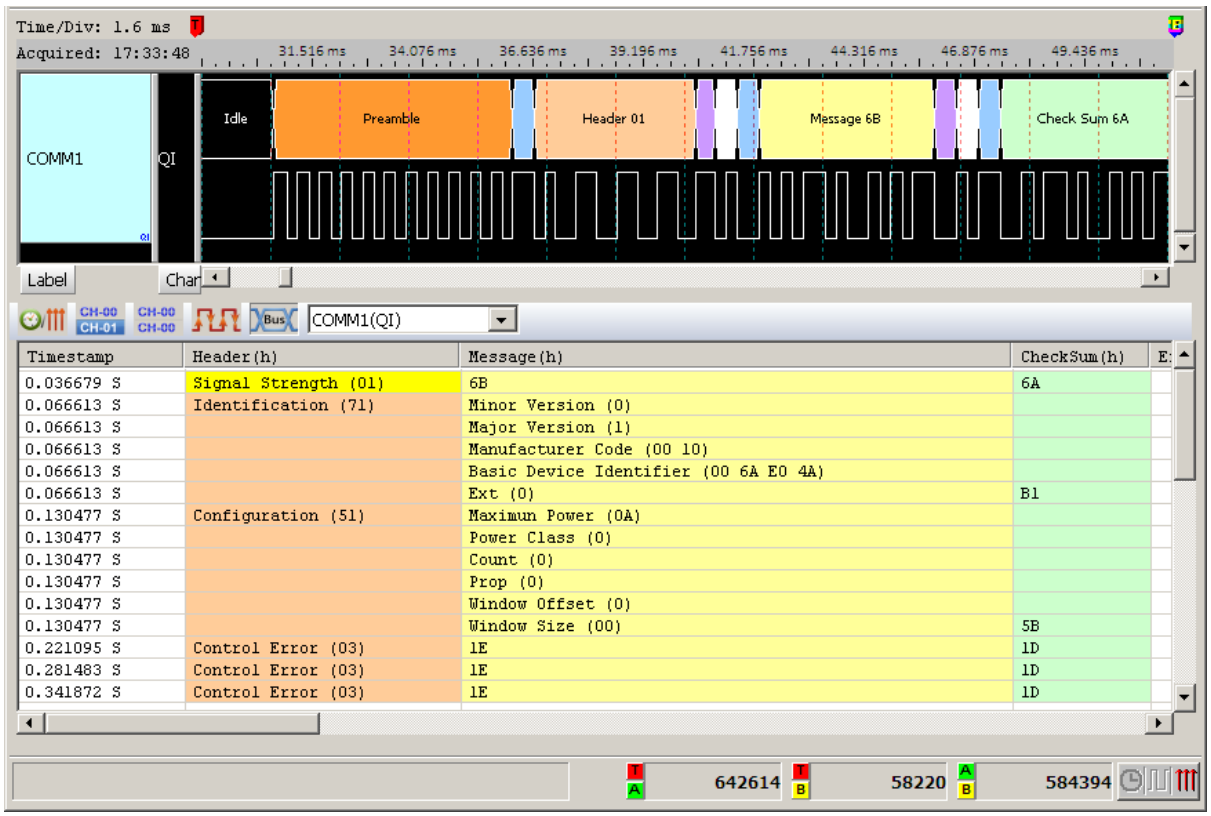
Settings



QI Channel: Show the selected channel.

Advance Decode: show detail message decode

Result

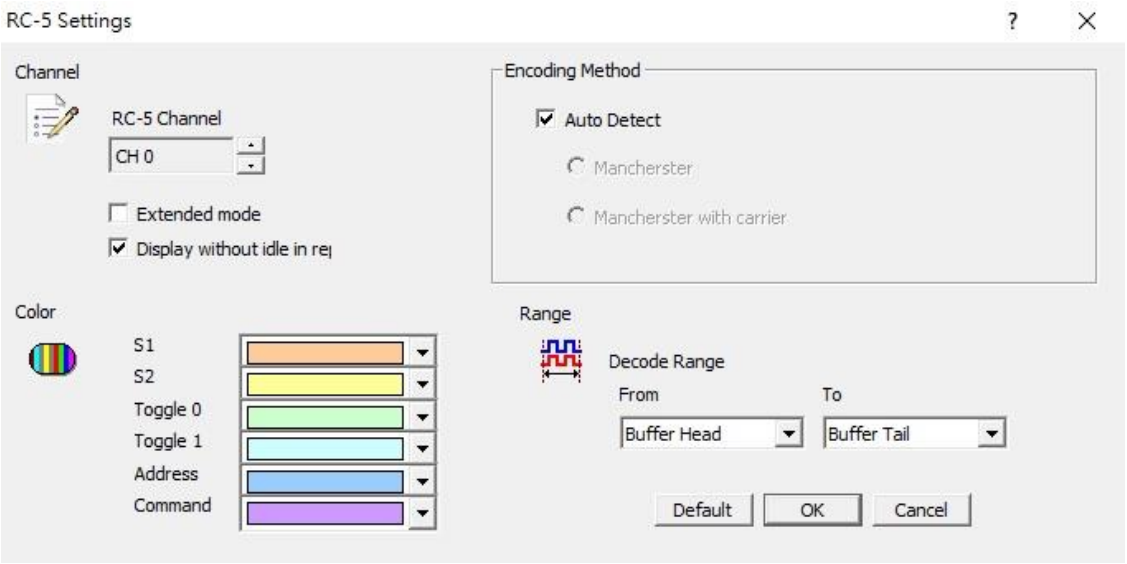


Timestamp	Header(h)	Message(h)	CheckSum(h)	E:
0.036679 S	Signal Strength (01)	6B	6A	
0.066613 S	Identification (71)	Minor Version (0)		
0.066613 S		Major Version (1)		
0.066613 S		Manufacturer Code (00 10)		
0.066613 S		Basic Device Identifier (00 6A E0 4A)		
0.066613 S		Ext (0)	B1	
0.130477 S	Configuration (51)	Maximun Power (0A)		
0.130477 S		Power Class (0)		
0.130477 S		Count (0)		
0.130477 S		Prop (0)		
0.130477 S		Window Offset (0)		
0.130477 S		Window Size (00)	5B	
0.221095 S	Control Error (03)	1E	1D	
0.281483 S	Control Error (03)	1E	1D	
0.341872 S	Control Error (03)	1E	1D	

RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

Settings



Channel: Show the selected channel (CH 0).

Extended mode: When the Extended enabled, the S2 will be converted into seventh bit of the Command. There is an Extend Command on the Waveform Window.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Encoding Method: Auto Detect mode, Mancherster mode and Mancherster with carrier mode.

S1/S2: Start bit.

Toggle 0/Toggle 1: The difference is that has been used while sending the message to

repeat, or send a new message.

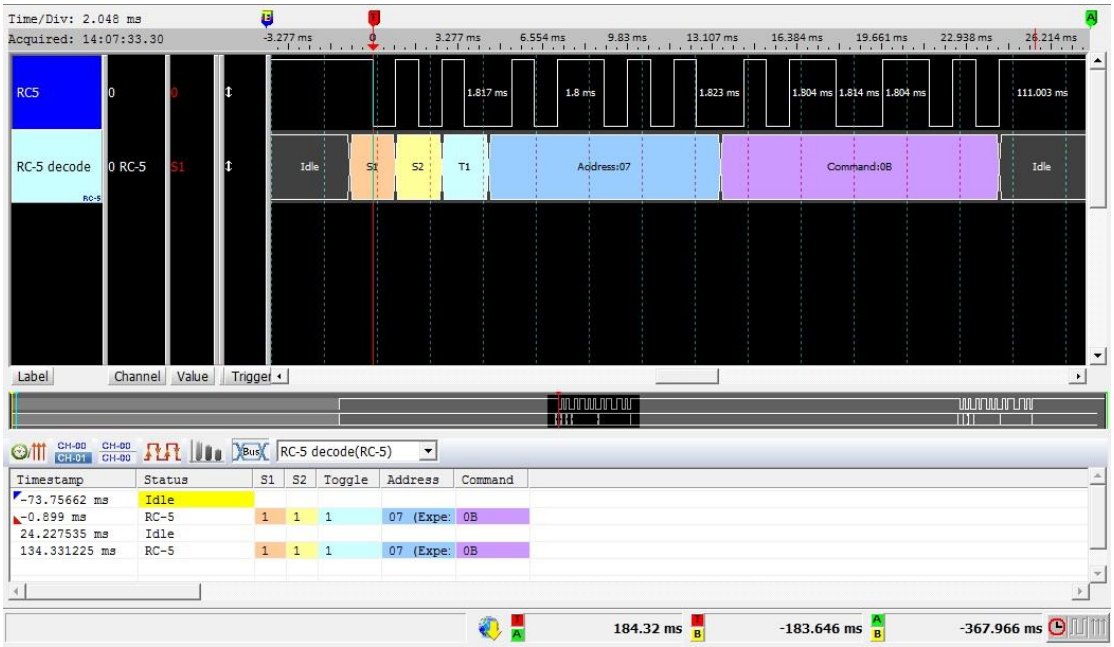
Address: To represent different device addresses.

Command: To represent the different button commands.

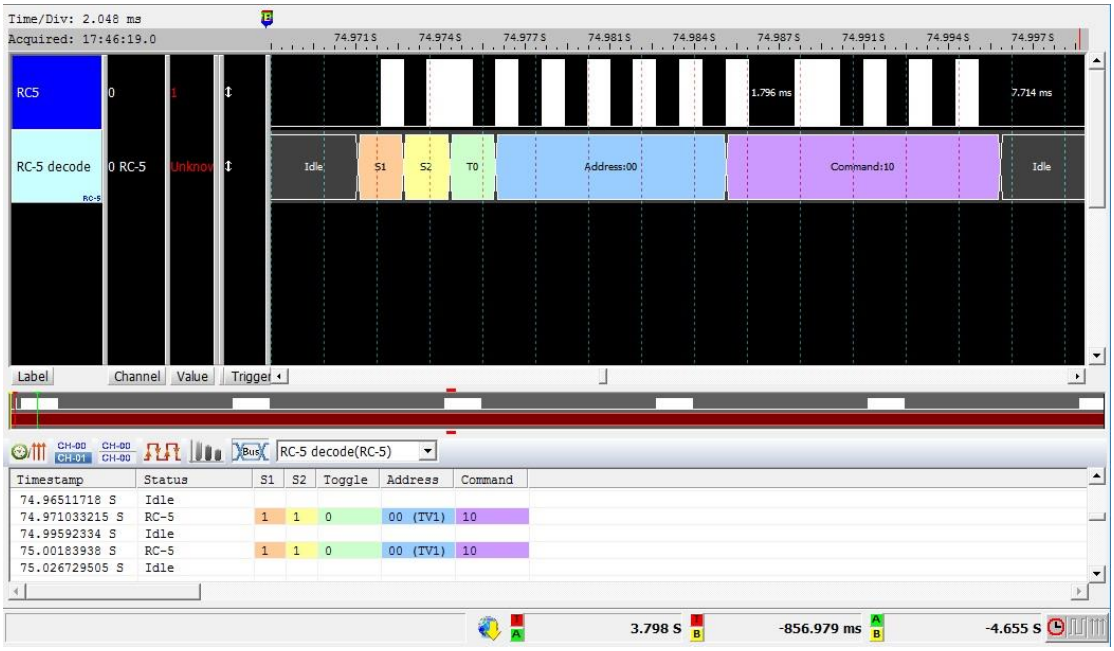
Result

Click **OK** to run the RC-5 decode and see the result on the Waveform Window below.

RC5 without carrier



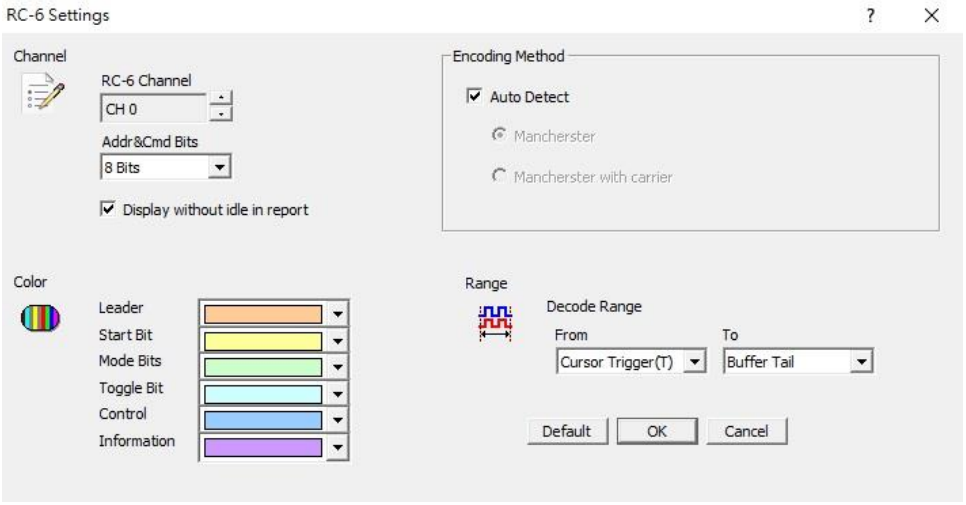
RC5 with carrier



RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

Settings



Channel: Show the selected channel (CH 0).

Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and information in the control label.

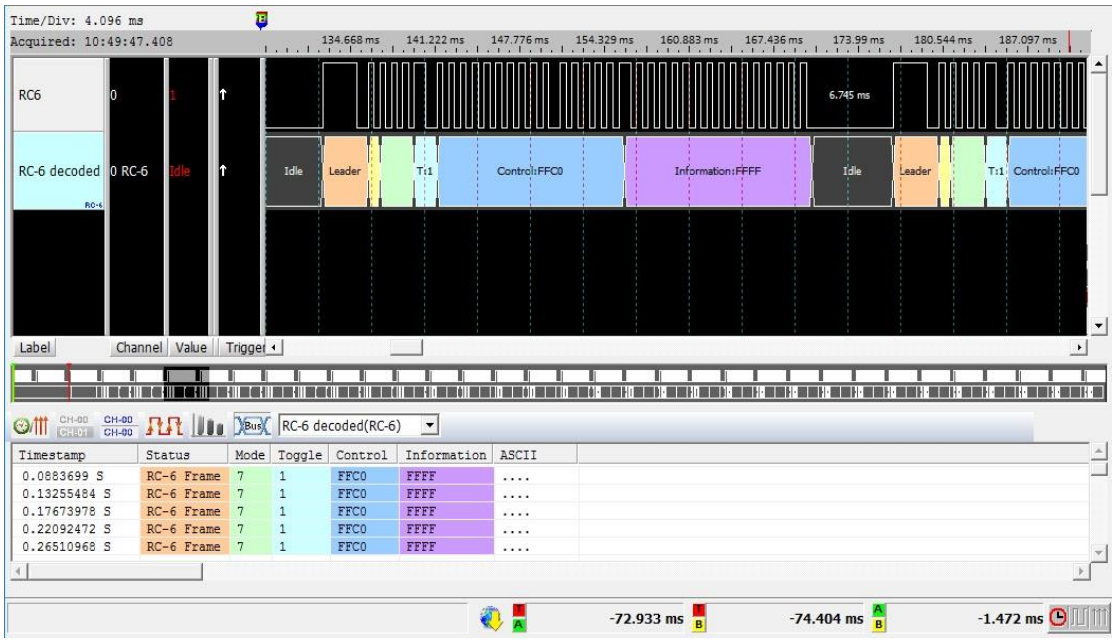
Display without idle in report: Do not display any idle in the Report Window.

Encoding Method: Auto detect mode, Mancherster mode, Mancherster with carrier mode.

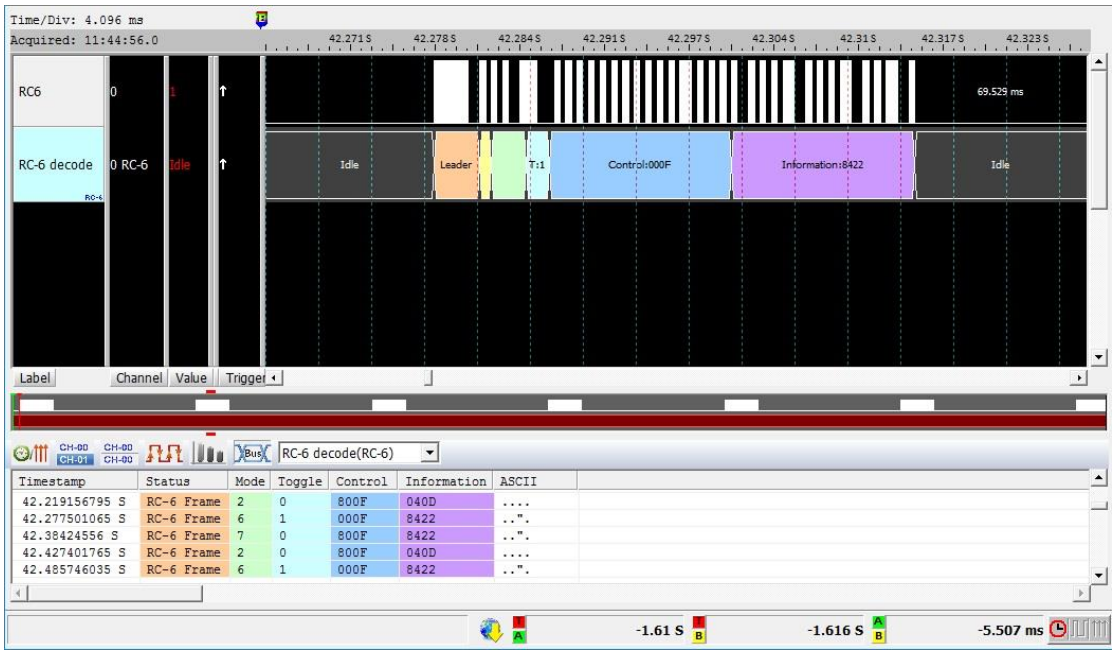
Result

Click **OK** to run the RC-6 decode and see the result on the Waveform Window below.

RC6 without carrier



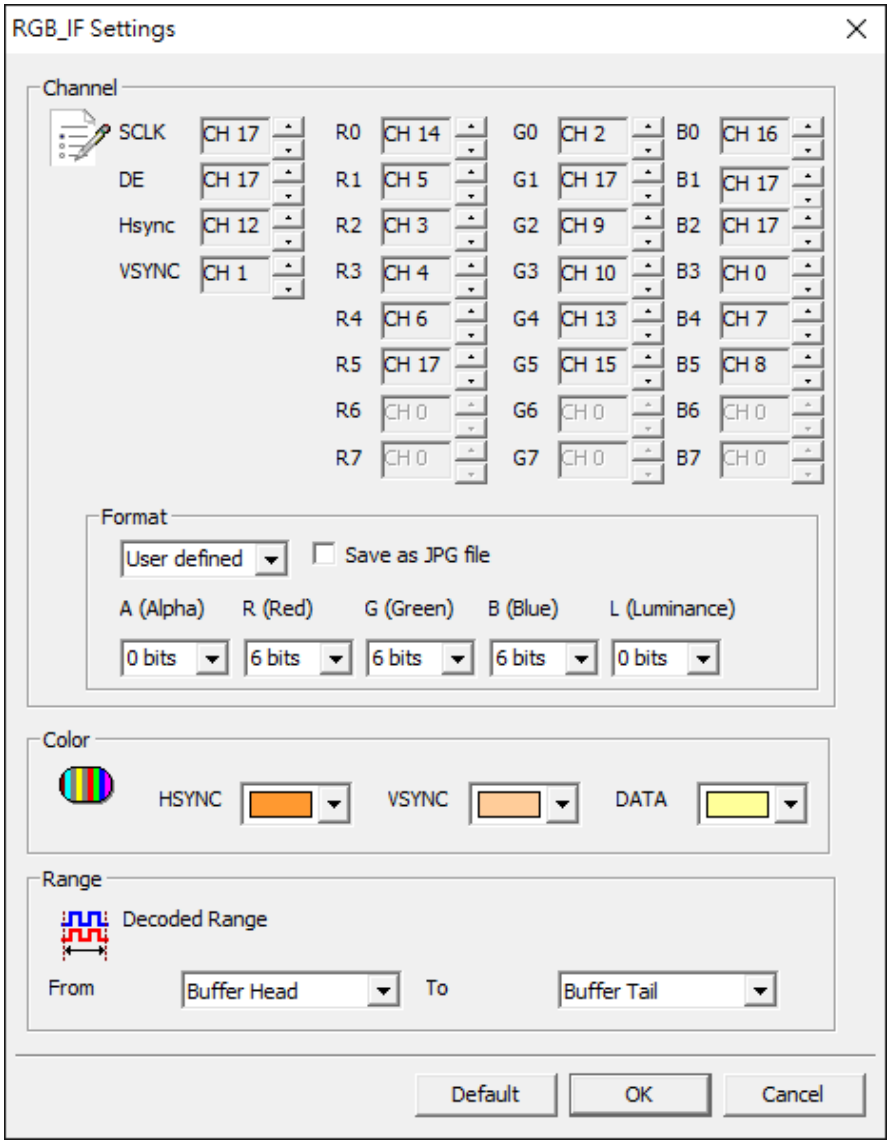
RC6 with carrier



RGB Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

Settings



SCLK: The Clock pin.

DE: The Data Enable pin.

Hsync: The Horizontal synchronization pin.

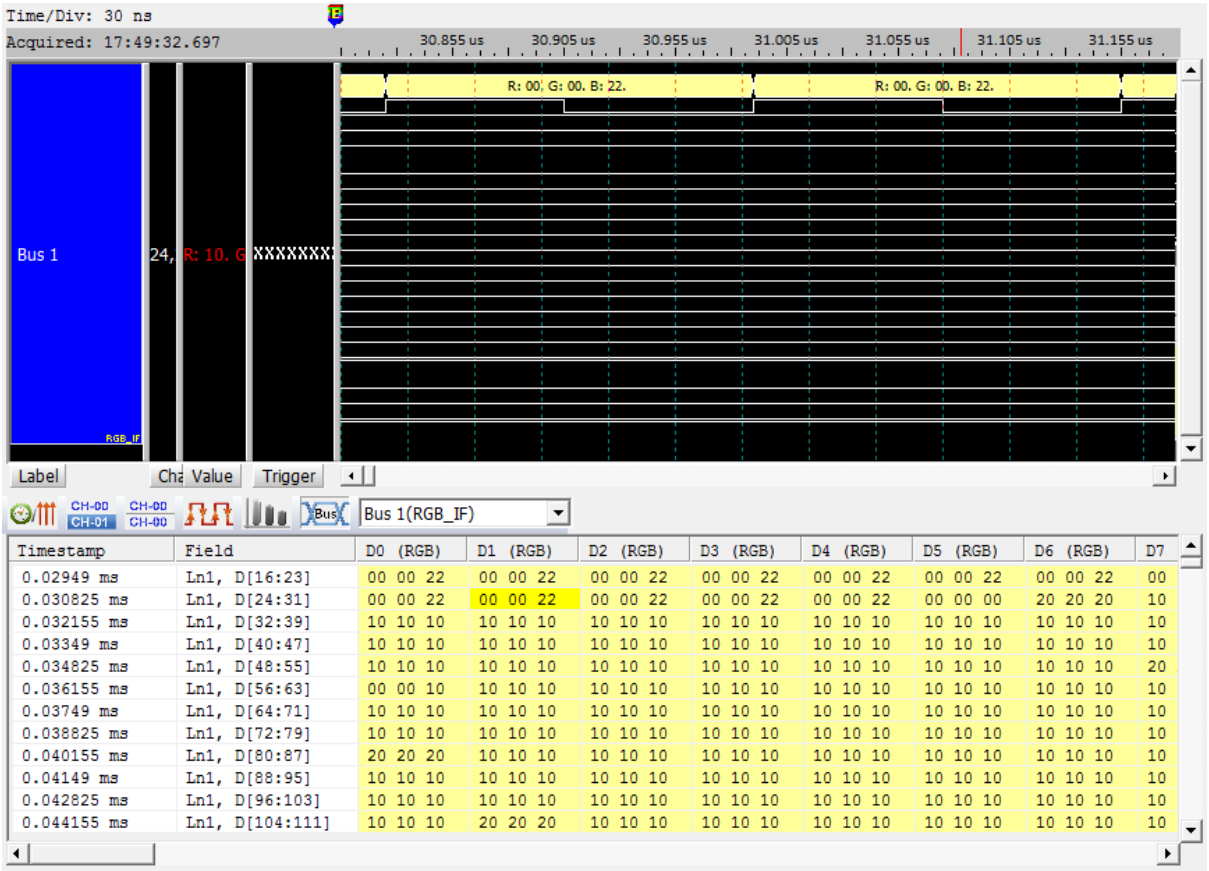
Vsync: The Vertical synchronization pin.

R0 – 7, G0 – 7, B0 – 7: RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of LA.

Result



Timestamp	Field	D0 (RGB)	D1 (RGB)	D2 (RGB)	D3 (RGB)	D4 (RGB)	D5 (RGB)	D6 (RGB)	D7
0.02949 ms	Ln1, D[16:23]	00 00 22	00 00 22	00 00 22	00 00 22	00 00 22	00 00 22	00 00 22	00
0.030825 ms	Ln1, D[24:31]	00 00 22	00 00 22	00 00 22	00 00 22	00 00 22	00 00 00	20 20 20	10
0.032155 ms	Ln1, D[32:39]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.03349 ms	Ln1, D[40:47]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.034825 ms	Ln1, D[48:55]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	20
0.036155 ms	Ln1, D[56:63]	00 00 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.03749 ms	Ln1, D[64:71]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.038825 ms	Ln1, D[72:79]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.040155 ms	Ln1, D[80:87]	20 20 20	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.04149 ms	Ln1, D[88:95]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.042825 ms	Ln1, D[96:103]	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10
0.044155 ms	Ln1, D[104:111]	10 10 10	20 20 20	10 10 10	10 10 10	10 10 10	10 10 10	10 10 10	10

S/PDIF

The Sony/Philips Digital Interconnect Format (S/PDIF) is a digital audio transmission interface with the detailed specifications below:

Data format: Default is 16 bits, up to 24 bits.

Sampling frequency:

44.1Khz from CD → Bit Rate 2.8224 Mbit/s

48 Khz from DAT →Bit Rate 3.072 Mbit/s

32 Khz from DSR → Bit Rate 2.048 Mbit/s

Deliver method: One way.

V (Validity) bit: Audio samples to confirm effectiveness, if this bit is 0, the receiver should ignore this sub-frame.

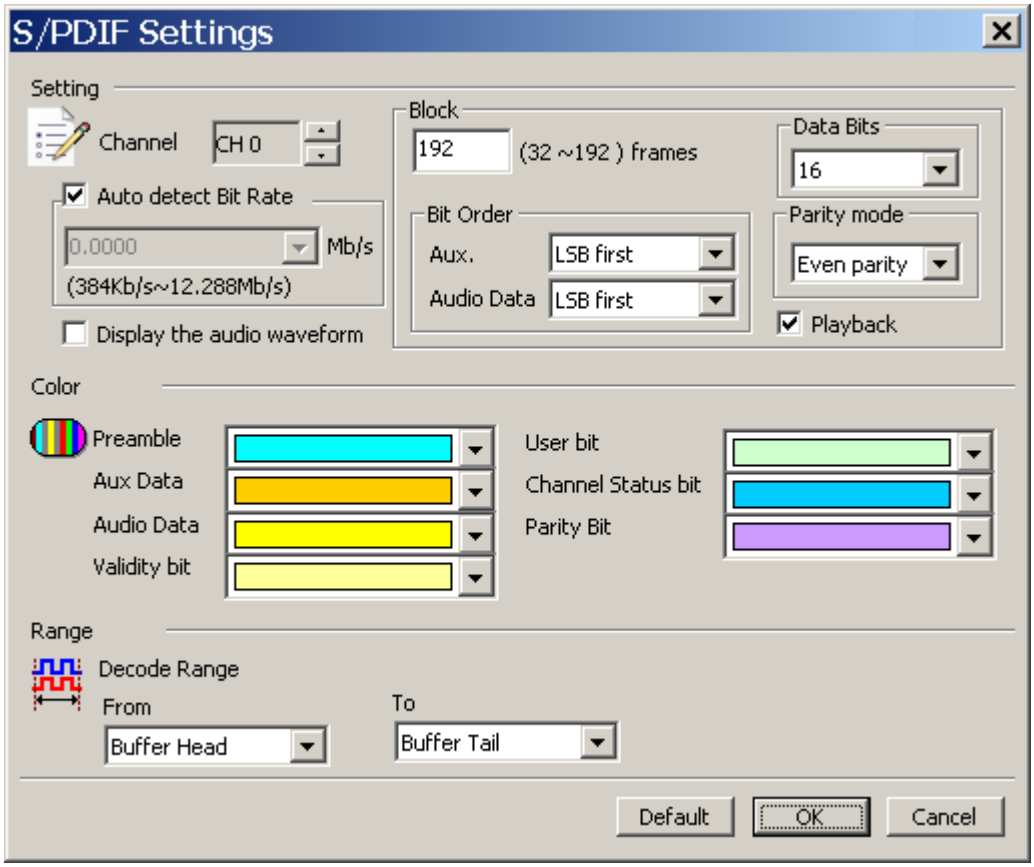
U (User) bit: User log information.

C (Channel status) bit: Channel state information.

P (Parity) bit: Parity bit check for the error.

The basic principle is to split the data bits into two parts. If the data is 1, split it into 01 or 10 or if the data is 0, split it into 00 or 11.

Settings



Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.

Num of frame: 192 frames within each block by default, used to analyze each sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

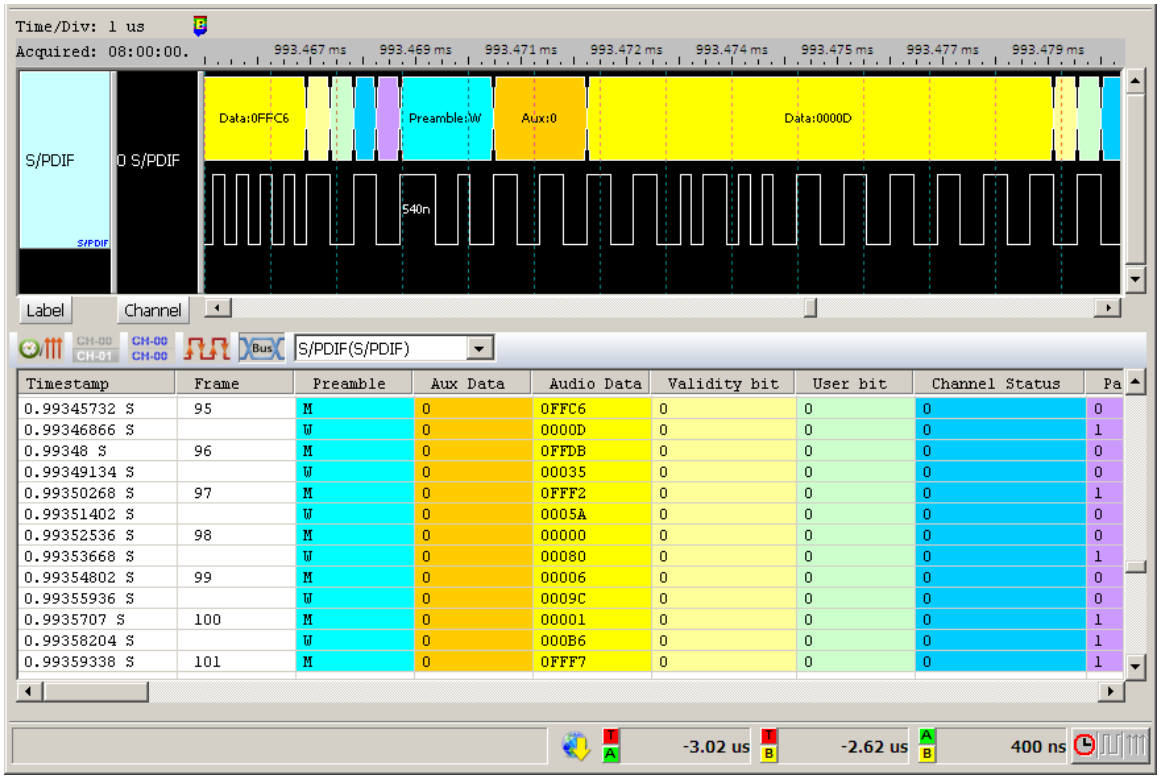
Parity mode: The default is even parity.

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

Result

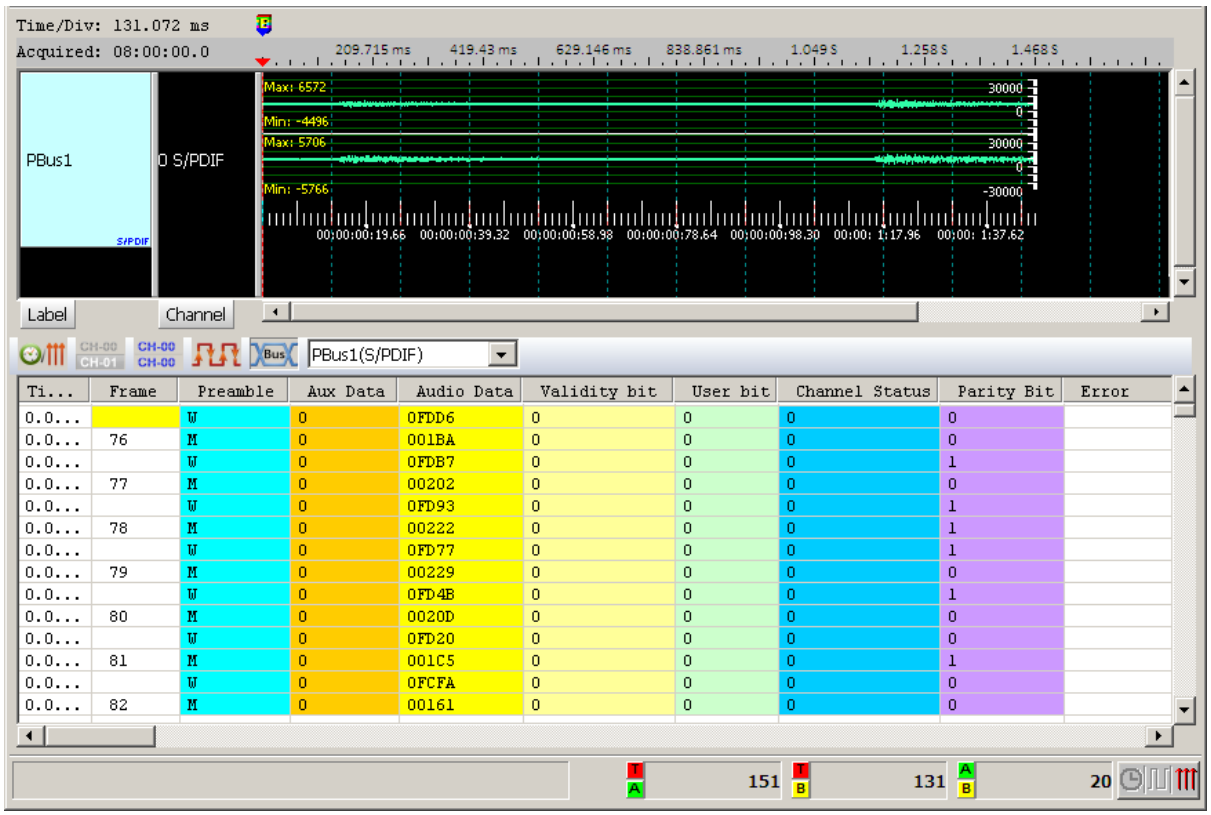
Click **OK** to run the S/PDIF Decode and see the result on the Waveform Window

below.



Timestamp	Frame	Preamble	Aux Data	Audio Data	Validity bit	User bit	Channel Status	Pa
0.99345732 S	95	M	0	0FFC6	0	0	0	0
0.99346866 S		W	0	0000D	0	0	0	1
0.99348 S	96	M	0	0FFDB	0	0	0	0
0.99349134 S		W	0	00035	0	0	0	0
0.99350268 S	97	M	0	0FFF2	0	0	0	1
0.99351402 S		W	0	0005A	0	0	0	0
0.99352536 S	98	M	0	00000	0	0	0	0
0.99353668 S		W	0	00080	0	0	0	1
0.99354802 S	99	M	0	00006	0	0	0	0
0.99355936 S		W	0	0009C	0	0	0	0
0.9935707 S	100	M	0	00001	0	0	0	1
0.99358204 S		W	0	000B6	0	0	0	1
0.99359338 S	101	M	0	0FFF7	0	0	0	1

Show wave:

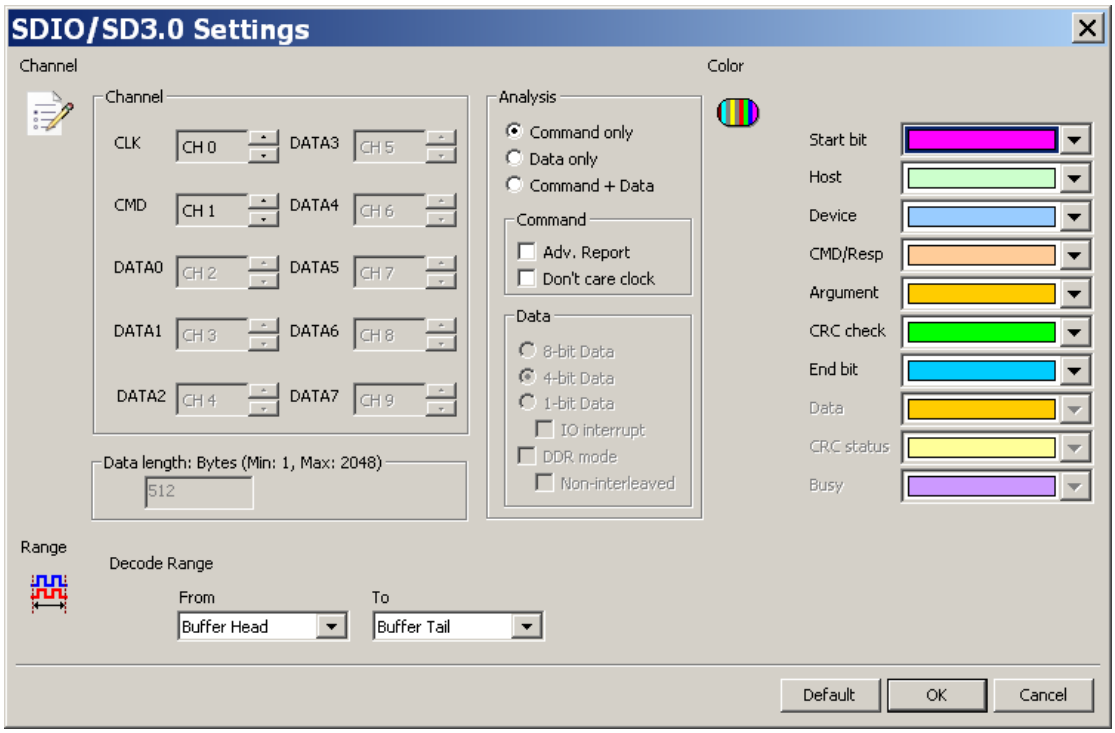


Ti...	Frame	Preamble	Aux Data	Audio Data	Validity bit	User bit	Channel Status	Parity Bit	Error
0.0...		W	0	0FDD6	0	0	0	0	
0.0...	76	M	0	001BA	0	0	0	0	
0.0...		W	0	0FDB7	0	0	0	1	
0.0...	77	M	0	00202	0	0	0	0	
0.0...		W	0	0FD93	0	0	0	1	
0.0...	78	M	0	00222	0	0	0	1	
0.0...		W	0	0FD77	0	0	0	1	
0.0...	79	M	0	00229	0	0	0	0	
0.0...		W	0	0FD4B	0	0	0	1	
0.0...	80	M	0	0020D	0	0	0	0	
0.0...		W	0	0FD20	0	0	0	0	
0.0...	81	M	0	001C5	0	0	0	1	
0.0...		W	0	0FCFA	0	0	0	0	
0.0...	82	M	0	00161	0	0	0	0	

SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for interfacing with SD (Secure Digital) Flash memory cards.

Settings



Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data.

Command + Data: Analyze Command and Data in the report window.

Adv. Report: Analyze the command argument

Don't care clock: decode only depend on the CMD channel.

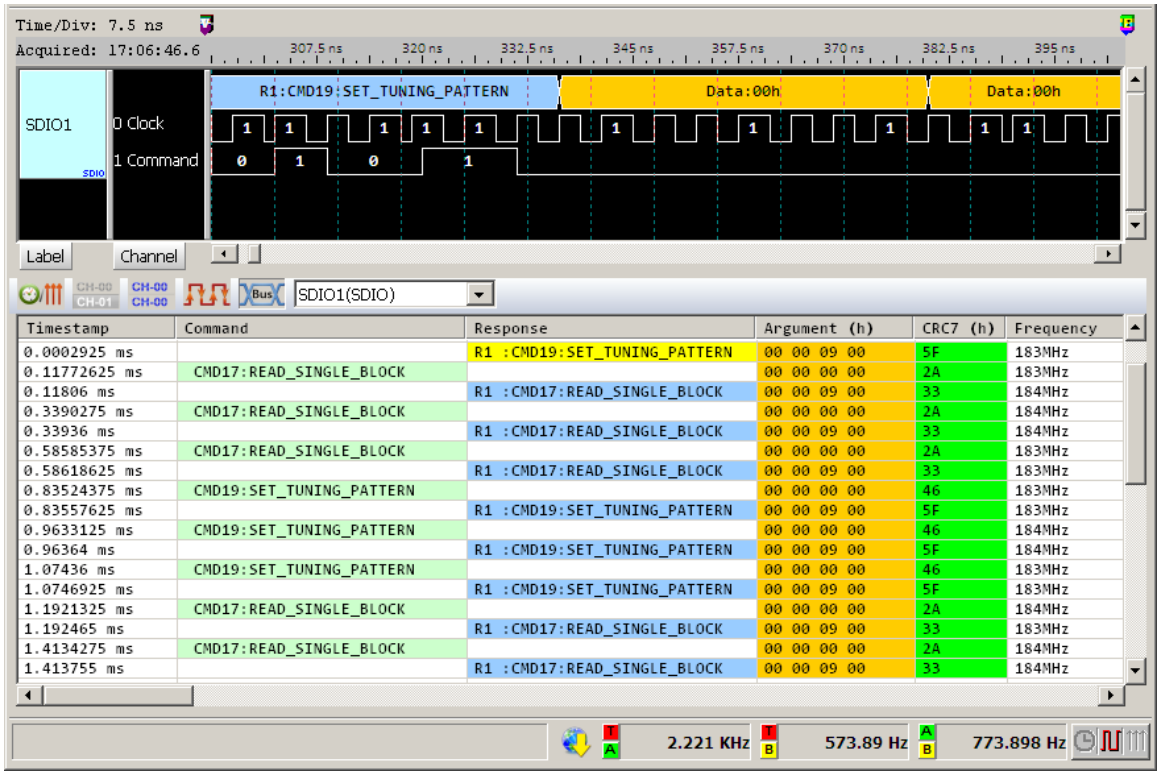
Data: 1/4/8 bits or DDR mode, check "IO interrupt" when SDIO 1 bit mode and support the IO interrupt decode via DATA1 channel, check "DDR mode" and " "Non-interleaved" to analyze data without interleaved.

Data length: Set the length of data.

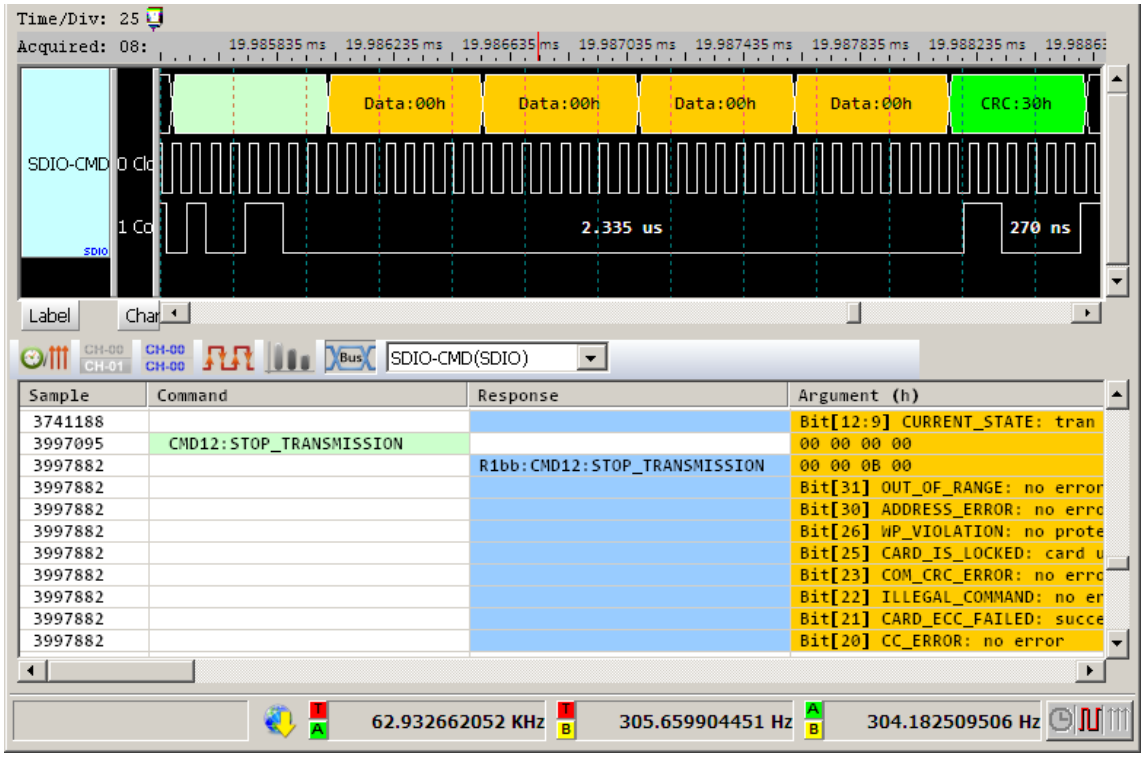
Result

Click **OK** to run the SDI/O decode and see the result on the Waveform Window below.

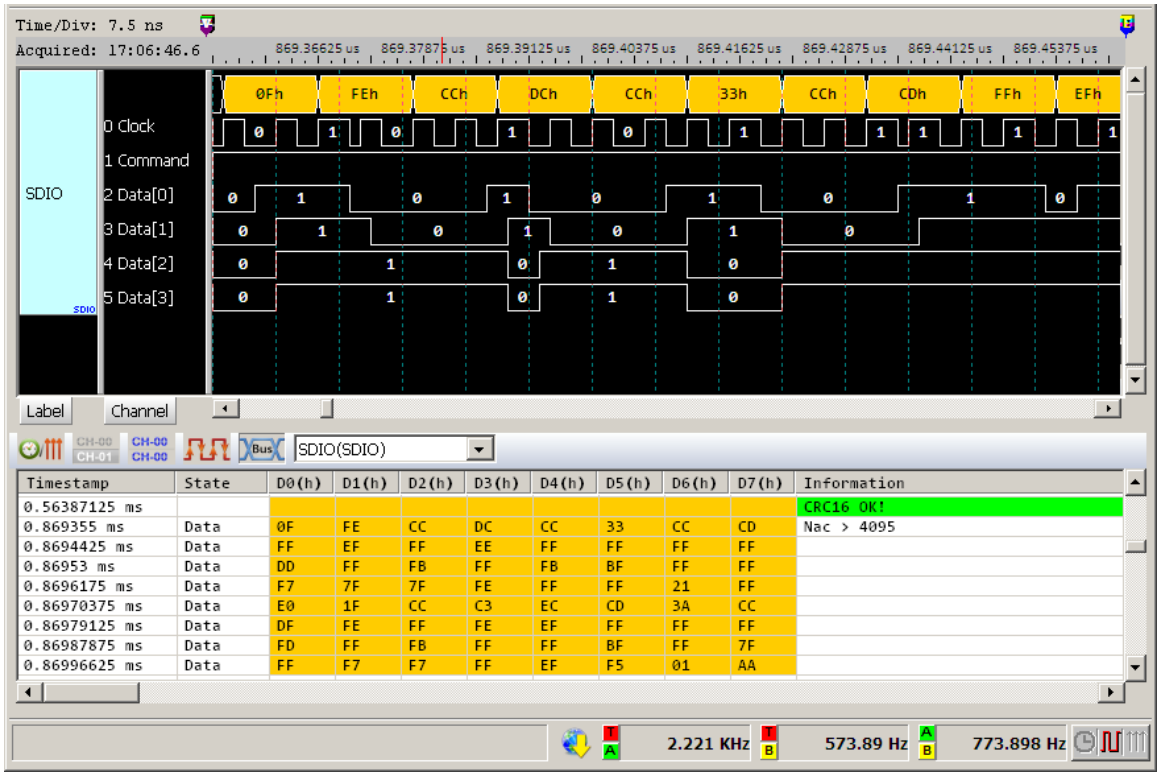
CMD mode



Adv. Report



Data mode

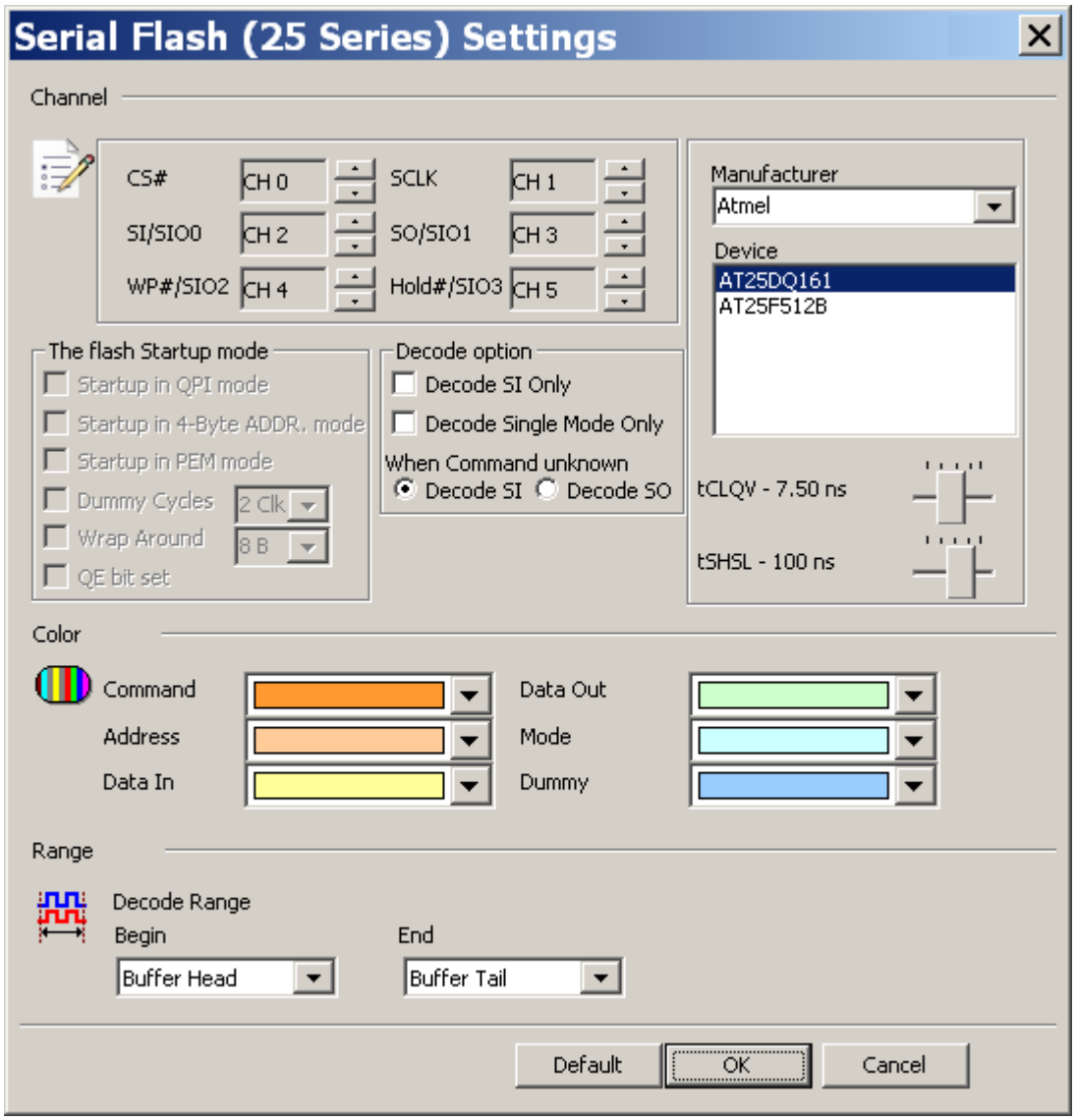


Timestamp	State	D0(h)	D1(h)	D2(h)	D3(h)	D4(h)	D5(h)	D6(h)	D7(h)	Information
0.56387125 ms										CRC16 OK!
0.869355 ms	Data	0F	FE	CC	DC	CC	33	CC	CD	Nac > 4095
0.8694425 ms	Data	FF	EF	FF	EE	FF	FF	FF	FF	
0.86953 ms	Data	DD	FF	FB	FF	FB	BF	FF	FF	
0.8696175 ms	Data	F7	7F	7F	FE	FF	FF	21	FF	
0.86970375 ms	Data	E0	1F	CC	C3	EC	CD	3A	CC	
0.86979125 ms	Data	DF	FE	FF	FE	EF	FF	FF	FF	
0.86987875 ms	Data	FD	FF	FB	FF	FF	BF	FF	7F	
0.86996625 ms	Data	FF	F7	F7	FF	EF	F5	01	AA	

Serial Flash

SPI Serial Flash is small, low-power flash memory that features Serial Peripheral Interface (SPI) and pin-for-pin compatibility with industry-standard SPI EEPROM devices.

Settings



Channel: Show the selected channels (CH0 – CH5).

Manufacturer/Device: Select the Serial Flash device type, tCLQV and tSHSL.

QPI mode: Quad Peripheral Interface Mode/Quad SPI Mode

4-Byte mode: 4-Byte Address Mode

PEM mode: Performance Enhance Mode

Dummy Cycles: Clock buffers between read command and data.

Wrap Around: Wrap number

QE bit: Enable or disable the QPI mode.

Decode SI Only: Single mode, 3-wire → CS#, SCLK, SI.

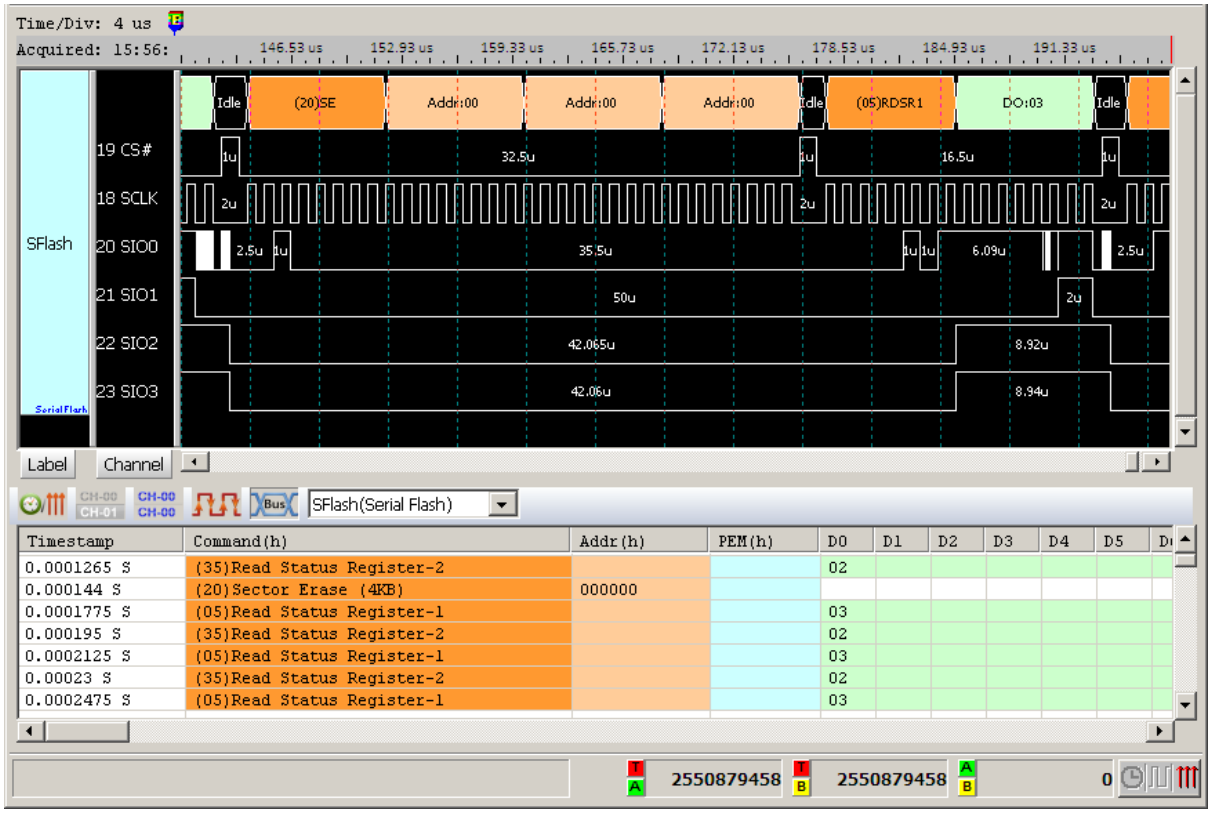
Decode Single Mode Only: Single mode, 4-wire → CS, Clock, SI, SO.

The LA viewer will choose 4-wire or 6-wire to analyze according to the Serial Flash device type.

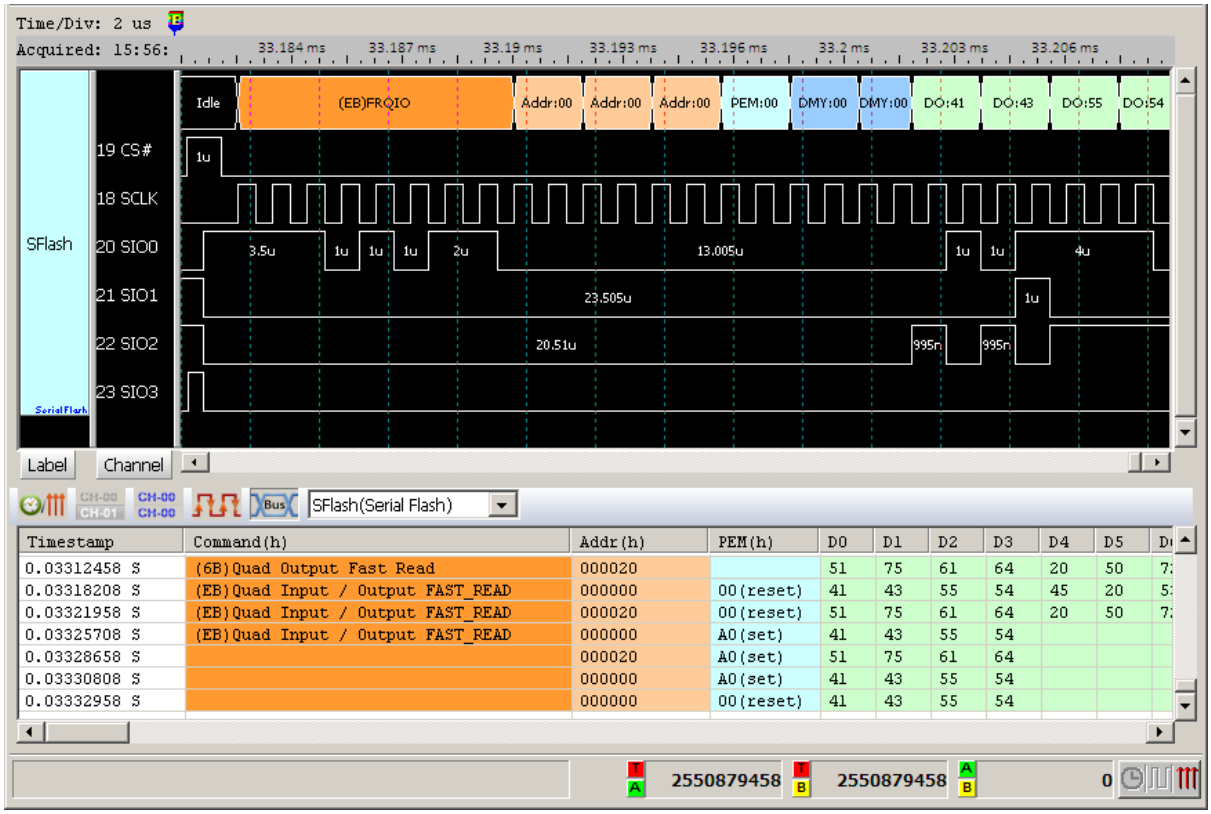
Result

Click **OK** to run the Serial Flash decode and see the result on the Waveform Window below.

Serial Flash decode within SPI mode.



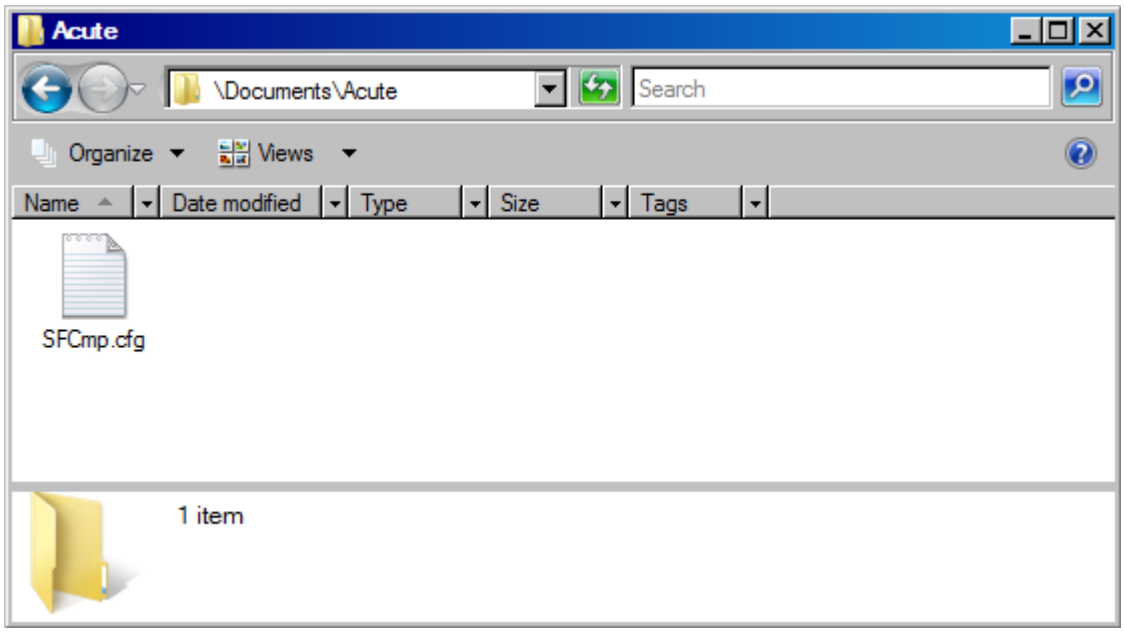
Serial Flash decode within QPI mode.



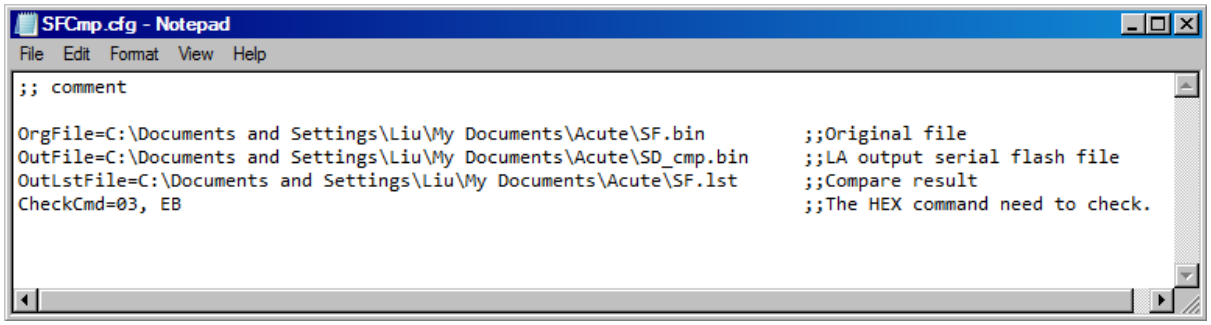
Serial Flash data Comparison : Compare the Serial Flash data by the waveform

files.

Method: Create a file by text editor and save it as SFCmp.cfg in order to compare with the real Serial Flash waveform to find the bug, the default path is “My Documents\Acute”



SFCmp.cfg information:



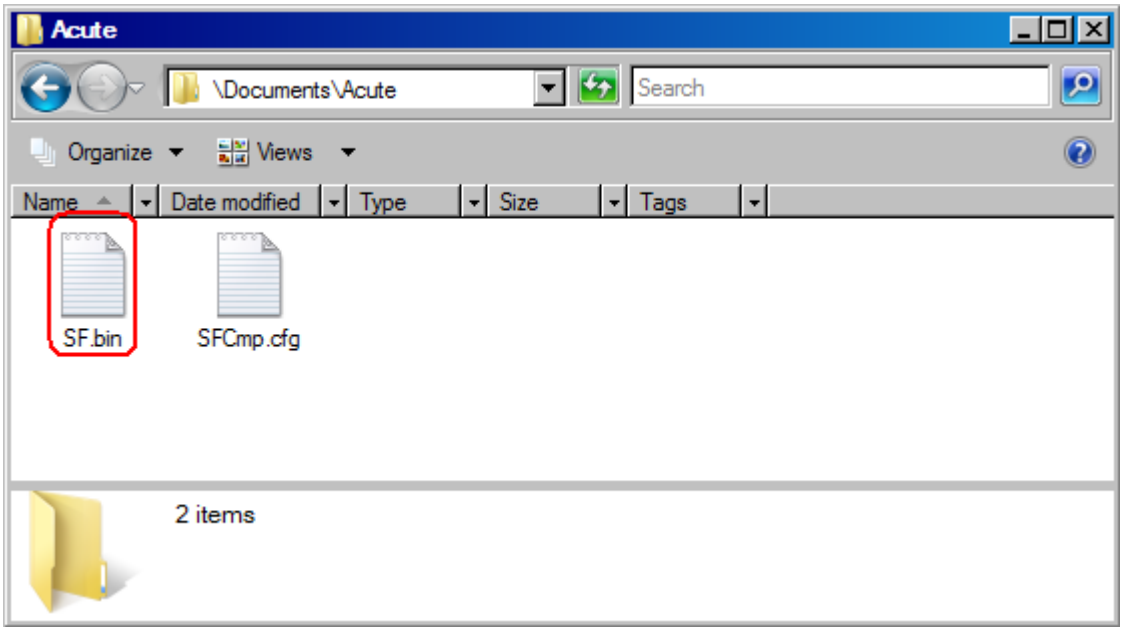
OrgFile=File_Path: Key in the file path of the original Serial Flash data file (.bin).

OutFile=File_Path: Key in the file path of the Serial Flash output file.

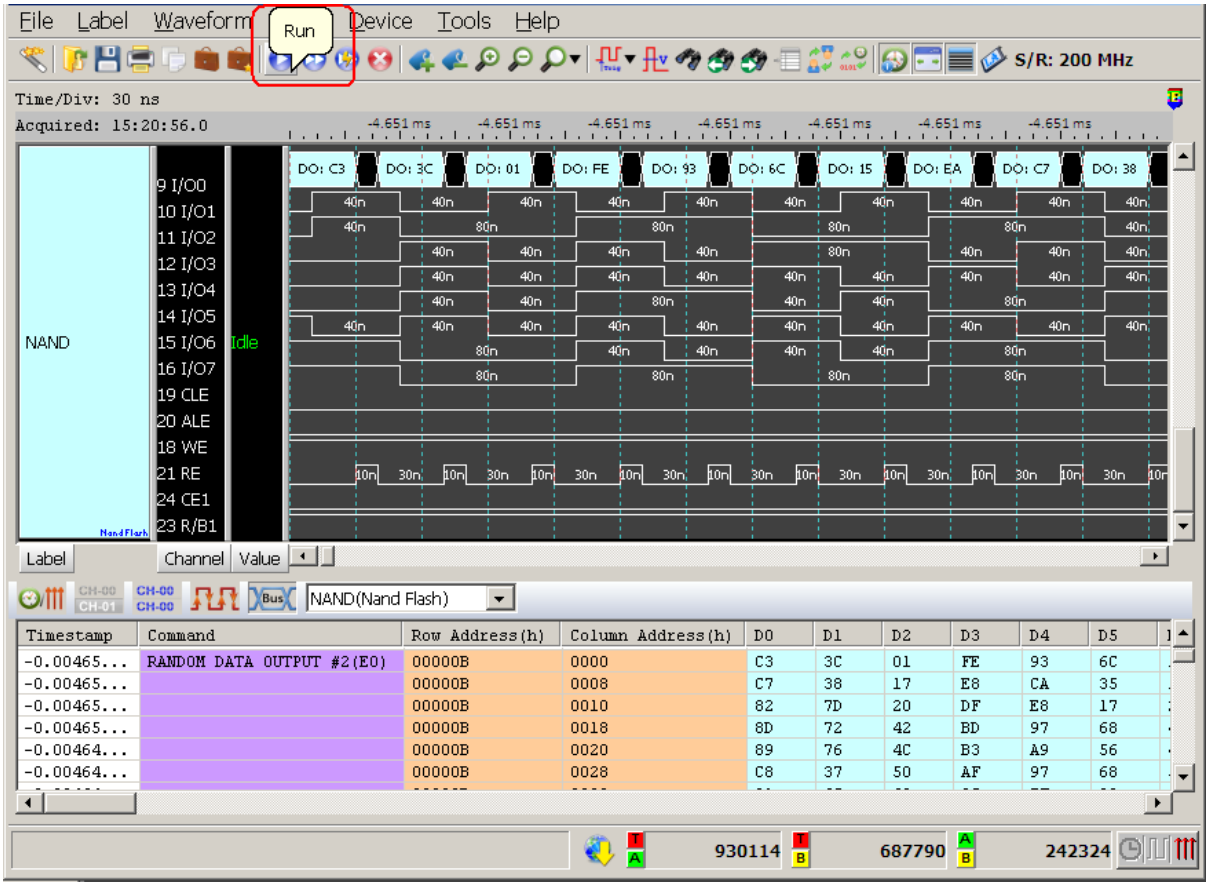
OutLstFile=File_Path: Key in the file path of the comparison result. The file name will has extension “.lst”.

CheckCmd=Serial Flash command: Key in the command in Hex that are separated by commas.

Save the OrgFile to the OrgFile file path.



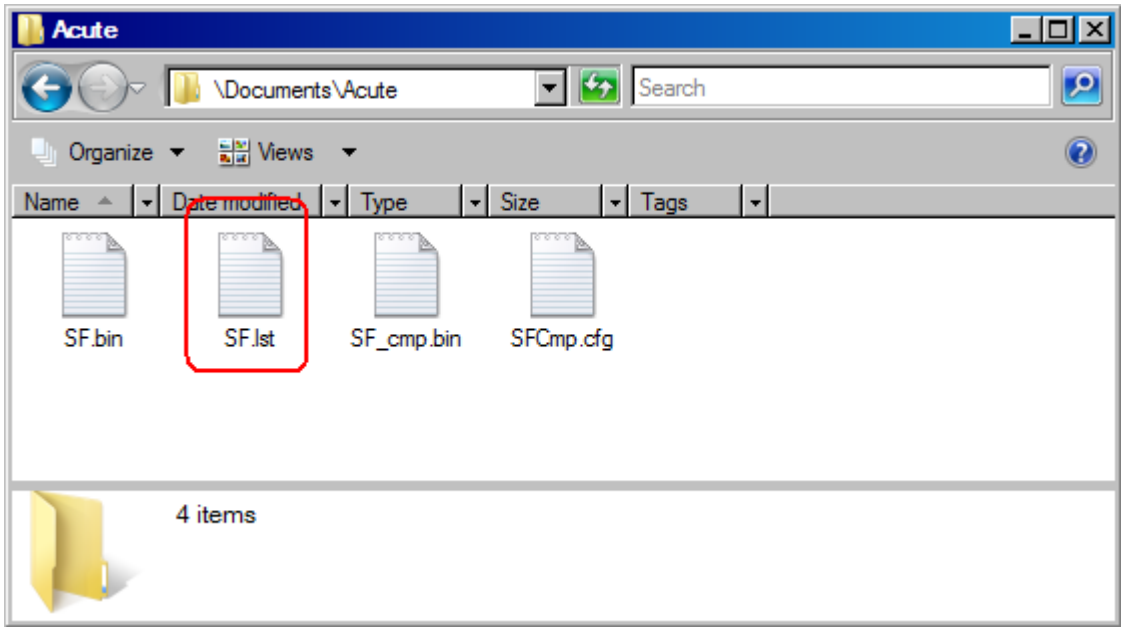
Run the Serial Flash Bus Decode to capture the Serial Flash signal.



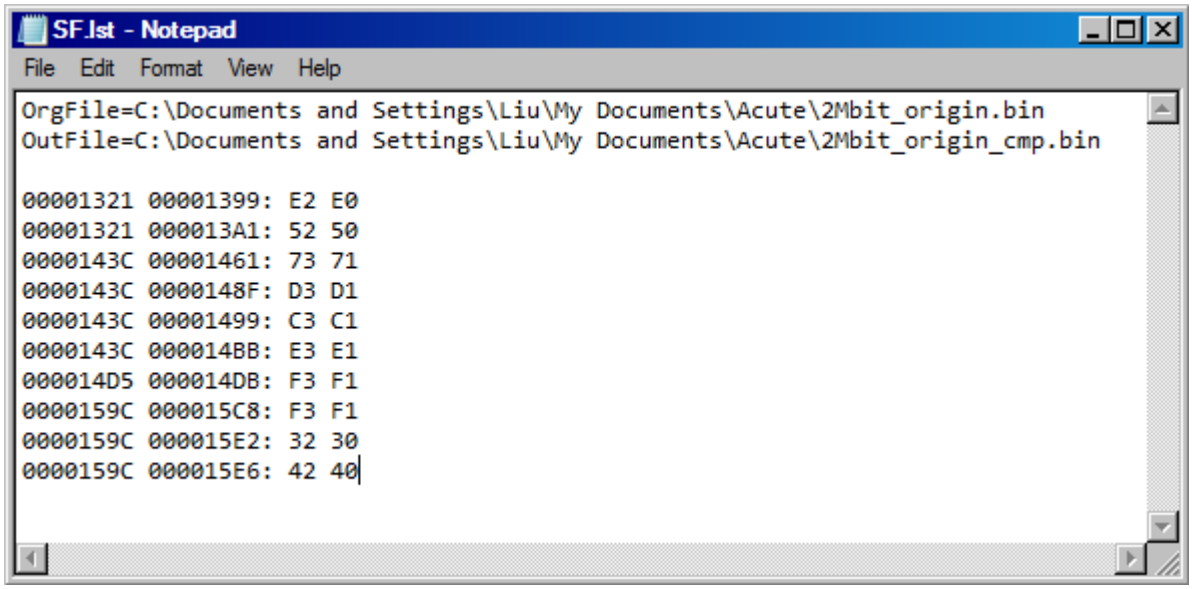
If the OutFile does not exit, it will copy the OrgFile to the OutFile and write the data

to it according to the CheckCmd.

Compare result:



The OutLstFile:

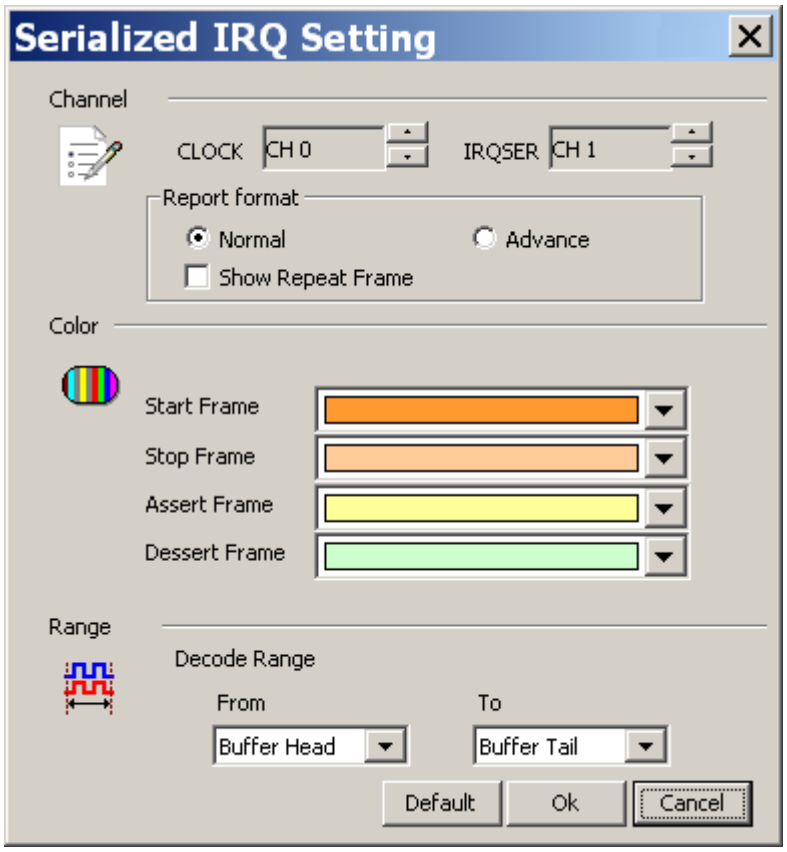


The first column is the compared address from OrgFile, the second column is the different address from OutFile.

Serial IRQ

The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame. This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

Settings



CLOCK: PCI Clock channel

IRQSER; IRQSER channel

Normal: Not show repeat frame

Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10286946	22830	Continue mode		A					A						A				
10291906	22841	Continue mode		A											A				
10404663	23091	Continue mode		A					A						A				
10415039	23114	Continue mode		A											A				
10459240	23212	Continue mode		A					A						A				
10461943	23218	Continue mode		A											A				
10580112	23480	Continue mode		A					A						A				
10590037	23502	Continue mode		A											A				
10634238	23600	Continue mode		A					A						A				
10636941	23606	Continue mode		A											A				

Show repeat frame

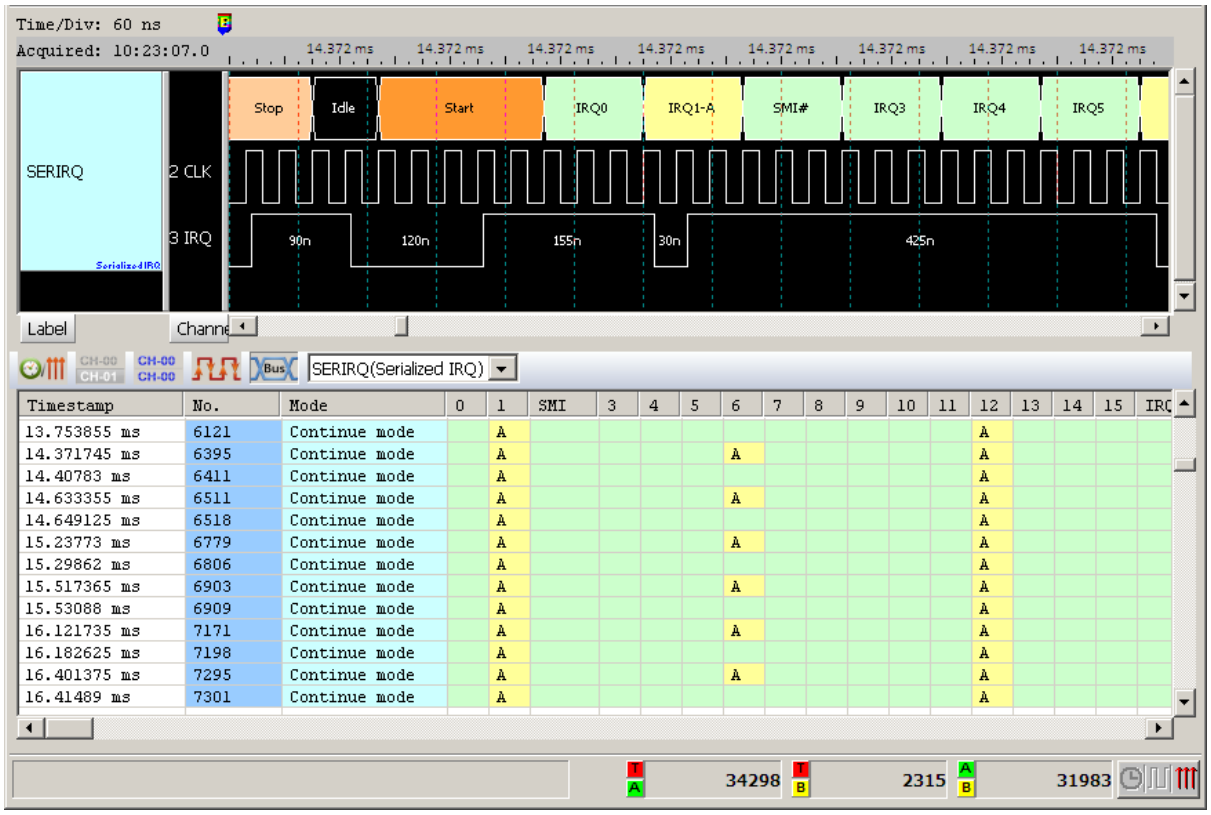
Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10457887	23209	Continue mode		A											A				
10458338	23210	Continue mode		A											A				
10458789	23211	Continue mode		A											A				
10459240	23212	Continue mode		A					A						A				
10459690	23213	Continue mode		A					A						A				
10460140	23214	Continue mode		A					A						A				
10460590	23215	Continue mode		A					A						A				
10461041	23216	Continue mode		A					A						A				
10461492	23217	Continue mode		A					A						A				
10461943	23218	Continue mode		A											A				
10462394	23219	Continue mode		A											A				
10462846	23220	Continue mode		A											A				
10463298	23221	Continue mode		A											A				

Advance:

Clock	IRQ/Data Frame	Signal Sampled	# of clocks past Start
-9470	1	IRQ0	2
-9452	2	IRQ1	5
-9434	3	SMI#	8
-9416	4	IRQ3	11
-9398	5	IRQ4	14
-9380	6	IRQ5	17
-9362	7	IRQ6	20
-9344	8	IRQ7	23
-9326	9	IRQ8	26
-9308	10	IRQ9	29
-9290	11	IRQ10	32
-9272	12	IRQ11	35
-9254	13	IRQ12	38
-9236	14	IRQ13	41
-9217	15	IRQ14	44
-9199	16	IRQ15	47
-9181	17	IOCHCK#	50
-9163	18	INTA#	53
-9145	19	INTB#	56
-9127	20	INTC#	59
-9109	21	INTD#	62
-9019	1	IRQ0	2
-9001	2	IRQ1	5

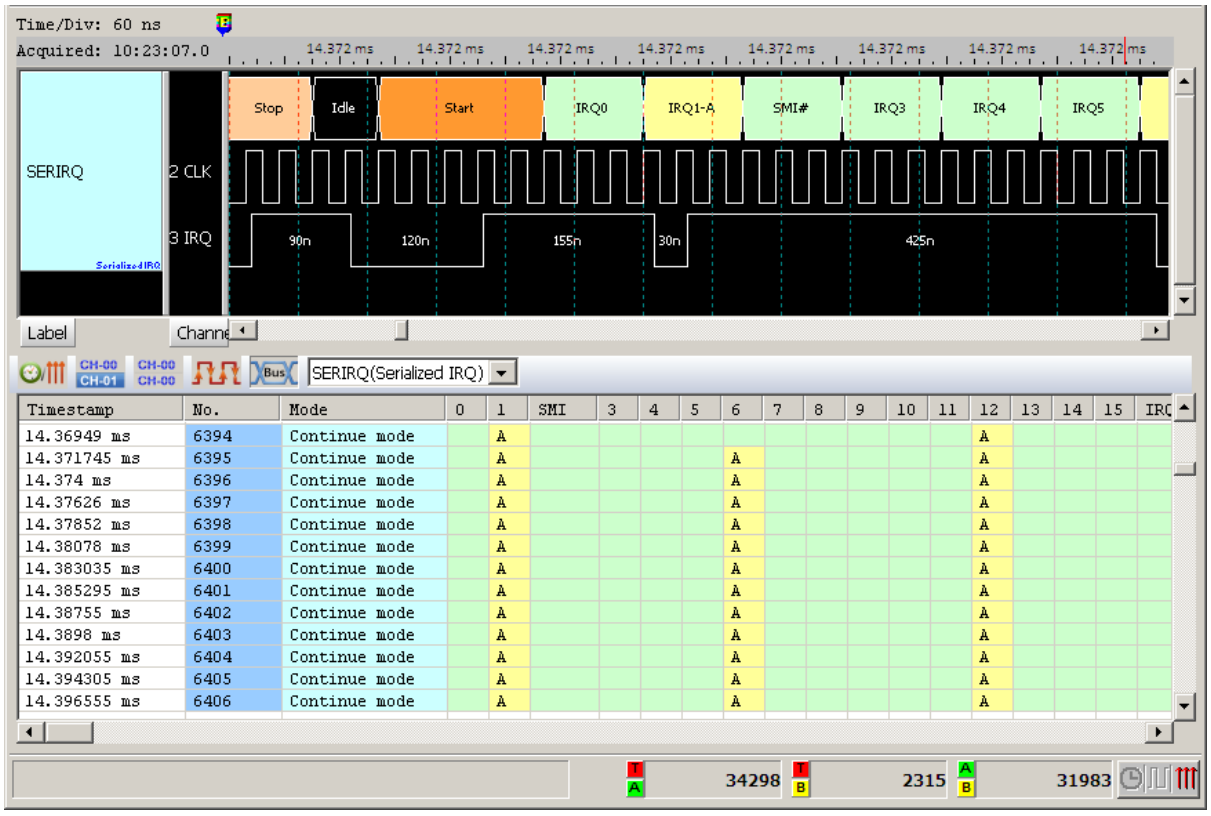
Result

Normal mode



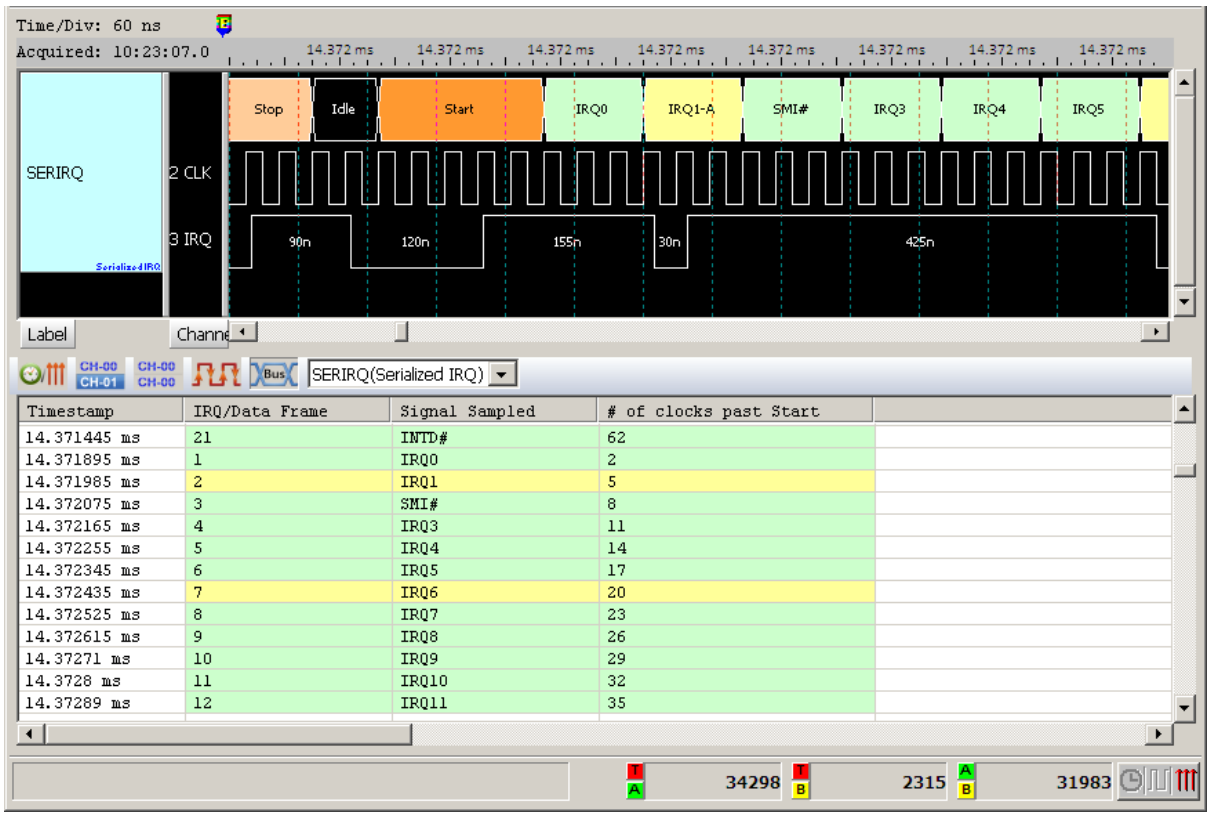
Timestamp	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
13.753855 ms	6121	Continue mode		A											A				
14.371745 ms	6395	Continue mode		A					A						A				
14.40783 ms	6411	Continue mode		A											A				
14.633355 ms	6511	Continue mode		A					A						A				
14.649125 ms	6518	Continue mode		A											A				
15.23773 ms	6779	Continue mode		A					A						A				
15.29862 ms	6806	Continue mode		A											A				
15.517365 ms	6903	Continue mode		A					A						A				
15.53088 ms	6909	Continue mode		A											A				
16.121735 ms	7171	Continue mode		A					A						A				
16.182625 ms	7198	Continue mode		A											A				
16.401375 ms	7295	Continue mode		A					A						A				
16.41489 ms	7301	Continue mode		A											A				

Normal mode(Show repeat frame)



Timestamp	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
14.36949 ms	6394	Continue mode		A											A				
14.371745 ms	6395	Continue mode		A					A						A				
14.374 ms	6396	Continue mode		A					A						A				
14.37626 ms	6397	Continue mode		A					A						A				
14.37852 ms	6398	Continue mode		A					A						A				
14.38078 ms	6399	Continue mode		A					A						A				
14.383035 ms	6400	Continue mode		A					A						A				
14.385295 ms	6401	Continue mode		A					A						A				
14.38755 ms	6402	Continue mode		A					A						A				
14.3898 ms	6403	Continue mode		A					A						A				
14.392055 ms	6404	Continue mode		A					A						A				
14.394305 ms	6405	Continue mode		A					A						A				
14.396555 ms	6406	Continue mode		A					A						A				

Advance mode

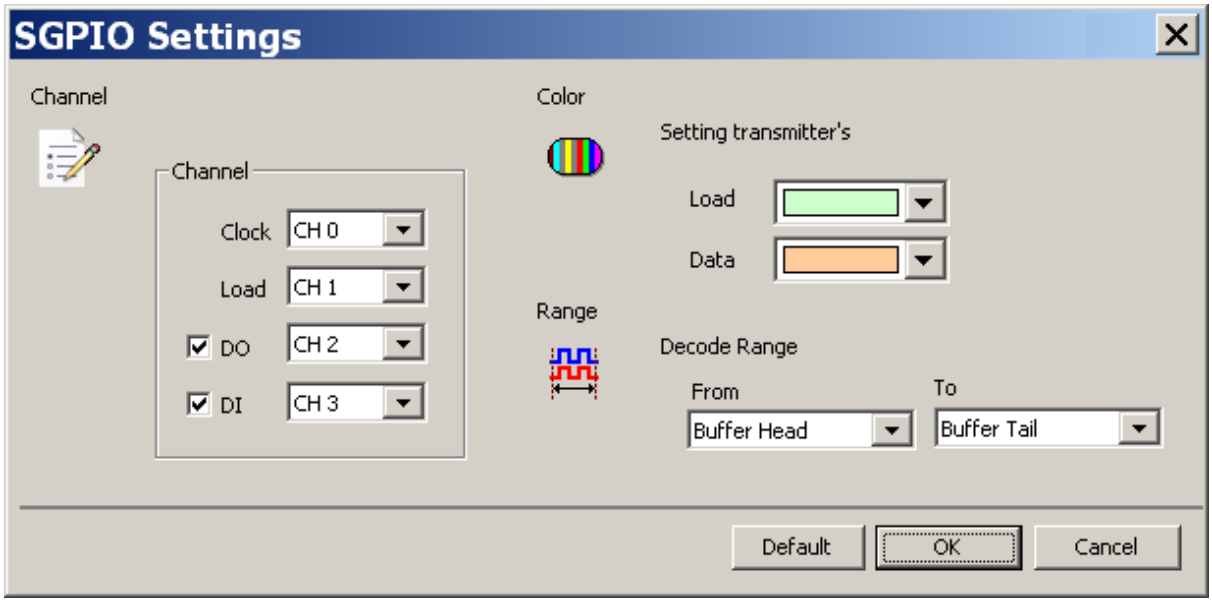


Timestamp	IRQ/Data Frame	Signal Sampled	# of clocks past Start
14.371445 ms	21	INTD#	62
14.371895 ms	1	IRQ0	2
14.371985 ms	2	IRQ1	5
14.372075 ms	3	SMI#	8
14.372165 ms	4	IRQ3	11
14.372255 ms	5	IRQ4	14
14.372345 ms	6	IRQ5	17
14.372435 ms	7	IRQ6	20
14.372525 ms	8	IRQ7	23
14.372615 ms	9	IRQ8	26
14.37271 ms	10	IRQ9	29
14.3728 ms	11	IRQ10	32
14.37289 ms	12	IRQ11	35

Serial General Purpose Input Output (SGPIO)

The SGPIO is a method to serialize general purpose IO signals. SGPIO defines the communication between an initiator and a target.

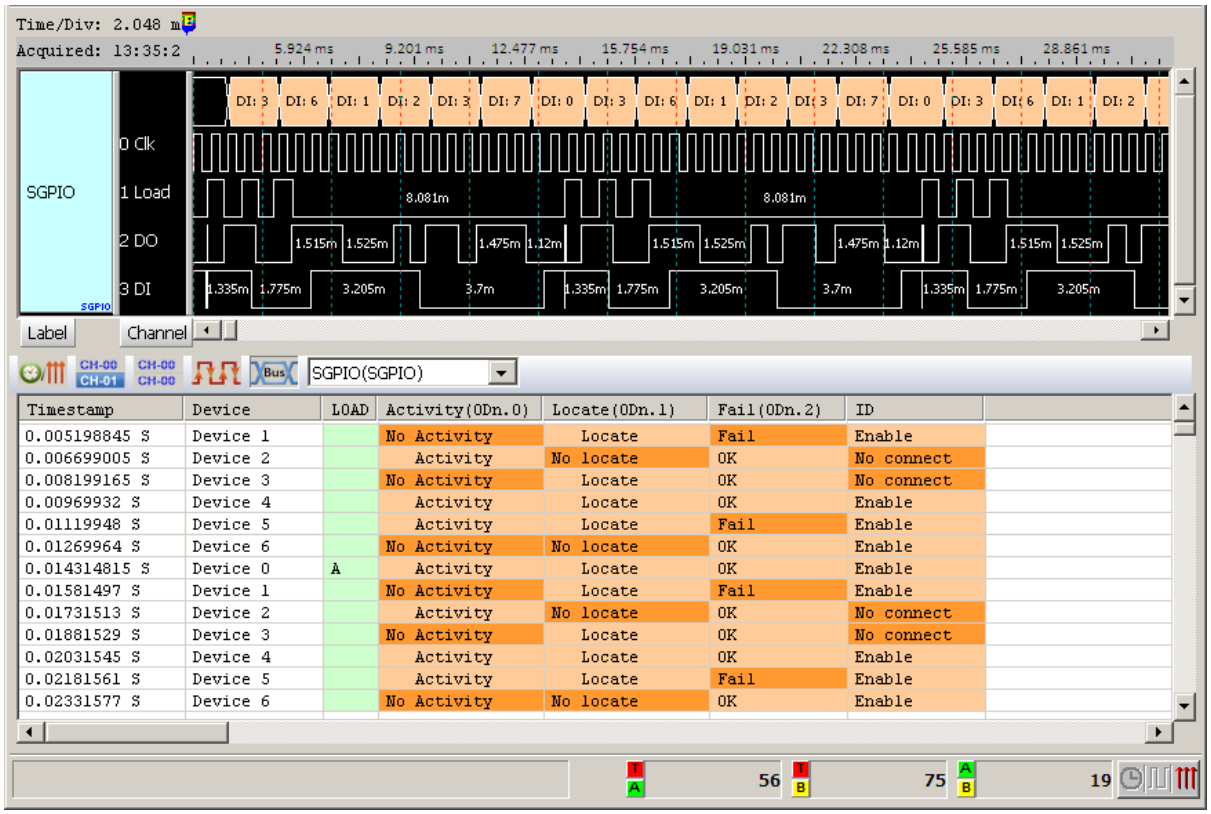
Settings



Channel: Show the selected channels (Clock, Load and Data), it can only use data out or date in or both.

Result:

Click OK to run the Smart Card decode and see the result on the Waveform Window below.

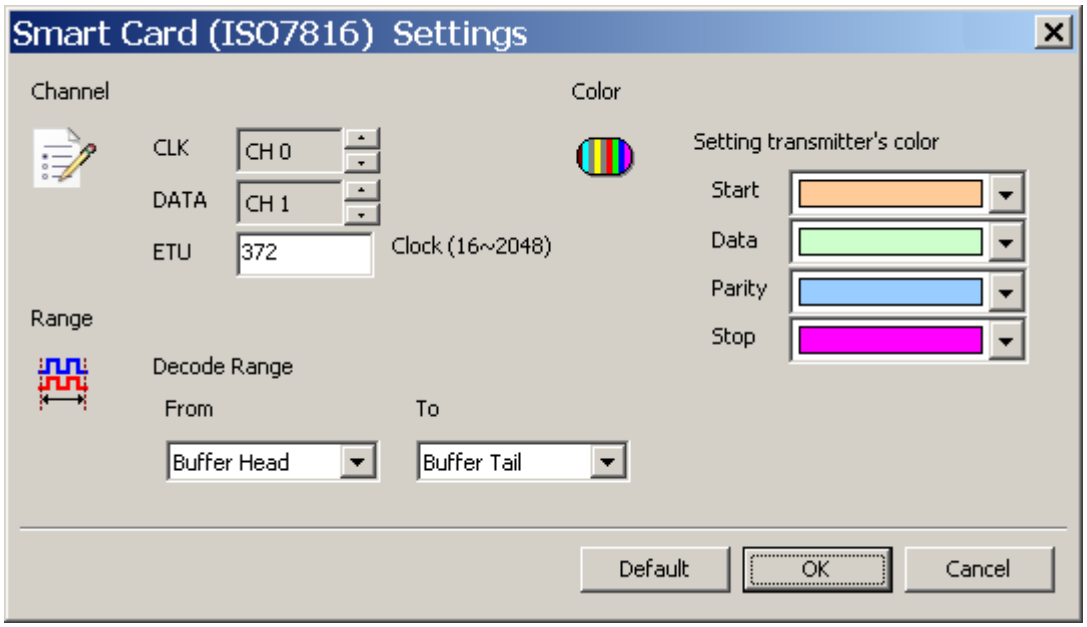


Timestamp	Device	LOAD	Activity(ODn.0)	Locate(ODn.1)	Fail(ODn.2)	ID
0.005198845 S	Device 1		No Activity	Locate	Fail	Enable
0.006699005 S	Device 2		Activity	No locate	OK	No connect
0.008199165 S	Device 3		No Activity	Locate	OK	No connect
0.00969932 S	Device 4		Activity	Locate	OK	Enable
0.01119948 S	Device 5		Activity	Locate	Fail	Enable
0.01269964 S	Device 6		No Activity	No locate	OK	Enable
0.014314815 S	Device 0	A	Activity	Locate	OK	Enable
0.01581497 S	Device 1		No Activity	Locate	Fail	Enable
0.01731513 S	Device 2		Activity	No locate	OK	No connect
0.01881529 S	Device 3		No Activity	Locate	OK	No connect
0.02031545 S	Device 4		Activity	Locate	OK	Enable
0.02181561 S	Device 5		Activity	Locate	Fail	Enable
0.02331577 S	Device 6		No Activity	No locate	OK	Enable

Smart Card (ISO7816)

The card is made of plastic and provides strong security authentication for single sign-on within large organizations.

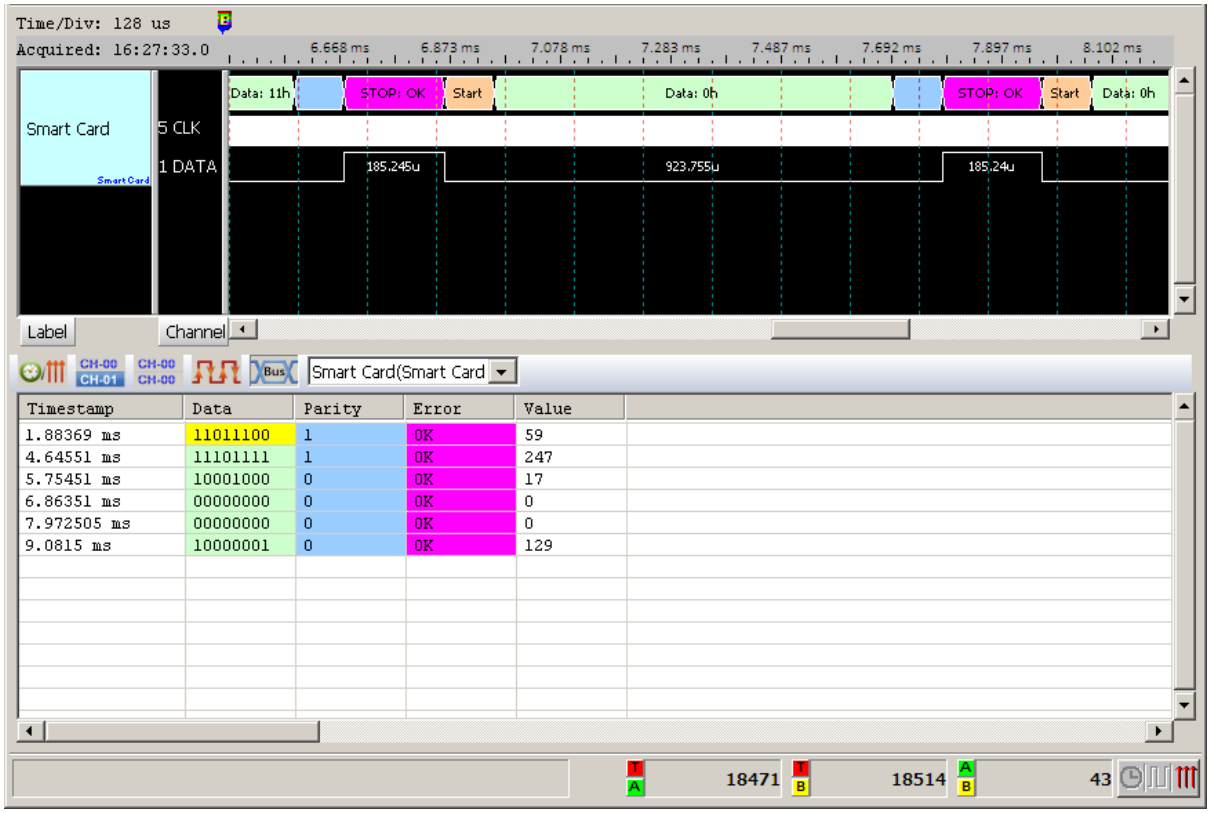
Settings



Channel: Show the selected channels (CLK and DATA) and the number of clocks within the bit (ETU).

Result

Click **OK** to run the Smart Card decode and see the result on the Waveform Window below.

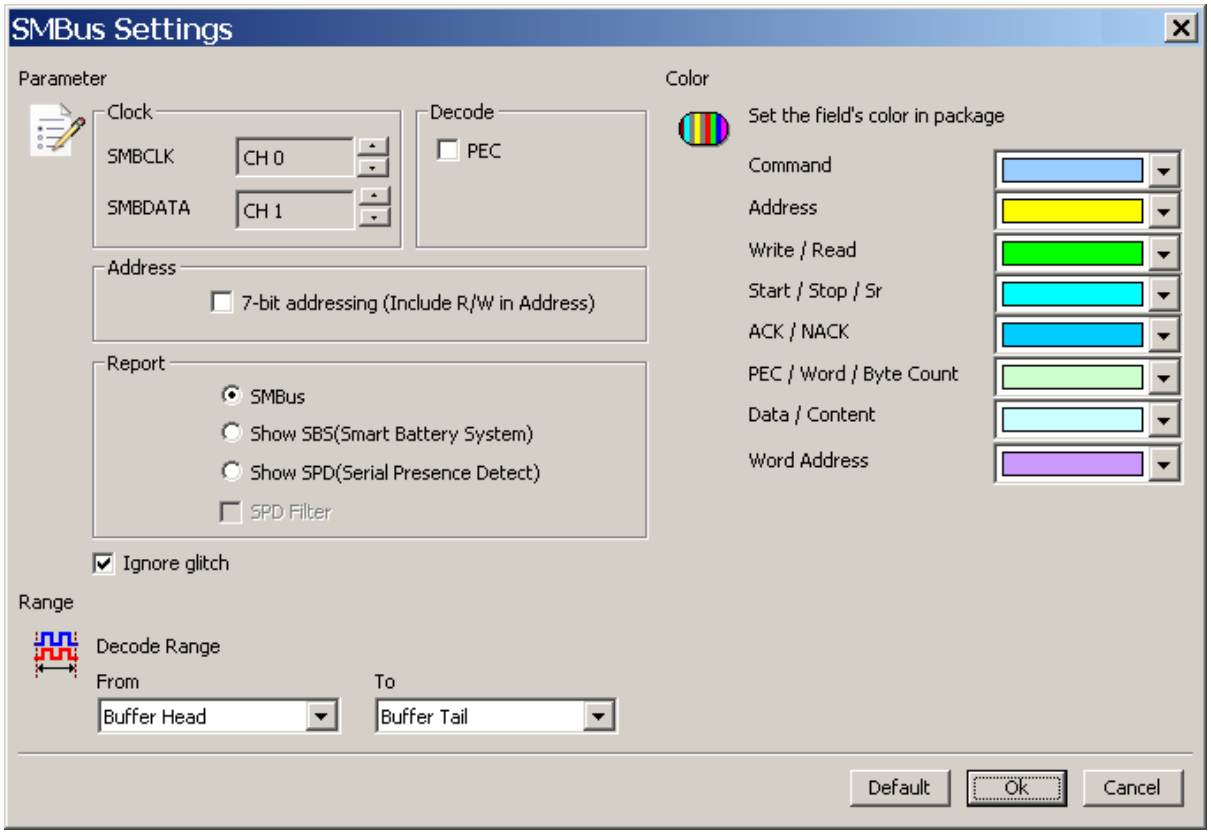


Timestamp	Data	Parity	Error	Value
1.88369 ms	11011100	1	OK	59
4.64551 ms	11101111	1	OK	247
5.75451 ms	10001000	0	OK	17
6.86351 ms	00000000	0	OK	0
7.972505 ms	00000000	0	OK	0
9.0815 ms	10000001	0	OK	129

System Management Bus (SMBus)

The SMBus (SMB) is a two-wire bus.

Settings



Clock: Show the selected channels (SMBCLK CH0 and SMBDATA CH1).

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

Show SBS (Smart Battery System): Show the Smart Battery System: voltage, electric current and the manufacturer.

Show SPD(Serial Presence Detect)：Report window show the configuration of memory module(DDR3, DDR2, DDR, SPD SDRAM) in EEPROM.

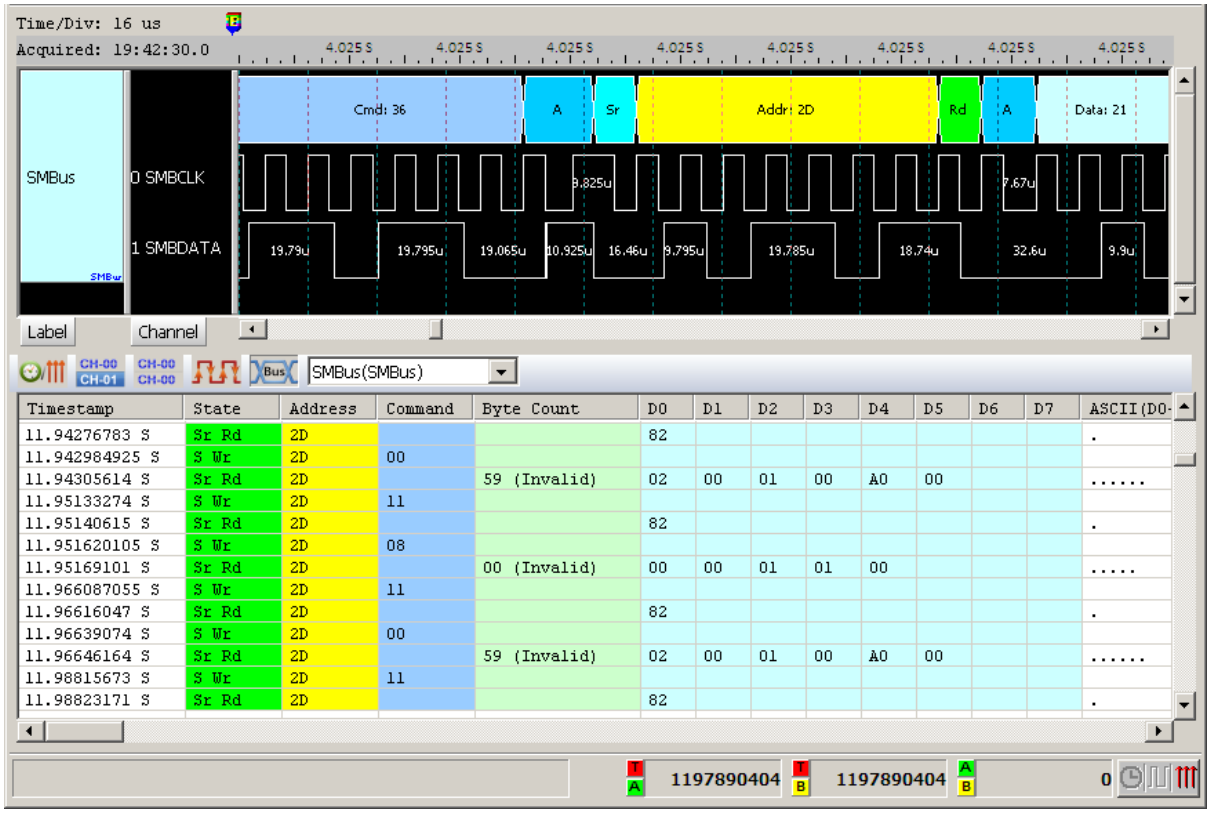
SBS/SPD Filter: Report window only show SBS/SPD packet.

Ignore glitch: Ignore the glitch when the slow transitions.

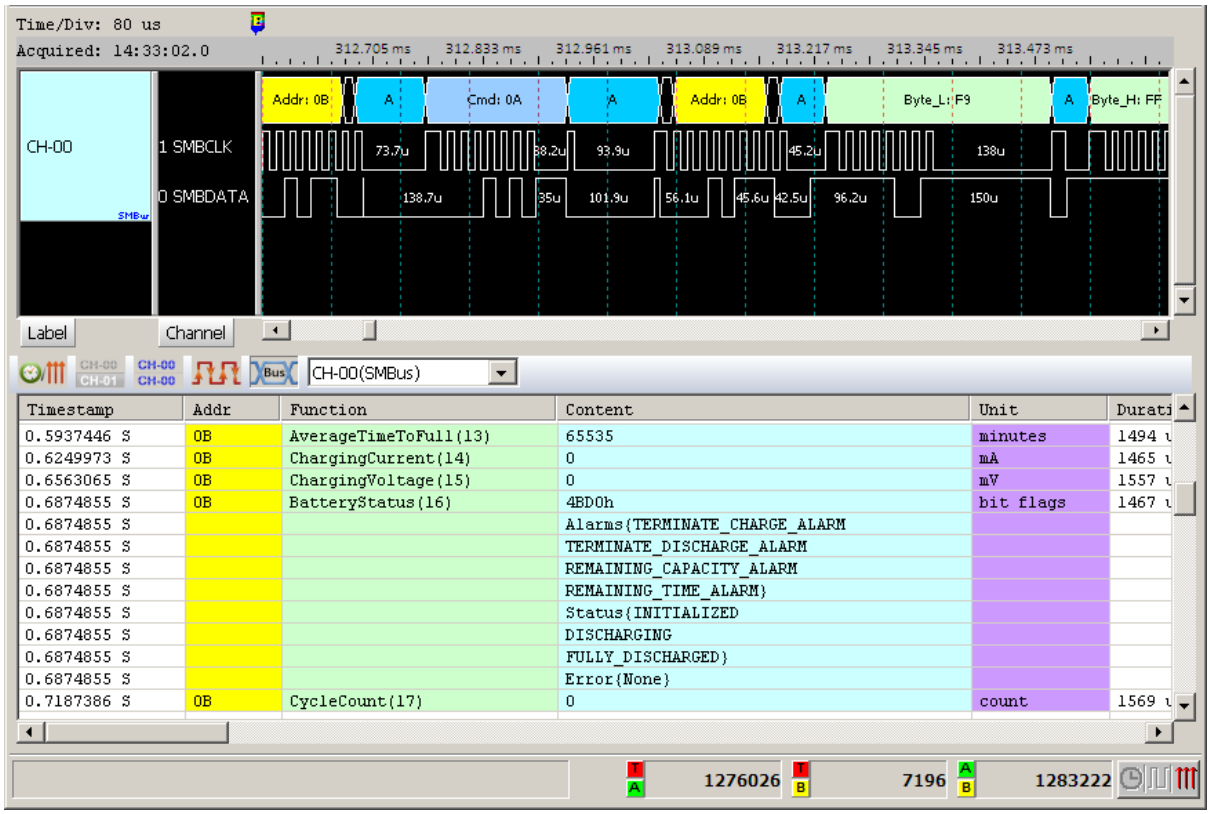
Result

Click **OK** to run the SMBus Decode and see the result on the Waveform Window below.

SMBus

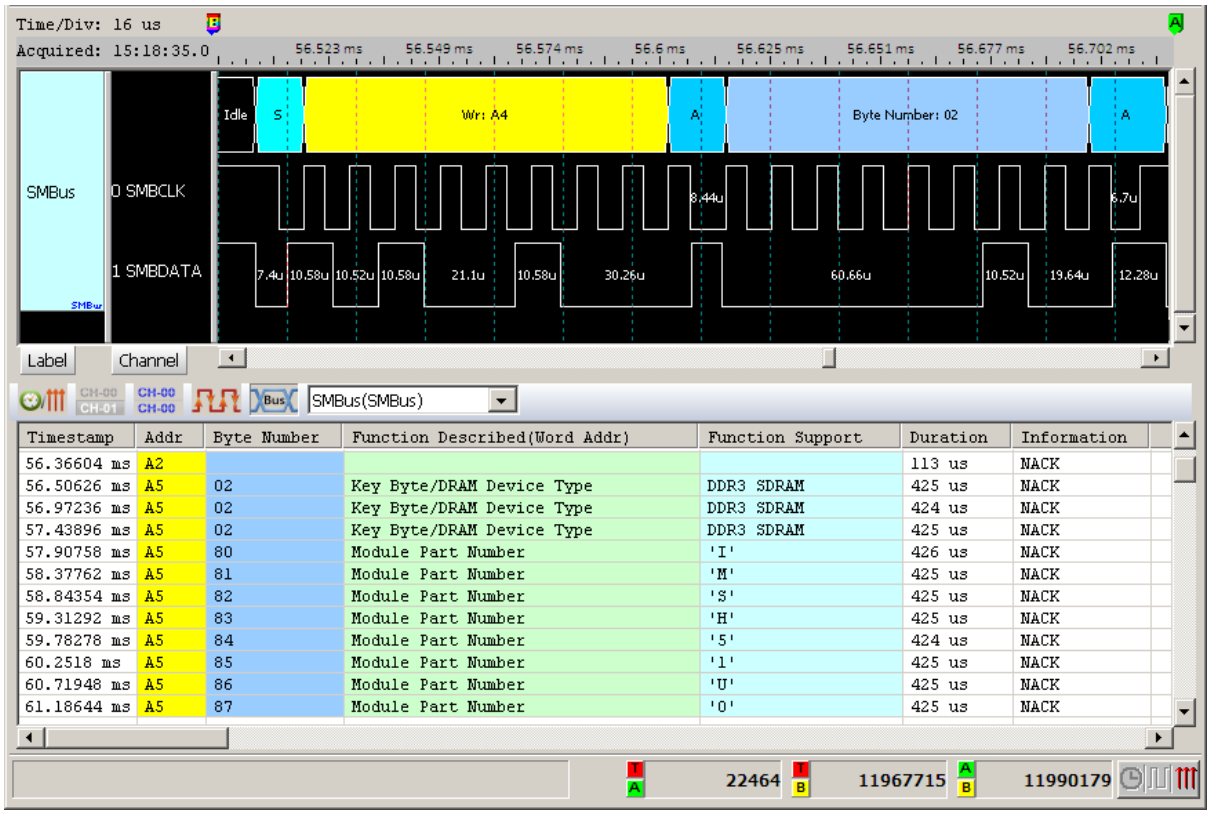


Show SBS (Smart Battery System)



Timestamp	Addr	Function	Content	Unit	Durati
0.5937446 S	0B	AverageTimeToFull(13)	65535	minutes	1494 u
0.6249973 S	0B	ChargingCurrent(14)	0	mA	1465 u
0.6563065 S	0B	ChargingVoltage(15)	0	mV	1557 u
0.6874855 S	0B	BatteryStatus(16)	4BD0h	bit flags	1467 u
0.6874855 S			Alarms{TERMINATE_CHARGE_ALARM		
0.6874855 S			TERMINATE_DISCHARGE_ALARM		
0.6874855 S			REMAINING_CAPACITY_ALARM		
0.6874855 S			REMAINING_TIME_ALARM}		
0.6874855 S			Status{INITIALIZED		
0.6874855 S			DISCHARGING		
0.6874855 S			FULLY_DISCHARGED}		
0.6874855 S			Error{None}		
0.7187386 S	0B	CycleCount(17)	0	count	1569 u

Show SPD (Serial Presence Detect)

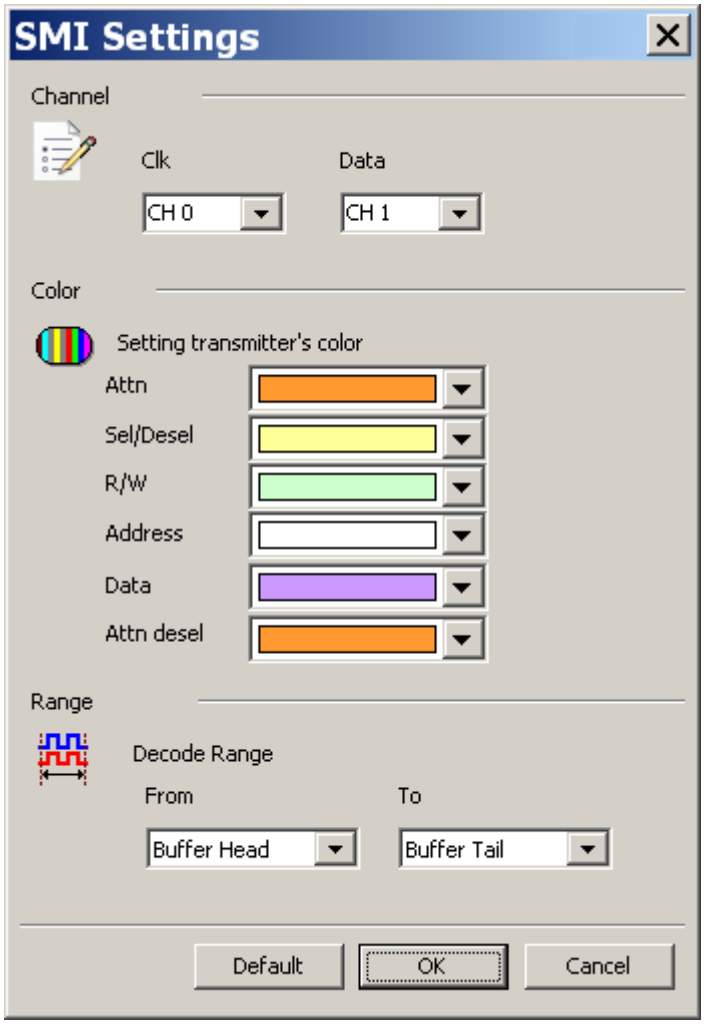


Timestamp	Addr	Byte Number	Function Described(Word Addr)	Function Support	Duration	Information
56.36604 ms	A2				113 us	NACK
56.50626 ms	A5	02	Key Byte/DRAM Device Type	DDR3 SDRAM	425 us	NACK
56.97236 ms	A5	02	Key Byte/DRAM Device Type	DDR3 SDRAM	424 us	NACK
57.43896 ms	A5	02	Key Byte/DRAM Device Type	DDR3 SDRAM	425 us	NACK
57.90758 ms	A5	80	Module Part Number	'I'	426 us	NACK
58.37762 ms	A5	81	Module Part Number	'M'	425 us	NACK
58.84354 ms	A5	82	Module Part Number	'S'	425 us	NACK
59.31292 ms	A5	83	Module Part Number	'H'	425 us	NACK
59.78278 ms	A5	84	Module Part Number	'5'	424 us	NACK
60.2518 ms	A5	85	Module Part Number	'1'	425 us	NACK
60.71948 ms	A5	86	Module Part Number	'U'	425 us	NACK
61.18644 ms	A5	87	Module Part Number	'0'	425 us	NACK

Serial Microprocessor Interface (SMI)

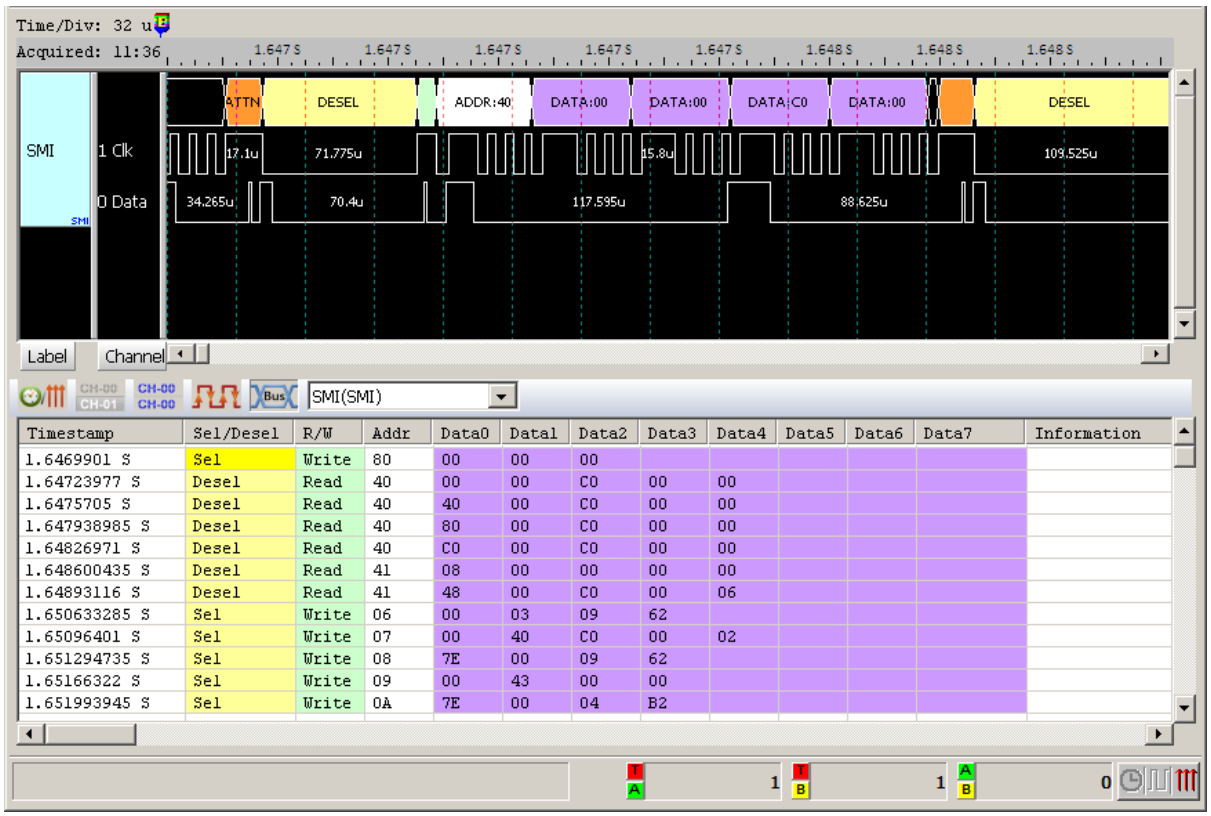
The SMI is a two-wire bus.

Settings



Channel: Show the selected channels (Clk and Data)

Result



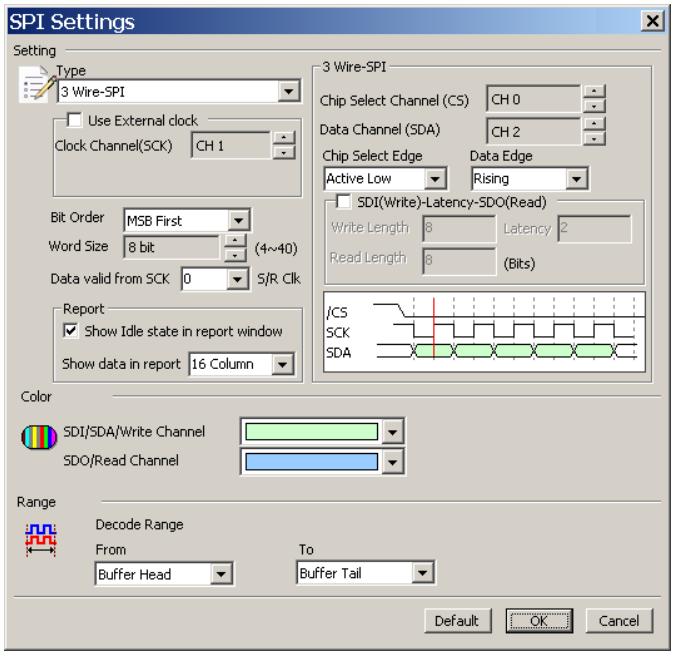
Timestamp	Sel/Desel	R/W	Addr	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Information
1.6469901 S	Sel	Write	80	00	00	00						
1.64723977 S	Desel	Read	40	00	00	C0	00	00				
1.6475705 S	Desel	Read	40	40	00	C0	00	00				
1.647938985 S	Desel	Read	40	80	00	C0	00	00				
1.64826971 S	Desel	Read	40	C0	00	C0	00	00				
1.648600435 S	Desel	Read	41	08	00	00	00	00				
1.64893116 S	Desel	Read	41	48	00	C0	00	06				
1.650633285 S	Sel	Write	06	00	03	09	62					
1.65096401 S	Sel	Write	07	00	40	C0	00	02				
1.651294735 S	Sel	Write	08	7E	00	09	62					
1.65166322 S	Sel	Write	09	00	43	00	00					
1.651993945 S	Sel	Write	0A	7E	00	04	B2					

Serial Peripheral Interface (SPI)

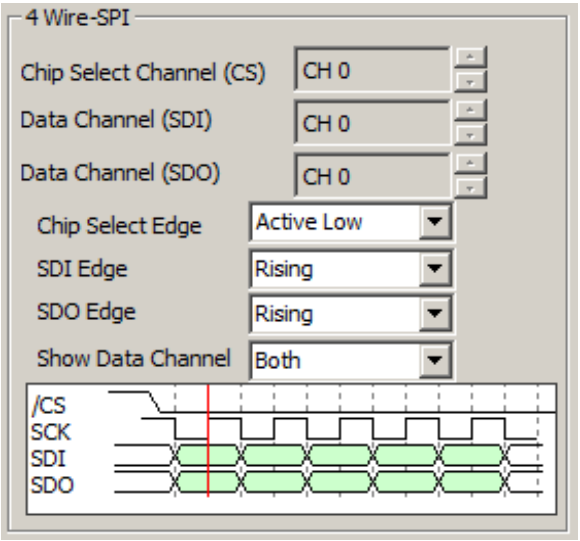
The SPI, is one kind of 4-wires synchronous serial data link. The SPI bus can be 4 wires, 3 wires, or 2 wires.

Settings

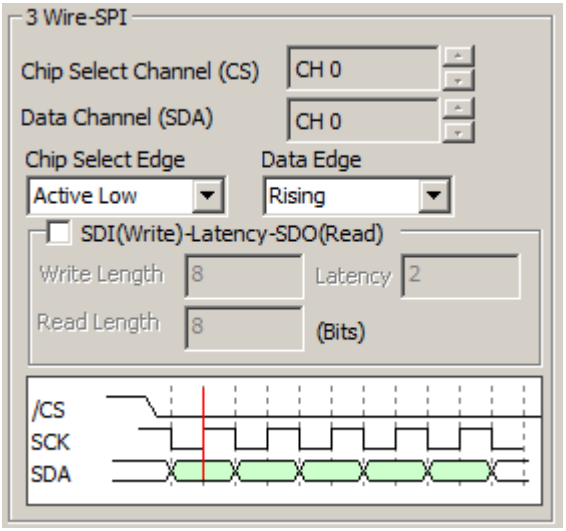
Type: The default is 3 Wire-SPI.



4 Wire-SPI dialog box ➔CS, SCK, SDI, SDO

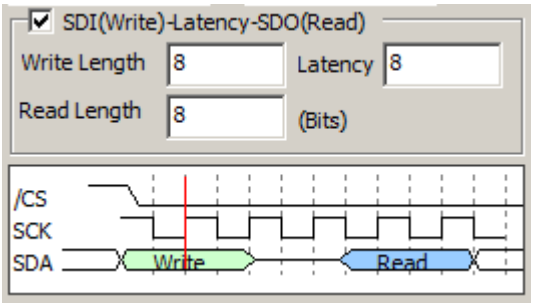


3 Wire-SPI dialog box ➔ CS, SCK, SDA

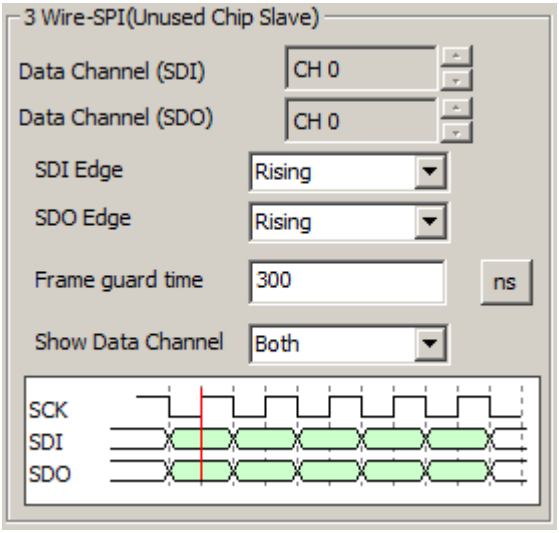


Click the SDI(Write)-Latency-SDO(Read) to show the dialog below.

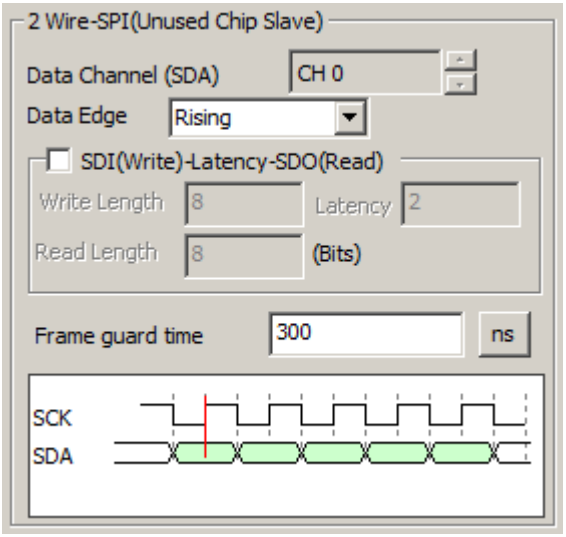
The maximum length is 65535 (Bits)



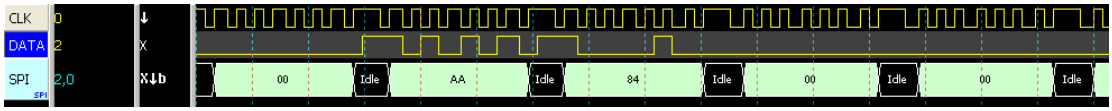
3 Wire-SPI (Unused Chip Slave) dialog box ➔ SCK, SDI, SDO

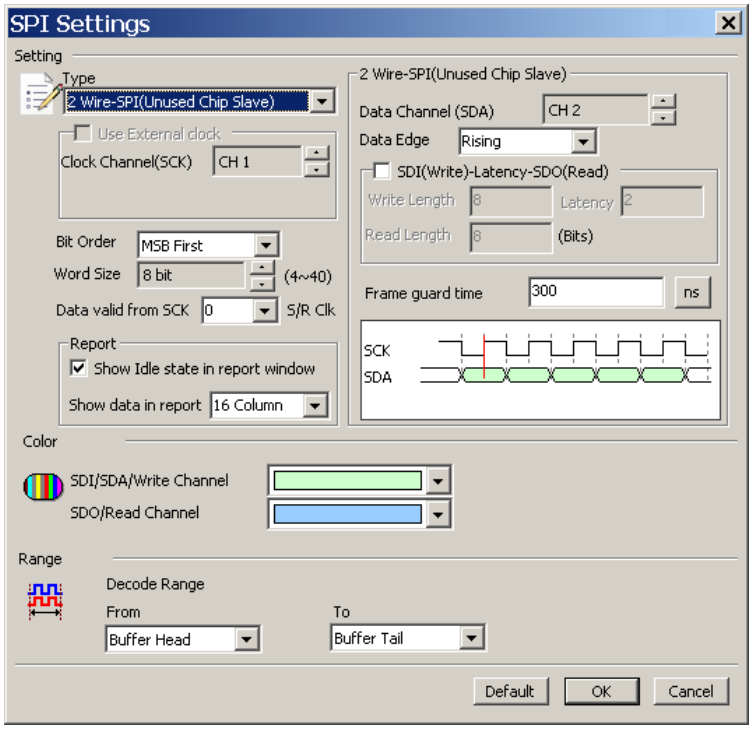


2 Wire-SPI (Unused Chip Slave) dialog box ➔ SCK, SDA

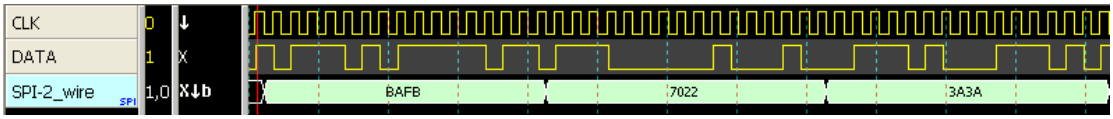


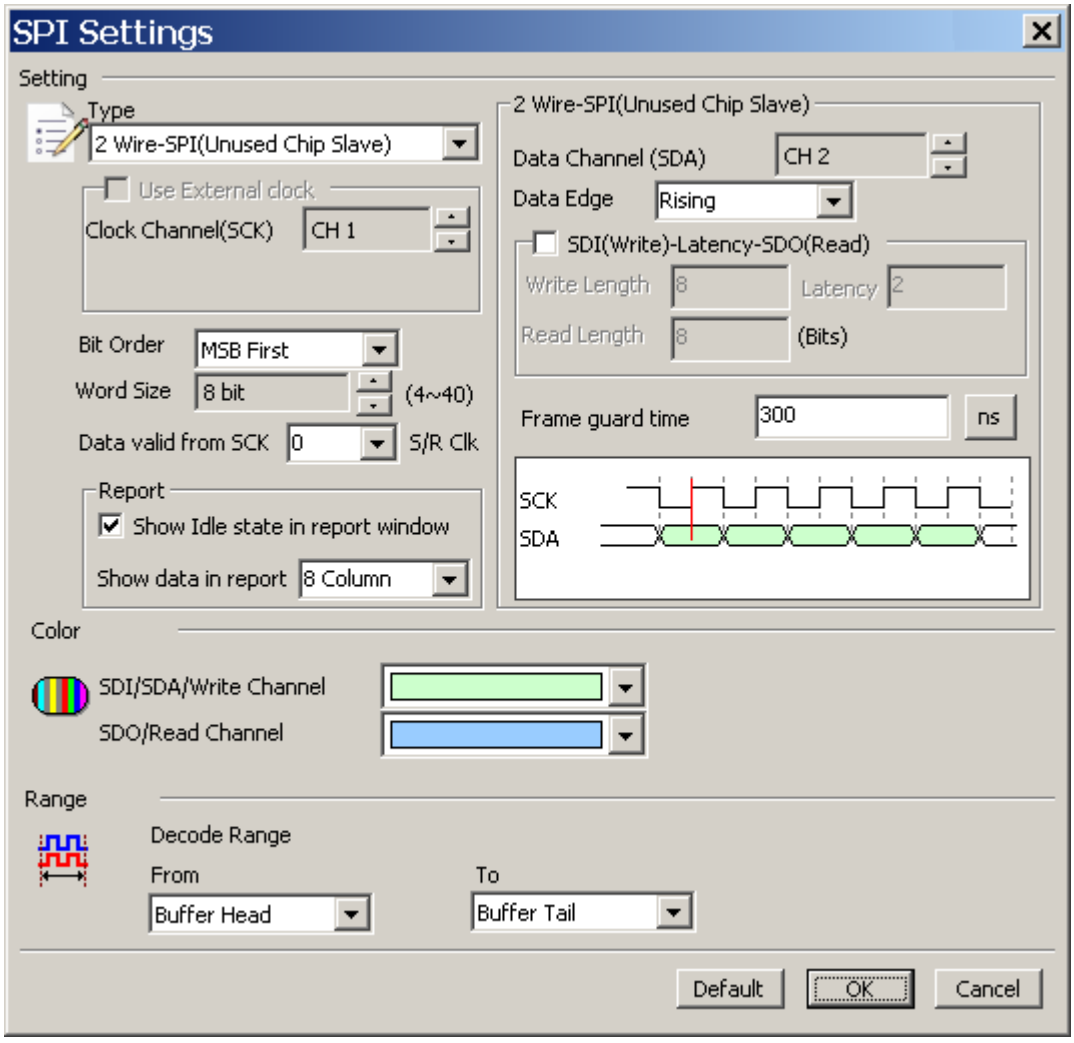
If the chip slave is not used and the interval between frames is not 0. You can set the interval as 6us, any data bit higher than 6us will be seen as Idle.



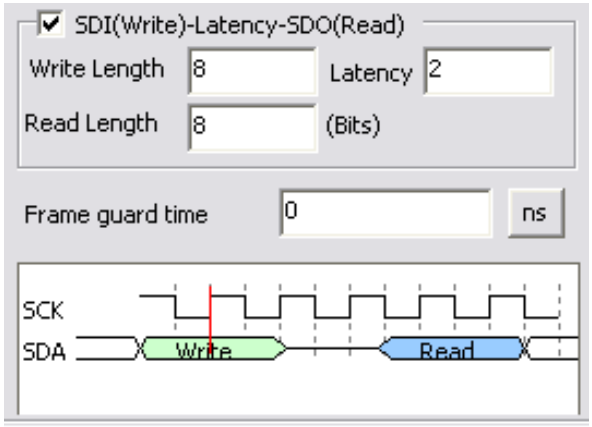


If the chip slave is not used and the interval between frames is 0. You can see the data continuous as the dialog below.





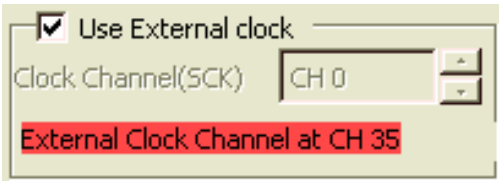
We also offer bi-direction mode as the dialog below.



C heck the SDI(Write)-Latency-SDO(Read)to set the bit numbers for the 3 columns;

Write and Read (1~65535), Latency (0~65535).

Use External clock: Connect to the last channel of your instrument.



Bit Order: MSB first or LSB first.

Word size: Default is 8 bits, minimum is 4 and maximum is 32.

Report: Show Idle state in report window, You can disable this default for not to display the idle state on the Report Window.

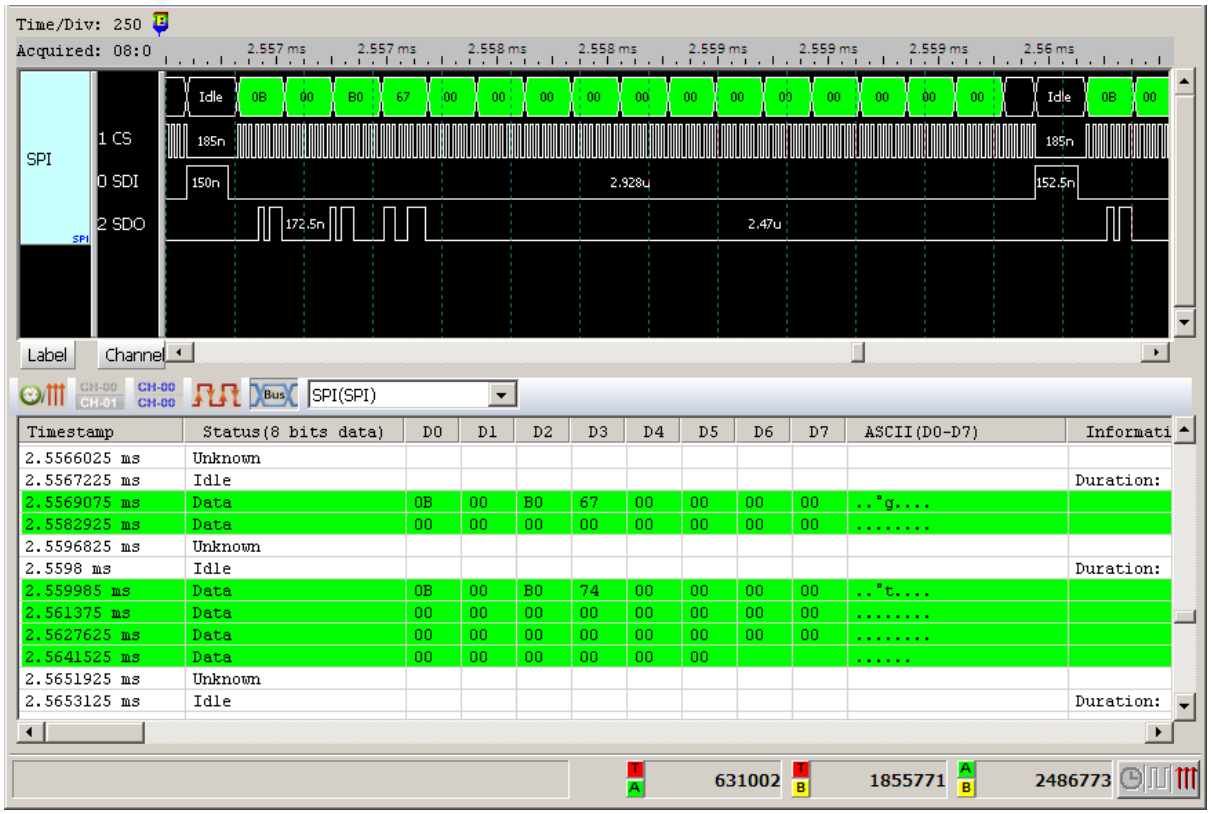
Show data in report: Display the ASCII code with default 16 columns on the Report Window.

Data Valid from SCK: In some SPI devices, the data is not valid right after the data output or the clock edge. You can set the data valid after 0-3 units of the sampling rate in Data valid from SCK; if the unit is 1 and the sampling rate is 200MHz, the delay time is 5 ns.

Result

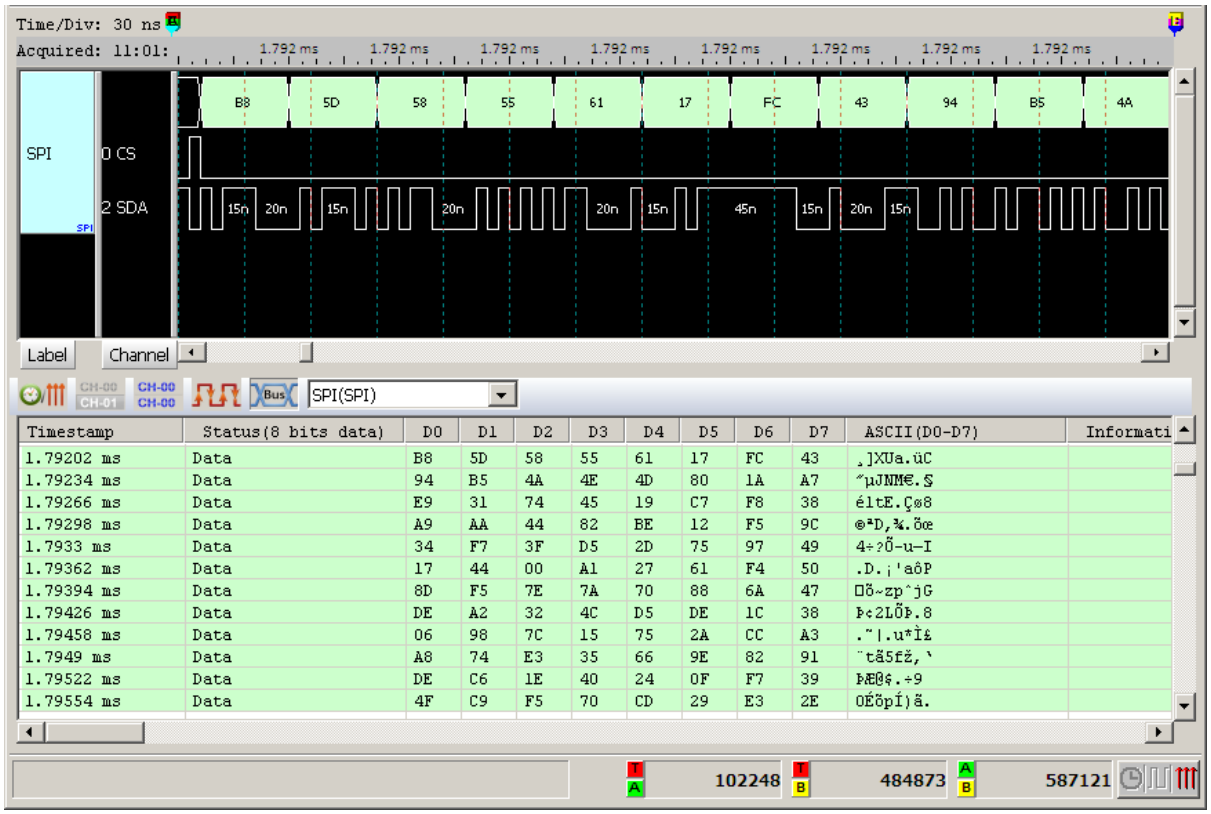
Click **OK** to run the SPI decode and see the result on the Waveform Window below.

3-Wire SPI, Internal clock mode



Timestamp	Status(8 bits data)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Informati
2.5566025 ms	Unknown										
2.5567225 ms	Idle										Duration:
2.5569075 ms	Data	0B	00	B0	67	00	00	00	00	..°g....	
2.5582925 ms	Data	00	00	00	00	00	00	00	00	....	
2.5596825 ms	Unknown										
2.5598 ms	Idle										Duration:
2.559985 ms	Data	0B	00	B0	74	00	00	00	00	..°t....	
2.561375 ms	Data	00	00	00	00	00	00	00	00	....	
2.5627625 ms	Data	00	00	00	00	00	00	00	00	....	
2.5641525 ms	Data	00	00	00	00	00	00			......	
2.5651925 ms	Unknown										
2.5653125 ms	Idle										Duration:

3-Wire SPI, External clock mode

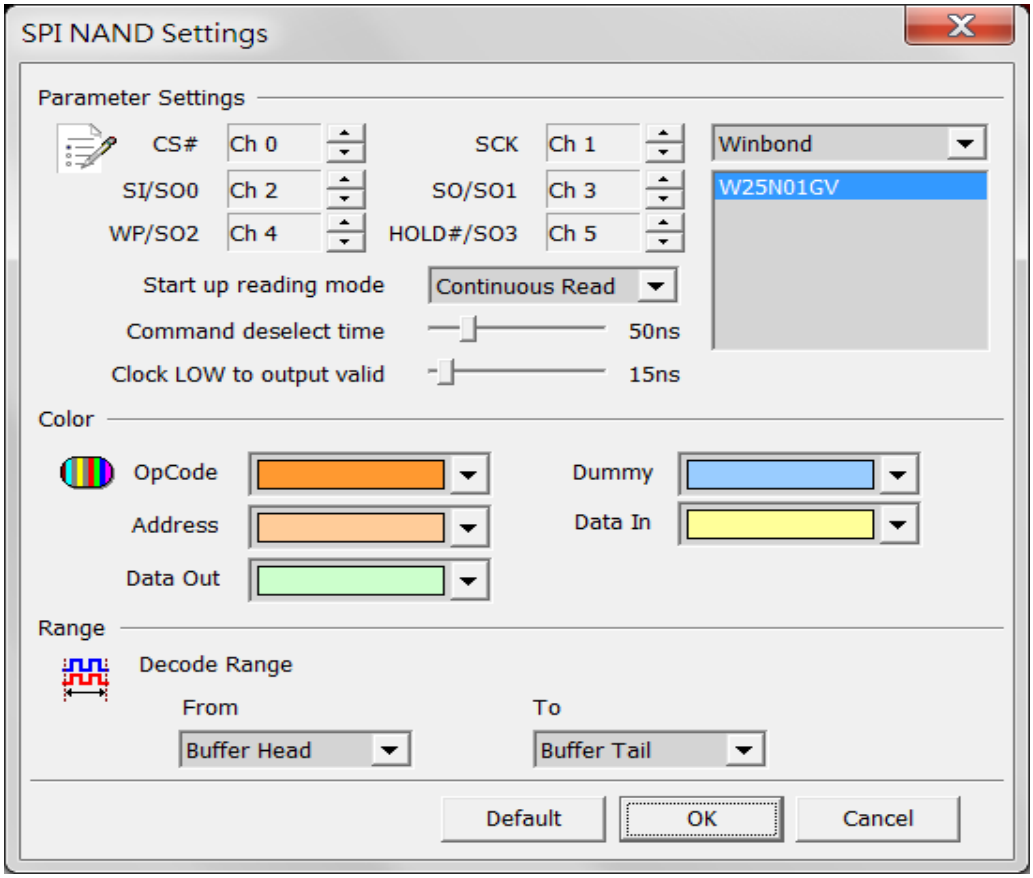


Timestamp	Status(8 bits data)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Informati
1.79202 ms	Data	B8	5D	58	55	61	17	FC	43	¸]XUa.üC	
1.79234 ms	Data	94	B5	4A	4E	4D	80	1A	A7	”µJNM€.§	
1.79266 ms	Data	E9	31	74	45	19	C7	F8	38	é1tE.Ç¤8	
1.79298 ms	Data	A9	AA	44	82	BE	12	F5	9C	©ªD‚¾.õœ	
1.7933 ms	Data	34	F7	3F	D5	2D	75	97	49	4÷?Õ-u—I	
1.79362 ms	Data	17	44	00	A1	27	61	F4	50	.D.¡'aôP	
1.79394 ms	Data	8D	F5	7E	7A	70	88	6A	47	õ~zpˆjG	
1.79426 ms	Data	DE	A2	32	4C	D5	DE	1C	38	Þ¢2LÕÞ.8	
1.79458 ms	Data	06	98	7C	15	75	2A	CC	A3	.˜|.u*Ì£	
1.7949 ms	Data	A8	74	E3	35	66	9E	82	91	¨tã5fž‚‘	
1.79522 ms	Data	DE	C6	1E	40	24	0F	F7	39	ÞÆ@$.÷9	
1.79554 ms	Data	4F	C9	F5	70	CD	29	E3	2E	OÉõpÍ)ã.	

Serial Peripheral Interface NAND (SPI NAND)

SPI NAND Flash is a SPI/QPI interfaced NAND flash memory. The decoder translates the bus signal to command/address/data field to provide an easier way to exam the SPI NAND waveform.

Settings



CS#: Chip select

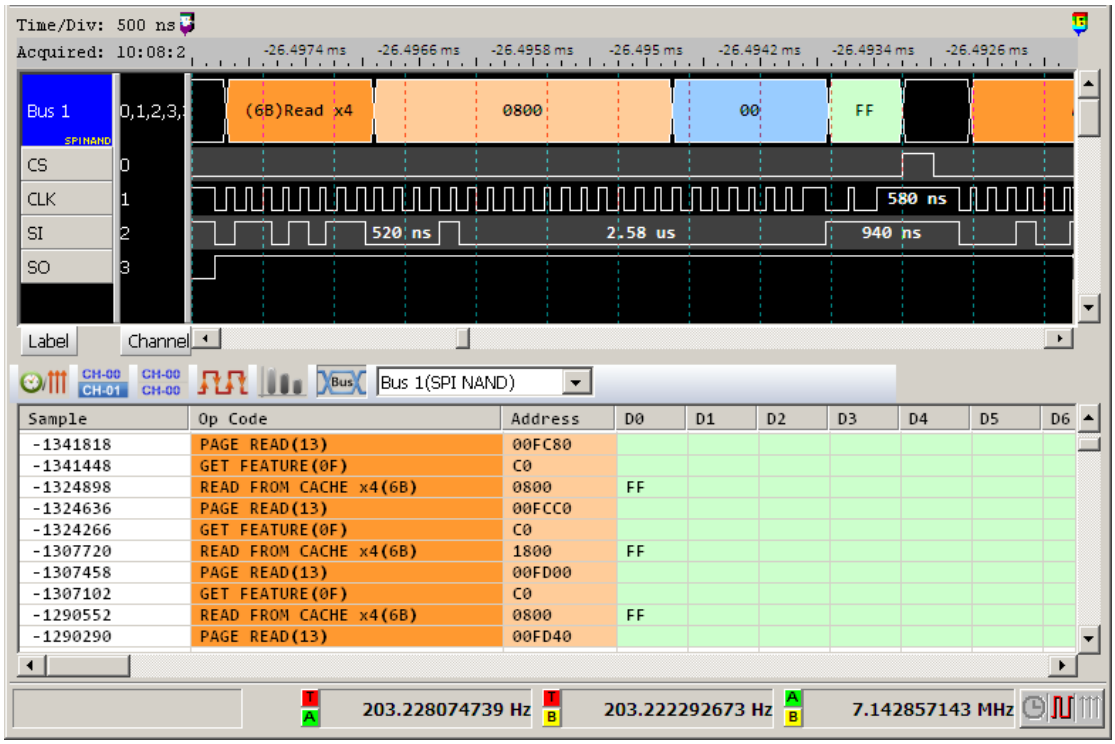
SCLK: Clock

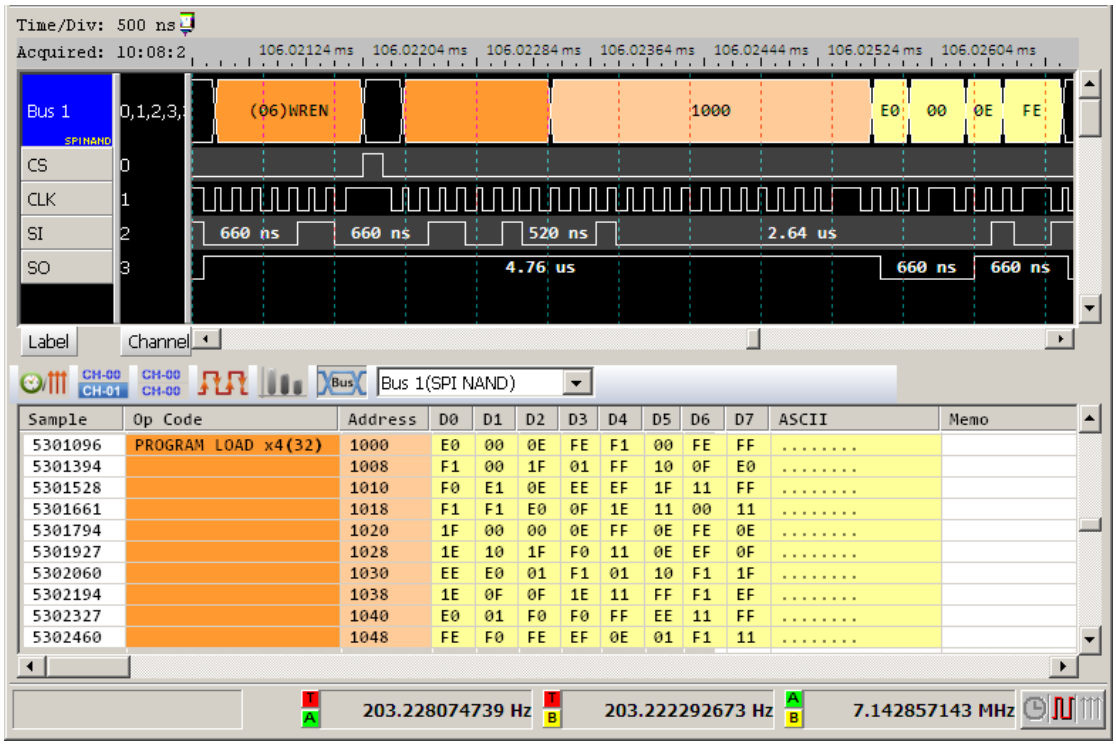
SIO0 – SIO3: Data

Start up reading mode: The initial setting of the reading mode for the decoder.

Command deselect time: The minimum required time for #CS deselecting. Clock LOW to output valid: The data probe time after clock falling.

Result

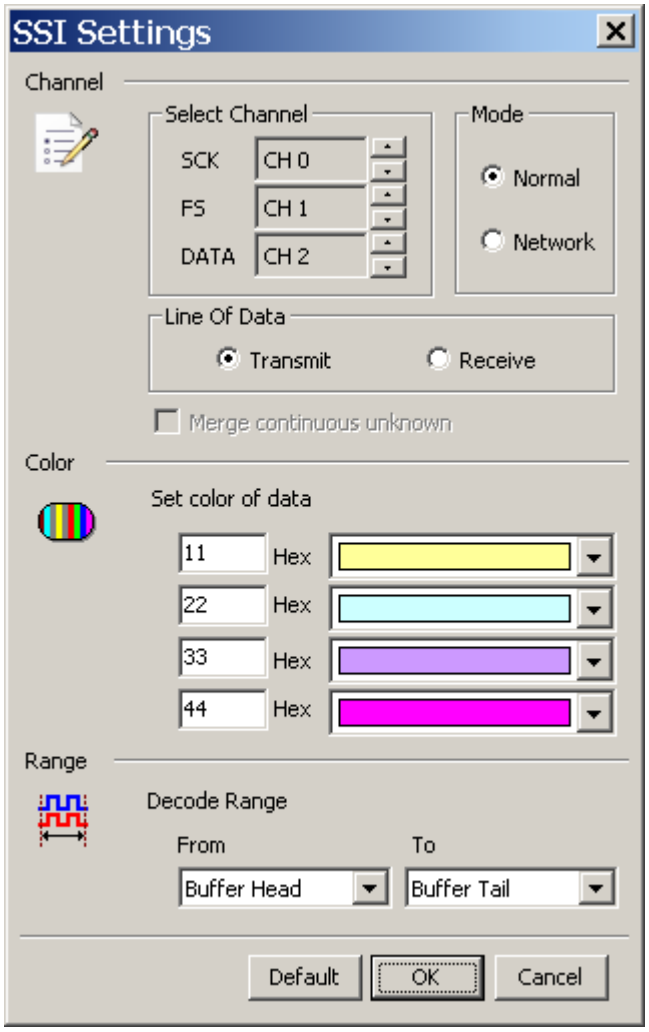




SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals: Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame Synchronous (FS). The SSI protocol supports either the Normal or Network mode that is independent of whether the transmitter and the receiver are synchronous or asynchronous.

Settings



Select Channel: Show the selected channels.

Mode: Normal or Network.

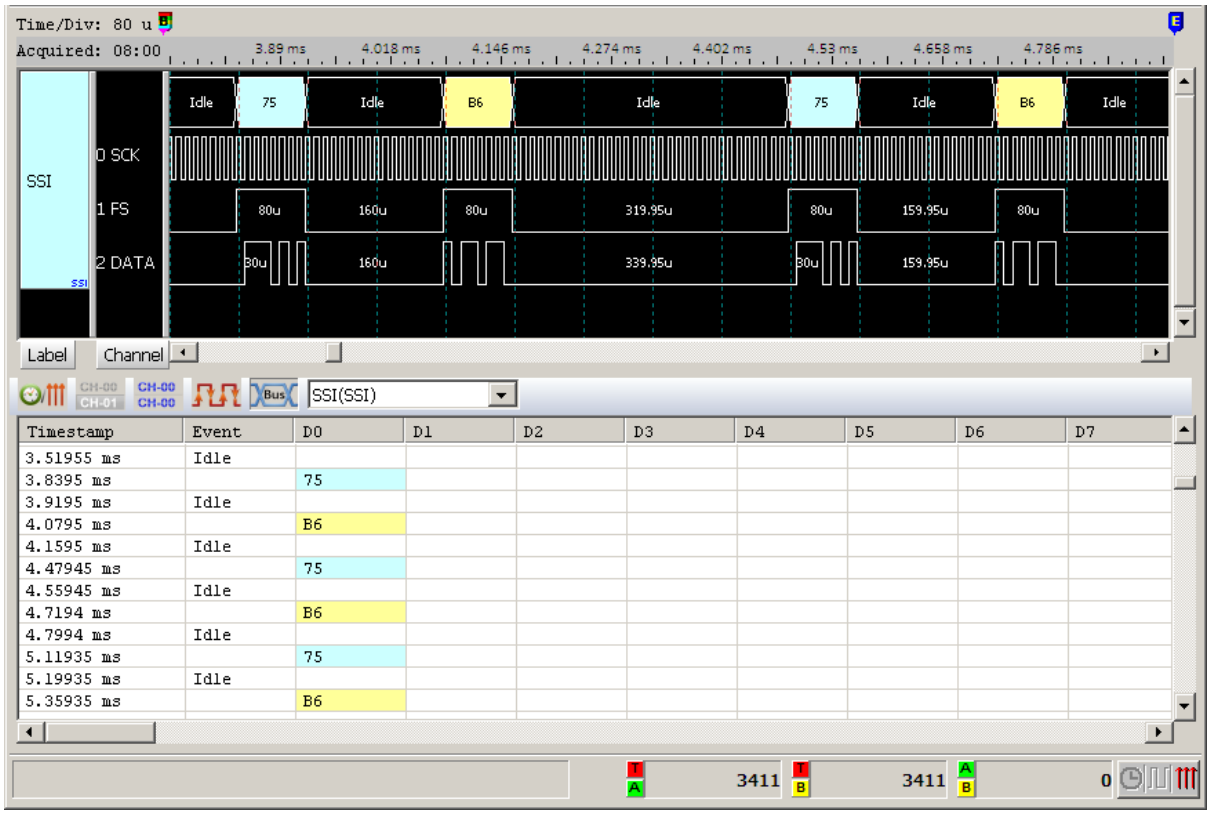
Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

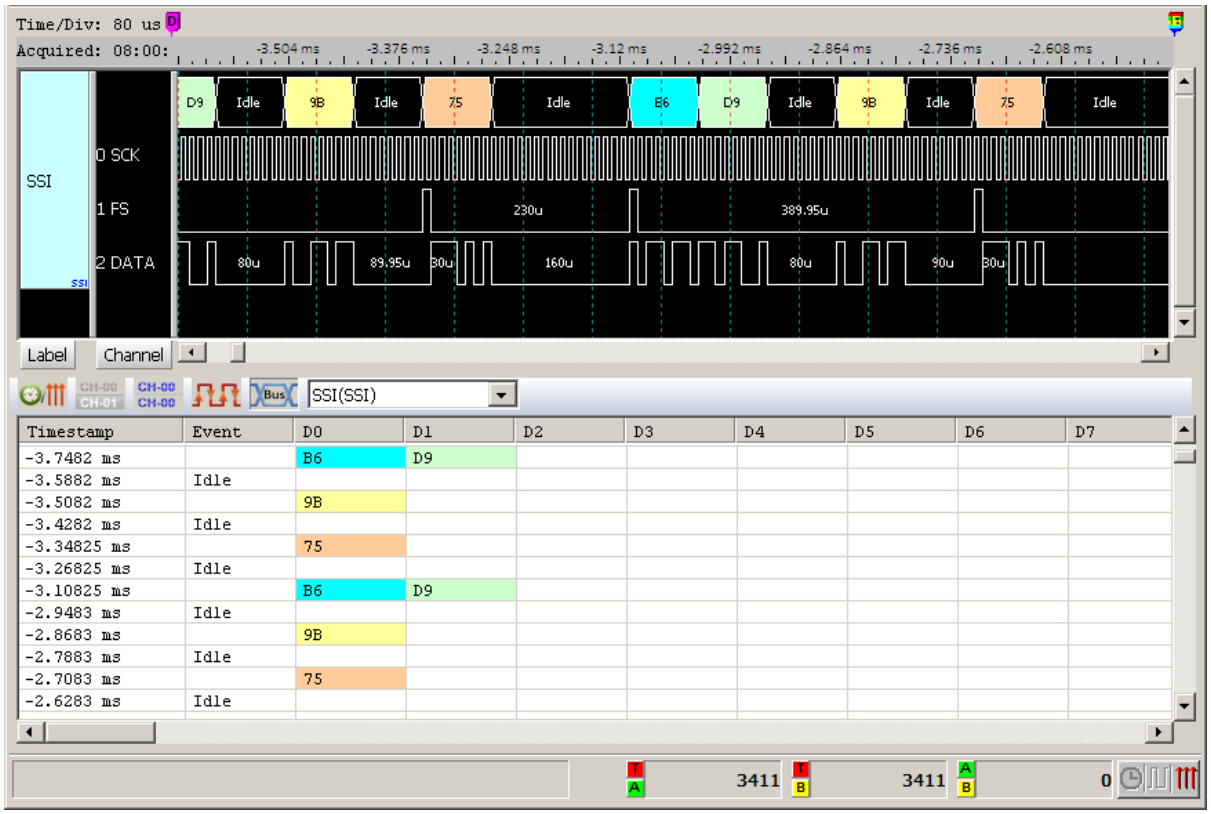
Result

Click **OK** to run SSI decode and see the result on the Report Window below.

Normal Transmit



Normal Receive



Network Transmit

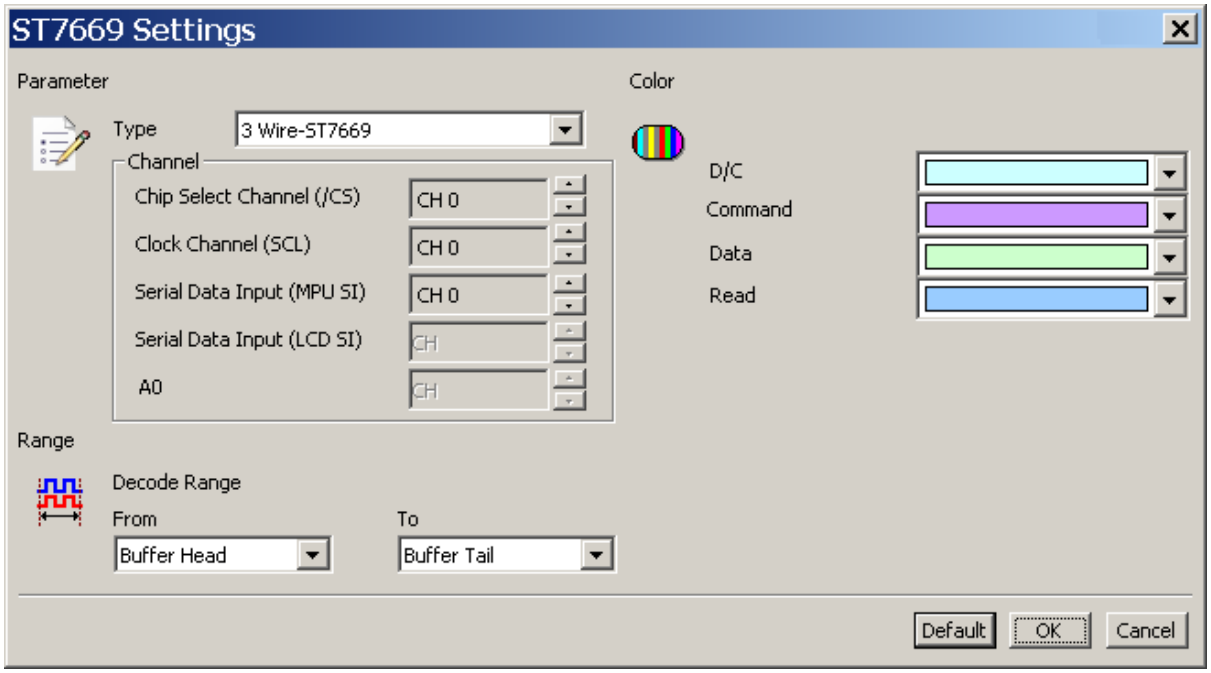
Network Receive

Timestamp	Event	D0	D1	D2	D3	D4	D5	D6
47.4456 ms		B6	D9					
47.60555 ms	Idle							
47.68555 ms		9B						
47.76555 ms	Idle							
47.84555 ms		75						
47.92555 ms	Idle							
48.0855 ms		B6	D9					
48.2455 ms	Idle							
48.3255 ms		9B						
48.40545 ms	Idle							
48.48545 ms		75						
48.56545 ms	Idle							

ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

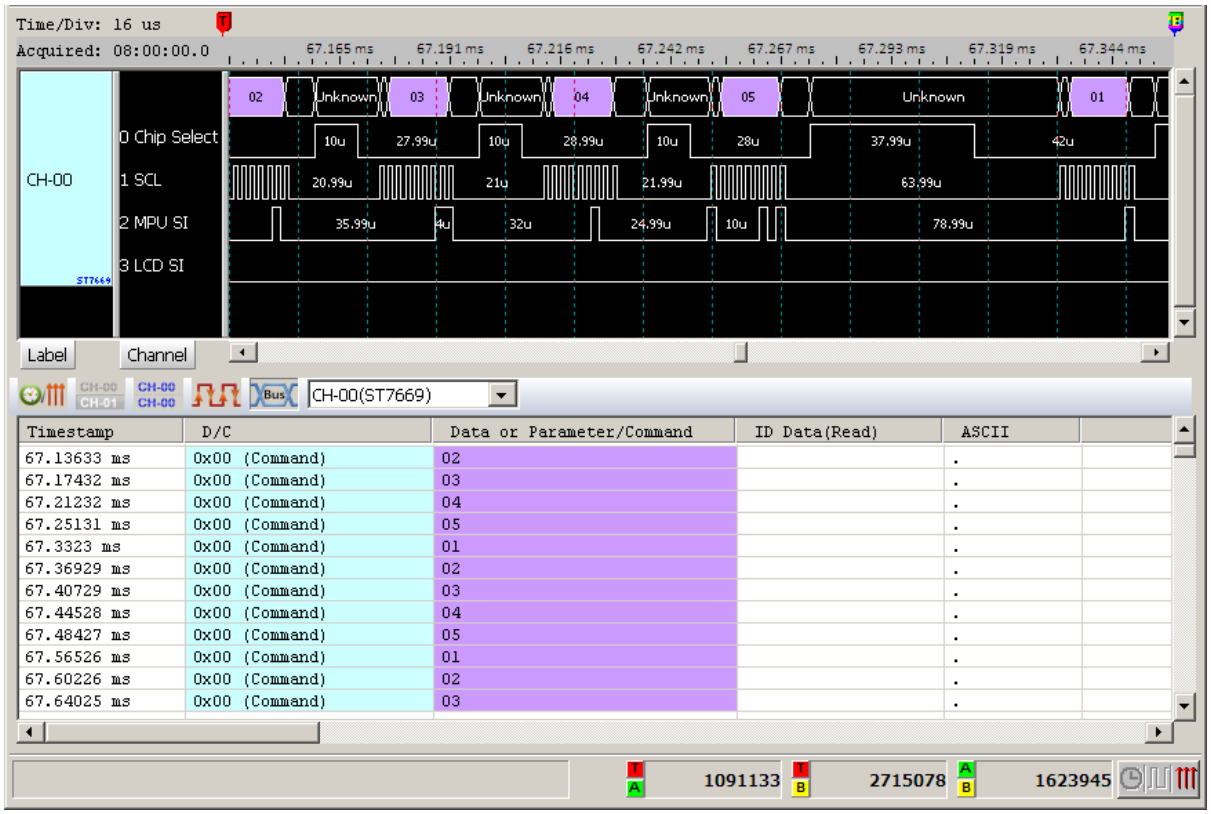
Settings



Channel: Show the selected channels.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window below.

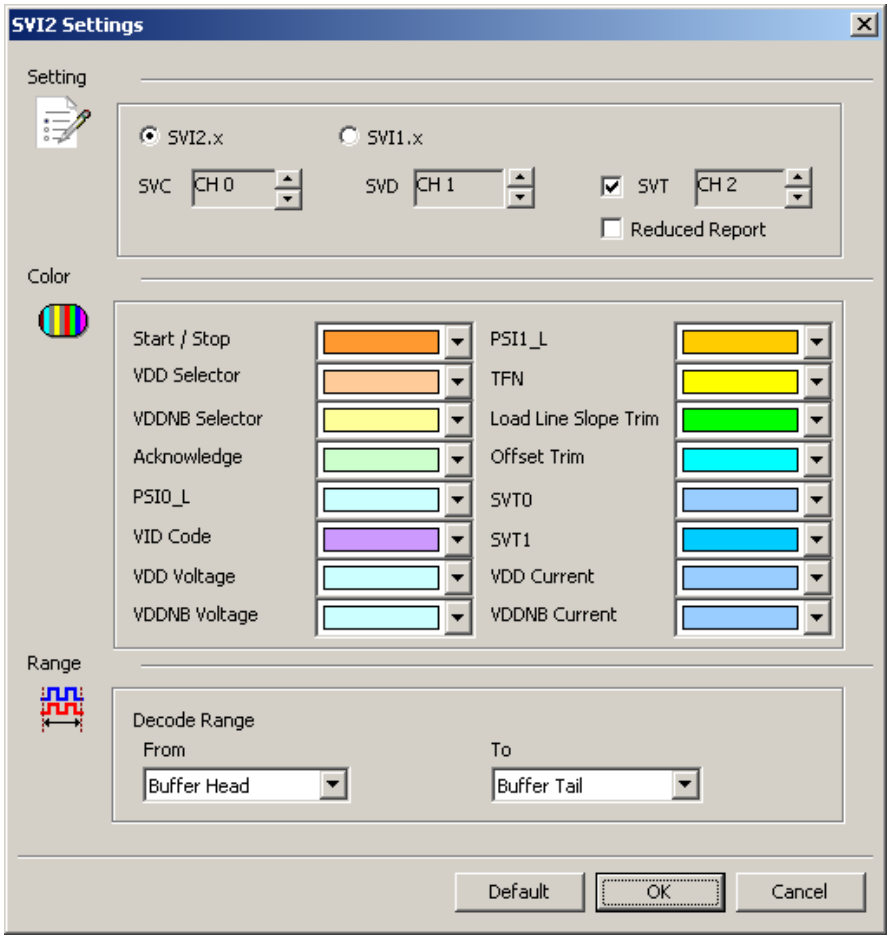


Serial VID Interface 2.0 (SVI2)

The SVI2 protocol is an interface for power management and developed by AMD.

The SVI2 working voltage is between 1V to 1.6V and its maximum frequency is at 20MHz with 3 bits： SVC/ SVD/ SVT.

Settings



SVC: SVI2 clock.

SVD: SVI2 data.

SVT: SVI2 telemetry data line. Telemetry will not be decoded if the SVT is not checked.

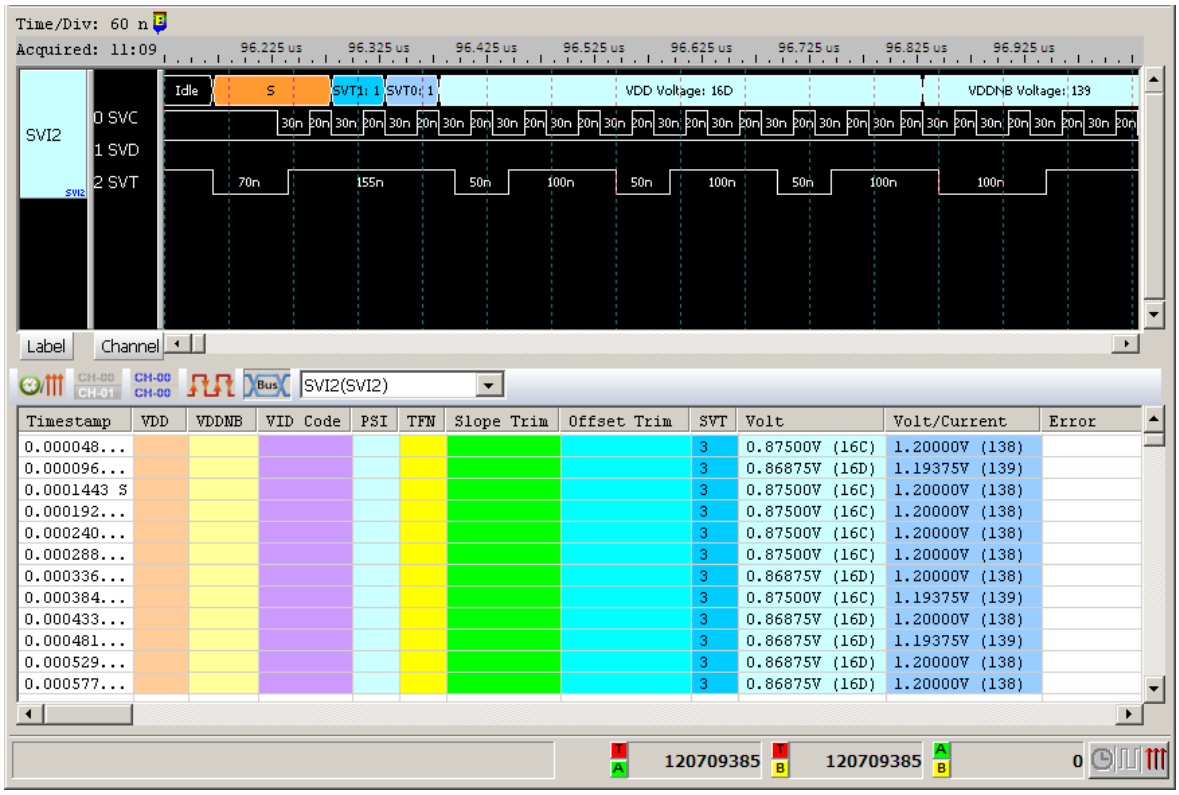
SVI2.x / SVI1.x: Select SVI2 / SVI protocol to decode.

Reduced Report: Only show SVD / VOTFC packet in the report window.

Result

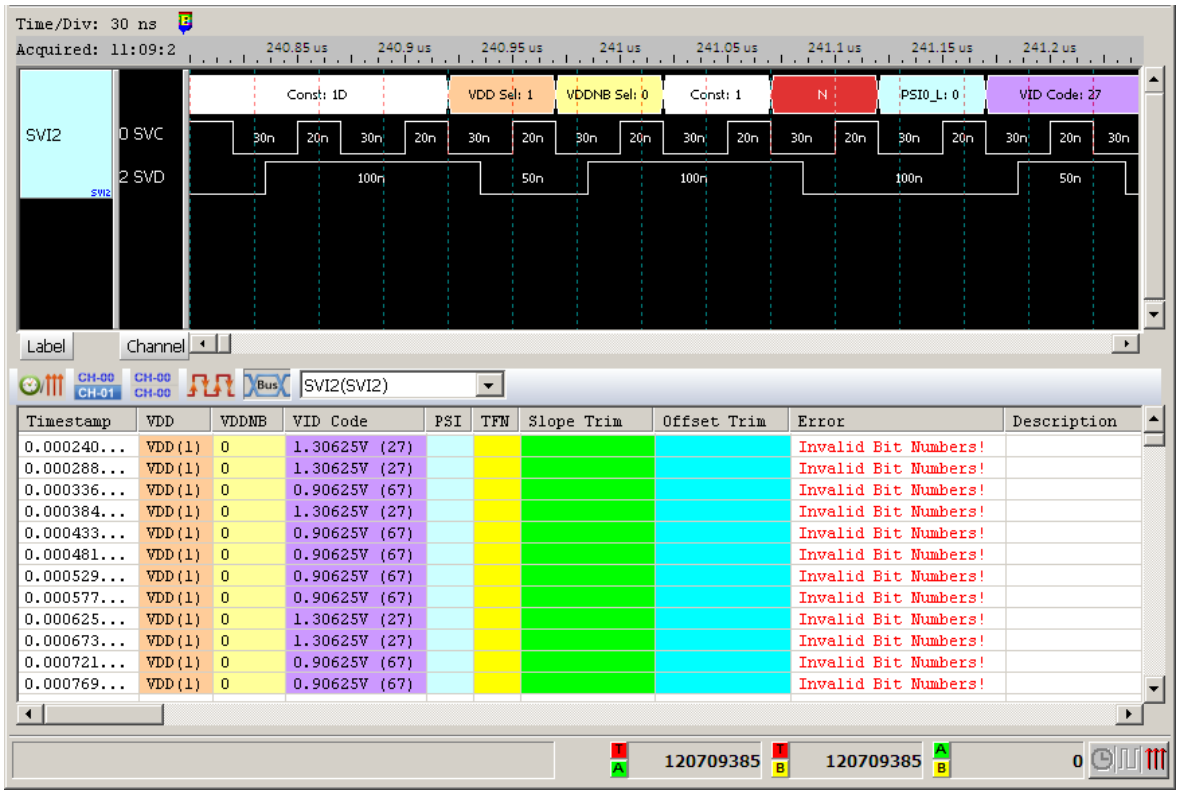
Click **OK** to run the SVI2 decode and see the result on the Waveform Window below.

Show SVT



Timestamp	VDD	VDDNB	VID Code	PSI	TFN	Slope Trim	Offset Trim	SVT	Volt	Volt/Current	Error
0.000048...								3	0.87500V (16C)	1.20000V (138)	
0.000096...								3	0.86875V (16D)	1.19375V (139)	
0.0001443 S								3	0.87500V (16C)	1.20000V (138)	
0.000192...								3	0.87500V (16C)	1.20000V (138)	
0.000240...								3	0.87500V (16C)	1.20000V (138)	
0.000288...								3	0.87500V (16C)	1.20000V (138)	
0.000336...								3	0.86875V (16D)	1.20000V (138)	
0.000384...								3	0.87500V (16C)	1.19375V (139)	
0.000433...								3	0.86875V (16D)	1.20000V (138)	
0.000481...								3	0.86875V (16D)	1.19375V (139)	
0.000529...								3	0.86875V (16D)	1.20000V (138)	
0.000577...								3	0.86875V (16D)	1.20000V (138)	

Without SVT



Timestamp	VDD	VDDNB	VID Code	PSI	TFN	Slope Trim	Offset Trim	Error	Description
0.000240...	VDD(1)	0	1.30625V (27)					Invalid Bit Numbers!	
0.000288...	VDD(1)	0	1.30625V (27)					Invalid Bit Numbers!	
0.000336...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	
0.000384...	VDD(1)	0	1.30625V (27)					Invalid Bit Numbers!	
0.000433...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	
0.000481...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	
0.000529...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	
0.000577...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	
0.000625...	VDD(1)	0	1.30625V (27)					Invalid Bit Numbers!	
0.000673...	VDD(1)	0	1.30625V (27)					Invalid Bit Numbers!	
0.000721...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	
0.000769...	VDD(1)	0	0.90625V (67)					Invalid Bit Numbers!	

Serial VID (SVID) (Upon Request)

Serial VID (SVID) protocol is for power management and developed by Intel. SVID voltage is between 1.0V to 1.1V, maximum frequency at 26.25MHz and is 3 wires：SCLK/ SDATA/ ALERT.

Supported version:

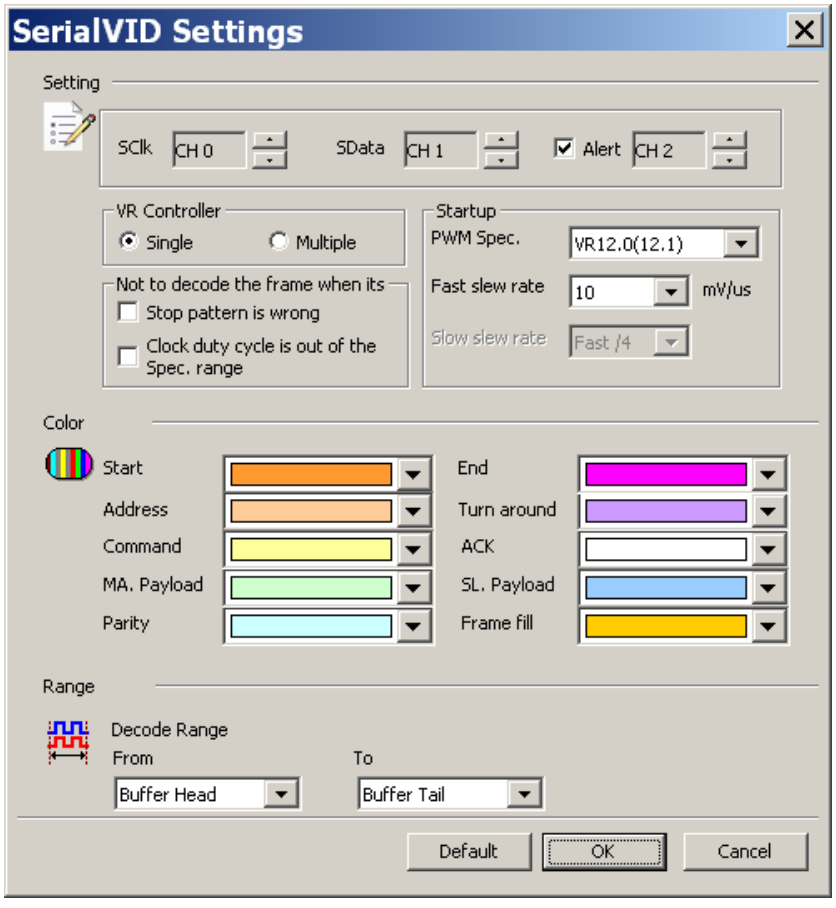
IMVP7/VR12, VR12.1, VR12.5, VR12.6

IMVP8/VR13

IMVP9/VR14

If you have any issues with SVID protocol features, please contact your Intel Field Representative.

Settings



SClk: SVID clock.

SData: SVID data.

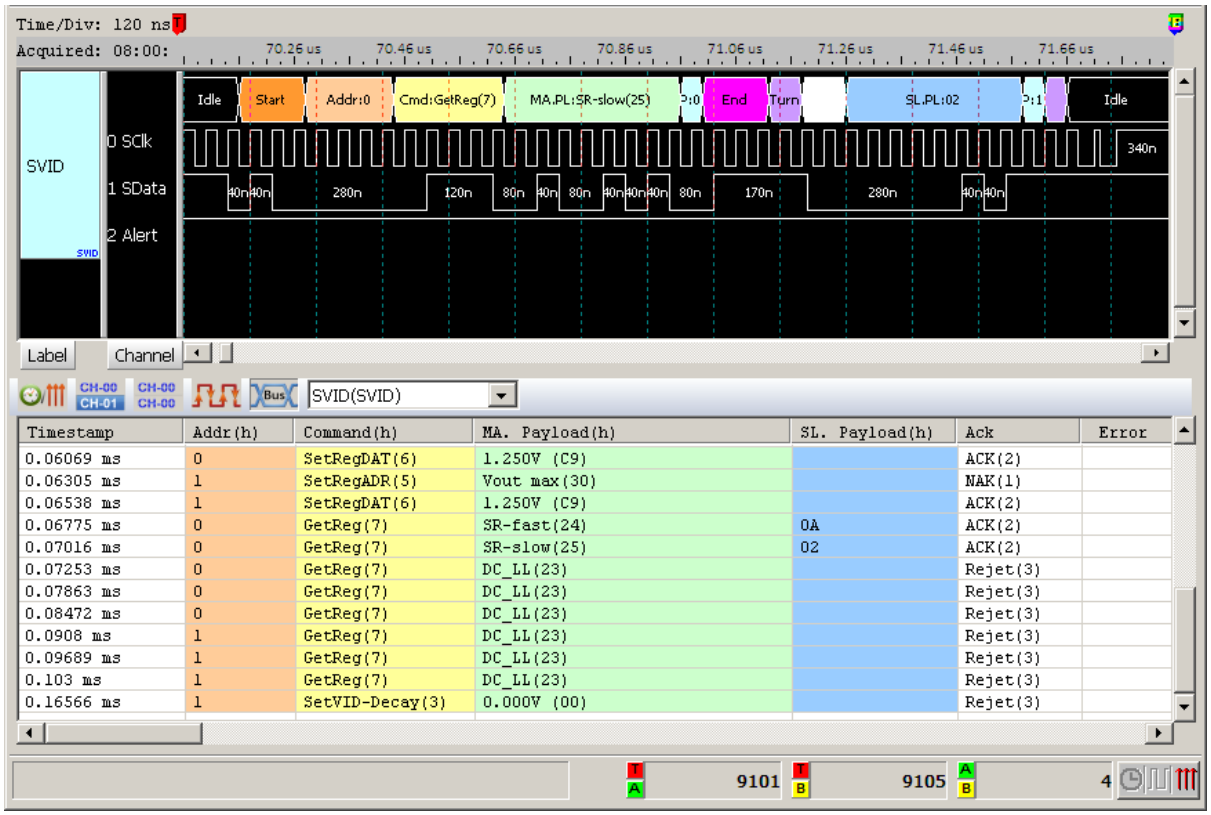
Alert: Alert, optional reminder.

VR Controller: Set single or multiple controllers in current VR. Set different address.

Not to decode the frame when its stop pattern wrong or clock duty cycle is out of range.

Result

Click OK to run the SVID decode and see the result on the Waveform Window below.

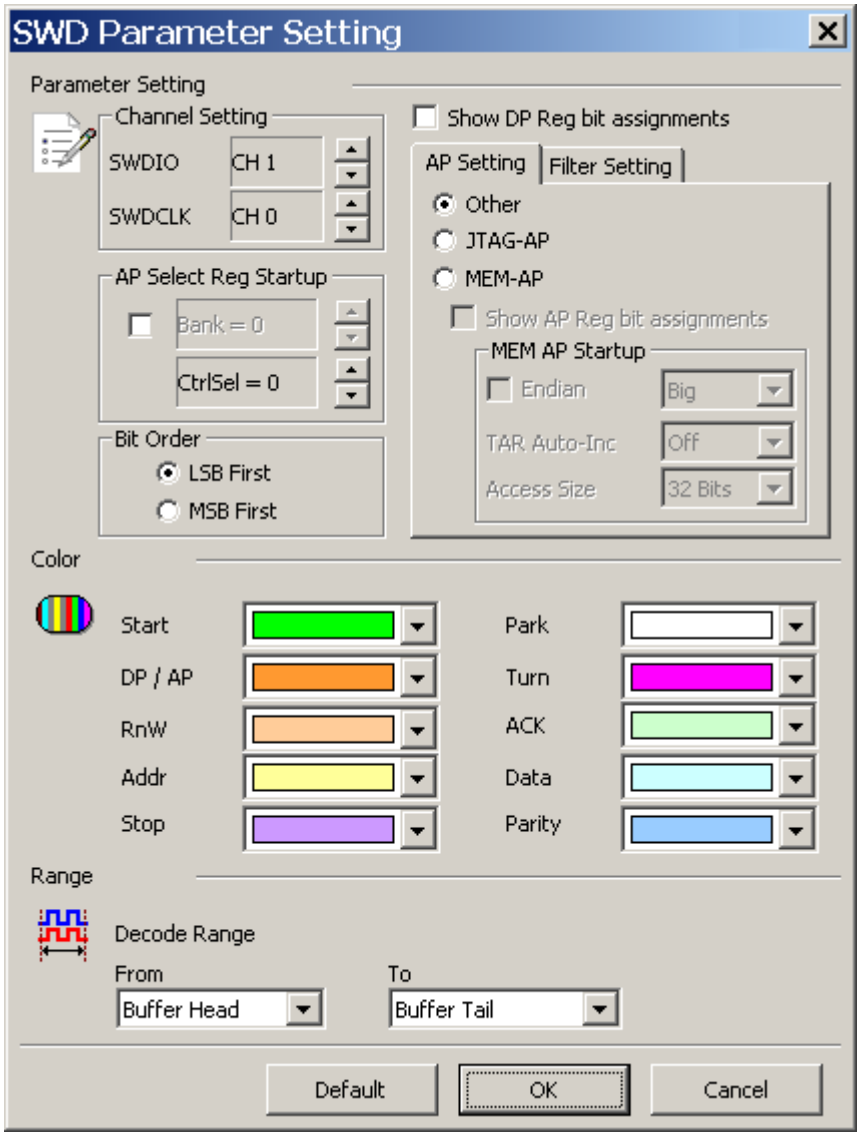


Timestamp	Addr(h)	Command(h)	MA. Payload(h)	SL. Payload(h)	Ack	Error
0.06069 ms	0	SetRegDAT(6)	1.250V (C9)		ACK(2)	
0.06305 ms	1	SetRegADR(5)	Vout max(30)		NAK(1)	
0.06538 ms	1	SetRegDAT(6)	1.250V (C9)		ACK(2)	
0.06775 ms	0	GetReg(7)	SR-fast(24)	0A	ACK(2)	
0.07016 ms	0	GetReg(7)	SR-slow(25)	02	ACK(2)	
0.07253 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.07863 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.08472 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.0908 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.09689 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.103 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.16566 ms	1	SetVID-Decay(3)	0.000V (00)		Rejet(3)	

Serial Wire Debug (SWD)

The SWD is a 2-pin electrical alternative JTAG interface that has the same JTAG protocol on top. It uses the existing GND connection. SWD uses an ARM CPU standard bi-directional wire protocol, defined in the ARM Debug Interface v5.

Settings

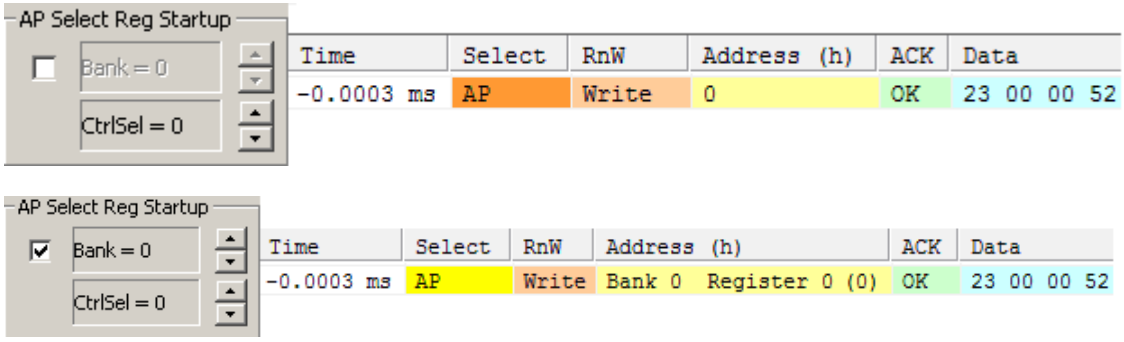


SWDIO: I/O data.

SWDCLK: Clock.

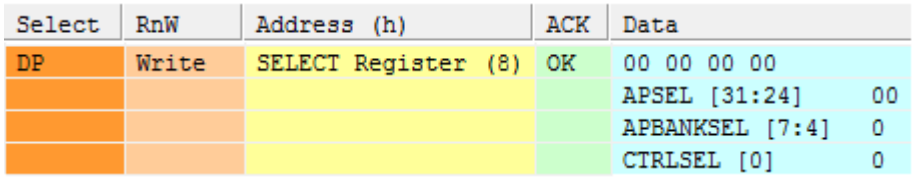
AP Select Reg Startup: When the AP Select Reg Startup is not assigned, only the

address information will be shown. You may input the Bank and Ctrl/Select initial values manually.



Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

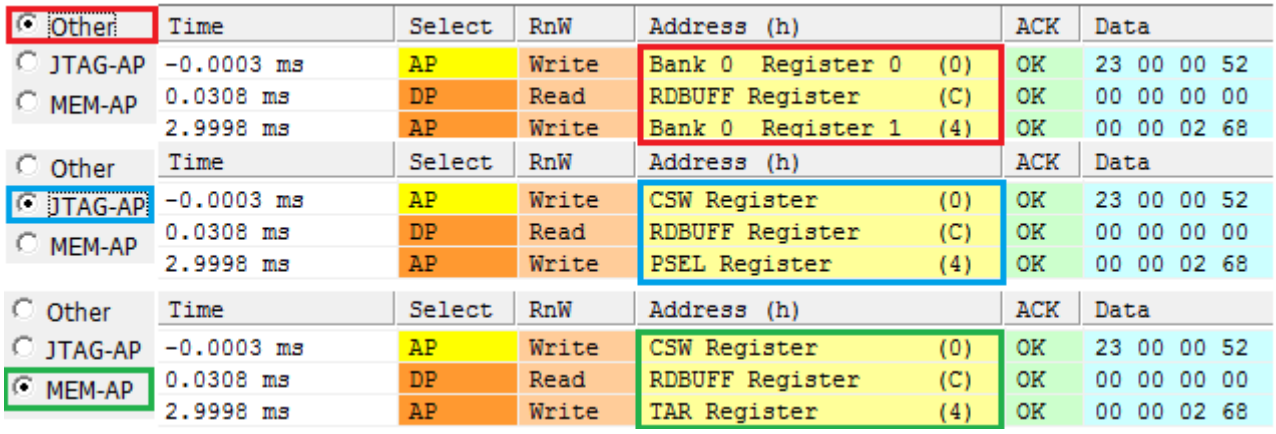


AP Setting:

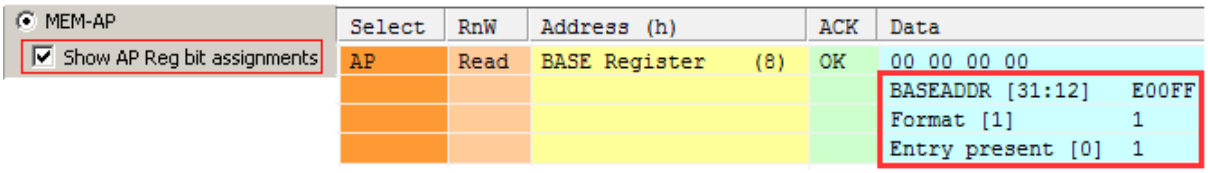
JTAG-AP: Show the JTAG AP decode.

MEM-AP: Show the MEM AP decode.

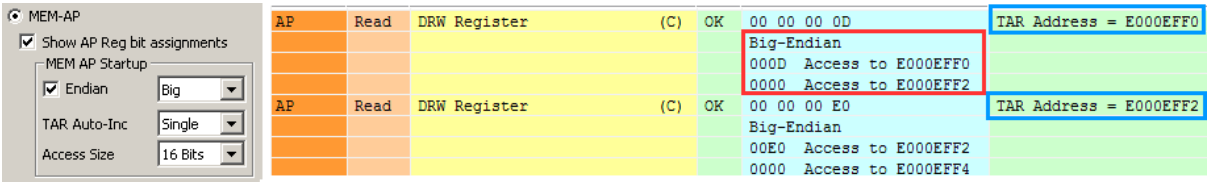
Other: Show Bank X Register X.



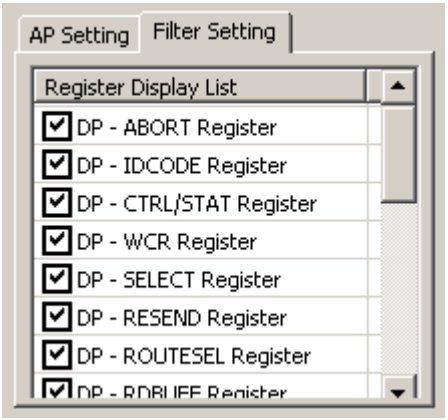
Show AP Reg bit assignments: Display the AP register information if JTAG-AP or MEM-AP checked.



MEM AP Startup: Assign the initial MEM-AP value.

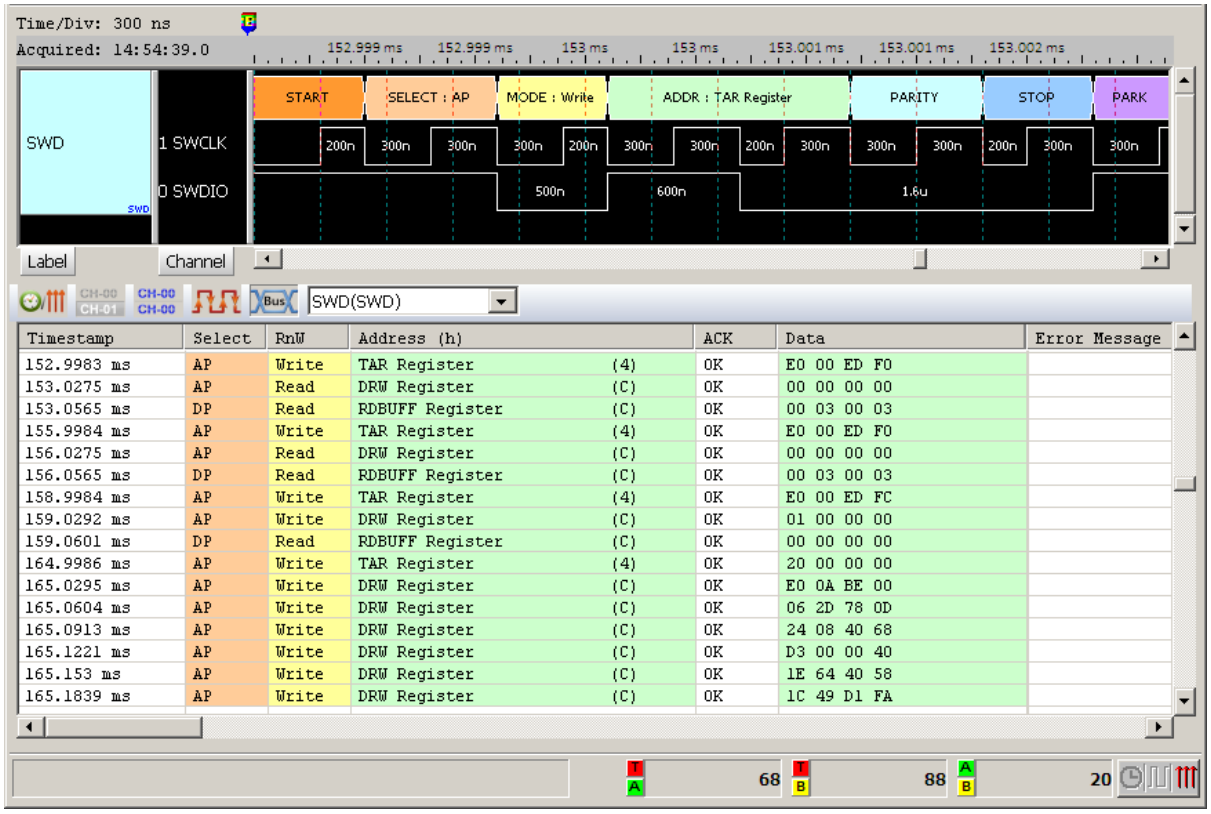


Filter Setting: Filter the unwanted Registers.

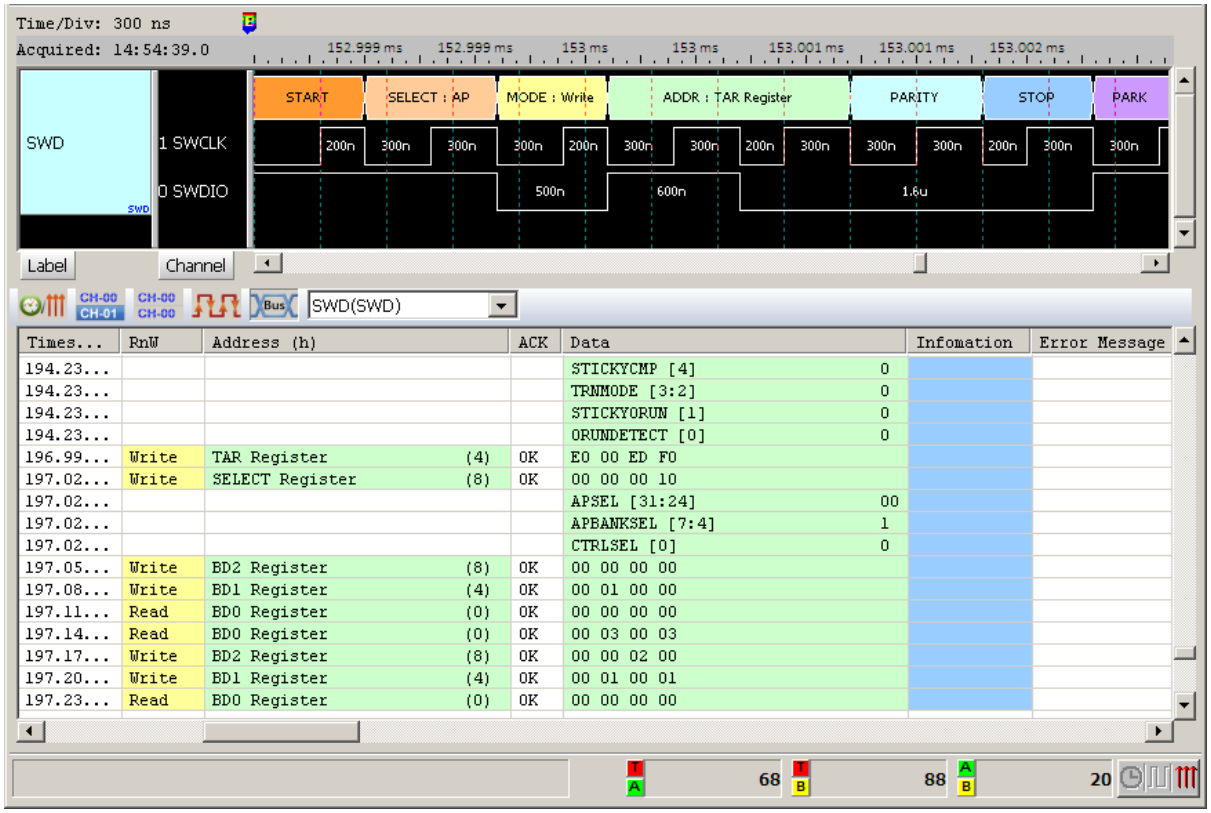


Result

Display the decoded waveform without the MEM-AP bit assignments.



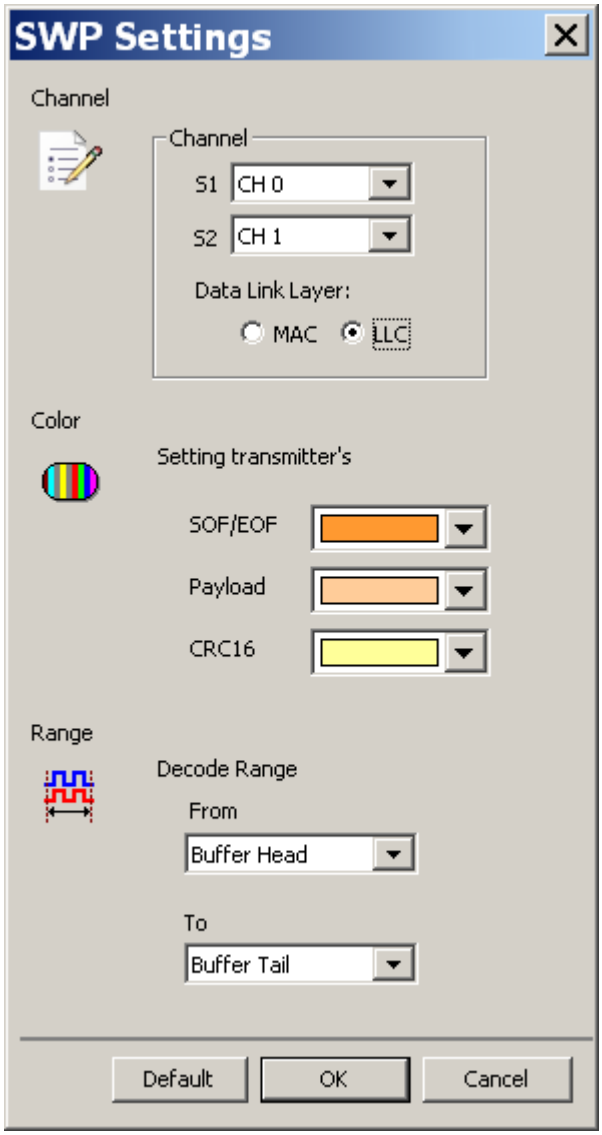
Display the decoded waveform with the MEM-AP bit assignments.



SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

Settings

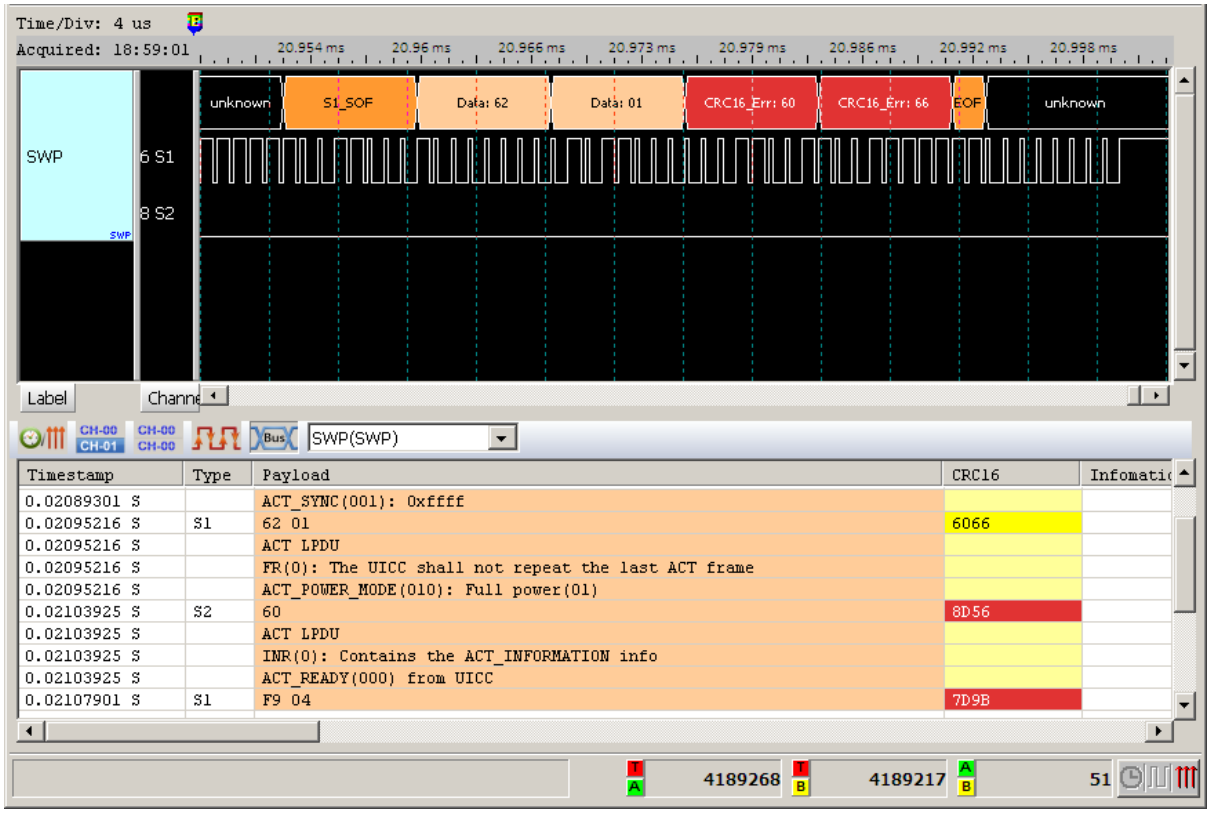


S1: I/O data.

S2: I/O data in current domain and it need convert to voltage domain.

Data Link Layer: Supported MAC and LLC layers

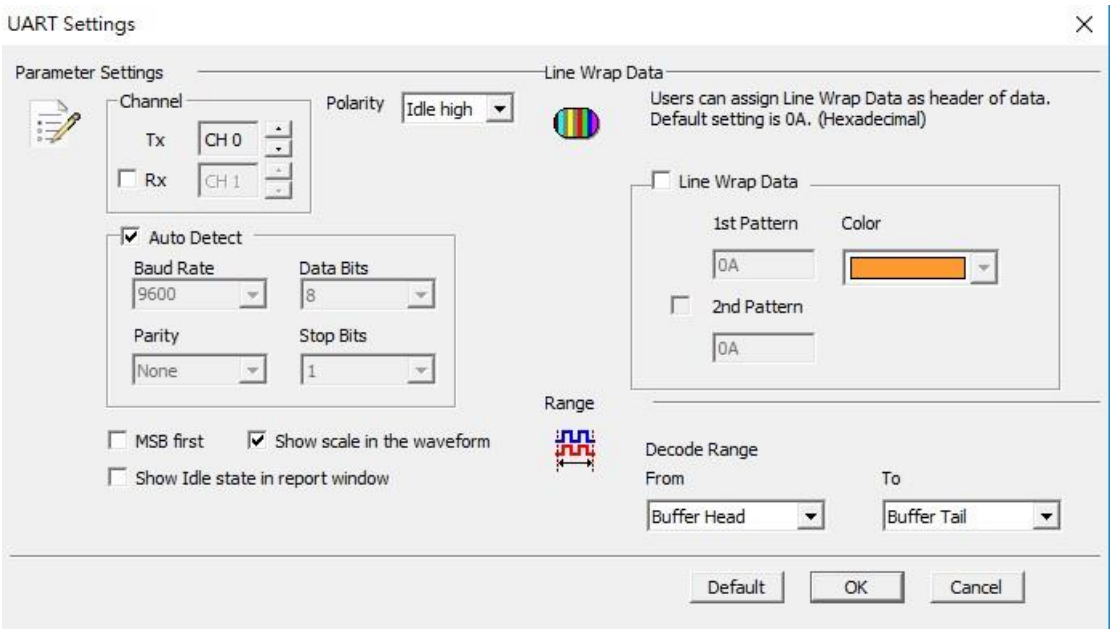
Result



Universal Asynchronous Receiver/Transmitter (UART)

The UART (RS-232 or RS-485) protocol has two message types: Transmitter (TX) and Receiver (RX); you can measure the UART protocol in one signal or two signals. RS-485 need convert to logic signal, because LA can not capture differential signal.

Settings



Data: Show the selected channel (CH0).

Rx: Show Rx data in report window.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Protocol: (Parity - Data Bits - Stop Bits)

Parity: N (None), O (Odd), or E (Even).

Data Bits: 5 to 10 bits.

Stop Bits: 1 to 2 bits.

MSB first: The default is LSB first; click it to change to MSB first.

Report Unknown and Idle: Display the unknown and idle data in the Report Window.

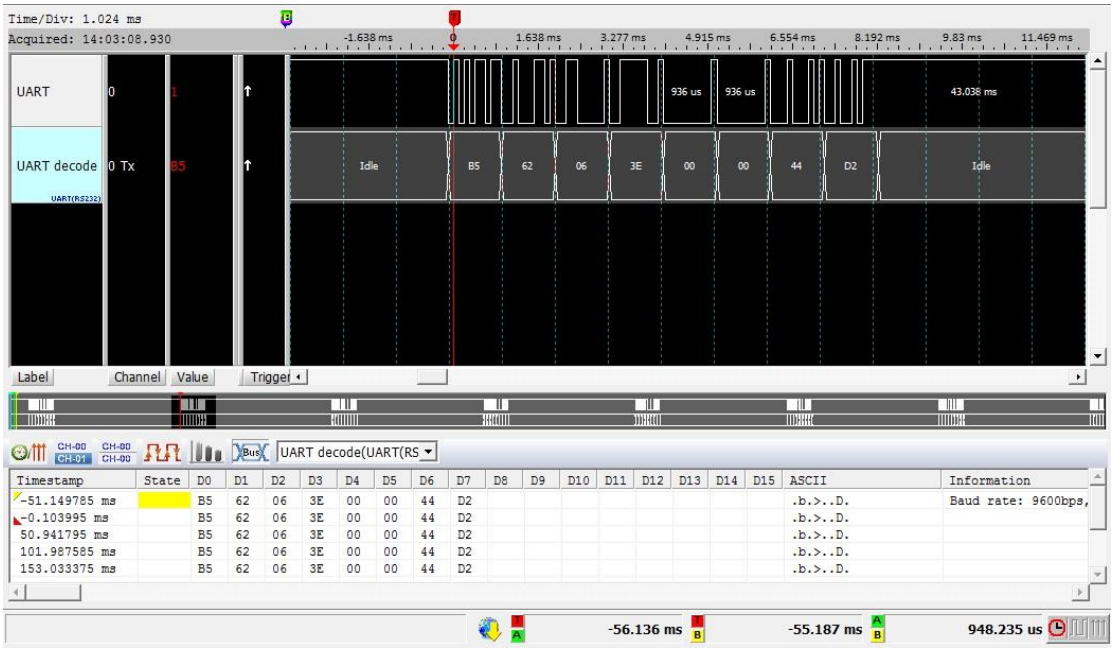
Show scale in the waveform: Display the waveforms with scales.

Line Wrap Data: Use 1-2 value (hex) as header of data.

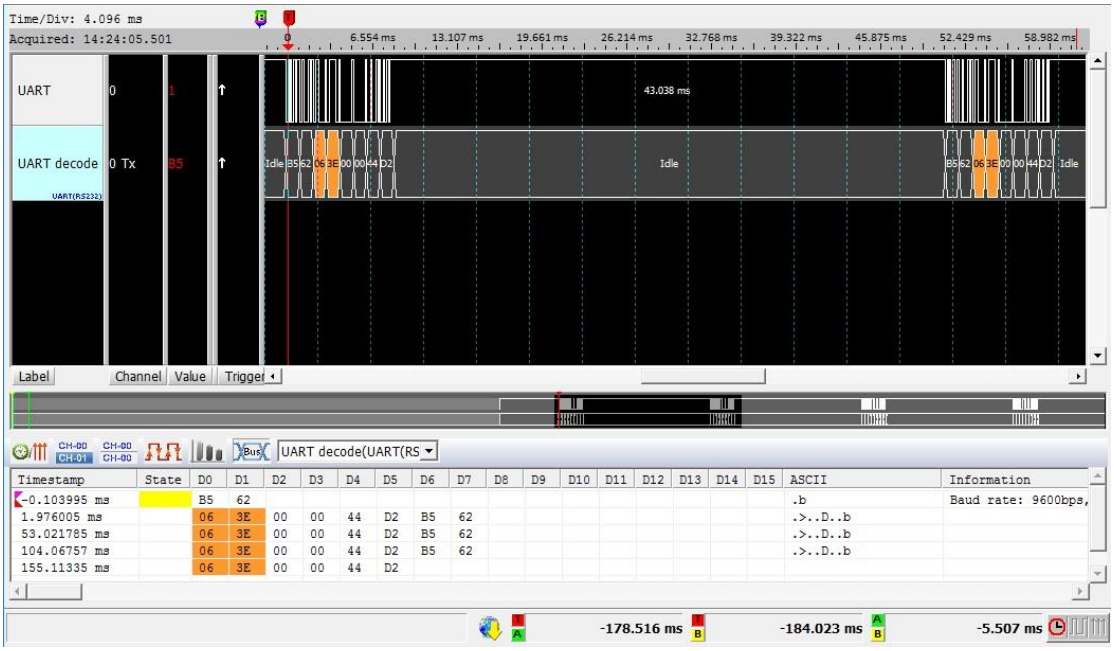
Result

Click **OK** to run UART Decode and see result on the Waveform Window below.

Normal mode



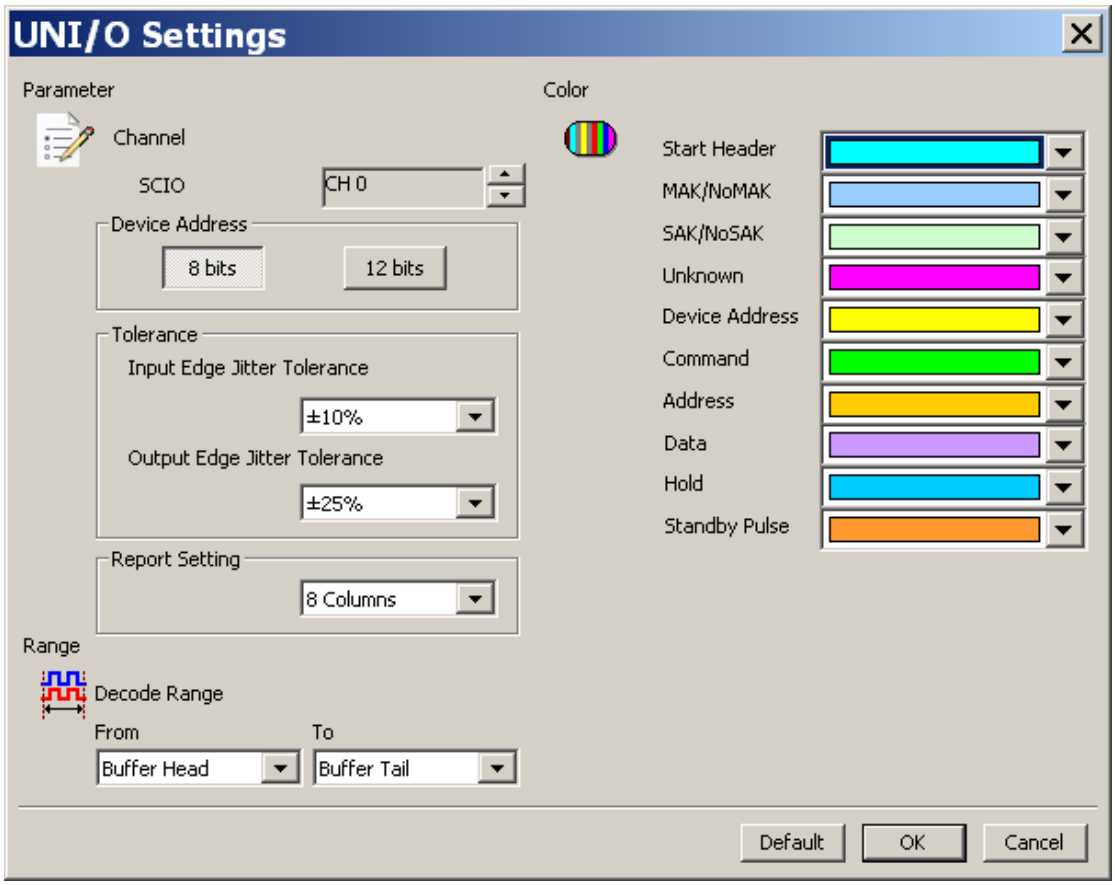
Line Wrap Data mode



UNI/O

The UNI/O interface was developed by Microchip. The data transfer rate is 10Kbps to 100Kbps.

Settings



Channel: Show the selected channels (SCIO CH0).

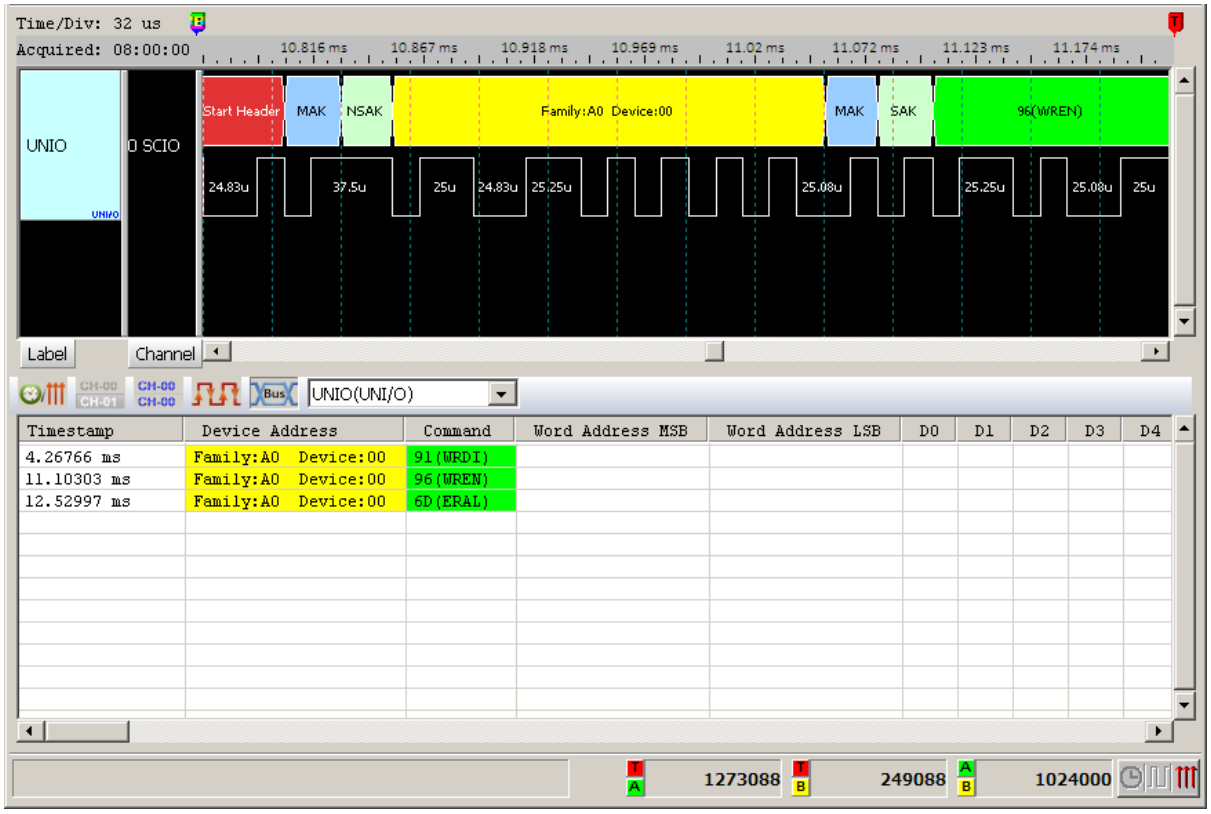
Device Address: Set data bits for the device address.

Tolerance: Set the Input / Output Edge Jitter Tolerance, ±10% / ±25% default.

Report Setting: To show the data by 8 or 16 columns in the Report Window.

Result

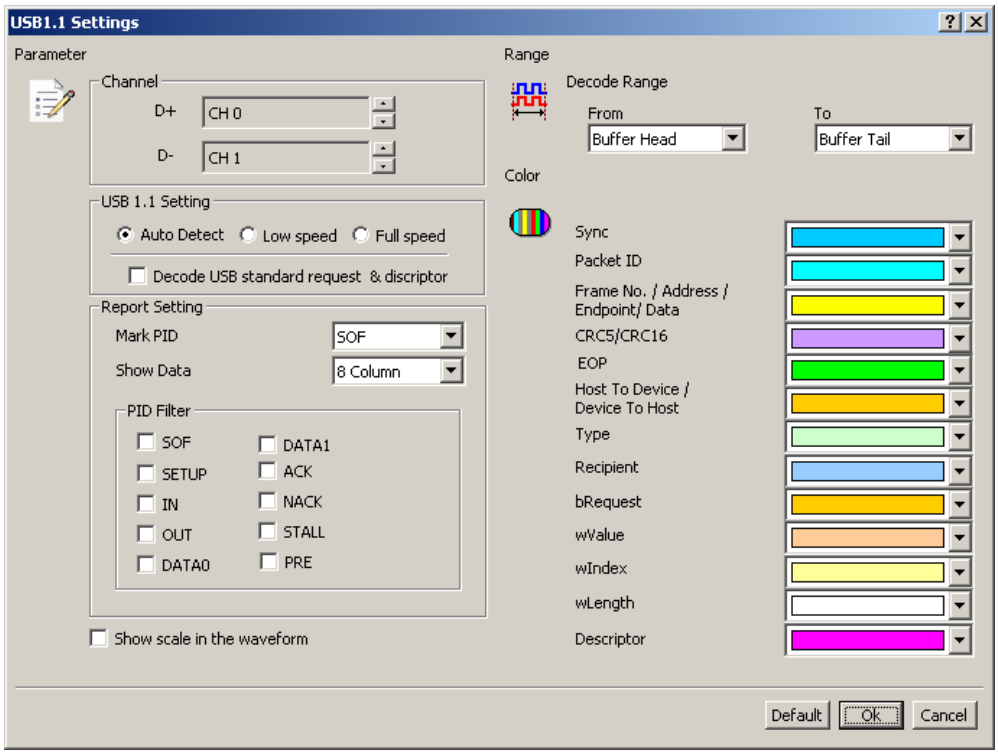
Click **OK** to run the UNI/O decode and see the result on the Waveform Window below.



USB1.1

The USB 1.0 specification was introduced in 1994. USB signals are transmitted on a twisted pair data cable with 90 Ohm ±15% impedance, labeled D+ and D−.

Settings

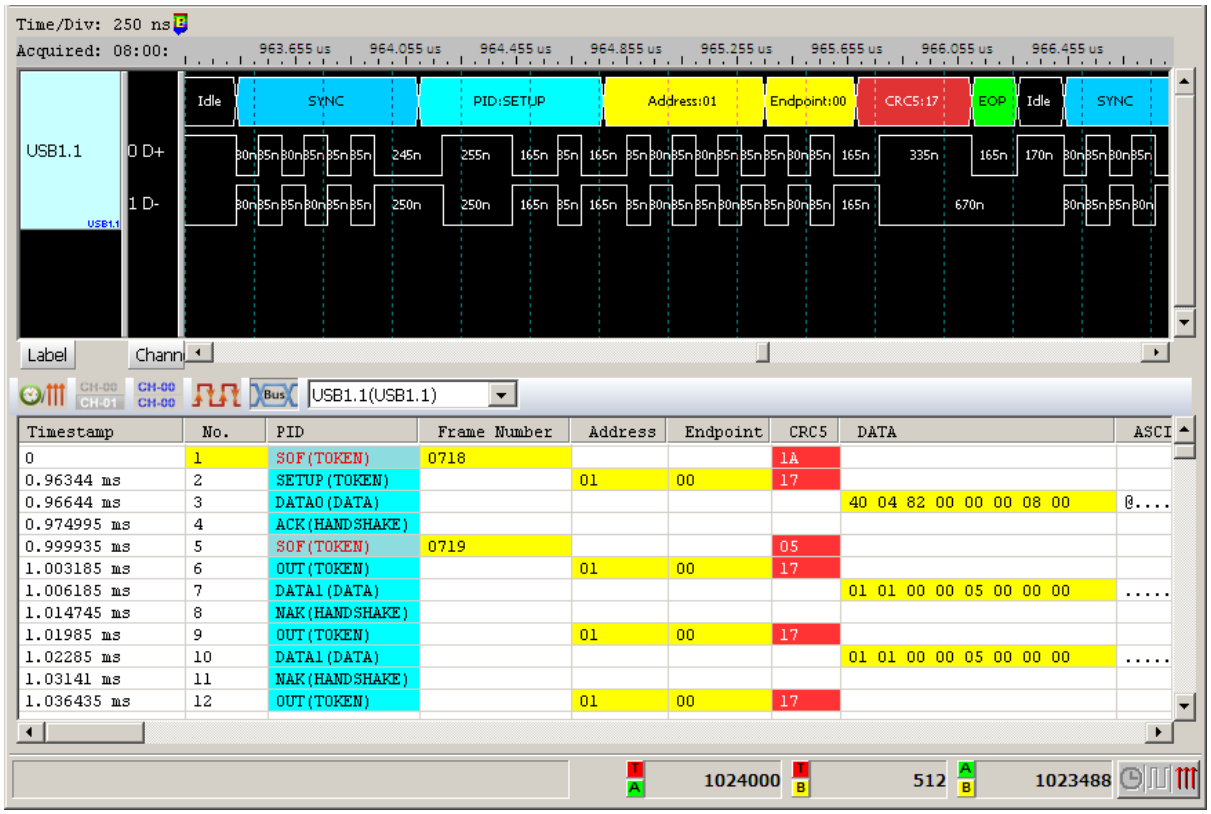


Channel: Show the selected channels (D+ CH0 and D- CH1).

USB1.1 Setting: Select USB state (low speed or full speed) and decode the USB standard request and descriptor.

Result

Click **OK** to run the USB1.1 decode and see the result on the Waveform Window.

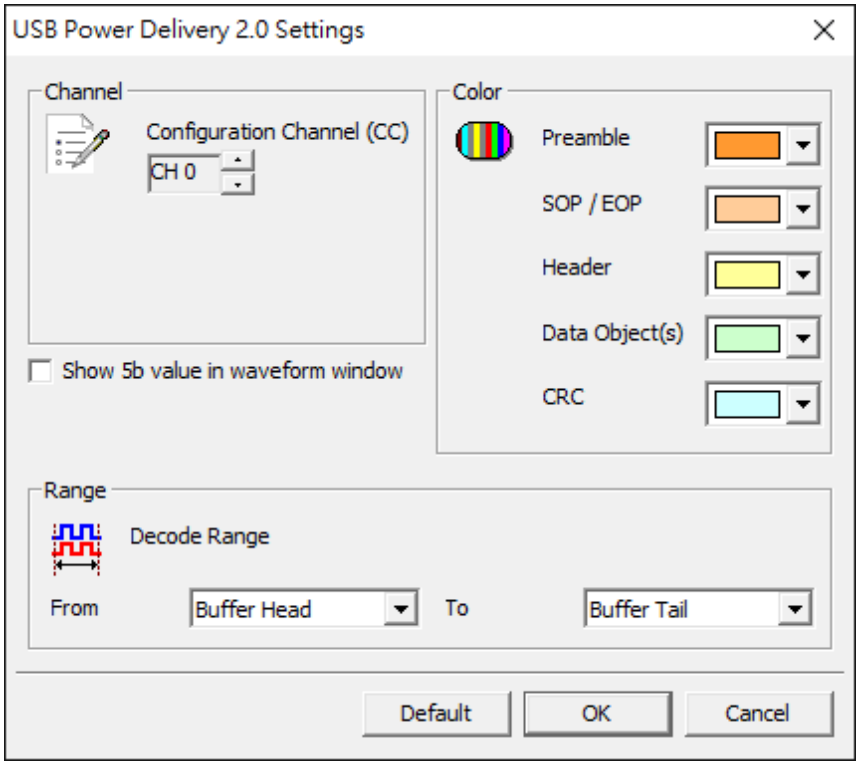


Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC5	DATA	ASCI
0	1	SOF(TOKEN)	0718			1A		
0.96344 ms	2	SETUP(TOKEN)		01	00	17		
0.96644 ms	3	DATA0(DATA)					40 04 82 00 00 00 08 00	@....
0.974995 ms	4	ACK(HANDSHAKE)						
0.999935 ms	5	SOF(TOKEN)	0719			05		
1.003185 ms	6	OUT(TOKEN)		01	00	17		
1.006185 ms	7	DATA1(DATA)					01 01 00 00 05 00 00 00	.....
1.014745 ms	8	NAK(HANDSHAKE)						
1.01985 ms	9	OUT(TOKEN)		01	00	17		
1.02285 ms	10	DATA1(DATA)					01 01 00 00 05 00 00 00	.....
1.03141 ms	11	NAK(HANDSHAKE)						
1.036435 ms	12	OUT(TOKEN)		01	00	17		

USB PD 2.0

USB PD (Power Delivery) 2.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 100W, and the users can charge the device by supporting USB Type-C connector.

Settings

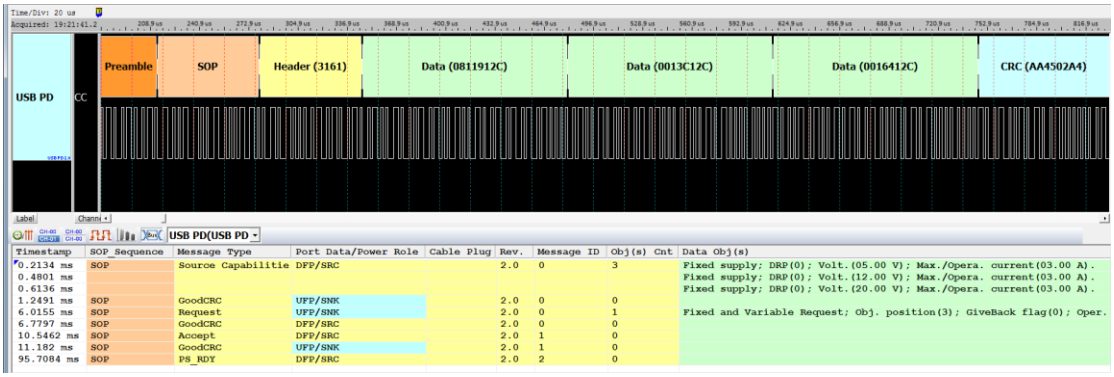


Channel: Set Configuration Channel (CC).

Show 5b value in waveform window: Show 4b or 5b value in the waveform.

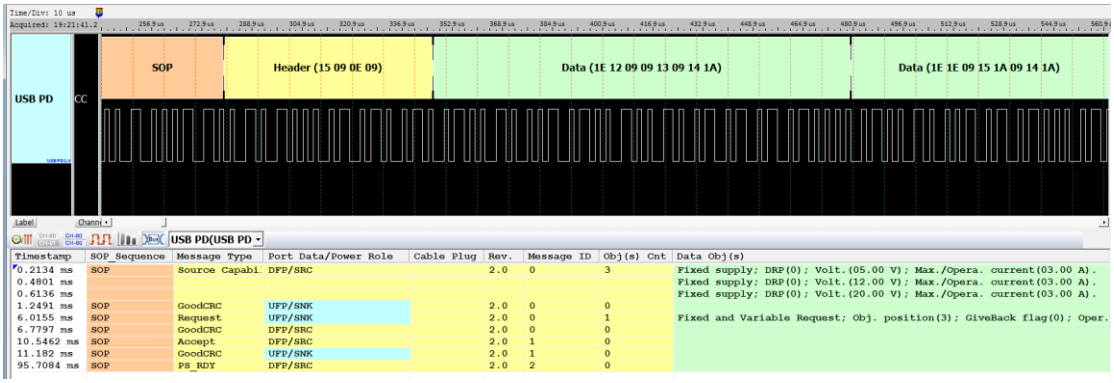
Result

Show 4b value.



Timestamp	SOP_Sequence	Message Type	Port Data/Power Role	Cable Plug	Rev.	Message ID	Obj(s) Cnt	Data Obj(s)
0.2134 ms	SOP	Source Capabilitie	DFP/SRC		2.0	0	3	Fixed supply; DRP(0); Volt.(05.00 V); Max./Opera. current(03.00 A).
0.4801 ms								Fixed supply; DRP(0); Volt.(12.00 V); Max./Opera. current(03.00 A).
0.6136 ms								Fixed supply; DRP(0); Volt.(20.00 V); Max./Opera. current(03.00 A).
1.2491 ms	SOP	GoodCRC	UFP/SNK		2.0	0	0	
6.0155 ms	SOP	Request	UFP/SNK		2.0	0	1	Fixed and Variable Request; Obj. position(3); GiveBack flag(0); Oper.
6.7797 ms	SOP	GoodCRC	DFP/SRC		2.0	0	0	
10.5462 ms	SOP	Accept	DFP/SRC		2.0	1	0	
11.182 ms	SOP	GoodCRC	UFP/SNK		2.0	1	0	
95.7084 ms	SOP	PS_RDY	DFP/SRC		2.0	2	0	

Show 5b value.

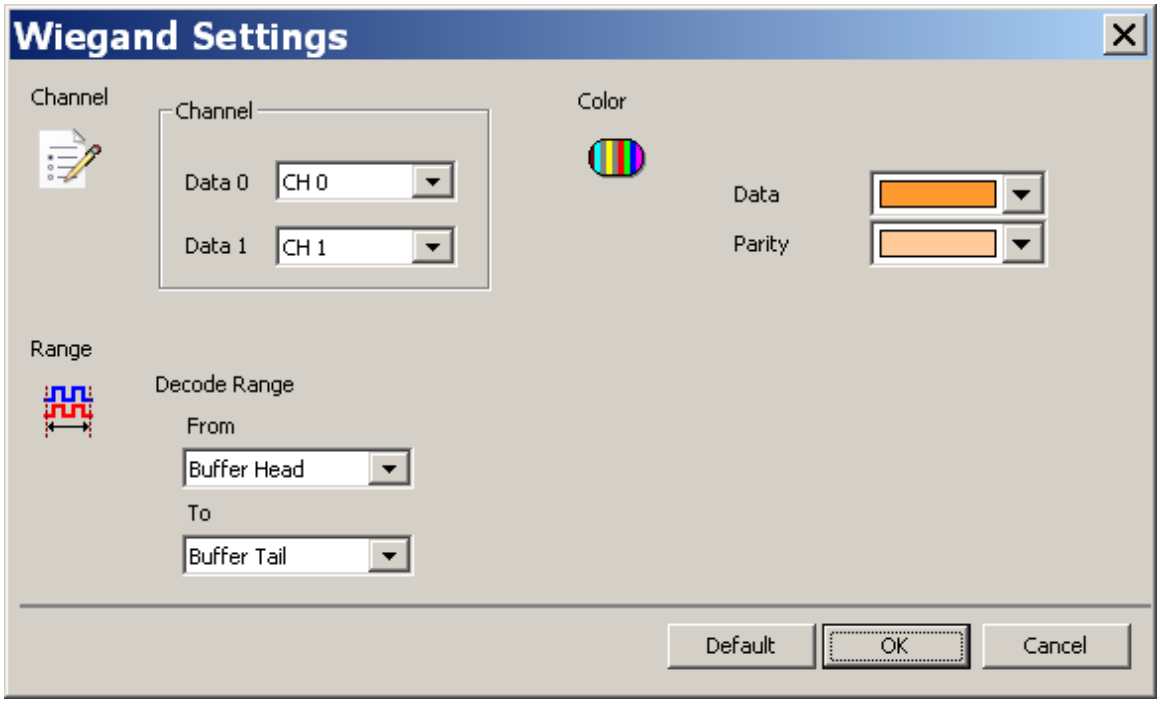


Timestamp	SOP_Sequence	Message Type	Port Data/Power Role	Cable Plug	Rev.	Message ID	Obj(s) Cnt	Data Obj(s)
0.2134 ms	SOP	Source Capabi	DFP/SRC		2.0	0	3	Fixed supply; DRP(0); Volt.(05.00 V); Max./Opera. current(03.00 A).
0.4801 ms								Fixed supply; DRP(0); Volt.(12.00 V); Max./Opera. current(03.00 A).
0.6136 ms								Fixed supply; DRP(0); Volt.(20.00 V); Max./Opera. current(03.00 A).
1.2491 ms	SOP	GoodCRC	UFP/SNK		2.0	0	0	
6.0155 ms	SOP	Request	UFP/SNK		2.0	0	1	Fixed and Variable Request; Obj. position(3); GiveBack flag(0); Oper.
6.7797 ms	SOP	GoodCRC	DFP/SRC		2.0	0	0	
10.5462 ms	SOP	Accept	DFP/SRC		2.0	1	0	
11.182 ms	SOP	GoodCRC	UFP/SNK		2.0	1	0	
95.7084 ms	SOP	PS_RDY	DFP/SRC		2.0	2	0	

Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic entry system..

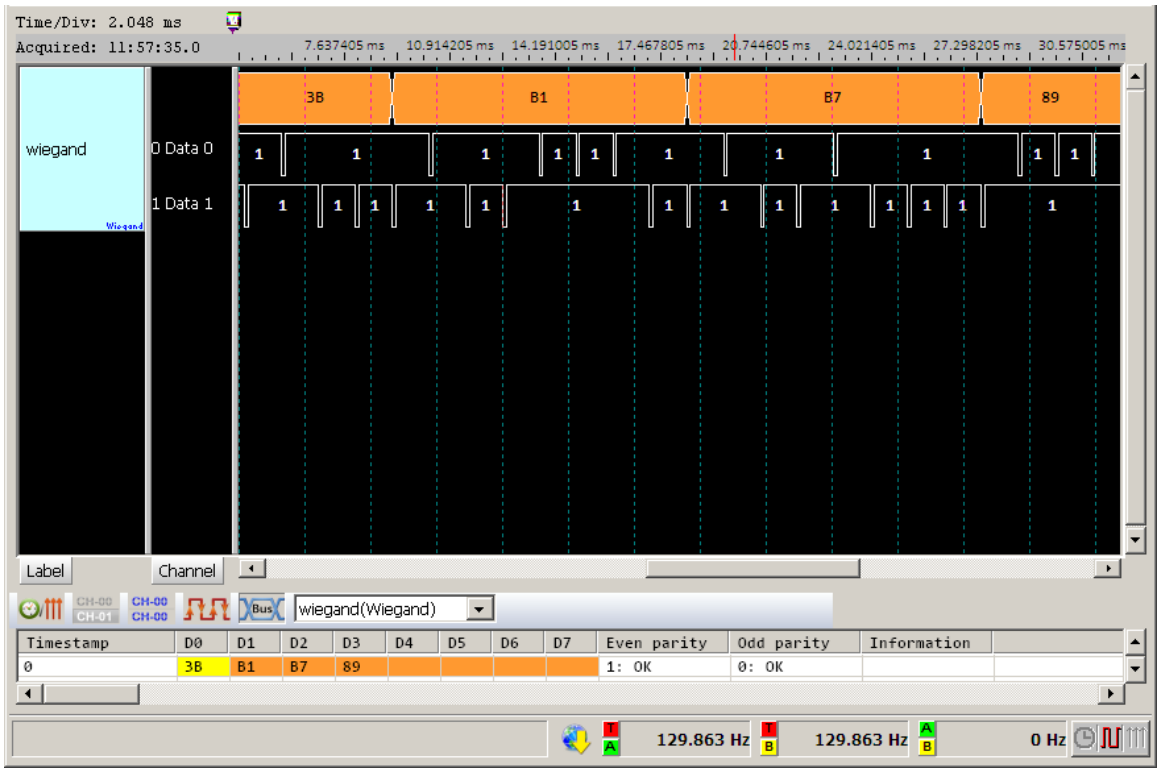
Settings



Channel: Show the selected channels (Data 0 and Data 1).

Result

Click **OK** to run the wiegand decode and see the result on the Waveform Window.



Chapter 2 Bus Trigger

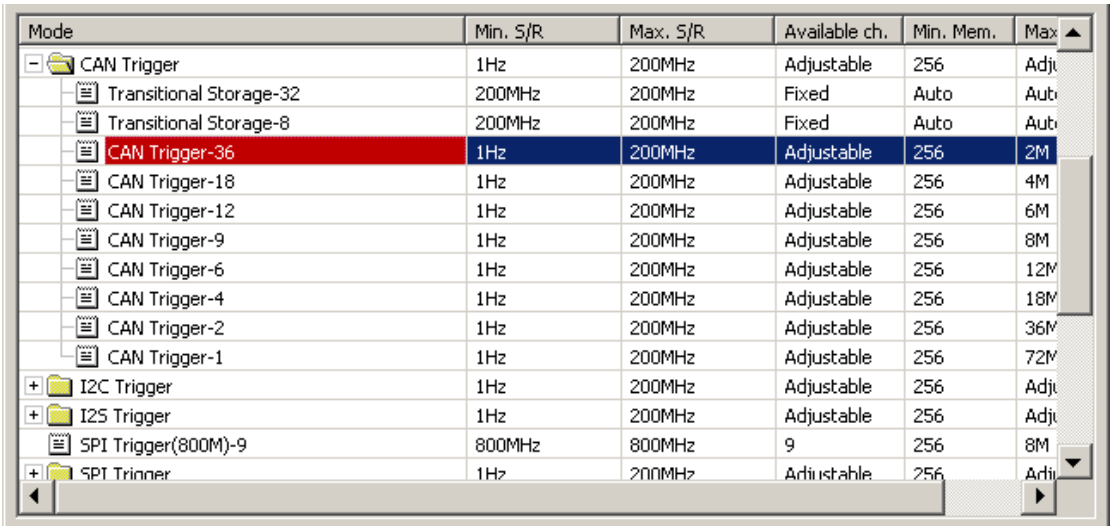
Bus Trigger

The bus trigger are only available for the TravelLogic ULA-4G36 AL Series.

Bus Trigger	TravelLogic B+	TravelLogic B	TravelLogic E	TravelLogic
CAN	◎	◎		◎
eSPI	◎			
I2C	◎	◎		◎
I2S	◎	◎	◎	◎
LIN	◎	◎		
LPC	◎	◎		
MIPI SPMI	◎			
NAND Flash	◎			
SD/eMMC	◎			
Serial Flash	◎			
SMBus/PMBus	◎	◎		
SPI	◎	◎		◎
SVI2	◎	◎		
SVID	◎	◎		◎
UART	◎	◎		◎
USB 1.1	◎	◎		

CAN Trigger

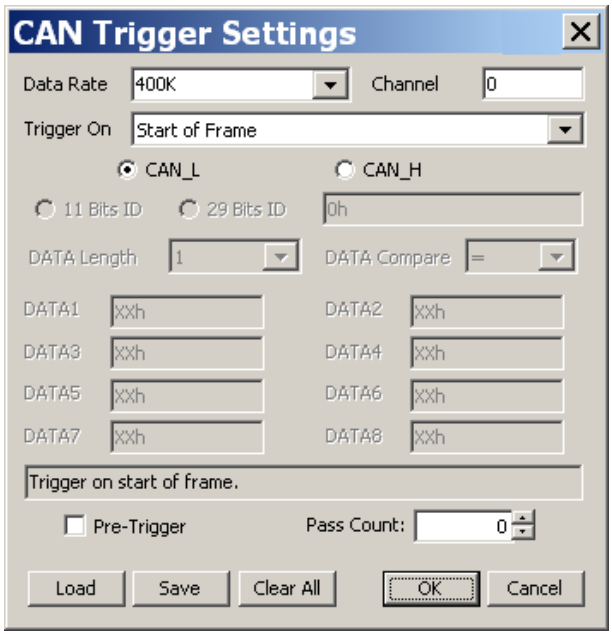
The settings dialog box below.



Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max
CAN Trigger	1Hz	200MHz	Adjustable	256	Adju
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
CAN Trigger-36	1Hz	200MHz	Adjustable	256	2M
CAN Trigger-18	1Hz	200MHz	Adjustable	256	4M
CAN Trigger-12	1Hz	200MHz	Adjustable	256	6M
CAN Trigger-9	1Hz	200MHz	Adjustable	256	8M
CAN Trigger-6	1Hz	200MHz	Adjustable	256	12M
CAN Trigger-4	1Hz	200MHz	Adjustable	256	18M
CAN Trigger-2	1Hz	200MHz	Adjustable	256	36M
CAN Trigger-1	1Hz	200MHz	Adjustable	256	72M
I2C Trigger	1Hz	200MHz	Adjustable	256	Adju
I2S Trigger	1Hz	200MHz	Adjustable	256	Adju
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
SPI Trigger	1Hz	200MHz	Adjustable	256	Adju

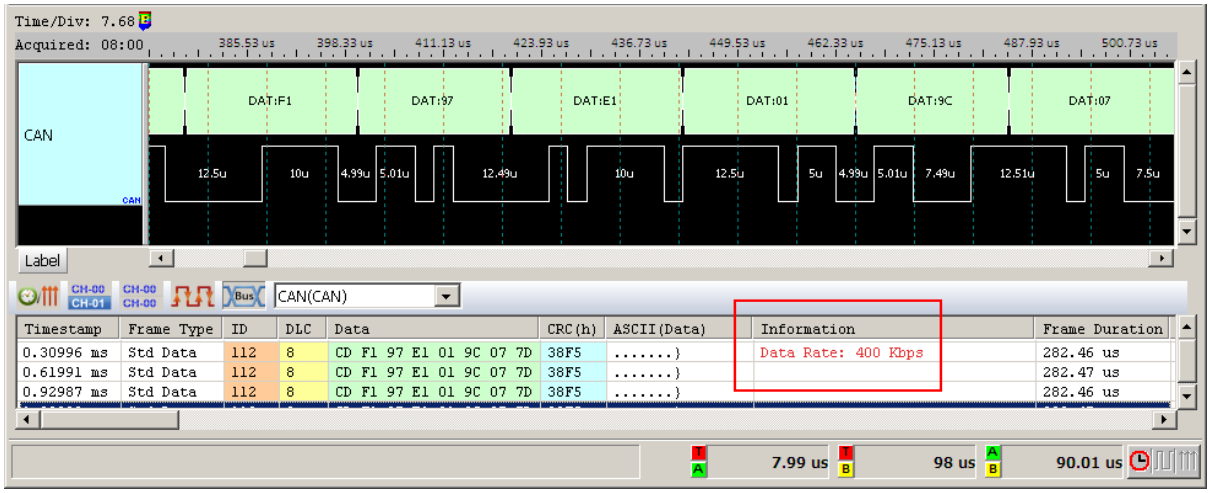
Trigger Settings

Select CAN Trigger-36 where "-36" means 36 channels and the sample rate is always 10 times of data rate, then click OK. Click the Trigger Settings button ( ) on Toolbar (or Device menu) to show the CAN Trigger Settings dialog box below.



Data Rate: Select a default data rate or run the CAN decode to measure the actual

data rate to enter (highly recommended). When the selected data rate is about 5% deviation from the actual data rate will lead to CAN trigger failure.



Channel: Select channels.

Trigger On: Select the data field to trigger on:

Start of Frame

ID Match Data Frame

Remote Frame

Error Frame

Overload Frame

Stuffing Error

CRC Error

Data Value

Missing ACK

End of Frame

ID Match & Data Value

CAN_H/CAN_L: Select CAN_H or CAN_L as the trigger channel.

11 Bits ID/29 Bits ID: Data bits of the Identification field.

DATA Length: The number of transmitted data, by Byte unit.

DATA Compare: To compare the data.

DATA1 ~ DATA8: Data like binary codes (e.g. 01000001b), decimal codes (e.g. 65), hexadecimal codes (e.g. 41h). If trigger on Date Value and need to pass some data, please enter XX. For example: To trigger the data 38h in the third byte of data frame, enter:

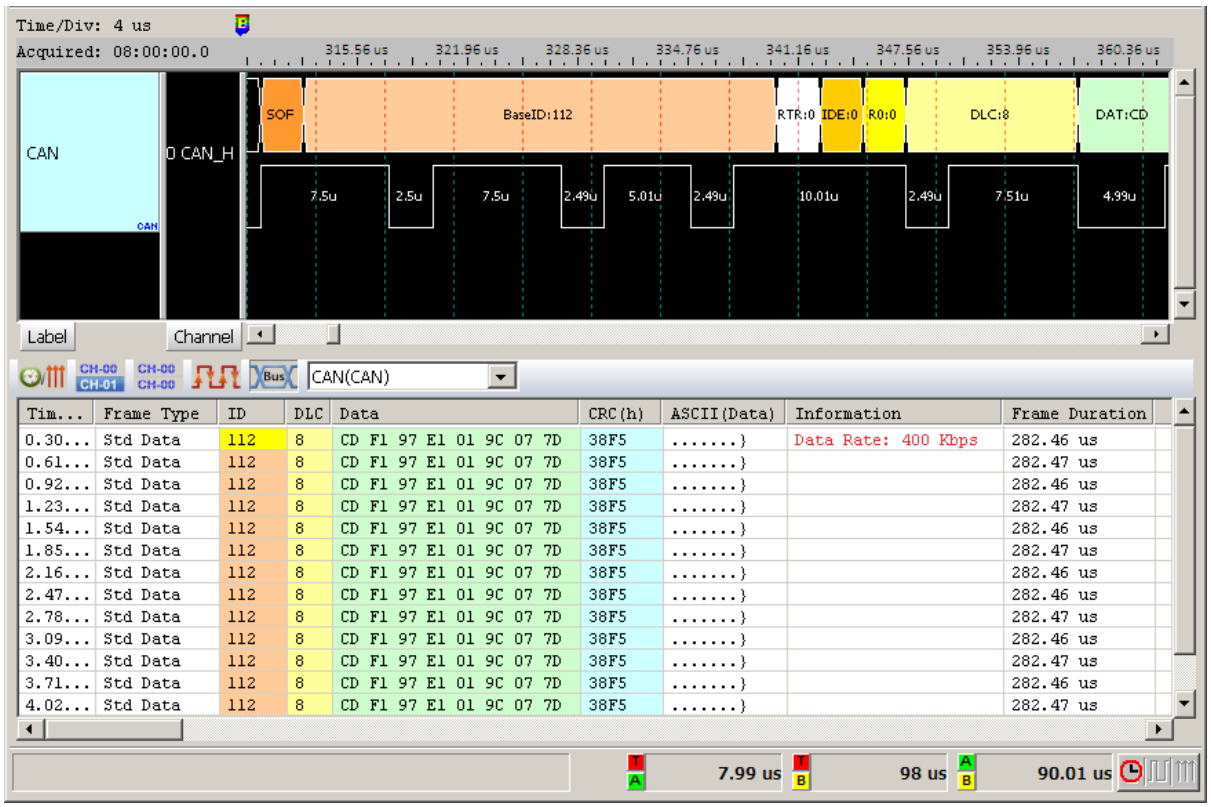
DATA Length = 3

DATA1 = XX

DATA2 = XX

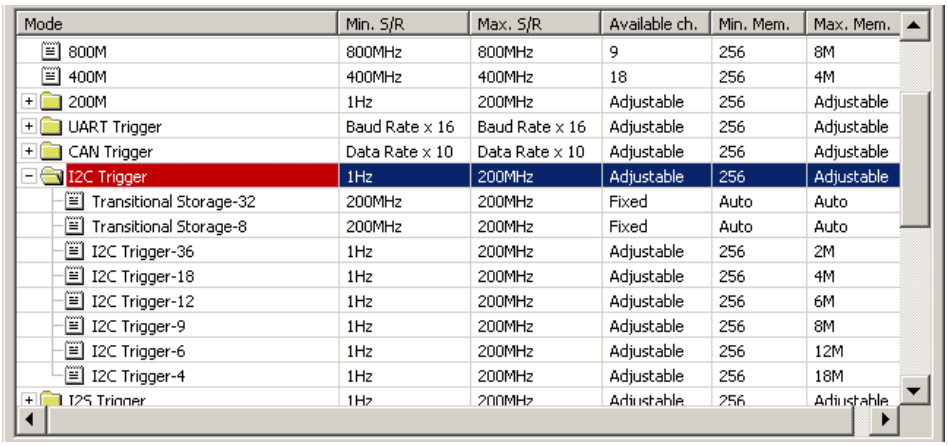
DATA3 = 38h

Result



I²C Trigger

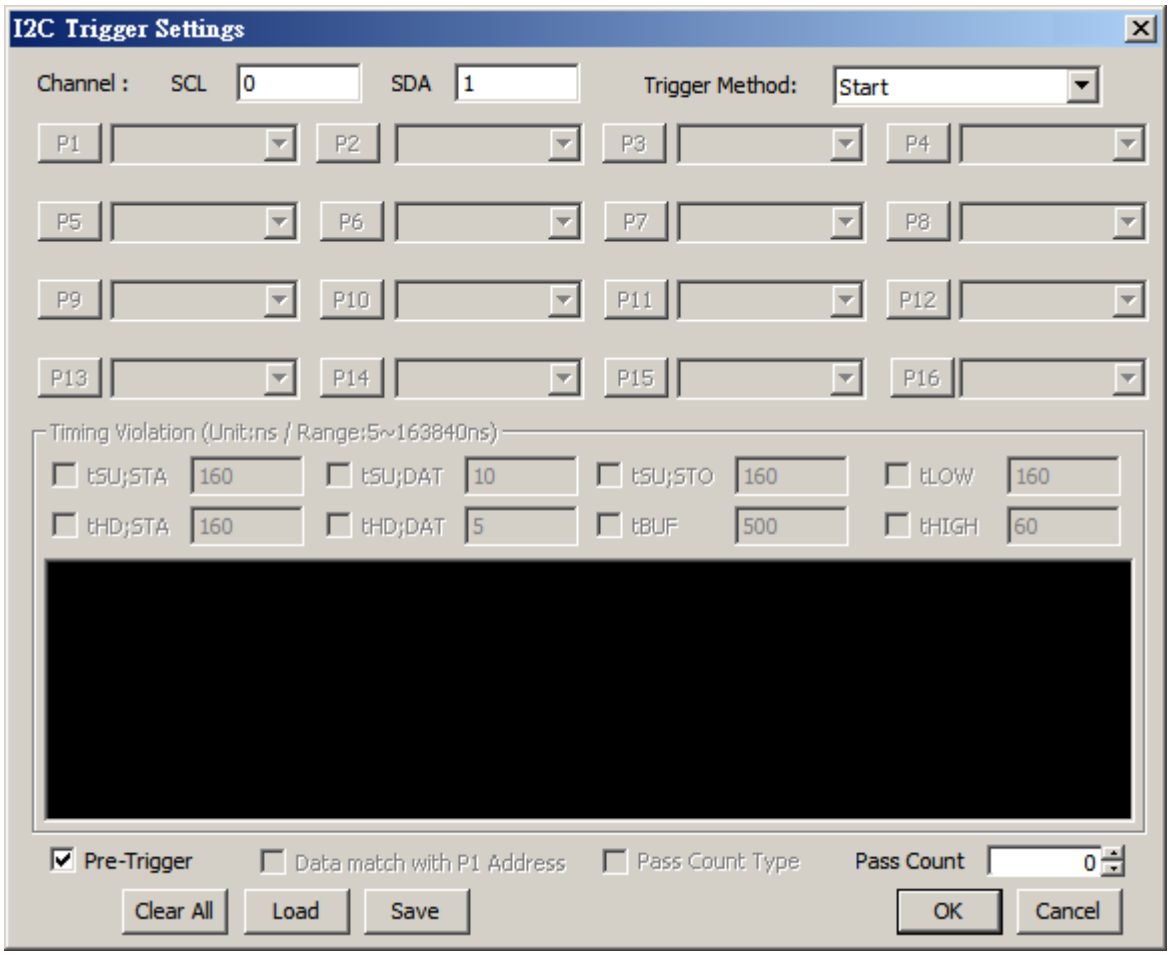
The settings dialog box below.



Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
800M	800MHz	800MHz	9	256	8M
400M	400MHz	400MHz	18	256	4M
200M	1Hz	200MHz	Adjustable	256	Adjustable
UART Trigger	Baud Rate x 16	Baud Rate x 16	Adjustable	256	Adjustable
CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
I2C Trigger-36	1Hz	200MHz	Adjustable	256	2M
I2C Trigger-18	1Hz	200MHz	Adjustable	256	4M
I2C Trigger-12	1Hz	200MHz	Adjustable	256	6M
I2C Trigger-9	1Hz	200MHz	Adjustable	256	8M
I2C Trigger-6	1Hz	200MHz	Adjustable	256	12M
I2C Trigger-4	1Hz	200MHz	Adjustable	256	18M
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Settings

Select I²C Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button () on Toolbar (or Device menu) to show the I²C Trigger Settings dialog box below.



Channel: Select two channels for the serial clock (SCK) and the serial data (SDA).

Trigger Method: Offer nine models for user to choose.

Start

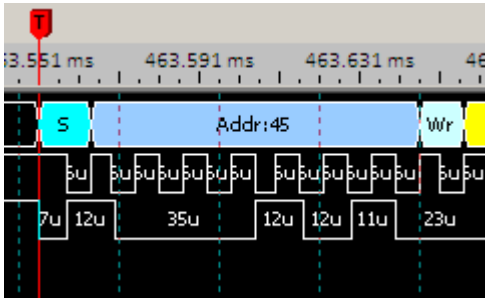
Re-Start

Start or Re-Start

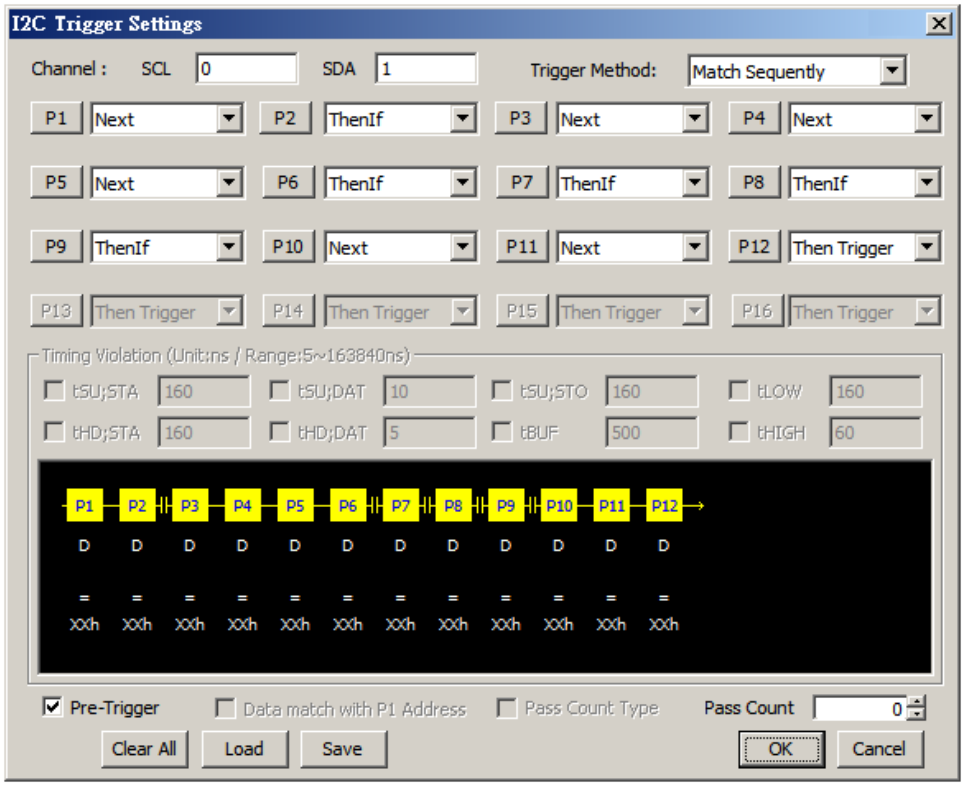
Stop

Missing Ack (Not Acknowledge (NACK))

For the first five ways of Trigger Method, Cursor T will stay at the beginning of the condition as below if the trigger succeeds.

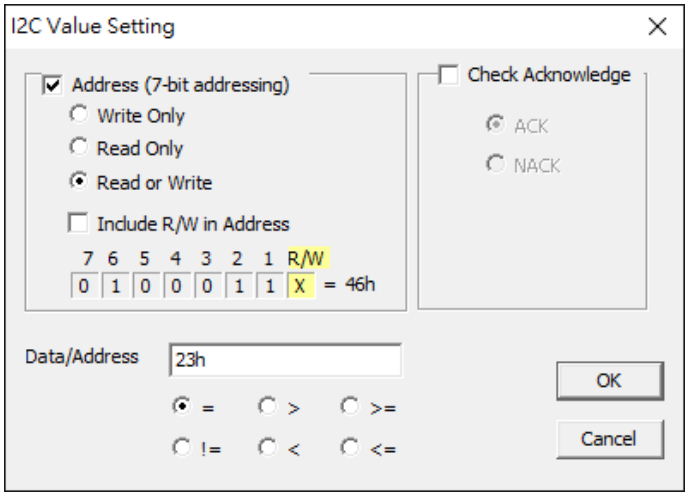


Match Sequentially: Similar to the Sequence Trigger, the I^{2}C Trigger has up to 16 levels of sequential conditions below.

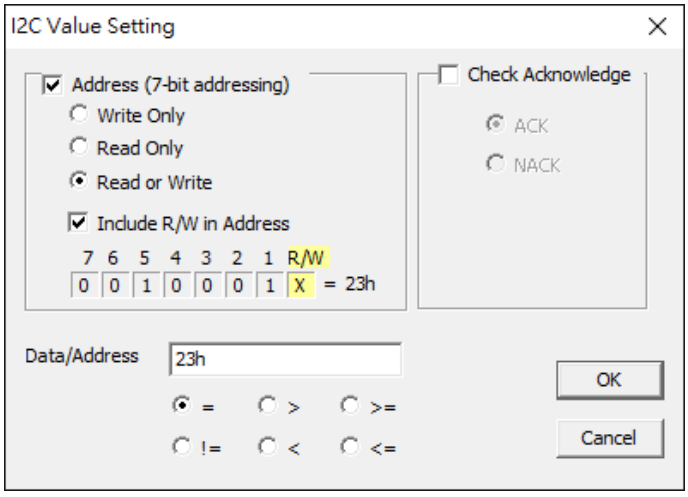


Click any condition (P1 ~ P16) and the I^{2}C Value Setting dialog box below will show.

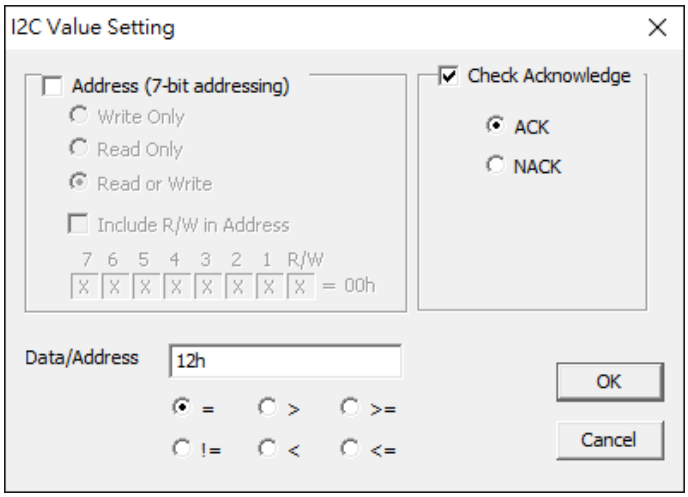
Address:



Write Only, Read Only or Read or Write. When Address is checked, it is the address will be analyzed. Address starts from bit 1 without including R/W in address.



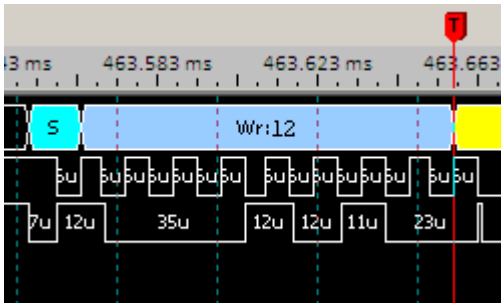
Address starts from bit R/W including R/W in address.



If Address is not checked, the data (Data 12h) will be analyzed.

Check Acknowledge: ACK (Acknowledge), NACK (Not Acknowledge). If the Check Acknowledge is not checked, it can be either ACK or NACK.

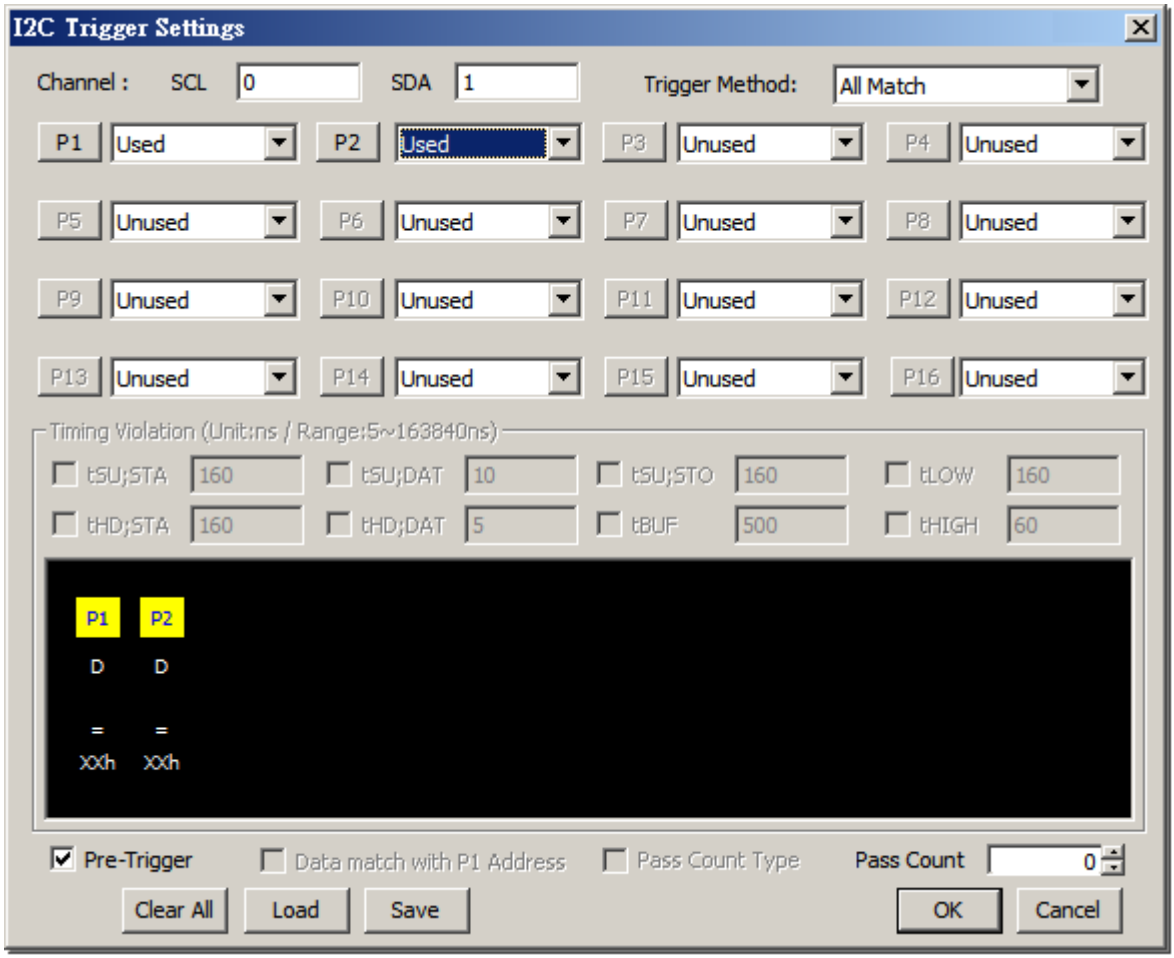
Data/Address:



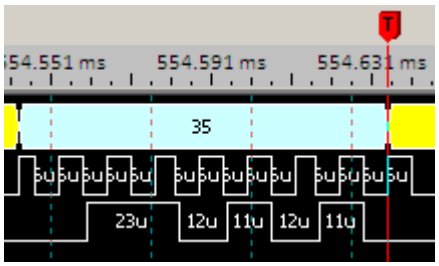
Data or Address can be in binary or hexadecimal code like 00010010b or 12h. Also, you can input X (Don't care) as the value; if the data is 10h, 20h, 30h, you can set X0h or 00XX0000b.

Cursor T will stay at the end of the condition as below if the trigger succeeds.

All Match: All input conditions must be satisfied to trigger.

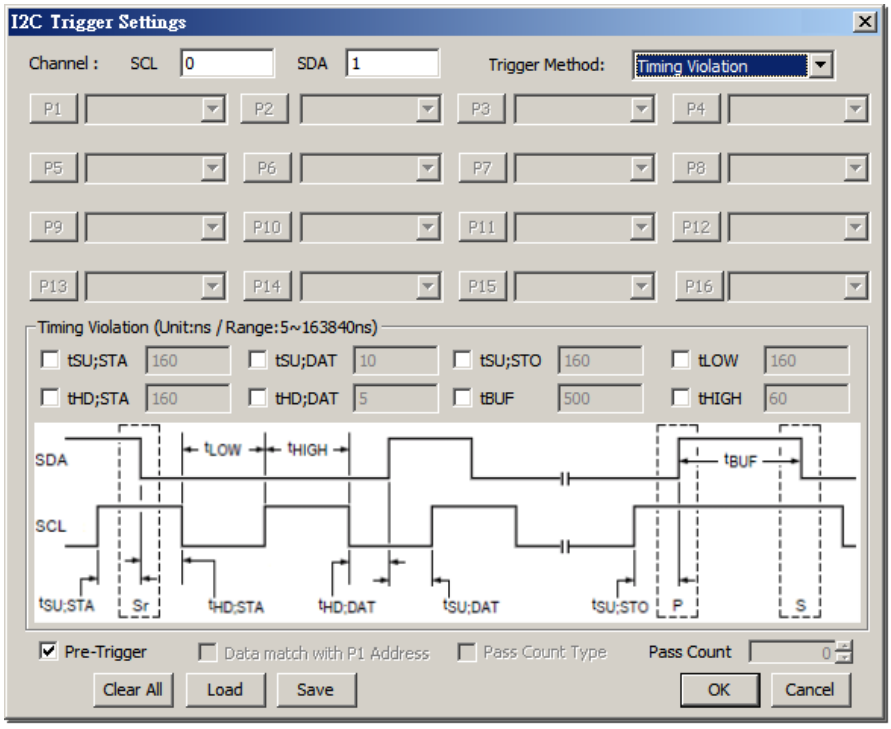


If P1 > 30h and P2 < 40, Cursor T will stay at the end of the condition as below if the trigger succeeds.

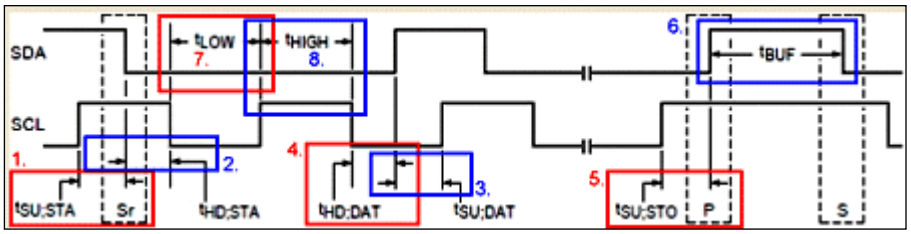


Any Match: Any of input conditions is satisfied to trigger.

Timing Violation: There are eight timing values provided as the trigger condition. If the timing of the signal is less than the input value, then the instrument will trigger. For this function, the 200MHz timing analysis is strongly recommended for better resolution.



About each:



Red 1: tSU;STA: The setup time of Re-Start, also the time when the clock (SCL) is from high to low.

Blue 2: tHD;STA: The hold time of Re-Start, also the time when the clock (SCL) is from high to low.

Blue 3: tSU;DAT: The setup time of Data, also the time when the clock (SCL) is from rising to falling.

Red 4: tHD;DAT: The hold time of Data, also the time when the clock (SCL) is from falling to rising.

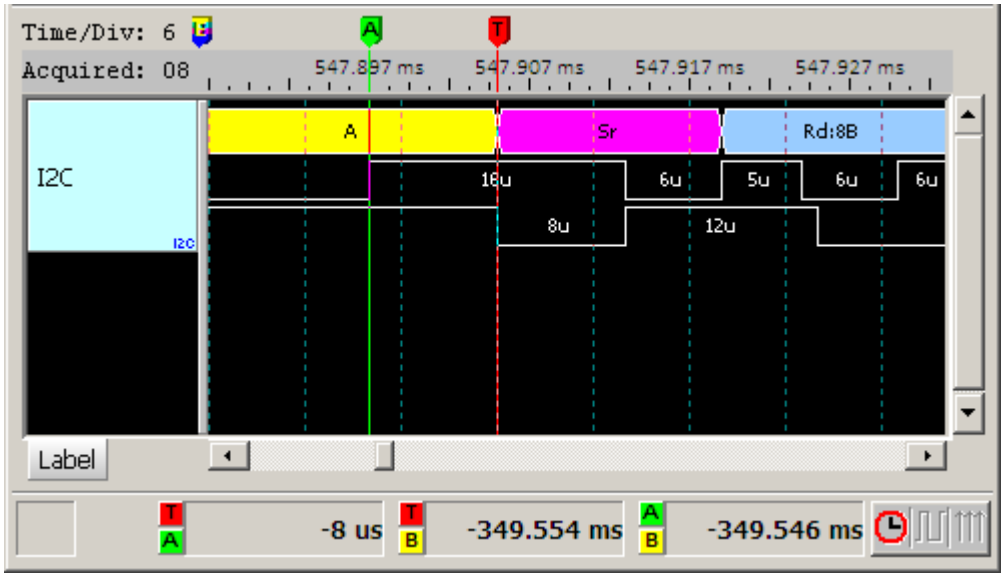
Red 5: tSU; STO: The setup time of Stop, also the time when the clock (SCL) is from high to low.

Blue 6: tBUF: Bus Free Time, that is between Start and Stop.

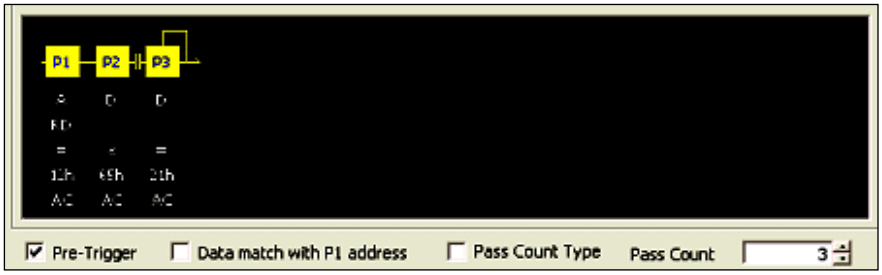
Red 7: tLOW: The time the clock (SCL) is low.

Blue 8: tHIGH: The time the clock (SCL) is high.

The following figure is an example to trigger the setup time (8005ns) of Re-Start (tSU; STA), where the time between cursor T and cursor A is 8us (8000ns < 8005ns).



Pass Count: Pass Count will pass N times that triggers occurred in the non-sequential trigger condition. In the following example, the trigger will pass three triggers in P3 (non-sequential trigger condition) and trigger at the fourth time.

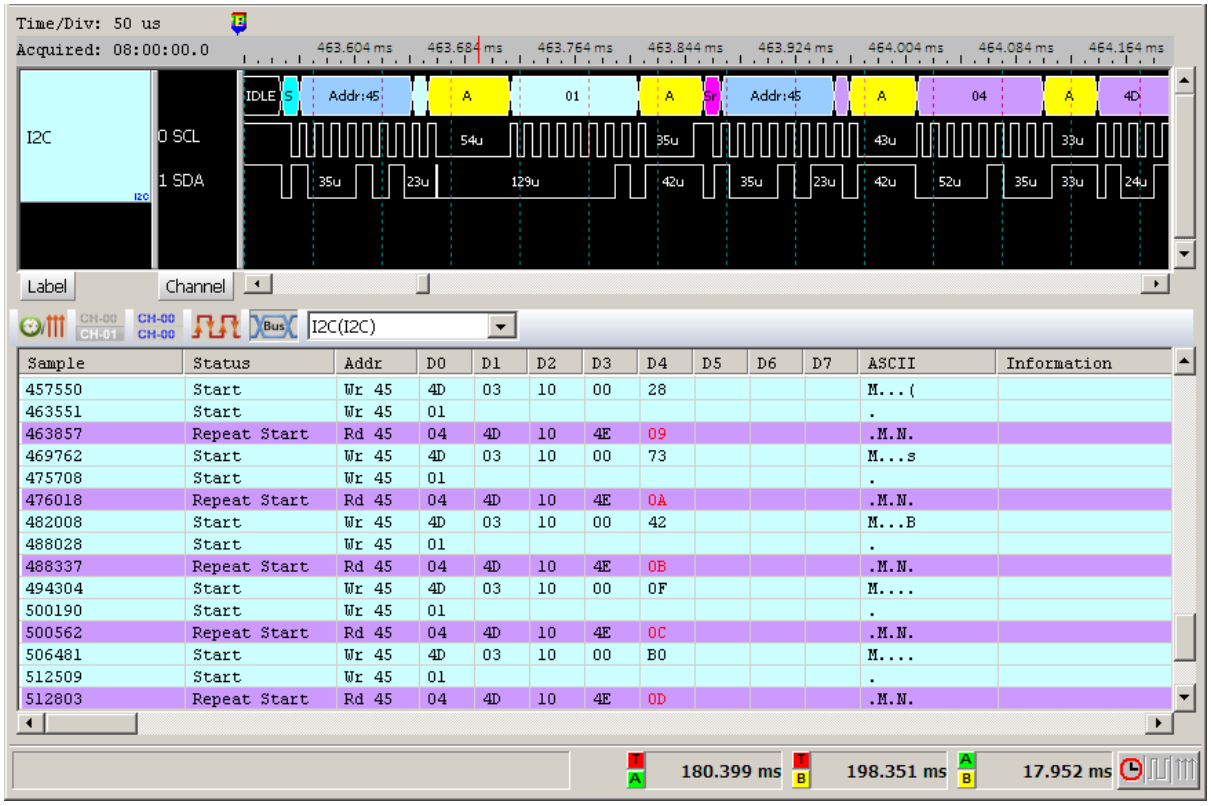


Pass Count Type: If Pass Count Type is checked, then the loop will start run from the first trigger condition (P1).

Data match with P1 address: P1 must be set as address and followed by data; this function is only available in Match Sequentially. And the first level (P1) parameter must be set the address (not data), the function will be open.

For more information of I^2C trigger, please refer to I^2C Application Note.

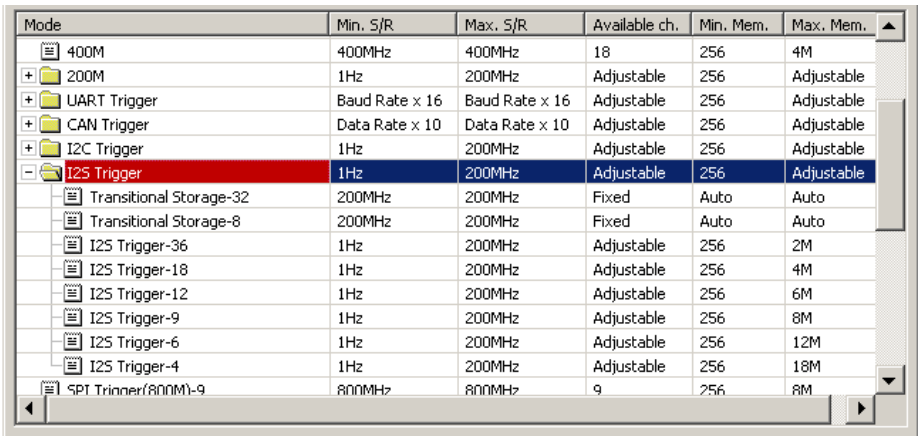
Result



Sample	Status	Addr	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Information
457550	Start	Wr 45	4D	03	10	00	28				M...(	
463551	Start	Wr 45	01								.	
463857	Repeat Start	Rd 45	04	4D	10	4E	09				.M.N.	
469762	Start	Wr 45	4D	03	10	00	73				M...s	
475708	Start	Wr 45	01								.	
476018	Repeat Start	Rd 45	04	4D	10	4E	0A				.M.N.	
482008	Start	Wr 45	4D	03	10	00	42				M...B	
488028	Start	Wr 45	01								.	
488337	Repeat Start	Rd 45	04	4D	10	4E	0B				.M.N.	
494304	Start	Wr 45	4D	03	10	00	0F				M....	
500190	Start	Wr 45	01								.	
500562	Repeat Start	Rd 45	04	4D	10	4E	0C				.M.N.	
506481	Start	Wr 45	4D	03	10	00	B0				M....	
512509	Start	Wr 45	01								.	
512803	Repeat Start	Rd 45	04	4D	10	4E	0D				.M.N.	

I²S Trigger

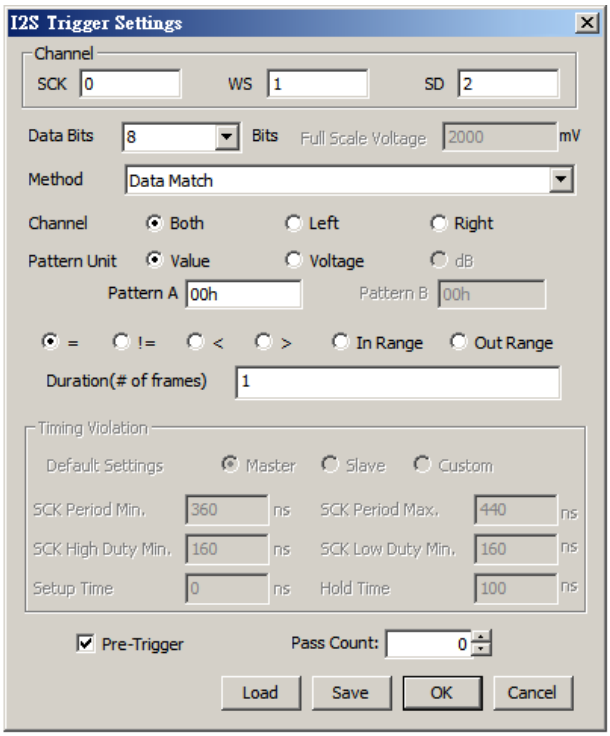
The settings dialog box below.



Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
400M	400MHz	400MHz	18	256	4M
200M	1Hz	200MHz	Adjustable	256	Adjustable
UART Trigger	Baud Rate x 16	Baud Rate x 16	Adjustable	256	Adjustable
CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
I2S Trigger-36	1Hz	200MHz	Adjustable	256	2M
I2S Trigger-18	1Hz	200MHz	Adjustable	256	4M
I2S Trigger-12	1Hz	200MHz	Adjustable	256	6M
I2S Trigger-9	1Hz	200MHz	Adjustable	256	8M
I2S Trigger-6	1Hz	200MHz	Adjustable	256	12M
I2S Trigger-4	1Hz	200MHz	Adjustable	256	18M
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M

Trigger Setting

Select I²S Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button () on Toolbar (or Device menu) to show the I²S Trigger Settings dialog box below.



Channel: There are three channels: Serial clock (SCK), word select (WS) and serial data (SDA).

Data Bits: 1-32 bits, normally it is 8, 12, 16, 24 or 32.

Channel: Both, Left or Right.

Pattern Unit: Value, Voltage or dB as the trigger codition. If it is Value, only hexadecimal (xxxh) or decimal numbers are allowed.

Trigger method: = (is equal), !=(isn't equal), < (less than), >(more than), In Range (between Pattern A and B), or Out Range (out of Pattern A and B)

Duration (# of frames): Continuous frames and trigger when the condition is matched.

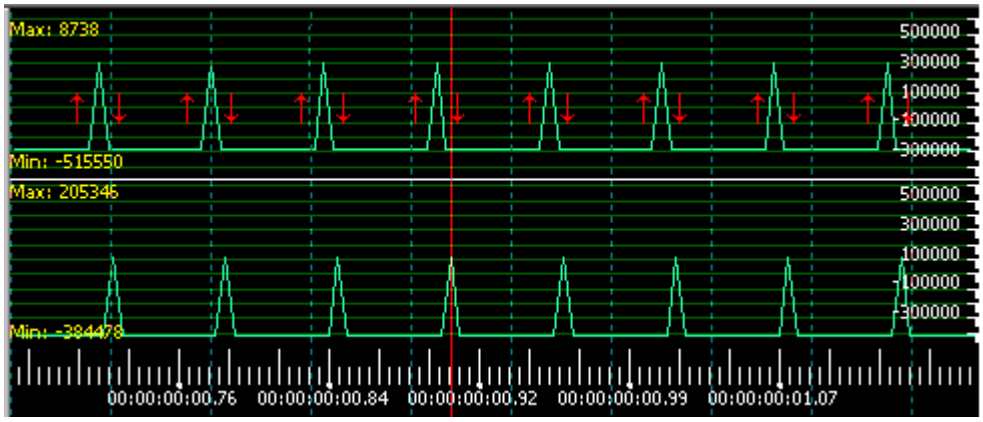
Method:

Data Match: Trigger when the conditions matched.

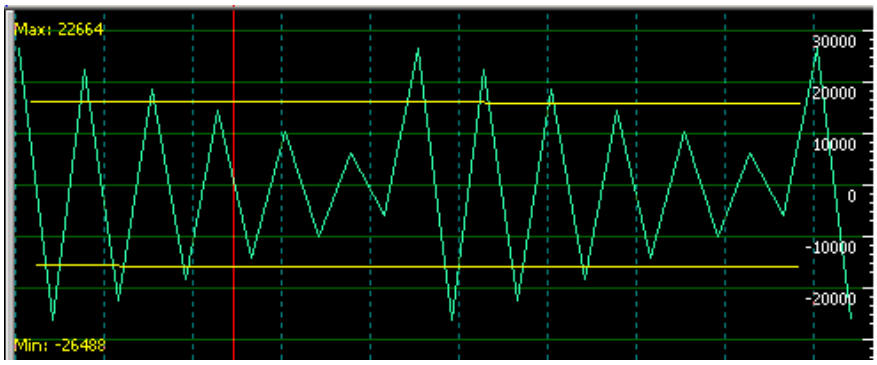
Rising Edged: Trigger when it is a rising edge between two patterns.

Falling Edged: Trigger when it is a falling edge between two patterns.

Glitch: Trigger when there is a glitch.



Mute: When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X < +P.



Clip: When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of –P < X ∪ +P > X.

Timing Violation: There are two default (Master or Slave) and one custom types of timing violation triggers as below.

Master: select the default Master values as the trigger condition.

Slave: select the default Slave values as the trigger condition.

Custom: set trigger parameters manaully.

SCK Period Min.: Trigger when the value is less than the minimum SCK period.

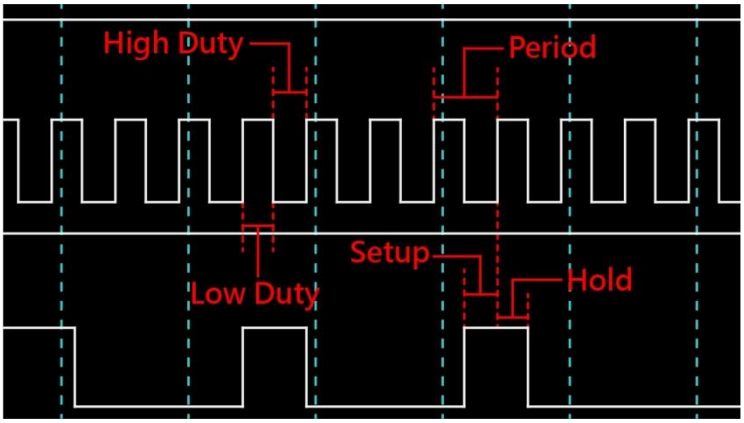
SCK Period Max.: Trigger when the value is more than the maximum SCK period.

SCK High Duty Min.: Trigger when the value is less than the minimum SCK High Duty.

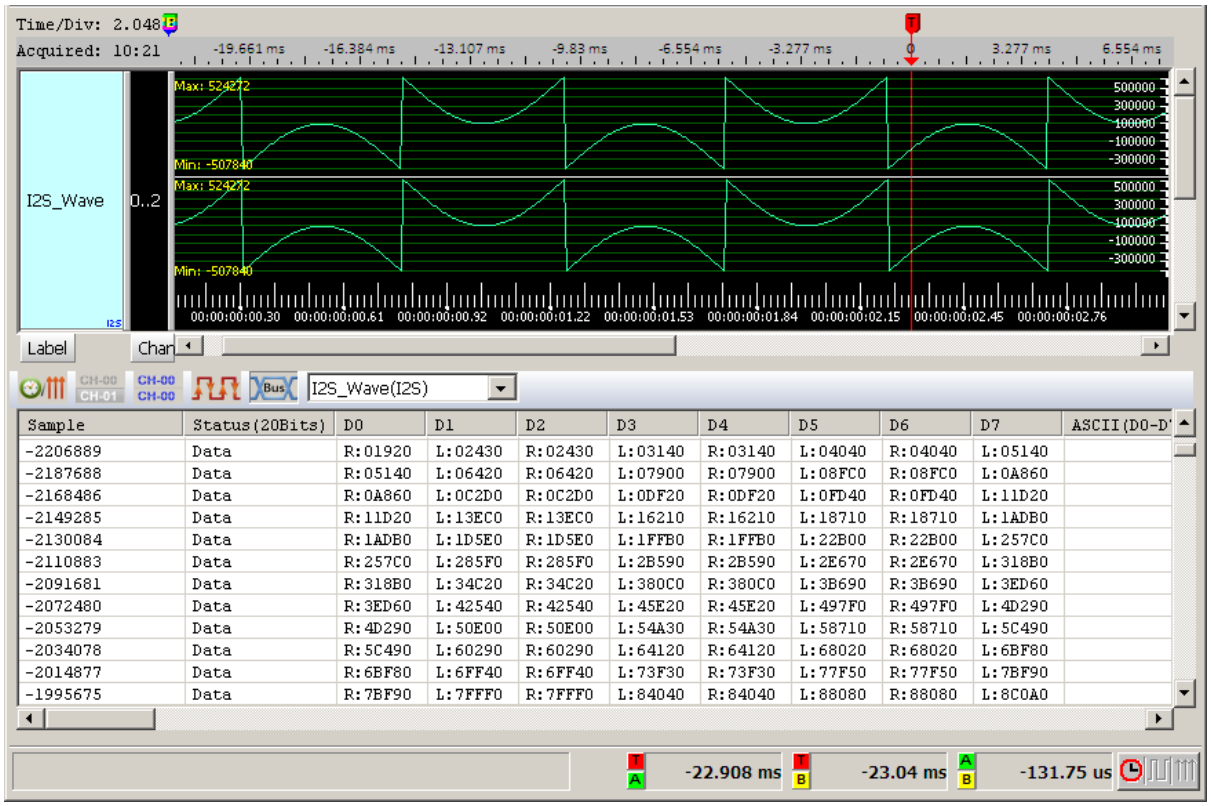
SCK Low Duty Min.: Trigger when the value is less than the minimum SCK Low Duty.

Setup Time: Trigger when the value is less than the Setup time.

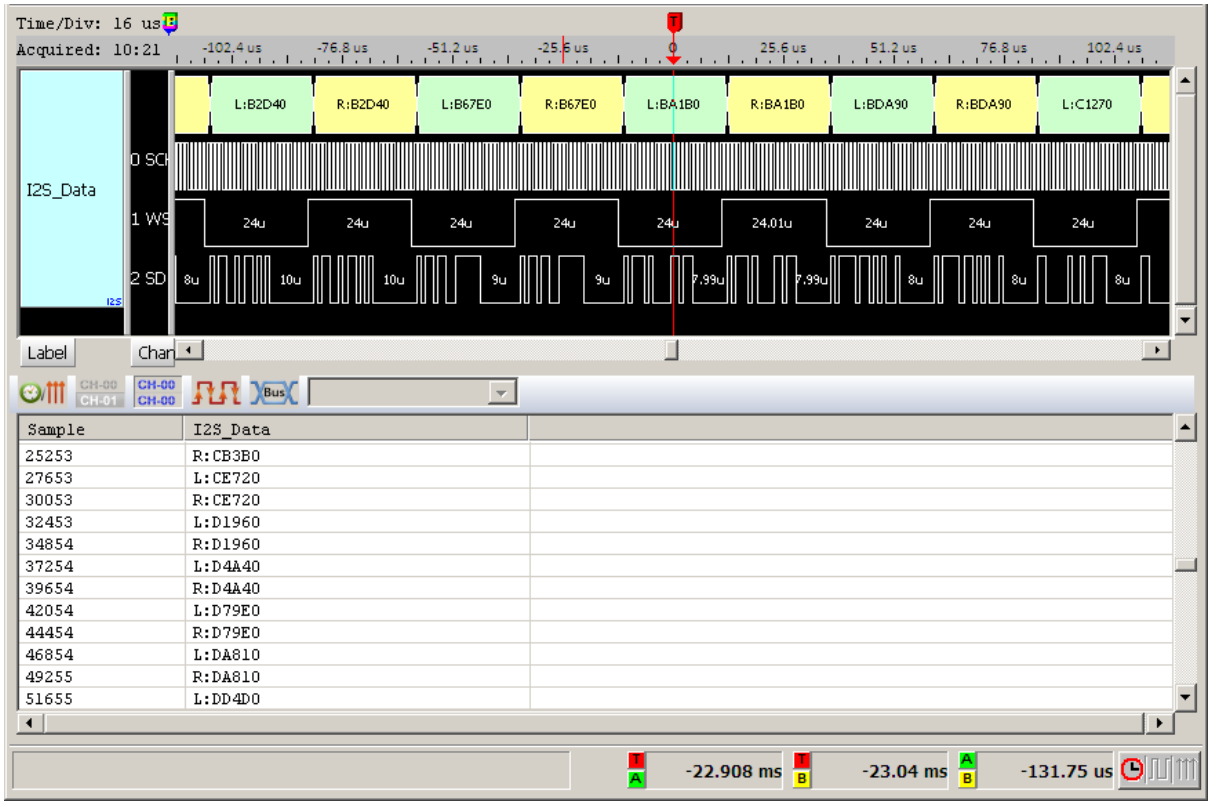
Hold Time: Trigger when the value is less than the Hold time.



Result



Sample	Status(20Bits)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D'
-2206889	Data	R:01920	L:02430	R:02430	L:03140	R:03140	L:04040	R:04040	L:05140	
-2187688	Data	R:05140	L:06420	R:06420	L:07900	R:07900	L:08FC0	R:08FC0	L:0A860	
-2168486	Data	R:0A860	L:0C2D0	R:0C2D0	L:0DF20	R:0DF20	L:0FD40	R:0FD40	L:11D20	
-2149285	Data	R:11D20	L:13EC0	R:13EC0	L:16210	R:16210	L:18710	R:18710	L:1ADB0	
-2130084	Data	R:1ADB0	L:1D5E0	R:1D5E0	L:1FFB0	R:1FFB0	L:22B00	R:22B00	L:257C0	
-2110883	Data	R:257C0	L:285F0	R:285F0	L:2B590	R:2B590	L:2E670	R:2E670	L:318B0	
-2091681	Data	R:318B0	L:34C20	R:34C20	L:380C0	R:380C0	L:3B690	R:3B690	L:3ED60	
-2072480	Data	R:3ED60	L:42540	R:42540	L:45E20	R:45E20	L:497F0	R:497F0	L:4D290	
-2053279	Data	R:4D290	L:50E00	R:50E00	L:54A30	R:54A30	L:58710	R:58710	L:5C490	
-2034078	Data	R:5C490	L:60290	R:60290	L:64120	R:64120	L:68020	R:68020	L:6BF80	
-2014877	Data	R:6BF80	L:6FF40	R:6FF40	L:73F30	R:73F30	L:77F50	R:77F50	L:7BF90	
-1995675	Data	R:7BF90	L:7FFF0	R:7FFF0	L:84040	R:84040	L:88080	R:88080	L:8C0A0	

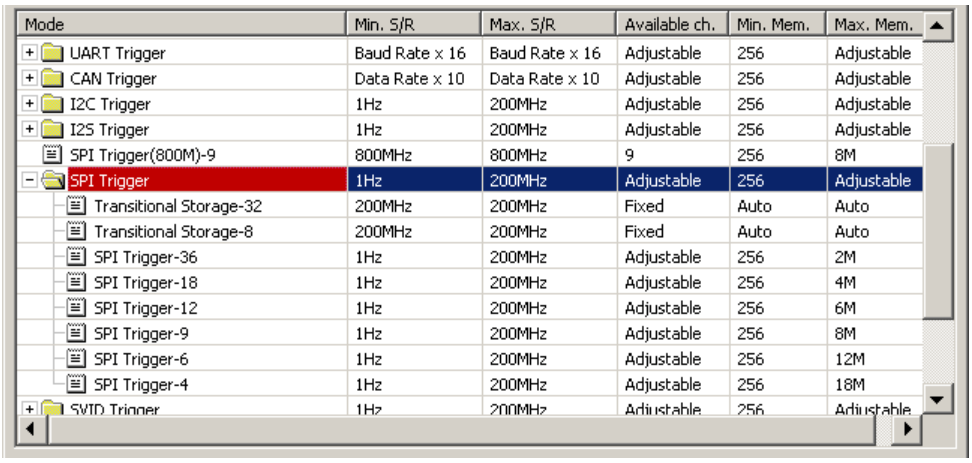


Sample	I2S_Data
25253	R:CB3B0
27653	L:CE720
30053	R:CE720
32453	L:D1960
34854	R:D1960
37254	L:D4A40
39654	R:D4A40
42054	L:D79E0
44454	R:D79E0
46854	L:DA810
49255	R:DA810
51655	L:DD4D0

SPI Trigger

The settings dialog box below.

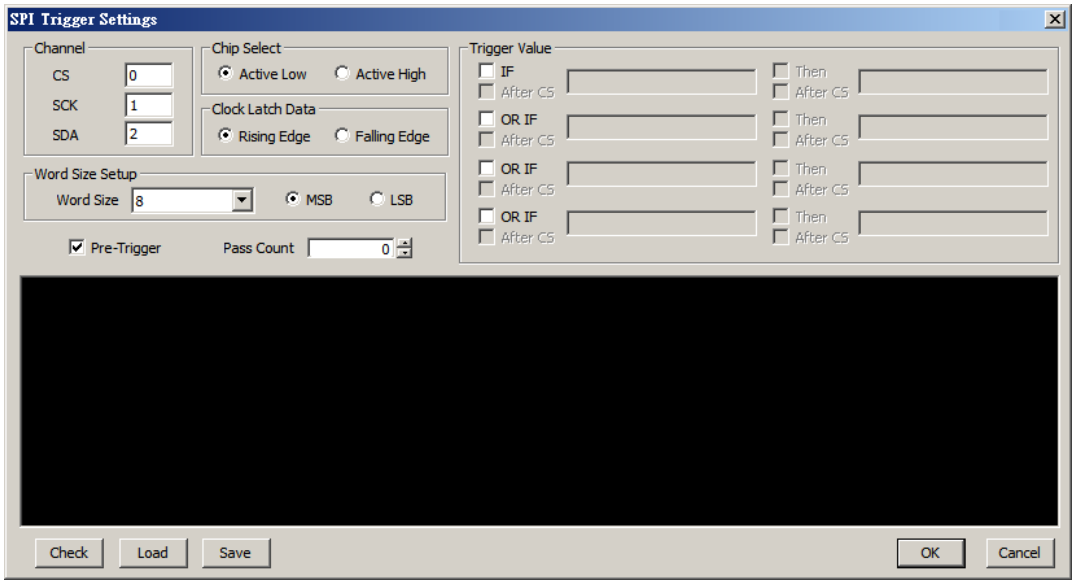
If need higher Sample rate for SPI, choose SPI-800M which is 800MHz Sample Rate with 9 channels. In SPI-800M, you can only use the default parameter settings.



Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
UART Trigger	Baud Rate x 16	Baud Rate x 16	Adjustable	256	Adjustable
CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
SPI Trigger-36	1Hz	200MHz	Adjustable	256	2M
SPI Trigger-18	1Hz	200MHz	Adjustable	256	4M
SPI Trigger-12	1Hz	200MHz	Adjustable	256	6M
SPI Trigger-9	1Hz	200MHz	Adjustable	256	8M
SPI Trigger-6	1Hz	200MHz	Adjustable	256	12M
SPI Trigger-4	1Hz	200MHz	Adjustable	256	18M
SYID Trigger	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Setting

Select SPI Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button ( ) on Toolbar (or Device menu) to show the SPI Trigger Settings dialog box below.



Channel: Select three channels for Chip Select (CH 0), serial clock (CH 1), and serial data (CH 2).

Chip Select: Select Active Low or Active High to enable Chip Select.

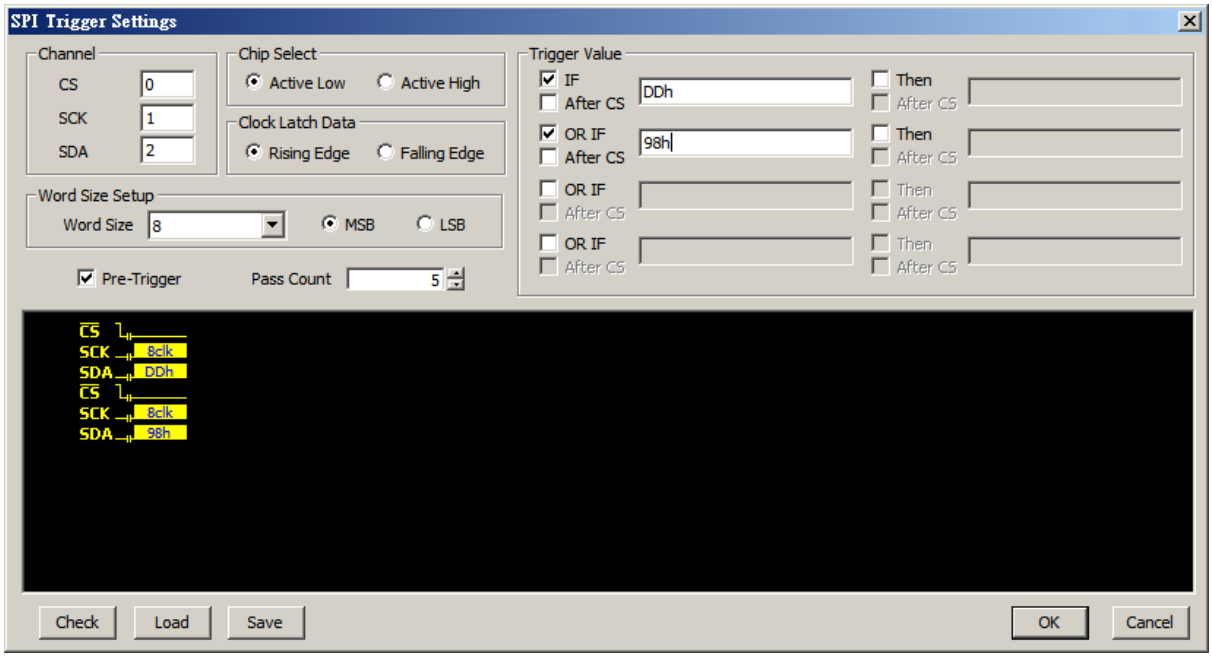
Clock Latch Data: Select Rising Edge or Falling Edge to latch data.

Word Size Setup: Select the number of data bits (4~24).

MSB/LSB: Select MSB first (MSB → LSB) or LSB first (LSB → MSB) to transmit the data.

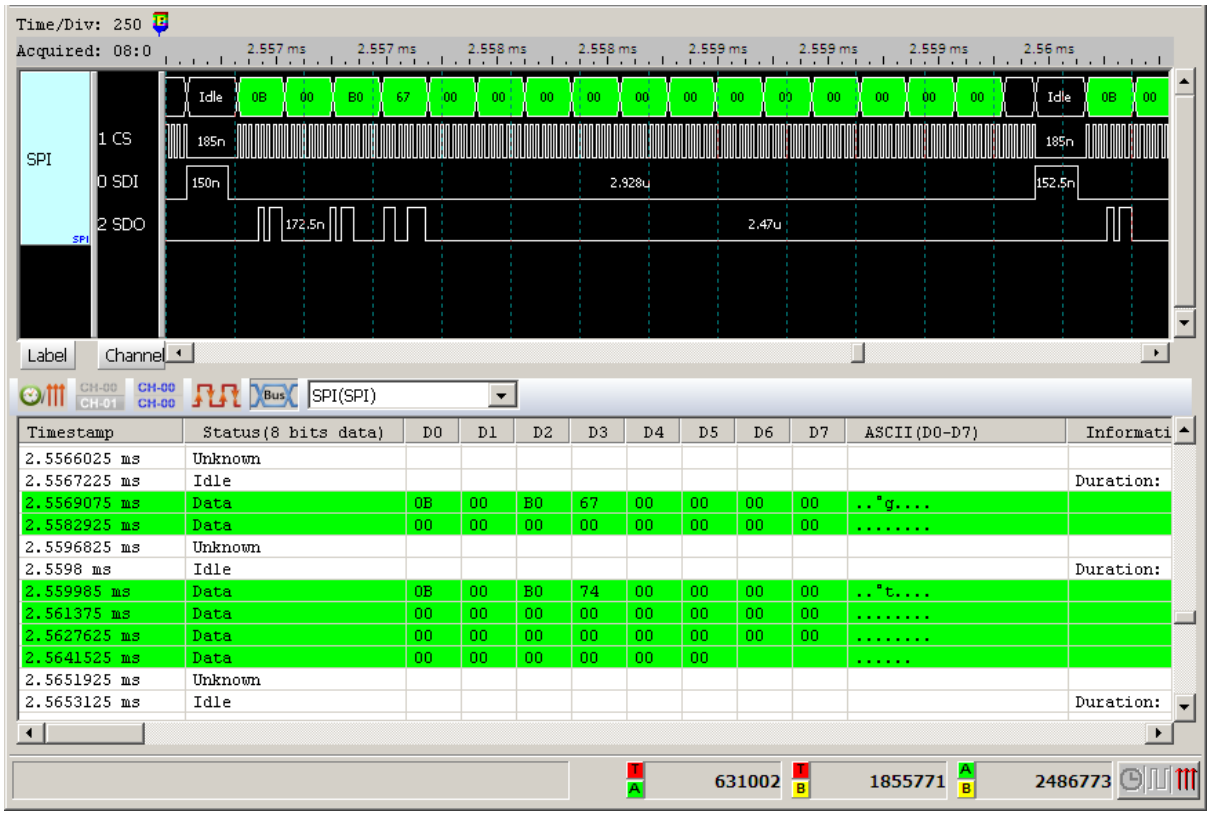
Trigger Value: The SPI Trigger has four IF/Then triggers, but ONLY one will trigger when its condition is met first. The condition can be in characters, a string, decimal numbers or hexadecimal codes with no more than 16 characters and: Characters and the string MUST be within single or double quotation marks, e.g. 'A' or "Acute"; A string can be entered with characters, a string and hexadecimal code with a blank space between each two different inputs, 'A'_"cute" or 'A'_63h_'u'_'t'_65h e.g.

Pass Count: Pass Count will pass N times that triggers occurred. If the Pass Count is 5 as the dialog box below, all triggers in all IF/Then conditions are counted and the instrument will trigger at the 6th trigger.



Check Trigger: Check the validity of trigger conditions.

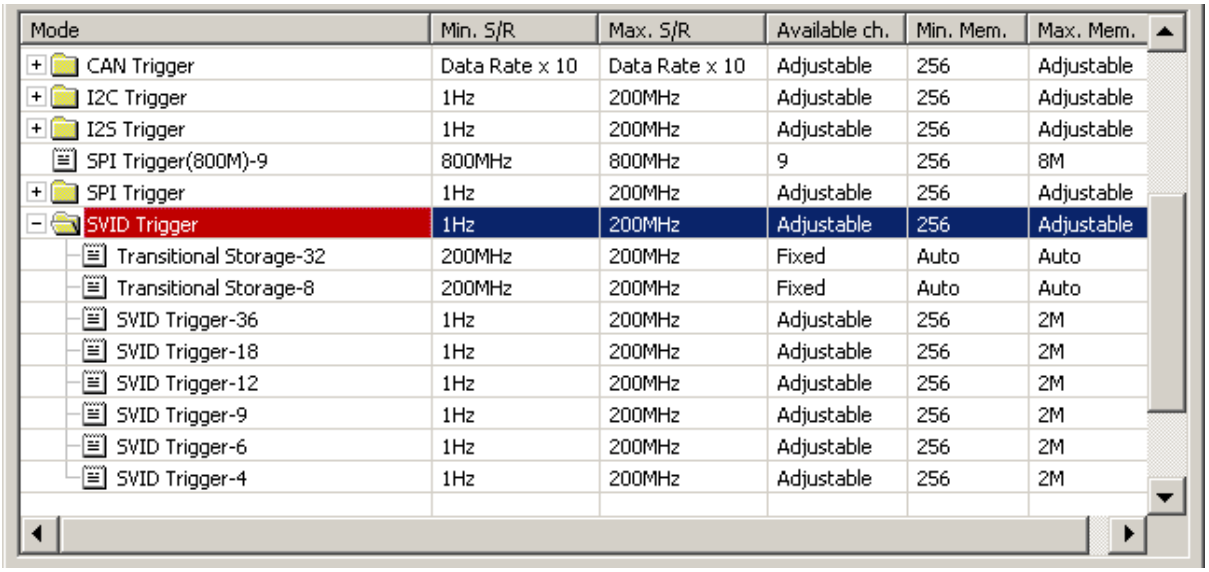
Result



Timestamp	Status(8 bits data)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Informati
2.5566025 ms	Unknown										
2.5567225 ms	Idle										Duration:
2.5569075 ms	Data	0B	00	B0	67	00	00	00	00	..°g....	
2.5582925 ms	Data	00	00	00	00	00	00	00	00	....	
2.5596825 ms	Unknown										
2.5598 ms	Idle										Duration:
2.559985 ms	Data	0B	00	B0	74	00	00	00	00	..°t....	
2.561375 ms	Data	00	00	00	00	00	00	00	00	....	
2.5627625 ms	Data	00	00	00	00	00	00	00	00	....	
2.5641525 ms	Data	00	00	00	00	00	00			.....	
2.5651925 ms	Unknown										
2.5653125 ms	Idle										Duration:

SVID Trigger (Upon Request)

The settings dialog box below.

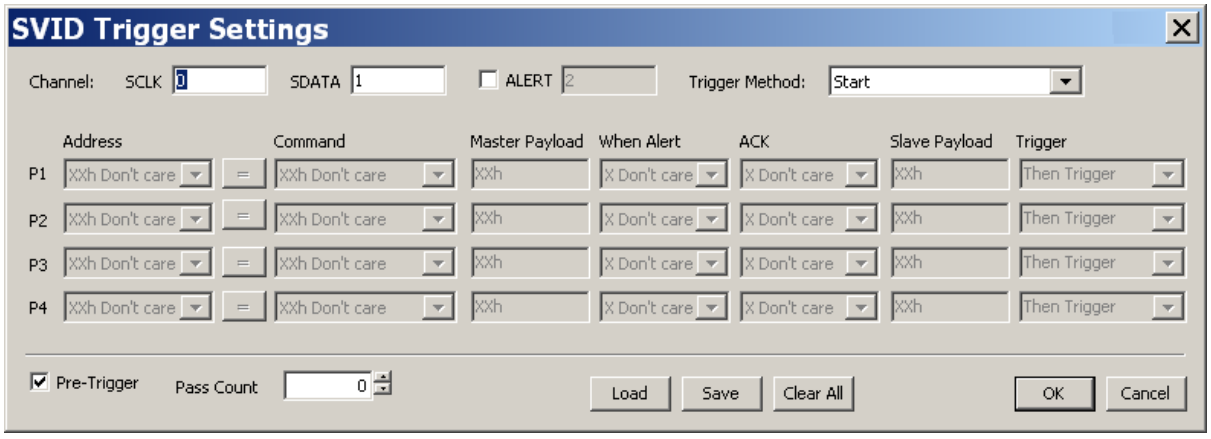


Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
SVID Trigger-36	1Hz	200MHz	Adjustable	256	2M
SVID Trigger-18	1Hz	200MHz	Adjustable	256	2M
SVID Trigger-12	1Hz	200MHz	Adjustable	256	2M
SVID Trigger-9	1Hz	200MHz	Adjustable	256	2M
SVID Trigger-6	1Hz	200MHz	Adjustable	256	2M
SVID Trigger-4	1Hz	200MHz	Adjustable	256	2M

If you have any issues with SVID protocol features, please contact your Intel Field Representative.

Trigger Settings

Select SVID Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button on Toolbar (or Device menu) to show the SVID Trigger Settings dialog box below.



Channel: Set the 2 channels (SCLK and SDATA) to form the trigger signal, ALERT

is option.

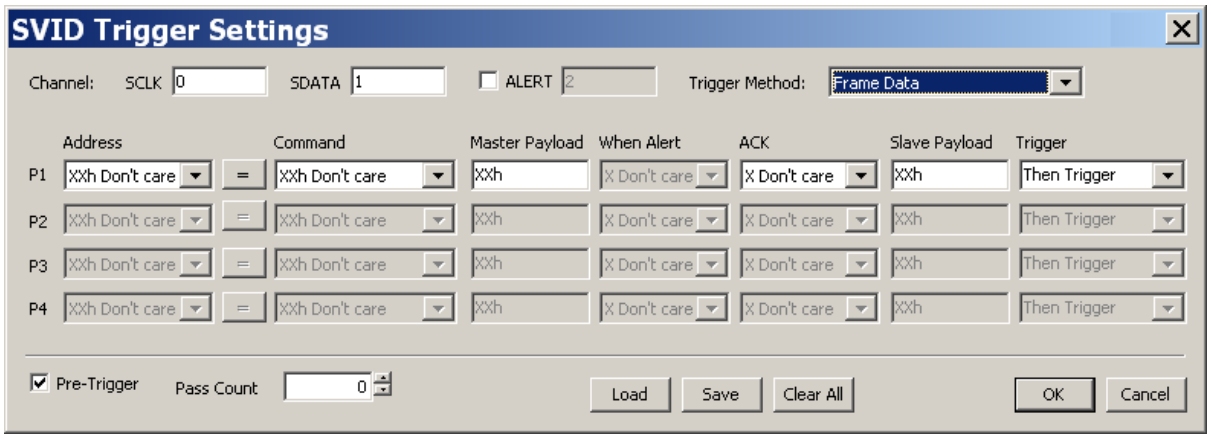
Trigger Mode:

Start: Trigger when the SVID packet is valid.

Frame Data: Trigger according to the frame data.

Parity Error: Trigger when the parity error happens.

Frame Data Settings:



You can set 4 (most) frame data packets as trigger conditions. Each column in those frame data can be set as any value or Don't care (xxh) and set trigger condition equal to the command or not.

The Payload column is 1 byte only, can be character (like 'A'), decimal number (like 65) or hexa-decimal number (like 41h), but any input value over 1 byte will be filtered.

The ALTER channel can be '0', '1' or don't care.

Trigger column includes:

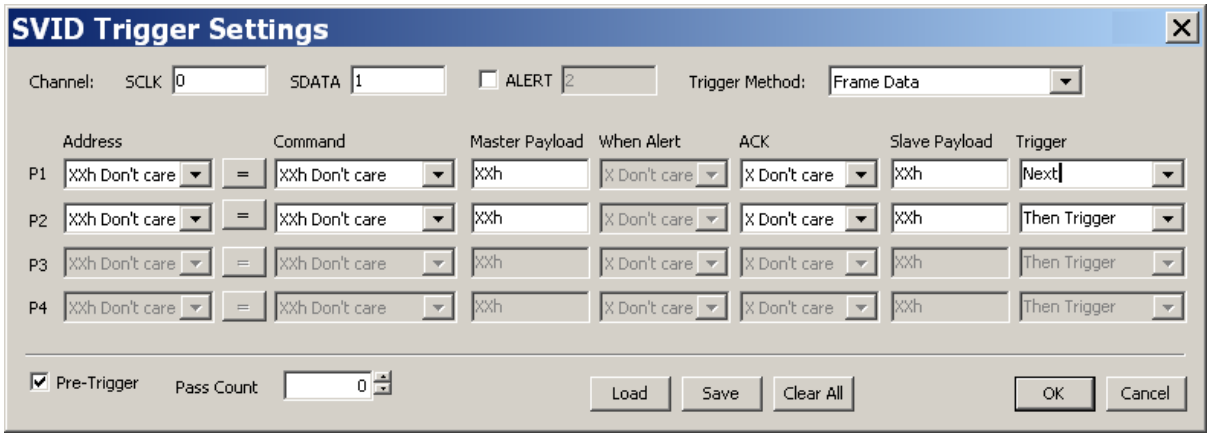
Then Trigger: If conditions matched, trigger right away.

Then If: If conditions matched, wait for the next matched frame data.

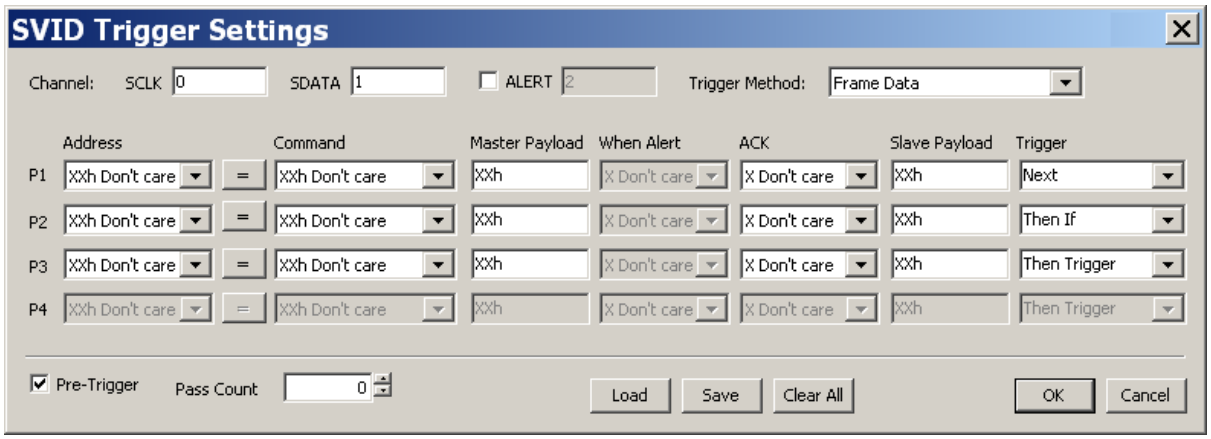
Next: If conditions matched, wait for any next frame data.

Pass Count: The Pass Count function in the SVID Trigger is very unique. If you set the frame data conditions like P1 and P2 in the SVID Trigger Settings table below, the

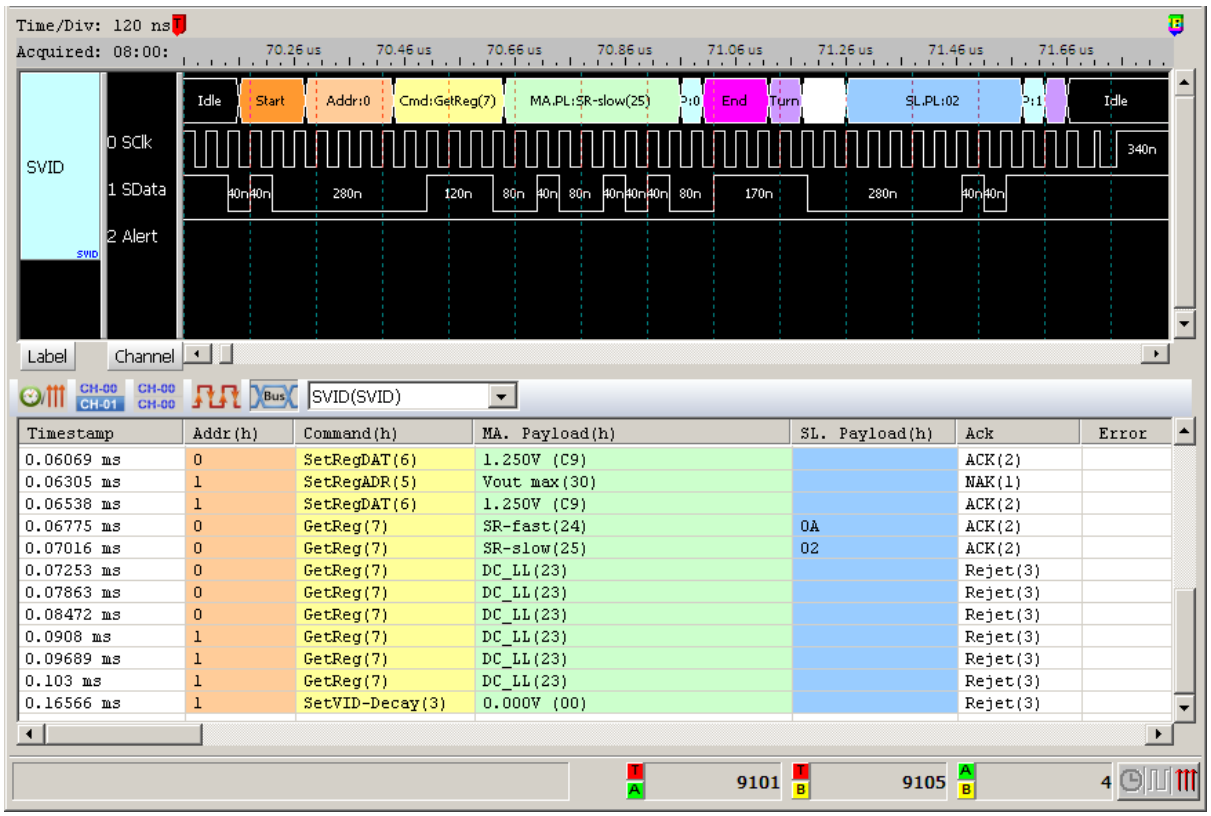
pass count will only count 1 time when both P1 and P2 are matched. It will trigger after 2 matches (P1 and P2).



If you set the frame data conditions like P1, P2 and P3 in the SVID Trigger Settings table below, the pass count will only count 1 time when both P1 and P2 are matched first and then P3 is matched. It will trigger after 2 matches (P3).



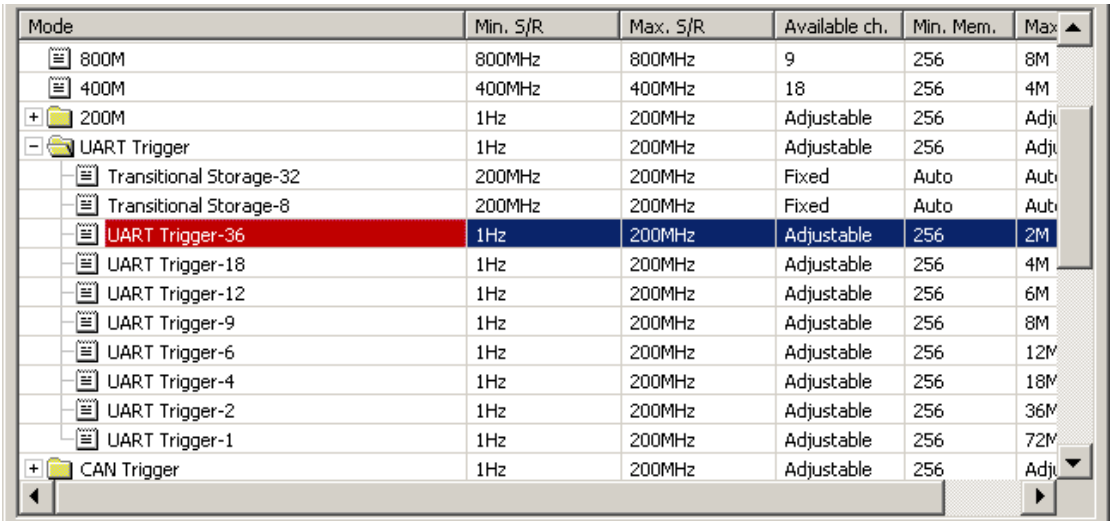
Result



Timestamp	Addr(h)	Command(h)	MA. Payload(h)	SL. Payload(h)	Ack	Error
0.06069 ms	0	SetRegDAT(6)	1.250V (C9)		ACK(2)	
0.06305 ms	1	SetRegADR(5)	Vout max(30)		NAK(1)	
0.06538 ms	1	SetRegDAT(6)	1.250V (C9)		ACK(2)	
0.06775 ms	0	GetReg(7)	SR-fast(24)	0A	ACK(2)	
0.07016 ms	0	GetReg(7)	SR-slow(25)	02	ACK(2)	
0.07253 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.07863 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.08472 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.0908 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.09689 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.103 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.16566 ms	1	SetVID-Decay(3)	0.000V (00)		Rejet(3)	

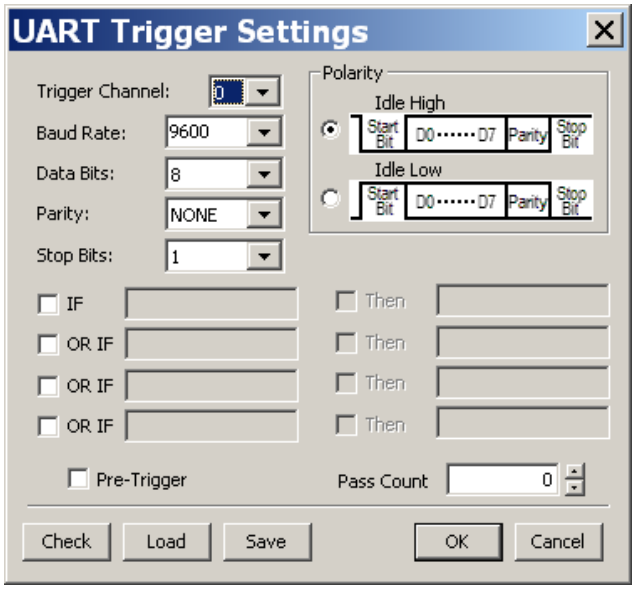
UART Trigger

The settings dialog box below.



Trigger Settings

Select UART Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button( ) on Toolbar (or Device menu) to show the UART Trigger Settings dialog box below.



Trigger Channel: Only one channel can be selected.

Baud Rate: The range is 110 ~ 2M bits per second (bps).

Data Bits: 5, 6, 7, or 8.

Parity: EVEN, ODD, or NONE.

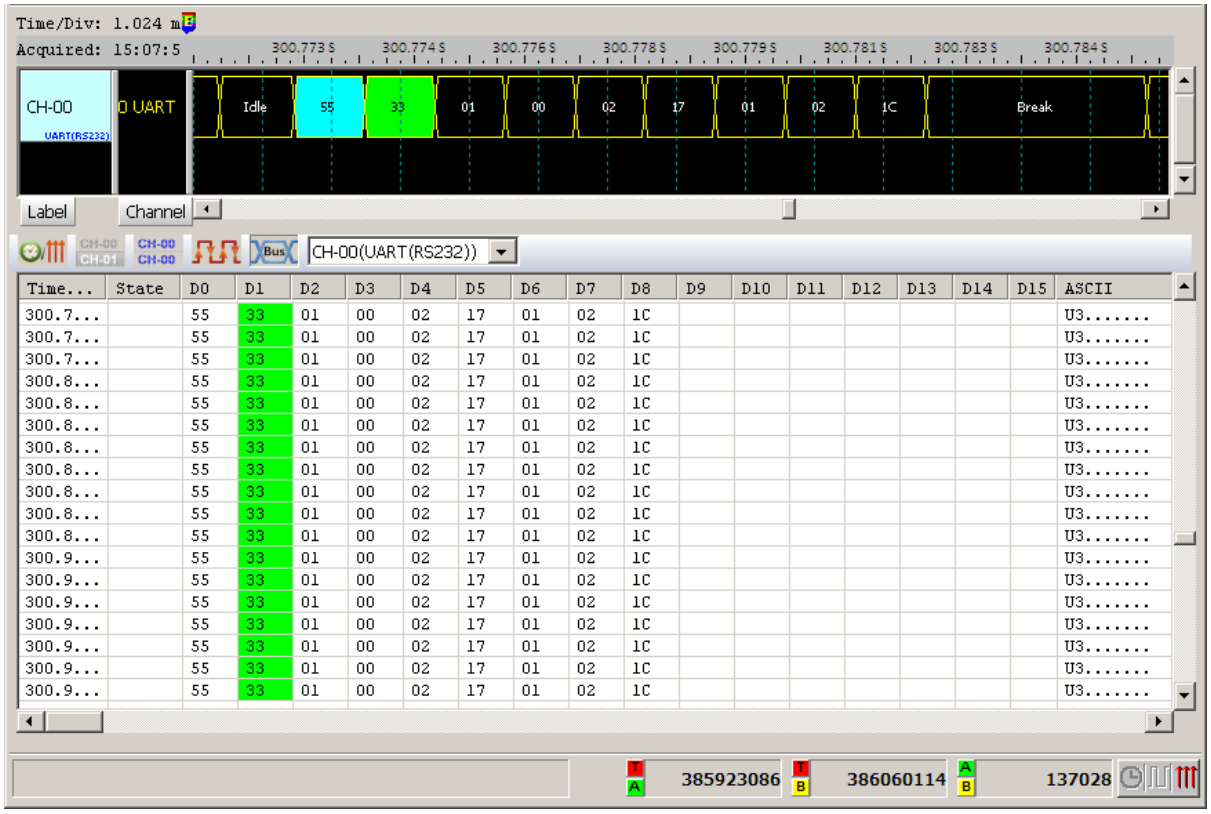
Stop Bits: 1 or 2.

Trigger Type: Falling Edge or Rising Edge.

IF/Then trigger: The UART Trigger has four IF/Then triggers, but ONLY one will trigger when its condition is met first. The condition can be in characters, a string, decimal numbers or hexadecimal codes with no more than 16 characters and: Characters and the string MUST be within single or double quotation marks, e.g. 'A' or "Acute"; A string can be entered with characters, a string and hexadecimal code with a blank space between each two different inputs, 'A'_"cute" or 'A'_63h_'u'_'t'_65h e.g.

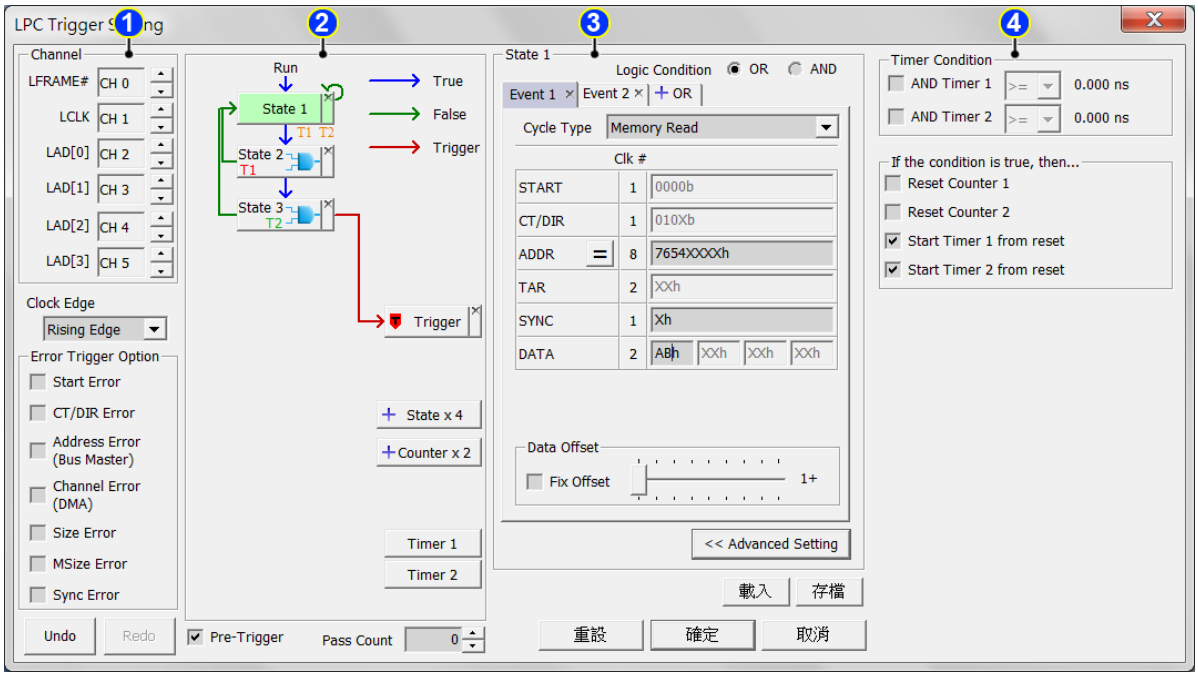
Check Trigger Settings: Check the validity of trigger conditions.

Result



Clause Trigger

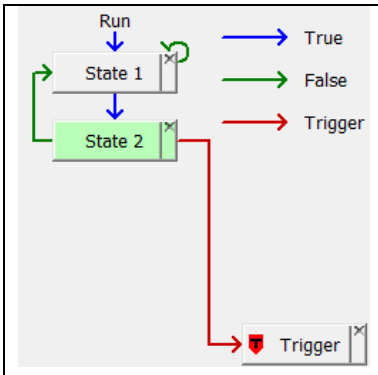
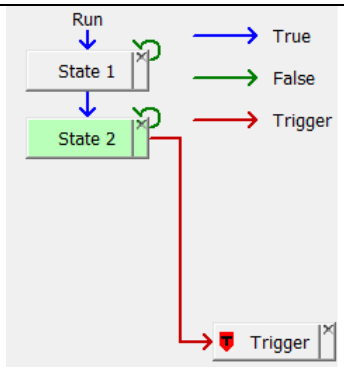
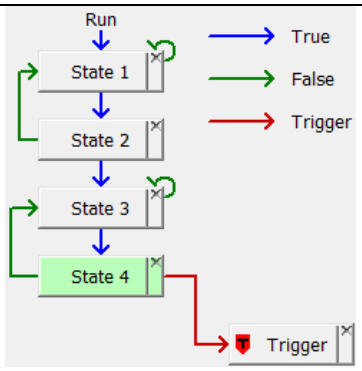
The Clause trigger settings dialog box is as below.

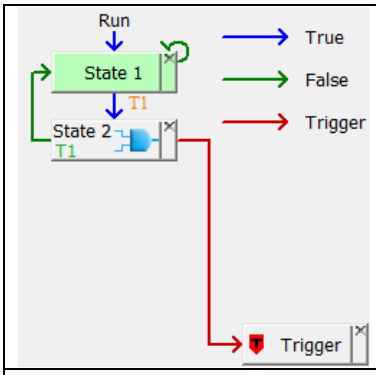
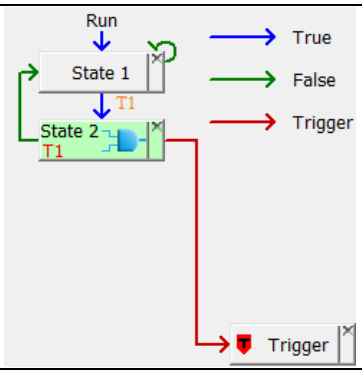


1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.

2. Flow chart

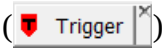
		
State 1 next State 2	State 1 then State 2	State 1 next State 2 then State 3 next State 4

	
State 1 (Active T1) next State 2 (Time >= T1)	State 1 (Active T1) next State 2 (Time < T1)

A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:

Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.

Double click any state, the state will branch to itself if it is false.

Click the state button and trigger button (

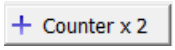
): triggere when the state conditions is satisfied.

Delete any state by clicking the cross sign on the state.

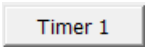
Clear the links to the trigger button by clicking on the trigger button (

)

Click 

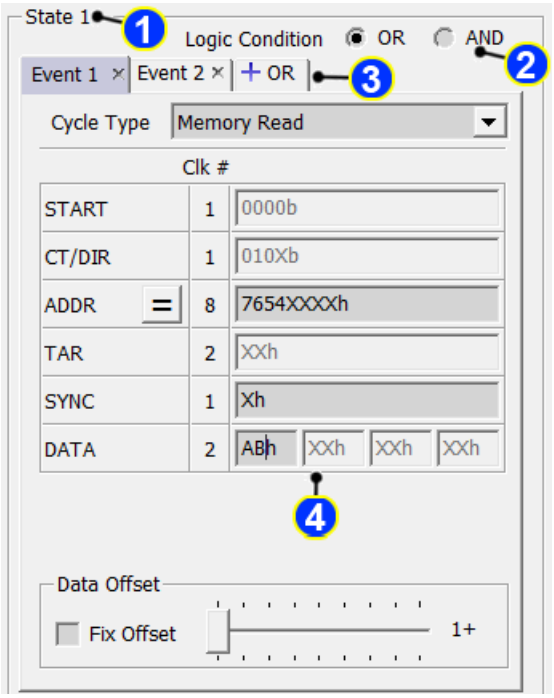
and 

to add a new state.



: The timer ranges from 5 ns to 8 days.

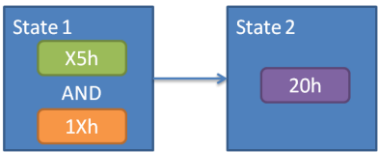
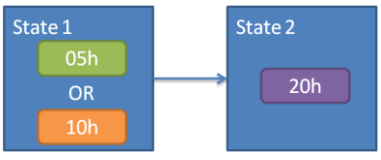
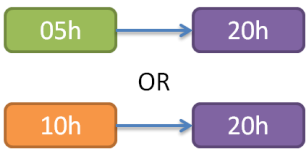
3. State settings



The trigger conditions of the state:

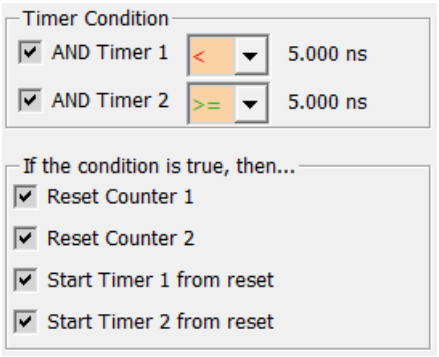
1. The current state index
2. Logic condition between every event in the state.
3. Switch between the tab windows to edit the trigger events . Click | + OR | / | + AND | to add new events (up to 8 events).
4. The bus trigger settings.

The relations between events and the trigger condition:

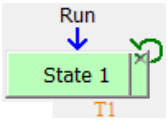
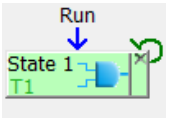
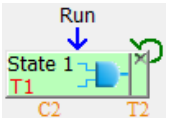
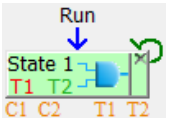
	AND	OR
Event settings		
Trigger condition		

4. Timer and Counter settings

Press Advanced Setting >> button to edit the timer/counter reset settings of the state.



The following table describes the state button icons:

				
Conditions	State 1	State 1 And timer > T1	State 1 And timer < T1	State 1 And T2 < timer <T1
satisfied condition	Start T1	X	Start T2 Reset C2	Start T1 and T2 Reset C1 and C2

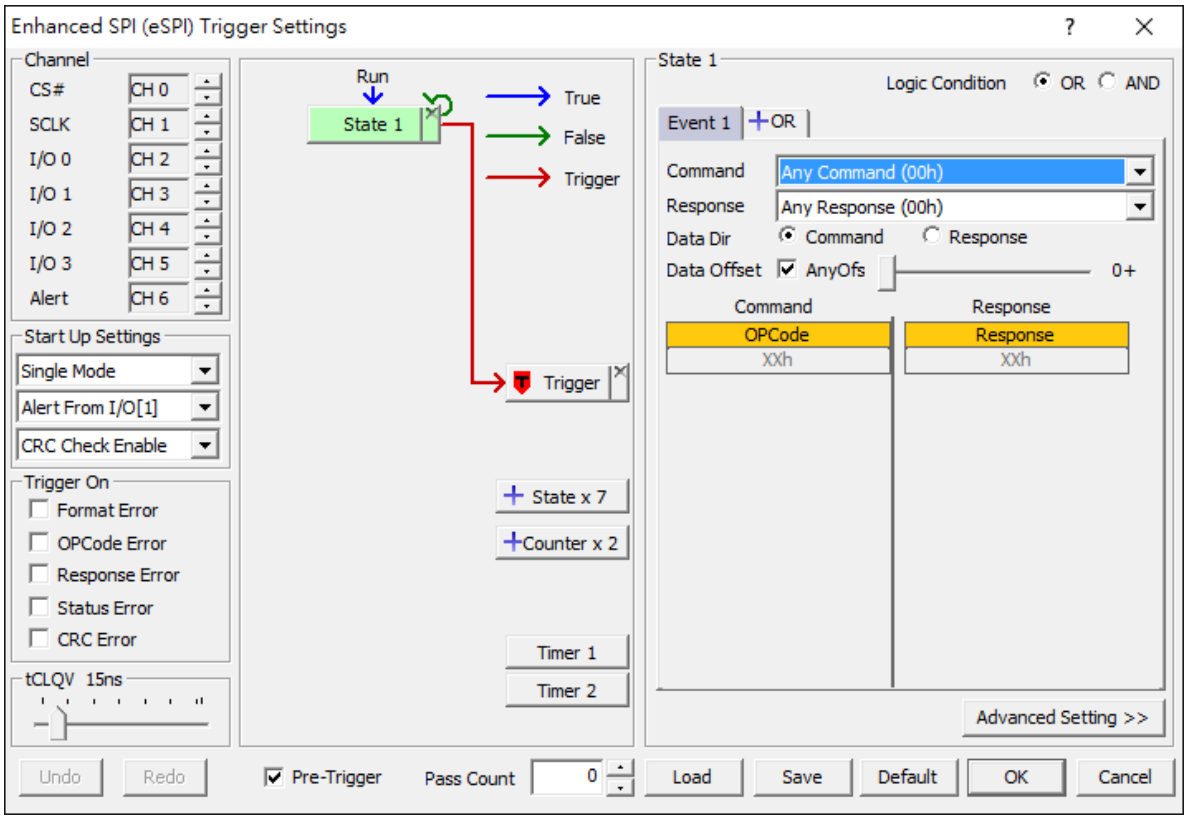
eSPI Trigger

Select eSPI Trigger in Hardware Settings.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
200M	1Hz	200MHz	Adjustable	256	Adjustable
CAN Trigger	1Hz	200MHz	Adjustable	256	Adjustable
eSPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage(400M)-16	400MHz	400MHz	Fixed	Auto	Auto
eSPI Trigger(400M)-18	400MHz	400MHz	18	256	4M
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
eSPI Trigger-36	1Hz	200MHz	Adjustable	256	2M
eSPI Trigger-18	1Hz	200MHz	Adjustable	256	4M
eSPI Trigger-12	1Hz	200MHz	Adjustable	256	6M
eSPI Trigger-9	1Hz	200MHz	Adjustable	256	8M
eSPI Trigger-6	1Hz	200MHz	Adjustable	256	12M
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
LIN Trigger	1Hz	200MHz	Adjustable	256	Adjustable
LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Settings

Select “eSPI” in Trigger Settings.



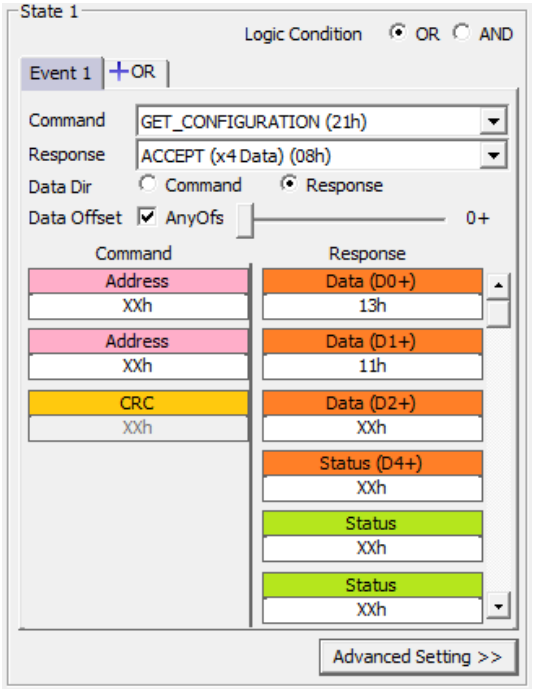
Channel: Please refer to the Bus Decode of eSPI.

Start Up Settings: There are three modes including single, dual and quad mode. Set the current mode to be any of them and the setting would be automatically switched by monitoring the bus in hardware. Then choose the Alert signal and the CRC Check.

Trigger On: Select any error of format, OP Code, Response, Status and CRC to trigger.

tCLQV: The delay time of I/O and Clock in Response. The incorrect setting may cause that Response cannot be triggered.

Trigger State Settings:



eSPI Trigger offers many kinds of Command and Response. You may set “Any Command” to capture the signal, and choose the proper setting of trigger by the decode of eSPI.

Timestamp	OpCode/Response	CycType	Tag	LEN	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
-0.00000245 S	GET_CONFIGURATION(21)				0010											58	
0.00000086 S	ACCEPT(08)					13	11	00	00					....	030F	95	
0.000003 S	SET_CONFIGURATION(22)				0010	01	11	00	00					....		F5	
0.000005935 S	ACCEPT(08)														030F	9B	
0.000008455 S	GET_STATUS(25)															FB	
0.000009365 S	ACCEPT(08)														030F	9B	
0.001601195 S	GET_CONFIGURATION(21)				0010											58	
0.001602795 S	ACCEPT(08)					13	11	00	00					....	030F	95	
0.001606635 S	SET_CONFIGURATION(22)				0010	01	11	00	00					....		F5	
0.001609575 S	ACCEPT(08)														030F	9B	

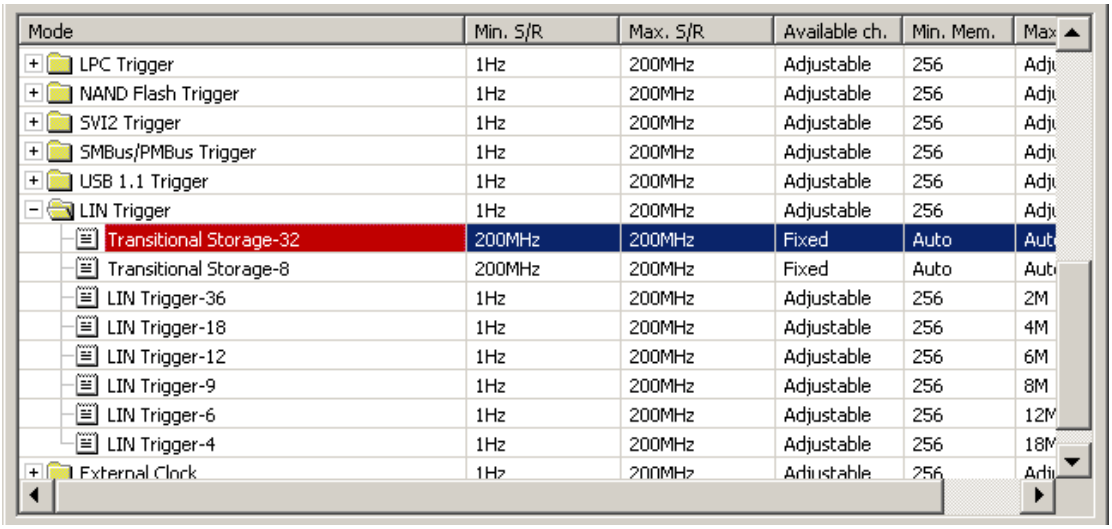
eSPI decode result

Data Dir: Trigger the data in the Command or Response.

Data Offset: Trigger the data from start of data frame without any offset. For example, setting D0 13h will check the first byte of data frame. With any offset, the siganl would be triggered by the byte pattern. For instance, setting D0+ XXh D1+ 11h, and the byte pattern of XXh and 11h will be triggered regardless of the position of the data.

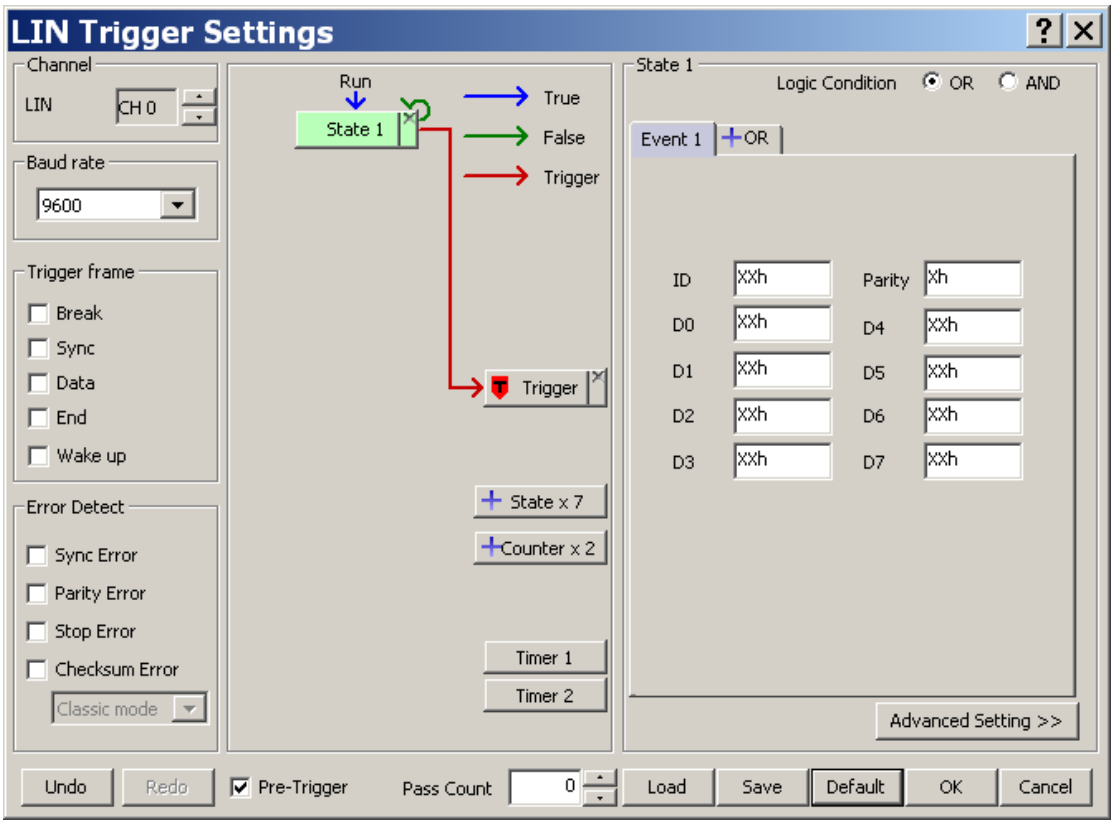
LIN Trigger

Select LIN Trigger Settings.



Trigger Settings

The LIN trigger settings dialog box is as below.



Channel: Select channels.

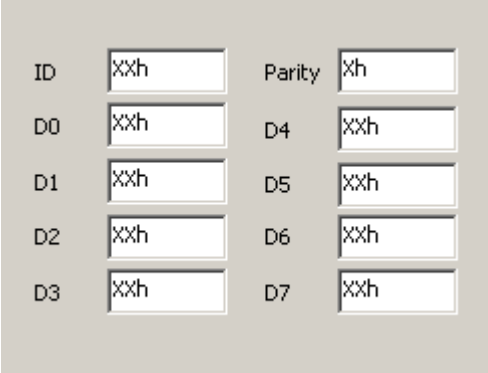
Baud rate: Select baud rate.

Trigger frame: Provide Break / Sync / Data / End / Wake up triggers.

Error Detect: Provide Sync / Parity / Stop / Checksum error triggers, checksum error detect include “Classic” and “Enhanced” mode.

Redo / Undo: Click these buttons to redo/restore previous setting.

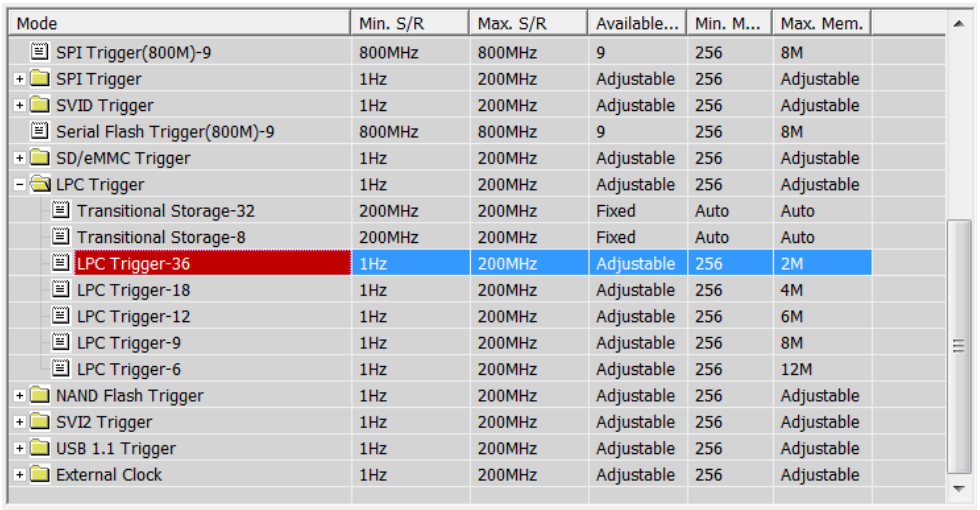
Trigger settings:



Provide the ID / Parity / Data triggers。

LPC Trigger

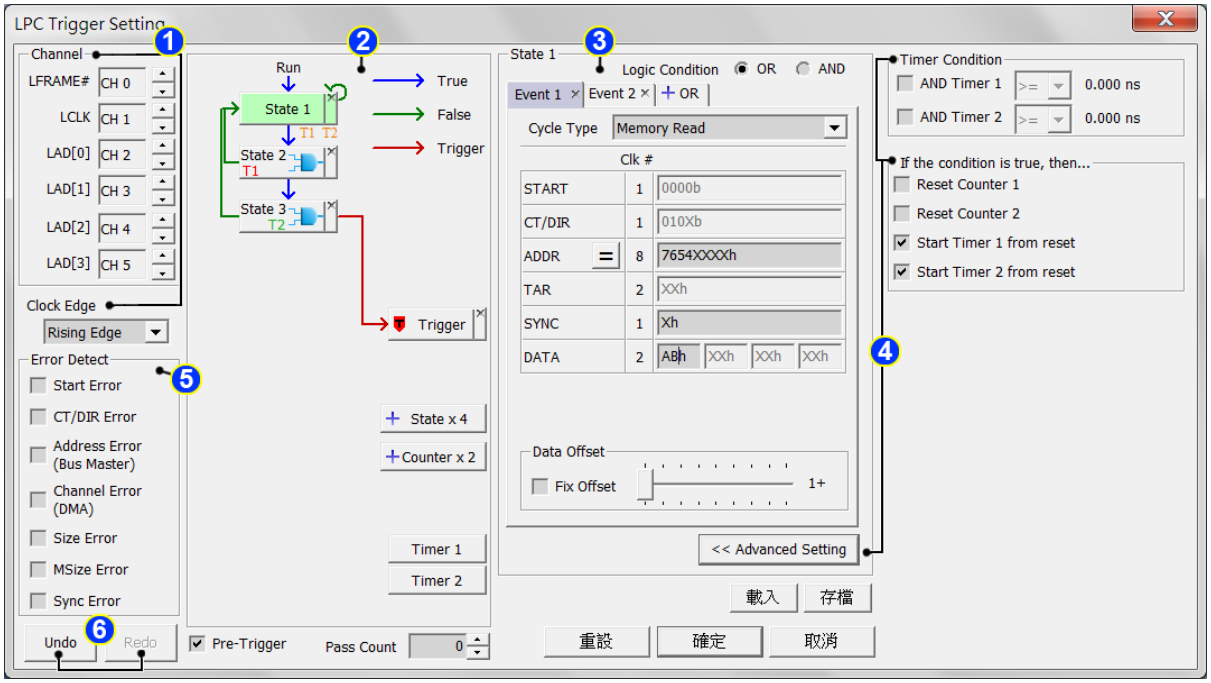
The LPC trigger settings dialog box is as below.



Mode	Min. S/R	Max. S/R	Available...	Min. M...	Max. Mem.
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
+ SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
+ SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M
+ SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
- LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
LPC Trigger-36	1Hz	200MHz	Adjustable	256	2M
LPC Trigger-18	1Hz	200MHz	Adjustable	256	4M
LPC Trigger-12	1Hz	200MHz	Adjustable	256	6M
LPC Trigger-9	1Hz	200MHz	Adjustable	256	8M
LPC Trigger-6	1Hz	200MHz	Adjustable	256	12M
+ NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable
+ SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
+ USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
+ External Clock	1Hz	200MHz	Adjustable	256	Adjustable

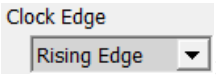
Trigger Settings

Select LPC Trigger Settings.



1. Channel

Select channels

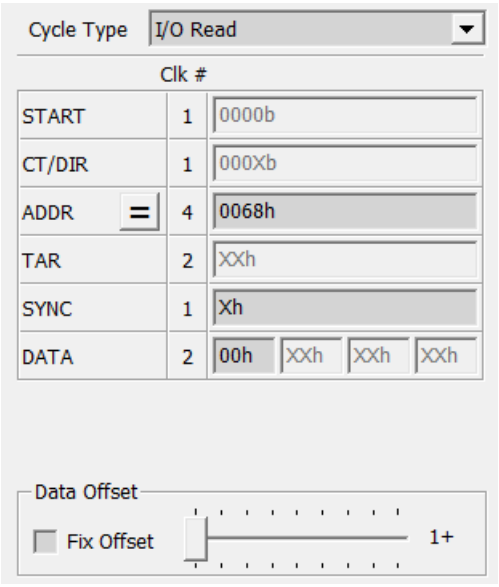


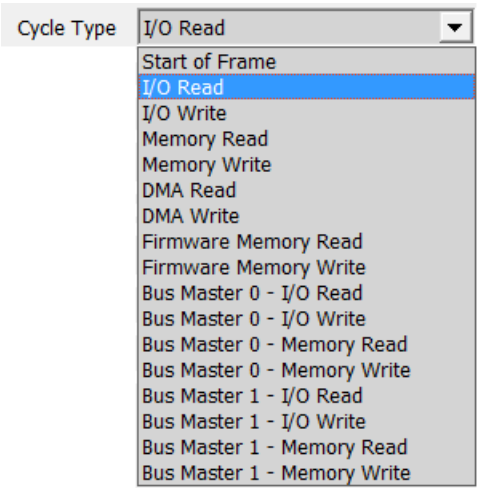
: Latch data when Clock Rising or Falling Edge

2. Clause trigger settings

Please refer to the Clause Trigger

3. Trigger settings





The LPC trigger supports many cycle types. Please select “Start of Frame” and capture, then choose the cycle type you need.

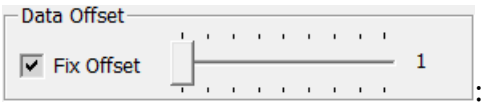
Sample	Field	#Clocks	LAD	Comment
7002909	START	1	0	Used for Memory or I/O or DMA cycles.
7002917	CYCLETYPE+DIR	1	0	I/O Read
7002925	ADDR	4	0068	
7002959	TAR	2	FF	
7002975	SYNC	1	6	Long Wait
7002984	SYNC	1	6	Long Wait
7002992	SYNC	1	6	Long Wait
7003000	SYNC	1	0	Ready
7003009	DATA	2	00	
7003025	TAR	2	FF	
7082283	START	1	0	Used for Memory or I/O or DMA cycles.
7082291	CYCLETYPE+DIR	1	0	I/O Read
7082299	ADDR	4	0064	

LPC decoder result

Other settings：

Switch =/≠/>/≤ by click = buttonmn.

The input ‘X’ means don’t care.



: Data offset setting

4. Timer and Counter

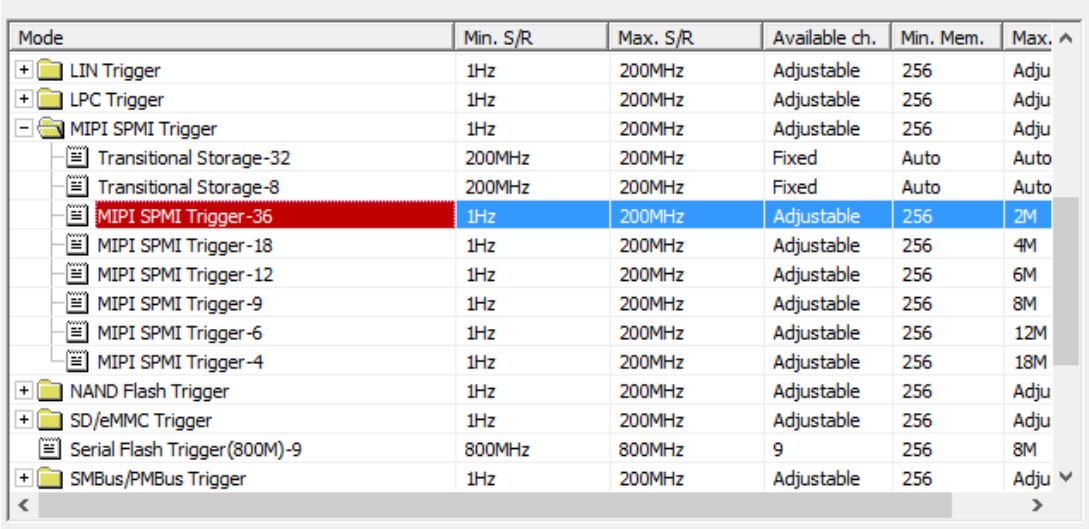
   Please refer to the Clause Trigger

5. Trigger when an error is detected based on the Intel® Low Pin Count Interface Specification.

6. Redo/Undo

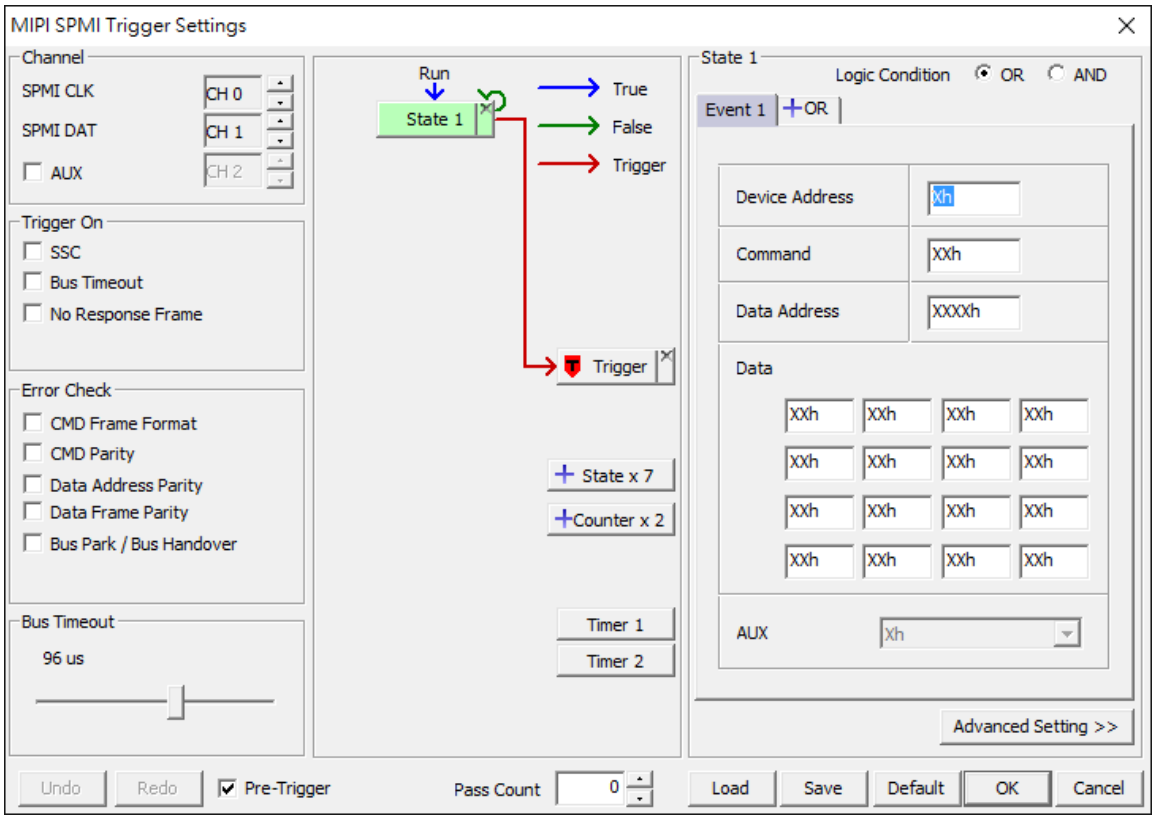
MIPI SPMI Trigger

Select eSPI Trigger in Hardware Settings.



Trigger Settings

Select “MIPI SPMI” in Trigger Settings.

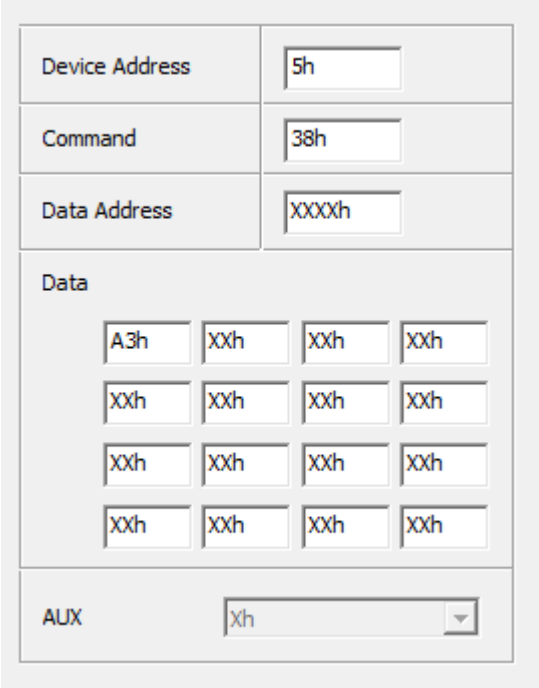


Trigger On: Select Sequence Start Condition (SSC), Bus Timeout, or No Response Frame to trigger.

Error Check: Check the error of Frame Format, Parity, and Bus Park / Bus Handover.

Bus Timeout: Set the period of time to wait for SSC.

State Settings:



MIPI SPMI Trigger offer Address, Command and Data parameter to trigger. You may capture the data with don't care (X). Trigger the specific address, command or data by the decode of MIPI SPMI.

Timestamp	A	SR	Device Address(Hex)	Command(Hex)	Data Address - High(Hex)	Data Address - Low(Hex)	Data Frame
-0.838595 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5C	46	00
-0.82933 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	5C	46	80
-0.02058 ms	MPL3		SA=05	38 (Extended Register Read Long: 1Bytes)	1D	40	00
-0.011155 ms	MPL3		SA=05	30 (Extended Register Write Long: 1Bytes)	1D	40	00
-0.00293 ms	MPL3		SA=05	38 (Extended Register Read Long: 1Bytes)	1D	41	A3
0.006135 ms	MPL3		SA=05	30 (Extended Register Write Long: 1Bytes)	1D	41	D2
3.5403 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	56	46	00
3.549725 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	56	46	80
4.058525 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	57	46	00
4.06811 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	57	46	80
4.343265 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5B	46	00
4.352585 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	5B	46	80
4.618265 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5C	46	00

MIPI SPMI decode result

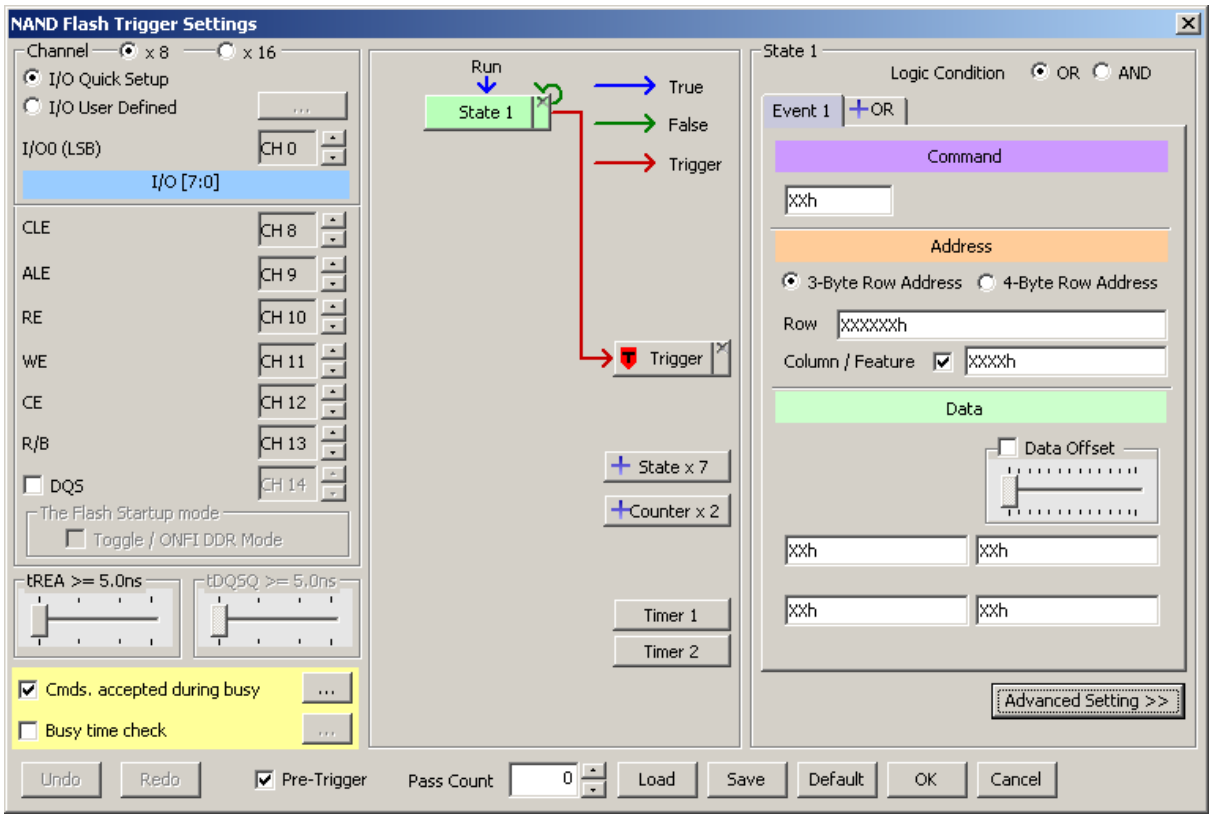
NAND Flash Trigger

The settings dialog box below.

Mode	Min. S/R	Max. S/R	Available...	Min. M...	Max. Mem.
CAN Trigger	Data Rate...	Data Rate...	Adjustable	256	Adjustable
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M
SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable
NAND Flash Trigger(400M)-18	400MHz	400MHz	18	256	4M
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
NAND Flash Trigger-36	1Hz	200MHz	Adjustable	256	2M
NAND Flash Trigger-18	1Hz	200MHz	Adjustable	256	4M
SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
External Clock	1Hz	200MHz	Adjustable	256	Adjustable

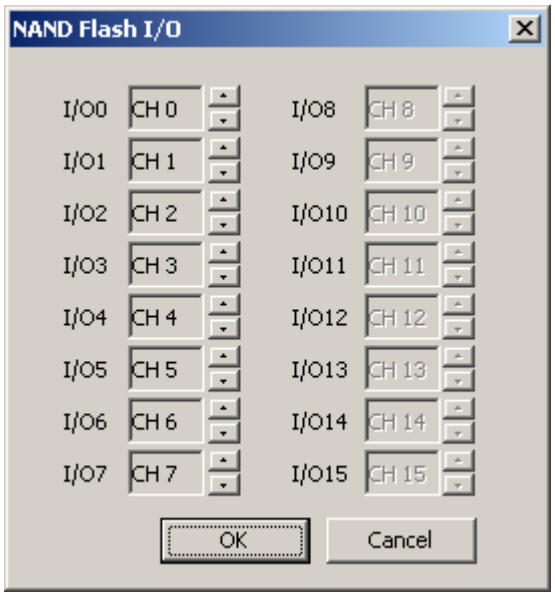
Trigger Settings

Select NAND Flash trigger settings dialog box is as below.

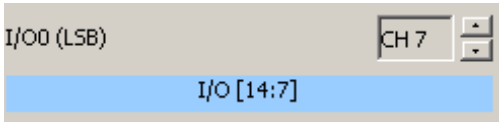


Channel:

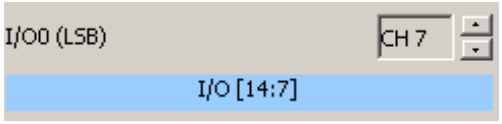
Select x8 or x16 to trigger 8 / 16 NAND Flash. Just set the I/O0 (LSB) channel when check the I/O Quick Setup; pressing the button when check the I/O User Defined will show the dialog below:



I/O Quick Setup:



Set LSB = CH 0, MSB = CH 7

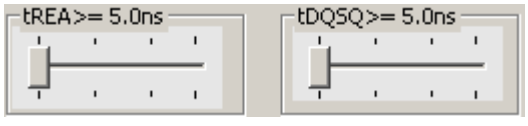


Set LSB = CH 7, MSB = CH 14

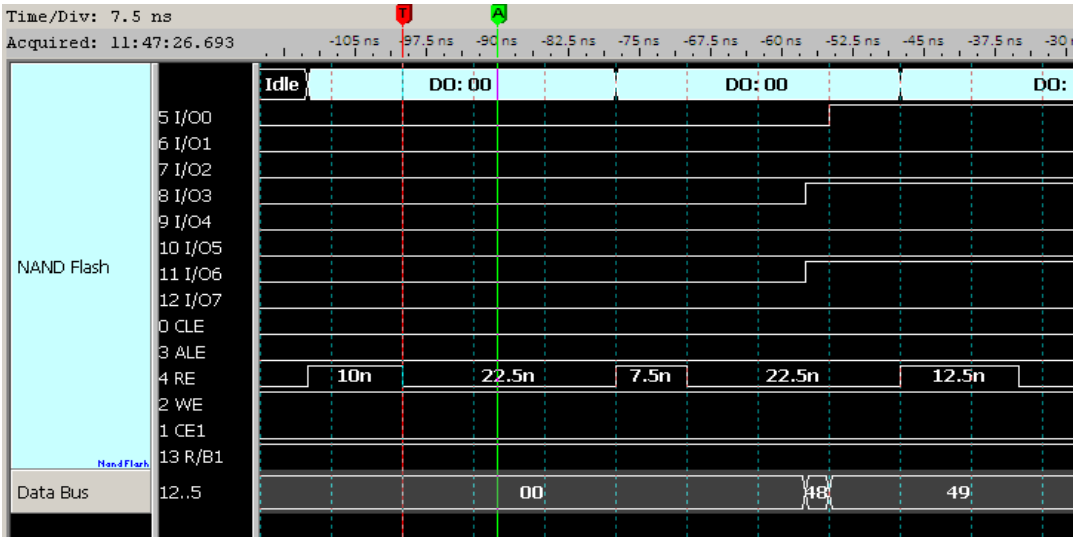
DQS: Check DQS pin to select the DDR (Double Data Rate) mode; SDR (Single Data Rate) mode default.

The Flash Startup mode: Check DQS pin and Toggle / ONFI DDR Mode when trigger NAND Command/Address/Data under NAND DDR mode.

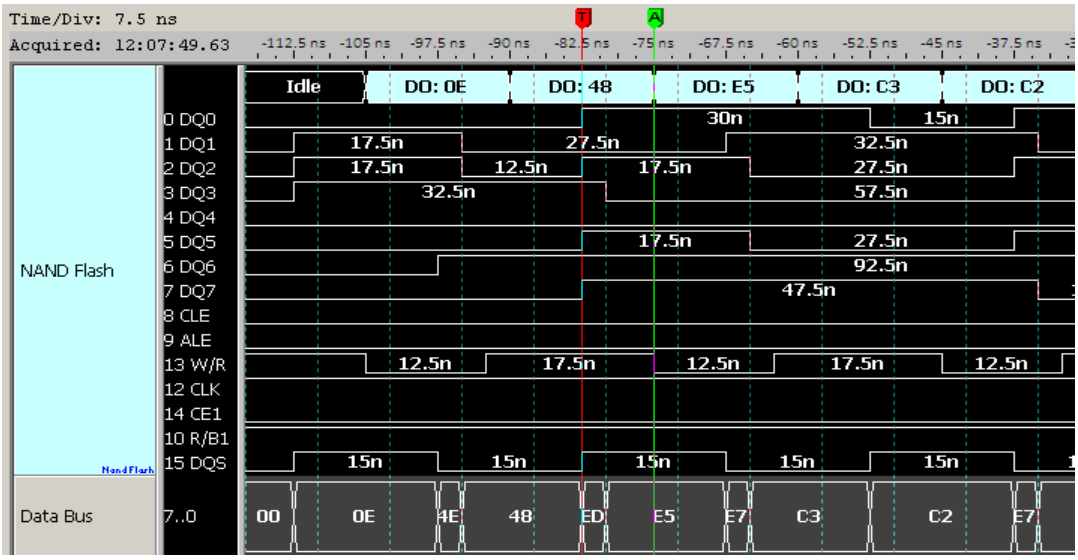
tREA / tDQSQ:



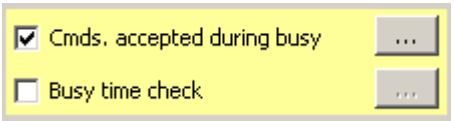
NAND will access data from the edge delay a period. This period call tREA under SDR mode and tDQSQ under DDR mode. The unit is 5 ns under 200 MHz sampling rate and 2.5 ns under 400MHz sampling rate of LA. The period between cursor T and cursor A is tREA.



The period between cursor T and cursor A is tDQSQ.

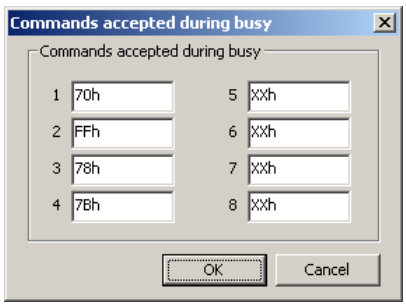


Commands accepted during busy / Busy time check:



The Command accepted during busy checked default, pressing  will show the

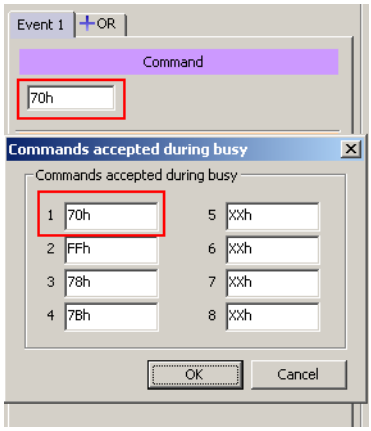
dialog below:

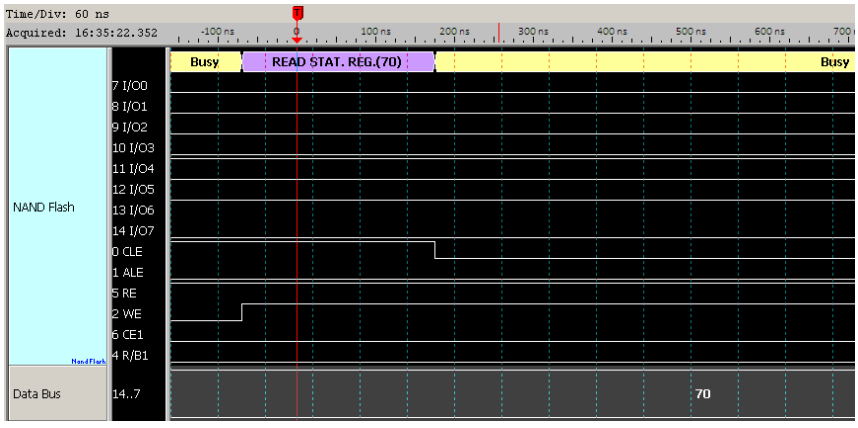


It means NAND commands still can be triggered while checking the Busy time check.

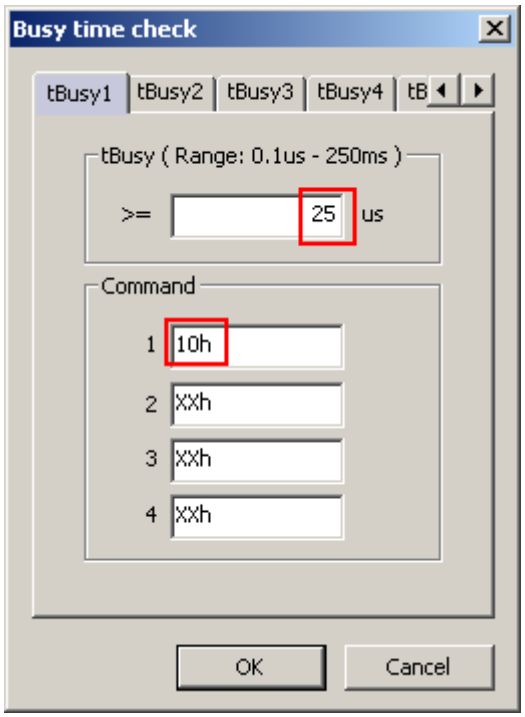
NAND command (70h/FFh/78h/7Bh) filled default.

Trigger Command 70h during busy time





Check the Busy time check function and pressing ... will show the dialog below:



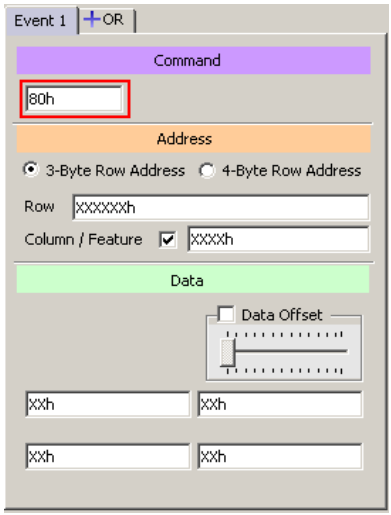
The Busy time check function provide 6 NAND Flash busy time to check and every busy time can be used by 4 commands. It will trigger when the busy time is more than or equal to the tBusy users filled.

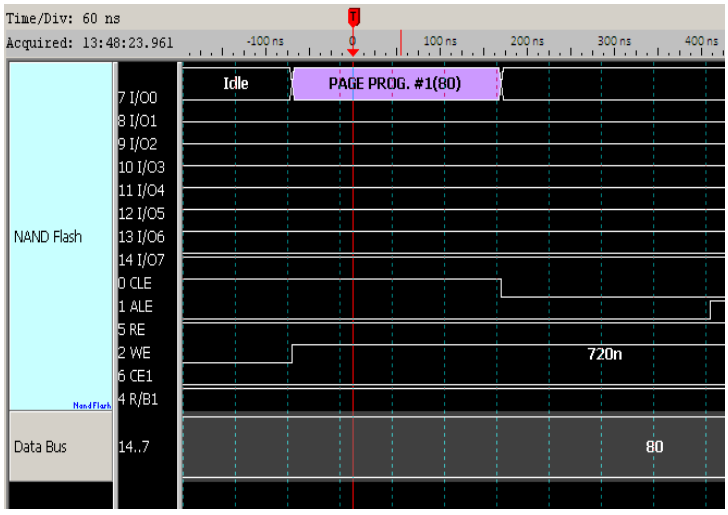
Trigger the busy time >= 25 us after NAND command 10h

State / Event: Trigger NAND Command / Address / Data

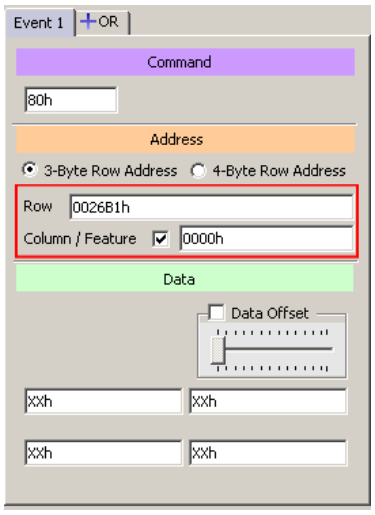
PAGE PROGRAM #1(80)	0026B1	0000	7B	9D	ED	8A	C3	E7	00	30
	0026B1	0008	26	A0	71	CD	BC	57	EA	25
	0026B1	0010	61	66	31	77	58	AC	39	56
	0026B1	0018	07	BE	9B	63	74	36	C5	B8
	0026B1	0020	4D	C5	68	F0	3B	84	58	14

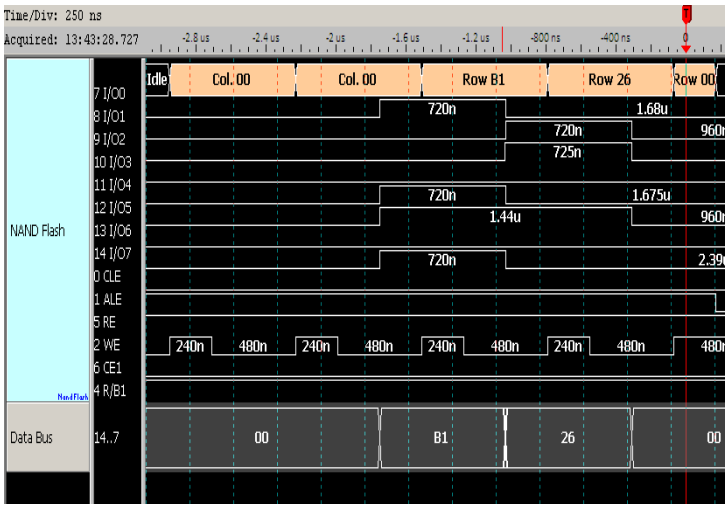
Trigger Command 80h



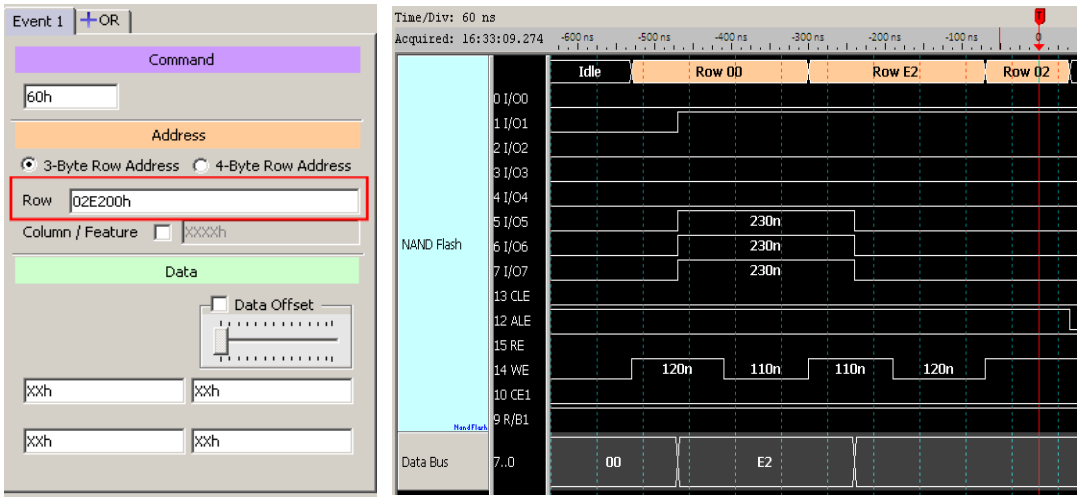


Trigger Row Address: 0026B1h, Column Address: 0000h

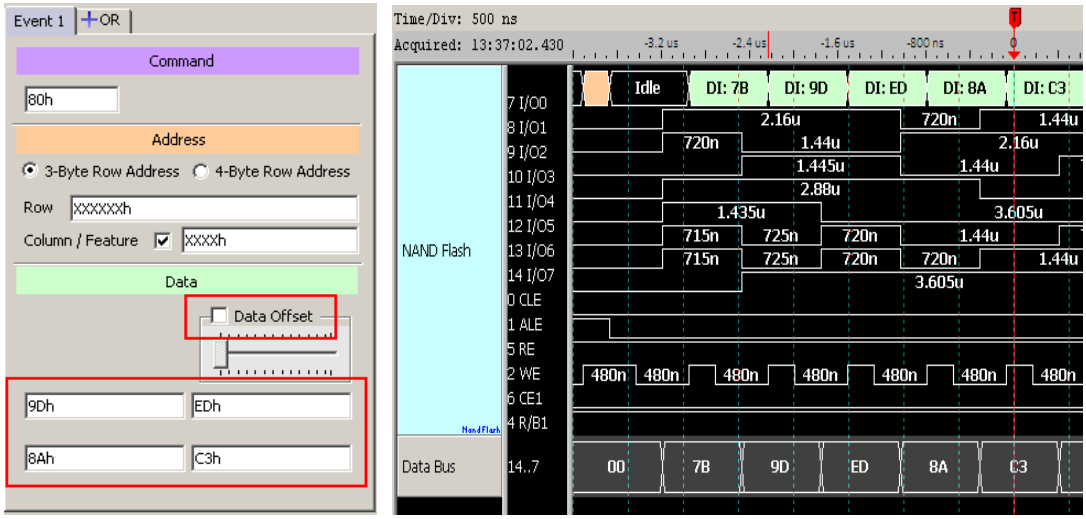




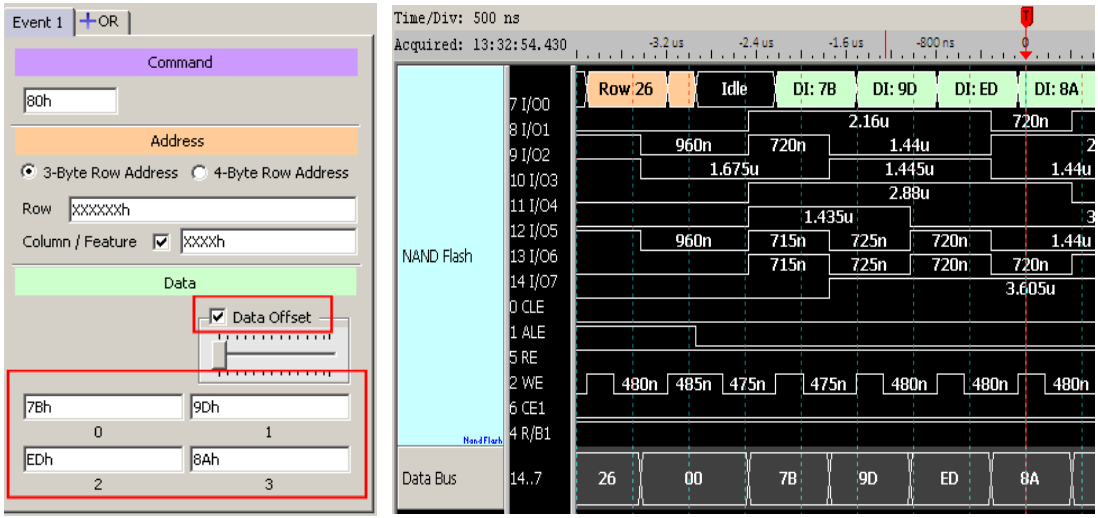
Trigger Row Address: 02E200h, no Column Address



Trigger the NAND Data

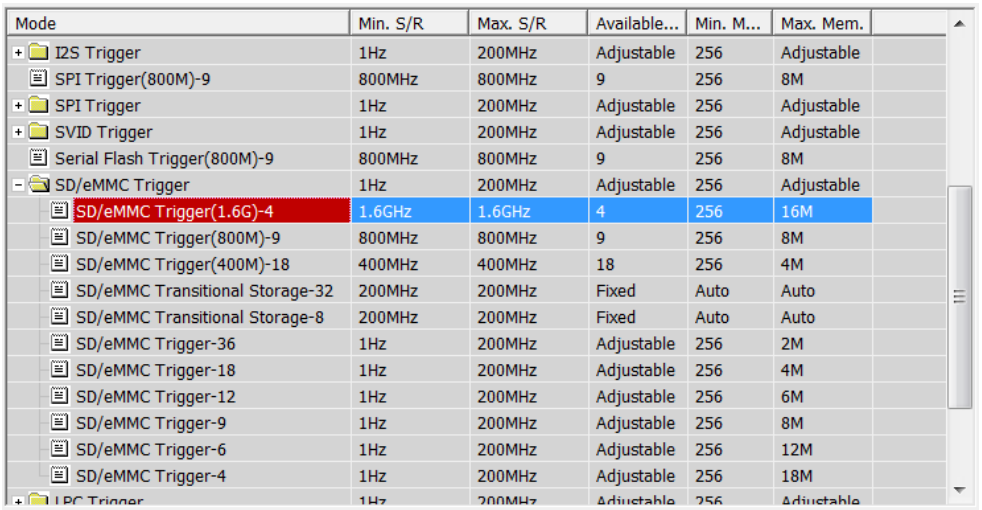


Trigger the NAND Data (fixed offset)



SD/eMMC Trigger

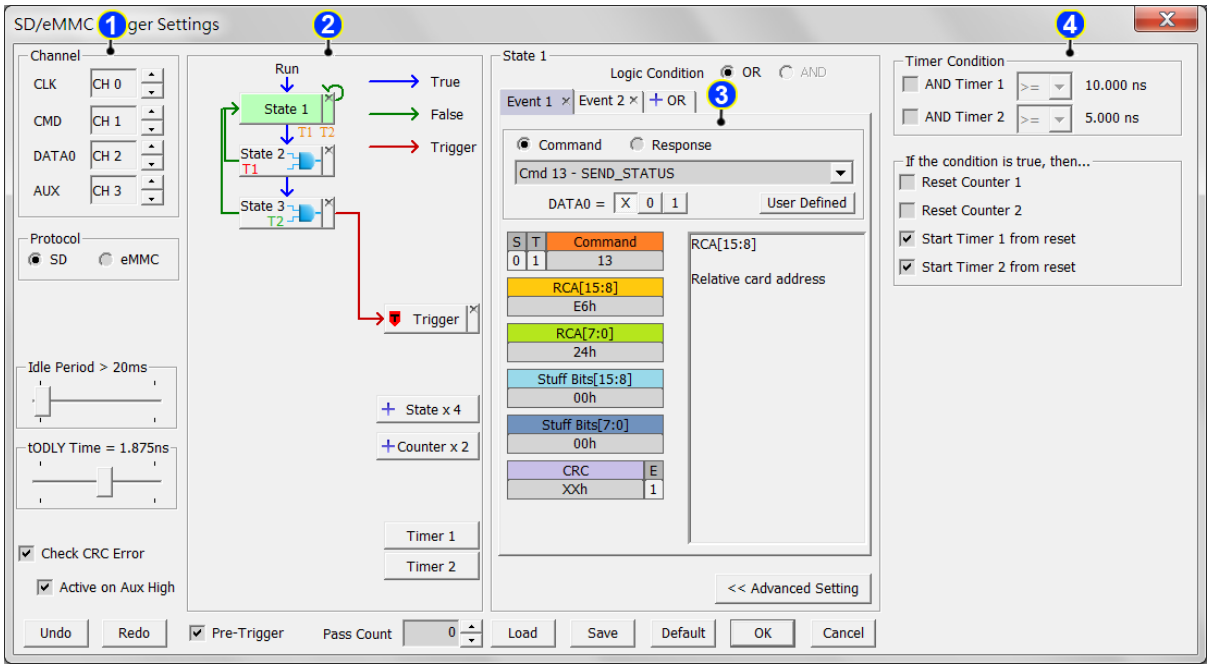
The settings dialog box below.



Mode	Min. S/R	Max. S/R	Available...	Min. M...	Max. Mem.
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M
SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SD/eMMC Trigger(1.6G)-4	1.6GHz	1.6GHz	4	256	16M
SD/eMMC Trigger(800M)-9	800MHz	800MHz	9	256	8M
SD/eMMC Trigger(400M)-18	400MHz	400MHz	18	256	4M
SD/eMMC Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
SD/eMMC Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
SD/eMMC Trigger-36	1Hz	200MHz	Adjustable	256	2M
SD/eMMC Trigger-18	1Hz	200MHz	Adjustable	256	4M
SD/eMMC Trigger-12	1Hz	200MHz	Adjustable	256	6M
SD/eMMC Trigger-9	1Hz	200MHz	Adjustable	256	8M
SD/eMMC Trigger-6	1Hz	200MHz	Adjustable	256	12M
SD/eMMC Trigger-4	1Hz	200MHz	Adjustable	256	18M
LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Settings

Select SD/eMMC Trigger Settings dialog box below.



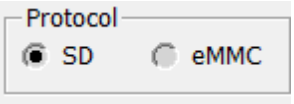
1. Channel

CLK: Clock signal.

CMD: Command signal.

Data0: eMMC only and judge response is R1 or R1b.

AUX: auxiliary CRC check.



select SD or eMMC trigger.

Idle Period:If clock keep idle and over the idle period value, then reset the state.

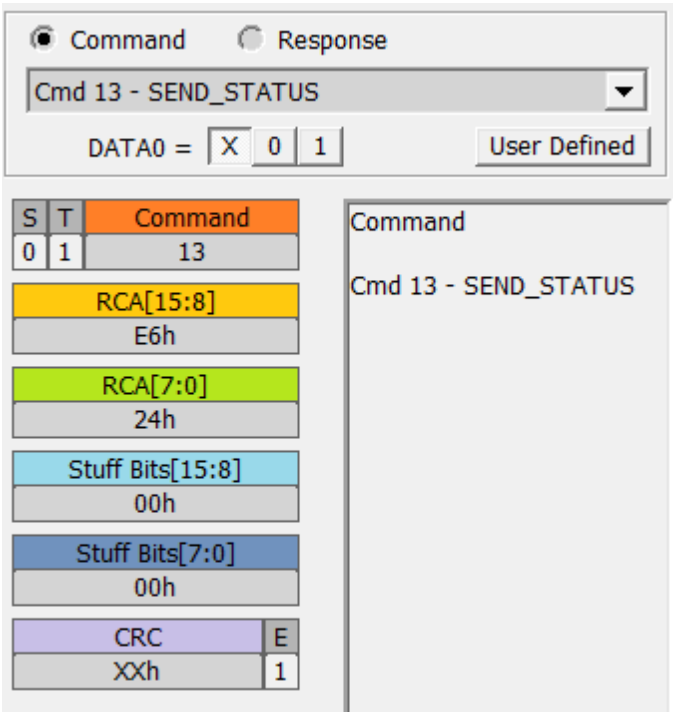
tODLY (Output delay) Time:When response, the delay time after clock edge is the valid command data.

Check CRC Error:Trigger the CRC error, if "Active on AUX High" is checked, the CRC check only when the AUX channel keeps high.

2. Clause trigger settings

Please reference Clause Trigger chapter

3. Trigger settings



Timestamp	Command	Response	Data	CRC7	Information
0.011239375 ms	CMD18:READ_MULTIPLE_BLOCK		0042 59C0h	6Ah	
0.011560625 ms		R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h	
0.413851875 ms	CMD12:STOP_TRANSMISSION		0000 0000h	30h	
0.414173125 ms		R1b:CMD12:STOP_TRANSMISSION	0000 0B00h	3Fh	
0.976969375 ms	CMD13:SEND_STATUS		E624 0000h	38h	
0.977285 ms		R1 :CMD13:SEND_STATUS	0000 0900h	1Fh	
0.98829625 ms	CMD18:READ_MULTIPLE_BLOCK		0042 5CC0h	4Dh	
0.9886175 ms		R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h	
1.330894375 ms	CMD12:STOP_TRANSMISSION		0000 0000h	30h	
1.331215625 ms		R1b:CMD12:STOP_TRANSMISSION	0000 0B00h	3Fh	
2.150086875 ms	CMD13:SEND_STATUS		E624 0000h	38h	
2.1504025 ms		R1 :CMD13:SEND_STATUS	0000 0900h	1Fh	
2.161419375 ms	CMD18:READ_MULTIPLE_BLOCK		0043 4000h	0Ah	
2.161740625 ms		R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h	

SD/eMMC decoder

Parameter：

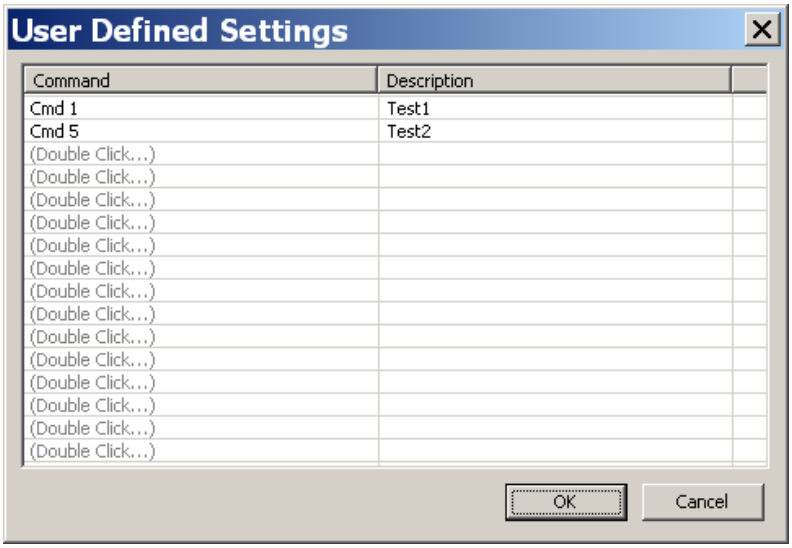
: use Data0 to judge the R1 and R1b.

Input trigger value, input ‘X’ means don’t care.

Append ‘h’ for HEX, ‘b’ for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

add the command reserved:



4. Timer and Counter

Please refer to the Clause Trigger

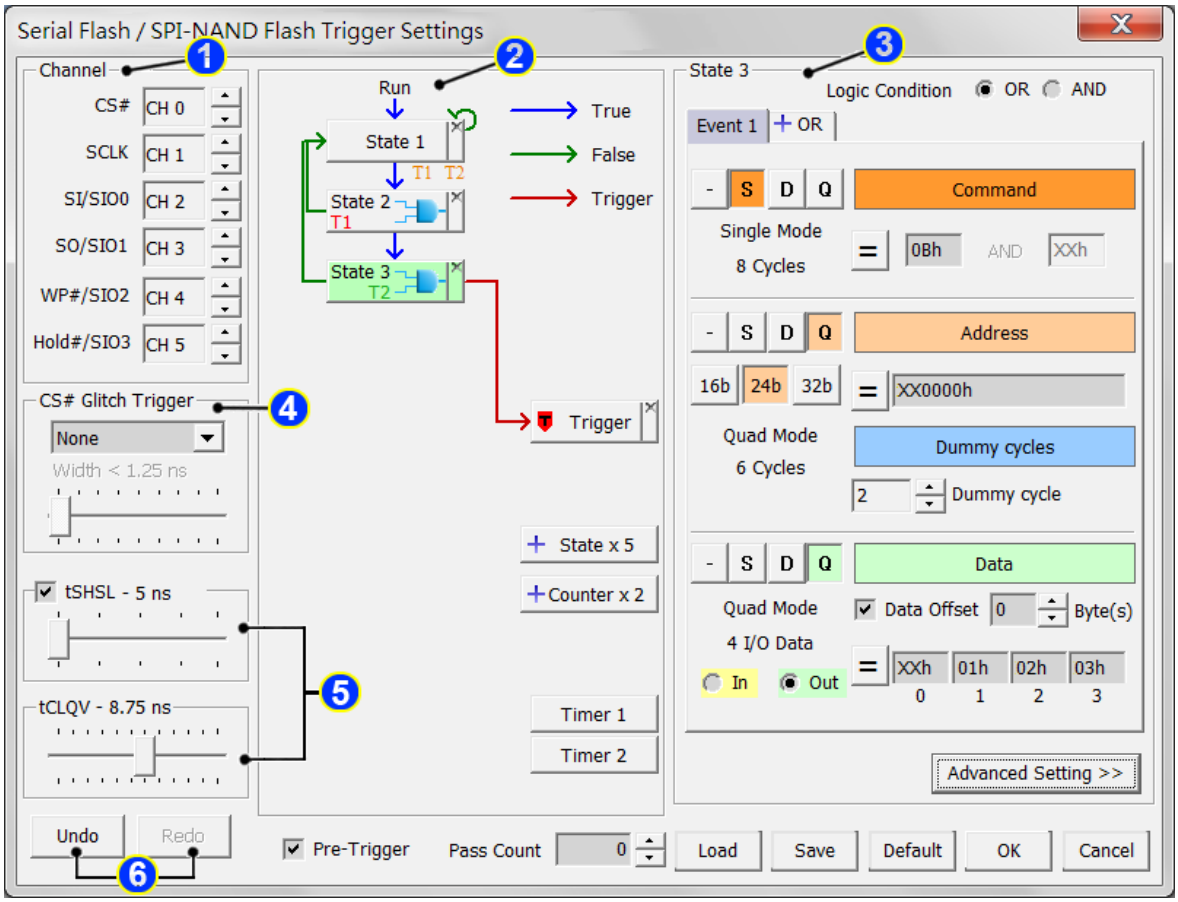
Serial Flash Trigger

The settings dialog box below.

Mode	Min. S/R	Max. S/R	Available...	Min. M...	Max. Mem.
800M	800MHz	800MHz	9	256	8M
400M	400MHz	400MHz	18	256	4M
200M	1Hz	200MHz	Adjustable	256	Adjustable
UART Trigger	Baud Rat...	Baud Rat...	Adjustable	256	Adjustable
CAN Trigger	Data Rate...	Data Rate...	Adjustable	256	Adjustable
I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M
SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
External Clock	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Settings

Select Serial Flash Trigger Settings dialog box below.



1. Channel:

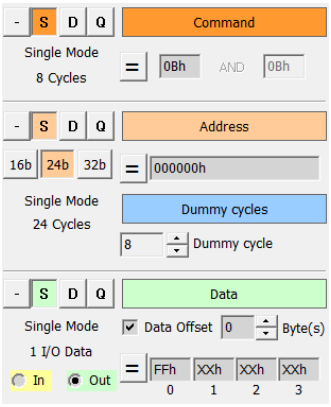
Select channels

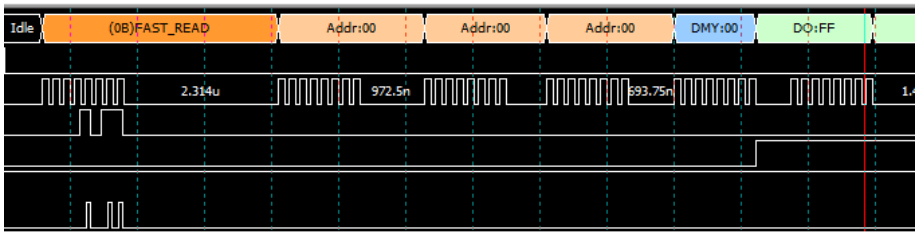
2. Clause trigger settings

Please reference Clause Trigger chapter

3. Trigger settings

The setting result will show in the trigger flow chart.





Select the mode of command:

- S D Q	- S D Q Single Mode 8 Cycles	- S D Q Dual Mode 4 Cycles	- S D Q Quad Mode 2 Cycles
Don't Care	Single Mode	Dual Mode	Quad Mode

Specified values in command, address and data fields, or input 'X' for don't care.

Check ☑ Data Offset to trigger on data at specified position.

EX: if Data Offset = 0, Data = FFh XXh XXh XXh. It will trigger on Data0= FFh and Data1, 2, 3=any data.

Dummy cycles is needed when data field is specified, it could be 0 to 8 clocks wide

depends on the waveform.

Click  button to switch NOT trigger  , it can have 2 input values when NOT trigger was selected.

4. CS Glitch Trigger

   Trigger when CS glitch (High/Low/Either) pulse. The glitch pulse setting can be from 0.625ns to 80ns.

5. tSHSL and tCLQV.

6. Redo/Undo

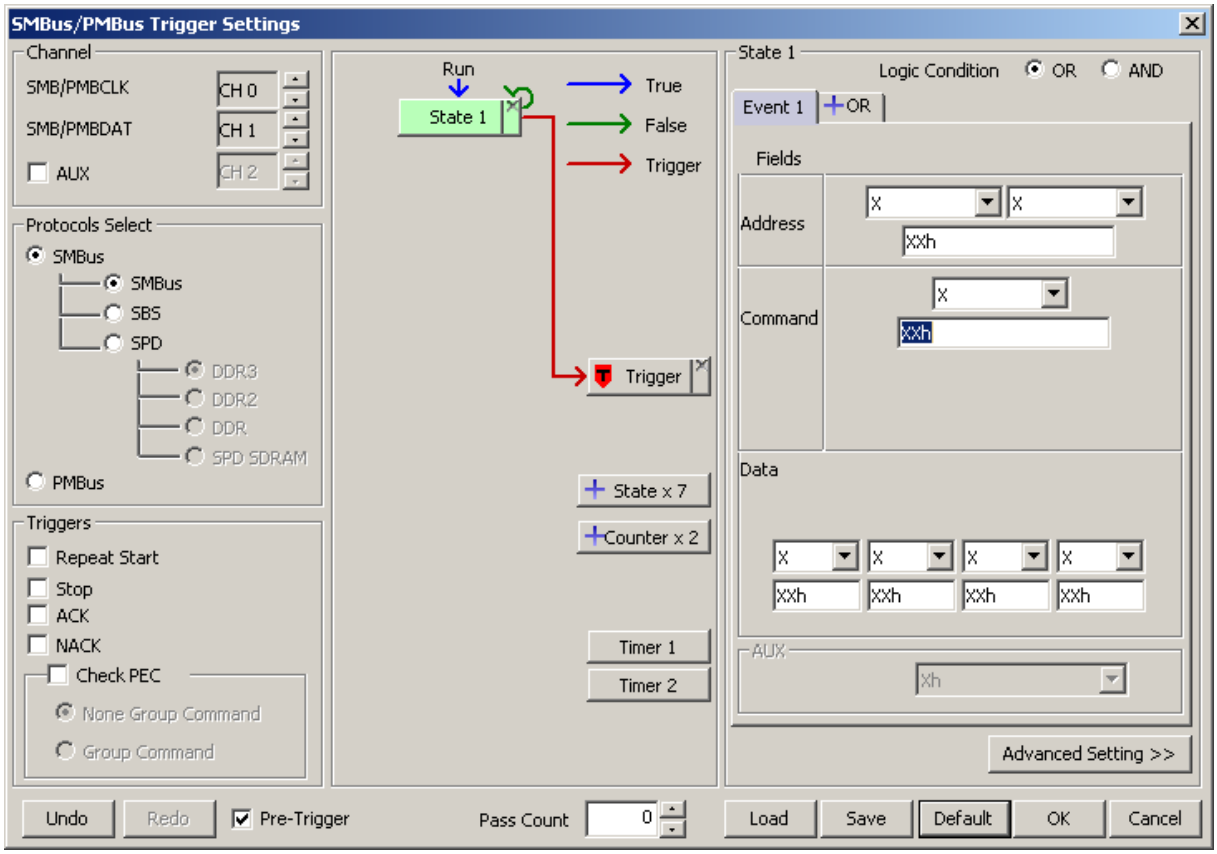
SMBus/PMBus Trigger

Select SMBus/PMBus Trigger Settings.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M
SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SMBus/PMBus Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
SMBus/PMBus Trigger-36	1Hz	200MHz	Adjustable	256	2M
SMBus/PMBus Trigger-18	1Hz	200MHz	Adjustable	256	4M
SMBus/PMBus Trigger-12	1Hz	200MHz	Adjustable	256	6M
SMBus/PMBus Trigger-9	1Hz	200MHz	Adjustable	256	8M
SMBus/PMBus Trigger-6	1Hz	200MHz	Adjustable	256	12M
SMBus/PMBus Trigger-4	1Hz	200MHz	Adjustable	256	18M
USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Settings

The SMBus/PMBus trigger settings dialog box is as below.



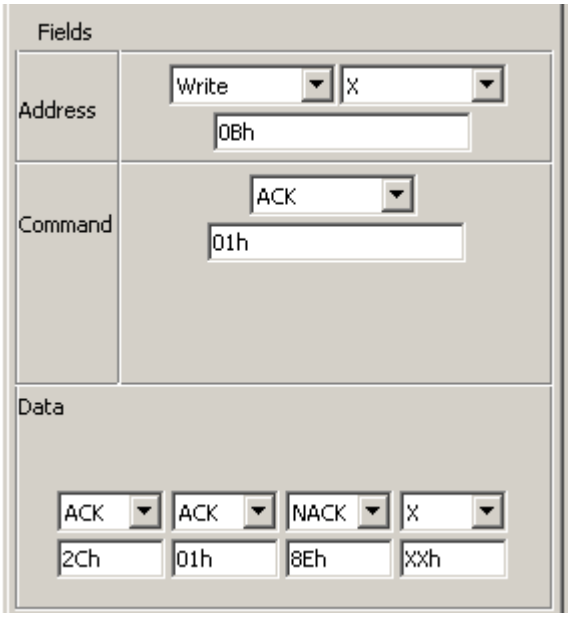
Channel: Select channels. AUX unchecked default.

Protocols Select: Select Protocols, it provides SMBus / PMBus trigger function.

Triggers: Provide the Repeat Start / Stop / ACK / NACK and Check PEC triggers.

Redo / Undo: Click these buttons to redo/restore previous setting.

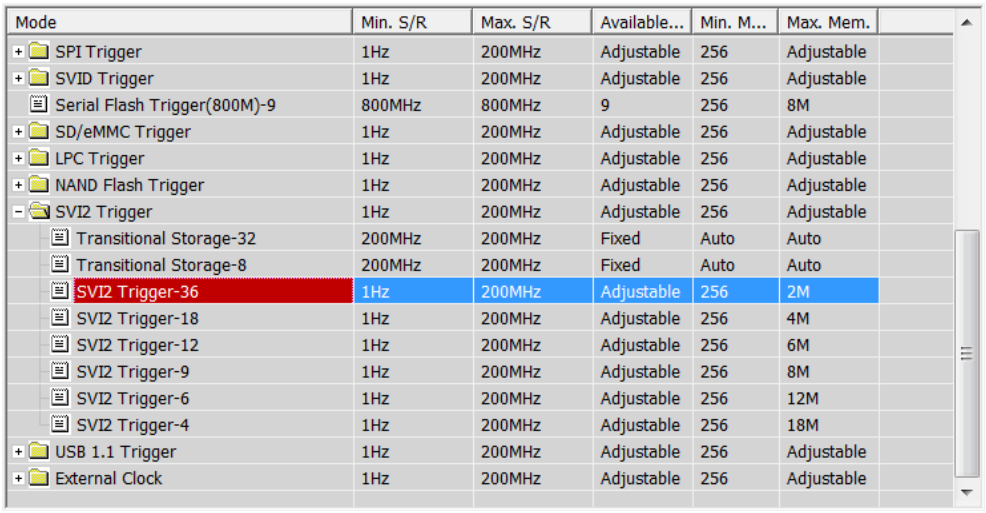
Trigger settings:



Provide the Wr/Rd Address / Command / Data and Acknowledge triggers.

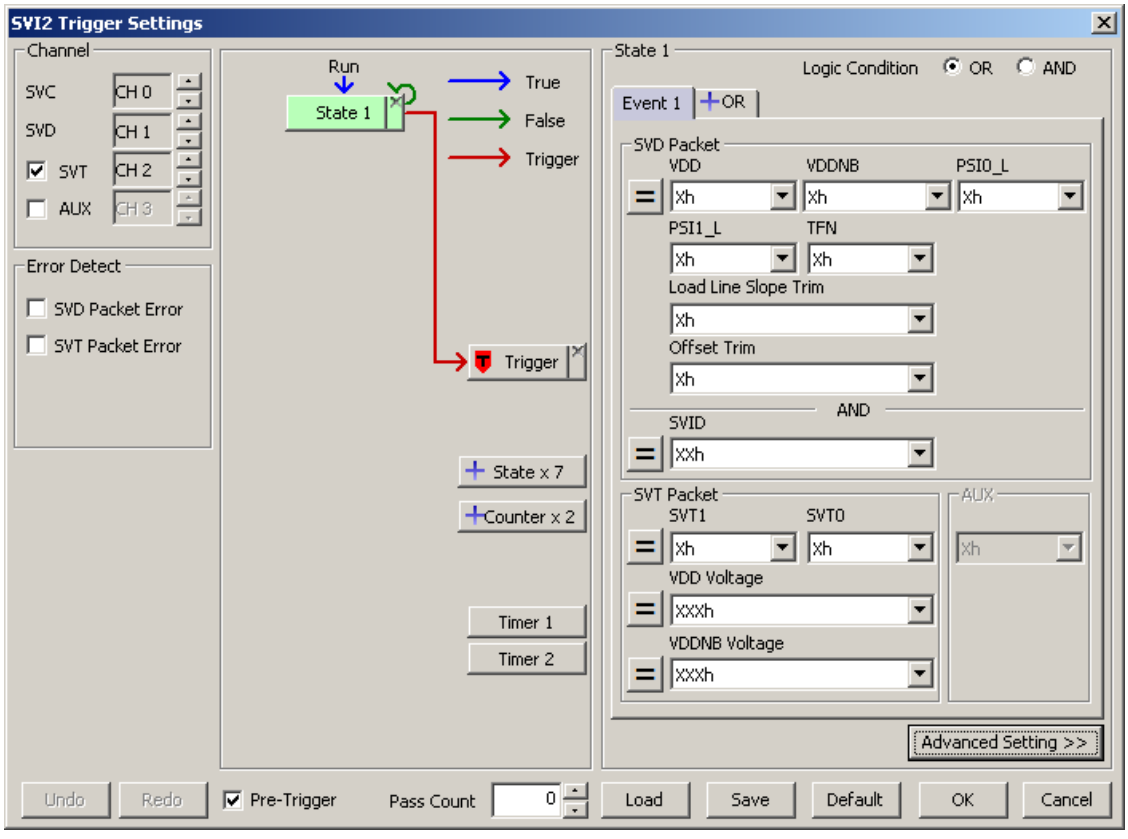
SVI2 Trigger

Select SVI2 Trigger Settings.



Trigger Settings

The SVI2 trigger settings dialog box is as below.



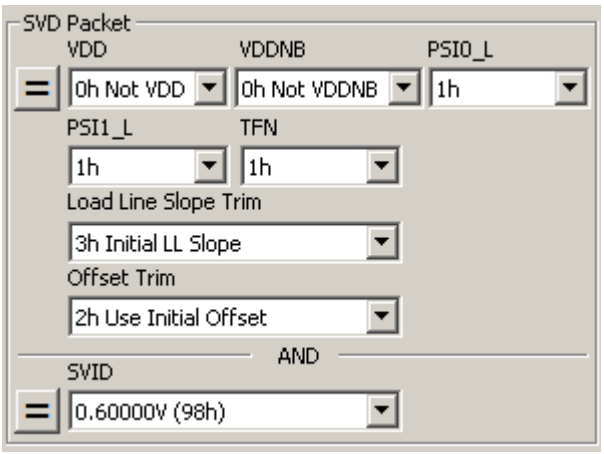
Channel: Select channels, SVT checked default.

Error Detect: Detect SVD / SVT packet error. It will check the size of packet.

Redo/Undo: Click these buttons to redo/restore previous setting.

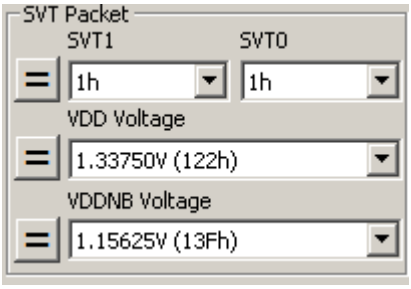
Trigger settings: Trigger SVD / SVT packet.

SVD Packet:



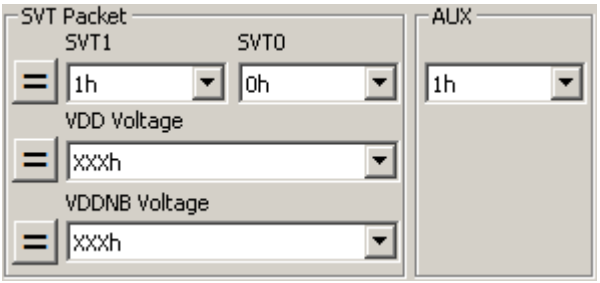
Timestamp	VDD	VDDNB	SVID Code	PSI	TFN	Slope Trim	Offset Trim	SVT	Volt	Volt/Current
-0.00144 ms	0	0	0.60000V (98)	3	1	Initial LL Slope(3)	Use Initial Offset(2)			
0.016945 ms	VDD(1)	0	1.30000V (28)	3	0	Initial LL Slope(3)	Use Initial Offset(2)			

SVT Packet:

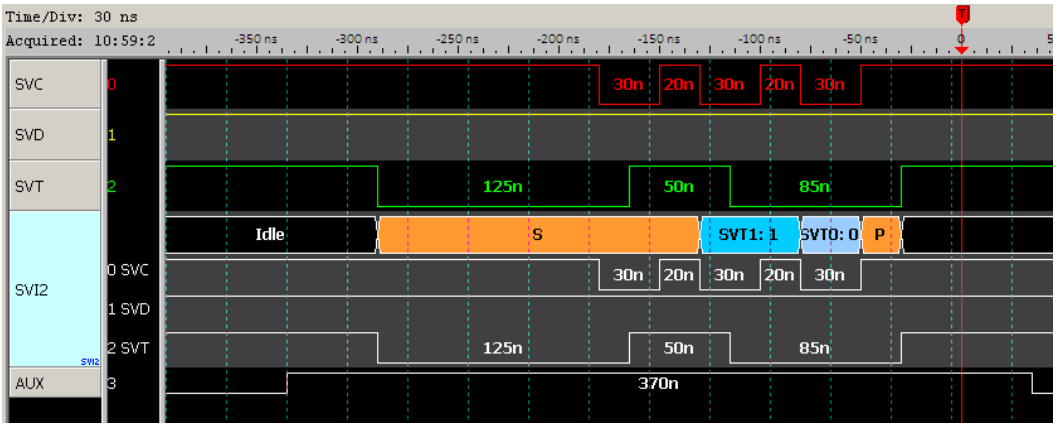


Timestamp	VDD	VDDNB	SVID Code	PSI	TFN	Slope Trim	Offset Trim	SVT	Volt	Volt/Current
-0.001175 ms								3	1.33750V (122)	1.15625V (13F)
0.018485 ms								3	1.16250V (13E)	1.15000V (140)
0.038145 ms								3	0.97500V (15C)	1.15000V (140)

VOTF Complete + AUX High



Timestamp	Offset Trim	SVT	Volt	Volt/Current	Error	Description
-0.014045 ms		3	0.97500V (15C)	1.15000V (140)		Voltage Only
-0.00029 ms		2				VOTF Complete
0.00561 ms		3	0.75625V (17F)	1.15000V (140)		Voltage Only



Other settings: Switch = / ≠ by clicking = button when trigger VDD, VDDNB…Offset Trim in SVD packet.

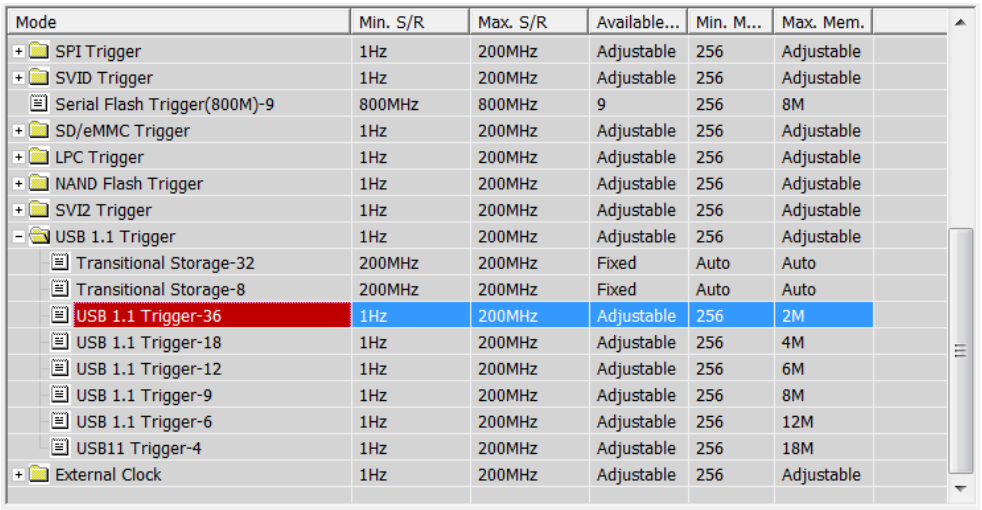
Switch = / ≠ / > / ≤ by clicking = button when trigger SVID in SVD packet.

Switch = / ≠ by clicking = button when trigger SVT1, SVT0 in SVT packet.

Switch = / ≠ / > / ≤ by clicking = button when trigger VDD Voltage / VDDNB Voltage in SVT packet.

USB1.1 Trigger

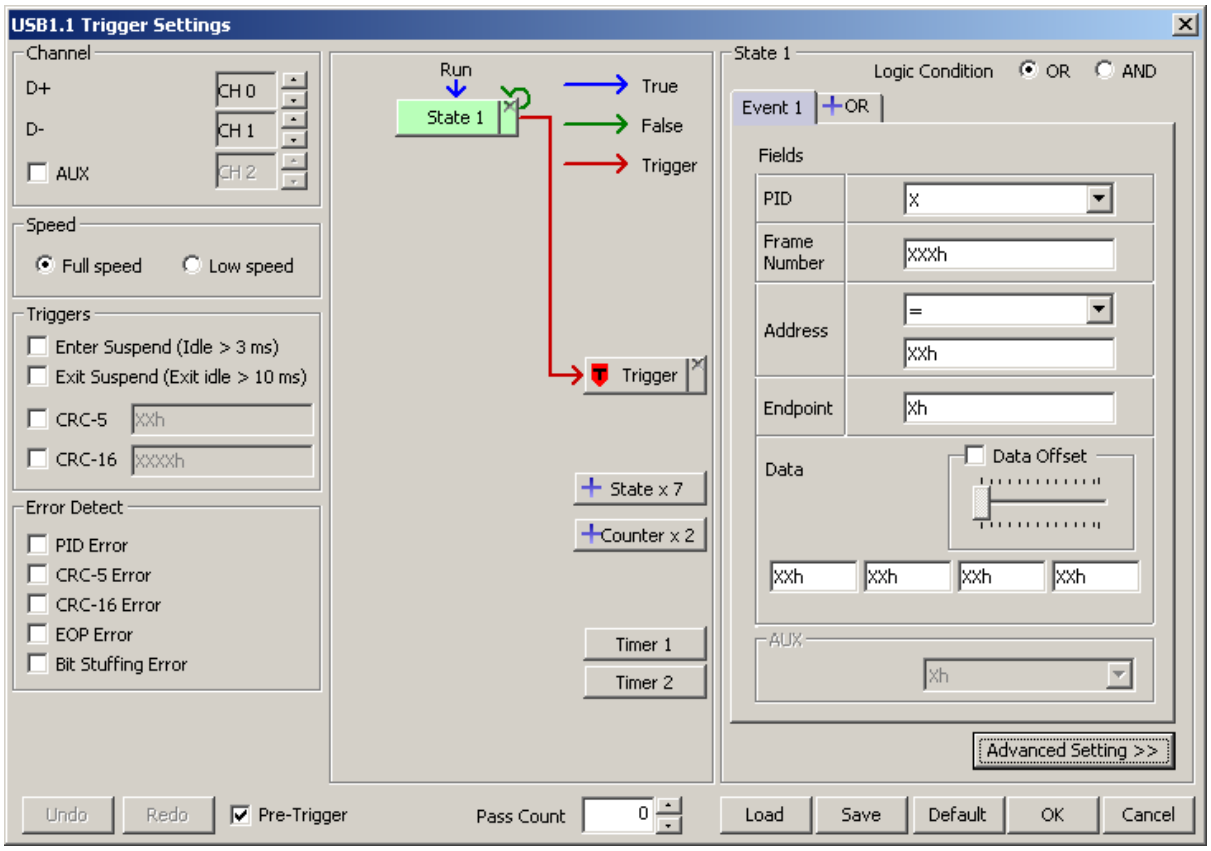
Select USB1.1 Trigger Settings.



Mode	Min. S/R	Max. S/R	Available...	Min. M...	Max. Mem.
SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M
SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable
NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
USB 1.1 Trigger-36	1Hz	200MHz	Adjustable	256	2M
USB 1.1 Trigger-18	1Hz	200MHz	Adjustable	256	4M
USB 1.1 Trigger-12	1Hz	200MHz	Adjustable	256	6M
USB 1.1 Trigger-9	1Hz	200MHz	Adjustable	256	8M
USB 1.1 Trigger-6	1Hz	200MHz	Adjustable	256	12M
USB11 Trigger-4	1Hz	200MHz	Adjustable	256	18M
External Clock	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Settings

The USB1.1 trigger settings dialog box is as below.



Channel: Select channels. AUX unchecked default.

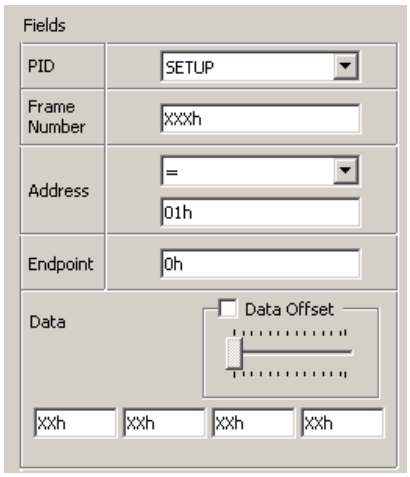
Speed: Speed mode. Select Full / Low speed.

Triggers: Trigger Enter Suspend / Exit Suspend / CRC-5 / CRC-16.

Error Detect: Trigger PID Error / CRC-5 Error / CRC-16 Error / EOP Error / Bit Stuffing Error.

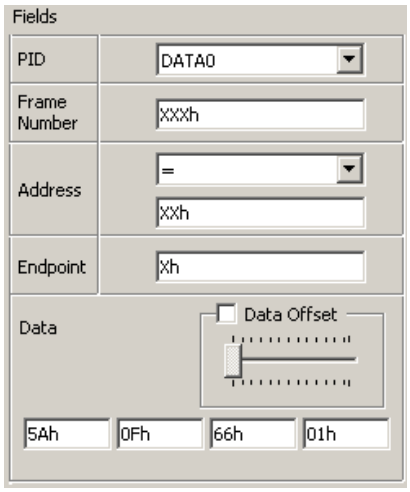
Redo/Undo: Click these buttons to redo/restore previous setting.

Trigger settings: Trigger PID:SETUP; Address = 01h; Endpoint = 0h



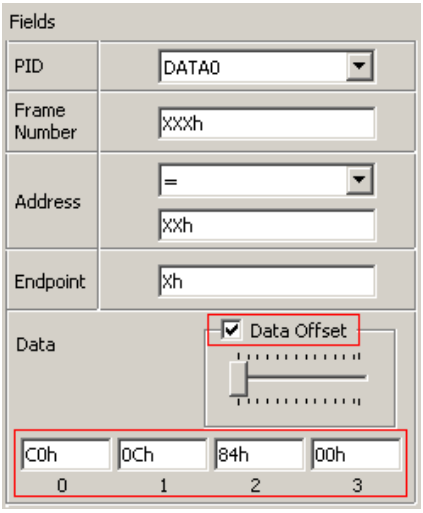
Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC5	DATA	ASCII	CRC16	Packet Duration
-0.00591 ms	357	SOF(TOKEN)	0288			01				3 us(33 Bits)
-0.002245 ms	358	SETUP(TOKEN)		01	00	17				3 us(33 Bits)
0.00142 ms	359	DATA0(DATA)					C0 0C 84 00 00 00 01 00	.....	060E	8 us(96 Bits)
0.010425 ms	360	ACK(HANDSHAKE)								1 us(17 Bits)
1.009085 ms	361	SOF(TOKEN)	0289			1E				3 us(33 Bits)
1.012755 ms	362	OUT(TOKEN)		01	02	03				3 us(33 Bits)
1.01642 ms	363	DATA0(DATA)					5A 0F 66 01	Z.f.	EC06	6 us(64 Bits)
1.022755 ms	364	ACK(HANDSHAKE)								1 us(17 Bits)

Trigger PID:DATA0; Data: 5Ah, 0Fh, 66h, 01h



Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC5	DATA	ASCII	CRC16	Packet Duration
-45.379 ms	1	SOF(TOKEN)	0289			1E				3 us(33 Bits)
-45.375335 ms	2	OUT(TOKEN)		01	02	03				3 us(33 Bits)
-45.371665 ms	3	DATA0(DATA)					5A 0F 66 01	Z.f.	EC06	5 us(64 Bits)
-45.365335 ms	4	ACK(HANDSHAKE)								2 us(17 Bits)
-45.362915 ms	5	SOF(TOKEN)	0288			01				3 us(33 Bits)
-45.35925 ms	6	SETUP(TOKEN)		01	00	17				3 us(33 Bits)
-45.355585 ms	7	DATA0(DATA)					C0 0C 84 00 00 00 01 00	.....	060E	8 us(96 Bits)
-45.346585 ms	8	ACK(HANDSHAKE)								2 us(17 Bits)

Trigger PID:DATA0; 4 Byte Data(Fixed offset): C0h, 0Ch, 84h, 00h



Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC5	DATA	ASCII	CRC16	Packet Duration
2.03475 ms	369	SOF(TOKEN)	0289			1E				3 us(33 Bits)
2.038415 ms	370	OUT(TOKEN)		01	02	03				3 us(33 Bits)
2.042085 ms	371	DATA0(DATA)					5A 0F 66 01	Z.f.	EC06	5 us(64 Bits)
2.04842 ms	372	ACK(HANDSHAKE)								1 us(17 Bits)
2.050835 ms	373	SOF(TOKEN)	0288			01				3 us(33 Bits)
2.054505 ms	374	SETUP(TOKEN)		01	00	17				3 us(33 Bits)
2.05817 ms	375	DATA0(DATA)					C0 0C 84 00 00 00 01 00	.....	060E	8 us(96 Bits)
2.06717 ms	376	ACK(HANDSHAKE)								1 us(17 Bits)

Other settings: Select =, <, >, <=, >=, InRange, Not InRange in the Address field.