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Chapter 1 Bus Decode



Add a Bus Decode:

Method 1:

Click the wizard in the menu, and select the bus decode.

😤 📴 🖶 💼 💼 🕐 👀 👀 🐥 🕰 🔎	₽₽₽₩₹₩	7 (7 (7 (7	🕄 😂 🐼 📼 🖿	📕 💯 🕕 🔗 S/R: 2	200 MHz
Time/Div: 125 ns 📕	A B	C	D G		
Acquired: 10:03:09.828	ns 430 ns	630 ns	830 ns 1.03 i	us 1.23 us	1.43 us
Label Ch. Value Activity Trigger					×
			400 ns 📕	500 ns 🔒	100 ns 🕒 🕕 🎁
Bus(Signal) Wizard			×		
Select a wizard					
HDMI-CEC	Create t	the I2C labe	el.		
DALI					
Line Decoding					
DMX512					
DP_AuxCh					
DDC(EDID)					
Line Encoding					
FlexRay					
HD Audio					
HDQ					
I2C					
I2C(EEPROM)					
125					
180					
IDE					
Indicator					
IrDA					
ITU656					
JTAG					
LCD1602					
LIN	▼				
₩ With color	OK		Cancel		

Method 2:

Click Add Bus Decode in the Label menu or right-click the label field to show the

dialog box.



Add Bus De	code 🔀	
Bus Name -		
	Enter a label name with 31 characters or less	
Color		
	Select the waveform color	
Parameter	<u> </u>	
3	Select a decode type and click the Advance button to set more parameters Display the waveforms with decode	
\sim	1-Wire Advance	5)
4	1-Wire 7-Segment CAN DALI DSO	
	FlexRay HD Audio HDMI-CEC HDQ I2C	

- 1. **Bus Name:** Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
- 2. **Color:** Set the waveform color.

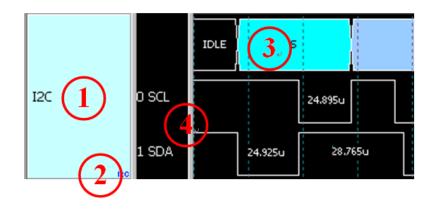
3. Display the waveforms with decode

- 4. Display the waveforms with its decode together.
- 5. Advance:



LIN SHEET	ngs 🔀
Channel —	
P	Sunai Canao Canao
	Overloummede P Depeix P Enhanced
	ih Damei 011 👘 🖉 Stevanie
	linal site (A.F.) . Ips
Color —	
	Vokeop
Range	Decode Range From Buffer Head To Buffer Tail
	Default OK Cancel

Set the decode parameters or press **OK** to use default settings. There are "Channel", "Color", "Range" settings



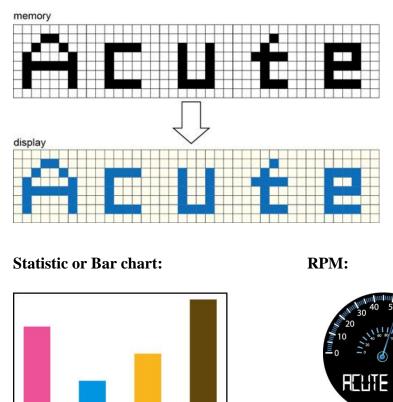


- 1. Bus name
- 2. Decode type
- 3. Result
- 4. Channel name & signal

Specially Bus Decode:

The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode...), image, analog waveform (ADC decode) etc.

In the future, we will extend the original form display to more applications like:

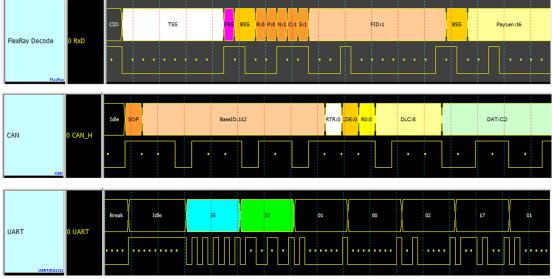


LCD/CMOS image sensor bus decodes:

The following original data form display for bus decodes are already available in the past.



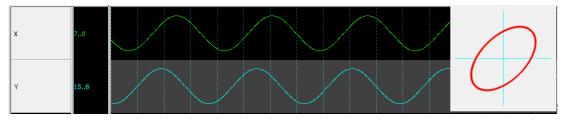
UART/CAN/FlexRay..bus decodes (released in 2009/9, LA Viewer Ver. 2.0):



The data is displayed according to bit points in order to calculate the bit number •

Lissajous analysis (released in 2009/09, LA Viewer Ver.2.0):

Display the signal in graph by X-Y or I-Q data. \circ





S/PDIF analysis (2010/11, LA Viewer Ver. 2.5):

Display the data in sound waveform $\,\circ\,$

S/PDIF(wave) 0 S/PDIF	Max: 6572 Min: -4496 Max: 5706 Min: -5766 HIIII HIII HIIII 00:00: 1:15.73 00:		30000 10000 -10000 30000 -10000 -30000 -30000 -30000 -30000 -30000 -30000 -30000 -30000 -30000
Setting Channel CH 0 CH 0	▼ Mb/s /s)	Block 192 (32 ~192) frames Bit Order Aux. Data LSB first Audio Data LSB first	Data Bits 16 ▼ Parity mode Even parity ▼ Playback

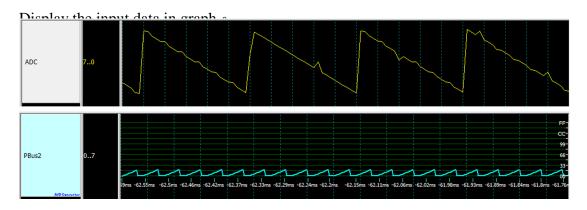
I2S analysis (2011/09, Ver. 2.6.3): 分析 (2011/09, LA Viewer Ver 2.6.3)

Display the data in sound waveform $\,\circ\,$

125 02 Max: 14157 Min: 17570 Min: 20934 Hittinitinitinitiniti	2000 3000 2000 2000 2000 2000 2000 2000
Channel	
Clock Channel (SCK)	CH 0 •
Word Select Channel (WS)	CH 1 -
Data Channel (SD)	CH 2
Data bits	16 Bits
Display the audio waveform	V Playback
Mode	Report
I2S Justified Mode 💌	8 Column 💌

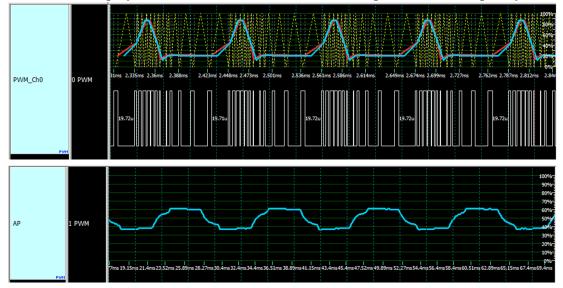


ADC bus decode (2012/08, LA Viewer Ver. 2.7.3):



PWM analysis (2012/08, LA Viewer Ver. 2.7.3):

Restore and display the data in the waveform window as percentile or frequency °





1-Wire

The 1-Wire bus has data bits (Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, Read 0) in standard or overdrive speed as the diagram below.

Settings

1-Wire	Settings X
Channel -	
1	Communication Speed Standard Bit Order LSB First
	Sampling Point
	35 us ↓
	Setting the channel of 1-wire in LA CH 0
Color —	
	Set color of data
U	Reset Pulse
	Presence Pulse
	Data
Range —	
inni	Decode Range
	From Buffer Head 🗨
	To Buffer Tail
	Default OK Cancel

Communication Speed: Standard or overdrive.

Bit Order: LSB first or MSB first.

Sampling point: Set the sampling point N microseconds (us) after the beginning of each data bit.

Result

Click OK to run the 1-Wire decode and see the result on the Waveform Window



ime/Div: 640 us cquired: 08:00:	· · · · · · · · · · · · · · · · · · ·	67 ms 54.691 ms	55.715 ms 56.739 ms	57.763 ms	58.787 ms 59.811	ms 60.835 ms
1-Wire 0 1-Wi	Idle	Réset Pulse Presen	ce Pulse CC BE	A6	01	Idle
1-Wire	C	947.8u	817u			1.844m
Label Chanr	nel 💶					
			V Data	ASCIT		
Fimestamp	Reset	1-Wire(1-Wire) Presence	▼ Data	ASCII		
Fimestamp 0.0303 ms	Reset Unknown	Presence	Data			<u>ت</u>
Timestamp 0.0303 ms 2.3578 ms	Reset Unknown Reset Pulse	Presence Presence Pulse	Data CC BE A6 01	••••		
"imestamp 0.0303 ms 2.3578 ms 0.3575 ms	Reset Unknown Reset Pulse Reset Pulse	Presence Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44	 .D		-
Fimestamp 0.0303 ms 2.3578 ms 0.3575 ms 53.6916 ms	Reset Unknown Reset Pulse Reset Pulse Reset Pulse	Presence Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01	 .D		
Fimestamp -0.0303 ms 22.3578 ms 30.3575 ms 53.6916 ms 51.697 ms	Reset Unknown Reset Pulse Reset Pulse Reset Pulse Reset Pulse	Presence Presence Pulse Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01 CC 44	 .D .D		
Fimestamp -0.0303 ms 22.3578 ms 30.3575 ms 53.6916 ms 51.697 ms 35.0284 ms	Reset Unknown Reset Pulse Reset Pulse Reset Pulse Reset Pulse	Presence Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01	 .D		
Finestamp -0.0303 ms -2.3578 ms -0.3575 ms -3.6916 ms -1.697 ms -3.0284 ms -3.0326 ms	Reset Unknown Reset Pulse Reset Pulse Reset Pulse Reset Pulse Reset Pulse	Presence Presence Pulse Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01 CC 44	 .D .D .D		
CHAOL CHAOL	Reset Unknown Reset Pulse	Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01	 .D .D		
Timestamp -0.0303 ms -2.3578 ms 30.3575 ms -3.6916 ms -1.697 ms -35.0284 ms -30.0326 ms -1.6.3656 ms -24.3646 ms	Reset Unknown Reset Pulse	Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01			
Timestamp -0.0303 ms 22.3578 ms 30.3575 ms 53.6916 ms 51.697 ms 35.0284 ms 33.0326 ms 116.3656 ms	Reset Unknown Reset Pulse Reset Pulse	Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse Presence Pulse	Data CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01 CC 44 CC BE A6 01			



3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

3-Wire (HOLTEK)) Settings			×
Parameters Channel CS CH C WR CH 1 WR CH 1	× × ×		OPERATION ADDRESS COMMAND DATA	
DATA CH 2 Application C LED Driver IC C LCD Driver IC C EEPROM HT1620x HT93LC46 x8	_	Fr	START ecode Range rom suffer Head	To Buffer Tail
Latch Chip Select Edge C Active High Data Edge C Rising	 Active Low Falling 		Default	OK Cancel

Settings

Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

EEPROM: Select EEPROM application.

Active High: Select Active High.



Active Low: Select low chip select (CS).

Rising: Select Rising Data Edge.

Falling: Select Falling Data Edge.

Result

_					-
Time/Div: 2 us 👎					
Acquired: 13:17: ₁	3.33 us 6.53 us	9.73 us 12.93 us 16.13 us	19.33 us	22.53 us	25.73 us
2 CS 3-Wire	IDLE OPER.(WRITE): 5	ADDR: 00			DATA: 0
1 WR 0 DAT.	1.335u 1.34u 1.335u 1.34u 1.33 2.675u 2.675u	5u 1.34u 1.335u 1.34u 1.335u 1.34u 1.335u 1.34u	1.335u 1.34u 1.	335u 1.34u 1.335u	1.34u 1.335u 1.34u
3-Wire					
Label Chann	•				
CH-00 CH-00 CH-01 CH-00 CH-01 CH-00	3-Wire(3-Wire)	•			
Timestamp	Operation	Command	Address	Data	▲
0.000001335 \$	5(WRITE)		00	0	
0.000036115 %					
			01	0	
0.000046815 S			01	0	
0.000046815 S 0.00005752 S				-	
			02	0	
0.00005752 S			02	0	
0.00005752 S 0.000068225 S			02 03 04	0 0 3	
0.00005752 S 0.000068225 S 0.000078925 S			02 03 04 05	0 0 3 7	
0.00005752 S 0.000068225 S 0.000078925 S 0.00008963 S			02 03 04 05 06	0 0 3 7 0	
0.00005752 S 0.000068225 S 0.000078925 S 0.00008963 S 0.00010033 S			02 03 04 05 06 07	0 0 3 7 0 0	
0.00005752 \$ 0.000068225 \$ 0.000078925 \$ 0.00008963 \$ 0.00010033 \$ 0.000111035 \$			02 03 04 05 06 07 08	0 0 3 7 0 0 5 F	
0.00005752 \$ 0.000068225 \$ 0.000078925 \$ 0.00008963 \$ 0.00010033 \$ 0.000111035 \$ 0.00012174 \$			02 03 04 05 06 07 08 08	0 0 3 7 0 0 5 F B	
0.00005752 S 0.000068225 S 0.000078925 S 0.00008963 S 0.00010033 S 0.000111035 S 0.00012174 S 0.00013244 S			02 03 04 05 06 07 08 08 09 09	0 0 3 7 0 0 F B B F	
0.00005752 \$ 0.000068225 \$ 0.000078925 \$ 0.00008963 \$ 0.00010033 \$ 0.000111035 \$ 0.00012174 \$ 0.00012244 \$ 0.00013244 \$			02 03 04 05 06 07 08 09 09 0A 0B	0 0 3 7 0 0 7 0 0 5 F B F B B	
0.00005752 S 0.000068225 S 0.000078925 S 0.00010033 S 0.000111035 S 0.00012174 S 0.00012244 S 0.00013244 S 0.00013245 S		3.645 m	02 03 04 05 06 07 08 07 08 09 04 09 0A 00 00 00	0 0 3 7 0 0 7 0 0 5 F B F B B	



7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit	LED	А	В	С	D	E	F	G
0	F G B C C D DP	ON	ON	ON	ON	ON	ON	OFF
1	F G B E C D DP	OFF	ON	ON	OFF	OFF	OFF	OFF
2	F G B E C D DP	ON	ON	OFF	ON	ON	OFF	ON
3	F G B E C D DP	ON	ON	ON	ON	OFF	OFF	ON
4	F G B F C D DP	OFF	ON	ON	OFF	OFF	ON	ON
5		ON	OFF	ON	ON	OFF	ON	ON
6	F G B E C C D DP	ON	OFF	ON	ON	ON	ON	ON
7	F G B F C D DP	ON	ON	ON	OFF	OFF	OFF	OFF
8	F G B F C C D DP	ON						
9		ON	ON	ON	ON	OFF	ON	ON



Settings

7-Segmen	t Settings				×
Channel					
1				A	
A CH		E CH 4		F	7
в сн	11	F CH 5	— 	G	в
ССн		G СН 6	— <u>-</u>	Е	
РСН	13			ľ 🦲	,
• Co	mmon cathode	C Comm	on anode	D	DP
Color —					
Set	color of data				
				_	
Range —					
	ecode Range				
	rom		То		
	Buffer Head	-	Buffer Tail	-	
			fault	ок	Cancel
					Cancer

Channel: Show the selected channel (CH 0).

DP: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.



Result

Click **OK** to run the 7 Segment decode and see the result on the Waveform Window

below.

		2.	Unknown	3.	Jnknown)	4. Unknown	5.	Unknown	7.	(Unknown)	ь.	(Unknown)	C I
ΟA			300n	300n		900n	300n	300n	300n				
18			300n	300n	300n	300n	900n		300n			Î	
20				300n	300n	300n 300n	300n] 300n	300n] 300n [300n	300n	
7-segment		300n	300n	300n		900n			- 900n		300n	300n	
4 E		300n				2.7u	_				300n	300n	
5 F						300n 300n	300n		900n		300n	300n	
		300n		300n		300n 300n	300n		900n		300n		
60		300n 300n		300n [300n]					300n 300n		300n		
7-Segment 7 D)H	300n	300n	J 300n [300n	300n <u>300n</u>	300n	300n	_ 300n	300n	300n	300n	
⊙/∰ <u>CH-00</u> CH CH-01 CH	hannel	Bus 7-segmer	it(7-Segmer	nt 💌		-							_
⊙/∰ CH-00 CH CH-01 CH Timestamp		Bus 7-segmer	t(7-Segmer	nt 💌 D		E	F	G	;	DP		Value	_
CH-01 CH	nn [E 0	F			DP 1		Value	_
Timestamp	A	В	С	D					I				
CH-01 CH Timestamp -0.0072 ms	A 0	B 1	C 1	D 0		0	0	0		1		1.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms	A 0 1	B 1 1	C 1 0	D 0 1		0	0	0		1		1.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.006 ms	A 0 1 1 1	B 1 1 1 1	C 1 0 1	D 0 1 1		0 1 0	0 0 0 0 0	0		1 1 1		1. 2. 3.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.006 ms -0.0054 ms -0.0048 ms -0.0042 ms	A 0 1 1 0 1 1 1 1 1 1	B 1 1 1 1 1 0 1	C 1 0 1 1 1	D 0 1 1 0 1 1 0		0 1 0 0	0 0 1 1 0	0 1 1 1		1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.0064 ms -0.0054 ms -0.0048 ms -0.0048 ms -0.0048 ms -0.0036 ms -0.0036 ms		B 1 1 1 1 1 0 1 0 1 0	C 1 0 1 1 1 1 1 1 1 1 1 1	D 0 1 1 0 1 0 1 0 1		0 1 0 0 0 0 0 1	0 0 1 1 0 1			1 1 1 1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7. b.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.0054 ms -0.0054 ms -0.0042 ms -0.0042 ms -0.0036 ms -0.003 ms	A O I I O I I O I I O I O O O	B 1 1 1 1 1 0 1 0 0 0 0 0 0	C 1 0 1 1 1 1 1 1 1 1 1 1 1	D 0 1 1 0 1 0 1 1 0 1 1		0 1 0 0 0 0 1 1	0 0 1 1 0 1 1 1 1 1			1 1 1 1 1 1 1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7. b. C.	
CH-01 CH-01 CH Timestamp -0.0072 ns -0.0066 ms -0.0054 ms -0.0048 ns -0.0042 ms -0.0036 ms -0.003 ms -0.0034 ms	A O 1 1 O 1 1 O 1 0 1 0 0 0 O 0	B 1 1 1 1 0 0 0 0 1	C 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	D 0 1 1 0 1 0 1 1 1 1 1		0 1 0 0 0 1 1 1	0 0 1 1 0 1 1 1 0 1 0			1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7. b. C. d.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.0054 ms -0.0054 ms -0.0054 ms -0.0048 ms -0.0042 ms -0.0036 ms -0.003 ms -0.0034 ms -0.0034 ms	A 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 0 1 1 0 1	B 1 1 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0	C 1 0 1 1 1 1 1 1 1 1 1 1 1 1 0	D 0 1 1 0 1 0 1 1 1 1 1 1		0 1 0 0 0 1 1 1 1 1	0 0 1 1 0 1 1 0 1 0 1 1 0		· · · · · ·	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7. b. C. d. E.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.0054 ms -0.0054 ms -0.0054 ms -0.0048 ms -0.0036 ms -0.003 ms -0.0034 ms -0.003 ms -0.0034 ms -0.0034 ms -0.0034 ms	A 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 0 0 0 1 1	B 1 1 1 1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 0 0 0 0 0 0	C 1 0 1 1 1 1 1 1 1 0 0 0	D 0 1 0 1 1 0 1 1 1 1 1 0 0		0 1 0 0 0 1 1 1 1 1 1	0 0 1 1 1 0 1 1 0 1 1 1		· · · · · ·	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7. b. C. d. E. F.	
CH-01 CH Timestamp -0.0072 ms -0.0066 ms -0.0054 ms -0.0054 ms -0.0042 ms -0.0042 ms -0.0036 ms -0.003 ms	A 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 0 1 1 0 1	B 1 1 1 0 1 0 1 0 1 0 1 0 0 0 0 0 0 0 0	C 1 0 1 1 1 1 1 1 1 1 1 1 1 1 0	D 0 1 1 0 1 0 1 1 1 1 1 1		0 1 0 0 0 1 1 1 1 1	0 0 1 1 0 1 1 0 1 0 1 1 0		· · · · ·	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1. 2. 3. 4. 5. 7. b. C. d. E.	



A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

Settings

A/D Converter Settings	×
A/D Converter Settings Parameters Channel Data Channel Data Channel Channel Start From CH 2 CH 1 CH 1 Data Data MSB First Chip Select Edge Chative High Active Low Data Edge Chising Falling	Color DATA Range Pecode Range From To Buffer Head I Buffer Tail I
Draw Color Curve: Time(X)-Data(Y) Color Use the maximum and minimum as the bound of Y axis Insert Y axis bound(Save it in the LA work directory) Top(Decimal) 255 Bottom(Decimal)	Default Cancel

Data Channel Start From: ADC data channel start from

CLK Channel: ADC clock in channel

CS(OE) Channel: ADC chip select (output enable) channel

Data Width: ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted

2's Complement: Show the 2's complement result.

Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

Curve: Time(X)-Data(Y) Show the diagram in form of time as X axis; data as Y



axis.

Color: Select the curve color

Use the maximum and minimum as the bound of Y axis: Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis.

Insert Y axis bound: Set the maximum and minimum bounds of Y axis.

Note: When Insert Y axis boundaries is actived (Save it in the LA file directory), the Top and Bottom values will always be saved as an independent text file named as ADC.txt, different from the waveform file, at file work directory unless a different name is assigned. If you need the specific boundary settings, please save it, so you can reload the settings next time.

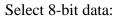
Result

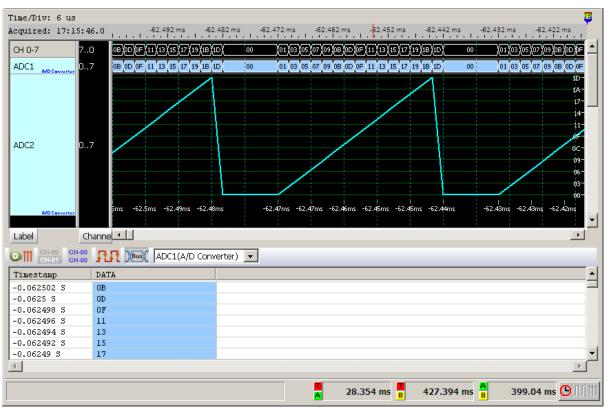
Click **OK** to run the A/D Converter decode and see the result on the Waveform Window below.



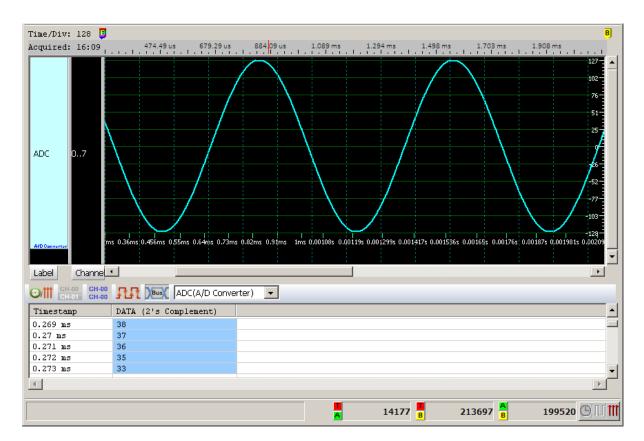
Time/Div: 15.36	· · · · · · · · · · · · · · · · · · ·				B
Acquired: 13:03	26.0 399.53 US		.33 us 501.93 us	527.53 us 553.13	us 578.73 us
CH-00					
CH-01	17u	62,99u	17u	62.99w	17u
СН 2-9	02 WWWWW 00 Y	$\dot{\mathbf{w}}$	X 00 XXXXXXXXXXXX	www.www.www.	00 YYYYYYYY
		NAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA	//////////////////////////////////		
ADC1 A/D Converter)9 131517191810 IDLE 00	01 03 05 07 09 18 10 1F 11 13 15 17 19 18	1D IDLE 00 01 03 05 07 0	9 (B)D0F 11 13 15 17 19 18 10	DLE 00 01 03 05 07
A/D Convertor	09 fms 0.3899ms 0.4139m Chann	s 0.4299ms 0.4459ms 0.4619ms	0.4939ms 0.5099ms	: 0.5259ms 0.5419ms	0.5739ms 0.5899ms
CH-00 CH-0	ADC1(A/D C	onverter) 💌			
Timestamp	DATA				•
0.36995 ms	11				
0.37395 ms	13				
0.37795 ms	15				
0.38194 ms	17				
0.38594 ms	19				
0.38994 ms	1B				
0.39394 ms	1D				-
4					Þ
			141.77 us 📕	2.137 ms 🔒	1.995 ms 🕒 🛄 🎁

Select 8-bit data, CLK/CS channels:









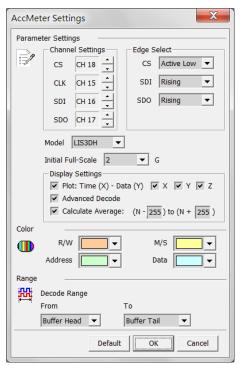
Select 8-bit data, 2's complement



AcceleroMeter

AcceleroMeter (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

Settings



CS: Chip Select, must specified the active state of the CS pin.

CLK: Clock

SDI: Data Input Pin, must specified the data sampling edge.

SDO: Data Output Pin, must specified the data sampling edge.

Model: The IC model of the target accelerometer.

Initial Full-Scale: The default Full-Scale setting.

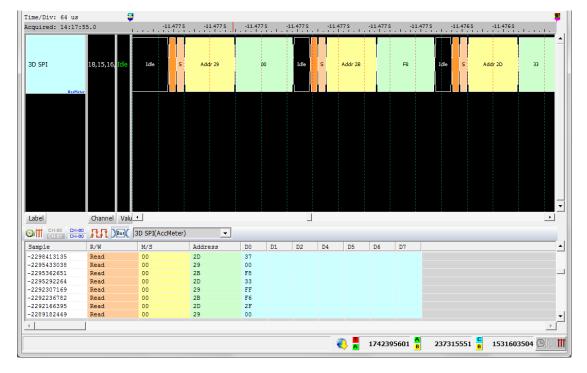
Plot: Enable/Disable to display the waveform in Time-Value curve.

Advanced Decode: Enable/Disable the address, value convert function.



Result

Standard decoder result



Advanced decode result + Time-Value curve display

cquired: 14:17:5	5.0		-16.636 \$ -1 <mark>4.958 \$</mark>	-13.281 S	-11.603 S	-9.925 S	-8.24	3S -6.	57S -	4.892 S	-3.214 S
3D SPI	18,15,16	, Idle	× z z 								200- 160- 130- 0.40- -0,40- -0,40- -0,40- -120- -120- -120- -200- 3415ms -2572ms -1744ms
Label	Channe										•
3/111 CH-00 CH-00	A A	Bus	3D SPI(AccMeter)								
Sample	R/W	M/S	Address	Data	Acc. X	Acc. Y	Acc. Z	Avr. X	Avr. Y	Avr. Z	
-3220320060	Read	00	OUTX_H(29)	03	0.047G			0.055G			
-3220320000	Read	00	OUTY_H(2B)	F9		-0.109G			-0.109G		
-3220249673	Read	00	OUTZ_H(2D)	3F			0.984G			0.993G	
-3220249673 -3220179286			OUTX_H(29)	04	0.063G			0.058G			
-3220249673 -3220179286 -3217215386	Read	00		F9		-0.109G			-0.109G		
-3220249673 -3220179286 -3217215386 -3217144999	Read	00	OUTY_H(2B)				1.000G			0,990G	
-3220320060 -3220249673 -3220179286 -3217215386 -3217144999 -3217074612			OUTZ_H(2D)	40			1.000G			0.9906	
-3220249673 -3220179286 -3217215386 -3217144999	Read	00	OUTZ_H(2D) OUTX_H(29)		0.063G		1.000G	0.063G		0.9906	
-3220249673 -3220179286 -3217215386 -3217144999 -3217074612	Read Read	00 00	OUTZ_H(2D)	40	0.063G	-0.109G	1.000G	0.063G	-0.109G	0.9906	
-3220249673 -3220179286 -3217215386 -3217144999 -3217074612 -3214087317	Read Read Read	00 00 00	OUTZ_H(2D) OUTX_H(29)	40 04	0.063G	-0.109G	1.0006	0.063G	-0.109G	0.9906	,



AD-Mux Flash

AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

Settings

AD I	Mux Flash Setting	×
Channel Amax A22 ADQ[0](LSB) CH 7 C Quick Setup ADQ[15:0] => CH[22:7] C User Defined A[22:16] => CH[29:23] Flash CE#f CH 24 AVD# CH 23 OE# CH 29 CLK CH 26 CH	Configuration Wait State Burst Length 9th 9th 16-Word Linear Burst RDY Polarity Burst Wrap Around with data Yes Color Range	•
WE# OH 33 A RDYf/WAITP OH 30 A PSRAM V has PSRAM LB#p OH 28 A CE#p OH 25 UB#p OH 32 A CE#p OH 25 A UB#p OH 32 A CH 30 A CH	Address Burst Address Burst Address Write Data Default Default	▼ ▼ Cancel

Amax: Setting the number of address pin.

Quick Setup/User Defined: Only set ADQ[0](LSB) when select the Quick Setup,

other channels will be set automatically. When check User Defined and press the

button will show the dialog below:

			Address /	′ Data Bเ	s	×
ADQ[0]	СН 7 📩	ADQ[8]	CH 21 ·	A[16]	CH 0 A[24]	сно –
ADQ[1]	СН 8 -	ADQ[9]	CH 22 -	A[17]	CH 1 -	
ADQ[2]	CH 15 ·	ADQ[10]	СН 9 📩	A[18]		
ADQ[3]	CH 16 ·	ADQ[11]	CH 10 -	A[19]		
ADQ[4]	CH 17 ·	ADQ[12]	CH 11 ·	A[20]		
ADQ[5]	CH 18 ·	ADQ[13]	CH 12 -	A[21]		
ADQ[6]	CH 19 ·	ADQ[14]	CH 13 ·	A[22]	СН 6	
ADQ[7]	CH 20 ·	ADQ[15]	CH 14 ·	A[23]		
					OK	Cancel



Flash: Control pins of flash.

PSRAM: Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when "has PSRAM" is checked. **Configuration:** The default setting of configuration register. User must set here to make a correct analysis.

Result

Click OK to run the AD-Mux Flash Decode and see result on the Waveform Windows below.

-	0.00:00			162.435 us	162.4	41 us	1. 16	2.447 us		162.45	us I I I	162.	459 us	1	62.465 u	15 I.I	162.4	71 us	16	2.477 us	162.48
Address/Dat	a <mark>6,5</mark> 004	200 00403600003	4						000000								þ 24	370		03487	
AVD#	23 1																		12	ns	
Œ#f	24 1																				
Έ#p	25 1																				
lk	26 0		6 m	s 4 ns		6 ns		6	i ns		ns	6	i ns				16 ns				4 ns 6 ns
REp	27 0																				
B#p	28 1									_	_		20 ns		_	_					
)F#	29 1																				
RDYf/WAIT													-								
ESET#f	31 1																				
	- 31																				
JB#p	32 1		_		_		_		_				20 ns								
VE#	33 1																				
D-Mux Flas	h 24,	5	PB_W:0000		PB_W	:0000						1	dle					_1	Idle	FE	A:034870 Ide
.abel	Cha Va	lue																			
																					ł
CH-00	CH-00	R II 🔊	🕺 AD-Mux	k Flash(AD-Mux	F																
	Device	Description			DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	ASCII
.16224	PSRAM		024B30	Sync.Write	0140	0132	0000	0000	803D	8036	8044	8036	0000	0000	403D	4036	4044	4036	0000	0000	0.2=.
.16247	Flash		034B70	Sync.Read	0000	0000	013D	0136	0144	0136	0000	0000	803E	8037	8044	8037	0000	0000	403E	4037	=.6.D.
.16276	PSRAM		024B40	Sync.Write	203D	2036	2044	2036	0000	0000	103D	1036	1044	1036	0000	0000	083D	0836	0844	0836	= 6 D 6
0.16299			034B80	Sync.Read	4044	4037	0000	0000	203E	2037	2044	2037	0000	0000	103E	1037	1044	1037	0000	0000	D070>
0.16329			024B50	Sync.Write	0000	0000	043D	0436	0444	0436	0000	0000	023D	0236	0244	0236	0000	0000	013D	0136	=.6.D.
0.16351			034B90	Sync.Read	083E	0837	0844	0837	0000	0000	043E	0437	0444	0437	0000	0000	023E	0237	0244	0237	>.7.D.7
.16381	PSRAM		024B60	Sync.Write	0144	0136	0000	0000	803E	8037	8044	8037	0000	0000	403E	4037	4044	4037	0000	0000	D.6>.
0.16404	Flash		034BA0	Sync.Read	0000	0000	013E	0137	0144	0137	0000	0000	013B	0134	0142	0134	0000	0000	023B	0234	>.7.D.
0.10404	PSRAM		024B70	Sync.Write	203E	2037	2044	2037	0000	0000	103E	1037	1044	1037	0000	0000	083E	0837	0844	0837	> 7 D 7
0.16433			034BB0	Sync.Read	0242	0234	0000	0000	043B	0434	0442	0434	0000	0000	083B	0834	0842	0834	0000	0000	B.4;.
	Flash																				
.16433	Flash																				[]



Advanced Platform Management Link (APML)

APML protocol is established by AMD for it's Opteron CPU platform.

Settings	
APML Settings	×
Parameter Channel SCL CH 0 SDA CH 1 Address Address 7-bit addressing (Include R/W in Address) PEC J Ignore glitch	Color Set the field's color in packet Command Address Write / Read Start / Stop / Sr Start / Stop / Sr ACK / NACK PEC / Byte Count /Word Data
Range Decode Range From To Buffer Head I Buffer Tail	DefaultOK Cancel

Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

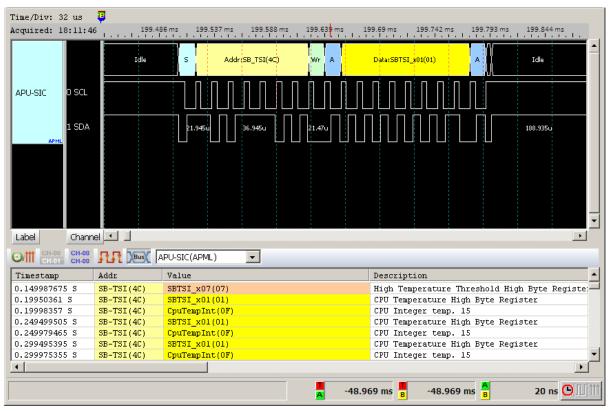
7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit R/W).

PEC: Packet Error Check.

Ignore glitch: Ignore the glitch when the slow transitions.



Result





BiSS-C

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings

BiSS-C Settin	g ×
Channel MA CH 0 SLO CH 1 Type of data Single Cycle Data Serial data length (bits) 12 Range Pecoded Range From Buffer Head To Buffer Tail	Color Ack/ADR Start Start CDS/CTS Data/Cmd Data/Cmd Flag/IDL/ID CRC Stop/Ex Stop/Ex Read/IDS Write/IDA
Default	t OK Cancel

MA/SLO: Setting the channel of MA and SLO.

Type of data: Setting the type you want to decode. It include "Register Data-CDM",

"Register Data-CDS", "Single Cycle Data".

Serial data length(bits): Setting the data length when Single Cycle Data mode.



Result

Time/Div: Acquired:		9:42.569 ₁	173.1968	385 ms		17	3.20008	15 ms		173	3.20328	5 ms		173	3.206489	Ą
SCD	BiSS-C	0,1	IDLE	A S				D:000				F:3		CRC:3A		
CDM	BISS-C	0,1	Reading						s							
			CRC:7						Р							
CDS		МА				\Box	ЛŢ			ΠΠ	Лſ	Ш		\square		
	BISS-C	SLO					5	.65 us	-			2.1	85 us			
																-
Label		Channel	•												<u> </u>	I
	ICH CH		Bus	CDM(BIS	5-C)		•									
Sample	CTS	ID(IDS)	ADR (CMD)	R/W	DØ	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
2089753	1	0	7C	Read	00											
2381312	1	0	ØF	Read	00	40	80	80	00	ØA	00	82	00	00	00	
4426118	1	0	1F	Read	00											
4662456	1	0	42	Read	2C	0C										
5251012	1	0	78	Read	4D	48	59	20	00	00	00	00				
6346663	1	0	76	Read	1F 00	00		_								_
6950714	1	0	7D	Read	00	00	00						_			I.
•															•	
			1	5.7723	14129	Hz	3	0.1291	69282	3 Hz	A B	0.12	63420	772 Hz	Θ <mark>ル</mark>	1111

Click OK to run the BiSS-C Decode and see result on the Waveform Windows below.



BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

Settings

BSD Se	ettings	×
Channel Data CH 0	Color DIR Address	
Bit rate Auto	Data	
Range		
Decode Range		
From Buffer Head	To Buffer Ta	ail 💌
De	fault OK	Cancel

Data: The BSD data.

Bit rate: The bit rate of the BSD data

Result

Click OK to run the BSD Decode and see result on the Waveform Windows below.

Time/Div: 1.28 ms	U I												
Acquired: 13:01:3	3.558	288.127 ms	290.175 ms 292	.223 ms	294.271 m	s 296.319 m	s 298.3	367 ms 3	00.415 ms 302.4	463 ms 30	4.511 ms	306.559 ms 308.60	07 ms
BSD BSD		JNKNOWN	Sync Master	Salve Addr:	6	Register Addr: 9	P1 Ok		Data: 1		P2 Ok	UNKNOWN	
850.			749 us 749 us									82.429 ms	
													-
	annel Tri												•
Off CH-00 CH-00 CH-01 CH-00	RR III	BSD(BS	D) 💌										
Timestamp	DIR	Salve Addr	Register Addr	P1	Data	P2 Acl	:						•
0.1908714 S	Master	6	2	Ok									
0.2908838 S	Master	6	9	Ok	01	Ok							
0.390865 S	Master	6	2	Ok									
0.4909086 S 0.590874 S	Master Master	6	8	Ok Ok	6a	Ok							
0.6909072 5	Master	6	9	Ok	01	Ok							
0.7908986 S	Master	6	2	Ok									
0.890911 S	Master	6	8	Ok	6a	Ok							-1
Image: A state of the state) }
					1	D 📕		101274	8	101274	A B	0 ()]][]]]] []



CAN 2.0B/ CAN FD

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN_H) and CAN Low (CAN_L).

The data rate is flexible in CAN FD (CAN with Flexible Data-Rate). When CAN FD is transferring, it is 64 (bytes/per data) and including CRC17/CRC21.

Settings

CAN Settings	X
Setting	
Channel	Auto detect Data Rate
CAN_L(Rx) CAN_L CH 0	0.00 v Kbps
	(5 Kbps ~ 1 Mbps)
	Show scale in the waveform
CAN_L (Rx)	CAN FD
	ISO-CRC Non ISO-CRC
	Data phase
	500 🔻 Kbps
Color	
•	
Start of Frame RTR bit	· · · · · · · · · · · · · · · · · · ·
Identifier SRR bit	· · · · · · · · · · · · · · · · · · ·
Data length code 📃 👻 IDE bit	· · · · · · · · · · · · · · · · · · ·
Data Reserved bit	•
CRC Delimiter bit	· · · · · · · · · · · · · · · · · · ·
ACK Slot	· · · · · · · · · · · · · · · · · · ·
End of Frame Error State	•
Range	
Decode Range	
From To	
Buffer Head 🔻 Buffer Tail 💌	
Default	OK Cancel



Channel: The differential data from the DSO channel (CAN_H or CAN_L) is shown by default.

Auto detect Data Rate: Check this option for auto-detecting the CAN bit rate by the

LA Viewer; this option will be disabled when enabling CAN FD decode, the

maximum input range of the Data rate is from 5Kbps-1Mbps.

Show scale in the waveform: Display the scale in the Waveform Window, this option will be disabled when enabling CAN FD decode.

Result

Time/Div: 25 us Acquired: 08:00:0	U.O -40 us	40 us		80 us 120 us 160 us	200	us 240 us	1.1.1.
CAN 1,	,0 Idle	DAT: 10 DAT: 0	0 DAT:00	DAT:00 DAT:10 DAT:70 DAT:00 DAT:80 CR	C:566C	EOF	
CAN_H D	502		<u> </u>	I. P. M. C. J. R. A.M.	M	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	1-V/Div
-	501				M	~~~~	L -2.52 V L -2.52 V Vpp 8.709 V H 3.723 V L -3.246 V
Label	-hanne						•
⊙/Ⅲ <u>CH-00</u> CH-00 CH-01 CH-00		CAN(CAN)]				
Timestamp	Frame Type	ID	DLC	Data	CRC (h)	ASCII (Data)	Inform 🔺
-0.0451195 S	Std Data	622	8	12 00 00 00 00 00 00 00	0A40		Data F
-0.0384585 S	Std Data	624	8	1A 00 00 49 47 40 00 00	1B27	IG0	
-0.031284 S	Std Data	630	8	17 00 00 00 00 00 00 00	2D04		
-0.024107 S	Std Data	638	8	13 00 10 00 00 00 00 00	0E45		
-0.000026 \$	Std Data	620	8	10 00 00 00 10 70 00 80	566C	p	
0.035053 %	Std Data	440	8	42 02 00 00 00 00 00 00	2301	B	
•	 						
				-91.117 ms 📕 -	85.874 m	s <mark>B</mark> 5.242 ı	ms 🕒 🖽 🏦

Click **OK** to run the CAN decode and see the result on the Waveform Window below.



cquired	: 08:00:00.0		3	15.56 us	32	1.96 us		.36 us 3	334.76 us 34	1.16 us	347.56 us 3	353.96 us	360.36 us
CAN	0 CAN	H	F				BaseID: 11	2	F	RTR:0 IDE:0	R0:0 DLC	C:8	DAT:CD
	CAN		7.50	J	2.5u	7.50		2.490 5.010	2,490	10.01u	2,49ن	7 [,] 51u	4.99u
Label	Chann	nel 💶	[▶
9/111 <mark>8</mark>	I-00 CH-00 R	R Bus	C CA	N(CAN)	I	-							
)/111 🔡 Tim	ноо СН-00 Л 101 СН-00 Л Frame Type	ID	CA DLC	N(CAN) Data	1	-]	CRC (h)	ASCII(Data)	Informat	cion	Frame Dur	ation
ン/ <u>C</u> Tim	1-01 CH-00 🗗 L		_	Data	97 E1		_	CRC (h) 38F5	ASCII(Data)		cion te: 400 Kbps	Frame Dun 282.46 un	
Zim D.30	<mark>⊫01 сн.00 ♪</mark> ∟ Frame Type	ID	DLC	Data CD F1		01 90							3
Tim 0.30 0.61	Frame Type Std Data	ID 112	DLC 8	Data CD F1 CD F1	97 E1	01 9C 01 9C	07 7D 07 7D	38F5				282.46 us	3
Fim 0.30 0.61 0.92	Frame Type Std Data Std Data	ID 112 112	DLC 8 8	Data CD F1 CD F1 CD F1	97 E1 97 E1	01 9C 01 9C 01 9C	07 7D 07 7D 07 7D 07 7D	38F5 38F5	·····}			282.46 u 282.47 u	3
Cim D.30 D.61 D.92 L.23	Frame Type Std Data Std Data Std Data Std Data	ID 112 112 112	DLC 8 8 8	Data CD F1 CD F1 CD F1 CD F1	97 E1 97 E1 97 E1	01 9C 01 9C 01 9C 01 9C 01 9C	07 7D 07 7D 07 7D 07 7D 07 7D	38F5 38F5 38F5	·····} ·····}			282.46 us 282.47 us 282.46 us	3 3 3 3
Tim 0.30 0.61 0.92 1.23 1.54	Frame Type Std Data Std Data Std Data Std Data Std Data	ID 112 112 112 112 112	DLC 8 8 8 8 8	Data CD F1 CD F1 CD F1 CD F1 CD F1	97 El 97 El 97 El 97 El	01 9C 01 9C 01 9C 01 9C 01 9C 01 9C	07 7D 07 7D 07 7D 07 7D 07 7D 07 7D	38F5 38F5 38F5 38F5 38F5	······} ······}			282.46 us 282.47 us 282.46 us 282.46 us	3 3 3 3 3
Tim).30).61).92 1.23 1.54 1.85	Frame Type Std Data Std Data Std Data Std Data Std Data Std Data Std Data	ID 112 112 112 112 112 112	DLC 8 8 8 8 8 8	Data CD F1 CD F1 CD F1 CD F1 CD F1 CD F1	97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C	07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5	······} ······}			282.46 us 282.47 us 282.47 us 282.46 us 282.47 us 282.47 us	3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
Tim 0.30 0.61 0.92 1.23 1.54 1.85 2.16	Frame Type Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data	ID 112 112 112 112 112 112 112	DLC 8 8 8 8 8 8 8 8	Data CD F1 CD F1 CD F1 CD F1 CD F1 CD F1 CD F1	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C	07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······} ······}			282.46 us 282.47 us 282.47 us 282.46 us 282.47 us 282.46 us 282.47 us	3 3 3 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5
Tim 0.30 0.61 0.92 1.23 1.54 1.85 2.16 2.47	Frame Type Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data	ID 112 112 112 112 112 112 112 112	DLC 8 8 8 8 8 8 8 8 8 8 8 8 8	Data CD F1	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C	07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······} ······}			282.46 us 282.47 us 282.47 us 282.46 us 282.47 us 282.46 us 282.46 us 282.47 us 282.46 us	3 3 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5
Tim 0.30 0.61 0.92 1.23 1.54 2.16 2.16 2.78	Frame Type Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data	ID 112 112 112 112 112 112 112 112 112	DLC 8 8 8 8 8 8 8 8 8 8 8 8 8	Data CD F1 CD F1 CD F1 CD F1 CD F1 CD F1 CD F1 CD F1	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C 01 9C	07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······} ······} ······}			282.46 us 282.47 us 282.47 us 282.46 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us	3 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
Tim 0.30 0.61 0.92 1.23 1.54 1.85 2.16 2.47 2.78 3.09	Frame Type Std Data Std Data	ID 112 112 112 112 112 112 112 11	DLC 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	Data CD F1 CD F1 CD F1 CD F1 CD F1 CD F1 CD F1 CD F1 CD F1	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C	07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	· · · · · · · · · · · · · · · · · · ·			282.46 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us	3 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
Tim 0.30 0.61 0.92 1.23 1.54 1.85 2.16 2.47 2.78	Frame Type Std Data Std Data	ID 112 112 112 112 112 112 112 11	DLC 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	Data CD F1	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C	07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	· · · · · · · · · · · · · · · · · · ·			282.46 u: 282.47 u: 282.47 u: 282.47 u: 282.47 u: 282.46 u: 282.46 u: 282.46 u: 282.46 u: 282.46 u: 282.46 u:	3
Tim 0.30 0.61 0.92 1.54 1.54 1.85 2.16 2.47 2.78 3.09 3.40	Frame Type Std Data Std Data	ID 112 112 112 112 112 112 112 11	DLC 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	Data CD F1 CD F1	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	01 9C 01 9C	07 7D 07 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5				282.46 us 282.47 us 282.47 us 282.46 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us 282.47 us 282.46 us 282.47 us	3



Closed Caption

Closed captioning is the process of displaying text on a TV or video screen. The text is encoded in the video data stream.

Settings

Closed	Caption Settings	×
Channel	A Channcel CH 0	_
Color —		
	Clock run-in Start Data Parity Clock run-in Parity Clock run-in Parity Clock run-in Clock run	
Range	Decode Range From To Buffer Head v Buffer Tail v	
	DefaultOkCanc	el

LA Channel: Show the selected channel (CH0).

Result

Click OK to run the Closed Caption Decode and see result on the Waveform Window

below.



Acquired: 16:44:	-2.102 S	-2.102 S	-2.102 S	-2.102 S -2.102	.s2.1	102 S -2.102	S -2.102 S
22 22	Idle	Clock run-in	Start	Data:00	Ρ	Data:00	P Idle
Clared Ception.			4.2u	14.2u		14u	33.317m
Label Channe							Þ
Channe Channe CH-00 CH-01 CH-01		CC(Closed Caption)) 🔽				•
		CC(Closed Caption)) 🔽				
⊙/∰ CH-00 CH-00 CH-01 CH-00							ت :
CH-00 CH-00 CH-01 CH-00 Timestamp	Data Byte 1	Data Byte 2	ASCII				
CH-00 CH-00 CH-01 CH-00 Timestamp -2.1021082 S -2.0687414 S	Data Byte 1	Data Byte 2 00	ASCII				
CH-00 CH-01 CH-01 Timestamp -2.1021082 \$ -2.0687414 \$ -2.0353746 \$	Data Byte 1 00 00	Data Byte 2 00 00	ASCII 				
CH-00 CH-00 CH-00 Timestamp -2.1021082 S -2.0687414 S -2.0353746 S -2.0020078 S	Data Byte 1 00 00 00	Data Byte 2 00 00 00	ASCII 				
CH-00 CH-01 CH-00 Timestamp -2.1021082 S -2.0687414 S -2.0353746 S -2.0020078 S -1.968641 S	Data Byte 1 00 00 00 00 00	Data Byte 2 00 00 00 00 00	ASCII 				
CH-00 CH-00 CH-00 CH-01 CH-01 CH-00 Timestamp -2.1021082 S -2.0687414 S -2.0353746 S -2.0020078 S -1.968641 S -1.9352742 S	Data Byte 1 00 00 00 00 00 00 00 00 00	Data Byte 2 00 00 00 00 00 00	ASCII 				
C)/fff CH-00 CH-00 CH-01 CH-01 CH-00 Timestamp -2.1021082 S -2.0687414 S -2.0353746 S -2.0020078 S -1.968641 S -1.968641 S -1.9052742 S -1.9019074 S -1.8685406 S	Data Byte 1 00 00 00 00 00 00 00 00 00 0	Data Byte 2 00 00 00 00 00 00 00 00	ASCII 				
C) (11 CH-00	Data Byte 1 00 00 00 00 00 00 00 00 00 0	Data Byte 2 00 00 00 00 00 00 00 00 00 00	ASCII 				-
C) (11 CH-00	Data Byte 1 00 00 00 00 00 00 00 00 00 0	Data Byte 2 00 00 00 00 00 00 00 00 00 00	ASCII 				
C)/fff CH-00 CH-00 CH-01 CH-01 CH-00 Timestamp -2.1021082 S -2.0687414 S -2.0353746 S -2.0020078 S -1.968641 S -1.968641 S -1.9052742 S -1.9019074 S -1.8685406 S -1.8351738 S	Data Byte 1 00 00 00 00 00 00 00 00 00 0	Data Byte 2 00 00 00 00 00 00 00 00 00 00	ASCII 			-15 us	



DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings		
DALI S	Settings	×
Channel		
1	LA Channel CH 0 • Polarity D-	-
	Show scale	
Color —		
	Start	•
	Address	-
	Command	•
	Response	•
	Stop	-
Range —		
inn:	Decode Range	
₩	From Buffer Head	•
	To Buffer Tail	•
	Default OK Cancel	

LA Channel: Show the selected channel (CH0).

Polarity:

D-: Access side of the signal polarity is D-.

D+: Access side of the signal polarity is D+.

Auto: Automatically detect the polarity of the access end signal.

Show scale: Show Scale on the waveform.



Click OK to run DALI Decode and see result on the Waveform Window below.

Idle Sta	3 ms 122.3 ms 124.3 ms 12 	· · · · · · · · · · ·		
1			Cmd:OFF(00)	Stop
•				•
		Response		Frame Duration
01	OFF(00)		Data Rate: 3.333 Kbps	
	· · ·		Data Rate: 5.555 KDps	15.10 ms
01	0FF(00)		Data Rate: 5.555 KDps	15.10 ms
01	OFF(00) OFF(00)		Data Rate: 5.555 KDps	15.10 ms 15.10 ms
01 01	OFF(00) OFF(00) OFF(00)		Data Rate: 5.333 KBps	15.10 ms 15.10 ms 15.10 ms
01 01 01	OFF(00) OFF(00) OFF(00) MIN(06)		Data Rate: 5.333 RDps	15.10 ms 15.10 ms 15.10 ms 15.00 ms
01 01 01 01 01	OFF(00) OFF(00) OFF(00) MIN(06) MIN(06)		Data Rate: 5.333 KDps	15.10 ms 15.10 ms 15.10 ms 15.00 ms 15.00 ms
01 01 01 01 01 01	OFF(00) OFF(00) OFF(00) MIN(06) MIN(06) MIN(06)		Data Rate: 5.333 KDps	15.10 ms 15.10 ms 15.10 ms 15.00 ms 15.00 ms 15.00 ms
01 01 01 01 01 01 01	OFF(00) OFF(00) OFF(00) MIN(06) MIN(06) MIN(06) MIN(06)		Data Rate: 5.333 KDps	15.10 ms 15.10 ms 15.10 ms 15.00 ms 15.00 ms 15.00 ms 15.00 ms
01 01 01 01 01 01 01 01	OFF(00) OFF(00) MIN(06) MIN(06) MIN(06) MIN(06) UP(01)		Data Rate: 5.333 Kbps	15.10 ms 15.10 ms 15.10 ms 15.00 ms 15.00 ms 15.00 ms 15.00 ms 15.00 ms
01 01 01 01 01 01 01	OFF(00) OFF(00) OFF(00) MIN(06) MIN(06) MIN(06) MIN(06)			15.10 ms 15.10 ms 15.10 ms 15.00 ms 15.00 ms 15.00 ms 15.00 ms
		Address Command	Address Command Response	Address Command Response Information

Response data

Time/Div: 1.2 m 📮					
Acquired: 17:43:	88.14 	65 88.1485 88.155 88.1528	88.154 S	88.156 \$ 88.15	85 88.165
DALI O DALI		art Addr;01		Cmd:Query(90)	Stop Idle
DALL				···	
					· · · · · · · · · · · · · · · · · · ·
Label Channel	•				
CH-00 CH-00 CH-01 CH-00	RA Bus	DALI(DALI)			
Timestamp	Address	Command	Response	Information	Frame Duration
Timestamp 88.4336 S			Response	Information	Frame Duration
	Address	Command	Response	Information	· · · · · · · · · · · · · · · · · · ·
88.4336 \$ 88.4532 \$ 88.7137 \$	Address	Command		Information	15.10 ms 8.30 ms 15.10 ms
88.4336 \$ 88.4532 \$ 88.7137 \$ 88.7333 \$	Address 01 01	Command Query(90) Query(90)		Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms
88.4336 \$ 88.4532 \$ 88.7137 \$ 88.7333 \$ 89.0578 \$	Address 01	Command Query(90)	04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.00 ms 15.00 ms
88.4336 \$ 88.4532 \$ 88.7137 \$ 88.7333 \$ 89.0578 \$ 89.0773 \$	Address 01 01 01 01	Command Query(90) Query(90) Query(90)	04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.00 ms 8.40 ms
88.4336 \$ 88.4532 \$ 88.7137 \$ 89.7333 \$ 89.0578 \$ 89.0773 \$ 89.4257 \$	Address 01 01	Command Query(90) Query(90)	04 04 04 04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.00 ms 8.40 ms 15.00 ms 15.00 ms
88.4336 S 88.4532 S 88.7137 S 88.7333 S 89.0578 S 89.0578 S 89.4257 S 89.4257 S	Address 01 01 01 01 01	Command Query(90) Query(90) Query(90) Query(90)	04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.00 ms 8.40 ms 15.00 ms 8.40 ms
88.4336 S 88.4532 S 88.7137 S 88.7333 S 89.0578 S 89.0578 S 89.4257 S 89.4452 S 89.4452 S	Address 01 01 01 01	Command Query(90) Query(90) Query(90)	04 04 04 04 04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.00 ms 8.40 ms 15.00 ms 8.40 ms 15.10 ms
88.4336 S 88.4532 S 88.7137 S 88.7333 S 89.0578 S 89.4257 S 89.4257 S 89.4452 S 89.7618 S 89.7814 S	Address 01 01 01 01 01 01	Command Query(90) Query(90) Query(90) Query(90) Query(90)	04 04 04 04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.10 ms 8.40 ms 15.00 ms 8.40 ms 15.10 ms 8.40 ms
88.4336 S 88.4532 S 88.7137 S 88.7333 S 89.0578 S 89.0773 S 89.4257 S 89.4452 S 89.7618 S 89.7618 S 89.7814 S 90.0658 S	Address 01 01 01 01 01	Command Query(90) Query(90) Query(90) Query(90)	04 04 04 04 04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.00 ms 8.40 ms 15.00 ms 8.40 ms 15.10 ms
88.4336 S 88.4532 S 88.7137 S 88.7333 S 89.0578 S 89.4257 S 89.4257 S 89.4452 S 89.7618 S 89.7814 S	Address 01 01 01 01 01 01	Command Query(90) Query(90) Query(90) Query(90) Query(90)	04 04 04 04 04	Information	15.10 ms 8.30 ms 15.10 ms 8.30 ms 15.10 ms 8.40 ms 15.00 ms 8.40 ms 15.10 ms 8.40 ms



DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings

DMX51	.2 Settings 🛛 🔀
Channel —	
1	Channel Data CH 0
	Auto Detect
	Baud 250000
Range	
	Decode Range
* *	From
	Buffer Head
	То
	Buffer Tail
	Default OK Cancel

Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

Result

Use grayscale to display the decode results.



	iv: 19.2 ed: 10:2		Ģ 0 _{1.1}	4	10.8 us	7	2.8 us	. 1	04.8 us		136.8	us	168	3.8 us		200.8 u	5 1.1	232.8	US	26	4.8 us	<mark>8</mark>
DMX51	2 0	Data	Idle	Dal	a: AE		Data:	6F		Data:	BA		Da	ita: D3			Data: A'	1		Data: I	FB	
	DM8512		8	u 12u	12	2.3u	16u	8u		12u	12	:3u	8u 8u]] 1	.6.3u	1	6u	12.3u	8u		28.3u	
																						-
Label	C	Thannel																				
©/111	CH-00 CH-01 C	H-00 H-00	nn	Bus	DMX51	2(DMX	512)	-														
⊙/ 111 s	CH-00 CH-01 State	H-00 H-00 D0	D1	Bus D2	DMX51 D3	2(DMX D4	512) D5	• D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	Infor	mati	on		
			D1		,				D7	D8	D9	D10	D11	D12	D13	D14	D15	Infor Baud			50000H	∎ Iz
s	State Idle Un		D1		,				D7	D8	D9	D10	D11	D12	D13	D14	D15				50000H	Iz
S -6 -1514 0	State Idle Un Idle	DO		D2	D3	D4	D5			D8											50000H	Iz
S -6 -1514 0 325	State Idle Un Idle Data	D0 AE	6F		,		D5 FB		FB	D8	D9 EE	D10 EF	D11 A5	D12 FA	D13 BB	D14 B9	D15				50000H	IZ
5 -6 -1514 0 325 14411	State Idle Un Idle Data Data	DO		D2	D3	D4	D5			D8 62 4B											50000H	IZ
S -6 -1514 0 325 14411 22325	State Idle Un Idle Data Data Idle	D0 AE	6F	D2	D3	D4	D5 FB		FB	D8 62 4B											50000H	
S -6 -1514 0 325 14411 22325 22391	State Idle Un Idle Data Data Idle Un	DO AE F8	6F C7	D2 BA 21	D3 D3 6A	D4	FB 97		FB	D8 62 48		EF	Α5	FA	BB						60000H	
s -6 -1514 0 325 14411 22325 22391 23210	State Idle Un Idle Data Data Idle Un Data	D0 AE	6F C7 C3	D2	D3	D4	D5 FB	D6 26 68 5A	FB E7 38	D8 62 48 90				FA		B9 40	A5 32				50000H	
S -6 -1514 0 325 14411 22325 22391 23210 37291	State Idle Un Idle Data Data Idle Un Data Data	DO AE F8	6F C7	D2 BA 21 F1 58	D3 D3 6A	D4	FB 97		FB	D8 52 4B 9C 3D		EF	Α5	FA	BB						50000H	
s -6 -1514 0 325 14411 22325 22391 23210	State Idle Un Idle Data Data Idle Un Data Data Data	DO AE F8	6F C7 C3 F1	D2 BA 21	D3 D3 6A	D4 A1 56 9A 41	D5 FB 97 B9 7F	D6 26 68 5A	FB E7 38 BB	D8 62 48 90 30 48 DE	EE 2B 4A	EF	Α5	FA AB 15	BB	B9 40	A5 32				60000H	
S -6 -1514 0 325 14411 22325 22391 23210 37291 51371	State Idle Un Idle Data Data Idle Un Data Data Data	DO AE F8	6F C7 C3 F1	D2 BA 21 F1 58	D3 D3 6A	D4 A1 56 9A 41	 D5 FB 97 89 7F A9 	D6 26 68 5A	FB E7 38 BB	62 4B 9C 3D 4B	EE 2B 4A	EF	Α5	FA AB 15	BB	B9 40	A5 32				50000H	
s -6 -1514 0 325 14411 22325 22391 23210 37291 51371 65450	State Idle Un Idle Data Data Idle Un Data Data Data	DO AE F8	6F C7 C3 F1	D2 BA 21 F1 58	D3 D3 6A	D4 A1 56 9A 41	 D5 FB 97 89 7F A9 	D6 26 68 5A	FB E7 38 BB	62 4B 9C 3D 4B	EE 2B 4A	EF	Α5	FA AB 15 11	BB	B9 40 03 10	A5 32	Baud	rate	= 25	:0000H	



Display Port Auxiliary Channel (DP Aux Ch)

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard.

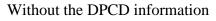
Settings

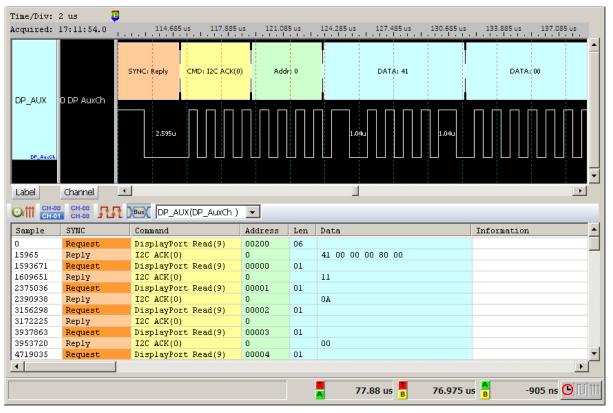
DP AU	X CH Settings 🛛 🛛 🔀
Channel	
P	Channel
	Data CH 0
Color	
	Setting transmitter's
	Request 🗾 🗸 Address 📃 🗸
	Reply Data
	CMD 🔽 🖌 Stop
Range —	
. <u></u>	Decode Range
*	From To
	Buffer Head 💌 Buffer Tail 💌
	Default OK Cancel

Data: Show the selected channel (CH0).

Show DPCD: Show the Display Port Configuration data.







Show the DPCD information

Time/Div: 2	2 us 🧧					
Acquired: 1	· · · · · · · · · · · · · · · · · · ·	114 202	- 121.09	Eur	124.285 us 127.485 us 130.685 u	- 122 00E un 127 00E un
Acquired: 1	17:11:54.0		1. 1. 1. 1. 1.		124.285 us 127.485 us 130.685 u	
DP_AUX	D DP AuxCh	SYNC: Reply CMD: I2C ACK(0) Add	r; 0	DATA: 41	DATA; 00
DP_AuxCh		2.595u			1.040	
Label	Channel		i	•		
€)/111 CH-00		 DP_AUX(DP_AuxCh)	•			
Sample	SYNC	Command	Address	Len	Data	▲
5500186	Request	DisplayPort Read(9)	00005	01		
5516087	Reply	12C ACK(0)	0		00	
5516087					00005h Bit[0] DWN STRM PORT PH	ESENT: 0
5516087					00005h Bit[2:1] Downstream por	
5516087					00005h Bit[3] This Branch Devi	
6281329	Request	DisplayPort Read(9)	00006	01		
6297167	Reply	12C ACK(0)	0		00	
6297167					00006h Bit[0] ANSI 8B/10B: 0	
7062464	Request	DisplayPort Read(9)	00007	01		
7078247	Reply	12C ACK(0)	0		00	
7843600	Request	DisplayPort Read(9)	00008	01		-
•						
					77.88 us 📕 76.975	us 🐣 -905 ns 🕒 💷 🏥



Enhanced Serial Peripheral Interface (eSPI)

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings

Enhanced	SPI (eS	PI) Parameter Se	ttings		X
Channel Se	ttings — CS# I/O 0 I/O 2 Alert	Ch 0 + Ch 2 + Ch 4 + Ch 4 +	SCK I/O 1 I/O 3	Ch 1 • Ch 3 • Ch 5 •	Advanced Decode Setting Show Configuration Detail Show Status Bit Def. Reduced Report Show Selected Contents
	I/O I Defaul	,	gle Mode m I/O[1]]	v v 50ns 15ns	PUT_IOWR_SHORT • GET_OOB • PUT_NP • GET_NP •
Cycle	oCode Type Tag ength		• • •	Address Data Response Status	▼ ▼ ▼ ▼
	Decode I From Buff		To Buffer	Tail 💌 Default	OK Cancel

Channel:

CS#:	Chip Select (Active Low)
------	--------------------------

- SCK: Clock
- $I\!/O0-I\!/O3\!:\quad Data\ input\ /\ output$
- Alert: Alert signal (Optional)

Startup Settings:



I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I / O

state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

Command deselect time: Set tSHSL, Chip Select# Deassertion Time.

Clock LOW to output valid: Set tCLQV, Output Data Valid Time.

Advanced Decode Setting:

Show Configuration Detail: Show details of SET_CONFIG / GET_CONFIG.

Show Status Bit Def.: Show details of Status.

Reduced Report: Reducing the report is easy to check the Command Flow.

Filter Setting: To show or hide the specific OP Code / Cycle Type or Address

range in the report.

Note: The setting of Address Filter would be saved as LA\eSPI\eSPIFilterX.bin in the work directory.

Result

Click **OK** to run the eSPI decode and see the result on the Waveform Window below.

			_														
ime/Div: 125 ns	9																
cquired: 16:26:02.21	-400 ns	-200 ns	1 😫	200 ns	400	ns 	600 ns	. 80	Ons	1 2	105	1	1	.2 us	1.1	1.4 us	1.60
													- 1				
0.004	IDL	GET	CONFIGURATIO	ON(21)	ADDR (00)		ADDR (10))			CRC (se)			TURN (88)	RESP (08)
0 CS#				1						1						1	
1 SCK		85 m	80 ns 85 ns	85 ns 85 ns	85 ns 85 ns	80 ns 85 ns	85 ns 85 n	15 85	ns 85	ns 80	ns 8	IS ns	85 ns	85 ns	85 n	85 ns 85	ns 85 ns
Spi 2 SI/SO0	165 ns	170 ns	165 ns	335	~	170 ns	170 ns	F	170 ns	-i		-					_
3 50/50						2/0113	1/010		1/0113	-		-	-		-		_
		170 ns	-		_				_	_		-	_		_		
4 WP/SO	2			1.175 us					170 ns	L							
5 Hold#/	503 165 ns				1.175 us								515	ns			170 ns
4071																	
Label Channel	· · ·																•
	10. 000																
CH-00 CH-00 PL	L Bus	[eSpi(eSPI)		*													
OpCode/Response	CycType						Address	DO	D1	D2	D3	D4	D5	D6	D7	Status	CRC
GET CONFIGURATION (21							0010										58
							0010										
							0010	13	11	00	00					030F	95
	Channel 0 C						0010	13	11	00	00					030F	95
	Peripheral (Channel Maxi	Imum Read R	equest Siz				13	11	00	00					030F	95
	Peripheral (Peripheral (Channel Maxi Channel Maxi	lmum Read R Lmum Payloa	equest Siz d Size Sel	ected = 6	4 bytes (1		13	11	00	00					030F	95.
	Peripheral (Peripheral (Peripheral (Channel Maxi Channel Maxi Channel Maxi	lmum Read R Lmum Payloa	equest Siz d Size Sel	ected = 6	4 bytes (1		13	11	00	00					030F	95
	Peripheral (Peripheral (Peripheral (Bus Master)	Channel Maxi Channel Maxi Channel Maxi	imum Read R Imum Payloa Imum Payloa	equest Siz d Size Sel	ected = 6	4 bytes (1		13	11	00	00					030F	95
	Peripheral (Peripheral (Bus Master) Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0	imum Read R Imum Payloa Imum Payloa iy = 1	equest Siz d Size Sel	ected = 6	4 bytes (1		13	11	00	00					030F	95
ACCEPT (08)	Peripheral (Peripheral (Bus Master) Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Read	imum Read R Imum Payloa Imum Payloa iy = 1	equest Siz d Size Sel	ected = 6	4 bytes (1			11							030F	95
ACCEPT (08)	Peripheral (Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 Co	Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Read Channel Enab apabilities	imum Read R imum Payloa imum Payloa iy = 1 ble = 1 and Config	equest Siz d Size Sel d Size Sup urations	ected = 6 ported = 0	4 bytes() 64 bytes:										030F	95
ACCEPT (08)	Peripheral (Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 C Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Read Channel Enab apabilities Channel Maxi	imum Read R imum Payloa imum Payloa iy = 1 ble = 1 and Config imum Read R	equest Siz d Size Sel d Size Sup urations equest Siz	ected = 6 ported = 0 e = 64 by	4 bytes() 64 bytes; tes(1)	0010									030F	95
ACCEPT (08)	Peripheral (Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 C Peripheral (Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Read Channel Enab apabilities Channel Maxi Channel Maxi	imum Read R imum Payloa imum Payloa iy = 1 ble = 1 and Config imum Read R	equest Siz d Size Sel d Size Sup urations equest Siz	ected = 6 ported = 0 e = 64 by	4 bytes() 64 bytes; tes(1)	0010									030F	95
ACCEPT (08)	Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 C Peripheral (Peripheral (Bus Master)	Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Reac Channel Enab apabilities Channel Maxi Channel Maxi Enable = 0	imum Read R imum Payloa imum Payloa iy = 1 ole = 1 and Config imum Read R imum Payloa	equest Siz d Size Sel d Size Sup urations equest Siz	ected = 6 ported = 0 e = 64 by	4 bytes() 64 bytes; tes(1)	0010									030F	95
ACCEPT (08)	Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 C Peripheral (Peripheral (Bus Master) Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Read Channel Maxi Channel Maxi Channel Maxi Channel Maxi	imum Read R imum Payloa imum Payloa iy = 1 ole = 1 and Config imum Read R imum Payloa iy = 0	equest Siz d Size Sel d Size Sup urations equest Siz	ected = 6 ported = 0 e = 64 by	4 bytes() 64 bytes; tes(1)	0010									030F	95.
ACCEPT (08) SET_CONFIGURATION (22 ACCEPT (08)	Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 C Peripheral (Peripheral (Bus Master) Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Reac Channel Enab apabilities Channel Maxi Channel Maxi Enable = 0	imum Read R imum Payloa imum Payloa iy = 1 ole = 1 and Config imum Read R imum Payloa iy = 0	equest Siz d Size Sel d Size Sup urations equest Siz	ected = 6 ported = 0 e = 64 by	4 bytes() 64 bytes; tes(1)	0010									030F	95.
ACCEPT (08) SET_CONFIGURATION (22	Peripheral (Peripheral (Bus Master) Peripheral (Peripheral (Channel 0 C Peripheral (Peripheral (Bus Master) Peripheral (Channel Maxi Channel Maxi Channel Maxi Enable = 0 Channel Read Channel Maxi Channel Maxi Channel Maxi Channel Maxi	imum Read R imum Payloa imum Payloa iy = 1 ole = 1 and Config imum Read R imum Payloa iy = 0	equest Siz d Size Sel d Size Sup urations equest Siz	ected = 6 ported = 0 e = 64 by	4 bytes() 64 bytes; tes(1)	0010										95 F5

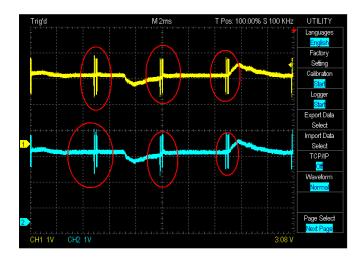


FlexRay

The FlexRay protocol has 2 bits with timing at 10Mbps.

FlexRay signal

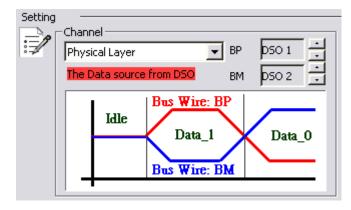
Physical Layer: We use the DSO to measure the differential signal at the FlexRay physical layer and get the blue-color BP signal and the yellow-color BM signal as the picture below.



Then, we subtract BP and BM values and get the red-color signal used by the logic analyzer to decode the FlexRay bus as the picture above.

In order to trigger from the logic analyzer, you need to connect the logic analyzer to

either the BP or BM pin in the setting dialog on the right.





Communication Data Layer: The FlexRay communication data is either at transmitter (Txd) or receiver (Rxd) of the FlexRay transceiver. You may set the threshold according to the FlexRay transceiver voltage.

FlexRay Settings
Setting Channel Physical Layer The Data source from DSO BM DSO 2 Setting Auto detect Data Rate 10 (1 Mbps ~ 20 Mbps) (1 Mbps ~ 20 Mbps)
Bus Wire: BP Data_0 Bus Wire: BM Data_0
Color
Indicator Bits Frame ID Payload Length Header CRC Cycle count Data CRC CRC TSS TSS TSS FSS FSS FSS TSS FSS TSS FSS FES TSS Cycle count Data CRC CAS/MTS
Range
Decode Range From To Buffer Head To Buffer Tail
DefaultCancel

Settings

Channel: Display the channel, Physical Layer is the default.

Physical Layer: The signals (BP, BM) are from the DSODSO channels can be Ch1 -

Ch6.

Communication Data (TxD): The TxD data is from the TxD and TxEN of the

FlexRay transceiver.



Communication Data (RxD): The RxD data is from the RxD and RxEN of the

FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in

Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.

FlexRay Channel: Channel A or B, for Frame CRC checking.

Errors are:

Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

Abbreviations are:

Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol
WUP	Wakeup Pattern
CID	Channel Idle Delimiter

Result

Click **OK** to run the FlexRay decode and see the result on the Waveform Window

below.

10Mbps FlexRay Communication Data(RxD)



HexRay Decode 0 RxD 200n 300n 300n 300n 300n 800n 200n 300n Label Channe	-6.38 us -5.98 us
CHIO CHOO CHIO FlexRay Decode(FlexRa**) Sample RPNCS Frame Id Pay Len HCRC (h) Cyc Cnt D0 D1 D2 D3 D4 D5 D6 D7 CRC (h) DTS ASCII (D0-Dr -238953	BSS PayLen: 16
Sample RPNCS Frame Id Pay Len HCRC(h) Cyc Cnt D0 D1 D2 D3 D4 D5 D6 D7 CRC(h) DTS ASCII(DO-D) -238953	
-238953 - 0 00	
-420 00111 1 16 0F2 28 00 21 00 F0 00 22 00 14	S ASCII(DO-D7) Informat 🔺
230 Image: Constraint of the second seco	
630 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030 (1) 1030	
1030	
7082 00111 4 16 6D3 28 FC 18 00	
7732 Image: Constraint of the constrai	· · · · · · · · ·
8132	· · · · · · · · · · · · · · · · · · ·
8532 9582 00100 5 16 005 28 04 4C 00	
9582 00100 5 16 005 28 04 4C 00 0A 0F 00 0A Image: Constraint of the const	
10232 00 1E 00	
10632 11032 100 00 00 00 00 00 00 00 00 00 00 00 00	· L · · · · ·
11032 00 00 00 00 00 00 00 00 4BE2A6 00	
	• • • • • • • • • • • • • • • • • • • •
-3.812 ms -3.812	ns 📙 180 ns 🕒 🕕 🕅



HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

Settings

HD A	udio	Settin	gs						×
Chann	nel —								
Þ	SYNC BCLK	сн о Сн 1	•	I/O 0	сн з	÷	Direction © SDI	O SDO	
Color									
	-Strean	n Data Preamble Length			•	Stream Sample		<u> </u>	
[Respo	nse (SDI) – Valid	, 			UnSol			7
		Reserved			<u> </u>	Respon	ise	•	
[-Comm	and (SDO) - Reserved			-	CAd		-	
		NID				Verb ID			
		Payload			-				
Range	•								
.	Deco From	de Range		То	I				
	Buff	er Head	-	В	uffer Tail		-		
					Default		OK	Cancel	

Channel: Show the selected channel (CH 0-CH3).

Direction: Show the data with SDI or SDO decoding.



Click **OK** to run the HD Audio decode and see the result on the Waveform Window

Time/Div: 60 ns ۲ Acquired: 08:00:00.0 166.775 us 166.875 us 166.975 us 167.075 us 167.175 us 167.275 us 166.575 us 166.675 us ample:00 Frame Sync:FF alid: Reserved:0 Response:00000000 SYNC 165 SDI_Bus BCLK Sample:00 VID:0 Frame Sync:FP Reserved:00 CAd:0 NID:00 SDO_Bus • Channel 💶 ► Label CH-00 SDI_Bus(HD Audio) CH-00 • Sample Frame Sync Valid Unsol Reserved Respone ٠ Stream Tag Length Sample 32757 00 00 00 00 00 00 00 00 33307 FF 00000000 0 00 00 00 00 00 00 00 00 00 00 00 00 00 34790 00 00 00 00 00 00 00 00 00 00 00 00 35857 00 00 00 00 00 00 00 00 00 00 00 00 36924 00 00 00 00 00 00 00 00 37474 FF 00000000 0 00 00 00 00 00 00 00 00 00 00 00 00 00 38957 00 00 00 00 00 00 00 00 00 00 00 🔻 F 28.265 us 🚪 38.04 us 9.775 us 🕒 🔟 🇰 A

below.



HDMI-CEC

The HDMI-CEC bus is a one-wire, "party line" that connects up to ten (10) AV devices through standard HDMI cabling. The CEC protocol includes automatic mechanisms for physical address (topology) discovery, (product type based) logical addressing, arbitration, retransmission, broadcasting, and routing control. Message opcodes support both device specific (e.g. set-top-box, DTV, and player) and general features (e.g. for power, signal routing, remote control pass-through, and on-screen display).

Settings

HDMI	-CEC Settings	×	٤
Channel			-
	Report Format		
:7	Oefault	O Advanced	
Color	Setting the channel o	of LA of CEC CH 0	
	Setting transmitter's	color	
U	Start Bit		
	Header Block		
	Data Block	· ·	
	EOM Bit		
	ACK Bit		
_	OPCode Block		
Range	Decode Range		
1	From	То	
	Buffer Head	▼ Buffer Tail ▼	
	Defaul	t OK Cancel	

Latch data: Nominal (1.05 micro seconds) or User Define.



Click \mathbf{OK} to run the HDMI-CEC decode and see the result on the Waveform Window

below.

Time/Div: 6.4 ms		76.04	- 1			262	46.400				Ţ
Acquired: 08:00:0	0.0	-76.84	8 ms - F	56.608 ms	-56	.368 ms	-46.128 n	ns -35. I.I.I	.888 ms	-25.648 ms -15.408	sms -5.168 ms
CEC 0 Dat		Start	Head	er : 36			Data :	36		Data : A9	Start A
нрміново	3.6m					UUL	ЛП				3.6m
											Ţ
			1		i	-	-	-			
Label Cha	nnel 💶										
CH-00 CH-00 CH-01 CH-00 CH-01 CH-00		CEC(H	HDMI-CEC)	[•						
Sample	Header	DO	Dl	D2	D3	D4	D5	D6	D7	ASCII	<u> </u>
-162107	36	36	A9							6.	
-82905	36	36	A9							6.	
-3702	36	36	A9							6.	
75501	36	36	A9							6.	
154704	36	36	A9							6.	
233907	36	36	A9							6.	
313110	36	36	A9							6.	
392312	36	36	A9							6.	
471515	36	36	A9							6.	
550718	36	36	A9							6.	
629921	36	36	A9							6.	
709124	36	36	A9							6.	
788327	36	36	A9							6.	
867529	36	36	A9							6.	
946732	36	36	A9							6.	•
											•
							A	8.241 m	s <mark>I</mark> B	75.31 ms <mark>B</mark>	67.069 ms 🕒 🔟 📖



HDMI-DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings

DDC(EDID) Setting	
Parameter Setting Channel Setting SCL Ch 0 SDA Ch 1	-
Address Mode	
7-Bit Addressing	
7-Bit Addressing(Include R/W in address)	
Ignore glitch Statistics Mode	
Color	-
Start Read/Write	
Stop 🔽 ACK	
Address NACK	
Data 🗾 👻	
Range	-
Decode Range	
From to	
Buffer Head 💌 Buffer Head 💌	
Default OK Cancel	

Channel: Display the channels (CH0 and CH1).

7-bit addressing: Show 7-bit addressing



7-bit addressing(Include R/W in Address): Show 8-bit addressing(include 7-bit

addressing and 1-bit Rd/Wr).

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Statistic Mode: Collect all the data frames into one report by register address order.

cquired: 18:07:3	8.0	10.0185 10.0185	10.0185 10.0185 10.0185	10.018 \$ 10	.0185 10.0185
	Idle	S Wr:74	A 00	S Rd:75	A 4F
DDC 1 SCL					
		35.15u 34.	106.78u	32.66u	23.07u 15.8u
_abel Chan	nel 💶				Þ
CH-00 CH-00 CH-00 CH-00		DDC(DDC(EDID))]		
ample	Address(h)	Offset(h)	EDID Register Name	EDID Data	
603521947	74(HDCP)				
	74(HDCP) 74(HDCP)		HDCP Offset = 00h		
003597004		0x00	HDCP Offset = 00h HDCP Receiver KSV(Bksv, Rd)	4F C6 AC B3 A0h	
003597004 003665359	74(HDCP)	0x00		4F C6 AC B3 A0h	
003597004 003665359 003802225	74(HDCP) 75(HDCP)	0x00 0x40	HDCP Receiver KSV(Bksv, Rd)	4F C6 AC B3 AOh	
003597004 003665359 003802225 003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h	4F C6 AC B3 AOh	
003597004 003665359 003802225 003870336 003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd)		
003597004 003665359 003802225 003870336 003870336 003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED	1	
003597004 003665359 003802225 003870336 003870336 003870336 003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready FAST	1 0	
003597004 003665359 003802225 003870336 003870336 003870336 003870336 003870336 003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready	1 0 0	
003597004 003665359 003802225 003870336 003870336 003870336 003870336 003870336 003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready FAST	1 0 0 1	
003597004 003665359 003802225 0003870336 0003870336 003870336 003870336 003870336 003870336 0003870336 0003870336	74(HDCP) 75(HDCP) 74(HDCP) 75(HDCP) 75(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready FAST Reserved, 2Bits	1 0 0 1 0	
1603521947 200365359 2003605255 2003802225 2003870336 2003870336 2003870336 2003870336 2003870336 2003870336 2003870336 2003870336 2003870336	74(HDCP) 75(HDCP) 74(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready FAST Reserved, 2Bits 1.1_FEATURES	1 0 0 1 0 0	
003597004 003665359 003802225 003870336 003870336 003870336 003870336 003870336 003870336 003870336 003870336 003870336	74(HDCP) 75(HDCP) 74(HDCP) 75(HDCP) 75(HDCP)		HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready FAST Reserved, 2Bits 1.1_FEATURES	1 0 0 1 0 0	
003597004 003665359 003802225 0003870336 0003870336 003870336 003870336 003870336 003870336 0003870336 0003870336	74(HDCP) 75(HDCP) 74(HDCP) 75(HDCP) 75(HDCP) 76(HDCP)	0x 40	HDCP Receiver KSV(Bksv, Rd) HDCP Offset = 40h Bcaps(Rd) HDMI_RESERVED HDCP Repeater capability KSV FIFO ready FAST Reserved, 2Bits 1.1_FEATURES	1 0 0 1 0 0 1	

Result



HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

Settings

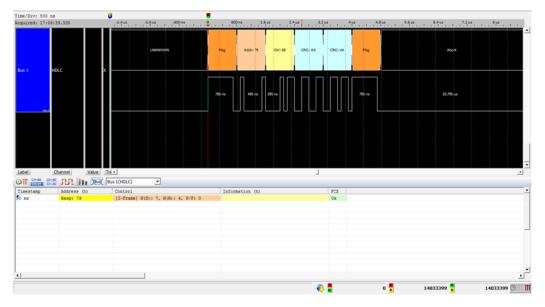
HDLC Settings		×
Channel HDLC CH 0 : Mode Synchronous V Bit rate Auto V	Color Flag Addr Control Information FCS	
Range Decode Range From Buffer Head	To Buffer Tail	•
D	efault OK	Cancel

HDLC: Set the channel of the signal.

Mode: Synchronous or Asynchronous mode.

Bit rate: Set the specific data rate or auto detection.

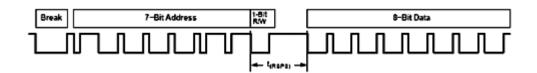
Result



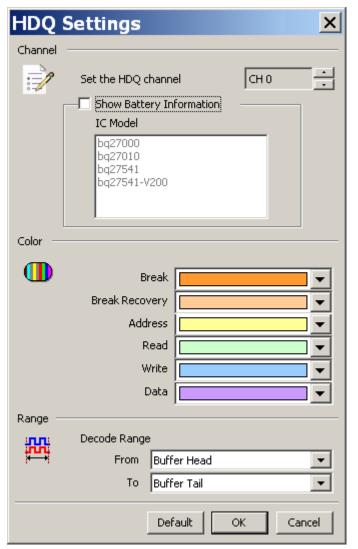


HDQ

The HDQ bus has two kinds of formats: 8 bits or 16 bits signals as the diagram below.



Settings



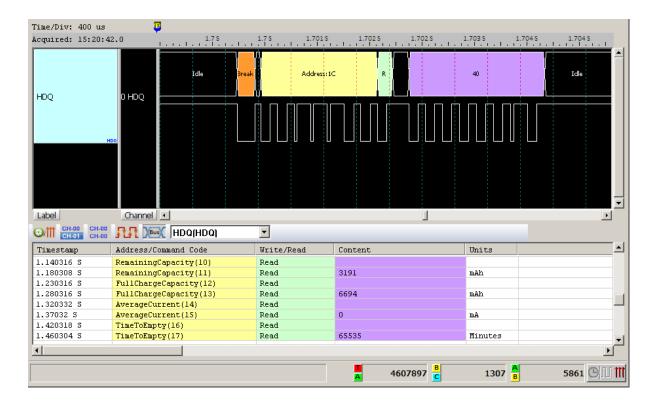
Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.



Time/Div: 400 us	. 📮								
Acquired: 15:20:4	2.0		640 us	1.28 ms	1.92 ms	2.56 ms	3.2 ms	3.84 ms	4.48 ms
HDQ	0 HDQ	Idle Break	Add	lress:00	R		19		Idle
н	DQ								
									_
Label	Channel								
CH-00 CH-00 CH-00 CH-01 CH-00 CH-00		 K HDQ(HDQ)	•		-				
Timestamp	Address	Read/Write	Data	ASCII					<u> </u>
0.00031 S	00	Read	19						
0.040312 5	01	Read	60	•					
0.090846 S	00	Write	07						
0.135214 S	01	Write	00	-					
0.16467 S	00	Read	00	-					
0.210318 \$	01	Read	00	-					
0.250882 \$	00	Write	00						
0.29522 \$	01	Write	00	-					
•	1								Þ
					4 6	07897 <mark>B</mark>	1307	A B	5861 🕒 🕕

Click **OK** to run the HDQ decode and see the result on the Waveform Window below.





HID Over I²C

HID Over I2C (Human Interface Device Over I2C) protocol is established by

Microsoft. It's applied for Windows 8 ARM platform.

Settings

HIDover	12C Settings				<u>? ×</u>
Setting			Color		
	Channel SCL SDA ATTN/Interrupt Address Mode • 7-bit addressing • 7-bit addressing (Ind • 10-bit addressing	CH 0 + CH 1 + CH 2 + CH 2 +		Start / Restart Address Write / Read Data ACK NACK STOP	
Range					
10.01	Decode Range				
	From Buffer Head	To Buffer Tail			
				Default	OK Cancel

Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Ignore glitch: Ignore the glitches occurred due to the slow transitions.



Time/Div: 1.2 us	9					Ş
Acquired: 13:44:	31.921 .	83.6 us	85.6 us 87.6 us 89.6 u	91.6 us 93.6	us 95.6 us 97.6 us 99	.6 us 101.6 us
		A	HID Desc: 1E	Α	HID Desc: 00	A
0 HID_Over_I2C	SCL SC			4.9 us		5 us
1	SDA		2.4 us 1.2 us	4,7 us	5.2 us	4.7 us
B HiDevori20	ATTN					
Label C	hannel Value 💶					· · · · · · · · · · · · · · · · · · ·
CH-00 CH-00 CH-00 CH-00		HID_Over_12	C(HIDover 🔻			
Timestamp	Status	Address	Field		Information	*
0.0327 ms	Repeat Start	Wr 4A	HID Descriptor Address(000	0)	HID Descriptor	
0.0939 ms	Repeat Start	Rd 4A	wHIDDescLength(001E)		30 bytes HID Descript	or
0.1138 ms			bcdVersion(0100)		Compliant with Version	n 1.00
0.1336 ms			wReportDescLength(00B5)		181 bytes Report Desc:	riptor
0.1535 ms			wReportDescRegister(001E)		Identifier to read Rep	port Descriptor
0.1000 82			wInputRegister(00D3)		Identifier to read In	put Report
0.1733 ms					20 bytes length field	
			wMaxInputLength(0014)		Zo byces rengen riera	of Input Report
0.1733 ms	-		wMaxInputLength(0014) wOutputRegister(00E7)		Identifier to read Ou	
0.1733 ms 0.1931 ms	-					tput Report
0.1733 ms 0.1931 ms 0.2129 ms			w0utputRegister(00E7)		Identifier to read Ou	tput Report of Output Report
0.1733 ms 0.1931 ms 0.2129 ms 0.2328 ms			wOutputRegister(00E7) wMaxOutputLength(0014)		Identifier to read Ou 20 bytes length field	tput Report of Output Report



I^2C

The Inter-Integrated Circuit (I²C) bus has two data bits: Serial Data (SDA) and Serial Clock (SCL).

Settings

I2C Settings		×
Parameters	Color	
Channel	Assign color	for specific data.
Clock Channel (SCL) CH 0	Address	
Data Channel (SDA) CH 0	Data Write	
Address mode	Data Read	
• 7-bit addressing	Unknown	•
7-bit addressing (Include R/W in Address)	Start	
C 10-bit addressing	Re-Start	
Report	Stop	•
Show data in report 8 Column 💌	ACK	
Ignore glitch	NACK	•
Range & Misc.	Reserved Address	
Decode Range		_
From To		
Buffer Head 💌 Buffer Tail 💌		
	Default	OK Cancel

Channel: Display the channels (CH0 and CH1).

Address Mode: Select the 7-bit or 10-bit address.

7-bit addressing: Show 7-bit addressing.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Report: Show either 8 or 16-columns data in the report window.



Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Result

Click OK to run the I²C decode and see the result on the Waveform Window below.

It shows frequency in the Information fi	eld.
--	------

'ime/Div: 50 u .cquired: 08:0	· · · · · · · · · · · · · · · · · · ·	463.604 ms	463.6	84 ms	463.7	64 ms	463.84	44 ms	463.9	24 ms	464.004 ms	464.084 ms 464.164 ms
equired. 00.0	1.1.1		1.1.1.1	Γl'iT.		1 . I .						
		Addr:45		A	0	1	A	s.	Addr:4	5	A O	14 <mark>A</mark> 4D -
I2C	O SCL			54u			35u				43u	33ч
								הר	П			
120		35u	23u	1	29u		42u	L	35u	23u	42u 52u	35u 33u 24u
Label	Channel 💶											•
CH-00 CH		I2C(I2C)		-								
⊙/Ⅲ <u>CH-01</u> CH	1-00	120(120)										
Sample	Status	Addr	DO	Dl	D2	D3	D4	D5	D6	D7	ASCII	Information
457550	Start	Wr 45	4D	03	10	00	28				M(
463551	Start	Wr 45	01									
463857	Repeat Start	Rd 45	04	4D	10	4E	09				.M.N.	
469762	Start	Wr 45	4D	03	10	00	73				Мз	
475708	Start	Wr 45	01									
476018	Repeat Start	Rd 45	04	4D	10	4E	0A				.M.N.	
482008	Start	Wr 45	4D	03	10	00	42				МВ	
488028	Start	Wr 45	01								•	
488337	Repeat Start	Rd 45	04	4D	10	4E	OB				.M.N.	
494304	Start	Wr 45	4D	03	10	00	OF				M	
500190	Start	Wr 45	01									
500562	Repeat Start		04	4D	10	4E	00				.M.N.	
506481	Start	Wr 45	4D	03	10	00	BO				M	
512509	Start	Wr 45	01									
512803	Repeat Start	Rd 45	04	4D	10	4E	OD				.M.N.	
•												•
					_		-		_		198.351 ms 🔒	
									9 ms		.98.351 ms 🔒	17.952 ms 🕒 🛄



I3C

I³C is a bus interface for connecting sensors to an application processor. It is a core sensor integration technology that can combine multiple sensors from different vendors in a device to streamline integration and improve cost efficiencies. It gives developers unprecedented opportunity to craft innovative designs for any mobile product, from smartphones, to wearables, to safety systems in automobiles.

Settings

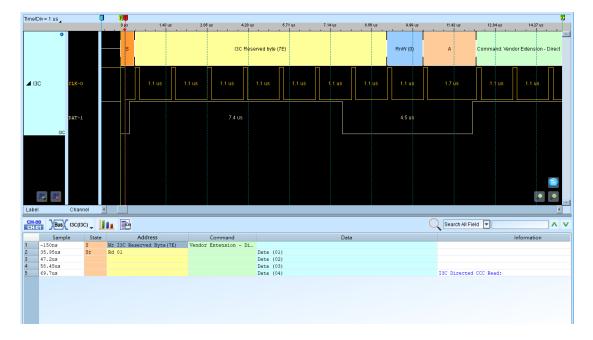
I3C Settings	×
Channel SCL A0 SDA A1	Color S / Sr / P ACK / NACK Address
Range Decode Range From To	Command Data RnW T / PAR HDR RESTART
Buffer Head V Buffer Tail V	HDR Exit

Channel: Display the channels (CH0 and CH1).



Click **OK** to run the $I^{3}C$ decode and see the result on the Waveform Window below.

It shows frequency in the Information field.







I²C EEPROM

EEPROM can be erased and reprogrammed (written to) repeatedly through the application of higher than normal electrical voltage generated externally or internally in the case of modern EEPROMs.

Settings

I2C(EEPROM 24 Series) Setti	ngs X
Parameters	Color
Channel Clock Channel (SCL) CH 0	Assign color for specific data.
	Start 🗾 👻 Output Enable 🔽 🗸
Data Channel (SDA) CH 1	Control Vevice ID
Address	Address Command Select
Address Width 7	Read Data
	Write Stop
7-bit addressing (Include R/W in Address)	
24LCS61 / 24LCS62 Ignore glitch	
Range & Misc.	
Decode Range	
From To	
Buffer Head 🔽 Buffer Tail 🔽	
	(Default) OK Cancel

Channel: Display the channels (CH0 and CH1)

Address: The default address width is 7.

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit Rd/Wr).

24LCS61/24LCS62: 24LCS61/24LCS62 EEPROM protocol.

Ignore glitch: Ignore the glitch when the slow transitions.



Click OK to run the I^2C EEPROM decode and see the result on the Waveform

Time/Div: 5 us Acquired: 13:36:	9 41.0	91.1	us	99.1 us 1	107.1 u <mark>s</mark>	115.1 us		123.1 us		131,1 us		139,1 us	1	.47.1 us
	A	s	Control		Select: 00 Rd	A				Data: 2				
	SDA	2.7u 3.1 3u	2.8ú 2.5u 2.	50 100	2.6u	7.:	2u 13.4u		2.5u 2.5u	J 2.5u	5u	5u] [2.8u
Label	Channel 💶													•
CH-00 CH-00 CH-00 CH-01 CH-01 CH-00	RA Neus	I2C_e	eProm(I2C(EEPR										
Sample	Ctrl Code	CS	Rd/Wr	Addr Hi	Addr Lo	DO	D1	D2	D3	D4	D5	D6	D7	ASCII 🔺
15	0A	00	Wr	00	00									-
867	0A	00	Rd			29	6B	D6	EB	20	A9	03	21)k,.
3362						BB	EF	5F	5F	4C	FC	10	EC	L.
5515						BE	D4	ED	51	06	45	4D	99	Q.E
7669						25	8E	51	65	53	05	5C	33	%.QeS.
						EC	ЗF	54	16	A7	22	CD	CC	.?T"
9822						8F	60	D4	F3	4E	4A	60	3D	.`NJ
9822 11975						CB	EE	2F	68	16	75	93	6D	/h.u
								77.0	OD	40	E6	05	39	53L.
11975						35	33	F4	00	40	20			
11975 14129	OA	00	Wr	00	40	35	33	F4	00	-10	20			
11975 14129 16282	0A 0A	00	Wr Rd	00	40	35 21	33	73	11	8B	DO	Al	5A	!.s
11975 14129 16282 74398				00	40									!.s Pc.2
11975 14129 16282 74398 75265				00	40	21	10	73	11	8B	DO	Al	5A	
11975 14129 16282 74398 75265 77760				00	40	21 50	10 63	73 91	11 32	8B D8	DO F6	A1 A8	5A E9	Pc.2

Window below.



I^2S

The Inter-Integrated Circuit Sound (I2S) bus has three data bits: Serial Clock (SCK), Word Select Line (WS) and Multiplex Data Line (SD).

Settings

I2S Settings			×
Channel Clock Channel (SCK) Word Select Channel (WS) Data Channel (SD) Data bits	CH 1 ÷		User can assign color for specific pattern. First Pattern & Color 0
Display the audio waveform Save as WAV file Mode I25 Justified Mode	 ✓ Playback Report 8 Column 	Range	Decode Range From Buffer Head To Buffer Tail
			Default OK Cancel

Channel: Show the selected channels (CH0, CH1 and CH2) and set Data bits (16

bits).

Display the audio waveform: Click to display the audio waveform in the Waveform

Window.

Playback: Click to display the audio from the speaker..

Save as WAV file: Click to save the data to a audio file(.wav) in the work directory.

Mode: I²S Justified/MSB Justified/LSB Justified/PCM/TDM.

Report: Select the column number.

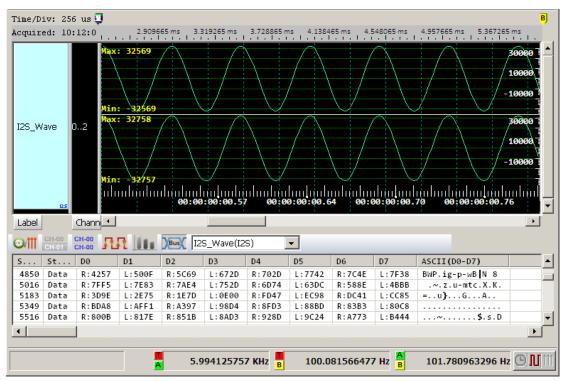
Result

Click OK to run I²S decode and see the result on the Waveform Window below.



Time/Div: 16 us					Ţ					
Acquired: 10:21	-102.4 us	-76.8 us	-51.2 us	-25.6 us	🐓	25.6 us	51.2 us	76.8 us	102.4 us	
	L:B2D40	R:B2D40	L:B67E0	R:B67E0	L:BA1B0	R:BA1B0	L:BDA90	R:BDA90	L:C1270	
0 SCH I2S_Data										
1 WS	24u	24u	24u	24u	24u	24.01u	24u	24u	24u	
2 SD	80 100	100		90		J .990) 8u	84		-
Label Chan	·								Þ	
CH-00 CH-00 CH-01 CH-00	RR Xes(7							
Sample	I2S_Data									•
25253	R:CB3B0									
27653	L:CE720									
30053	R:CE720									
32453	L:D1960									
34854	R:D1960									
37254	L:D4A40									
39654	R:D4A40									
42054	L:D79E0									
44454	R:D79E0									
46854	L:DA810									
49255	R:DA810									_
51655	L:DD4D0									_
•									>	
					-22.9	908 ms 📕	-23.04 r	ns <mark>A</mark> -1	31.75 us 🕒 🗌	ſ <u>↑</u> ↑↑

Display the audio waveform





I80

The I80 controls 3 or 4-pins (WR, RD, CS, D/C) data.

Settings

I80 Setti	ings 🛛 🗾
Channel —	
-	Select Channel
:=//	D0 CH 0 + D8 CH 11 + D16 CH 19 +
	WR CH0 + D1 CH0 + D9 CH 12 + D17 CH 20 +
	RD CH0 🛨 D2 CH0 🕂 D10 CH 13 🕂 D18 CH 21 🗧
	CS CH0 🛨 D3 CH0 🕂 D11 CH 14 🕂 D19 CH 22 🗧
	D4 CH 0 🕂 D12 CH 15 🗧 D20 CH 23 🗧
	□ On D/C D5 CH 0 + D13 CH 16 + D21 CH 24 +
	D7 CH 0 🕂 D15 CH 18 🐳 D23 CH 26 🐳
	Data Bus Bit Order Report Data 8 Bits LSB First 8 Column
Color ——	Calling Calu
	Setting Color
_	Command Read
	Data 🗾 🚽 Write 🗾 🚽
Range	
inni	Decode Range
	From To
	Buffer Head 💽 Buffer Tail 💌
	DefaultOKCancel

Select Channel: Show the selected channels (WR, RD, CS, D0, D1, D2, D3, D4, D5,

D6,...).

On D/C: Use the D/C pin as Command (Low) or Data (High).

Data Bus: Select 4 Bit, 8 Bit, 12 Bit, 16 Bit, 20 Bit, or 24 Bit.

Bit Order: Select LSB First or MSB First.



Report Data: Select 8 columns or 16 columns.

Result

Click **OK** to run the I80 decode and see the result on the Waveform Window below.

Time/Div: 240 ns Acquired: 13:59:5.		2.05 ms 2.0	51ms 2.05	1ms 2.	051ms 2.05.	2 ms 2	2.052 ms 2.	053 ms	2.053 ms
		Idle			Command Write:E			Idle	· · · · · · · · ·
2 1/	VR		360n						
3 R									
0 C								3.66u	
4 D	0								
5 D	1								
^{I80} 6 D									
7 D						1			
8 D									
9 D									
10 11									
1 D									
180 1 10	ν ^η C								T
Label Ch	nannel 💶 📕								
CH-00 CH-00 CH-01 CH-00		30(I80)	•						
Sample	Data/Command	Write/Read	Data		ASCII				•
52077	Data	Write	CO		À				
102559	Command	Write	DE		Þ				
102925	Data	Write	01						
103310	Data	Write	00		•				
153792 154158	Command Data	Write	BB OA		»				
154543	Data	Write Write	0A 00		•				
205025	Command	Write	B7		•				
•									
•									
				–	-5.06 us	B	-4.66 us 🔒	400) ns 🕒 🖽 🏦



IDE

IDE (Integrated Device Electronics) is a computer hardware bus and has the following data bits:

General Channel (11 pins): DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP,

DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-,

RESET-, CSEL, IOCS16-.

Register Channel (5 pins): CS(0:1)-, DA(2:0).

Data Bus (16 pins): DD(15:0)

We recommend that IDE bus of the target system to be connected to the instrument as

the followin	g table:		
IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4
Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14



Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25		Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMAR DY- :DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24
Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		



Settings

IDE S	Settings		×
Channe	el		
-2	General Register Data B	us	
:7	DIOR-HDMARDY-HSTROBE	H 19 PDIAG-:CBL	ID- CH 26 📑
	DIOW-ISTOP	H 18 DASP	• СН 31 🕂
		H 17 RESE	
	IORDY:DDMARDY-:DSTROBE	H 20 CSEL	CH 21 ÷
		H 22 IOCS	16 CH 24
	····· 、 ,	H 23 🚔	
Color a	nd Setting	. r .	
	Transferring Mode Registe	er Color Analysis Re	port
	Transferring Mode	Max Transferring Rate	Standard 🔺
	DMA Single word, Mode 2	8.33MByte/sec	ATA
	DMA Multiple word, Mod	4.17MByte/sec	ATA
	DMA Multiple word, Mod	13.3MByte/sec	ATA-2
	DMA Multiple word, Mod	16.7MByte/sec	ATA-3
	ULTRA DMA Mode 0	16.6MByte/sec	ATA-4
	ULTRA DMA Mode 1	25MByte/sec	ATA-4
	ULTRA DMA Mode 2	33MByte/sec	ATA-4
	ULTRA DMA Mode 3	44MByte/sec	ATA-5
	ULTRA DMA Mode 4	66MByte/sec	ATA-5
	ULTRA DMA Mode 5	100MByte/sec	ATA-6
	ULTRA DMA Mode 6	133MByte/sec	ATA-7 🔽
_			
Range	Decode Range From	То	
	Buffer Head 📃	Buffer Tail	▼
		Default	Cancel

Channel: Set channel number for General, Register, and Data Bus.

Transferring Mode: Select the target system.

Analysis Report: Filter the data in the Report Window.



Result

Time/Div: 300 ns Acquired: 08:00:00	0.0	F	2.1 us	2.6 us	3.1us	3.6 us	4.1 us	4.6 us 5.	1 us
ΑΤΑ/ΑΤΑΡΙ	_{DE} 15,3		tor cnt:01	LBA Low	1	A Mid:00	LBA High:00		
DIOR-:HDMARDY-:HS	TROBE 19								
DIOW-:STOP	18		300n	500n	300n 400r	n 300n	500n	300n 600n	
Data(015)	16,:	14,12,: 0101) 51	01	3200	X	0000 X	00A1)0CA
Register	29,3	30,28,2 OA	(18) OB	(18)	0C	X	0D (18)	0E 🕺 18	X OF
DMARQ	17								
IORDY:DDMARDY-:D	STROBE 20								
DMACK-	22								
INTRQ-	23								
PDIAG-:CBLID-	26								
DASP-	31								
Label	Ch	annel 💶							•
CH-00 CH-00 CH-00 CH-00		ATA/ATAPI(ID	E) 💌						
Sample	Event	Register	Data Hi	Data Lo	Command	Drive	Description	Time interval	
16	Wr Sector	1F2		01		0		1.300 us	
23	LBA Low	1F3		01		0		700 ns	
31	LBA Mid	1F4		00		0		800 ns	
38	LBA High	1F5		00		0		700 ns	
46 55	Wr Device Wr Command	1F6 1F7		Al CA	WRITE DMA	0	DEVO DMA command	800 ns 900 ns	
84	Wr Data	1F0	3C	EB	WRITE DHA	0	ASCII=<.	2.900 us	
87	Wr Data	1F0	44	53		0	ASCII=Q.	300 ns	-
					A 10	D us 📕	11.5 us 🔒	1.5 us 🤇	111 UL C

Click **OK** to run the IDE decode and see the result on the Waveform Window below.



Indicator

Indicator is to display with the time or clock samples on the Waveform window to be helpful to read the waveform.

Settings

Indicator Settin	gs	×
Reference		
Cursor Tr	rigger(T)	•
		_
Conly of	lisplay time	
Default	OK	Cancel

Reference: Set the reference position (Trigger cursor), time value on the right (left) is positive (negative). Default reference position is the trigger cursor and also shows time or sample rate.

Only display time: to show time only.

KUSUII			
Time/Div: 32 us			R
Acquired: 10:36:1	0.0 546.605 us	597.805 us 649.005 us 700.205 us 75	1.405 us 802.605 us 853.805 us
indicator	528.0us 576.	0us 624,0us 672,0us 720,0us	768.0us 816.0us 864.0us
ChO	0 1 <u> </u>	23.444	19.53u
			•
Label	Channel Value		Þ
CH-00 CH-00 CH-01 CH-00 CH-01 CH-00	FLR)Bus(
Sample	indicator	Ch0	<u>•</u>
-335872		0	
781		0	
1562		1	
3907 4687		0	
5469		1 0	
7813		1	
8594		0	
•			
		A 2.387 ms B -2	2.141 ms 🦰 -4.527 ms 🕒 🔟 🇰

Result

Add two Indicators for two channels with two different cursors as the references to display the result on the Waveform Window below.



IrDA

The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

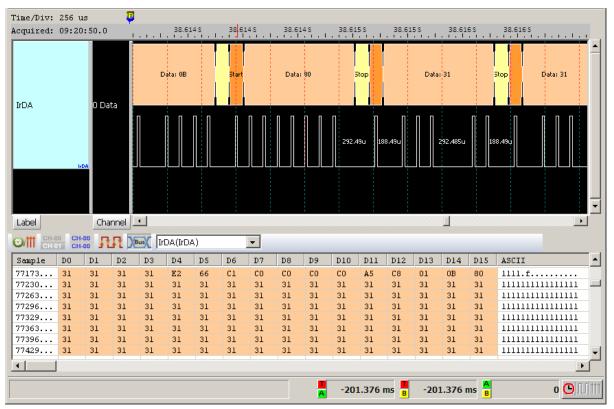
Settings

IrDA S	Settings	×
Channel	LA channel CH 0 💌	
Color		
	Start 🗾 💌	
	Data 🗾 🔽	
	STOP	
	Addr 🗾 🔽	
Range —		
	Decode Range	
ر میں ا	From To	
	Buffer Head 💌 Buffer Tail 💌	
	Default OK Cancel	

Channel: Show the selected channel.



Result





ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

Settings

ITU656(CC	CIR656) Settings
Channel –	
=	Channel Data Bits
0 - 2	Clk CH 0 + Data 5 CH 6 + 8 Fits
	Data 0 CH 1 🕂 Data 6 CH 7 🕂
	Data 0 CH 1 + Data 6 CH 7 + Data 1 CH 2 + Data 7 CH 8 + Data 2 CH 3 + Data 8 CH 9 +
	Data 2 CH 3 🗧 Data 8 CH 9 🚊
	Data 3 CH 4 🗧 Data 9 CH 10 🚊
	Data 4 CH 5 ÷
Color	
	Setting transmitter's color
	SAV CR CR
	EAV CB
	Blanking Y
Range	
-	Decode Range
	From To
1 1	Buffer Head Buffer Tail
	, _
	· · · · · · · · · · · · · · · · · · ·
	Default OK Cancel

Channel: Show the selected channel (Clk, Data 0 – Data 9).

Data Bits: Show the number of data bits.



Result

	: 500 ns					.25 us	37.05	us	್ರತ್ತ	7.85 US 38	5.65 US 39.45 US	5
Acquired:	: 09:55:5	33.85 us 34.65	5 US		<u>, 1, 15</u>	1.1.1.1	1 1		1.1.1			1.1.1.1
		UNKNOWN)	5	AV(80): Feld	1, elsewhe	ere.				¢B: 80	Y: 10	CR: 80
	0 Clk	500n 505n 495n	500n	500n	500n	500n	505n	495	in [505n 495n	505n 495n	505n
	1 Data0											
	2 Data1	1.005u										
	3 Data2	1.0054										
ITU656	4 Data3	1.005u										
	5 Data4	1.0050				4.1650				1	815n	
	6 Data5	1.0054										
		1.0050										
	7 Data6	1.0050		4.675	_		475				1.145u	
ITU656	8 Data7			1.975ų	_		975n	L	_	865n	1.145u	
Label	Chauser					i	i		- i	i		
Label					i		i			•		
	Channel	— -	56)									
		— -	56) CB	• ¥	CR	Y	C. Y	CR	У	EAV	Information	
			CB		CR 80	у 10	C. Y	CR	¥	EAV 98: Error	Information	
⊙/∰ CH CH Sample			CB 80	Y			с. ч	CR	У		Information	
Sample 2519 6736 10953		SAV B0: Field 1, elsewhere. 80: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80	Y 10	80 80 80	10 10 10	с. у	CR	У	98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171		SAV 80: Field 1, elsewhere. 80: Field 1, elsewhere. 80: Field 1, elsewhere. 80: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80	Y 10 10 10 10 10	80 80 80 80	10 10 10 10	с. ч	CR	Y	98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388		SAV 80: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80	Y 10 10 10 10 10 10	80 80 80 80 80	10 10 10 10 10	С. У	CR	Y	98: Error 98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388 23605		SAV 80: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80 80	Υ 10 10 10 10 10 10 10 10	80 80 80 80 80 80	10 10 10 10 10 10	с. ч	CR	Y	98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388 23605 27822		SAV 60: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80 80 80	Y 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80	10 10 10 10 10 10 10 10	<u>C.</u> Y	CR	Y	98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388 23605 27822 32040		SAV 60: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80 80 80 80	Υ 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80	10 10 10 10 10 10 10 10 10	C. Y	CR	Y	98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388 23605 27822 32040 36257		SAV 80: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80 80 80 80 80 80 80	Υ 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80	10 10 10 10 10 10 10 10 10 10	C. Y	CR	Y	98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388 23605 27822 32040		SAV 60: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80 80 80 80 80 80 80	Υ 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80	10 10 10 10 10 10 10 10 10	¥		Y	98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error	Information	
Sample 2519 6736 10953 15171 19388 23605 27822 32040 36257		SAV 80: Field 1, elsewhere. 80: Field 1, elsewhere.	CB 80 80 80 80 80 80 80 80 80 80 80 80	Υ 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	80 80 80 80 80 80 80 80 80	10 10 10 10 10 10 10 10 10 10	C. Y		Y	98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error 98: Error	Information	



JTAG

Joint Test Action Group (JTAG) is the common name used for the IEEE 1149.1 standard entitled Standard Test Access Port and Boundary-Scan Architecture for test access ports used for testing printed circuit boards using boundary scan.

A JTAG interface is a special four/five-pins interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met, and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board.

Settings

JTAG	6 Settings			×
Setting	, ———			
2	Channel Setting Report	t		
	Test Clock (TCK)	СН0 :	Test Reset (TREST)	СН 4 🗧
	Test Mode Select (TMS)	<u>·</u>	<u>ا</u> '	
	Test Data Input (TDI)	сн 2 🕂		
	Test Data Output (TDO)	сн з 🕂	1	
Color				
TEST	_LOGIC_RESET	-	EXIT1-IR	•
RUN_	TEST_IDLE	▼	EXIT1-DR	•
SELE	CT-IR		PAUSE-IR	•
SELE	CT-DR	_	PAUSE-DR	
CAPT	URE-IR		EXIT2-IR	
CAPT	URE-DR	-	EXIT2-DR	
SHIF	T-IR	_	UPDATE-IR	-
SHIF	T-DR		UPDATE-DR	
Range	e			
**	Decode Range From	То		
	Buffer Head 💌	Buffer Tail	•	
			Default Ok	Cancel



Settings: Includes Channel, Setting, and Report.

Channel: Set the channel number.

Show the test data is: The data is TDI or TDO.

Test Data Bit Order: LSB First or MSB First.

Channel	Setting	Report					
-Show th	ne test dal	a is ——		🔽 In	terpreter instr	ruction	
Test	t Data Inp	ut (TDI)		ID	Name		Len
CT	- D 0	put (TDO)		000	ARM7~ARM9	9	4
l vo resi	t Data Oui	puc (TDO)		001	ARM10		4
			1	002	ARM11		5
_ Test Da	ita Bit Ord	er ———					
LSB Fir	~h	_					
JESO FI	st	<u> </u>		L			
						Refresh	Edit

Interpreter instruction: Check the Interpreter Instruction and you will see a list of commands. The JTAG decode will display its updated commands in the Instruction Register, which is the temporary memory buffer for the commands. Click Edit to edit the commands in the Interpreter Instructions; then click Refresh to update the commands in the Interpreter Instructions.

Acute JTAG Instruction table (JtagInst.txt): This file is supported by the JTAG DLL and can be modified if needed. The JTAG Decode also supports the BSDL format. You can load the BSDL file in order to save time on editing commands. If you are interested in more details, please refer to the Acute JTAG Instruction table Syntax Description in the end of the JTAG Decode chapter.

Report: You can filter the data you want to see on the Report Window.

Channel Setting Report	
Show the state in report	
☑ Test-Logic-Reset	
Run-Test/Idle	
Select-DR-Scan	
Select-IR-Scan	
Capture-DR	
Capture-IR	_
Show TDI or TDO Show TDI and TDO	D

Show TDI or/and TDO



Result

The Altera EPM3256AT144 Programming Schematic JTAG decode on the

		Rur	n-Test/Idle		Select-Di	R-Scan	Select-	IR-Scan	Capti	ure-IR		TD:	I:1	
	о тск	4,12u	4.22u	4.12u	4.22u	4.12u	4.24u	4.12u	4.22u	4.12u	4.24u	4.12u	4.22u]
4 I	1 TM5	8	.34u	-	16.7	7u				-				
Itag bus	2 TDI			-				L		-		8.	34u]
	з тро											-4]
	4 TRE			-										
JT														
Label	Chanr 🔹													•
		Bus	Jtag bus(J	TAG)	-									
CH-01	CH-00 CH-00													
		state		Instr	uction re	g TD	I/TDO D	ata						
Sample	TAP			Instr	uction re	g TD	I/TDO D	ata						
Sample 921651	TAP Run	state	le	Instru	uction re	ig TD	I/TDO D	ata						
Sample 921651 925625	TAP Run Sel	state -Test/Idl	le can	Instr	uction re	ig TD	I/TDO D	ata						
Sample 921651 925625 926042	TAP Run Sel Sel	state -Test/Idl ect-DR-Sc	le can	Instr	uction re	:g TD	I/TDO D	ata						
Sample 921651 925625 926042 926460	TAP Run Sel Sel Cap	state -Test/Idl ect-DR-So ect-IR-So	le can	Instr	uction re	g TD		ata						
Sample 921651 925625 926042 926460 926877 928130	TAP Run Sel Sel Cap Shi	state -Test/IdJ ect-DR-So ect-IR-So ture-IR	le can	Instru	uction re			ata						
Sample 921651 925625 926042 926460 926877 928130	TAP Run Sel Sel Cap Shi Exi	state -Test/Idl ect-DR-So ect-IR-So ture-IR ft-IR	le can	Instr SCAN 1				ata						
Sample 921651 925625 926042 926460 926877	TAP Run Sel Sel Cap Shi Exi Upd	state -Test/Idl ect-DR-So ect-IR-So ture-IR ft-IR t1-IR	le can can					ata						

Waveform Window



Time/Div: 4 us Acquired: 08:00:0	0	.8us	511.2 us	51	7.6 us	524 us	5	30.4 us	536.8	us l.i	543.2 us	549.6	us 	
	Select-DR-Scan	Select-II	R-Scan		Test-Log	gic-Reset			Run-Te	est/Idle		Select-D	R-Scan	1
от	CK 4.12u	4.22u	4.12u	4.24u	4.12u	4.22u	4.12u	4.22u	4.12u	4.24u	4.12u	4.22u	4.12u	
Jtag bus	TMS							16.	7u					
2 T	DI													
зт	DQ													
4 T	RE											-		i
JIAG														
														Ŀ
													<u> </u>	1
CH-00 CH-00 CH-01 CH-00	RR Bus(Jtag bus(.	JTAG)	•										
Sample	TAP state		Instr	uction 1	reg T	DI/TDO D)ata							
-63	Run-Test/Idl													
153	Select-DR-So													
571	Select-IR-So													
988	Test-Logic-F													
23964 24799	Run-Test/Idl Select-DR-So													
25217	Select-IR-So													
25634	Test-Logic-H													-
1	ices hogie i											-		Ľ
							-10	60 ns 🧧		3.32 us	A B	3.48	us 🕒 🗍	i 111

The ARM7 Read IDCODE JTAG decode on the Waveform Window

Acute JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

#ID: Command list number; the range is 00 - FF and , MUST be entered in order or

will be seen as the end of commands.

#NAME: Command Name, 32 bytes most will be shown in the command list.

#LENGTH: Command length, unit in bits.

#CAPTURE: Command Capture Code, is stored in Instruction Register..

#INST: Command List, listed by Command Code and Command Name or will be

seen as the end of commands..

#TRST: Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

#BSDL: Load the BSDL file. Use the BSDL file as step 1-6.



Example:#ID:00

#NAME:ARM7-ARM9

#LENGTH:4

#CAPTURE:1

#INST:0, EXTEST

#INST:2, SCAN_N

#INST:3, SAMPLE/PRELOAD

#INST:4, RESTART

#INST:5, CLAMP

#INST:7, HIGHZ

#INST:9, CLAMPZ

#INST:C, INTEST

#INST:E, IDCODE

#INST:F, BYPASS

#INST:

#ID:01

#BSDL:C:\3256at144_1532.bsd



LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits: Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select (E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

Settings

LCD16	02 Settings 🛛 🗙
Channel	
	Channel RS CH 0 + DB7 CH 3 + DB3 CH 7 + RW CH 1 + DB6 CH 4 + DB2 CH 8 + E CH 2 + DB5 CH 5 + DB1 CH 9 + DB4 CH 6 + DB0 CH 10 +
	Data Mode
Color	
	Setting Commands Color
_	SCREEN CLEAR GRAM AD SET
	CURSOR RETURN DDRAM AD SET
	INPUT SET
	DISPLAY SWITCH 📃 🗸 DATA WRITE
	SHIFT 📃 💌 DATA READ 📃 💌
	BUSY/AD READ CT
Range	Decode Range
.	_
с - 1	From To Buffer Head
	Default OK Cancel

Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.



To merge the same command: Merge data with its command.

Result

Click **OK** to run the LCD1602 decode and see the result on the Waveform Window

below.

Time/Div: 40 us		💗 🧶 📮
Acquired: 08:00:00).0 -64 us	64 us 128 us 192 us 256 us 320 us 384 us
0 RS	Cursor Return 02	CGRAM/DDRAM Data Write:56 CGRAM/DDRAM Data Write:69 CGRAM/DDRAM Data Write:6F
1 RW		
2 E 3 DB7	,	61.5u 82.4u 61.4u 62.4u 61.5u
LCD1602 ⁴ DB6		371.5u
5 DB5 6 DB4		123.8u 247.7u
7 DB3 8 DB2		123.8u 123.8u
9 DB1	1	123.8u
LCD1602 10 DE	30	247.70
Label Char	nnel	
CH-00 CH-00 CH-00 CH-00	FLT ICD1602(LCD	01602)
Sample	Command	Data ASCII
-79875	Cursor Return	02 .
0	CGRAM/DDRAM Data Write	56 69 6F 3A 20 33 2E 33 38 20 56 20 20 20 20 20 Vio: 3.38 V
•		
		407.7 us 📕 6.912 ms 🛔 6.505 ms 🕒 🗍



LIN

The Local Interconnect Network (LIN) bus (version 2.1) has two message types: Header and Response.

- Header contains three data frames: Synchronization Break (Break),
 Synchronization Field (Sync) and Identifier Field (Identifier).
- (2) Response contains two data frames: Data Field (Data) and Checksum Field (Checksum). Checksum contains data and identifier (Enhanced mode), but version 1.3 or below (Classic mode) contains data only.

LIN bus has two states - Sleep mode and Active mode. While data is on the bus, all

LIN nodes are in active state; but after a specified timeout, the nodes enter Sleep mode and will be released back to active state by a WAKEUP frame.

Settings

LIN Sett	ings 🛛 🔀
Channel —	
1	Version C LIN 2.1 C LIN 2.0 C LIN 1.2
	Checksum mode Classic C Enhanced
	LA Channel CH 0 💽 🔽 Show scale
	Baud rate AUTO 💌 bps
Color —	
	Wake-up Break Synch Identifier Data Checksum
Range	Decode Range From Buffer Head To Buffer Tail
	Default OK Cancel



Version: Select LIN version.

Checksum Mode: Select Classic: data only or Enhanced: data and identifier.

LA Channel: Show the selected channel (CH0 for LIN).

Show Scale: Show scale on the waveform.

Baud rate: Show the selected baud rate.

Result

Click **OK** to run the Lin decode and see the result on the Waveform Window below.

Time/Div: 400 us		P					Ç.
Acquired: 08:00:0	0.0 2.6	42 ms 3.2	82 ms	3.922 ms 4.5	62 m s 5.202 m s 5.842 m	ns 6.482 ms	
LIN Bus O	Wakeup	Break	Syno		EA 88 48	i ri i	
Label							
CH-00 CH-00 CH-00 ⊙/Ⅲ CH-01 CH-00 CH-01 CH-00		(LIN)	•				
Sample	Event Type	PID(ID+P)	ID	Parity	Data	Checksum(h)	ASCII 🔺
2085	Wakeup						
5002	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	H?
18753	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?
28336	Diagnostic Frame	30	30	0	OO FF FF FF FF FF FF FF	00	
41253	Wakeup						
44170	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	H?
57921	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?
67504	Diagnostic Frame	30	30	0	OO FF FF FF FF FF FF FF	00	
80421	Wakeup						
83338	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	H?
97088	LIN Frame	25	25	0	31 B4 2C 3F	AE	1.,?
106672	Diagnostic Frame	30	30	0	OO FF FF FF FF FF FF FF	00	
119589	Wakeup						
122506	LIN Frame	B1	31	2	EA 8B 48 3F ED 9C B5 A7	1A	H? 🗸
•			_				
				2	3.445 ms 📕 28.688 ms	A B 5.242	ms 🕒 🔟 🕅



Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.



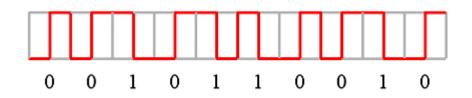
NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.



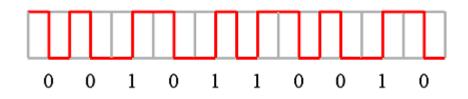
Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.

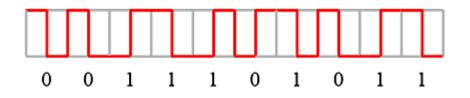




Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



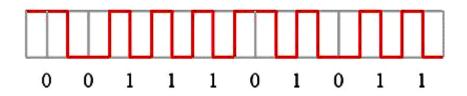
Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult. When



encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because

the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.

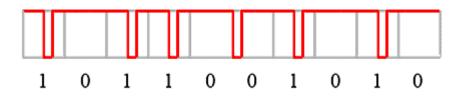


Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits



and synchronizing clock pulses which are output from the data separation circuit.

This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings

Line De	ecoding Settings			×
Select Deco	oding	Channel		
1	Select waveform format for decode. And set the parameters.	쁐	Data Channel CH 0	
	NRZI(Transition occurs for a one)	Range		
			Decode Range	
	1 1 0 1 0 0 1 1 0	₩ —•	From	
	Show Unknown Show Bus		Buffer Head	•
	🗹 Auto-Detect Data Rate		То	
	Data Rate 1 MHz		Buffer Tail	-
			ОК	Cancel

Select Decoding: Select the line code you want to decode.

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate

is not selected.

Channel: Show the selected channel (CH 0).

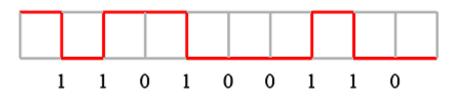
Range: Select the range within the waveform you want to decode.



Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

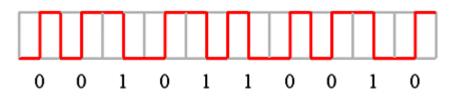


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.



Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

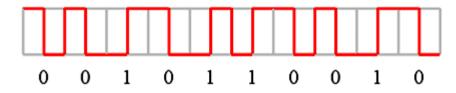
Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.





Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by

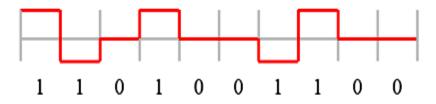
high-to-low transition.



Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit, i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.

AMI (Alternate Mark Inversion): There are four modes:

AMI (Standard): AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.

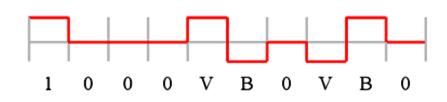


AMI (B8ZS): Bipolar-8-Zero Substitution

If 1 is +, 00000000 is represented to 000+-0-+

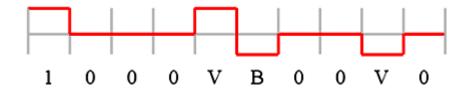
1 is -, 00000000 is represented to 000-+0+-

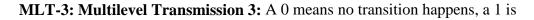




AMI (HDB3): High Density Bipolar 3

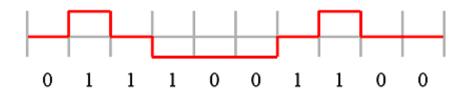
The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.







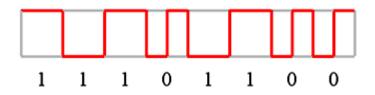
represented by a transition (0, +, 0, -).



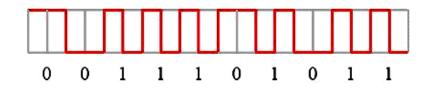
Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).



CMI (Coded Mark Inversion): A zero is sent a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.



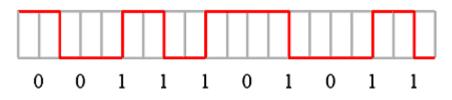


Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

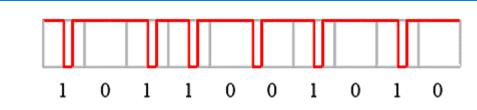
Delay encoding is used primarily for encoding radio signals because

the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit. This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:





Settings

Line Encoding Settings			×
Select Encoding	Channel		
NRZI(Transition occurs for a one)	뿂	Data Channel	сно т
	Range		
1 1 0 1 0 0 1 1 0	: ##:	Decode Range	
	* *	From	
🔽 Auto-Detect Data Rate		Buffer Head	
Data Rate 1 MHz		To Buffer Tail	
		·	
			OK Cancel

Select Encoding: Select the line code you want to encode.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Date Rate

is not selected.

Channel: Show the selected channel (CH 0).

Range: Select the range within the waveforms you want to encode.



Lissajous

Add a Lissajous decode: The Virtual Waveform Generator, only available when no instrument is connected to your PC, can generate sine waves to form a Lissajous graph. Click Virtual Waveform Generator from the Device menu or click Virtual Waveform Generator button on the Toolbar to show the dialog box below.

Virtual W	aveform Ge	nerator	×
Channel:	Item:	Frequency:	
CHO - CH7	Sine	20	MHz
CH8 - CH15	Sine	20	MHz
CH16 - CH23	Down Counter 💌	18	MHz
CH24 - CH31	Random data 💌	17	MHz
CH32 - CH39	Random data 🖉	16	MHz
CH40 - CH47	Down Counter 💌	15	MHz
CH48 - CH55	Random data 🖉	14	MHz
CH56 - CH63	Up Counter 🔄	13	MHz
	<u></u>	Cancel Del	fault

Set parameters like Item (Sine, ..., Up Counter) and Frequency (20MHz, ..., 13MHz). Note: CH0 and CH8 are the least significant bits (LSB), CH7 and CH15 are the most significant bits (MSB).

Combine the eight labels (CH0-CH7/CH8-CH17) to form a Sine wave bus and enter a new name (X/Y), then double click on the label name (X/Y) to show the Label Settings dialog box below.



Label Settin	rgs	×
Label Name		
<mark>∕</mark> ■	Enter a label name with 31 characters or less	
Channel		
онз <mark>ли</mark> онз <mark>ли</mark>	Set the channel number, value type and color	
CH8 JU	Channel Number Value Type	
	7 Value(2' Comp.)	•
	Color Aqua	•
Waveform -	Waveform parameter settings	
	Invert Gray Code Display the waveforms with decode	
	LA Advance	2
	OK Cano	:el

Set more parameters for Sine waves X/Y like Value Type (2' Comp), Color (Aqua)

		Ę	J								
x	70	*****	\wedge	\bigwedge	\bigvee	\bigvee	\bigvee	\bigwedge	$\bigvee \land$	\bigwedge	<u> </u>
Y	158	x	\bigvee	\bigvee	\bigvee	\bigwedge	\mathbb{N}	\mathbb{N}	\bigvee	\bigwedge	\mathbb{N}
Label	Channel V	alue Trigger									•
Label		aiue ji rigger					0 <mark>A</mark> B		0 <mark>A</mark> B		• • •

and click OK to generate the sine waves below.

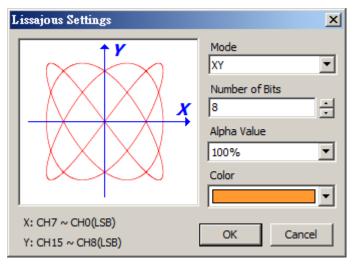
Click Add Bus Decode in the Label menu to show the dialog box below.



Add Bus D	ecode 🔀
Bus Name	
/모	Enter a label name with 31 characters or less
	Lissajous
Color	
CH3 11 CH5 11 CH5 11	Select the waveform color
Parameter	
OW	Select a decode type and click the Advance button to set more parameters
<u> </u>	Lissajous Advance
	Display the waveforms with decode
	OK Cancel

Select Lissajous in Parameter and click Advance to show the dialog box below.

Settings



Mode: Set the mode for the axis (XY or IQ).

Number of Bits: Set the number of data bits (8).

Alpha Value: The higher, the less transparent for the Lissajous graph on the

Waveform Window.

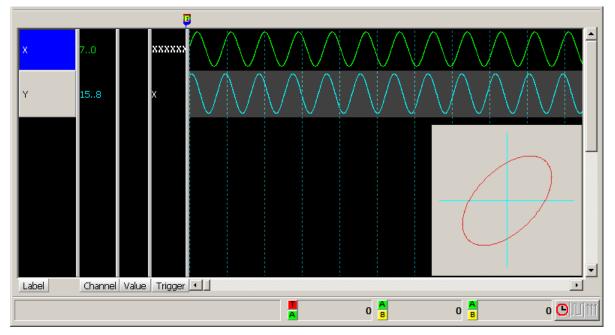
Color: Set the color for the Lissajous graph.

Result



Click **OK** to see the Lissajous graph on the lower-right corner of the Waveform

Window.



Right-click the Lissajous graph to show the dialog box below.

Close Properties...

Close: Close the Lissajous graph.

Properties: Return to the Lissajous Settings.



Low Pin Count (LPC)

The LPC bus, for the data transmissions, was developed by Intel to replace the ISA bus.

Settings

LPC Settings	X
Channel	
LFRAME# CH 1 CH LAD[2] CH 4 CLLK CH 0 LAD[0] CH 2 LAD[3] CH 5 Data Edge Falling U LAD[1] CH 3 CH 5	
Show the field in report	-
✓ START ✓ CYCLETYPE+DIR ✓ SIZE ✓ TAR	-
Color	
START ADDR CYCTYPE+DIR DATA CHANNEL SYNC TAR IDSEL SIZE/MSIZE STOP	▼ ▼ ▼ ▼
Range	
Decode Range From To Buffer Head V Buffer Tail V	
Default Cano	:el

Channel: Show the selected channels.

LFRAME#: Frame indicator.

LAD[0-3]: Data bits.

LCLK: Clock.

Filter the data in the report window: You can filter the data in the Report Window.



Result

Click **OK** to run the LPC decode and see the result on the Waveform Window below.

I/O Read Cycle.

Time/Div: 30 n Acquired: 08:0	· · · · · · · · · · · · · · · · · · ·	50.05	100 m	150	105	200.05	250.05	-	100 ns	350 ns		P
Acquired: 00:0	u:uu.u I.I.¥.	50 ns			1. 	1.1.1.1						
		START	I/O Rd	ADDR	0064		TAR	\$YNC:	6 ¹ \$YNC: 6	SYNC: 6	\$YNC: 6	11
	0 LCLK 15n 15n	15n 15n 15n	15n 15n 15n :	l5n 15n 15n	15n 15n 1	5n 15n 15n	15n 15n 15	n 15n 15	n 15n 15n	15n 15n	15n 15n 1	G
	1 LFRAME	25n								-		
LPC Bus	2 LAD[0]		180n			55n						
	3 LAD[1]		120n	25n	35n				-			
	4 LAD[2]		120n						_			
			12011 180n									
LPC	5 LAD[3]		180n			55n						
			i i		i i	i			1		1	.
Label	Channel 💶 📘											1
CH-00 CH		C D (1 D C)										
CH-01 CH-01		C BUS(LPC)	•									
Sample	Field	#Clocks	LAD	Comment								
6	START	1	0	Used for	Memory (or I/O or	DMA cycl	es.				
12	CYCLETYPE+DIR	1	0	I/O Read								
18	ADDR	4	0064									
42	TAR	2	FF									
54	SYNC	1	6	Long Wai								
60	SYNC	1	6	Long Wai								
66	SYNC	1	6	Long Wai								
72	SYNC	1	6	Long Wai								
78	SYNC	1	6	Long Wai								
84	SYNC	1	6	Long Wai								
90	SYNC	1	6	Long Wai								
96	SYNC	1	6	Long Wai								
102	SYNC	1	6	Long Wai								
109	SYNC	1	6	Long Wai	t							
•												·
					-		-					-
					2	29.24 us	22	29.24 us	s A		o 🕒 🛛	[]][[]
							_		-			-

Memory Read Cycle

Time/Div: 30 ns	s 📮												8
Acquired: 08:00	0:00.0	270 ns	320 ns	370 ns	420 ns		470 ns	520) ns	570 ns		620 ns	
		ADDR: FFFFFF0	1	TAR				SYNC: 6				SYNC: 6	
	0 LCLK	15n 15n 15n 15r	15n 15n 15n	15n 15n 15n	15n 15n	15n 15n	15n 15n	15n 15n	15n 15n	15n 15n	15n 15n	15n 15n	
	1 LFRAME												
LPC Bus	2 LAD[0]	30	n 55n										
	3 LAD[1]	30			-								
									1 1 1	: : :		• •	
	4 LAD[2]	30											
LPC	5 LAD[3]	30	n 55n		-				1 1 1	-		1	-
Label		•				•						•	
												<u></u>	-
⊘/Ⅲ CH-00 CH CH-01 CH		LPC Bus(LPC)	-										
		-		a .									-
Sample	Field	#Clocks	LAD	Comment									
20 68	ADDR TAR	8	FFFFFFF0 FF										
68 80	SYNC	1	6	Long Wait									
86	SYNC	1	6	Long Wait									
92	SYNC	1	6	Long Walt									
98	SYNC	1	6	Long Wait									
104	SYNC	1	6	Long Wait									
110	SYNC	1	6	Long Wait									
116	SYNC	1	6	Long Wait									
122	SYNC	1	6	Long Wait									
128	SYNC	1	6	Long Wait									
134	SYNC	1	6	Long Wait									
140	SYNC	1	6	Long Wait									
146	SYNC	1	6	Long Wait									-
) • [1
					1	1.014 n	ıs <mark>B</mark>	1.0	L4 ms	A. B		0 <mark>()</mark>]]	5 111



Line Printer Terminal Port (LPT)

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals. This decode only support EPP Mode.

LPT(EPP) Setting
Channel	Color
Data0(LSB) CH 1	Read Address
Data[7:0] => CH[8:1]	Write Address
/nWrite CH 0 ·	Read Data
/nWait CH 10 •	Write Data
/nDStrb CH 13	
/nAStrb CH 16	Range
	Decoded Range
	From Buffer Head
Address Table Report	To Buffer Tail
	Default Cancel

Settings

Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other channel will be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

/nAStrb: Indicates the address cycle.

/nInit: Indicates a termination cycle in order to return the interface to the

Compatibility mode. User can option to use this channel or not.



/nIntr: This is an interrupt signal. User can option to use this channel or not.

Result

Click OK to run the LPT Decode and see result on the Waveform Windows below.

Time/Div: 60 ns	7													(
Acquired: 15:23:2	.9	06.45 us -60	06.35 us	-6	06.25 us	s -6	506.15 us	s -6	506.05 u	s -6	05.95 u	s -	505.85 us	
			_		- 1	-		:85			_	1	LE	<u> </u>
	<u>к</u>		n i	R/D:64		IDLE	K/U	1	IDLE	, к	/D 88	1		
		165 ns 165 ns		_	165	ns			0 ns 0 ns		_	165 n	5	
							335 n	5	<u>, , , , , , , , , , , , , , , , , , , </u>					
		165 ns	,				335 n	5				-		
LPT 1,2,3,4,5,6			3	0 ns					1	335	ns			
					165	ns								
						_								_
			ns	65 n		105 ns	6		100		65 ns		0 ns	
	6	5 ns 100 r	15	<u>65 ns</u>	10	5 ns	<u>60</u> r	15	105 ns	6	<u>ins</u>	100	ns _	
LPT														
Label Channel	•													Ľ
CH-00 CH-00 CH-00 CH-00	- FR	Bus LPT	(LPT)			-								
Sample	R/W	Addr/Data	DØ	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D1:
-121299	Read	Data	2B	64	85	88	BB	00	07	FF	F3			
-4	Write	Address	A5		_	_	_	_	_	_	_	_	_	_
108263 214850	Write Write	Address Address	F2 F6			_		_	_	_			_	
323117	Write	Address	FØ			_			_			_	_	
439491	Write	Address	A7			-	-	-	-	-	_	-	-	
557892	Write	Address	AB											
748212	Write	Data	5A	ØF	77	04								
813532	Read	Data	2B	64	05	88	BB	00	07	FF	F3			
•														
		_												
		A 1.84	73532	205 KH	z 📕	455	5.0718	89982	Hz 🔒	6	03.813	68724	19 Hz 🤇	Ше



M-Bus

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

Settings

MBus Settings		×
Color	Channel Master CH 0 Polarity Auto Slave CH 0 Polarity Auto Parity None Parity None Parity None MSB first MSB first Adv. report User can assign color for specific pattern. Start / Stop CI Field C Field C Field C Field Check Sum A Field Check Sum C Field C Field Check Sum C Field C Field	
Range	From To Buffer Head	
	Default OK Cancel	

Channel: Set the channel of the signal and Polarity.

Baud rate: Set the specific data rate or auto detection.

Parity: Error detection.

MSB first: Set MSB format.

Adv. Report: Advanced report.



Result

	16.228	.915 5	3.916 \$	3.918 \$	3.92 \$ 3.921 \$	3.923 \$ 3.924 \$ 3.926 \$ 3.928 \$ 3.929 \$	3.9	31 S
M bus 0 I	Master X	L: 04h	L: 04h S: 68h	C: 53h	A: FEh CI: Soh D: 10h C	S: 범위, E <mark>Stop: 16h S: E5h S: 58h L: 13h L: 13h S: 68h C: 08l</mark> 월 전 전 전 전 전 전 전 전 전 전 전 전 전 전 전 전 전 전 전		
Label C	hannel Tri •		: :	:	: : :		:	•
						2		-
Э/Ш Сн-00 Сн-00	AR III Dest	M DUS(I	IBus) 💌					
Timestamp	Telegram Format	L	C Field(h)	A	CI Field(h)	User Data(h)	c	In
3.913347075 S	Long Frame	04	SND_UD(53)	FE	Application reset(50)	10	B1	
3.92376468 S	Single Character							
	Single Character Long Frame	13	RSP_UD(08)	05	Fixed data respond(73	78, 56, 34, 12, 0A, 00, E9, 7E		
3.92480644 S		13	RSP_UD(08)	05	Fixed data respond(73	78, 56, 34, 12, 0A, 00, E9, 7E 01, 00, 00, 00, 35, 01, 00, 00		
3.92376468 S 3.92480644 S 3.92480644 S 3.92480644 S		13	RSP_UD(08)	05	Fixed data respond(73		3C	
3.92480644 S 3.92480644 S 3.92480644 S		13 1F	RSP_UD(08) RSP_UD(08)	05			зc	
3.92480644 S 3.92480644 S 3.92480644 S 3.95085045 S	Long Frame		- · ·			01, 00, 00, 00, 35, 01, 00, 00	3C	
3.92480644 S 3.92480644 S	Long Frame		- · ·			01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07		
3.92480644 S 3.92480644 S 3.92480644 S 3.95085045 S 3.95085045 S 3.95085045 S	Long Frame Long Frame		- · ·			01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 15, 31	18	
3.92480644 S 3.92480644 S 3.92480644 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.98085045 S	Long Frame	1F 06	- · ·		Variable data respond Data send(51)	01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 15, 31 00, DA, 02, 3B, 13, 01, 8B, 60 04, 37, 18, 02 01, 7A, 08		
3.92480644 S 3.92480644 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.98939559 S 4.001896715 S	Long Frame Long Frame	1F	RSP_UD (08)	02	Variable data respond	01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 15, 31 00, DA, 02, 38, 13, 01, 88, 60 04, 37, 18, 02 01, 7A, 08 07, 79, 04, 03, 02, 01, 24, 40	18 25	
3.92480644 S 3.92480644 S 3.92480644 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.96085045 S 3.96085045 S 4.001896715 S	Long Frame Long Frame Long Frame Long Frame	1F 06 0D	RSP_UD(08) SND_UD(53) SND_UD(53)	02 FE FE	Variable data respond Data send(51) Data send(51)	01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 15, 31 00, DA, 02, 3B, 13, 01, 8B, 60 04, 37, 18, 02 01, 7A, 08 07, 79, 04, 03, 02, 01, 24, 40 01, 04	18	
3.92480644 S 3.92480644 S 3.92480644 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.98085045 S 3.980939559 S 4.001896715 S	Long Frame Long Frame Long Frame	1F 06	RSP_UD(08) SND_UD(53)	02 FE	Variable data respond Data send(51)	01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 15, 31 00, DA, 02, 38, 13, 01, 88, 60 04, 37, 18, 02 01, 7A, 08 07, 79, 04, 03, 02, 01, 24, 40	18 25	
3.92480644 S 3.92480644 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.95085045 S 3.9809559 S 4.001896715 S	Long Frame Long Frame Long Frame Long Frame	1F 06 0D	RSP_UD(08) SND_UD(53) SND_UD(53)	02 FE FE	Variable data respond Data send(51) Data send(51)	01, 00, 00, 00, 35, 01, 00, 00 78, 56, 34, 12, 24, 40, 01, 07 55, 00, 00, 00, 03, 13, 15, 31 00, DA, 02, 3B, 13, 01, 8B, 60 04, 37, 18, 02 01, 7A, 08 07, 79, 04, 03, 02, 01, 24, 40 01, 04	18 25	



Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR, OR,NAND, NOR, XNOR operation for the channel or combined channels.

ttings		
ath Settings		×
Channel Settings Waveform Settings Case Settings		,
Setting	Math List: A + B	
Operand 1:	A XOR B (A + B) + (A XOR B)	
B		
+ =	1	
Operand 2:		
В		
	Add List Item to Operand	Delete List Item
]	OK Cancel
ath Settings		×
Channel Settings Waveform Settings Case Settings		
Math List:	-	
A + B		
A XOR B (A + B) + (A XOR B)		•
	Range	
	Calculational Range	
		To
	Buffer Head	Buffer Tail
	[OK Cancel
ath Settings		>
Channel Settings Waveform Settings Case Settings		
Math List:	Case Color	
A + B A XOR B		
(A + B) + (A XOR B)		
	Calculational Result	
	=	00h
	Color	
		_
1		



Operand: Select the channel(s) in the waveform window.

"+": Select "+", "-", "X", "/", "AND", "XOR", "OR", "NAND", "NOR", "XNOR" operator.

"=": Add operation type.

Add List Item to Operand: Add operation type to operand.

Delete List Item: Delete operation type from the list.

Color: Set the colors for the data bits.

Range: Select the range within the waveform you want to decode.

Case Settings: Select condition and frame color.

Acquired: 10:20):09.0		160.67 L	IS .	162.27 u	5	163.87	7 us	165.47 us	167	.07 us	168.67	us 1	70.27 us	171	l.87 us	
B	40 5	1	2	3	4		4	5 3.99	6 95u	7	9 1.005u	9 995n	B 1.005u	В 995n	D	D 995n	
	7,6					_			2							<u>χ</u> 1	
D	8							5.005u									
E	119	2)	3	(0							
F	1512			D		X	1 }	(2)	(3)	4	χ <u>5</u>	Х 6	χ 7) s) <u> </u>) A	
																	Ŀ
Label	Channel 上															F	1
Э/Ш <u>Сн-00</u> Сн-	AA 00-	Bus	A(Math))		-											
CH-OT CH-		~~~~		, 													
Sample	À + B	<u>~~~</u>		,		_											
Sample 31801	A + B 1			, 													
Sample 31801 32000	A + B 1 2	<u>~_~</u>		,													
Sample 31801 32000 32200	A + B 1 2 4			, 		_											
Sample 31801 32000 32200 32202	A + B 1 2 4 3					_											
Sample 31801 32000 32200 32202 32400	À + B 1 2 4 3 4 4																
Sample 31801 32000 32200 32202 32400 32599	À + B 1 2 4 3 4 8					_											
Sample 31801 32200 32200 32202 32400 32599 32600	A + B 1 2 4 3 4 8 7																
Sample 31801 32200 32202 32400 32599 32600 32602	A + B 1 2 4 3 4 8 7 4																
Sample 31801 32200 32202 32400 32599 32600 32602 32602 32800	A + B 1 2 4 3 4 8 7 4 5																
Sample 31801 32000 32202 32400 32599 32600 32602 32600 33800	A + B 1 2 4 3 4 8 7 4 5 7																
Sample 31801 32200 32202 32400 32599 32600 32602 32800 33000 33003	A + B 1 2 4 3 4 5 7 6																
Sample 31801 32000 32200 32202 32400 32599 32600 32602 32800 33000 33003	A + B 1 2 4 3 4 8 7 4 5 7																
	A + B 1 2 4 3 4 5 7 6															<u> </u>	

Result

Note: When the Math settings are finished, the settings will always be saved as an independent text file named as AqMath.txt, different from the waveform file, at work directory unless other name assigned. If you need the specific Math settings, please save it, so you can reload the settings next time you open the specific waveform file.



Mobile Display Digital Interface (MDDI)

The Mobile Display Digital Interface (MDDI) is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link for connecting portable computing, communication, and entertainment devices to wearable micro displays. This decoder is based on VESA Mobile Display Digital Interface Standard Version 1.2, only Type I communication is supported in this decoder.

1. MDDI Parameter Settings

MDDI Set	ttings			
Channel :	Settings	CH 2 •	○ MDDI D0 + ◎ MDDI D0 - CH 0 →	_
Color —				-
	Packet Length		▼	
	Packet Header			
	Packet Data		▼	
Range -				_
2	Decode Range			
	From		То	
	Buffer Head	▼	Buffer Tail	
			Default OK Cancel	

Channel Settings

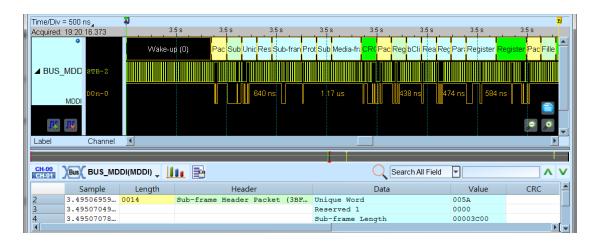
MDDI STB: MDDI Strobe MDDI D0+/-: MDDI Data 0 +/-

Configure the Channel setup for the decoder, and choose the data source



from Data 0+ or Data 0-.

2. Result





MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

Settings

MDI) Settings					? ×
Setting	Channel			Color		
7	Management Data C	lock (MDC)	сно -		Preamble (PRE)	
	Management Data Ir	put/Output (MDIO)	СН 1 .		Start of Frame (ST)	
					OP Code (OP)	
	Preamble				PHY Address (PHYADR)	
	32		▼ Bit		Register Address (REGADR)	
	Data				Turnaround (TA)	
	Data Edge	Rising	C Falling		DeviceType (DEVTYPE)	
Range					Address (ADDR)	
	Decode Range				Data (DATA)	
	From	Buffer Head	•			
	То	Buffer Tail	-			
					Default	OK Cancel

MDC: Clock.

MDIO: Data Input / Output.

Preamble: Set the MDIO preamble width, 32 bit default.

Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising Edge

default.

Result

Click \mathbf{OK} to run the MDIO decode and see the result on the Waveform Window

below.



Time/Div: 1 us	Ģ						9
Acquired: 08:00:0	0 8.26	us 9.86 us	11.46 us	13.06 us 14.66 us	16.26 us	17.86 us 19.46 us	
	Pr	eamble	PHYAC	<mark>PR: 05</mark> REGADR: 04 TA	C	DATA: 5446 Tole	•
Clk 0 MD							
1 MD.	IC		640n 960n	640ri 800ri	640h	960n 960n 480n	
							-
Label Char	nne 💶					•	
O/TT CH-00 CH-00 CH-01 CH-00 CH-00	RA Nex C	ik(MDIO)	•				
Sample	ST	OP	PHYADR	REGADR	DATA		^
10	Clause22	Read	05	04	DATA: 5446		
							-1
•						►	
				_	T		
				A 24.18 us	<mark>8</mark> 24.74 נ	ıs 🔒 560 ns 🕒 🔲	



MHL-CBUS

Mobile High-definition Link (MHL) is an HD audio and video interface, Control Bus (CBUS) is used to control it.

Settings

CBUS	Settings			×
Channel	Channel CBUS CH 0	Color	Setting transmitter's SYNC	
Range	Decode Range From Buffer Head To Buffer Tail		cPacketdPacketCMD / DATAPARITYACKArbitration	
		[Default OK Ca	ancel

LA Channel: Show the selected channel (CH0).

Result

Click OK to run the MHL-CBUS Decode and see result on the Waveform Window

below.



'ime/Div: 2.5 us .cquired: 14:17:0	9.0	200.25 us	204.25 us 208.25 us 212.2	5 us 216.25 us 220.25 us	224.25 us 228.25 us
CBUS	•	1.10	4.4u 1.55u 1.1u 1.1u	J.10	97.10
Bus 1	0 MHL-CI	Idle	Idle SYNC DDC(00)	ACK(33)	Idle
BUS I MHL-CBUS		1.iu	4.4u 1.55u 1.1u 1.1		97.1u
Label	Channel 🔳				
CH-00 CH-00 CH-01 CH-00	Bus Bus	Bus 1(MHL-CBU	S) 🔽		
Sample	Header	Ctrl	SRC Packet	SINK Packet	Information
447	DDC(00)	dPacket	Address: 74		
4126	DDC(00)	cPacket		ACK(33)	
6490	DDC (00)	dPacket	Offset: 08		-
10167	DDC (00)	cPacket		ACK(33)	
10959	DDC(00)	cPacket	SOF(30)		
12879	DDC(00)	dPacket	Address: 75		
13413	DDC(00)	cPacket		ACK(33)	
13947	DDC(00)	cPacket	CONT(50)		
16849	DDC(00)	dPacket		Data: F7	
19205	DDC(00)	cPacket	CONT(50)		
20105	DDC (00)	dPacket		Data: 30	
22460	DDC(00)	cPacket	STOP(51)		•
•					



MII/RMII

MII/RMII (Media Independent Interface/Reduced Media Independent Interface) is a protocol formulated by 802.3u that applied to Fast Ethernet, connecting MAC of Data Link Layer and PHY layer. Its clock frequency is either 25MHz or 2.5MHz (Ethernet); they are TX_CLK and RX_CLK. TX [0:3], RX [0:3] are 4-bit-width bus and TX_EN, RX_EN enable the IN/OUT; TX_ER, RX_ER can detect the errors on the bus; RX_DV inform bus the data received is valid or not; COL can detect the collision on the bus. Serial Management Interface (SMI), also known as MDIO, is also an important part of MII.

Settings

MII / RMII Settings		×
Setting		Color
- 0	only CLK and DATA pins used	
- Mode		Data 🗾 🗸
Transmit(Tx)		Error
C Receive(Rx)		Collision
C Duplex(Tx+Rx)		Idle
Transmit(Tx)	Receive(Rx)	
	RX_CLK CH 0	Preamble / SFD
TX_D0 CH 1	RX_D0 CH 1	Range
TX_D1 CH 2	RX_D1 CH 2	Decode Range
TX_D2 CH 3 + TX_D3 CH 4 +	RX_D2 CH 3	From
TX_D3 CH 4	RX_D3 CH 4	Buffer Head
TX_EN CH 5	RX_DV CH 5	To
TX_ER CH 6	RX_ER CH 6	Buffer Tail
Data	Report	
Data Edge	Data columns	
Rising O Falling	💿 8 Columns 🖸 16 Columns	
		Default OK Cancel



MII / RMII: Select the MII / RMII bus decode

GMII / RGMII: Select the GMII / RGMII bus decode

Only CLK and Data pins used(M/G): Select MII / GMII the CLK and Data pins

only.

Transmit (Tx): Select TX mode

Receive (Rx): Select Rx mode

Duplex (**Tx**+**Rx**) : Select duplex mode

Channel: Set the channel number.

Rising: Select rising edge to latch data

Falling: Select falling edge to latch data

8 columns: show 8 columns data field in the report window

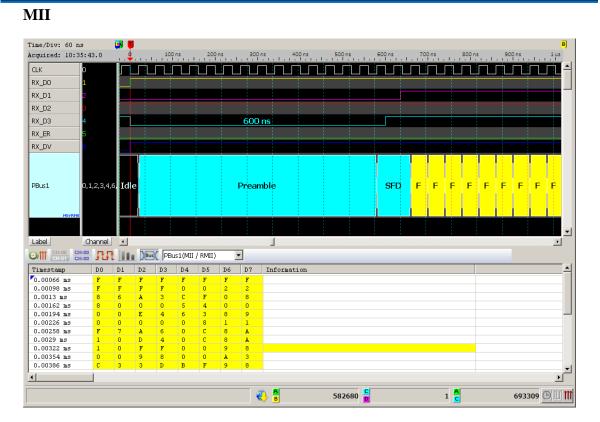
16 columns: show 16 columns data field in the report window

Result

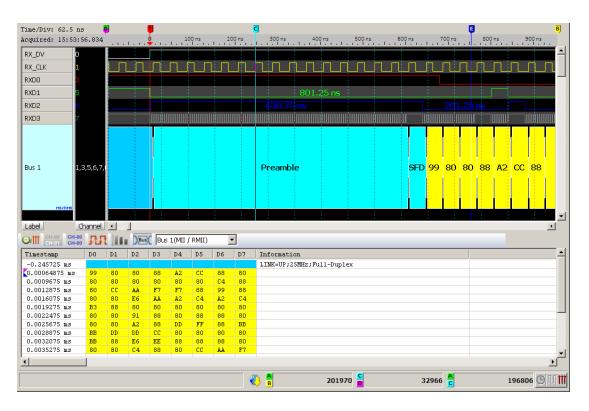
Click **OK** to run the MII/RMII decode and see the result on the Waveform Window

below.





RGMII





Microwire

The Microwire bus has four data bits: Chip Select (CS), Serial Clock (SK), Data Input (DI), and Data Output (DO).

Settings

MICROWI	RE Settings		×
Channel		Color	
	Channel Chip Select Channel (CS) Clock Channel (SK) Data In Channel (DI) Data Out Channel (DO) CH 3 CH 2 Data Chip Select Edge Chip Select Edge Ch		ERASE/WRITE ENABLE
	EEPROMs 93xx46A or 93xx46C, 8 Bits	Range	Decode Range From To
	Show data in report 8 Column		Buffer Head Buffer Tail Default Cancel

Channel: Show the selected channels.

Chip Select Edge: Active Low or Active High.

Data Edge: Rising or Falling.

EEPROMs: Select EEPROMs.

Report: Show data in report.

Result

Click **OK** to run the Microwire decode and see the result on the Waveform Window

below.

Read



Time/Div: 2.5 us Acquired: 08:00:00	7 0.0	3.981 ms	3.985 m	IS 1.1.	3.989 m	ns I.I.	3.993 r	ns 1.1.	3.997 n	15 1.I.	4.001 ms 4.00)5 ms	4.009 ms
Microwire 1 CLK 2 Data HIGROWIRE 3 Data	Select		A≠040 5u		3.3u	21		1 2.2u		3.8u		11 ЛИПИЛИ 7 10 Л 10	88 2.3u
CH-00 CH-00 CH-00 CH-00		Aicrowire(MICR)	OWIRE)	•									
Sample	Command	Address	DO	Dl	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)		
39765	Read	040	21	10	73	11	8B	DO	Al	5A	!.sZ		
40265			50	63	91	32	D8	F6	A8	E9	Pc.2		
40645			F9	FF	FF	FF	FF	FF	FF	FF			
41025			FF	FF	FF	FF	FF	FF	FF	FF			
41405			FF	FF	FF	FF	FF	FF	FF	FF			
41785			FF	FF	FF	FF	FF	FF	FF	FF			
42165			FF	FF	FF	FF	FF	FF	FF	FF			
•													Þ
						A		3.895	ms 📕	10	2.398 ms 🔒	98.503	ms 🕒 🔟

Write

Fime/Div: 1.2 u Acquired: 08:00		396.724 ms	396.726 ms	396.7	28 ms	396.73 m	is 39 i . l . i	6.732 ms	39 	96.734 ms	396.736 ms	396.738 n	ns
	nip Select	Write				A=06E					67		
Microwire 1 CL		ſ	חחח	пп	2.7u	Π		חחר	1	2.6u	ппп		
2 Da	ata In		1.4u		2.4u	7	00n	1u		2.4u	700n 600r		
MICROWIRE 3 Da	ata Out												
Label Ch	annel 💶											l	•
O/TT CH-00 CH CH-01 CH		Microwire(MI	ROWIRE)	-									
Sample	Command	Address	DO	D1 D	2 D3	D4	D5	D6	D7	ASCII(DO)-D7)		<u> </u>
3967220	Write	06E	67							g			
4002950	Write	06F	A8							•			
4038681 4074411	Write Write	070 071	2B D4							+			
4074411 4110142	Write	072	7E			-				•			
4145873	Write	072	1E										
4181603	Write	074	F2										-
•													▶
						_					-		
							3.895 r	ns 🚪	102	2.398 ms	A 98	.503 ms 🕒	



MIPI DSI

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

Settings

MIPI DS	I Settings
Channe	LP Mode Channel Dp Ch 0 + Dn Ch 1 + Mater -> Slave LP Mode Channel Data Lane 4 D0+ Ch 3 + D1+ Ch 4 + D0+ Ch 3 + D1+ Ch 4 + D0+ Ch 3 + D1+ Ch 4 + D1+ Ch 4 + D1+ Ch 4 + D2+ Ch 5 + D3+ Ch 6 + Mater -> Slave
Color -	
	Start of Transmission Word Count
	Transmission Mode Data Frame
	Escape Mode Action
	Data Identifier DCS Command
Range	
inn:	Decode Range
*	From To
	Buffer Head 💌 Buffer Tail 💌
	Default OK Cancel

Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines

Advanced Decode: Enable DSI format decode and display.

Show DCS Command: Enable DCS Command decode and display.



Always goes to HS Mode: Ignore the Dp and Dn status and decode all the data frame

in HS mode

Initial Bus Direction: Select the Initial direction of the bus transmission.

Result

Advanced Decode Disabled:

Time/Div: 2	2.56 us	1			Ţ														
Acquired: 1	16:55:26.0	-3.2 us			•		3.2	JS		6.4 us	9.6 	ius I	12.8 us		16 us	19.2 us		2.4 us	
MIPI DSI-LP:				(37 N N)5u	01		25u		1D	2.65u	08 1.85u	0F		0F 1.85u	01	Ĺ
Jahal	Char																		- -
Label	Chanr																		
⊙/∰ CH-00 CH-01	CH-00 CH-00	Busk M	IPI DS	SI-LP1	(MIP)	I DSI-	LP)	-											
Sample	Mode	Action	DO	D1	D2	D3	D4	D5	D6	D7									▲
-890	LP_ESC	LPDT	37	01	00	1D	08	OF	0F	01									
5230	LP_ESC	LPDT	06	0A	00	3F	80	OF	0F	01									
11350 11602	LP_BTA	LPDT	21	08	00														
12791	LP_ESC LP BTA	LPDI	21	08	00	37													
12/91	LP_DIA																		
																			_
•																			•
													32	078 <mark>A</mark> B		83 <mark>B</mark>		16	3 © 11

Advanced Decode Enabled:

	16:55:26.0	Ģ	2.05	32115 64115 6	6.05	12	8.05		16.	10	1	9.2		22.4		
	10:55:20.0	' . I . I .	1.1.1	3.2 us 6.4 us 5	1.1.1			. 1.,	1.11	° I	^	. 1 .	i <mark>l</mark> a 1		us 	
MIPI DSI-LI	P1 Dp	Idle				2.65	ſ	01 08 1.85		0₣	.85u		0F 1.8	354	ECC 01 3.05u	
					LIUL				μU			JUUL				
			.45u		1.45u				1.8	85u		1.85u	<u> </u>			
																-
Label	Ch	ann 💶 🗌														
	1 CH-00	LT Bus	MIPI D	SI-LP1(MIPI DSI-LP)												
				1												
Sample	Mode	Action	VC	DT	WC	DO	D1	D2	D3	D4	D5	D6	D7	ECC	CRC	·
-890	Mode LP_ESC	Action LPDT	VC 00	Set Maximum Return Packet Size (37)	WC	01	D1 00	D2	D3	D4	D5	D6	D7	1D	CRC	·
-890 2480	LP_ESC	LPDT	00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp)	WC	01 0F	00 0F	D2	D3	D4	D5	D6	D7	1D 01	CRC	
-890 2480 5230			00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06)	WC	01 0F 0A	00 0F 00	D2	D3	D4	D5	D6	D7	1D 01 3F	CRC	
-890 2480 5230 8600	LP_ESC	LPDT	00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp)	WC	01 0F	00 0F 00	D2	D3	D4	D5	D6	D7	1D 01	CRC	
-890 2480 5230 8600 11350	LP_ESC LP_ESC LP_BTA	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
Sample -890 2480 5230 8600 11350 11602	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT	00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06)	WC	01 0F 0A	00 0F 00	D2	D3	D4	D5	D6		1D 01 3F	CRC	
-890 2480 5230 8600 11350 11602	LP_ESC LP_ESC LP_BTA	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
-890 2480 5230 8600 11350 11602	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
-890 2480 5230 8600 11350	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
-890 2480 5230 8600 11350 11602	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
-890 2480 5230 8600 11350 11602	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
-890 2480 5230 8600 11350 11602 12791	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp)	WC	01 0F 0A 0F	00 0F 00 0F	D2	D3	D4	D5	D6		1D 01 3F 01	CRC	
-890 2480 5230 8600 11350 11602	LP_ESC LP_ESC LP_BTA LP_ESC	LPDT LPDT	00 00 00 00	Set Maximum Return Packet Size (37) End of Transmission packet (EoTp) DCS READ, no parameters (06) End of Transmission packet (EoTp) DCS Short READ Response, 1 byte r	WC	01 0F 0A 0F	00 0F 00 0F		D3	D4		D6		1D 01 3F 01		



MIPI RFFE

MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

Settings

MIPI RFFE Settings			×
Channel SCLK CH 0 : SDATA CH 1 :	Color SSC SA Command BC	Address Data P BP	
Range Decode Range From Buffer Head	To But	ffer Tail	
		Default OK	Cancel

Channel: Set the channels of SCLK and SDATA.

Result

	SSC	SA 4			Command: Re	g. Wr		Address 0	1
MIPI RFFE	sak	30 ns 30	ns	3	0 ns	30 r	s		30 ns
	SDATA 55 ns	100 ns 55 ns	15	5 ns	50 ns				
HEIMITE									
abel	Channel •								
				-					-
		PIRFE(MIPIRFE)							
ample	SA	Command	Byte Count	Address	Data	Information			
1778	Spare (user-defined)								
				1C	PM_TRIG(07)				
	Spare (user-defined)	Register Write Command		01	04				
117965	Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command	0	01 CF	04				
117965 118340	Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command	0	01	04 00 00				
117965 118340 118705	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register 0 Write Command		01 CF CC	04 00 00 02				
117965 118340 118705 118913	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register 0 Write Command Register Write Command		01 CF CC 1C	04 00 00 02 PM_TRIG(01)				
117694 117965 118340 118705 118913 119215	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register 0 Write Command Register Write Command Register Write Command		01 CF CC 1C 01	04 00 00 02 PM_TRIG(01) 48				
117965 118340 118705 118913 119215 119486	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register Write Command Register Write Command Register Write Command		01 CF CC 1C 01 1C	04 00 02 PM_TRIG(01) 48 PM_TRIG(07)				
117965 118340 118705 118913 119215 119486 133090	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register Write Command Register Write Command Register Write Command Register Write Command	0	01 CF CC 1C 01 1C 01	04 00 02 PM_TRIG(01) 48 PM_TRIG(07) 04				
117965 118340 118705 118913 119215 119486 133090 133361	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register 0 Write Command Register Write Command Register Write Command Register Write Command Extended Register Write Command	0	01 CF CC 1C 01 1C 01 CF	04 00 02 PM_TRIG(01) 48 PM_TRIG(07) 04 00				
117965 118340 118705 118913 119215 119486 133090 133361 133736	Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined) Spare (user-defined)	Register Wite Command Extended Register Wite Command Register 0 Wite Command Register 0 Wite Command Register Wite Command Register Wite Command Register Wite Command Extended Register Wite Command Extended Register Wite Command	0	01 CF CC 1C 01 1C 01	04 00 02 FM_TRIG(01) 48 FM_TRIG(07) 04 00 00				
117965 118340 118705 118913 119215 119486 133090 133361 133736 133736	Spare (user-defined) Spare (user-defined)	Register Write Command Extended Register Write Command Extended Register Write Command Register O Write Command Register Write Command Register Write Command Extended Register Write Command Extended Register Write Command Extended Register Write Command	0	01 CF CC 01 1C 01 CF CC	04 00 02 PM_TRIG(01) 48 PM_TRIG(07) 04 00 00 00 02				
17965 18340 18705 18913 19215 19486 33090 33361 33736	Spare (user-defined) Spare (user-defined)	Register Wite Command Extended Register Wite Command Register 0 Wite Command Register 0 Wite Command Register Wite Command Register Wite Command Register Wite Command Extended Register Wite Command Extended Register Wite Command	0	01 CF CC 1C 01 1C 01 CF	04 00 02 PM_TRIG(01) 48 PM_TRIG(07) 04 00 00				



MIPI SPMI

MIPI SPMI(System Power Management Interface) designed by MIPI alliance. SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

MIPI	SPMI Con	figuration	×
Channel		SDATA CH	
Color			
Start Start	—	SSC	— -
C-bit	—	Command Frame	-
A-bit	— –	Data Frame	— -
SR-bit	_	Parity bit	-
Master Arbitration	_	Bus Park	_
Slave Arbitration	—	No Response Frame	
Range			
Decoded Range			
From Buffer Head	▼ To	Buffer Tai	i 🔻
	Defaul	t OK	Cancel

Settings

Channel: Set the channels of SCLK and SDATA.

Result

Click OK to run the MIPI SPMI Decode and see result on the Waveform Windows below.



			BP	С0 А0	MPL3	
/IPI_SPM	NI SCLK		3	ð ns 30 ns 30 ns 30 ns	30 ns	30 ns 30 ns
	SDA'	r ⊨		310 ns		
	MIPLSPMI					
.abel	Cha	nne 🔹				•
			_			
	-00 CH-00 -01 CH-00	лл		Bus MIPI_SPMI(MIPI SPMI)		
a	C A	SR	Devi	Command(Hex)	Data	Data Frame(Hex)
22268	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	0F 00 FF F8
22269	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	03 07 08 F8
22270	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	35 52 32 F8
22271	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	32 32 36 F8
22271	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	34 2E 31 F8
22272	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	38 00 00 F8
22273	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	02 05 00 F8
22274	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	7041	80
22275	MPL3		SA=00	31 (Extended Register Write Long: 2Bytes)	7042	FC 07
22275	MPL3		SA=00	3B (Extended Register Read Long: 4Bytes)	704C	00 11 00 F8
22276	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	7040	00
22277	MPL3		SA=04	38 (Extended Register Read Long: 1Bytes)	7004	16
22278	MPL3		SA=04	30 (Extended Register Write Long: 1Bytes)	7040	80



MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC) version 5.0 is a flash memory card standard.

Settin	gs			
MMC	Settings			×
	Channel CLK CH 0 • Data3 CH 0 • CMD CH 1 • Data4 CH 0 • Data0 CH 0 • Data5 CH 0 • Data1 CH 0 • Data6 CH 0 • Data2 CH 0 • Data7 CH 0 • DQS CH 0 •	Analysis Command only Data only Command + Data Command + Data Adv. Report Don't care clock Data C 8-bit Data C 4-bit Data C 1-bit Data DDR mode Mon-interleaved Data Strobe	Color Start bit Host Device CMD/Resp CMD/Resp CRC check End bit Data CRC status	
Range	Data lengthBytes (Min: 1, Max: 16384) Decode Range From To Buffer Head To Buffer Tail		Busy	ncel

Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data

Command + Data: Analyze Command and Data in the report window.

Ref. DAT0: To help analyze the R1/R1b of the response.

Adv. Report: To analyze the command argument.

Don't care clock: To decode only depend on the CMD channel without the CLK

channel.

Data: 1/4/8 bits or DDR mode, check "DDR mode" and " "Non-interleaved" to

analyze data without interleaved. Check "Data Strobe" to analyze data with the DQS channel.



Data length: Set the number of data bits.

Result

Command:

.cquired: 14:27:25.2	-1.35160	05 ms -1.351505 ms -1.351405 n	ns -1.35 <mark>1</mark> 305 ms	-1.351205 ms	-1.351105 ms	-1.351005 ms	-1.350905 ms	9
	Idle	CMD16:SET_BLOCKLEN		Data			Data:00h	1
MMC O Clock	101010		0101010	1010	10101	010101	010101	
1 Command	1 0	1 0 1						
Label Channel	•						Þ	
3) 111 CH-00 CH-00 CH-00		C(MMC)						
Timestamp Command		Response	Argument (h)	CRC7 (h)	Frequency	Timing	Information	- 🛋
					riequency	TIMITIE	Information	
-0.0013		R1 :CMD13:SEND_STATUS	00 00 09 00	1F	26MHz	Ncr: 5	Information	
	SET_BLOCKLEN	R1 :CMD13:SEND_STATUS		1F 0A			Información	
-0.0013 -0.0013 CMD16: -0.0013	SET_BLOCKLEN	R1 :CMD13:SEND_STATUS R1 :CMD16:SET_BLOCKLEN	00 00 09 00		26MHz	Ncr: 5	Información	
-0.0013 CMD16: -0.0013 -0.0012 CMD08:	SET_BLOCKLEN	R1 :CMD16:SET_BLOCKLEN	00 00 09 00 00 00 02 00	0A 05 61	26MHz 25MHz 26MHz 26MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0012	_ SEND_EXT_CSD	_	00 00 09 00 00 00 02 00 00 00 09 00 00 00 09 00 00 00 09 00 00 00 09 00 00 00 00 00 00 00 00 00 00 00	0A 05 61 78	26MHz 25MHz 26MHz 26MHz 26MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Ncr: 5		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0012 -0.0000 CMD06:	_ SEND_EXT_CSD	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD	00 00 09 00 00 00 02 00 00 00 02 00 00 00 09 00 00 00 00 00 00 00 00 00 00 00 09 00 00 00 09 00 03 B9 01 00	0A 05 61 78 17	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Ncr: 5 Nrc: 5 Nrc > 4095		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0012 -0.0000 CMD06: 0.00000	_ SEND_EXT_CSD SWITCH	R1 :CMD16:SET_BLOCKLEN	00 00 09 00 00 00 02 00 00 00 09 00 00 00 09 00 00 00 00 00 00 00 00 00 00 00 09 00 00 00 09 00 00 00 00 00 00 00 08 00	0A 05 61 78 17 65	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Ncr: 5 Nrc > 4095 Ncr: 5		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0012 -0.0000 CMD06: 0.00001 CMD13:	_ SEND_EXT_CSD	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD R1b:CMD6:SWITCH	00 00 09 00 00 00 02 00 00 00 09 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 09 00 00 00 09 00 00 00 09 00 00 00 00 00 00 01 00 00	0A 05 61 78 17 65 29	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Ncr: 5 Nrc > 4095 Ncr: 5 Nrc: 1329		
-0.0013 CMD16: -0.0013 CMD08: -0.0012 CMD08: -0.0000 CMD06: 0.00000 CMD13: 0.00011 CMD13:	SEND_EXT_CSD SWITCH SEND_STATUS	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD	00 00 09 00 00 00 02 00 00 00 09 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 09 00 03 B9 01 00 00 08 00 00 01 00 00 00 00 09 00	0A 05 61 78 17 65 29 1F	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Nrc: 5 Nrc: 4095 Ncr: 5 Nrc: 1329 Ncr: 5		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0012 -0.0000 CMD06: 0.00001 CMD13: 0.00011 0.00011	_ SEND_EXT_CSD SWITCH	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD R1b:CMD6:SWITCH R1 :CMD13:SEND_STATUS	00 00 09 00 00 00 02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00	0A 05 61 78 17 65 29 1F 46	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 52MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Nrc: 5 Nrc > 4095 Nrc: 5 Nrc: 1329 Ncr: 5 Nrc: 21		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0002 -0.00000 0.00000 0.00011 CMD13: 0.00011 CMD19: 0.00110	SEND_EXT_CSD SWITCH SEND_STATUS BUSTEST_W	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD R1b:CMD6:SWITCH	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	0A 05 61 78 17 65 29 1F 46 5F	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 52MHz 52MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Nrc: 22 Nrc: 5 Nrc: 4095 Nrc: 5 Nrc: 1329 Nrc: 5 Nrc: 21 Nrc: 5		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0012 -0.00000 0.00000 0.00011 CMD13: 0.00011 0.00110 0.00110 0.00110	SEND_EXT_CSD SWITCH SEND_STATUS	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD R1b:CMD6:SWITCH R1 :CMD13:SEND_STATUS	00 00 09 00 00 00 02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00	0A 05 61 78 17 65 29 1F 46	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 52MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Nrc: 5 Nrc > 4095 Nrc: 5 Nrc: 1329 Ncr: 5 Nrc: 21		
-0.0013 CMD16: -0.0013 -0.0012 CMD08: -0.0002 -0.00000 0.00000 0.00011 CMD13: 0.00011 CMD19: 0.00110	SEND_EXT_CSD SWITCH SEND_STATUS BUSTEST_W	R1 :CMD16:SET_BLOCKLEN R1 :CMD8:SEND_EXT_CSD R1b:CMD6:SWITCH R1 :CMD13:SEND_STATUS	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	0A 05 61 78 17 65 29 1F 46 5F	26MHz 25MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 26MHz 52MHz 52MHz	Ncr: 5 Nrc: 21 Ncr: 5 Nrc: 22 Nrc: 22 Nrc: 5 Nrc: 4095 Nrc: 5 Nrc: 1329 Nrc: 5 Nrc: 21 Nrc: 5		

Adv. Report:

TIME/D1	.v: 16 us 📴					
Acquire	ed: 14:25:38.0	266.388275 ms	266.439475 ms 266.490675 r	ms	266.54187	
MMC_C		CMD1:SEND_OP_COND	Data:40h Data:FCh	Data:(•
	CH-00 CH-00 RR 000					
5	Command	() () () () () () () () () ()				- 1
		Kesponse	Argument (h)	CRC7 (h)	Frequency	▲
5327		Response	Argument (h) 40 FC 00 00	CRC7 (h)	Frequency · 187KHz	^
5327	CMD01:SEND_OP_COND	R3 :Check bit(63)	Argument (h) 40 FC 00 00 00 FF 80 00	CRC7 (h) 27 7F	Frequency 187KHz 187KHz	<u> </u>
			40 FC 00 00	27	187KHz	^
5333			40 FC 00 00 00 FF 80 00	27	187KHz	•
5333 5333			40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK	27	187KHz	•
5333 5333 5333			40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode	27	187KHz	•
5333 5333 5333 5333	CMD01:SEND_OP_COND		40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card	27 7F	187KHz 187KHz	•
5333 5333 5333 5333 5333 5359 5364 5364	CMD01:SEND_OP_COND	R3 :Check bit(63)	40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card 40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK	27 7F 27	187KHz 187KHz 187KHz	•
5333 5333 5333 5333 5359 5364 5364 5364	CMD01:SEND_OP_COND	R3 :Check bit(63)	40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card 40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode	27 7F 27	187KHz 187KHz 187KHz	
5333) 5333) 5333) 5333) 5359 5364 5364 5364 5364 5364	CMD01:SEND_OP_COND CMD01:SEND_OP_COND	R3 :Check bit(63)	40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card 40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card	27 7F 27 7F	187KHz 187KHz 187KHz 187KHz	
5333 5333 5333 5333 5359 5364 5364 5364	CMD01:SEND_OP_COND	R3 :Check bit(63)	40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card 40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode	27 7F 27	187KHz 187KHz 187KHz	
5333) 5333) 5333) 5333) 5359 5364 5364 5364 5364 5364	CMD01:SEND_OP_COND CMD01:SEND_OP_COND	R3 :Check bit(63)	40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card 40 FC 00 00 00 FF 80 00 Bit[31] OCR register power up not OK Bit[30:29] Access mode: byte mode Bit[7] High voltage Multimedia card	27 7F 27 7F	187KHz 187KHz 187KHz 187KHz	•



Data:

	4 2.3749	45 ms	2.37497	5 ms	2.375005	oms III.	2.375035	ms I.I.	2.375065 n	ns 2.375095 ms	2.375125 ms	
	00h		45h		4	7h		00h		75h	00h	-
8 Clock	1	1	0 1	0	1 0	1 () 1	0 1	ø	1 0 1 0	1 0 1	0
9 Comman	d											
DATA 0 Data[0]	0		1	0		1	Ø)		1		
1 Data[1]			0			1	0		1		0	
2 Data[2]	0			1			6			1	0	-1
3 Data[3]				- I								
MMC S Data[S]												- 1
							1		:			•
Label Channel	•											•
CH-00 CH-00 CH-01 CH-00		🗙 Dat	A(MMC)		-							
Timestamp	State	D0(h)	D1(h)	D2(h)	D3(h)							
		00(11)	D1(I)	02(11)	D3(n)	D4(h)	D5(h)	D6(h)	D7(h)	Information		
	Data	72	74	ØD	0A	00	D5(h) 00	00	00	Information		4
0.113655 ms	Data Data											
0.113655 ms 0.11397 ms		72	74	ØD	0A	00	00	00	00	CRC16 OK!		
0.113655 ms 0.11397 ms 0.11435 ms	Data	72 00	74 AC	0D CB	0A D8	00 00	00 00	00 55	00 AA	CRC16 OK! CRC status: non-		
0.113655 ms 0.11397 ms 0.11435 ms 2.369365 ms	Data Data	72	74	ØD	0A	00	00	00	00 AA FF	CRC16 OK!		-
0.113655 ms 0.11397 ms 0.11435 ms 2.369365 ms 2.369685 ms	Data	72 00 42	74 AC 66	0D CB 00	0A D8 00	00 00 00	00 00 FF	00 55 FF	00 AA	CRC16 OK! CRC status: non-		
0.113655 ms 0.11397 ms 0.11435 ms 2.369365 ms 2.369685 ms 2.37 ms 2.37032 ms	Data Data Data	72 00 42 FF	74 AC 66 FF FF FF	0D CB 00 FF	0A D8 00 0F	00 00 00 00	00 00 FF 25	00 55 FF FF	00 AA FF FF	CRC16 OK! CRC status: non-		
0.113655 ms 0.11397 ms 0.11435 ms 2.369365 ms 2.369685 ms 2.37 ms 2.37082 ms 2.370635 ms	Data Data Data Data Data Data Data	72 00 42 FF FF FF 01	74 AC 66 FF FF FF 55	0D CB 00 FF FF 00 00	0A D8 00 0F FF 00 73	00 00 00 00 FF FF 00	00 00 FF 25 FF FF 65	00 55 FF FF FF FF 00	00 AA FF FF FF FF FF 72	CRC16 OK! CRC status: non-		
0.113335 ms 0.113655 ms 0.11397 ms 0.11435 ms 0.369365 ms 0.369365 ms 0.369685 ms 0.37 ms 0.370635 ms 0.370655 ms 0.37095 ms	Data Data Data Data Data Data Data Data	72 00 42 FF FF FF 01 00	74 AC 66 FF FF FF 55 20	0D CB 00 FF FF 00 00 00 00	0A D8 00 0F FF 00 73 0F	00 00 00 00 FF FF 00 00 00	00 00 FF 25 FF FF 65 25	00 55 FF FF FF FF 00 47	00 AA FF FF FF FF 72 00	CRC16 OK! CRC status: non-		
0.113655 ms 0.11397 ms 0.11435 ms 2.369365 ms 2.369685 ms 2.37082 ms 2.37032 ms 2.370635 ms 2.370635 ms 2.37095 ms 2.37127 ms	Data Data Data Data Data Data Data Data	72 00 42 FF FF FF 01 00 75	74 AC 66 FF FF FF 55 20 00	0D CB 00 FF FF 00 00 00 00 69	0A D8 00 0F FF 00 73 0F 00	00 00 00 00 FF FF 00 00 64	00 00 FF 25 FF FF 65 25 00	00 55 FF FF FF FF 00 47 65	00 AA FF FF FF FF 72 00 00	CRC16 OK! CRC status: non-		
0.113655 ms 0.11397 ms 0.11435 ms 2.369365 ms 2.369685 ms 2.37 ms 2.37032 ms 2.370635 ms 2.370635 ms 2.370955 ms	Data Data Data Data Data Data Data Data	72 00 42 FF FF FF 01 00	74 AC 66 FF FF FF 55 20	0D CB 00 FF FF 00 00 00 00	0A D8 00 0F FF 00 73 0F	00 00 00 00 FF FF 00 00 00	00 00 FF 25 FF FF 65 25	00 55 FF FF FF FF 00 47	00 AA FF FF FF FF 72 00	CRC16 OK! CRC status: non-		



ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

Settings

Modbus Settings	×
Setting	Color
Modbus (Tx) Modbus (Tx) Modbus (Rx) H 1 Transmission Mode ASCII Protocol Setting Polarity Baud Rate Auto Parity None Show scale in the waveform MSB First LRC Check	Header
Range Decode Range From To Buffer Head I	
	Default OK Cancel

Channel: Modbus (Tx) or Modbus (Rx).

Transmission Mode: ASCII and RTU mode.

Auto: Auto detection idle polarity.

Idle high: Idle condition shows High.



Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Parity: N-None Parity, O-Odd Parity, E-Even Parity.

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Display the waveforms with scales.

Result

Acquired: 15:03:2	1.0 51.42	us 51.52 us	51.62 us	51.72 us 51.82 us 51.92 us	52.02 us	52.12 us
T., 0.M-	Idle	Start	Data: 7F	Stop	Break	
Tx O Mo	abus					
Rx 1 Mo	Break		Start	Data: 7F	Stop	Idle
Madbur						-
Label Cha		;			i i	
	nnel 💶			<u> </u>		
CH-00 CH-01 CH-00		1odbus)	•			
Timestamp	Field	Parity	ASCII	Information		^
-0.000495 ms	Data: 7E		~	Data Rate: 33.333 Mbps		
-0.00058 ms	Data: 7F			(Rx)		
0.05148 ms	Data: 7F					
0.05157 ms	Data: 7F			(Rx)		
0.10365 ms	Data: 7E		~			
0.103565 ms	Data: 7F			(Rx)		
0.15563 ms	Data: 7F					
0.15572 ms	Data: 7F			(Rx)		
0.25989 ms 0.259805 ms	Data: 7E Data: 7F		~	(Der)		
0.259805 ms 0.31186 ms	Data: 7F Data: 7F			(Rx)		
0.311955 ms	Data: 7F			(Rx)		
0.364035 ms	Data: 7E		~	(100)		
•	1	1				
•						
					997 <mark>A</mark>	



NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB storage devices known as USB flash drives, as well as most memory card formats and solid-state drives available today.

Settings

NAND Flash Settings			×
Setting			
Channel Device Width — (* x8 - (* x16)) #CE/RE ① I/O Quick Setup (* x10)) (* x10)) ① I/O User Defined CE#1 I/O0 (LSB) CH 0 I/O [7:0] CE#3 CLE CH 8	C x2 C x4 CH 12 • R/B#1 CH 13 • CH 0 • R/B#2 CH 0 • CH 0 • R/B#3 CH 0 • CH 0 • R/B#3 CH 0 • CH 0 • R/B#4 CH 0 •	Device information Vendors Hynix Model HY275F16 HY275F16 HY275F16 HY275F16 HY27UG08 HY27UG08 HY27UG08	91G2A 92G2B 92G2B 94G2M 98G5M
RE# CH 10 · WE# CH 11 · DQS CH 0 ·	Flash Startup mode Toggle / ONFI DDR Mode Out Cycles A >= 20.0ns tDQ5Q >= 5.0ns	Color Command Address Busy Data In Data Out Range	
Save the NAND Flash Data Reduced Report Show the DDR Data Output / Input Timing Don't care R/B # signal Reduced Command in the waveform window	☐ Don't care CE# signal ☐ Don't care ALE signal	Decode Range From To Default	Buffer Head Buffer Tail OK Cancel

Channel:

Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel



RE	W/R	Read Enable and Write/Read channel
WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel
CE#	CE#	Chip Enable channel
	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O Quick Setup, other channels will be set automatically. when check the I/O User Defined and press the button will show the dialog below:

NAND Flag	sh I/O	×	I
			l
I/O0	сно 🕂	I/O8 CH 0 🗾	l
I/O1	СН 1 📩	I/O9 CH 0 👘	l
I/O2	сн 2 🕂	I/O10 СН 0 👘	l
I/O3	снз	I/011 СН 0 🖂	l
I/04	сн 4 💽	I/012 CH 0 🖂	l
I/05	сн 5 🕂	I/013 CH 0 💡	l
I/06	сн 6	I/014 CH 8 👘	l
I/07	сн 7	I/015 CH 9 👘	l
	OK	Cancel	

User can set NAND I/O channel by channel.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

tREA / tDQSQ: Set the delay time to access the NAND data under SDR / DDR **Save the NAND Flash Data:** Save the read/write data. Program will save the NAND Flash read/write data as a file when check Save the NAND Flash Data. It will be saved into



the LA work directory.

mode.

Reduced Report: Only show NAND Flash command in the Report window when

check it.

Show the DDR Data Output/Input Timing: Only show timing information under

DDR mode.

Reduced Command in the waveform window: Only show NAND Command value

in the waveform window.

Don't care ALE/RB#/CE# signal: Ignore the signal selected when decode.

Description of file name as following:

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxh	Row Address
_Colxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF_DI_Row017821h_Col0000h_CE1_1.bin

NF_DO_Row017821h_Col0000h_CE1_2.bin

NF_DO_Row_Col_CE1_3.bin

Compare the content of file with the one of report.



D0 D1 D2 D3 D4 D5 D6 D7 5A A6 6F 36 B2 38 B8 B7 06 8A B7 0B B1 19 C8 21 7E CE 58 EF BD 18 47 7C 5E DD 9A E3 A5 E4 02 11 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5 55 54 68
06 8A B7 0B B1 19 C8 21 7E CE 58 EF BD 18 47 7C 5E DD 9A E3 A5 E4 02 11 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
7E CE 58 EF BD 18 47 7C 5E DD 9A E3 A5 E4 02 11 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
5E DD 9A E3 A5 E4 02 11 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
53 10 60 79 EA B6 D6 CE 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
8A 73 B3 B1 82 19 B9 46 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
1C E5 20 3D 9F 74 BB E5
55 54 68 4C 69 86 AC OF

000000	5A	A6	6F	36	B2	38	B8	B7	06	8A	B7	ØB	B1	19	C8	21
000010	7E	CE	58	EF	BD	18	47	7C	5E	DD	9A	E3	A5	E4	02	11
000020	E9	2D	96	14	86	32	CE	F4	53	10	60	79	EA	B6	D6	CE
000030	5A	22	53	A5	F1	9E	DB	58	8A	73	B 3	B1	82	19	B9	46
000040	92	25	76	EA	E4	CE	74	A7	10	E5	20	3D	9F	74	BB	E5
000050	55	54	68	40	69	86	AC	ØF	F1	A2	47	FA	37	4B	04	ØD

Device information

Vendors: Select the NAND Flash Vendor. Please refer to the

following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a AqNFCustom.txt file into the LA work directory when

select the **Custom** vendor item and edit NAND Flash Command set.

```
Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , , Y, N, Y, 70
Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10
```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description
Manufacturer	NAND Flash Vendor.
PartNo	NAND Flash IC Model.
#CE/RB	Number of targets, only 1/2/4 acceptable.
X16	8/16 bits device width, only Y/N acceptable.
SyncMode	Only Y/N acceptable, Y: Synchronous data interface supported; N: Not supported.
	Cmd is composed of several parts, it's divided with comma.
	1. Complete command name.



2. Abbreviation of command.
Name of first busy time check. Put a space and add a comma if
unused.
Value of first busy time check. Its unit is micro seconds. Put a space and add a comma if unused.
Name of second busy time check. Put a space and add a comma if unused.
Value of second busy time check. Its unit is micro mseconds. Put a space and add a comma if unused.
First flag. It's acceptable command during busy.
Second flag. It can be inserted by some command or not.
Third flag. It can insert into some multi plane command or not.
Command.

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,

N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

Read Stat. / TPP Prog. : abbreviation of command.

Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is

5000 us. It will show some information when violation of busy time.

3 Flags: 1st flag of "Read Status" is Y means it's acceptable command

During busy; 2nd flag of "Two-Plane Page Program" and 3rd flag of "Read

Status" means any command between 11h and 81h is prohibited except

"Read Status (70h)".



Vendors	Custom	-
Model	Samsung-K9F1G08U0B	
	Toshiba-TH58TVG7D2G	
	Hynix-HY275F081G2A	
	Micron-MT29F2G08AAD	
	Samsung-K9F2G08R0A	
	Samsung-K9F2G08U0A	
	Samsung-K9F4G08U0M	



Result

SDR Data In

71	/OD Idle Col. 00 Col	. 00 Row B2 Row 26	Idle DI	:4B	DI: 83 I	DI: 2E	DI: DB	DI: F	D 🗋
	/01			1 44u	720n		2.	.16u	
	/02	1,44u	960n		2.88u			720n	
	I/03	720n	2.4u		720n	720	0n	720n	
			720n	720n			2.88u		
	I/04	720n	3.84u				1.44u		720n
	I/05	1.44u	2.4u	1	720n	720	0n		
	I/06	_	720n		1.44u		1.44u		720n
	I/07	720n	2.4u	720n	720n		1.44u		
00									
1 /	ALE I								
5 F	E								
21	VE 240n 480n 240n	480n 240n 480n 240n 480r	n 480n 480n 240n	480n 240n	480n 240n	480n 240	0n 480n	240n 4	80m 240m
60	Έ1 <u> </u>								
NandFlach 4 P	/B1								
J U	hannel •		÷	-: -:		:			-
									•
									_
CH-00 CH-00 CH-00 CH-00)							_
CH-00 CH-00) Row Address(h)	Column Address(h)	D0 :	D1 D2	D3	D4	D5	
CH-00 CH-00 CH-00 CH-00	CLE(Nand Flash		Column Address(h)		D1 D2 83 2E	D3 DB	D4 FD	D5 2B	
CH-00 CH-01 CH-01 CH-01 CH-00	CLE(Nand Flash	Row Address(h)		4B 44	83 2E 4F D1	DB 05	FD CD	2B F4	
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CHIECE CH	CLE(Nand Flash	Row Address(h) 0026B2	0000 0008 0010 0018 0020 0028 0030 0038 0040 0040 0048 0050	4B 44 ED 94 F9 2E 7D 7D 73 9A 3F DC	83 2E 4F D1 12 3E 58 3A 37 FC F4 49 EE B9 85 38 21 E3 CE B7 C7 8F	DB 05 7B C7 C3 98 CC 97 FF 1D 11	FD CD 91 67 19 7A E7 64 2E E6 75	2B F4 AF 61 FF 44 88 CD FA 5A 71	D6 A 72 AA 00 9C 87 29 21 A4 92 36 CC CC

DDR Data Out

		25n 12.5 62.5	5n		12.5n	62.5		50n		12.5n 50n	12.5n	37. 25n	12.5n
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nearne 4 R/B. Label Char Office Char Office Char Timestamp 0.00071045 s 0.00071065 s 0.00071068 s 0.00071108 s 0.00071130 s 0.00071132 s 0.00071173 s 0.00071194 s 0.00071194 s 0.00071194 s 0.00071194 s	2 Inel I	B. NAN	D Bus(Na	and Flash		008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0	0 0 0 0 0 0 0 0 0 0 0 0	037 038 039 039 034 03A 03B 03B	8 0 8 0 8 0 8 0 8 0 8	ress (ř	F F F F F F F F	F F F F F F F F F F	FF FF FF FF FF FF FF FF	FF FF FF FF FF FF FF FF FF	F F F F F F F F F	F F F F F F F F	FF	FF FF FF FF FF FF FF FF FF	D F F F F F F F F
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nearne 1 R/B: Label Char Officient Char Officient Char D:00071045 S 0:00071065 S 0:0007108 S 0:00071108 S 0:00071103 S 0:00071135 S 0:00071135 S 0:00071135 S 0:00071135 S 0:000711345 S 0:00071245 S 0:00071237 S 0:000712385 S	2 Inel I	B. NAN	D Bus(Na	and Flash		008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	037 038 039 039 034 034 038 038 038 036 036	8 0 8 8 0 8 0 8 0 8 0 8 0 8	iress (ř	F F F F F F F F F F	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	FF FF	FF FF FF FF FF FF FF FF FF FF	F F F F F F F F F F F	F F F F F F F F F F F	FF FF	FF FF FF FF FF FF FF FF FF FF	D F F F F F F F F F
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NandFlank 4 R/B Label Chan	2 Inel I		D Bus(Na	and Flash		008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0 008E0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	037 038 039 039 034 034 038 038 038 036 036	8 0 8 8 0 8 0 8 0 8 0 8 0 8	iress (ř	F F F F F F F F F F	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	FF FF	FF FF FF FF FF FF FF FF FF FF	F F F F F F F F F F F	F F F F F F F F F F F	FF FF	FF FF FF FF FF FF FF FF FF FF	D F F F F F F F F F F F F F F F F



NEC IR

It needs only one channel to analysis NEC signals.

Settings

NEC Se	ttings	×
Channel	Color	
.=`?	NEC Channel	Leader 🗾 💌
:7	сно 🕂 🛄	Address 🗾 👻
	Extended Mode	/Address
	Display without idle in report	Command 📃 💌
	Swap Bits	/Command
	Polarity Auto 👻	Repeat 🗾 🔽
	· _	Stop 🔽 🗸
Range	-	
inn:	Decode Range	
	From To	
	Buffer Head 📃 Buffer Tail	•
	Defaul	t Cancel

Channel: Display the channel (CH 0).

Extended Mode: It integrates /Address and Address into 16 Bits Address, /Command

and Command into 16 Bits Command.

Display without idle in report: It will not idle on the Report Window for the user to

observe and analyze data.

Swap Bits: Switch LSB First to MSB First.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.



Result

Click \mathbf{OK} to run the NEC IR decode and see the result on the Waveform Window

below.

Time/Div: 12.8 ms	· · · · · · · · · · · · · · · · · · ·											Ģ
Acquired: 08:00:0	0.0	453.874 m	s 474.354	ms 494.83	4 ms 515	.314 ms	535.794	4 ms 5	56.274 ms	576.754 ms	597.234 ms	1
NEC 0								39.924m			309.321m	
		Idle	eader	/Address:E7				Idle	R	epeat	Idle	
												•
Label Cha	nnel 💶											·] _
(CH-00) CH-00 CH-01 CH-00		ws NEC de	coded(NEC IF	र) 💌								
Timestamp	Status	Address	/Address	Command	/Command	Stop	ASCII					
0	Leader	18	E7	00	FF	Y						
0.107282 S	Repeat					Y						
0.455853 S	Leader	18	E7	13	EC	Y						
0.563168 %	Repeat					Y						
0.884187 5	Leader	18	E7	17	E8	Y						
0.991449 5	Repeat					Y						- 11
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					A	4	21103	B	84736	A B	505839	



PECI

Platform Environment Control Interface, Platform management include thermal, power and electrical error monitoring.

Settings

PECI Se	ettings 🛛 🗶
Channel	
:2	Channel Report mode
o –	Data CH 0 🔄 💿 Normal 🔿 Advance
Color	
	Setting transmitter's
	Sync 🗾
	Address 🔽
	WL/RL
	FCS
	Data 📃
Range	
	Decode range
i •−−• i	From To
	Buffer Head 💌 Buffer Tail 💌
	Default OK Cancel

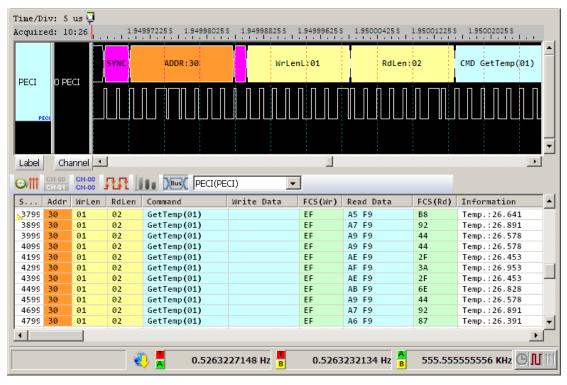
Channel: Show the selected channels.

Report mode: Normal or Advance



Result

Normal mode



Advance mode

Time/Div: 5 us 🖪				
· · · · · · · · · · · · · · · · · · ·	1.98 1.98	1.95 1.95 1.95	1.9S 1.9	95 1.95
PECI O PECI -	Jnknown SYNC ADDR:30	WrLenL:01	RdLen:02	CMD GetTemp(01)
PECI				
				-
Label Channel				•
CH-00 CH-00 CH-00 CH-00		•		
Timestamp	Field	Data	Status	Information 🔺
1.85005855 S	FCS	B8		
1.8999695 %	Client Address	30		
1.89998595 \$	Write Length	01		
1.90000065 \$	Read Length	02		
1.9000153 S	Cmd Code	GetTemp(01)		
1.90002995 \$	FCS	EF		
1.90004465 \$	Temp[7:0]	A5		
1.9000593 S	Temp[15:8]	F9		Temperature:26.641 —
1.9000593 \$	FCS	B8		
1.9499686 5	Client Address	30		
1.9499851 S	Write Length	01		
1.94999975 S	Read Length	02		
1.9500144 S	Cmd Code	GetTemp(01)		
1.95002905 %	FCS	EF		
1.95004375 \$	Temp[7:0]	Α7		•
•				<u> </u>
		4 3799	98690 <mark>B</mark> 37998690	o 🔓 🛛 o 🖸 🛙 🎁



PMBus

The Power Management Bus ("PMBus") is an open standard protocol that defines a means of communicating with power conversion and other devices.

Settings

PMBus Se	ettings						×
Channel					Color		
:	Clock Channel (S		СНО			Start	
	Data Channel (S	DA)	CH 1	• •		Address	
	🔲 Decode With	n PEC				Write	
	7-bit addres	sing (Ir	iclude R/W i	n Address)		Read	
	🔽 Ignore glitch	n				Command	
Range						Data	
	Decode Range	Э				PEC	
* *	From	Buffer	' Head	•		ACK	
	То	Buffer	' Tail	-		Stop	
		·					
					1	Default	OK Cancel

Channel: Show the selected channels.

Decode With PEC: Group command protocol with PEC.

7-bit addressing (Include R/W in address): Show 8-bit addressing (include 7-bit

addressing and 1-bit R/W).

Ignore glitch: Ignore the glitch when the slow transitions.

Result

Click **OK** to run the PMBus decode and see the result on the Waveform Window

below.



Timestamp Start Address Read/Write Ack Command Ack Data Ack Data Ack D 0.07999 ms start 3F Write No Ack EXTENDED (FE) Mo Ack Data Ack D Ack Ack D 0.12405 ms IN Start 46 Write No Ack VOUT_COMMAND (21) No Ack 6E No Ack 6B No Ack 9 0.40367 ms Start 12 Write No Ack EXTENDED (FE) No Ack No Ack 6B No Ack 9 0.40367 ms Start 12 Write No Ack EXTENDED (FE) No Ack No Ack 0				Address:3	F		Extended Cmd:FE		(Command:	5D		
FHS Label L	PM Bus	0 SCK											
Label Channel . <th< th=""><th>PMB</th><th></th><th></th><th>15u</th><th>2</th><th>2.5u</th><th>20u 2.5u</th><th>2.5u 2.5u 2.5</th><th>u 2.5u</th><th>7.5u</th><th>2</th><th>2.5u</th><th></th></th<>	PMB			15u	2	2.5u	20u 2.5u	2.5u 2.5u 2.5	u 2.5u	7.5u	2	2.5u	
Start Address Read/Write Ack Command Ack Data Ack Data Ack D 0.07999 ms start 3F Write No Ack EXTENDED (FE) No Ack Mo Ack CS No Ack Start Start Start No Ack Mo Ack CS No Ack CS No Ack Start													
Start 3F Urite No Ack EXTENDED (FE) No Ack C <thc< th=""> C <thc< th=""> <</thc<></thc<>	Label	Channel											Þ
Jorden and Start JF Urite No Ack EXTENDED (FE) No Ack C <thc< th=""> C C <thc< <="" td=""><td>Timesta</td><td></td><td>Start</td><td>Address</td><td>Read/Mrite</td><td>Ack</td><td>Command</td><td>Ack</td><td>Data</td><td><u>à ck</u></td><td>Data</td><td><u>àck</u></td><td>Dat</td></thc<></thc<>	Timesta		Start	Address	Read/Mrite	Ack	Command	Ack	Data	<u>à ck</u>	Data	<u>àck</u>	Dat
1.12405 ms Mo Ack Ack Mo					,				Data	110/1	Data	11031	24
.19656 ms start 46 Write No Ack VOUT_COMMAND (21) No Ack 3A No Ack 6B No Ack 9 .33315 ms ss 12 Write No Ack EXTENDED (FE) No Ack B4 No Ack C5 No Ack 1 .40367 ms start 12 Write No Ack EXTENDED (FE) No Ack No Ack 1 1 No Ack 1 No			Start	Jr	WIICE	NO ACK			6F	No. Ack			-
1.33315 ms Ico			etart	46	Write	No. Ack					8B	No. Ack	92
No 367 ms start 12 Write No Ack EXTENDED (FE) No Ack No Ack <td></td> <td>шо</td> <td>Scare</td> <td>40</td> <td>WIICC</td> <td>NO HOK</td> <td>VOOT_COMINND (21)</td> <td>NO ROX</td> <td></td> <td></td> <td></td> <td></td> <td>54</td>		шо	Scare	40	WIICC	NO HOK	VOOT_COMINND (21)	NO ROX					54
1.44836 ms Image: Marcine Marcin	33315	me											
1.47585 ns Re-start 22 Read No Ack EXTENDED (FE) No Ack D1 No Ack <td< td=""><td></td><td></td><td>start</td><td>12</td><td>Write</td><td>No. Ack</td><td>EXTENDED (FE)</td><td>No. Ack</td><td>B4</td><td>No Ack</td><td>63</td><td>NO ACK</td><td></td></td<>			start	12	Write	No. Ack	EXTENDED (FE)	No. Ack	B4	No Ack	63	NO ACK	
A.56991 ms Start 3F Write No Ack EXTENDED (FE) No Ack Mo Ack Mo <td>.40367</td> <td>ms</td> <td>start</td> <td>12</td> <td>Write</td> <td>No Ack</td> <td></td> <td></td> <td>84</td> <td>No Ack</td> <td>63</td> <td>NO ACK</td> <td></td>	.40367	ms	start	12	Write	No Ack			84	No Ack	63	NO ACK	
1.61397 ms Image: Marking and Ma	.40367 .44836	ns ns											
D.68648 ms start 46 Write No Ack VOUT_COMMAND (21) No Ack 3A No Ack 6B No Ack 9 0.80306 ms B4 No Ack C5 No Ack C5 No Ack C5 No Ack 9 0.80306 ms B4 No Ack C5 No Ack <t< td=""><td>).40367).44836).47585</td><td>ms ms ms</td><td>Re-start</td><td>22</td><td>Read</td><td>No Ack</td><td>VOUT_MODE (20)</td><td>No Ack</td><td></td><td></td><td></td><td></td><td></td></t<>).40367).44836).47585	ms ms ms	Re-start	22	Read	No Ack	VOUT_MODE (20)	No Ack					
D. 82306 ms Start 12 Urite No Ack EXTENDED (FE) No Ack B4 No Ack C5 No Ack 0.89358 ms start 12 Urite No Ack EXTENDED (FE) No Ack <td>).40367).44836).47585).56991</td> <td>ns ns ns ns</td> <td>Re-start</td> <td>22</td> <td>Read</td> <td>No Ack</td> <td>VOUT_MODE (20) EXTENDED (FE)</td> <td>No Ack No Ack</td> <td>32</td> <td>No Ack</td> <td></td> <td></td> <td></td>).40367).44836).47585).56991	ns ns ns ns	Re-start	22	Read	No Ack	VOUT_MODE (20) EXTENDED (FE)	No Ack No Ack	32	No Ack			
No Ack Start 12 Write No Ack EXTENDED (FE) No Ack	.40367 .44836 .47585 .56991 .61397	ns ns ns ns ns	Re-start start	22 3 F	Read Write	No Ack No Ack	VOUT_MODE (20) EXTENDED (FE) IIN_OC_WARN_LIMIT (5D)	No Ack No Ack No Ack	32 6E	No Ack No Ack	Dl	No Ack	92
N.93827 ms No No No Ack D Start 32 No Ack D No Ack D <thd< th=""> <thd< th=""></thd<></thd<>).40367).44836).47585).56991).61397).68648	ns ns ns ns ns ns	Re-start start	22 3 F	Read Write	No Ack No Ack	VOUT_MODE (20) EXTENDED (FE) IIN_OC_WARN_LIMIT (5D)	No Ack No Ack No Ack	32 6E 3A	No Ack No Ack No Ack	D1 8B	No Ack No Ack	92
D.96577 ms Re-start 22 Read No Ack EXTENDED (FE) No Ack D1 No Ack D1 No Ack .05983 ms start 3F Write No Ack EXTENDED (FE) No Ack Mo Ack <td>).40367).44836).47585).56991).61397).68648).82306</td> <td>ns ns ns ns ns ns ns</td> <td>Re-start start start</td> <td>22 3F 46</td> <td>Read Write Write</td> <td>No Ack No Ack No Ack</td> <td>VOUT_NODE (20) EXTENDED (FE) IIN_OC_WARN_LIMIT (5D) VOUT_COMMAND (21)</td> <td>No Ack No Ack No Ack No Ack</td> <td>32 6E 3A</td> <td>No Ack No Ack No Ack</td> <td>D1 8B</td> <td>No Ack No Ack</td> <td>92</td>).40367).44836).47585).56991).61397).68648).82306	ns ns ns ns ns ns ns	Re-start start start	22 3F 46	Read Write Write	No Ack No Ack No Ack	VOUT_NODE (20) EXTENDED (FE) IIN_OC_WARN_LIMIT (5D) VOUT_COMMAND (21)	No Ack No Ack No Ack No Ack	32 6E 3A	No Ack No Ack No Ack	D1 8B	No Ack No Ack	92
No Solution Start 3F Urite No Ack EXTENDED (FE) No Ack EXTENDED (FE) No Ack Comparison Co	.40367 .44836 .47585 .56991 .61397 .68648 .82306 .89358	ns ns ns ns ns ns ns ns	Re-start start start	22 3F 46	Read Write Write	No Ack No Ack No Ack	VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D) VOUT_COMMAND (21) EXTENDED (FE)	No Ack No Ack No Ack No Ack No Ack	32 6E 3A	No Ack No Ack No Ack	D1 8B	No Ack No Ack	92
.10389 ms 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	.40367 .44836 .47585 .56991 .61397 .68648 .82306 .89358 .93827	ns ns ns ns ns ns ns ns	Re-start start start start	22 3F 46 12	Read Write Write Write	No Ack No Ack No Ack No Ack	VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D) VOUT_COMMAND (21) EXTENDED (FE)	No Ack No Ack No Ack No Ack No Ack	32 6E 3A B4	No Ack No Ack No Ack No Ack	D1 8B C5	No Ack No Ack No Ack	92
.17639 ms start 46 Write No Ack VOUT_COMMAND (21) No Ack 3A No Ack 8B No Ack 9	.40367 .44836 .47585 .56991 .61397 .68648 .82306 .89358 .93827 .96577	ns ns ns ns ns ns ns ns ns	Re-start start start start start Re-start	22 3F 46 12 22	Read Write Write Write Read	No Ack No Ack No Ack No Ack No Ack	VOUT_NODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D) VOUT_COMMAND (21) EXTENDED (FE) VOUT_MODE (20)	No Ack No Ack No Ack No Ack No Ack No Ack No Ack	32 6E 3A B4	No Ack No Ack No Ack No Ack	D1 8B C5	No Ack No Ack No Ack	92
). 40367). 44836). 47585). 56991). 61397). 68648). 82306). 89358). 93827). 96577 05983	ns ns ns ns ns ns ns ns ns ns	Re-start start start start start Re-start	22 3F 46 12 22	Read Write Write Write Read	No Ack No Ack No Ack No Ack No Ack	VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LIMIT (5D) VOUT_COMMAND (21) EXTENDED (FE) VOUT_HODE (20) EXTENDED (FE)	No Ack No Ack No Ack No Ack No Ack No Ack	32 6E 3A B4 32	No Ack No Ack No Ack No Ack No Ack	D1 8B C5	No Ack No Ack No Ack	92
). 40367). 44836). 47585). 56991). 61397). 68648). 82306). 89358). 93827). 96577 L. 05983 L. 10389	ns ns ns ns ns ns ns ns ns ns ns	Re-start start start start Re-start start	22 3F 46 12 22 3F	Read Write Write Write Read Write	No Ack No Ack No Ack No Ack No Ack No Ack No Ack	VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D) VOUT_COMMAND (21) EXTENDED (FE) VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D)	No Ack No Ack No Ack No Ack No Ack No Ack No Ack No Ack	32 6E 3A B4 32 32	No Ack No Ack No Ack No Ack No Ack	D1 8B C5 D1	No Ack No Ack No Ack No Ack	
🍋 🚦 1298 🔒 0 🖥 0 🕑), 40367), 44836), 47585), 56991), 61397), 68648), 82306), 82306), 89358), 93827), 96577 , 05983 , 10389 , 17639	ns ns ns ns ns ns ns ns ns ns ns	Re-start start start start Re-start start	22 3F 46 12 22 3F	Read Write Write Write Read Write	No Ack No Ack No Ack No Ack No Ack No Ack No Ack	VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D) VOUT_COMMAND (21) EXTENDED (FE) VOUT_HODE (20) EXTENDED (FE) IIN_OC_WARN_LINIT (5D)	No Ack No Ack No Ack No Ack No Ack No Ack No Ack No Ack	32 6E 3A B4 32 32	No Ack No Ack No Ack No Ack No Ack	D1 8B C5 D1	No Ack No Ack No Ack No Ack	92



ProfiBus

ProfiBus (PROcess Field Bus) is implemented by RS485. It includes PROFIBUS DP, PROFIBUS PA and PROFIBUS FMS.

Settings

ProfiBus Settings				×
Parameters	Color			
Channel ProfiBus Channel CH 0 Polarity Idle high			SD	
,	SA		DA	
Auto Detect	DSAP	-	FC	
Baud Rate 9600 v bps	DU	—	SSAP	
MSB first	ED		FCS	—
Show scale in the waveform				
Range				
Decode Range				
From To Buffer Head Buffer Tail				
	De	efault	OK]	Cancel

Channel: Set the ProfiBus Channel

Polarity: Set the polarity Idle high / Idle low

Baud Rate/Auto Detect: Set the baud rate manually or auto detect

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section



Result

Time/Div: 4 us	E											
Acquired: 11:11:5	1.693	197.08 us 20	03.48 us 209	9.88 us 216.	28 us 222.68	us 229.08 us	s 235.48 us	241.88 us	248.28 us	254.68 us 26	1.08 us 26	7.48 us
Bus 1 0 F	Idle	SD2 68	LE 04	LEr 04	SD2 68	DA 02	SA 01	FC 5D	DSAP 00	FCS 60	ED 16	
PrefiBer							4.66 us		6.68 us			-
Label Ch	nannel					[
()/111 CH-00 CH-00 CH-01 CH-00	RR 111 0	Bus 1(Prot	fiBus) 💌]								
Timestamp	Frame	Information	1									▲
0.1944 ms	SD2 (68)	Start Delin	niter									
0.20173 ms	LE (04)	Datalen 04										
0.20906 ms	LEr (04)											
0.2164 ms	SD2 (68)											
0.22373 ms	DA (02)											
0.23106 ms	SA (01)		02 (Response									
0.2384 ms	FC (5D)		DL Data High	Resource For	Send Data							
0.24573 ms	DSAP (00)	Write_Read	Data									
0.25307 ms	FCS (60)											
0.26041 ms	ED (16)	End Delimi	ter									-
•	1											
					(🤁 🔓 263	.157894737	(Hz <mark>A</mark> 1.8	59427296 KHz	A 9.286	775632 KHz	© N 111



PS/2

The Personal System/2 (PS/2) protocol has 6 data bits, but only the first bit (Data) and the fifth bit (Clock) need to be analyzed.

PS/2 Settings

PS/2Se	ettings 🛛 🔀
Channel –	
1	General Analysis Report
	Clock CH 0 · Data CH 1 ·
	Convert scancode to keycode
	🔲 Export Matlab file
	🔽 Ignore glitch
Color —	
	Setting transmitter's color Host Device
Range —	
inn:	Decode Range
*	From To
	Buffer Head 💌 Buffer Tail 💌
	Default OK Cancel

Channel: Show the selected channels.

Convert scan code to key code: Transform data into keyboard characters.

Export MATLAB file: Export the data with MATLAB format as the following:

Time = [25.78484 25.785985 ...]

Description = [DH DH ...] DH = Device to Host, HD = Host to Device

Data = [58 FA 02 FA C4 ...]



The file (PS2_Matlab.m) will be saved at work directory

Ignore glitch: Ignore the glitch when the slow transitions.

Analysis Report: Show the selected status in report.

General	Analysis Report
Show t	the status in report
Des	cription
🗹 Dat	a
Erro	or
ASC ASC	
Idle Idle	
1	

Result

Click **OK** to run the PS/2 decode and see the result on the Waveform Window below.

ime/Div: 400 u cquired: 08:00	· · · · · · · · · · · · · · · · · · ·	9 ms 37.089 ms	37.729 ms	38.369 ms	39.009 ms	39.649 ms	40.289 ms	40.929 ms	(5
-s2 0		DtoH:18			DtoH:00		DtoH:00	Idle	
-32 0						ווח חוו			
	Data	324u 242u 3	284u	972 <mark>u</mark>	729u	283u	729u	13.702m	
PS/2									
abel (Channel 💶 📃								₽
CH-00 CH		2(09/2)	-						
//// CH-01 CH	Description	Data	Error					2	ASCI
.933 ms	Idle	Data	ELLOI	•					ADUT
.933 ms 6.607 ms	Device to Host	18							
7.514 ms	Idle	10						•	
7.619 ms	Device to Host	FF							
3.538 ms	Idle								
3.672 ms	Device to Host	00							
9.562 ms	Idle							-	
9.684 ms	Device to Host	00							
).585 ms	Idle								
4.115 ms	Device to Host	18							
5.048 ms	Idle								
5.168 ms	Device to Host	FF							
5.072 ms	Idle								
6.181 ms	Device to Host	00						-	
	Idle								
7.096 ms									
57.096 ms									
					255 🚪	3057	726 <mark>A</mark>	305981 🕒	



PWM

Pulse-width modulation (PWM) is a commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches.

Settings

PWM Settings	×
Setting	Color
Channel	Duty Cycle
PWM Channel CH 0	90%~100%
Draw PWM curve	80%~89%
- Source	70%~79%
	60%~69%
	50%~59%
Color	40%~49%
C Time(X) - Duty(Y) C Time(X) - Freq.(Y)	30%~39%
3 7 8	20%~29%
	10%~19%
Time (X)	0%~9%
Draw 0% and 100% Time(X) - RPM(Y)	Range
3	Decode Range
RPM (Y)	From Buffer Head
Time (X)	To Buffer Tail
Color	
	Default OK Cancel

Channel: Show the selected channel.

Draw PWM curve:

Source: Show the source waveform of the PWM.

Time(X)-Duty(Y): Show the curve diagram with Time(X) and Duty(Y)

Time(X)-Freq.(Y): Show the curve diagram with Time(X) and Freq.(Y)

Time(X)-RPM(Y): Show the curve diagram with Time(X) and RPM(Y)



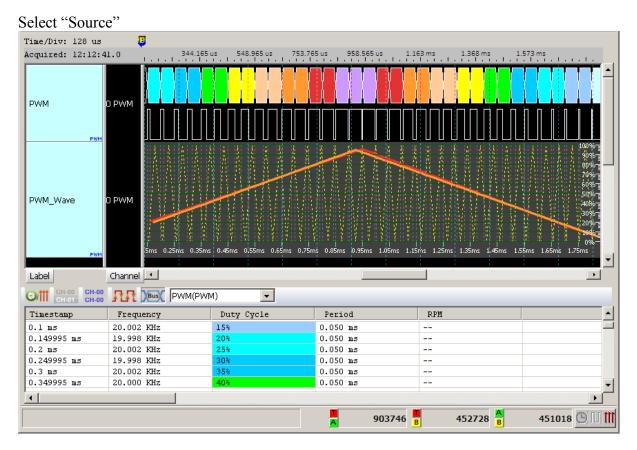
Draw 0% and 100%: When select the Time(X)-Duty(Y) drawing and check Draw 0% and 100%, the program will draw this duty curve of 0% or 100%; it will draw this duty curve of 0% or 100% when uncheck Draw 0% and 100%.

Draw 0 Hz: When select the Time(X)-Freq.(Y) drawing and check the item Draw 0 Hz, will show the Frequency from 0 Hz at Y axis.

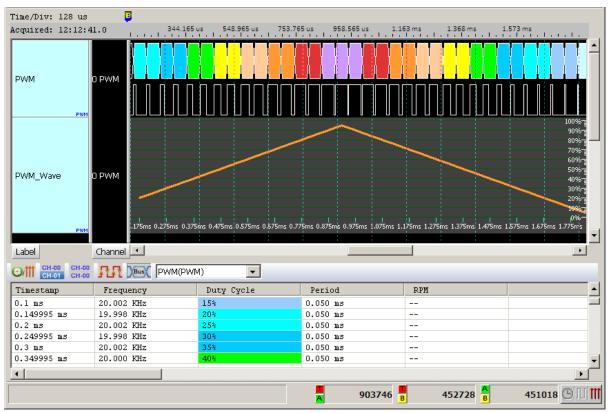
Result

Click OK to run the PWM decode and see the result on the Waveform Window

below.

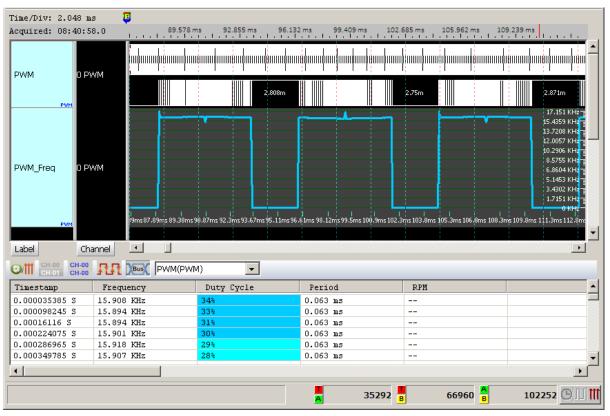






Select Time(X)-Duty(Y)

Select Time(X)-Freq.(Y)





Time/Div: 819.2 ms U Acquired: 14:50:04.0 6.554 S 9.175 \$ 10.486 \$ PWM_RPM O PWM 3.014s 0.9881s 2.005s • Channe ▶ Label -Timestamp Frequency Period RPM Duty Cycle 0.343341 S 0.374898 S 32 Hz 33 Hz 33 Hz 0.031 s 50% ---0.030 s 493 0.405376 S 0.030 s ---504 ---0.43545 S 34 Hz 0.029 s 49÷ 0.464679 S 0.029 s 34 Hz **4**9% 0.493741 S 35 Hz 49 0.029 s ÞÍ A 1408 📕 0 GII 11 1408 A

Select Time(X)-RPM(Y)



QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

Settings

QI Pa	rameter Setting
Channe	Setting
:	QI Channel CH 0 📩 🔽 Advanced Decode
Color —	
	Preamble 🗾 👻 Start 📃 💌
_	Head Parity
	Message Stop
	CheckSum
Range -	
<u></u>	Decode Range
6 B	From To
	Buffer Head 🔹 Buffer Head 💌
	Default OK Cancel

QI Channel: Show the selected channel.

Advance Decode: show detail message decode



Result

		s 36.636 ms 39.196 ms 41.756 ms 44.316 ms 46.876 m		
	Idle Preamble	Header 01 Message 6B	Check Sum 6A	
COMM1 QI				
Label Ch	nar 💶 🔄			•
⊙/∰ CH-00 CH-00 CH-01 CH-00		•		
Timestamp	Header(h)	Message(h)	CheckSum(h)	E: 4
0.036679 %	Signal Strength (01)	6B	6A	
0.066613 ន	Identification (71)	Minor Version (0)		
0.066613 %		Major Version (1)		
0.066613 %		Manufacturer Code (00 10)		
0.066613 5				
		Basic Device Identifier (00 6A EO 4A)		
		Easic Device Identifier (UU 6A EU 4A) Ext (O)	Bl	
0.066613 S 0.130477 S	Configuration (51)	Ext (O) Maximun Power (OA)	B1	
0.066613 S 0.130477 S 0.130477 S	Configuration (51)	Ext (0) Maximun Power (0A) Power Class (0)	Bl	
0.066613 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$	Configuration (51)	Ext (0) Maximun Power (0A) Power Class (0) Count (0)	Bl	
0.066613 S 0.130477 S 0.130477 S 0.130477 S 0.130477 S 0.130477 S	Configuration (51)	Ext (0) Maximun Power (OA) Power Class (0) Count (0) Prop (0)	Bl	
0.066613 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$	Configuration (51)	Ext (0) Maximun Power (0A) Power Class (0) Count (0) Prop (0) Window Offset (0)		
0.066613 S 0.130477 S 0.130477 S 0.130477 S 0.130477 S 0.130477 S 0.130477 S 0.130477 S		Ext (0) Maximun Power (0A) Power Class (0) Count (0) Prop (0) Window Offset (0) Window Size (00)	58	
0.066613 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$	Control Error (03)	Ext (0) Maximun Power (0A) Power Class (0) Count (0) Prop (0) Window Offset (0) Window Size (00) 1E	5B 1D	
0.066613 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.221095 \$ 0.281483 \$	Control Error (03) Control Error (03)	Ext (0) Maximum Power (0A) Power Class (0) Count (0) Prop (0) Window Offset (0) Window Size (00) 1E 1E	5B 1D 1D	
0.066613 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$	Control Error (03)	Ext (0) Maximun Power (0A) Power Class (0) Count (0) Prop (0) Window Offset (0) Window Size (00) 1E	5B 1D	
0.066613 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.130477 \$ 0.221095 \$ 0.281483 \$	Control Error (03) Control Error (03)	Ext (0) Maximum Power (0A) Power Class (0) Count (0) Prop (0) Window Offset (0) Window Size (00) 1E 1E	5B 1D 1D	



RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

Settings

RC-5 Set	tings		?	\times
Channel	RC-5 Channel CH 0	Encoding Method Auto Detect C Mancherster C Mancherster with carrier		
Color	S1 S2 Toggle 0 Toggle 1 Address Command	Range Decode Range From To Buffer Head Buffer Tail Default OK Cancel	•	

Channel: Show the selected channel (CH 0).

Extended mode: When the Extended enabled, the S2 will be converted into seventh

bit of the Command. There is an Extend Command on the Waveform Window.

Display without idle in report: It will not idle on the Report Window for the user to observe and analyze data.

Encoding Method: Auto Detect mode, Mancherster mode and Mancherster with carrier mode.

S1/S2: Start bit.

Toggle 0/Toggle 1: The difference is that has been used while sending the message to



repeat, or send a new message.

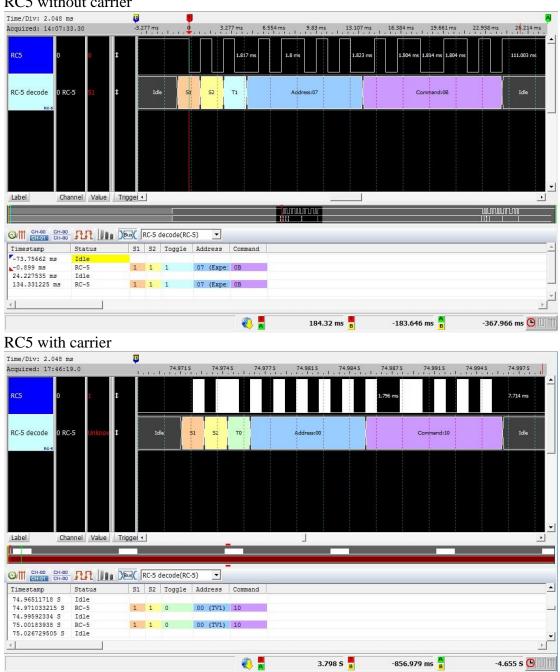
Address: To represent different device addresses.

Command: To represent the different button commands.



Result

Click **OK** to run the RC-5 decode and see the result on the Waveform Window below.



RC5 without carrier



RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

Settings

RC-6 Set	tings		? ×
Channel	RC-6 Channel CH 0 Addr&Cmd Bits 8 Bits Sits Sits Sits Sits	Encoding Method Auto Detect Mancherster Mancherster with carrier	
Color	Leader Start Bit Mode Bits Toggle Bit Control	Range Decode Range From To Cursor Trigger(T) V Buffer Tail]
	Information	Default OK Cancel	

Channel: Show the selected channel (CH 0).

Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and information in

the control label.

Display without idle in report: Do not display any idle in the Report Window.

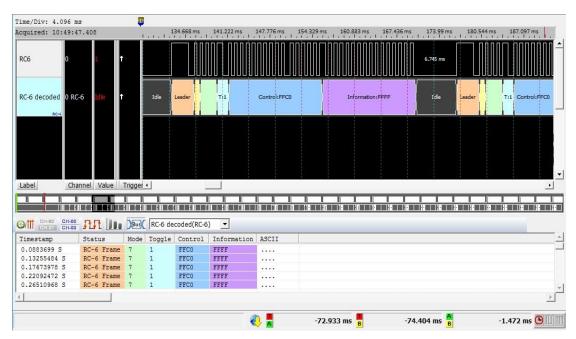
Encoding Method: Auto detect mode, Mancherster mode, Mancherster with carrier

mode.



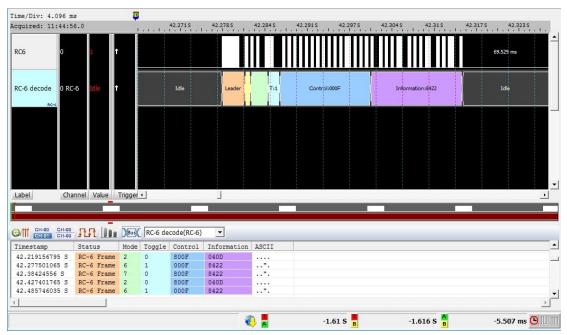
Result

Click **OK** to run the RC-6 decode and see the result on the Waveform Window below.



RC6 without carrier

RC6 with carrier





RGB Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

Settings

RGB_IF Settings	Х								
Channel									
SCLK CH 17 R0 CH 14 G0 CH 2 B0 CH 16 · DE CH 17 · R1 CH 5 G1 CH 17 · B1 CH 17 · Hsync CH 12 · R2 CH 3 · G2 CH 9 · B2 CH 17 · VSYNC CH 1 · R3 CH 4 · G3 CH 10 · B3 CH 0 · R4 CH 6 · G4 CH 13 · B4 CH 7 · R5 CH 17 · G5 CH 13 · B4 · · · R6 CH 0 · B5 CH 8 · R6 CH 0 · G6 CH 0 · B6 CH 0 · R									
R7 CH0 → G7 CH0 → B7 CH0 → Format User defined ▼ Save as JPG file A (Alpha) R (Red) G (Green) B (Blue) L (Luminance) 0 bits ▼ 6 bits ▼ 6 bits ▼ 0 bits ▼									
Range Decoded Range From Buffer Head To Buffer Tail									
Default OK Cancel									

SCLK: The Clock pin.



DE: The Data Enable pin.

Hsync: The Horizontal synchronization pin.

Vsync: The Vertical synchronization pin.

R0 – 7, G0 – 7, B0 – 7: RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of LA.

				30.855	us	30.905	us 30.95	55 US	31.005	us	31.05	5 US	31.10	US US	31.15	55 US
cquired: 17:49:3	32.697	1		1.1		- 1 - 1 - 1 -			1.1.1	6 I. A.			11.1.1.1		1.1.1	
Bus 1 24	, R: 10, G XX	*****			F	R: 00, G: 01). B: 22.				R: 00	I. G: 0). B: 22.			
					_											
3.111 CH-00 CH-00	1.0		•] Bus 1(RGB_IF	:)	•										Þ
Label CH-00 CH-00 CH-00 CH-01 CH-00	- AA 🛄		Bus 1(-		D2 (RGB)	D3	(RGB)	D4	(RGB)	D5	(RGB)	D6	(RGB)	
Label CH-00 CH-00 CH-00 CH-01 CH-00 Timestamp	Field	LL DBus(Bus 1((GB)	D1 ((RGB)	D2 (RGB)		(RGB)		(RGB)	D5	11		(RGB)	D7
Label C CH-00 CH-00 CH-00 CH-00 Timestamp 0.02949 ms	Field Ln1, D[10	6:23]	Bus 1((GB)	D1 (D2 (RGB) 00 00 22 00 00 22	00	(RGB) 00 22 00 22	00	(RGB) 00 22 00 22		00 22	00	(RGB) 00 22 20 20	
Label CH-00 CH-00 CH-01 CH-00 Timestamp 0.02949 ms 0.030825 ms	Field Ln1, D[10 Ln1, D[20	6:23] 4:31]	Bus 1(D0 (F 00 00 00 00	(GB) 22 22	D1 (00 0	(RGB)	00 00 22	00 00	00 22	00 00	00 22	00	00 22	00 20	00 22	D7
Label CH-00 CH-00 CH-00 CH-00 CH-00 Timestamp 0.02949 ms 0.030825 ms 0.032155 ms	Field Ln1, D[14 Ln1, D[24 Ln1, D[32	6:23] 4:31] 2:39]	Bus 1((GB) 22 22 20 10	D1 (00 (00 (10 1	(RGB) 00 22 00 22	00 00 22 00 00 22	00 00 10	00 22 00 22	00 00 10	00 22 00 22	00 00 10	00 22 00 00	00 20 10	00 22 20 20	D7 00 10
Label CH-00 CH-00 CH-01 CH-00 CH-00 Timestamp 0.02949 ms 0.030825 ms 0.032155 ms 0.03349 ms	Field Ln1, D[14 Ln1, D[24 Ln1, D[32 Ln1, D[40	6:23] 4:31] 2:39] 0:47]	Bus 1(D0 (F 00 00 10 10 10 10	AGB) 22 22 10 10 10	D1 (00 (00 (10 1 10 1	(RGB) 00 22 00 22 10 10 10 10	00 00 22 00 00 22 10 10 10 10 10 10	00 00 10 10	00 22 00 22 10 10 10 10	00 00 10 10	00 22 00 22 10 10 10 10	00 00 10 10	00 22 00 00 10 10 10 10	00 20 10 10	00 22 20 20 10 10 10 10	D7 00 10 10 10
Label CH-00 CH-00 CH-01 CH-00 CH-00 Timestamp 0.02949 ms 0.030825 ms 0.03349 ms 0.034825 ms	Field Field Ln1, D[14 Ln1, D[24 Ln1, D[32 Ln1, D[46 Ln1, D[46	6:23] 4:31] 2:39] 0:47] 8:55]	Bus 1(D0 (F 00 00 10 10 10 10 10 10	AGB) 22 22 10 10 10 10 10	D1 (00 (10 1 10 1 10 1	(RGB) 00 22 00 22 10 10 10 10 10 10	00 00 22 00 00 22 10 10 10 10 10 10 10 10 10	00 00 10 10 10	00 22 00 22 10 10 10 10 10 10	00 00 10 10 10	00 22 00 22 10 10 10 10 10 10	00 00 10 10	00 22 00 00 10 10 10 10 10 10	00 20 10 10	00 22 20 20 10 10 10 10 10 10	D7 00 10 10 10 20
Label CH-00 CH-00 CH-01 CH-00 CH-00 Timestamp 0.02949 ms 0.030825 ms 0.032155 ms 0.034825 ms 0.034825 ms 0.036155 ms	Field In1, D[14 In1, D[22 In1, D[33 In1, D[40 In1, D[40 In1, D[50	6:23] 4:31] 2:39] 0:47] 8:55] 6:63]	Bus 1(D0 (F 00 00 10 10 10 10 10 10 00 00	(GB) 22 22 10 10 10 10 10 10 10	D1 (00 (10 1 10 1 10 1	(RGB) 00 22 00 22 10 10 10 10 10 10 10 10	00 00 22 00 00 22 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10	00 00 10 10 10	00 22 00 00 10 10 10 10 10 10 10 10 10 10	00 20 10 10 10	00 22 20 20 10 10 10 10 10 10 10 10	D7 00 10 10 10 20 10
Label Close CH-00	Field In1, D[14 In1, D[24 In1, D[32 In1, D[40 In1, D[50 In1, D[50 In1, D[64	6:23] 4:31] 2:39] 0:47] 8:55] 6:63] 4:71]	Bus 1(D0 (F 00 00 10 10 10 10 10 10 10 10 10 10 10 10	AGB) 22 22 10 10 10 10 10 10 10 10 10 10	D1 (00 (10 1 10 1 10 1 10 1	(RGB) 00 22 00 22 10 10 10 10 10 10 10 10 10 10	00 00 22 00 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10	00 22 00 00 10 10 10 10 10 10 10 10 10 10 10 10	00 20 10 10 10 10 10	00 22 20 20 10 10 10 10 10 10 10 10 10 10 10 10	D7 00 10 10 10 20
Label CH-00 CH-00 CH-00 CH-00 CH-00 CH-00 CH-00 Timestamp 0.02949 ms 0.030825 ms 0.032155 ms 0.03349 ms 0.034825 ms 0.03749 ms 0.03749 ms 0.038825 ms	Field In1, D[14 In1, D[24 In1, D[33 In1, D[44 In1, D[44 In1, D[55 In1, D[64 In1, D[72	6:23] 4:31] 2:39] 0:47] 8:55] 6:63] 4:71] 2:79]	Bus 1(D0 (F 00 00 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	AGB) 22 22 10 10 10 10 10 10 10 10 10 10	D1 (00 (10 1 10 1 10 1 10 1 10 1	(RGB) 00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 22 00 00 22 10	00 00 10 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10	00 22 00 00 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 20 10 10 10 10 10	00 22 20 20 10 10 10 10 10 10 10 10 10 10 10 10 10 10	D7 00 10 10 10 20 10 10 10
Label CH-00	Field In1, D[14 In1, D[24 In1, D[32 In1, D[45 In1, D[46 In1, D[66 In1, D[72 In1, D[80	6:23] 4:31] 2:39] 0:47] 8:55] 6:63] 4:71] 2:79] 0:87]	Bus 1(D0 (F 00 00 00 00 10 10 10 10 10 10 10 10 10 10 10 10 20 20	RGB) 22 22 10 10 10 10 10 10 10 20 20	D1 (00 (10 1 10 1 10 1 10 1 10 1 10 1	(RGB) 00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 22 00 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10 10	00 22 00 00 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 20 10 10 10 10 10 10	00 22 20 20 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10 10	D7 00 10 10 10 20 10 10 10 10
Label CH-00 CH-00 CH-00 CH-00 CH-00 CH-00 CH-00 Timestamp 0.02949 ms 0.030825 ms 0.032155 ms 0.03349 ms 0.034825 ms 0.03749 ms 0.03749 ms 0.038825 ms	Field In1, D[14 In1, D[24 In1, D[33 In1, D[44 In1, D[44 In1, D[55 In1, D[64 In1, D[72	6:23] 4:31] 2:39] 0:47] 8:55] 6:63] 4:71] 2:79] 0:87] 8:95]	Bus 1(D0 (F 00 00 10 10 10 10 10 10 10 10 10 10 10 10 10 10	RGB) 22 22 10 10 10 10 10 10 10 20 10 10 10 10 10 10 10 10 10 1	D1 (00 (10 1 10 1 10 1 10 1 10 1 10 1 1	(RGB) 00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 22 00 00 22 10	00 00 10 10 10 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10 10	00 22 00 22 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 00 10 10 10 10 10 10 10	00 22 00 00 10 10 10 10 10 10 10 10 10 10 10 10 10 10	00 20 10 10 10 10 10 10 10	00 22 20 20 10 10 10 10 10 10 10 10 10 10 10 10 10 10	D7 00 10 10 10 20 10 10 10

Result



S/PDIF

The Sony/Philips Digital Interconnect Format (S/PDIF) is a digital audio transmission

interface with the detailed specifications below:

Data format: Default is 16 bits, up to 24 bits.

Sampling frequency:

44.1Khz from CD \rightarrow Bit Rate 2.8224 Mbit/s

48 Khz from DAT \rightarrow Bit Rate 3.072 Mbit/s

32 Khz from DSR \rightarrow Bit Rate 2.048 Mbit/s

Deliver method: One way.

V (Validity) bit: Audio samples to confirm effectiveness, if this bit is 0, the receiver

should ignore this sub-frame.

U (User) bit: User log information.

C (Channel status) bit: Channel state information.

P (**Parity**) **bit:** Parity bit check for the error.

The basic principle is to split the data bits into two parts. If the data is 1, split it into

01 or 10 or if the data is 0, split it into 00 or 11.

Settings



Setting Channel CHO Auto detect Bit Rate Coor Parity mode Even parity Parity mode Even parity Parity mode Even parity Parity mode Even parity Parity mode Even parity Parity mode Even parity Playback Color Preamble Aux Data Audio Data Validity bit Coor Preamble Aux Data Audio Data Validity bit Coor Preamble Aux Data Audio Data Coor Preamble Aux Data Coor Preamble Aux Data Coor Coo	S/PDIF Settings
Range Code Range	Setting Channel CH 0 Auto detect Bit Rate D.0000 Mb/s (384Kb/s~12.288Mb/s) Display the audio waveform Color Preamble Aux Data Audio Data Audio Data Color Preamble Aux Data Audio Data Color Preamble Aux Data Auto Data Color Preamble Aux Data Auto Data Color Preamble Aux Data Auto Data Color Preamble Aux Data Auto Data Color Color Preamble Aux Data Auto Data Color
Buffer Head Buffer Tail Default OK Cancel	Decode Range From To Buffer Head To Buffer Tail

Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.

Num of frame: 192 frames within each block by default, used to analyze each

sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

Parity mode: The default is even parity.

Display the audio waveform: Click to display the audio waveform in the Waveform

Window.

Result

Click **OK** to run the S/PDIF Decode and see the result on the Waveform Window



below.

/PDIF DS	5/PDIF	C6	Preamble:W 4	Aux:0	D	ata:0000D		
S/PDIF			540n					
								-
abel C	nannel 💶							
		S/PDIF(S/PD	DIF) 💌					
imestamp	Frame	Preamble	Aux Data	Audio Data	Validity bit	User bit	Channel Status	Pa 🔺
.99345732 S	95	М	0	OFFC6	0	0	0	0
.99346866 S		W	0	0000D	0	0	0	1
.99348 S	96	М	0	OFFDB	0	0	0	0
.99349134 S		W	0	00035	0	0	0	0
.99350268 ສ	97	М	0	OFFF2	0	0	0	1
.99351402 S		W	0	0005A	0	0	0	0
.99352536 S	98	M	0	00000	0	0	0	0
.99353668 S		U	0	00080	0	0	0	1
.99354802 S	99	M	0	00006	0	0	0	0 -
.99355936 S		W	0	00090	0	0	0	0
.9935707 ສ	100	M	0	00001	0	0	0	1
.99358204 S		W	0	000B6	0	0	0	1
.99359338 S	101	M	0	OFFF7	0	0	0	1 🗸

Show wave:

	: 131.072 : 08:00:0	· · · · · · · · · · · · · · · · · · ·	209.715 n	ns 419.43 ms	629.146 ms 8	38.861 ms	1.049 \$ 1.258	S 1.468 S	
PBus1	SIPDIF	Max Min S/PDIF Min	a 6572 4496 a 5706 5766				, uj de la de secto	30000 30000 -30000 -30000	
Label		ihannel 🔄							Þ
©/∰ 🗄	1-00 CH-00 1-01 CH-00		PBus1(S/PE	DIF) 🔽					
Ti	Frame	Preamble	Aux Data	Audio Data	Validity bit	User bit	Channel Status	Parity Bit	Error
0.0		U	0	OFDD6	0	0	0	0	
0.0	76	М	0	001BA	0	0	0	0	
0.0		U	0	OFDB7	0	0	0	1	
0.0	77	M	0	00202	0	0	0	0	
0.0		U	0	OFD93	0	0	0	1	
0.0	78	M	0	00222	0	0	0	1	
0.0		W	0	OFD77	0	0	0	1	
0.0	79	M	0	00229	0	0	0	0	
0.0		W	0	OFD4B	0	0	0	1	
0.0	80	M	0	0020D	0	0	0	0	
0.0		W	0	OFD20	0	0	0	0	
0.0	81	M	0	00105	0	0	0	1	
0.0		W	0	OFCFA	0	0	0	0	
0.0	82	M	0	00161	0	0	0	0	
•									•
						151	B 13	1 <mark>A</mark>	20 🕒 🛙 🚺



SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for

interfacing with SD (Secure Digital) Flash memory cards.

Settings

SDIO	SD3.0 Settings		×
Channel		Color	
:	Channel	Analysis Command only	Start bit
		C Data only C Command + Data	Host
	DATAO CH2 × DATAS CH7 ×	Adv. Report	CMD/Resp
	DATA1 CH3 × DATA6 CH8 ×	C 8-bit Data	
	DATA2 CH 4 + DATA7 CH 9 +	 4-bit Data 1-bit Data IO interrupt 	Data
	Data length: Bytes (Min: 1, Max: 2048)	DDR mode	CRC status
Range	Decode Range From To		
	Buffer Head 🗾 Buffer Tail	•	Default OK Cancel

Channel: Show the selected channels.

Command only: Analyze the command.

Data only: Analyze the data.

Command + Data: Analyze Command and Data in the report window.

Adv. Report: Analyze the command argument

Don't care clock: decode only depend on the CMD channel.

Data: 1/4/8 bits or DDR mode, check "IO interrupt" when SDIO 1 bit mode and

support the IO interrupt decode via DATA1 channel, check "DDR mode" and "

"Non-interleaved" to analyze data without interleaved.

Data length: Set the length of data.



Result

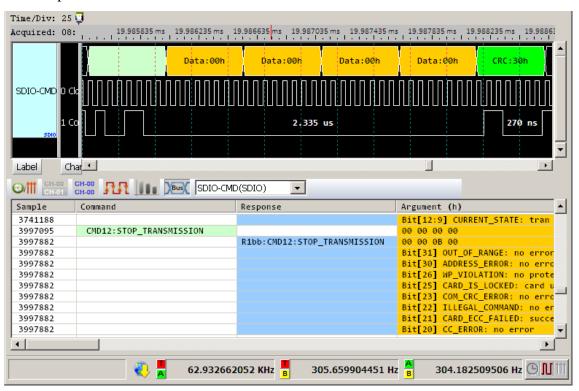
Click OK to run the SDI/O decode and see the result on the Waveform Window

below.

CMD mode

Time/Div: 7.5 ns					-	:
						2
Acquired: 17:06:46	5.6 307.5 ns 320 ns	332.5 ns 345 ns 357.5 r	ns 370 ns	382.5 ns	395 ns	
	R1:CMD19:SET_TUNING_PA				ta:00h	
SDIO1 O Clock				1	1	
1 Comma	and 0 1 0	1				
SDIO						•
Label Channel					•	
CH-00 CH-00 CH-00 CH-00	SDIO1(SDIO)	•				
Timestamp	Command	Response	Argument (h)	CRC7 (h)	Frequency	
0.0002925 ms		R1 :CMD19:SET TUNING PATTERN	00 00 09 00	5F	183MHz	-
0.11772625 ms	CMD17:READ SINGLE BLOCK		00 00 00 00	2A	183MHz	
0.11806 ms		R1 :CMD17:READ_SINGLE_BLOCK	00 00 09 00	33	184MHz	
0.3390275 ms	CMD17:READ_SINGLE_BLOCK		00 00 00 00	2A	184MHz	
0.33936 ms		R1 :CMD17:READ SINGLE BLOCK	00 00 09 00	33	184MHz	
0.58585375 ms	CMD17:READ SINGLE BLOCK		00 00 00 00	2A	183MHz	
0.58618625 ms		R1 :CMD17:READ SINGLE BLOCK	00 00 09 00	33	183MHz	
0.83524375 ms	CMD19:SET_TUNING_PATTERN		00 00 00 00	46	183MHz	
0.83557625 ms		R1 :CMD19:SET TUNING PATTERN	00 00 09 00	5F	183MHz	
0.9633125 ms	CMD19:SET_TUNING_PATTERN		00 00 00 00	46	184MHz	
0.96364 ms		R1 :CMD19:SET_TUNING_PATTERN	00 00 09 00	5F	184MHz	
1.07436 ms	CMD19:SET_TUNING_PATTERN		00 00 00 00	46	183MHz	
1.0746925 ms		R1 :CMD19:SET_TUNING_PATTERN	00 00 09 00	5F	183MHz	
1.1921325 ms	CMD17:READ_SINGLE_BLOCK		00 00 00 00	2A	184MHz	
1.192465 ms		R1 :CMD17:READ_SINGLE_BLOCK	00 00 09 00	33	183MHz	
1.4134275 ms	CMD17:READ_SINGLE_BLOCK		00 00 00 00	2A	184MHz	
1.413755 ms		R1 :CMD17:READ_SINGLE_BLOCK	00 00 09 00	33	184MHz	-
		🍋 🧧 2.221 KHz	Б 573.89 Hz	<mark>А</mark> 773.	898 Hz 🕒 🚺	111

Adv. Report





Data mode

	16.6	1	5 US 80	9.37876 us	869.39	125 us	\$69.40375	us 869.4	1625 us	869.42875 us 869.44125 us 86	9.45375 us
	e	Fh	FEh	cci	1	DCh	CCh	3	3h	CCh CDh FFh	EFh
0 Clock	0		i] [] e		1		0		1		1
1 Comma	nd										
			4								
DIO 2 Data[0]	0	1		0	1		3	1		0 1	0
3 Data[1]] 0	1		0	1		0		1	0	
4 Data[2]	0		1		0		1		0		
		-	1		0	-	-		0		
solo 5 Data[3]		_	1		2		1		0		
abel Channel	•										•
			(0010)		_						
СН-00 СН-00	ЛЛ 🕅	🕺 SDIC	(SDIO)		-						
imestamp	State	D0(h)	D1(h)	D2(h)	D3(h)	D4(h)	D5(h)	D6(h)	D7(h)	Information	
56387125 ms										CRC16 OK!	
869355 ms	Data	ØF	FE	CC	DC	CC	33	CC	CD	Nac > 4095	
8694425 ms	Data	FF	EF	FF	EE	FF	FF	FF	FF		
86953 ms	Data	DD	FF	FB	FF	FB	BF	FF	FF		
8696175 ms	Data	F7	7F	7F	FE	FF	FF	21	FF		
86970375 ms	Data	EØ	1F	CC	C3	EC	CD	3A	CC		
86979125 ms	Data	DF	FE	FF	FE	EF	FF	FF	FF		
86987875 ms	Data	FD	FF	FB	FF	FF	BF	FF	7F		
86996625 ms	Data	FF	F7	F7	FF	EF	F5	01	AA		
1 1											•



Serial Flash

SPI Serial Flash is small, low-power flash memory that features Serial Peripheral Interface (SPI) and pin-for-pin compatibility with industry-standard SPI EEPROM devices.

Serial	Flash	(25 Ser	ies) Se	ttings		×
Channel -						
The flash	up in PEM m ny Cycles	ode ode ADDR, mode ode 2 Clk 🖵	When Comm	ion	Manufacturer Atmel Device AT25DQ161 AT25F512B tCLQV - 7.50 ns	
🗖 QE bi		8B 🔻			tSHSL - 100 ns	—]-
Ad Da	ommand Idress ata In		▼ ▼ ▼	Data Out Mode Dummy		• •
	ecode Rang iegin Buffer Head		End Buffer Tai	T		
				Default	OK Ca	ncel

Settings

Channel: Show the selected channels (CH0 – CH5).

Manufacturer/Device: Select the Serial Flash device type, tCLQV and tSHSL.



QPI mode: Quad Peripheral Interface Mode/Quad SPI Mode

4-Byte mode: 4-Byte Address Mode

PEM mode: Performance Enhance Mode

Dummy Cycles: Clock buffers between read command and data.

Wrap Around: Wrap number

QE bit: Enable or disable the QPI mode.

Decode SI Only: Single mode, 3-wire \rightarrow CS#, SCLK, SI.

Decode Single Mode Only: Single mode, 4-wire \rightarrow CS, Clock, SI, SO.

The LA viewer will choose 4-wire or 6-wire to analyze according to the Serial Flash device type.

Result

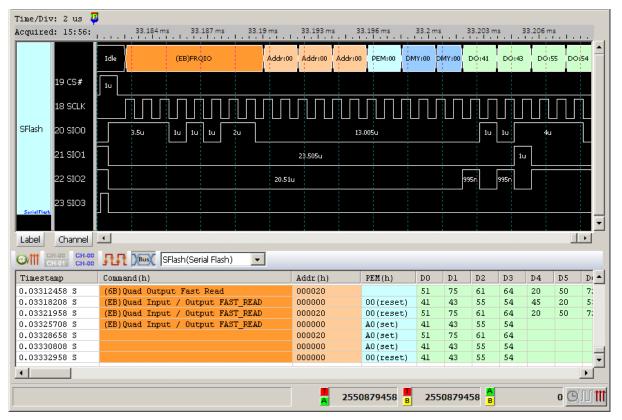
Click **OK** to run the Serial Flash decode and see the result on the Waveform Window below.

Serial Flash decode within SPI mode.



ime/Div: 4 us 📮 cquired: 15:56: ,	146.53 us 152.93	us 159.33 u	us 165.73 us	172.13 us	178.53	us 18	84.93 u	5	191.33 u	IS .	
	Idle (20)5E	Add::00	Addr:00	Addr:00	i I	05)RDSR1		DO:		Idle	
19 CS#	íu	32.5u			1u		16.5u			1u	
18 SCLK					20			ΠΠ		20	
SFlash 20 SIOO	2.5u tu		35,5u			ւսու	ء ۱	.09u		2.5	
21 SIO1			50u						24		
22 SIO2			42.065u					8.9	2u		
23 SIO3			42.06u					8.9	14u		
Label Channel	•										►
CH-00 CH-00 CH-01 CH-00	SFlash(Serial F	ilash) 💌									
Timestamp	Command(h)		Addr(h)	PEM(h)	DO	D1	D2	D3	D4	D5	D
).0001265 ສ	(35)Read Status Registe	r-2			02						
0.000144 S	(20)Sector Erase (4KB)		000000								
).0001775 S	(05)Read Status Registe				03						
0.000195 %	(35)Read Status Registe				02						
).0002125 S).00023 S	(05)Read Status Registe (35)Read Status Registe			03							
0.00023 5 0.0002475 5	(05)Read Status Registe				02						
•	(00)nead bodoub negiboe										
				2550879458		5087945	68 <mark>A</mark> B			0 (3	st m n

Serial Flash decode within QPI mode.



Serial Flash data Comparison : Compare the Serial Flash data by the waveform



files.

Method: Create a file by text editor and save it as SFCmp.cfg in order to compare

with the real Serial Flash waveform to find the bug, the default path is "My

Documents\Acute"

Acute
🚱 🖓 🐌 \Documents \Acute 💽 🚱 Search
🔄 Organize 🔻 🔊 Views 👻
Name 🔺 🕶 Date modified 💌 Type 💌 Size 💌 Tags 💌
SFCmp.cfg
1 item

SFCmp.cfg information:

📓 SFCmp.cfg - Notepad									
File Edit Format View Help									
<pre>;; comment OrgFile=C:\Documents and Settings\Liu\My Documents\Acute\SF.bin OutFile=C:\Documents and Settings\Liu\My Documents\Acute\SD_cmp.bin OutLstFile=C:\Documents and Settings\Liu\My Documents\Acute\SF.lst CheckCmd=03, EB</pre>	<pre>;;Original file ;;LA output serial flash file ;;Compare result ;;The HEX command need to check.</pre>								

OrgFile=File_Path: Key in the file path of the original Serial Flash data file (.bin).

OutFile=File_Path: Key in the file path of the Serial Flash output file.

OutLstFile=File_Path: Key in the file path of the comparison result. The file name

will has extension ".lst".

CheckCmd=Serial Flash command: Key in the command in Hex that are separated

by commas.



Save the OrgFile to the OrgFile file path.

Acute	
G Documents Acute	2
🕘 Organize 🔻 🔜 Views 👻	(?)
Name 🔺 🔻 Date modified 👻 Type 🗣 Size 🗣 Tags 👻	
SF.bin SFCmp.cfg	
2 items	

Run the Serial Flash Bus Decode to capture the Serial Flash signal.

Eile Label 😤 🍞 💾 🛊	<u>W</u> aveform	Run Devic) D▼ <u>₩</u> ▼ <u>╄</u> ⊻ <i>4</i> 9 (∰)	69 - 🗐 🕻	🕄 🔐 😥	 - Ø	• S/R: 200	MHz
Time/Div: 30	ns								
Acquired: 15:	20:56.0		1 ms -4.651 ms	-4.651 ms -4.651		4.651 ms	-4.651 ms	-4.651 ms	
NAND	9 I/O0 10 I/O1 11 I/O2 12 I/O3 13 I/O4 14 I/O5 15 I/O6 Idle 16 I/O7 19 CLE 20 ALE 18 WE 21 RE 21 RE 24 CE1 34 J/B1		40n 40n 40n 80n 80n 80n 30n 10n 30n 10n	DO: FE DO: 93 0 10 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n 40n	40n 40n 40n 40n 40n 40n 40n 40n 40n	DO: 15 40n 80n 40n 40n 40n 40n 40n 80n	DO: EA 40n 40n 40n 40n 40n	· • •	DO: 38 0 400. 400. 400. 400. 300 00 00
Label	Channel Value								•
		NAND(Nand	Flash) 🔻						
Timestamp	Command		Row Address(h)	Column Address(h)	DO	D1 D2	2 D3	D4	D5 1 🔺
-0.00465	RANDOM DATA OI	TTDITT #2(FO)	00000B	0000	C3	3C 01		93	60
-0.00465	THEFOIL DATA O	01101 %2(20)	00000B	0008	C7	38 17		CA	35
-0.00465			00000B	0010	82	7D 20		E8	17 :
-0.00465			00000B	0018	8D	72 42		97	68
-0.00464			00000B	0020	89	76 40		A9	56 .
-0.00464			00000B	0028	C8	37 50	AF	97	68 . 🖵
•									
				🦚 <mark>-</mark> 930	0114 📕	687	790 <mark>A</mark> B	2423	24 <mark>©∭</mark> ∭

If the OutFile does not exit, it will copy the OrgFile to the OutFile and write the data



to it according to the CheckCmd.

Compare result:

Acute		
()	📙 \Documents\Acute 🔽 🛃 Search	
🕒 Organize		0
Name 🔶 👻 [D <mark>atemodified, +</mark> Type + Size + Tags +	
SF.bin	SF.lst SF_cmp.bin SFCmp.cfg	
	4 items	

The OutLstFile:

///) S	F.Ist	- Notep	ad				_	
File	Edit	Format	View	Help				
						Documents\Acute\2Mbit_origin.b Documents\Acute\2Mbit_origin_c		1
000 000 000 000 000 000 000	0132: 0143(0143(0143(0143(0143(0142) 0159(0159(1 0000 1 0000 0 0000	13A1: 1461: 148F: 1499: 14BB: 14DB: 14DB: 15C8: 15E2:	52 5 73 7 D3 D C3 C E3 E F3 F F3 F 32 3	01111111			
•								▼ //

The first column is the compared address from OrgFile, the second column is the

different address from OutFile.



Serial IRQ

The IRQ/Data serializer is a Wired-OR structure that simply passes the state of one or more device's IRQ(s) and/or Data to the host controller. The transfer can be initiated by either a device or the host controller. A transfer, called an IRQSER Cycle, consists of three frame types: one Start Frame, several IRQ/Data Frames, and one Stop Frame. This protocol uses the PCI Clock as its clock source and conforms to the PCI bus electrical specification.

Settings

Seriali	zed IRQ Setting 🛛 🗙
Channel	CLOCK CH 0 IRQSER CH 1
Color —	Show Repeat Frame
	Start Frame Stop Frame Assert Frame Dessert Frame
Range	Decode Range From To Buffer Head Buffer Tail Default Ok Cance

CLOCK: PCI Clock channel

IRQSER; IRQSER channel

Normal: Not show repeat frame



Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10286946	22830	Continue mode		Α					Α						Α				
10291906	22841	Continue mode		Α											Α				
10404663	23091	Continue mode		Α					Α						Α				
10415039	23114	Continue mode		Α											Α				
10459240	23212	Continue mode		Α					Α						Α				
10461943	23218	Continue mode		Α											Α				
10580112	23480	Continue mode		Α					Α						Α				
10590037	23502	Continue mode		Α											Α				
10634238	23600	Continue mode		Α					Α						Α				
10636941	23606	Continue mode		Α											А				

Show repeat frame

Clock	No.	Mode	0	1	SMI	3	4	5	6	7	8	9	10	11	12	13	14	15	IRQ
10457887	23209	Continue mode		А											А				
10458338	23210	Continue mode		Α											Α				
10458789	23211	Continue mode		Α											Α				
10459240	23212	Continue mode		Α					Α						Α				
10459690	23213	Continue mode		Α					Α						Α				
10460140	23214	Continue mode		Α					Α						Α				
10460590	23215	Continue mode		Α					Α						Α				
10461041	23216	Continue mode		Α					Α						Α				
10461492	23217	Continue mode		Α					Α						Α				
10461943	23218	Continue mode		Α											Α				
10462394	23219	Continue mode		Α											Α				
10462846	23220	Continue mode		Α											Α				
10463298	23221	Continue mode		Α											Α				

Advance:

Clock	IRQ/Data Frame	Signal Sampled	# of clocks past Start
-9470	1	IRQO	2
-9452	2	IRQ1	5
-9434	3	SMI#	8
-9416	4	IRQ3	11
-9398	5	IRQ4	14
-9380	6	IRQ5	17
-9362	7	IRQ6	20
-9344	8	IRQ7	23
-9326	9	IRQ8	26
-9308	10	IRQ9	29
-9290	11	IRQ10	32
-9272	12	IRQ11	35
-9254	13	IRQ12	38
-9236	14	IRQ13	41
-9217	15	IRQ14	44
-9199	16	IRQ15	47
-9181	17	IOCHCK#	50
-9163	18	INTA#	53
-9145	19	INTB#	56
-9127	20	INTC#	59
-9109	21	INTD#	62
-9019	1	IRQ0	2
-9001	2	IRQ1	5

Result

Normal mode



cquired: 10:23:0		14.372 ms 14	.372 ms		14.372 ms		14.372	2 ms	14.37	2 ms	14.	372 ms		14.37	2 ms	14	.372 m	s .
	Sto	p Idle	Start		IRC	20	IF	RQ1-A	s	MI#	I	Q3		IRQ4		IRC	25	
SERIRQ																		
Sorialized IRQ		90n 120n			155n		30г	Ľ				4251	n					
																		Ī
Label	Channe																	
																		_
CH-00 CH-00 CH-01 CH-00 CH-01 CH-00		🕺 SERIRQ(Serialize	d IRQ)	-														
Timestamp	No.	Mode	0	1	SMI	3	4	5	6 7	8	9	10	11	12	13	14	15	IRC
13.753855 ms	6121	Continue mode		A										A				
14.371745 ms	6395	Continue mode		A					A					A				
14.40783 ms	6411	Continue mode		A										A				
14.633355 ms	6511	Continue mode		A					A					A				
14.649125 ms	6518	Continue mode		A										A				
15.23773 ms	6779	Continue mode		A					A					A				
15.29862 ms	6806	Continue mode		A										A				
15.517365 ms	6903	Continue mode		A					A					A				
15.53088 ms	6909	Continue mode		A										A				
16.121735 ms	7171	Continue mode		A					A					A				
16.182625 ms	7198	Continue mode		A										A				
16.401375 ms	7295	Continue mode		A					A					A				
16.41489 ms	7301	Continue mode		A										A				
•																		ъſ
																		_

Normal mode(Show repeat frame)

Time/Div: 60 ns Acquired: 10:23:	7. 0	14.372 ms	14.372 ms	5.	14.372 ms	1	14.372	2 ms	14.3	72 m	s .	14.3	72 ms		14.372	2 ms	. 14	4.372 m	15	
SERIRQ	2 CLK		Start					:Q1-A	1	MI#			425		IRQ4		IRC			•
Serialized IRQ	Channe 1		2011		1551		501						4251							•
CH-00		SERIRQ(Seria	lized IRQ) 0		SMI	3	4	5	6 7	,	8	9	10	11	12	13	14	15	IRC	•
14.36949 ms	6394	Continue mode		A	JIII	3	4	3	0 .		0	9	10	-11	A	13	14	10	IRC	_
14.36949 ms 14.371745 ms	6394	Continue mode		A					2						A					
14.371745 ms 14.374 ms	6396	Continue mode		A					A A						A					
14.37626 ms	6397	Continue mode	-	A					A A						A					
14.37852 ms	6398	Continue mode		A					A						A					
14.38078 ms	6399	Continue mode		A					A						A					
14.383035 ms	6400	Continue mode	-	A					A						A					
14.385295 ms	6401	Continue mode		A					A						A					
14.38755 ms	6402	Continue mode		A					A						A					
14.3898 ms	6403	Continue mode		A					A						A					
14.392055 ms	6404	Continue mode		A					A						A					
14.394305 ms	6405	Continue mode		A					A						A					
14.396555 ms	6406	Continue mode	2	A					A						A					•
•																			▶	
																				-



Advance mode

Time/Div: 60 ns	1			
Acquired: 10:23:0	· · · · · · · · · · · · · · · · · · ·	14.372 ms 14.372	ms 14.372 ms 14.372 ms	14 372 ms 14 372 ms 14 372 ms
Acquired. 10.25.0	····			14.372 ms 14.372 ms 14.372 ms
SERIRQ 2		Start	IRQU IRQI-A SMI#	IRQ3 IRQ4 IRQ5
3 Sorialized IRO	IRQ 90n	120n 155	300	425n
Label	Channe			I
O/Ⅲ CH-00 CH-00 CH-01 CH-00		erialized IRQ) 💌		
Timestamp	IRQ/Data Frame	Signal Sampled	# of clocks past Start	
14.371445 ms	21	INTD#	62	
14.371895 ms	1	IRQO	2	
14.371985 ms	2	IRQ1	5	
14.372075 ms	3	SMI#	8	
14.372165 ms	4	IRQ3	11	
14.372255 ms	5	IRQ4	14	
14.372345 ms	6	IRQ5	17	
14.372435 ms	7	IRQ6	20	
14.372525 ms	8	IRQ7	23	
14.372615 ms	9	IRQ8	26	
14.37271 ms	10	IRQ9	29	
14.3728 ms	11	IRQ10	32	
14.37289 ms	12	IRQ11	35	
•				
			A 34298 B	2315 B 31983



Serial General Purpose Input Output (SGPIO)

The SGPIO is a method to serialize general purpose IO signals. SGPIO defines the communication between an initiator and a target.

Settings

SGPIO	Settings	5			×
Channel	Load	CH 0 CH 1 CH 2 CH 2 CH 3	Color	Setting transmitter's Load Data Data Decode Range From To Buffer Head Buffer Tail]
				Default OK Cancel	

Channel: Show the selected channels (Clock, Load and Data), it can only use data out or date in or both.

Result:

Click OK to run the Smart Card decode and see the result on the Waveform Window below.



cquired: 13:	35:2 5.924	ms 	9.201 ms 12.477	ms 15.754 ms	19.031 ms 22	.308 ms 25.585 i	ms 28.861 ms
	DI: 3 DI:	6 DI: 1	DI: 2 DI: 3 DI: 7	DI:0 DI:3 DI:6 D	DI: 1 DI: 2 DI: 3	DI: 7 DI: 0 DI: 3	DI: 6 DI: 1 DI: 2
oc							
					1000000000		
SGPIO 1 L	pad		8.081m		8.081m		
2 D	0	15m 1.52	5m 1.475m 1.	12m 1.515m	1.525m	1.475m 1.12m	1.515m 1.525m
3 D	I 1.335m 1.775m	3.205	im 3.7m	1.335m 1.775m	3.205m 3.7	/m 1.335m 1	.775m 3.205m 7
SGPIO							
Label Ch	annel 💶						•
Э/Ш <u>Сн-00</u> с	H-00 RAR Bus	SGPIO(S	GPIO)				
			A statistic track ODer SA	Lange (ODer 1)	Te (1 (oper o)		
Timestamp	Device	LOAD	Activity(ODn.0)	Locate(ODn.1)	Fail(ODn.2)	ID	· · · · · · · · · · · · · · · · · · ·
		LUAD	No Activity	Locate (ODN.1)	Fail (0Dn.2)	ID Enable	
0.005198845 :	5 Device l	LUAD			· · ·		
0.005198845 : 0.006699005 :	5 Device 1 5 Device 2	LUAD	No Activity	Locate	Fail	Enable	
0.005198845 : 0.006699005 : 0.008199165 :	5 Device 1 5 Device 2		No Activity Activity	Locate No locate	Fail OK	Enable No connect	
0.005198845 0.006699005 0.008199165 0.00969932 \$	5 Device 1 5 Device 2 5 Device 3		No Activity Activity No Activity	Locate No locate Locate	Fail OK OK	Enable No connect No connect	
0.005198845 : 0.006699005 : 0.008199165 : 0.00969932	5 Device 1 5 Device 2 5 Device 3 Device 4		No Activity Activity No Activity Activity	Locate No locate Locate Locate	Fail OK OK OK	Enable No connect No connect Enable	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 \$ 0.01119948 \$ 0.011269964 \$	5 Device 1 5 Device 2 5 Device 3 0 Device 4 0 Device 5 0 Device 6	A	No Activity Activity No Activity Activity Activity	Locate No locate Locate Locate Locate	Fail OK OK OK Fail	Enable No connect No connect Enable Enable	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 \$ 0.01119948 \$ 0.01269964 \$ 0.014314815 3	5 Device 1 5 Device 2 5 Device 3 0 Device 4 0 Device 5 0 Device 6		No Activity Activity No Activity Activity Activity No Activity	Locate No locate Locate Locate Locate No locate	Fail OK OK OK Fail OK	Enable No connect No connect Enable Enable Enable	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 8 0.01119948 8 0.01269964 8 0.01269964 8 0.014314815 3 0.01581497 8	5 Device 1 5 Device 2 5 Device 3 5 Device 4 5 Device 5 5 Device 6 5 Device 0		No Activity Activity No Activity Activity No Activity Activity Activity	Locate No locate Locate Locate Locate No locate Locate	Fail 0K 0K 0K 0K 0K 0K 0K	Enable No connect No connect Enable Enable Enable Enable	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 \$ 0.01119948 \$ 0.01269964 \$ 0.014314815 3 0.01431497 \$ 0.01581497 \$	5 Device 1 5 Device 2 5 Device 3 Device 4 Device 5 Device 6 5 Device 0 Device 1		No Activity Activity No Activity Activity No Activity Activity Activity No Activity	Locate No locate Locate Locate Locate No locate Locate Locate	Fail OK OK OK Fail OK OK Fail	Enable No connect Enable Enable Enable Enable Enable Enable	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 8 0.01119948 8 0.01269964 8 0.01269964 8 0.01249487 8 0.01581487 8 0.01731513 8	5 Device 1 5 Device 2 5 Device 3 5 Device 4 5 Device 5 5 Device 6 5 Device 0 5 Device 1 5 Device 2		No Activity Activity No Activity Activity No Activity Activity Activity No Activity No Activity	Locate No locate Locate Locate No locate Locate Locate No locate	Fail 0K 0K 0K 0K Fail 0K Fail 0K	Enable No connect Enable Enable Enable Enable Enable Enable No connect	
Timestamp 0.005198845 : 0.006699005 : 0.008199165 : 0.00969932 \$ 0.0119948 \$ 0.0119948 \$ 0.01269964 \$ 0.014314815 : 0.01581497 \$ 0.01581497 \$ 0.01731513 \$ 0.01881529 \$ 0.02031545 \$	5 Device 1 5 Device 2 5 Device 3 5 Device 4 5 Device 4 5 Device 5 5 Device 6 5 Device 0 5 Device 1 5 Device 2 5 Device 3		No Activity Activity No Activity Activity No Activity No Activity No Activity No Activity No Activity	Locate No locate Locate Locate Locate No locate Locate No locate Locate Locate	Fail 0K 0K Fail 0K	Enable No connect Enable Enable Enable Enable Enable Enable No connect No connect	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 3 0.0119948 8 0.01269964 8 0.014314815 3 0.01581497 8 0.01581497 8 0.01581529 8 0.02031545 8 0.022181561 8	5 Device 1 5 Device 2 5 Device 3 5 Device 4 5 Device 4 5 Device 5 5 Device 6 5 Device 0 5 Device 1 5 Device 2 5 Device 3 5 Device 4		No Activity Activity No Activity Activity No Activity No Activity No Activity Activity No Activity No Activity No Activity	Locate No locate Locate Locate Locate No locate Locate No locate Locate Locate Locate	Fail 0K 0K 0K Fail 0K Fail 0K	Enable No connect Enable Enable Enable Enable Enable No connect No connect Enable	
0.005198845 3 0.006699005 3 0.008199165 3 0.00969932 \$ 0.0119948 \$ 0.01269964 \$ 0.01269964 \$ 0.01581497 \$ 0.01581497 \$ 0.01731513 \$ 0.01731513 \$ 0.01881529 \$ 0.02031545 \$	5 Device 1 5 Device 2 5 Device 3 Device 4 Device 5 Device 6 5 Device 0 Device 1 Device 2 Device 2 Device 3 Device 4 Device 5		No Activity Activity No Activity Activity Activity No Activity No Activity No Activity No Activity Activity Activity Activity	Locate No locate Locate Locate Locate Locate Locate No locate Locate Locate Locate Locate Locate	Fail 0K 0K	Enable No connect Enable Enable Enable Enable Enable No connect No connect Enable Enable	



Smart Card (ISO7816)

The card is made of plastic and provides strong security authentication for single sign-on within large organizations.

Settings

Smart (Card (ISO7816) Settings		×
Channel		Color	
1	CLK CH 0 + DATA CH 1 + ETU 372 Clock (16~2048)	Setting transmitter's color Start Data Parity	
Range	Decode Range	Stop	
###	From To Buffer Head 💌 Buffer Tail	•	
		Default OK Cancel	

Channel: Show the selected channels (CLK and DATA) and the number of clocks within the bit (ETU).

Result

Click **OK** to run the Smart Card decode and see the result on the Waveform Window below.



	Data: 11h	sto	P: OK Start		Data: 0h		STOP: OK	Start	Data: 0h
Smart Card									
1	DATA	185	.245u		923.755u		185,24u		
Smart Card									
Label	Channel								•
		C Smart Card	d(Smart Card	•					
⊙/∰ CH-00 CH-0 CH-01 CH-0	Data	Smart Card	d(Smart Card	Value					
CH-00 CH-00 CH-00 CH-01 CH-01 CH-00 Timestamp 1.88369 ms	Data 11011100	Parity 1	Error OK	Value 59					
CH-00 CH-01 CH-01 CH-01 CH-01 CH-01 Timestamp 1.88369 ms 4.64551 ms	Data 11011100 11101111	Parity 1 1	Error OK OK	Value 59 247					
CH-00 CH-01 CH-01 Timestamp CH-03 CH-04 1.88369 ms 4.64551 ms 5.75451 ms	Data 11011100 11101111 10001000	Parity 1 1 0	Error OK OK OK	Value 59 247 17					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms	Data Data 11011100 11101111 10001000 00000000	Parity 1 1 0 0	Error OK OK OK OK	Value 59 247 17 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms 7.972505 ms	Data Data 11011100 11101111 10001000 00000000 000000	Parity 1 1 0 0 0 0	Error OK OK OK OK OK	Value 59 247 17 0 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms	Data Data 11011100 11101111 10001000 00000000	Parity 1 1 0 0	Error OK OK OK OK	Value 59 247 17 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms 7.972505 ms	Data Data 11011100 11101111 10001000 00000000 000000	Parity 1 1 0 0 0 0	Error OK OK OK OK OK	Value 59 247 17 0 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms 7.972505 ms	Data Data 11011100 11101111 10001000 00000000 000000	Parity 1 1 0 0 0 0	Error OK OK OK OK OK	Value 59 247 17 0 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms 7.972505 ms	Data Data 11011100 11101111 10001000 00000000 000000	Parity 1 1 0 0 0 0	Error OK OK OK OK OK	Value 59 247 17 0 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms 7.972505 ms	Data Data 11011100 11101111 10001000 00000000 000000	Parity 1 1 0 0 0 0	Error OK OK OK OK OK	Value 59 247 17 0 0					
CH-00 CH-01 CH-0 Timestamp 1.88369 ms 4.64551 ms 5.75451 ms 6.86351 ms 7.972505 ms	Data Data 11011100 11101111 10001000 00000000 000000	Parity 1 1 0 0 0 0	Error OK OK OK OK OK	Value 59 247 17 0 0					



System Management Bus (SMBus)

The SMBus (SMB) is a two-wire bus.

Settings

SMBus Settings	×
Parameter Clock SMBCLK CH 0 SMBCLK CH 1 PEC PEC Address Address 7-bit addressing (Include R/W in Address) Report SMBus Show SBS(Smart Battery System) Show SPD(Serial Presence Detect) SPD Filter Find Peccede Range From To	Color Set the field's color in package Command Address Write / Read Start / Stop / Sr ACK / NACK PEC / Word / Byte Count Data / Content Word Address
Buffer Head 💌 Buffer Tail 💌	
	Default Ok Cancel

Clock: Show the selected channels (SMBCLK CH0 and SMBDATA CH1).

7-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit

addressing and 1-bit R/W).

Show SBS (Smart Battery System): Show the Smart Battery System: voltage,

electric current and the manufacturer.

Show SPD(Serial Presence Detect) : Report window show the configuration of

memory module(DDR3, DDR2, DDR, SPD SDRAM) in EEPROM.

SBS/SPD Filter: Report window only show SBS/SPD packet.

Ignore glitch: Ignore the glitch when the slow transitions.



Result

Click **OK** to run the SMBus Decode and see the result on the Waveform Window

below.

SMBus

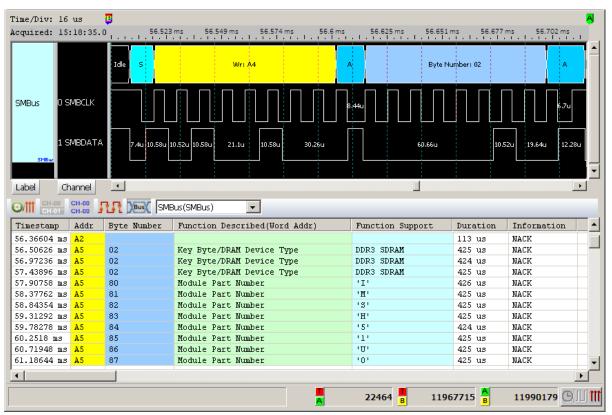
Time/Div: 16 us	5													
Acquired: 19:42:3	0.0	4.025 S	4.025	S 4.025 S	4.02	58 I	4.02	5 S	4.02	58 I	4.025	s	4.025 S	
SMBus O SMBO SMBw 1 SMBD Label Chann		9.79	d: 36	A Sr 9.825u 19.065u 10.925u 16	.460 9.75	J.J.	Addr:			R (7.6	7u	Data: 21	•
O/TT CH-00 CH-00 CH-01 CH-00		SMBus(9	6MBus)	•										
Timestamp	State	Address	Command	Byte Count	DO	Dl	D2	D3	D4	D5	D6	D7	ASCII(DO	
11.94276783 \$	Sr Rd	2D			82								•	
11.942984925 \$	S Wr	2D	00											
11.94305614 S	Sr Rd	2D		59 (Invalid)	02	00	01	00	AO	00				
11.95133274 S	S Wr	2D	11											
11.95140615 S	Sr Rd	2D			82								•	
11.951620105 \$	S Wr	2D	08											
11.95169101 \$	Sr Rd	2D		00 (Invalid)	00	00	01	01	00					
11.966087055 \$	S Wr	2D	11											
11.96616047 S	Sr Rd	2D			82								•	
11.96639074 S	S Wr	2D	00											
11.96646164 S	Sr Rd	2D		59 (Invalid)	02	00	01	00	AO	00				
11.98815673 S	S Wr	2D	11											-
11.98823171 \$	Sr Rd	2D			82								•	-
•													Þ	٢
					<mark>A</mark> 11	19789(0404	<mark>8</mark> 1	19789	0404	A B		0 🕒	



Acquired: 14:33:0	02.0	312.705 ms 312.833 ms	312.961 ms 313.089 ms 313.217 ms 313.345 ms	313.473 ms			
CH-OD 1 SMBCLK Addr: 0B A Cmd: 0A A Addr: 0E A Byte_L: F9 B B B B B B B B B B B B B B B B B<							
CH-01 CH-00	a ra r be						
	Addr	Function	Content	Unit	Durati 🔺		
Timestamp	Addr	Function	Content	Unit	Durati 🔺		
Timestamp 0.5937446 S	OB	AverageTimeToFull(13)	65535	minutes	1494 ı		
Timestamp 0.5937446 % 0.6249973 %	OB OB	AverageTimeToFull(13) ChargingCurrent(14)	65535 0	minutes mA	1494 i 1465 i		
Timestamp 0.5937446 \$ 0.6249973 \$ 0.6563065 \$	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 0	minutes mA mV	1494 ι 1465 ι 1557 ι		
Timestamp 0.5937446 % 0.6249973 % 0.6563065 % 0.6874855 %	OB OB	AverageTimeToFull(13) ChargingCurrent(14)	65535 0 0 4BD0h	minutes mA	1494 i 1465 i		
Timestamp 0.5937446 S 0.6249973 S 0.6563065 S 0.6874855 S 0.6874855 S	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 0 4EDOh Alarms (TERMINATE_CHARGE_ALARM	minutes mA mV	1494 ι 1465 ι 1557 ι		
Timestamp 0.5937446 % 0.6249973 % 0.6563065 % 0.6874855 %	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4BD0h Alarms (TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM	minutes mA mV	1494 i 1465 i 1557 i		
Timestamp 0.5937446 S 0.6249973 S 0.6563065 S 0.6874855 S 0.6874855 S 0.6874855 S	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4EDOh Alarms(TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM RENAINING_CAPACITY_ALARM	minutes mA mV	1494 ι 1465 ι 1557 ι		
Timestamp 0.5937446 S 0.6249973 S 0.6563065 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4BD0h Alarms (TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM	minutes mA mV	1494 i 1465 i 1557 i		
Timestamp 0.5937446 \$ 0.6249973 \$ 0.6563065 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4EDOh Alarms (TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM REMAINING_CAPACITY_ALARM REMAINING_TIME_ALARM)	minutes mA mV	1494 i 1465 i 1557 i		
Timestamp 0.5937446 \$ 0.6249973 \$ 0.6563065 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4EDOh Alarms(TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM REMAINING_CAPACITY_ALARM REMAINING_TIME_ALARM) Status(INITIALIZED	minutes mA mV	1494 i 1465 i 1557 i		
Timestamp 0.5937446 \$ 0.6249973 \$ 0.6563065 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$ 0.6874855 \$	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4EDOh Alarms(TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM REMAINING_CAPACITY_ALARM REMAINING_TIME_ALARM) Status(INITIALIZED DISCHARGING	minutes mA mV	1494 i 1465 i 1557 i		
Timestamp 0.5937446 \$ 0.6249973 \$ 0.6563065 \$ 0.687485	0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15)	65535 0 4EDOh Alarms(TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM REMAINING_CAPACITY_ALARM REMAINING_TIME_ALARM) Status(INITIALIZED DISCHARGING FULLY_DISCHARGED)	minutes mA mV	1494 i 1465 i 1557 i		
Timestamp 0.5937446 S 0.6249973 S 0.6563065 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S 0.6874855 S	0B 0B 0B 0B	AverageTimeToFull(13) ChargingCurrent(14) ChargingVoltage(15) BatteryStatus(16)	65535 0 4EDOh Alarms(TERMINATE_CHARGE_ALARM TERMINATE_DISCHARGE_ALARM REMAINING_CAPACITY_ALARM REMAINING_TIME_ALARM) Status(INITIALIZED DISCHARGING FULLY_DISCHARGED) Error(None)	minutes mA mV bit flags	1494 1 1465 1 1557 1 1467 1		

Show SBS (Smart Battery System)

Show SPD (Serial Presence Detect)





Serial Microprocessor Interface (SMI)

The SMI is a two-wire bus.

Settings

SMI Setting	s	×
Channel —		
📝 Cik	Data	
CH 0	▼ CH1 ▼	
Color		
Setting trans	smitter's color	
Attn		
Sel/Desel		
R/W		
Address		
Data		
Attn desel		
Range		
Decode Ra	ange	
From	То	
Buffer H	ead 💌 Buffer Tail 💌	- I
	Default OK Ca	ncel

Channel: Show the selected channels (Clk and Data)



Result

Time/Div: 32 u													
	1 647	c	1 647 9	1.54	17.5	1 647 9	1	647.9	1 648	c	1 648 9	1 648 9	
Acquired: 11:36		<u> </u>				1.047.0	<u>n Li Ĉ</u>	1		<u> </u>		1.0400	r - 1
	ATTN	DESEL		ADDR:4	40 DA	TA:00	DATA:00	DAT	A (C0	DATA:00		DESEL	Ê
SMI 1 Clk	17.1u	71.775u					15.8u					109,525u	
0 Data	34.265u	70,4u	,			117.595u				8.625u			
													-
Label Channel		-										•	
					_								
CH-00 CH-00 CH-01 CH-00		SMI(SN	4I)		•								
Timestamp	Sel/Desel	R/W	Addr	Data0	Datal	Data2	Data3	Data4	Data5	Data6	Data7	Information	
1.6469901 S	Sel	Write	80	00	00	00							
1.64723977 S	Desel	Read	40	00	00	CO	00	00					
1.6475705 \$	Desel	Read	40	40	00	CO	00	00					
1.647938985 \$	Desel	Read	40	80	00	CO	00	00					
1.64826971 S	Desel	Read	40	CO	00	CO	00	00					
1.648600435 \$	Desel	Read	41	08	00	00	00	00					
1.64893116 S	Desel	Read	41	48	00	CO	00	06					
1.04033110 5			-14										
1.650633285 S	Sel	Write	06	00	03	09	62						
	Sel Sel				03 40	09 CO	62 00	02					
1.650633285 S		Write	06	00				02					
1.650633285 S 1.65096401 S	Sel	Write Write	06 07	00	40	CO	00	02					
1.650633285 S 1.65096401 S 1.651294735 S	Sel Sel	Write Write Write	06 07 08	00 00 7E	40 00	C0 09	00 62	02					_
1.650633285 S 1.65096401 S 1.651294735 S 1.65166322 S	Sel Sel Sel	Write Write Write Write	06 07 08 09	00 00 7E 00	40 00 43	CO 09 00	00 62 00	02					
1.650633285 S 1.65096401 S 1.651294735 S 1.65166322 S	Sel Sel Sel	Write Write Write Write	06 07 08 09	00 00 7E 00	40 00 43	CO 09 00	00 62 00	02			1		-



Serial Peripheral Interface (SPI)

The SPI, is one kind of 4-wires synchronous serial data link. The SPI bus can be 4

wires, 3 wires, or 2 wires.

Settings

Type: The default is 3 Wire-SPI.

SPI Settings	X
Setting	
Туре	3 Wire-SPI
3 Wire-SPI	Chip Select Channel (CS) CH 0
Use External clock	Data Channel (SDA) CH 2
Clock Channel(SCK) CH 1	Chip Select Edge Data Edge
	Active Low Rising
	SDI(Write)-Latency-SDO(Read)
Bit Order MSB First	Write Length 8 Latency 2
Word Size 8 bit (4~40)	Read Length 8 (Bits)
Data valid from SCK 0 💽 S/R Clk	
Report	
Show Idle state in report window	
Show data in report 16 Column 💌	SDAXXXX
Color	
SDI/SDA/Write Channel	
SDO/Read Channel	
Range	
Decode Range	
Buffer Head 💌 B	uffer Tail
	Default OK Cancel

4 Wire-SPI dialog box →CS, SCK, SDI, SDO

4 Wire-SPI	
Chip Select Channel (CS	s) CH 0
Data Channel (SDI)	CH 0
Data Channel (SDO)	СН 0
Chip Select Edge	Active Low 💌
SDI Edge	Rising 💌
SDO Edge	Rising 💌
Show Data Channel	Both 💌
/CS SCK SDI SDO	



3 Wire-SPI dialog box → CS, SCK, SDA

3 Wire-SPI
Chip Select Channel (CS) CH 0
Data Channel (SDA) CH 0
Chip Select Edge Data Edge
Active Low 💌 Rising 💌
SDI(Write)-Latency-SDO(Read)
Write Length 8 Latency 2
Read Length 8 (Bits)
/cs

Click the SDI(Write)-Latency-SDO(Read) to show the dialog below.

The maximum length is 65535 (Bits)

SDI(Write)-Latency-SD	O(Read)
Write Length 8	Latency 8
Read Length 8	(Bits)
	Read

3 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDI, SDO

3 Wire-SPI(Unused Chi	ip Slave)
Data Channel (SDI)	CH 0 -
Data Channel (SDO)	CH 0
SDI Edge	Rising
SDO Edge	Rising
Frame guard time	300 ns
Show Data Channel	Both



2 Wire-SPI (Unused Chip Slave) dialog box -> SCK, S	2 \	Wire-SPI	(Unused	Chip	Slave)	dialog b	ox 🗲	SCK,	SD A
---	-----	----------	---------	------	--------	----------	------	------	-------------

2 Wire-SPI(Un	used Chip Slav	/e)	
Data Channel	(SDA)	CH 0	*
Data Edge	Rising	•	
DI SDI (Write	e)-Latency-SD	O(Read)	
Write Length	8	Latency 2	
Read Length	8	(Bits)	
Frame guard	time 30	0	ns
SCK	i hir x—x—		

If the chip slave is not used and the interval between frames is not 0. You can set the

interval as 6us, any data bit higher than 6us will be seen as Idle.

			ruuur	Ш
DATA 2 X SPI 2,0 X↓b 00	Idle AA Idle 84 Idle	00	Idle 00 Idle	
SP1 2,0 A+0	Late AA Late 34 Late	00		
SPI Settings	X	1		
Setting	_	1		
Туре	2 Wire-SPI(Unused Chip Slave)			
2 Wire-SPI(Unused Chip Slave)	Data Channel (SDA) CH 2			
Use External clock	Data Edge Rising 🗸			
Clock Channel(SCK) CH 1	SDI(Write)-Latency-SDO(Read)			
	Write Length 8 Latency 2			
Bit Order MSB First 💌	Read Length 8 (Bits)			
Word Size 8 bit (4~40)				
Data valid from SCK 0 V S/R Clk	Frame guard time 300 ns			
Report				
Show Idle state in report window				
Show data in report 16 Column 🗨				
Color				
SDI/SDA/Write Channel				
SDO/Read Channel				
Range				
From 1				
	o Buffer Tail			
	Default OK Cancel			

If the chip slave is not used and the interval between frames is 0. You can see the data continuous as the dialog below.



CLK D ↓ DATA 1 X SPI-2_wire SPI	
Setting Setting Yype 2 Wire-SPI(Unused Chip Slave) Use External clock Clock Channel(SCK) CH 1 Bit Order MSB First Word Size 8 bit (4~40) Data valid from SCK 0 S/R Clk Report	2 Wire-SPI(Unused Chip Slave) Data Channel (SDA) CH 2 Data Edge Rising SDI(Write)-Latency-SDO(Read) Write Length 8 Latency 2 Read Length 8 (Bits) Frame guard time 300 ns
✓ Show Idle state in report window Show data in report 8 Column Color ✓ ✓ SDI/SDA/Write Channel SDO/Read Channel ✓ Range ✓ ✓ Decode Range From To Buffer Head ▼	SDA

We also offer bi-direction mode as the dialog below.

SDI(Write))-Latency-SD	O(Read)	
Write Length	8	Latency 2	
Read Length	8	(Bits)	
Frame guard ti	me 0		ns

C heck the SDI(Write)-Latency-SDO(Read)to set the bit numbers for the 3 columns;



Write and Read (1~65535), Latency (0~65535).

Use External clock: Connect to the last channel of your instrument.

Use External clo	ck	
Clock Channel(SCK)	CH 0	- -
External Clock Chann	el at CH 35	

Bit Order: MSB first or LSB first.

Word size: Default is 8 bits, minimum is 4 and maximum is 32.

Report: Show Idle state in report window, You can disable this default for not to

display the idle state on the Report Window.

Show data in report: Display the ASCII code with default 16 columns on the Report Window.

Data Valid from SCK: In some SPI devices, the data is not valid right after the data output or the clock edge. You can set the data valid after 0-3 units of the sampling rate in Data valid from SCK; if the unit is 1 and the sampling rate is 200MHz, the delay time is 5 ns.

Result

Click **OK** to run the SPI decode and see the result on the Waveform Window below.

3-Wire SPI, Internal clock mode



cquired: 08:0	2.557 ms 2.557	ms 	2.558	ms I	2.558	ns III	2.559	ms 	2.559	ns 2.559 ms 2.56	6 ms
	Idle 0B 00 B0	67 00	00	00	00	00	00	00 🛔 0	0 00	00 00 00	Ide 0B 00
1 CS	100 1850 0000000000000000000000000000000									<u>nan ana ana ana ana ana ana ana ana ana</u>	1850
5PI		TANTANTANT	UUUUUUUUUUU		JULUUUUUUUU	ULUUUUUUU	ULUULUU <mark>.</mark> UU		000000000000		
O SDI	150n				2.	928u				15	52.5n
SPI 2 SDO	172.5n							2.47u			$\square \square$
SPI				1							
abel Channel										u	
MII CH-00 CH-0 CH-01 CH-0	SPI(SPI)		-]							
Fimestamp	Status(8 bits data)	DO	Dl	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Informati
2.5566025 ms	Unknown										
.5567225 ms	Idle										Duration:
.5569075 ms	Data	OB	00	BO	67	00	00	00	00	°g	
.5582925 ms	Data	00	00	00	00	00	00	00	00		
.5596825 ms	Unknown										
.5598 ms	Idle										Duration:
.559985 ms	Data	OB	00	BO	74	00	00	00	00	*t	
.561375 ms	Data	00	00	00	00	00	00	00	00		
.5627625 ms	Data	00	00	00	00	00	00	00	00		
.5641525 ms	Data	00	00	00	00	00	00				
.5651925 ms	Unknown										
.5653125 ms	Idle										Duration:

3-Wire SPI, External clock mode

SPI B8 5D 58 55 61 17 FC 43 94 B5 44 SPI CS 2 SDA 155 20 155 20 155 450 155 20 150 450 155 20 150 450 155 20 150 450 155 20 150 450 150 450 150 450 150 450 150 440 450 150 450 150 450 150 450 150 450 150 450 150 450 150 450 150 450 150 450 150 450 150 450 150 160 170 150 160 170 <t< th=""><th>cquired: 11:01:</th><th>1.792 ms 1.7</th><th>92 ms</th><th>1.792</th><th>2 ms</th><th>1.79</th><th>2 ms</th><th>1.79</th><th>2 ms</th><th>1.79</th><th>2 ms 1.792 ms</th><th>1.792 ms</th></t<>	cquired: 11:01:	1.792 ms 1.7	92 ms	1.792	2 ms	1.79	2 ms	1.79	2 ms	1.79	2 ms 1.792 ms	1.792 ms
span 2 SDA 15n 20n 15n 20n 15n 45n 15n 20n 15n 1		BB 5D	58	5	5	61		17	FC		43 94 E	35 4A
sr Channel SPI(SPI) Timestamp Status (8 bits data) D0 D1 D2 D3 D4 D5 D6 D7 ASCII (D0-D7) Informati 1.79202 ms Data B8 SD S8 S5 61 17 FC 43 ,]XUa.üC 1.79204 ms Data 94 B5 4A 4E 4D 80 1A A7< "µJNM€. S	SPI O CS	<u></u>										
Cheener Cheener SPI(SPI) Timestamp Status(8 bits data) D0 D1 D2 D3 D4 D5 D6 D7 ASCII(DD-D7) Informati 1.79202 ms Data B8 SD 58 55 61 17 FC 43 ,]XUa.ùC 1.79202 ms Data 94 B5 4A 4E 4D 80 1A A7 ~µuNM€.S 1.79206 ms Data A94 B5 4A 4E 4D 80 1A A7 ~µuNM€.S 1.79206 ms Data A9 AA 44 82 B1 C7 F8 38 éltE.Çø8 1.7928 ms Data A9 AA 44 82 E1 12 F5 0 Φ_1 , Δ_0 1.79280 ms Data 1.7928 Ma A4 44 82 E1 12 F5 0 Φ_1 , Δ_0 1.79280 ms Data 1.7 44 00 A1 27 61 F4		15n 20n 15n	20	▫_\\\		20n	15n		45n	15n	20n 15n	
CHOR SPI(SPI) Timestamp Status (8 bits data) D0 D1 D2 D3 D4 D5 D6 D7 ASCII (D0-D7) Informati 1.79202 ms Data B8 SD 58 55 61 17 FC 43 ,]XUa.ùC 1.792034 ms Data 94 B5 4A 4E 4D 80 1A A7 ~µuNM€.S 1.79206 ms Data P3 1.74 45 19 C7 F8 38 éltE.Çs8 1.79238 ms Data A9 AA 44 82 E1 12 F5 9C \$P1, A; & 1.79238 Data A9 AA 44 82 E1 12 F5 9C \$P1, A; & & 1.79238 Data A9 AA 44 82 E1 12 F5 9C \$P1, A; & & 1.79238 Data A1 44 82 E1 12 F5 Ture A1 76 F4 50												
Check Check SPI(SPI) Timestamp Status(8 bits data) D0 D1 D2 D3 D4 D5 D6 D7 ASCII(D0-D7) Informati 1.79202 ms Data B8 5D 58 55 61 17 FC 43 ,]XUa.ùC 1.79202 ms Data 94 B5 4A 4E 4D 80 1A A7 ~µuNM€, Ş 1.79266 ms Data E9 31 74 45 19 C7 F8 38 élte.Cq88 24 1.79266 ms Data A9 AA 44 82 E1 12 F5 9C \oplus^{1} , A_{1}^{*0} 26 1.79288 ms Data A9 AA 44 82 E1 12 F5 9C \oplus^{1} , A_{1}^{*0} 26 \oplus^{1} , A_{2}^{*0} 26 \oplus^{1} , A_{1}^{*0} 27 F8 82 \oplus^{1} , A_{1}^{*0} 28 28 29 A_{1}^{*0} 27 <t< td=""><td>Label Channel</td><td>•</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>	Label Channel	•										
TimestampStatus (8 bits data)D0D1D2D3D4D5D6D7ASCII (D0-D7)Informati1.79202 nsDataB85D58556117FC43,]XUa.ùC1.79234 nsData94B54A4E4D801AA7~µUNM€.S1.79266 nsDataE931744519C7F838éltE.Çø81.7928 nsDataA9AA4482BE12F59C $e^3D.4$ 1.7933 nsData34F73FD52D759749 $4\div0^2-u-I$ 1.79362 nsData8DF57E7A70886A47Dő-zp^*j61.79394 nsDataDataDEA2224CD5DE1C38 $b<2L\tilde{D}.8$ 1.79426 nsDataDEA2324CD5DE1C38 $b<2L\tilde{D}.8$ 1.79426 nsDataData66987C15752ACCA3 $-1u^{+1}A$ 1.79426 nsDataDataA874E335669E8291"täsfž,"1.79436 nsDataDataDEC61E40240FF739ME84.+91.7949 nsDataDataDEC61E40240FF739ME84.+91.79454 ns </td <td></td> <td></td> <td></td> <td>-</td> <td>1</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>				-	1							
1.79202 msDataDataB8SD58556117FC43,)XUa.iC1.79234 msData94B54A4E4D801AA7"µJNM€.S1.79266 msDataE931744519C7F838éltE.Çø81.79298 msDataA9AA4482BE12F59C $e^{a}D, %.õœ$ 1.7933 msData34F73FD52D759749 $4 \div 0^{2}-u-I$ 1.79362 msData174400A12761F450.D.; 'aôP1.79362 msDataBDF57E7A70886A47Dő-zp'j61.79364 msDataDataBDF57E7A70886A47Dő-zp'j61.79426 msDataDEA2324CD5DE1C38bc2LŐP.81.79426 msDataDEA2324CD5DE1C38bc2LŐP.81.79426 msDataDEA2324CD5DE1C38bc2LŐP.81.79426 msDataDataD6987C15752ACCA3.~1.u*1£1.79426 msDataDEC61E40240FF739bE8\$bc1.79438 msDataDEC61E40	CH-01 CH-01				-						1	
1.79234 msDataData94B54A4E4D801AA7"µJNM€.\$1.79266 msDataE931744519C7F838éltE.Çø81.79298 msDataA9AA4482BE12F59C $e^{+}D.$ 4.õœ1.7933 msData34F73FD52D759749 $4\div0^{-}u-I$ 1.79362 msData174400A12761F450.D.;'aôP1.79362 msData8DF57E7A70886A47Dő-zp'j61.79364 msDataDataBDF57E7A70886A47Dő-zp'j61.79426 msDataDEA2324CD5DE1C38 $b<210^{\circ} L$ 61.79426 msDataData06987C15752ACCA3.''u*i£1.79456 msDataDEC61E40240FF739bE84.+91.7949 msDataDEC61E40240FF739bE84.+91.79554 msDataA64FC9F570CD29E32E0É0jíjá.	Timestamn	Status(8 hits data)	DO	D1	D2	D3	D4	D.5	D6	D7	ASCIT(D0-D7)	Informati
1.79266 ms Data E9 31 74 45 19 C7 F8 38 éltE.Çø8 1.79298 ms Data A9 AA 44 82 EE 12 F5 9C e^D, %.õœ 1.79298 ms Data 34 F7 3F D5 2D 75 97 49 4÷0°-u-I 1.7933 ms Data 17 44 00 Al 27 61 F4 50 .D.; 'aôP 1.79362 ms Data 8D F5 7E 7A 70 88 6A 47 Dö-zp'j6 1.79394 ms Data DE A2 32 4C D5 DE 1C 38 bc2LÕ A bc2LÕ A 1.79426 ms Data DE A2 32 4C D5 DE 1C 38 bc2LÕ A c A </td <td>-</td> <td></td> <td>Informati</td>	-											Informati
.79298 ms Data A9 AA 44 82 BE 12 F5 9C *D,4,30e .7933 ms Data 34 F7 3F D5 2D 75 97 49 4+70-u-I .7936 ms Data 17 44 00 A1 27 61 F4 50 .D.; 'aôP .79364 ms Data 8D F5 7E 7A 70 88 6A 47 Dő-2p`jG .79426 ms Data DE A2 32 4C D5 DE 1C 38 bc2Lőb.8 .79426 ms Data 06 98 7C 15 75 2A CC A3 .'1.u*1£ .79458 ms Data 06 98 7C 15 75 2A CC A3 .'1.u*1£ .79499 ms Data A8 74 E3 35 66 9E 82 91 'tä5fž, ' .79522 ms Data Data DE C6 1E 40 24 0F </td <td>.79202 ms</td> <td>Data</td> <td>B8</td> <td>5D</td> <td>58</td> <td>55</td> <td>61</td> <td>17</td> <td>FC</td> <td>43</td> <td>,]XUa.üC</td> <td>Informati</td>	.79202 ms	Data	B8	5D	58	55	61	17	FC	43	,]XUa.üC	Informati
.7933 ms Data 34 F7 3F D5 2D 75 97 49 4+20-u-I .79362 ms Data 17 44 00 Al 27 61 F4 50 .D.; 'aôP .79364 ms Data 8D F5 7E 7A 70 88 6A 47 Dö-zp'jG .79426 ms Data DE A2 32 4C D5 DE 1C 38 62L0F.8 .79456 ms Data 06 98 7C 15 75 2A CC A3 .'I.u*1£ .7949 ms Data A8 74 E3 35 66 9E 82 91 'tä5fž,' .79522 ms Data DE C6 1E 40 24 0F F7 39 ME0\$ +9 .79554 ms Data 4F C9 F5 70 CD 29 E3 2E 0čôpíjá.	.79202 ms .79234 ms	Data Data	B8 94	5D B5	58 4A	55 4E	61 4D	17 80	FC 1A	43 A7	,]XUa.üC ″µJNM€.§	Informati
.79394 ms Data 8D F5 7E 7A 70 88 6A 47 Dö-zp'jG .79426 ms Data DE A2 32 4C D5 DE 1C 38 b<2LÖÞ.8	.79202 ms .79234 ms .79266 ms	Data Data Data	B8 94 E9	5D B5 31	58 4A 74	55 4E 45	61 4D 19	17 80 C7	FC 1A F8	43 A7 38	.]XUa.üC ″µJNM€.§ éltE.Çø8	Informati
.79394 ms Data 8D F5 7E 7A 70 88 6A 47 Dö-zp^jG .79426 ms Data DE A2 32 4C D5 DE 1C 38 bc2Lõb.8 .79456 ms Data O6 98 7C 15 75 2A CC A3 .71.u*1£ .7949 ms Data A8 74 E3 35 66 9E 82 91 "täsfž," .79522 ms Data DE C6 1E 40 24 0F F7 39 ÞÆØş.+9 .79554 ms Data 4F C9 F5 70 CD 29 E3 2E 0Ěopíjã.	.79202 ms .79234 ms .79266 ms .79298 ms	Data Data Data Data	B8 94 E9 A9	5D B5 31 AA	58 4A 74 44	55 4E 45 82	61 4D 19 BE	17 80 C7 12	FC 1A F8 F5	43 A7 38 90	,]XUa.üC ″µJNM€.S éltE.Çø8 ⊛°D,¾.õœ	Informati
79426 ms Data DE A2 32 4C D5 DE 1C 38 b<2LÖD.8 79458 ms Data 06 98 7C 15 75 2A CC A3 .~1.u*1£ 7949 ms Data A8 74 E3 35 66 9E 82 91 "tä5fž," 79522 ms Data DE C6 1E 40 24 0F F7 39 bE0§.+9 79554 ms Data 4F C9 F5 70 CD 29 E3 2E 0É0píjä.	.79202 ms .79234 ms .79266 ms .79298 ms .7933 ms	Data Data Data Data Data	B8 94 E9 A9 34	5D B5 31 AA F7	58 4A 74 44 3F	55 4E 45 82 D5	61 4D 19 BE 2D	17 80 C7 12 75	FC 1A F8 F5 97	43 A7 38 90 49	.]XUa.üC ″µJIM€.S éltE.Ç∞8 © ^a D.%.õœ 4÷2Õ-u-I	Informati
7949 ms Data A8 74 E3 35 66 9E 82 91 "tă5fž," 79522 ms Data DE C6 1E 40 24 0F F7 39 ₩E0\$(+9) 79554 ms Data 4F C9 F5 70 CD 29 E3 2E 0Éôp1)ă.	79202 ms 79234 ms 79266 ms 79298 ms 7933 ms 79362 ms	Data Data Data Data Data Data	B8 94 E9 A9 34 17	5D B5 31 AA F7 44	58 4A 74 44 3F 00	55 4E 45 82 D5 A1	61 4D 19 BE 2D 27	17 80 C7 12 75 61	FC 1A F8 F5 97 F4	43 A7 38 9C 49 50	.]XUa.üC ″µJMM€.Ş éltE.Çø8 @°D,¼.õœ 4÷?Õ-u-I .D.;'aôP	Informati
1.79522 ms Data DE C6 1E 40 24 OF F7 39 ME0\$\$.+9 1.79554 ms Data 4F C9 F5 70 CD 29 E3 2E OÉöpí)ã.	79202 ms 79234 ms 79266 ms 79298 ms 7933 ms 79362 ms 79394 ms	Data Data Data Data Data Data Data	B8 94 E9 A9 34 17 8D	5D B5 31 AA F7 44 F5	58 4A 74 44 3F 00 7E	55 4E 45 82 D5 A1 7A	61 4D 19 BE 2D 27 70	17 80 C7 12 75 61 88	FC 1A F8 F5 97 F4 6A	43 A7 38 9C 49 50 47	,]XUa.ùC ~µJNM€.S éltE.Ç∞8 ⊕*D,%.õœ 4÷20-u-I .D.;'*ôP Dõ~zp^jG	Informati
1.79554 ms Data 4F C9 F5 70 CD 29 E3 2E 0Éõpí)ã.	L. 79202 ms L. 79234 ms L. 79266 ms L. 79298 ms L. 7933 ms L. 79362 ms L. 79344 ms L. 793426 ms	Data Data Data Data Data Data Data Data	B8 94 E9 A9 34 17 8D DE	5D B5 31 AA F7 44 F5 A2	58 4A 74 44 3F 00 7E 32	55 4E 45 82 D5 A1 7A 4C	61 4D 19 BE 2D 27 70 D5	17 80 C7 12 75 61 88 DE	FC 1A F8 F5 97 F4 6A 1C	43 A7 38 9C 49 50 47 38	,]XUa.ùC ~µJNM€.S éltE.Çø8 ⊕D,%.õœ 4÷20-u-I .D.;'aôP ∐ő-zp'jG ▷<2LÖÞ.8	Informati
	L. 79202 ms L. 79234 ms L. 79266 ms L. 79298 ms L. 7933 ms L. 79362 ms L. 79344 ms L. 79426 ms L. 79458 ms	Data Data Data Data Data Data Data Data	B8 94 E9 A9 34 17 8D DE 06	5D B5 31 AA F7 44 F5 A2 98	58 4A 74 44 3F 00 7E 32 7C	55 4E 45 82 D5 A1 7A 4C 15	61 4D 19 BE 2D 27 70 D5 75	17 80 C7 12 75 61 88 DE 2A	FC 1A F8 F5 97 F4 6A 1C CC	43 A7 38 9C 49 50 47 38 A3	,]XUa.ùC ~µJNM€.S éltE.Ç⊗8 ⊕P,¾.õœ 4÷2Ö-u-I .D.;'aôP Dö-zp'jG b<2LÖb.8 .~].u*Ì£	Informati
	L. 79202 ms L. 79234 ms L. 79266 ms L. 79298 ms L. 7933 ms L. 79362 ms L. 79394 ms L. 79458 ms L. 79458 ms	Data Data Data Data Data Data Data Data	B8 94 E9 A9 34 17 8D DE 06 A8	5D B5 31 AA F7 44 F5 A2 98 74	58 4A 74 44 3F 00 7E 32 7C E3	55 4E 45 82 D5 A1 7A 4C 15 35	61 4D 19 BE 2D 27 70 D5 75 66	17 80 C7 12 75 61 88 DE 2A 9E	FC 1A F8 F5 97 F4 6A 1C CC 82	43 A7 38 9C 49 50 47 38 A3 91	,]XUa.ùC ~µJNM€.S éltE.Çø8 @*D,¾.õœ 4+?Ö-u-I .D.;'aôP DÕ~zp^jG b<2LÕP.8 .^!.u*̱ `täSfž,`	Informati
	79202 ms 79234 ms 79236 ms 79298 ms 7933 ms 79362 ms 79394 ms 79426 ms 79458 ms 79459 ms 79452 ms	Data Data Data Data Data Data Data Data	B8 94 E9 A9 34 17 8D DE 06 A8 DE	5D B5 31 AA F7 44 F5 A2 98 74 C6	58 4A 74 44 3F 00 7E 32 7C E3 1E	55 4E 45 82 D5 A1 7A 4C 15 35 40	61 4D 19 BE 2D 27 70 D5 75 66 24	17 80 C7 12 75 61 88 DE 2A 9E 0F	FC 1A F8 F5 97 F4 6A 1C CC 82 F7	43 A7 38 9C 49 50 47 38 A3 91 39	.]XUa.üC ~µJNM€.S éltE.Ç%8 @*D,%.õœ 4+?Õ-u-I .D.;'aôP Dõ-zp^jG P<2LÕP.8 .~ .u*Ì£ ~č&Sfž,` ÞÆ@\$.+9	Informati



Serial Peripheral Interface NAND (SPI NAND)

SPI NAND Flash is a SPI/QPI interfaced NAND flash memory. The decoder translates the bus signal to command/address/data field to provide an easier way to exam the SPI NAND waveform.

Settings

SPI NAND Settings	x
Parameter Settings	
CS# Ch 0 + SCK Ch 1 + Winbond	-
SI/S00 Ch 2 ÷ SO/S01 Ch 3 ÷ W25N01GV	
WP/SO2 Ch 4 + HOLD#/SO3 Ch 5 +	
Start up reading mode Continuous Read 💌	
Command deselect time 50ns	
Clock LOW to output valid 15ns	
Color	
OpCode Dummy	
Address Data In	
Data Out	
Range	
Decode Range	
From To	
Buffer Head 💌 Buffer Tail 💌	
Default OK Cancel	

CS#: Chip select

SCLK: Clock

SIO0 – SIO3: Data

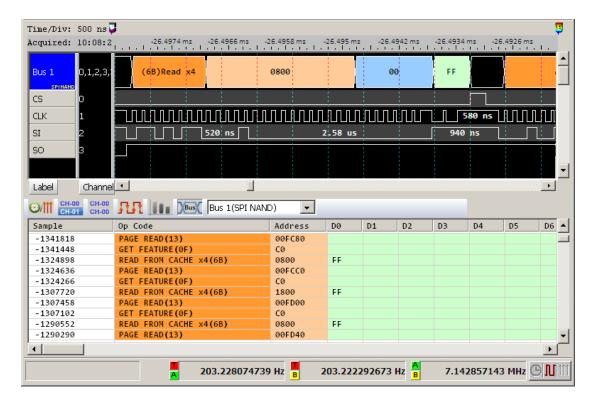
Start up reading mode: The initial setting of the reading mode for the decoder.

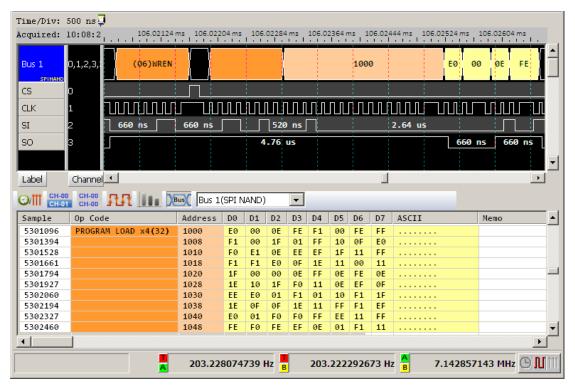
Command deselect time: The minimum required time for #CS deselecting. Clock

LOW to output valid: The data probe time after clock falling.



Result







SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals: Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame Synchronous (FS). The SSI protocol supports either the Normal or Network mode that is independent of whether the transmitter and the receiver are synchronous or asynchronous.

Settings

SSI Set	tings 🗾
Channel -	Select Channel SCK CH 0 • FS CH 1 • DATA CH 2 • Line Of Data
	Transmit C Receive
Color —	Merge continuous unknown Set color of data
	11 Hex 22 Hex 33 Hex
Danga —	44 Hex 🔽
Range —	Decode Range From To Buffer Head I Buffer Tail I
	Default OK Cancel

Select Channel: Show the selected channels.



Mode: Normal or Network.

Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

Result

Click **OK** to run SSI decode and see the result on the Report Window below.

Normal Transmit

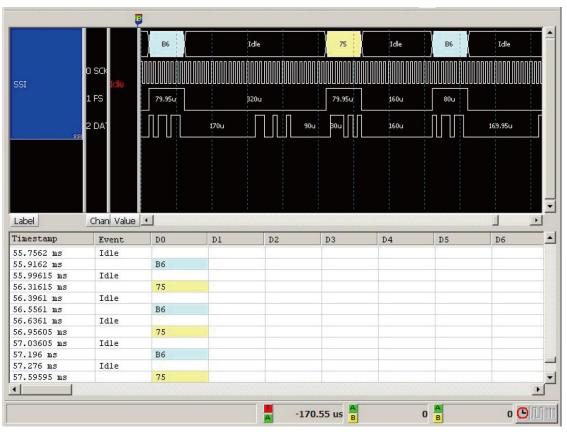
Time/Div: 80 u 📮									(9
Acquired: 08:00	3.89 n	ns 4.018 i	ms 4.146	ms 4.2	74 ms 4.402	ms 4.53 r	ms 4.658	ms 4.786	ims 	
	Idle 75	Idle	86 1000000000000000000000000000000000000		Idle NNN NNN NNN NNN	75	Idle	86 1000000000000000000000000000000000000	Idle	
O SCK										
SSI									1 1	
1 FS	80u	16Qu	80u		319.95u	80u	159.95u	80u		
2 DATA					339.95u	βου	159.95u			
	. 1									Ľ
Label Channel	<u>.</u>								•	
CH-00 CH-00 CH-00 CH-01 CH-00 CH-00		SSI(SSI)	•]						
Timestamp	Event	DO	Dl	D2	D3	D4	D5	D6	D7	
3.51955 ms	Idle									
3.8395 ms		75								
3.9195 ms	Idle									
4.0795 ms		B6								
4.1595 ms	Idle									
4.47945 ms		75								
4.55945 ms	Idle									
4.7194 ms		B6								
4.7994 ms	Idle									
5.11935 ms		75								
5.19935 ms	Idle									
5.35935 ms		B6								-
									Þ	
					_	3411 📕	3411	A B	0 🕒 🛙	₩



'ime/Div: 80 us	p]								
cquired: 08:00:	-3.9	504 ms -3.	376 ms -3.2	48 ms -3	.12 ms -2.99	2 ms -2.86	54 ms -2.7	36 ms -2.6	08 ms
	D9 Idle	Y i Y	dle 75	Idle		9 Idle	9B Id	1 1 1	Idle
O SCK SSI									
1 FS				230u		389 . 95u			
2 DATA 551	1		.95u B0u	160u		80u		u 30u	
Label Channel		:	: :				: :	:	
€H=01 CH-00 CH-00 CH-00		SSI(SSI)	•						
Timestamp	Event	DO	Dl	D2	D3	D4	D5	D6	D7
-3.7482 ms		B6	D9						
	Idle								
·3.5882 ms	rare								
	Idic	9B							
3.5082 ms	Idle	9B							
3.5082 ms 3.4282 ms		9B 75							
-3.5082 ms -3.4282 ms -3.34825 ms									
-3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms	Idle		D9						
-3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms -3.10825 ms	Idle	75	D9						
-3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms -3.10825 ms -2.9483 ms	Idle Idle	75	D9						
-3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms -3.10825 ms -2.9483 ms -2.8683 ms	Idle Idle	75 B6 9B	D9						
-3.5882 ms -3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms -3.10825 ms -2.9483 ms -2.8683 ms -2.7883 ms -2.7883 ms	Idle Idle Idle	75 B6	D9						
-3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms -3.10825 ms -2.9483 ms -2.8683 ms -2.7883 ms -2.7883 ms	Idle Idle Idle	75 B6 9B	D9						
-3.5082 ms -3.4282 ms -3.34825 ms -3.26825 ms -3.10825 ms -2.9483 ms -2.8683 ms -2.7883 ms	Idle Idle Idle Idle	75 B6 9B	D9						

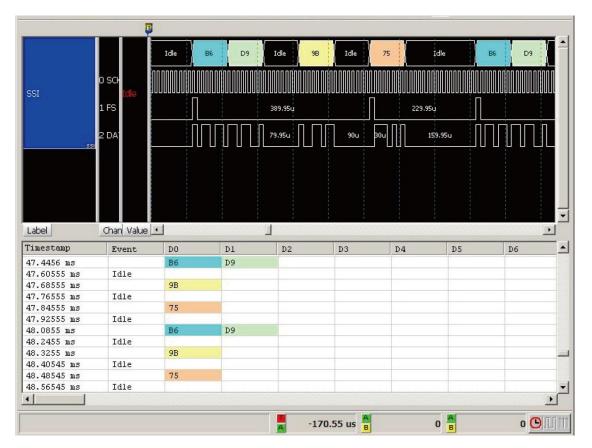
Normal Receive

Network Transmit





Network Receive





ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

Settings

ST766	9 Settings			×
Parameter	r		Color	
	Type 3 Wire-ST7669 Channel Chip Select Channel (/CS) Clock Channel (SCL) Serial Data Input (MPU SI) Serial Data Input (LCD SI) A0	▼ CH0 • CH0 · CH0 ·	D/C Comma Data Read	and
Range				
	Decode Range From Buffer Head	To Buffer Tail		
				Default OK Cancel

Channel: Show the selected channels.

Result

Click \mathbf{OK} to run the LCD1602 decode and see the result on the Waveform Window

below.



Acquired: 08:00:	00.0 67.165 ms	67.191 ms 67.216 ms	67.242 ms 67.267 n	ns 67.293 ms 67.319	ms 67.344 ms
	02 Unknown	03 Unknown 04	Unknown) 05	Unknown	1 01 T
0 Chip	Select 10u z	10u 28.99u	10u 28u	37.99u	42u
CH-00 1 SCL	20.99u	214	21.99u	 63,99u	
2 MPU	SI 35.99u	4u 32u	24.99u	78.99u	
3 LCD 9	SI				
517669					-
Label Chann	el +				
		i69) 🔽	_		
9/111 CH-01 CH-00 Timestamp		Data or Paramete	r/Command ID Da	ta(Read) ASCII	
67.13633 ms	0x00 (Command)	02			
67.17432 ms	0x00 (Command)	03			
67.21232 ms	0x00 (Command)	04			
67.25131 ms	0x00 (Command)	05			
67.3323 ms	0x00 (Command)	01			
67.36929 ms	Ox00 (Command)	02			
67.40729 ms	OxOO (Command)	03			
67.44528 ms	OxOO (Command)	04		-	
67.48427 ms	OxOO (Command)	05			
67.56526 ms	OxOO (Command)	01			
67.60226 ms	OxOO (Command)	02			
67.64025 ms	OxOO (Command)	03		•	
•					•



Serial VID Interface 2.0 (SVI2)

The SVI2 protocol is an interface for power management and developed by AMD. The SVI2 working voltage is between 1V to 1.6V and its maximum frequency is at 20MHz with 3 bits : SVC/SVD/SVT.

Settings

SVI2 Settir	ngs	×
Setting		
1	© SVI2.× O SVI1.×	
	SVC CH 0 SVD CH 1	SVT CH2
		Reduced Report
Color		
	Start / Stop	PSI1_L
	VDD Selector	
	VDDNB Selector	Load Line Slope Trim
	Acknowledge	Offset Trim
	PSIO_L	SVTO
	VID Code	SVT1
	VDD Voltage	VDD Current
	VDDNB Voltage	VDDNB Current
Range		
		
₩	Decode Range From	то
	Buffer Head	Buffer Tail
l		
		Default OK Cancel

SVC: SVI2 clock.

SVD: SVI2 data.

SVT: SVI2 telemetry data line. Telemetry will not be decoded if the SVT is not

checked.

SVI2.x / SVI1.x: Select SVI2 / SVI protocol to decode.

Reduced Report: Only show SVD / VOTFC packet in the report window.



Result

Click **OK** to run the SVI2 decode and see the result on the Waveform Window below.

Time/Div		- T										
Acquired	: 11:0	⁾⁹ ı.	96.	.225 us 9	96.325 ι	JS I.I	96.425 us	96.525 us 96	.625 us	96.725 us	96.825 us 96.929	Sus l
		Id	lle	s sv	T1: 1 SV	/T0; 1		VDD Volta	ge: 16D		VDDNB Vo	ltage: 139
SVI2	o svc			30n 20n 30	n 20n 30)n 20n (30n 20n 30n 20n 3	0n 20n 30n 20n 30n	20n 30n	20n 30n 20n 30n 20n 31	on 20n 30n 20n 30n 20n	30n 20n 30n 20n
3012	1 SVD											
SVI2	2 SVT		70r	<u>ا</u>	155n		50m 10)0n 50n	100n	50n 10	0n 100n	
3912												
												- -
Label	Chann											
	-											
©/∰ <u></u> ⊆	1-00 CI 1-01 CI	H-00 H-00	7.7 A.	Bus SVI2(9	SVI2)		-					
Timesta	mp \	VDD	VDDNB	VID Code	PSI	TFN	Slope Trim	Offset Trim	SVT	Volt	Volt/Current	Europe A
0.00004							STOPE IIIM	OFFDCC TFIM	241	1010	voic/currenc	Error 🔺
							wiope film	OTISCO TITM	3	0.87500V (16C)	1.20000V (138)	
0.00009	6						biope iiim	OTFOCC TITM	3 3	0.87500V (16C) 0.86875V (16D)	1.20000V (138) 1.19375V (139)	
0.00014	6 43 S						biope iiim	OTIDEE TITM	3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C)	1.20000V (138) 1.19375V (139) 1.20000V (138)	
0.00014	6 43 S 2						viope ilim		3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138)	
0.00014 0.00019 0.00024	6 43 S 2 0								3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138)	
0.00014 0.00019 0.00024 0.00028	6 43 S 2 0 8								3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138)	
0.00014 0.00019 0.00024 0.00028 0.00033	6 43 S 2 0 8 6								3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.86875V (16D)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138)	
0.00014 0.00019 0.00024 0.00028 0.00033 0.00038	6 43 S 2 0 8 6 4								3 3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.86875V (16D) 0.87500V (16C)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.19375V (139)	
0.00014 0.00019 0.00024 0.00028 0.00033	6 43 S 2 0 8 6 4 3								3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.8675V (16D) 0.86875V (16D)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.19375V (139) 1.20000V (138)	
0.00014 0.00019 0.00024 0.00028 0.00033 0.00038 0.00043	6 43 S 2 0 8 6 4 3 1								3 3 3 3 3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.86875V (16D) 0.86875V (16D) 0.86875V (16D)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.19375V (139) 1.19375V (139)	
0.00014 0.00019 0.00024 0.00028 0.00033 0.00038 0.00043 0.00048	6 43 S 2 0 8 6 4 3 1 9								3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.8675V (16D) 0.86875V (16D)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.19375V (139) 1.20000V (138)	
0.00014 0.00019 0.00024 0.00028 0.00033 0.00038 0.00043 0.00043 0.00048 0.00052	6 43 S 2 0 8 6 4 3 1 9								3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.86875V (16D) 0.86875V (16D) 0.86875V (16D) 0.86875V (16D)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.19375V (139) 1.20000V (138) 1.19375V (139)	
0.00014 0.00019 0.00024 0.00028 0.00033 0.00038 0.00043 0.00043 0.00048 0.00052 0.00057	6 43 S 2 0 8 6 4 3 1 9								3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	0.87500V (16C) 0.86875V (16D) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.87500V (16C) 0.86875V (16D) 0.86875V (16D) 0.86875V (16D) 0.86875V (16D) 0.86875V (16D)	1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.20000V (138) 1.19375V (139) 1.20000V (138) 1.20000V (138) 1.20000V (138)	

Show SVT

Without SVT

Time/Div: 30 Acquired: 11:	···· •	24	0.85 us 240.9	us	240.95 us	241 us	241.05 us	241.1 us	241.15 us	241.2 us	
			Const: 1D	-	/DD Sel: 1	VDDNB Sel: 0	Const: 1	N	PSI0_L: 0	VID Code: 27	
SVI2 0	svc	30n	20n 30n 2	:0n :	30n 20r	30n 20n	30n 20n	30n 20n	30n 20n	30n 20n 30n	
2 SVI2	SVD		100m		50r		100n		100n	50n	
216											-
Label (hannel 💻									<u></u>	
⊙/111 CH-00 CH-01	CH-00	Bus)	SVI2(SVI2)		•						
Timestamp	VDD	VDDNB	VID Code	PSI	TFN S.	lope Trim	Offset Trim	Error		Description	
0.000240	VDD(1)	0	1.30625V (27)					Invalid B	it Numbers!		
0.000288	VDD(1)	0	1.30625V (27)					Invalid B	it Numbers!		
0.000336	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		
0.000384	VDD(1)	0	1.30625V (27)					Invalid B	it Numbers!		
0.000433	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		
0.000481	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		
0.000529	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		
0.000577	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		
0.000625	VDD(1)	0	1.30625V (27)					Invalid B	it Numbers!		
0.000673	VDD(1)	0	1.30625V (27)					Invalid B	it Numbers!		
0.000721	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		
0.000769	VDD(1)	0	0.90625V (67)					Invalid B	it Numbers!		-
•										Þ	Ŀ
							120709385	120709	9385 <mark>A</mark>	0	11 11



Serial VID (SVID) (Upon Request)

Serial VID (SVID) protocol is for power management and developed by Intel. SVID

voltage is between 1.0V to 1.1V, maximum frequency at 26.25MHz and is 3 wires :

SCLK/ SDATA/ ALERT.

Supported version:

IMVP7/VR12, VR12.1, VR12.5, VR12.6

IMVP8/VR13

IMVP9/VR14

If you have any issues with SVID protocol features, please contact your Intel

Field Representative.

Settings

SerialVID Settings	X
Setting	
SCIK CHO 🕂 SData CH1 🕂 🗹 Alert CH2 🕂	
VR ControllerStartup	7
Single O Multiple PWM Spec. VR12.0(12.1)	
Not to decode the frame when its Fast slew rate 10 w/us	
Clock duty cycle is out of the Spec. range	
Color	
Start End	-
Address Turn around	-
Command ACK	•
MA. Payload SL. Payload	•
Parity Frame fill	•
Range	
Decode Range From To	
Buffer Head 💽 Buffer Tail 💌	
Default OK Cance	1



SClk: SVID clock.

SData: SVID data.

Alert: Alert, optional reminder.

VR Controller: Set single or multiple controllers in current VR. Set different address.

Not to decode the frame when its stop pattern wrong or clock duty cycle is out of range.

Result

Click OK to run the SVID decode and see the result on the Waveform Window

below.

Time/Div: 120 ns		6 us 70.46 us	70.66 us 70.86 us 71.06 us	71.26 us 71.4	46 us 71.66 us	Ų
	Y :					
	Idle Start	Addr:0 Cmd:GetRe	<mark>g(7)</mark> MA.PL:SR-slow(25) P:0 End Tu	n SL.PL:0	02 P:1	Idle
0 SClk SVID						340n
1 SData	40n40n	280n 120r	n 80n 40n 80n 40n 40n 40n 80n 170n	280n	40n 40n	
2 Alert						
SVID						
						_
Label Channel						
CH-00 CH-00	AA Des	SVID(SVID)	-			
Timestamp	Addr(h)	Command(h)	MA. Payload(h)	SL. Payload(h)	Ack	Error 🔺
0.06069 ms	0	SetRegDAT(6)	1.250V (C9)		ACK(2)	
0.06305 ms	1	SetRegADR(5)	Vout max(30)		NAK(1)	
0.06538 ms	1	SetRegDAT(6)	1.250V (C9)		ACK(2)	
0.06775 ms	0	GetReg(7)	SR-fast(24)	OA	ACK(2)	
0.07016 ms	0	GetReg(7)	SR-slow(25)	02	ACK(2)	
0.07253 ms	0	GetReg(7)	DC LL(23)		Rejet(3)	
0.07863 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.08472 ms	0	GetReg(7)	DC_LL(23)		Rejet(3)	
0.0908 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.09689 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.103 ms	1	GetReg(7)	DC_LL(23)		Rejet(3)	
0.16566 ms	1	SetVID-Decay(3)	0.000V (00)		Rejet(3)	-
·						
			9101	9105	A B	4 @IT[111



Serial Wire Debug (SWD)

The SWD is a 2-pin electrical alternative JTAG interface that has the same JTAG protocol on top. It uses the existing GND connection. SWD uses an ARM CPU standard bi-directional wire protocol, defined in the ARM Debug Interface v5.

Settings

SWD Parameter Setting) ×
Parameter Setting Channel Setting SWDIO CH 1 + SWDCLK CH 0 +	Show DP Reg bit assignments AP Setting Filter Setting Other JTAG-AP
AP Select Reg Startup Bank = 0	MEM-AP Show AP Reg bit assignments MEM AP Startup Endian Big TAR. Auto-Inc Off Access Size 32 Bits
Color	
DP / AP	▼ Park ▼
RnW	
Addr	▼ Data ▼
Stop	▼ Parity ▼
Range	
	To Buffer Tail
Default	OK Cancel

SWDIO: I/O data.

SWDCLK: Clock.

AP Select Reg Startup: When the AP Select Reg Startup is not assigned, only the



address information will be shown. You may input the Bank and Ctrl/Select initial values manually.

- AP Select Reg Startup						
Bank = 0	Time	Select	RnW	Address (h)	ACK	Data
	-0.0003 ms	AP	Write	0	OK	23 00 00 52
CtrlSel = 0						
- AP Select Reg Startup						
Bank = 0	.me Sel	ect RnW	Address	(h)	ACK	Data
	.0003 ms AP	Write	e Bank O	Register 0 (0)	OK	23 00 00 52
CtrlSel = 0						

Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

Select	RnW	Address (h)	ACK	Data						
DP	Write	SELECT Register (8)	OK	00 00 00 00						
				APSEL [31:24]	00					
				APBANKSEL [7:4]	0					
				CTRLSEL [0]	0					

AP Setting:

JTAG-AP: Show the JTAG AP decode.

MEM-AP: Show the MEM AP decode.

Other: Show Bank X Register X.

Other	Time	Select	RnW	Address (h)	ACK	Data
⊂ JTAG-AP	-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	ОК	23 00 00 52
C MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	Bank 0 Register 1 (4)	OK	00 00 02 68
O Other	Time	Select	RnW	Address (h)	ACK	Data
• JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
C MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	PSEL Register (4)	OK	00 00 02 68
O Other	Time	Select	RnW	Address (h)	ACK	Data
○ JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
S PIEPFAF	2.9998 ms	AP	Write	TAR Register (4)	OK	00 00 02 68

Show AP Reg bit assignments: Display the AP register information if JTAG-AP or

MEM-AP checked.



MEM-AP	Select	RnW	Address (h)		ACK	Data	
Show AP Reg bit assignments	AP	Read	BASE Register	(8)	OK	00 00 00 00	
						BASEADDR [31:12]	EOOFF
						Format [1]	1
						Entry present [0]	1

MEM AP Startup: Assign the initial MEM-AP value.

۰ ا	MEM-AP			AP	Read	DRW Register	(C)	OK	00 00 00 0D	TAR Address = E000EFF0
	Show AP Reg bit	assignmen	its						Big-Endian	
	MEM AP Startup								000D Access to E000EFF0	
	🔽 Endian	Big	–						0000 Access to E000EFF2	
		<u> </u>	-1	AP	Read	DRW Register	(C)	OK	00 00 00 E0	TAR Address = E000EFF2
	TAR Auto-Inc	Single	-						Big-Endian	
	Access Size	16 Bits	–						00E0 Access to E000EFF2	
		1							0000 Access to E000EFF4	

Filter Setting: Filter the unwanted Registers.

AP Setting Filter Setting							
Register Display List							
DP - ABORT Register							
DP - IDCODE Register							
DP - CTRL/STAT Register							
DP - WCR Register							
DP - SELECT Register							
DP - RESEND Register							
DP - ROUTESEL Register							
DP - RDBLIEF Register	Ψİ						

Result

Display the decoded waveform without the MEM-AP bit assignments.



cquired: 14:54:3	9.0		.999 ms 152.999	ms 153 ms	1.1.1	.53 ms	153.001 ms	153.001 m	s 153.)	002 ms		
		START	SELECT : AP	MODE : Write	AD	DR : TAR Re	egister	PARITY		STOP	PARK	
SWD 19	SWCLK	200	300n 300n	300n 200n	300n	300n 20	00n 300n	300n 30	0n 200n	300n	300n	
n s				500n	600	n		1.6u				
SWD						Ľ			_	_		-
Label Ch	hannel _	•									•	<u> </u>
⊙/∰ <u>CH-00</u> CH-00 CH-01 CH-00		Bus SWD	(SMD)	-								
				<u> </u>								- 10
Timestamp	Select	RnW	Address (h)			ACK	Data			Error	Message	
L52.9983 ms	AP	Write	TAR Register		(4)	OK	E0 00 H	ED FO				
53.0275 ms	AP	Read	DRW Register		(C)	OK	00 00 0	00 00				
153.0565 ms	DP	Read	RDBUFF Registe	r	(C)	0K	00 03 0	00 03				
155.9984 ms	AP	Write	TAR Register		(4)	0K	E0 00 H	CD FO				
156.0275 ms	AP	Read	DRW Register		(C)	0K	00 00 0	00 00				
156.0565 ms	DP	Read	RDBUFF Registe	r	(0)	OK	00 03 0	00 03				
158.9984 ms	AP	Write	TAR Register		(4)	OK	E0 00 H	ED FC				
159.0292 ms	AP	Write	DRW Register		(0)	0K	01 00 0	00 00				
159.0601 ms	DP	Read	RDBUFF Registe	r	(0)	0K	00 00 0	00 00				
164.9986 ms	AP	Write	TAR Register		(4)	0K	20 00 0	00 00				
l65.0295 ms	AP	Write	DRW Register		(C)	0K	EO OA H	3E 00				
165.0604 ms	AP	Write	DRW Register		(C)	0K	06 2D '	78 OD				
165.0913 ms	AP	Write	DRW Register		(C)	0K	24 08 4	40 68				
165.1221 ms	AP	Write	DRW Register		(C)	0K	D3 00 0	00 40				
165.153 ms	AP	Write	DRW Register		(C)	0K	1E 64 4	40 58				
165.1839 ms	AP	Write	DRW Register		(C)	OK	1C 49 I	01 FA				
•											Þ	

Display the decoded waveform with the MEM-AP bit assignments.

'ime/Div: 3 Cquired: 1		0 152.999	ms 152.999 r	ns I.I.I	153 ms 153 ms	153.001 ms	153.001 ms	153.002 ms	
		START	SELECT : AP	MODE :	Write ADDR : TAR Regi	ister	PARITY	STOP	PARK
SWD	1 SW	(CLK 200n 3	300n 300n	300n	200n 300n 300n 200r	n 300n 30	10n 300n	200n 300	n 300n
	o sw			500	n 600n		1.6u		
	SWD								
Label	Char	nnel 💶							
CH 00	_			_					
Э/Ш <u>Сн-00</u>	CH-00 CH-00	RR Dex SwD(Sw	D) ·	-					
Times	RnW	Address (h)		ACK	Data		Infoma	tion Erm	cor Message
194.23					STICKYCMP [4]		0		
94.23					TRNMODE [3:2]		0		
194.23					STICKYORUN [1]		0		
194.23					ORUNDETECT [0]		0		
196.99	Write	TAR Register	(4)	0K	E0 00 ED F0				
197.02	Write	SELECT Register	(8)	0K	00 00 00 10				
197.02					APSEL [31:24]		00		
197.02					APBANKSEL [7:4]		1		
197.02					CTRLSEL [0]		0		
197.05	Write	BD2 Register	(8)	OK	00 00 00 00				
197.08	Write	BD1 Register	(4)	OK	00 01 00 00				
197.11	Read	BDO Register	(0)	OK	00 00 00 00				
197.14	Read	BDO Register	(0)	OK	00 03 00 03				
197.17	Write	BD2 Register	(8)	OK	00 00 02 00				
197.20	Write	BD1 Register	(4)	OK	00 01 00 01				
197.23	Read	BDO Register	(0)	OK	00 00 00 00				
•									F
					6	8 📕	88 <mark>A</mark>		20 G.U



SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

Settings

SWP	Settings	×
Channel		
1	Channel S1 CH 0 S2 CH 1	
	Data Link Layer: O MAC O LLC	
Color		
	Setting transmitter's	
	SOF/EOF	
	Payload 🗾 💌	
	CRC16	
Range		
inn:	Decode Range	
* *	From	
	Buffer Head	
	To Buffer Tail	
	Default OK Cancel	

S1: I/O data.

S2: I/O data in current domain and it need convert to voltage domain.

Data Link Layer: Supported MAC and LLC layers



Result

Time/Div: 4 us	9		
Acquired: 18:59:01		20.954 ms 20.96 ms 20.966 ms 20.973 ms 20.979 ms 20.986 ms	20.992 ms 20.998 ms
	unknor		
SWP 6 S1			
8 S2			
211			
			T
Label Chan	ne		
()/111 CH-00 CH-00 CH-01 CH-00	ភភ	Bus (SWP(SWP)	
Timestamp	Туре	Payload	CRC16 Infomati(*
0.02089301 \$		ACT_SYNC(001): 0xffff	
0.02095216 \$	S1	62 01	6066
0.02095216 \$		ACT LPDU	
0.02095216 \$		FR(0): The UICC shall not repeat the last ACT frame	
0.02095216 \$		ACT_POWER_MODE(010): Full power(01)	
0.02103925 \$	S2	60	8D56
0.02103925 S 0.02103925 S		ACT LPDU	
0.02103925 5		<pre>INR(0): Contains the ACT_INFORMATION info ACT READY(000) from UICC</pre>	
0.02103925 5	S1	F9 04	7D9B
	51	12.04	
•			•
		A 4189268 B 418921	17 🔒 51 🕒 🕅



Universal Asynchronous Receiver/Transmitter (UART)

The UART (RS-232 or RS-485) protocol has two message types: Transmitter (TX) and Receiver (RX); you can measure the UART protocol in one signal or two signals. RS-485 need convert to logic signal, because LA can not capture differential signal.

Settings

Parameter Settings	Polarity Idle high 💌	-Line Wrap	Data Users can assign Line Wrap Data as header of data. Default setting is 0A. (Hexadecimal)
Rx CH 1 Auto Detect Baud Rate 9600 y Parity None y	Data Bits Stop Bits 1	Range	Line Wrap Data 1st Pattern Color OA 2nd Pattern OA
☐ MSB first 🔽	Show scale in the waveform		Decode Range From To Buffer Head v Buffer Tail v

Data: Show the selected channel (CH0).

Rx: Show Rx data in report window.

Auto: Shows High or Low when auto detection Idle.

Idle high: Idle condition shows High.

Idle low: Idle condition shows Low.

Auto Detect: Set the Baud Rate manually if not selected.

Baud Rate: Data rate (bits per second), and the range is 110 ~ 2M (bps).

Protocol: (Parity - Data Bits - Stop Bits)

Parity: N (None), O (Odd), or E (Even).



Data Bits: 5 to 10 bits.

Stop Bits: 1 to 2 bits.

MSB first: The default is LSB first; click it to change to MSB first.

Report Unknown and Idle: Display the unknown and idle data in the Report

Window.

Show scale in the waveform: Display the waveforms with scales.

Line Wrap Data: Use 1-2 value (hex) as header of data.



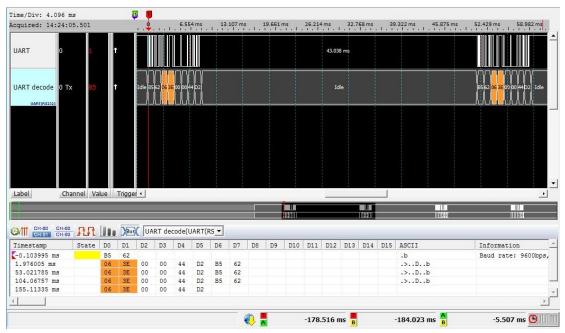
Result

Click **OK** to run UART Decode and see result on the Waveform Window below.

ime/Div: 1.024 ms	3																				
cquired: 14:03:00	8.930					-1.63	Bms	р. н. 1	g		1.638 m	s 	3.277	ms	4.91	5 ms	6.5	54 ms	8.192 ms	 9.83 ms	11.469 ms
UART 0	I		Ť												936 us	936 u	İ			43.038 ms	
UART decode 0 Tx	85		Ť			Id	le		BS		62	06	1	E	00	00		44	D2	Idle	
UNIT (12222)																					
Label Cha	nnel Va	alue	Tr	rigger	1				1												
	-					1011111												11			
3/111 CH-00 CH-00	-		Bus	(UA	ART de	code(l	JART(F	RS.▼				11									
Timestamp	State	DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	ASCII		Informat	ion
-51.149785 ms		B5	62	06	3E	00	00	44	D2		1							.b.>	D.	Baud rat	e: 9600bps
-0.103995 ms		B5	62	06	3E	00	00	44	D2									.b.>	D.		
50.941795 ms		B5	62	06	3E	00	00	44	D2									.b.>			
101.987585 ms		B5	62	06	3E	00	00	44	D2									.b.>			
		B5	62	06	3E	00	00	44	D2									.b.>	D.		
153.033375 ms																					0
153.033375 ms																					

Normal mode

Line Wrap Data mode





UNI/O

The UNI/O interface was developed by Microchip. The data transfer rate is 10Kbps to 100Kbps.

Settings

UNI/O Settings	×
Parameter	Color
Channel SCIO CH 0 Device Address 8 bits 12 bits Tolerance Input Edge Jitter Tolerance ±10% Output Edge Jitter Tolerance	Start Header MAK/NoMAK SAK/NoSAK Unknown Device Address Command Address Data
Report Setting Report Setting B Columns Range Pecode Range From To Buffer Head Buffer Tail	Hold Standby Pulse Default OK Cancel

Channel: Show the selected channels (SCIO CH0).

Device Address: Set data bits for the device address.

Tolerance: Set the Input / Output Edge Jitter Tolerance, $\pm 10\%$ / $\pm 25\%$ default.

Report Setting: To show the data by 8 or 16 columns in the Report Window.

Result

Click **OK** to run the UNI/O decode and see the result on the Waveform Window below.



Time/Div: 32 us Acquired: 08:00:00	0 10.816 ms 1	0.867 ms 10).918 ms 10.969 ms	11.02 ms 11.072 m	s 11.123 m	is 11.174 ms	
	Start Header MAK NSAK		Family:A0 Device:00		5АК	96(WREN)	
UNIZO	24.83u	25u 24.83u	J 25.25u	25.08u	25.25	25.08u	25u
							_
Label Chann							
CH-00 CH-00 CH-00 CH-01 CH-00 CH-00 Timestamp CH-00 CH-00	Device Address	D) -	Word Address MSB	Word Address LSB	D0 D1	D2 D3	D4 🔺
4.26766 ms	Family:A0 Device:00	91 (WRDI)	WOLD ADDIESS HAD	WOLD ADDEEDS BAD	20 21	DZ D3	1-1
11.10303 ms	Family:A0 Device:00	96 (WREN)					
12.52997 ms	Family:A0 Device:00	6D (ERAL)					
•							
			-	1273088 <mark>B</mark> 2	49088 <mark>A</mark> B	1024000 (9 JU 11



USB1.1

The USB 1.0 specification was introduced in 1994. USB signals are transmitted on a twisted pair data cable with 90 Ohm $\pm 15\%$ impedance, labeled D+ and D-.

Settings

USB1.1 Settings		<u>? ×</u>
USB1.1 Settings Parameter Channel D+ CH 0 CH 1 CH 1 CH 1 CH 1 CH 1 CH 1 CH 1 CH 1	Range Decode Range From Buffer Head Color Color Sync Packet ID Frame No. / Address / Endpoint/ Data CRC5/CRC16 EOP Host To Device / Device To Host Type Recipient	? ×
IN NACK OUT STALL DATAO PRE Show scale in the waveform	bRequest wValue wIndex wLength Descriptor	Default Cancel

Channel: Show the selected channels (D+ CH0 and D- CH1).

USB1.1 Setting: Select USB state (low speed or full speed) and decode the USB standard request and descriptor.

Result

Click **OK** to run the USB1.1 decode and see the result on the Waveform Window.



	Idle	SYNC	PID:SETUP	Ad	dress:01	Endpoint:(IO CRI	C5:17	OP I Idle	SYNC	
JSB1.1 0 D+		85n80n85n85n85n 245i	n 255n 165n B	5n 165n 85n80	85n 80n 85n 85n 8	5n80n85n	165n	335n 1	65n 170n	л 80n85n80n	85n
1 D-	800	85n85n80n85n85n 250	IN 250N 165N B				1650	670n		μ 80n85n85n	800
USB1.1					85n85n80n85n8						
											-
abel Chan	n										
		Bus USB1.1(USB1	1)								
CH-00 CH-00		Bus USB1.1(USB1	.1) 💌 Frame Number	Address	Endpoint	CRC 5	DATA				ASCI
	лл			Address	Endpoint	CRC 5	DATA	·			
CH-00 CH-00 CH-01 CH-00 imestamp	RR No.	PID	Frame Number	Address 01	Endpoint 00		DATA				_
CH-00 CH-00 CH-01 CH-00 Timestamp	No.	PID SOF(TOKEN)	Frame Number		-	1A		: 82 00 00	00 08 0		
MII CH-00 CH-00 imestamp .96344 ms .96644 ms	No. 1 2	PID SOF(TOKEN) SETUP(TOKEN)	Frame Number		-	1A		' 82 00 00	00 08 0		ASCI
CH-00 CH-01 CH-01	No. 1 2 3	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA)	Frame Number		-	1A		82 00 00	00 08 0		ASCI
CH-00 CH-00 imestamp .96344 ms .96644 ms .974995 ms .999935 ms	No. 1 2 3 4	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HAND SHAKE)	Frame Number 0718		-	1A 17		82 00 00	00 08 0		ASCI
.96344 ms .96644 ms .974995 ms .099385 ms .003185 ms	No. 1 2 3 4 5	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HANDSHAKE) SOF (TOKEN)	Frame Number 0718	01	00	1A 17 05	40 04	82 00 00		0 0	ASCI
.96344 ms .96344 ms .96644 ms .974995 ms .999935 ms .003185 ms .006185 ms	No. 1 2 3 4 5 6	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HAND SHAKE) SOF (TOKEN) OUT (TOKEN)	Frame Number 0718	01	00	1A 17 05	40 04			0 0	<u>ASCI</u>
CH-00 CH-00 CH-01 CH-00 CH-01 CH-00 CH-01 CH-01 CH-02 CH CH-02 CH CH-02 CH CH-02 CH CH CH CH CH CH CH CH CH CH CH CH CH C	No. 1 2 3 4 5 6 7	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HANDSHAKE) SOF (TOKEN) OUT (TOKEN) DATAI (DATA)	Frame Number 0718	01	00	1A 17 05	40 04			0 0	<u>ASCI</u>
CH-00 CH-00 CH-00 imestamp imestamp .96344 ms .96644 ms .974995 ms .999935 ms .003185 ms .003185 ms .006185 ms .0014745 ms .014745 ms .01985 ms	No. No. 2 3 4 5 6 7 8	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HAND SHAKE) SOF (TOKEN) OUT (TOKEN) DATAI (DATA) NAK (HAND SHAKE)	Frame Number 0718	01	00	1A 17 05 17	40 04 01 01		00 00 0	0 0	<u>ASCI</u>
96344 ms 96644 ms 974995 ms 999935 ms 003185 ms 003185 ms 014745 ms 01985 ms 01985 ms	No. No. 2 3 4 5 6 7 8 9	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HANDSHAKE) SOF (TOKEN) OUT (TOKEN) DATAI (DATA) NAK (HANDSHAKE) OUT (TOKEN)	Frame Number 0718	01	00	1A 17 05 17	40 04 01 01	00 00 05	00 00 0	0 0	<u>ASCI</u>
.96344 ms .96344 ms .96644 ms .974995 ms .999935 ms .003185 ms .006185 ms .014745 ms	No. No. 2 3 4 5 6 7 8 9 10	PID SOF (TOKEN) SETUP (TOKEN) DATAO (DATA) ACK (HAND SHAKE) SOF (TOKEN) OUT (TOKEN) DATAI (DATA) DATAI (DATA)	Frame Number 0718	01	00	1A 17 05 17	40 04 01 01	00 00 05	00 00 0	0 0	ASCI



USB PD 2.0

USB PD (Power Delivery) 2.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 100W, and the users can charge the device by supporting USB Type-C connector.

Settings

USB Power Delivery 2.0 Settings			×
Channel Configuration Channel (CC)	Color	Preamble SOP / EOP	
		Header	
Show 5b value in waveform window		Data Object(s) CRC	
Range Decode Range From Buffer Head	То	Buffer Tail	•
Def	fault	ОК	Cancel

Channel: Set Configuration Channel (CC).

Show 5b value in waveform window: Show 4b or 5b value in the waveform.



Result

Show 4b value.

Time/Div: 20 us										
		240,9 us 272,9 us 3	04.9 us 236.9 us 368.9 us	400.9 ut 412	9 L/E 44	64.9 us 496.9 us	\$28.9 us	560.9 us 592.9 us	624.9 us 656.9 us 638.9 us 720.9 us	752.9 us 784.9 us 816.9 us
Acquired: 19:2114	1.2				l					
USB PD CC	Preamble	SOP Hea	ader (3161) I	Data (0811917	!C)		Data (001	3C12C)	Data (0016412C)	CRC (AA4502A4)
VIRTO2 A										
CHOI CH-00 CH-00	AA IIII DOX I	USB PD(USB PD -								
Timestamp	SOP Sequence	Message Type	Port Data/Power Role	Cable Plug	Rev.	Message ID	Obj(s) Cnt	Data Obj(s)		
0.2134 ms	SOP	Source Capabilitie	DFP/SRC		2.0	0	3	Fixed supply; I	ORP(0); Volt.(05.00 V); Max./Oper	ra. current(03.00 A).
0.4801 ms									ORP(0); Volt. (12.00 V); Max./Oper	
0.6136 ms								Fixed supply; I	<pre>ORP(0); Volt.(20.00 V); Max./Oper</pre>	ca. current(03.00 A).
1.2491 ms	SOP		UFP/SNK		2.0	0	0			
6.0155 ms	SOP		UFP/SNK		2.0	0	1	Fixed and Varia	able Request; Obj. position(3); (GiveBack flag(0); Oper
6.7797 ms 10.5462 ms	SOP	GoodCRC	DFP/SRC DFP/SRC		2.0	1	0			
10.5462 ms 11.182 ms	SOP	Accept GoodCRC	UFP/SNK		2.0	1	0			
	SOP	PS RDY	DFP/SRC		2.0	2	0			
2011004 mB	002	20 101	DEETONO		2.0		•			

Show 5b value.

lime/Div: 10 us	1								
koquired: 19:21:4	1.2 256.9 us	272.9 us 288.9 us	s 304.9 us 320.9 us 336.9	us 352.9 us	368.9 us	384.9 us 44	0.9 us 416.9 us	432.9 us 448.9 us 464.9 us 4	80.9 us 496.9 us 512.9 us 528.9 us 544.9 us 560.
USB PD C	SOP		Header (15 09 0E 09)			Data (LE 12 09 09 13	: 09 14 1A)	Data (1E 1E 09 15 1A 09 14 1A)
U19702.2									
Label C	hann •								
		USB PD(USB PD -							
Timestamp			Port Data/Power Role	Cable Plug	Rev.	Message ID	Obi(s) Cnt	Data Obj(s)	
0.2134 ms 0.4801 ms 0.6136 ms	SOP	Source Capabi			2.0	0	3	Fixed supply; DRP(0); Volt Fixed supply; DRP(0); Volt	.(05.00 V); Max./Opera. current(03.00 A). .(12.00 V); Max./Opera. current(03.00 A). .(20.00 V); Max./Opera. current(03.00 A).
1.2491 ms	SOP	GoodCRC	UFP/SNK		2.0	0	0		
6.0155 ms	SOP	Request	UFP/SNK		2.0	0	1	Fixed and Variable Request	; Obj. position(3); GiveBack flag(0); Ope
	SOP	GoodCRC	DFP/SRC		2.0	0	0		
6.7797 ms		B	DFP/SRC		2.0	1	0		
10.5462 ms	SOP	Accept							
6.7797 ms 10.5462 ms 11.182 ms	SOP	GoodCRC	UFP/SNK		2.0	1	0		



Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic

entry system..

Settings

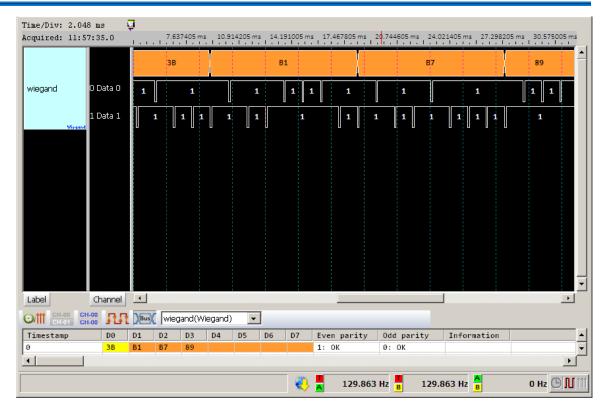
Wiega	nd Settings				×
Channel	Channel Data 0 CH 0 💌 Data 1 CH 1 💌	Color	Data Parity	•	
Range	Decode Range From Buffer Head To Buffer Tail				
			Default	OK Cance	

Channel: Show the selected channels (Data 0 and Data 1).

Result

Click **OK** to run the wiegand decode and see the result on the Waveform Window.







Chapter 2 Bus Trigger



Bus Trigger

Bus Trigger	TravelLogic B+	TravelLogic B	TravelLogic E	TravelLogic
CAN	0	0		\bigcirc
eSPI	\bigcirc			
I2C	\bigcirc	\bigcirc		\odot
128	\bigcirc	\odot	\odot	\odot
LIN	\bigcirc	\odot		
LPC	\bigcirc	\odot		
MIPI SPMI	\bigcirc			
NAND Flash	\bigcirc			
SD/eMMC	\bigcirc			
Serial Flash	\bigcirc			
SMBus/PMBus	\bigcirc	\bigcirc		
SPI	\bigcirc	\bigcirc		\odot
SVI2	\bigcirc	\bigcirc		
SVID	\bigcirc	\bigcirc		\odot
UART	\bigcirc	\bigcirc		\odot
USB 1.1	\bigcirc	\bigcirc		

The bus trigger are only available for the TravelLogic ULA-4G36 AL Series.



CAN Trigger

The settings dialog box below.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max -
- 🔄 CAN Trigger	1Hz	200MHz	Adjustable	256	Adju
—🗐 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
─	200MHz	200MHz	Fixed	Auto	Aub
- 🗐 CAN Trigger-36	1Hz	200MHz	Adjustable	256	2M
────── CAN Trigger-18	1Hz	200MHz	Adjustable	256	4M
───── CAN Trigger-12	1Hz	200MHz	Adjustable	256	6M
–	1Hz	200MHz	Adjustable	256	8M
────── CAN Trigger-6	1Hz	200MHz	Adjustable	256	12M
–≝ CAN Trigger-4	1Hz	200MHz	Adjustable	256	18M
────── CAN Trigger-2	1Hz	200MHz	Adjustable	256	36№
E CAN Trigger-1	1Hz	200MHz	Adjustable	256	72№
+ 🧰 I2C Trigger	1Hz	200MHz	Adjustable	256	Adju
+ 🧰 I25 Trigger	1Hz	200MHz	Adjustable	256	Adju
🗐 SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
+ 🧰 SPI Trigger	1Hz	200MHz	Adjustable	256	Adiu

Trigger Settings

Select CAN Trigger-36 where "-36" means 36 channels and the sample rate is always

10 times of data rate, then click OK. Click the Trigger Settings button (

Toolbar (or Device menu) to show the CAN Trigger Settings dialog box below.

CAN Trigger Setti	ngs X
Data Rate 400K	Channel O
Trigger On Start of Frame	-
CAN_L	C CAN_H
O 11 Bits ID O 29 Bits ID	0h
DATA Length 1	DATA Compare 📃 💌
DATA1 XXh	DATA2 XXh
DATA3 XXh	DATA4 XXh
DATA5 XXh	DATA6 XXh
DATA7 XXh	DATA8 XXh
Trigger on start of frame.	
Pre-Trigger	Pass Count: 0 🛨
Load Save Clear	All OK Cancel

Data Rate: Select a default data rate or run the CAN decode to measure the actual



data rate to enter (highly recommended). When the selected data rate is about 5%

Time/Div: 7.	68 📮														
Acquired: 08	:00	85.53 us	: 39 	98.33 us	411.13	us I .	423.93 u	s 	436.73 us	449.5	3us 462.	33 us 475.1	l3us 4	187.93 us 500).73 us
CAN		DAT	:F1		DAT:97			DAT:E	Ξ1		DAT:01	DAT	:9C	DAT:07	
	сан	,	10u	4.99u	5.01u	12.49			100	12.5	u 5u	4.99u 5.01u 7.	49u 12	2.51u 5u	7.5u
Label	•														
(CH-00) CH-01	Сн-00	Bus	CAN(CA	N)	•]							1		
Timestamp	Frame Type	ID	DLC	Data			CF	C(h)	ASCII (Da	ta)	Informati	lon		Frame Dur:	ation 🔺
0.30996 ms	Std Data	112	8	CD F1	97 El 01	90 07	7D 38	F5			Data Rate	e: 400 Kbps		282.46 us	
0.61991 ms	Std Data	112	8	CD F1	97 El 01	90 07	7D 38	F5						282.47 us	
0.92987 ms	Std Data	112	8	CD F1	97 El Ol	90 07	7D 38	F5	}	L			_	282.46 us	
•															
										_	7.99 us	B	98 us <mark>A</mark> B	90.01 us	<mark>⊖</mark>]]]]

deviation from the actual data rate will lead to CAN trigger failure.

Channel: Select channels.

Trigger On: Select the data field to trigger on:

Start of Frame

ID Match Data Frame

Remote Frame

Error Frame

Overload Frame

Stuffing Error

CRC Error

Data Value

Missing ACK

End of Frame

ID Match & Data Value

CAN_H/CAN_L: Select CAN_H or CAN_L as the trigger channel.

11 Bits ID/29 Bits ID: Data bits of the Identification field.

DATA Length: The number of transmitted data, by Byte unit.



DATA Compare: To compare the data.

DATA1 ~ DATA8: Data like binary codes (e.g. 01000001b), decimal codes (e.g. 65),

hexadecimal codes (e.g. 41h). If trigger on Date Value and need to pass some data,

please enter XX. For example: To trigger the data 38h in the third byte of data frame,

enter:

DATA Length = 3

DATA1 = XX

DATA2 = XX

DATA3 = 38h

Result

Acquirea	: 08:00:00.0	1		15.56 us	: 3 	21.96 ι	us I.I	328.	36 us 3	334.76 us 34	1.16 us 347	.56 us 39	3.96 us :	360.36 us
CAN	0 CAN	H SO	F				Bas	eID:112		R	.TR:0 IDE:0 R0:0	DLC	:8	DAT:CD
	CAN		7.5	L	2.5u	7	7.5u	2.	49u 5.01u	2.49u	10.01u	2.490	7 ^{/51u}	4.99u
Label	Chann	nel 💶												•
©/ 111 🔐	1-00 CH-00 R	R Bus	CA	N(CAN)		•							
Tim	Frame Type	ID	DLC	Data					CRC (h)	ASCII(Data)	Information		Frame Dur	ation 🔺
Tim 0.30	,	ID 112	DLC 8		. 97 EJ	L 01 :	9C 0'	7 7D	CRC (h) 38F5	ASCII(Data)	Information Data Rate:		Frame Dur 282.46 us	
0.30	,			CD FI	. 97 EJ . 97 EJ				· · · ·	· · · ·				
0.30 0.61 0.92	Std Data Std Data Std Data	112 112 112	8	CD FI CD FI		L 01 :	9C 0'	7 7D	38F5 38F5 38F5	}			282.46 us 282.47 us 282.46 us	
0.30 0.61 0.92 1.23	Std Data Std Data Std Data Std Data	112 112 112 112 112	8 8	CD FI CD FI CD FI	. 97 EJ	L 01 :	9C 0. 9C 0.	7 7D 7 7D	38F5 38F5 38F5 38F5 38F5	·····}			282.46 us 282.47 us 282.46 us 282.47 us	
0.30 0.61 0.92 1.23	Std Data Std Data Std Data	112 112 112	8 8 8	CD FI CD FI CD FI CD FI	97 EJ 97 EJ	L 01 9 L 01 9 L 01 9	9C 0' 9C 0' 9C 0'	7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5	·····} ·····}			282.46 us 282.47 us 282.46 us	
0.30 0.61 0.92 1.23 1.54 1.85	Std Data Std Data Std Data Std Data Std Data Std Data	112 112 112 112 112 112 112	8 8 8 8	CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ	97 EJ 97 EJ 97 EJ 97 EJ 97 EJ	L 01 2 L 01 2 L 01 2 L 01 2 L 01 2	9C 0 9C 0 9C 0 9C 0	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······}			282.46 us 282.47 us 282.46 us 282.47 us 282.46 us 282.47 us	
0.30 0.61 0.92 1.23 1.54 1.85 2.16	Std Data Std Data Std Data Std Data Std Data Std Data Std Data	112 112 112 112 112 112 112 112	8 8 8 8 8 8 8 8	CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ	97 E) 97 E) 97 E) 97 E) 97 E) 97 E) 97 E)	L 01 2 L 01 2 L 01 2 L 01 2 L 01 2 L 01 2	9C 0 9C 0 9C 0 9C 0	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······}			282.46 us 282.47 us 282.46 us 282.47 us 282.46 us 282.46 us 282.47 us 282.46 us	
0.30 0.61 0.92 1.23 1.54 1.85 2.16 2.47	Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data	112 112 112 112 112 112 112 112 112	8 8 8 8 8 8 8 8 8	CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ	97 EJ 97 EJ 97 EJ 97 EJ 97 EJ 97 EJ 97 EJ	L 01 2 L 01 2 L 01 2 L 01 2 L 01 2 L 01 2 L 01 2	9C 0 9C 0 9C 0 9C 0 9C 0	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······}			282.46 us 282.47 us 282.46 us 282.47 us 282.46 us 282.47 us 282.47 us 282.46 us 282.46 us	
0.30 0.61 0.92 1.23 1.54 2.16 2.16 2.47 2.78	Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data	112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112	8 8 8 8 8 8 8 8 8 8 8 8	CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	L 01 3 L 01 3	9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0'	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	· · · · · · · · · · · · · · · · · · ·			282.46 us 282.47 us 282.47 us 282.47 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us	
0.30 0.61 0.92 1.23 1.54 1.85 2.16 2.47 2.78 3.09	Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data Std Data	112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112 112	8 8 8 8 8 8 8 8 8 8 8 8 8 8	CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ CD FJ	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	L 01 2 L 01 2	9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0'	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	······} ······} ······}			282.46 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us 282.46 us	
0.30 0.61 1.23 1.54 2.16 2.47 2.78 3.09 3.40	Std Data Std Data	112 112 112 112 112 112 112 112 112 112	8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	CD FJ CD FJ	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	L 01 2 L 01 2	9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0'	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	· · · · · · · · · · · · · · · · · · ·			282.46 us 282.47 us 282.47 us 282.47 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us 282.47 us 282.46 us 282.47 us	
0.30 0.61 0.92 1.23 1.54 2.16 2.47 2.78 3.09 3.40 3.71	Std Data Std Data	112 112	8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	CD FJ CD FJ	97 E1 97 E1	L 01 2 L 01 2	9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0'	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	· · · · · · · · · · · · · · · · · · ·			282. 46 us 282. 47 us 282. 47 us 282. 46 us 282. 47 us 282. 46 us 282. 46 us 282. 46 us 282. 47 us 282. 46 us 282. 46 us 282. 46 us	
0.30 0.61 0.92 1.23 1.54 1.85 2.16 2.47 2.78 3.09 3.40 3.71	Std Data Std Data	112 112 112 112 112 112 112 112 112 112	8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	CD FJ CD FJ	97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1 97 E1	L 01 2 L 01 2	9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0' 9C 0'	7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D 7 7D	38F5 38F5 38F5 38F5 38F5 38F5 38F5 38F5	· · · · · · · · · · · · · · · · · · ·			282.46 us 282.47 us 282.47 us 282.47 us 282.47 us 282.46 us 282.46 us 282.46 us 282.46 us 282.47 us 282.46 us 282.47 us	



I²C Trigger

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
🗐 800M	800MHz	800MHz	9	256	8M
🗐 400M	400MHz	400MHz	18	256	4M
+ 🧰 200M	1Hz	200MHz	Adjustable	256	Adjustable
+ 🧰 UART Trigger	Baud Rate × 16	Baud Rate x 16	Adjustable	256	Adjustable
+ 🧰 CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
- 💼 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
—🗒 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
—🗒 Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
—	1Hz	200MHz	Adjustable	256	2M
—	1Hz	200MHz	Adjustable	256	4M
-🗒 I2C Trigger-12	1Hz	200MHz	Adjustable	256	6M
—	1Hz	200MHz	Adjustable	256	8M
—	1Hz	200MHz	Adjustable	256	12M
🔲 I2C Trigger-4	1Hz	200MHz	Adjustable	256	18M
+ 🧰 125 Trigger	1Hz	200MHz	Adjustable	256	Adjustable

The settings dialog box below.

Trigger Settings

Select I²C Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button () on Toolbar (or Device menu) to show the I²C Trigger Settings dialog box below.



I2C Trigger Setting	\$			×
Channel : SCL	0 SDA 1	Trigger Method:	Start	•
P1	▼ P2	▼ P3	▼ P4	Y
P5	▼ P6	P7	▼ P8	v
P9	▼ P10	▼ P11	▼ P12	~
P13	▼ P14	▼ P15	▼ P16	7
Timing Violation (Uni	it:ns / Range:5~163840ns) -			
LSU;STA 160	LSU;DAT 10	🗖 tSU;STO 🛛 160	🗖 tlow	160
tHD;STA 160	tHD;DAT 5	tBUF 500	🗖 thigh	60
Pre-Trigger	Data match with P1 Ad	dress 🔲 Pass Count Type	Pass Count	0 🗄
Clear All	Load Save		ОК	Cancel

Channel: Select two channels for the serial clock (SCK) and the serial data (SDA).

Trigger Method: Offer nine models for user to choose.

Start

Re-Start

Start or Re-Start

Stop

Missing Ack (Not Acknowledge (NACK))

For the first five ways of Trigger Method, Cursor T will stay at the beginning of the

condition as below if the trigger succeeds.





Match Sequentially: Similar to the Sequence Trigger, the I²C Trigger has up to 16

I2C Trigger Settings		×
Channel : SCL 0 SDA	1 Trigger I	Method: Match Sequently
P1 Next P2 The	nIf 🔽 P3 Nex	t 💌 P4 Next 💌
P5 Next P6 The	nIf P7 The	nIf 💌 P8 ThenIf 💌
P9 ThenIf P10 Nex	t P11 Nex	t 💌 P12 Then Trigger 💌
P13 Then Trigger P14 The	Trigger P15 The	n Trigger 💌 P16 Then Trigger 💌
Liming violation (Unitins) Rangers~153		160 LOW 160
thd;sta 160 🗖 thd;da	r 5 🗖 teuf	500 🗖 thigh 60
- P1 - P2 - P3 - P4 - P5 - P6	I P7 II P8 II P9 II P10	P11 - P12 →
		D D
		= =
xoth xoth xoth xoth xoth xoth	xxh xxh xxh xxh	xxh xxh
Pre-Trigger Data match wit	h Di Addanan 🗖 Darr Gar	unt Type Pass Count 0
Clear All Load Save	h P1 Address 🔲 Pass Cou	unt Type Pass Count 0

levels of sequential conditions below.

Click any condition (P1 ~ P16) and the I^2C Value Setting dialog box below will show.

Address:



I2C Value Setting	×
✓ Address (7-bit addressing) ○ Write Only ○ Read Only ○ Read or Write □ Include R/W in Address 7 6 5 4 3 2 1 R/W 0 1 0 0 1 1 X = 46h	Check Acknowledge
Data/Address 23h	OK Cancel

Write Only, Read Only or Read or Write. When Address is checked, it is the address

will be analyzed. Address starts from bit 1 without including R/W in address.

I2C Value Setting	×
Image: Address (7-bit addressing) C Write Only C Read Only C Read or Write Image: Include R/W in Address 7 6 5 4 3 2 1 R/W 0 0 1 0 0 1 X = 23h	Check Acknowledge
Data/Address 23h	OK

Address starts from bit R/W including R/W in address.

I2C Value Setting	×
 Address (7-bit addressing) C Write Only C Read Only C Read or Write Include R/W in Address 7 6 5 4 3 2 1 R/W X X X X X X X X X = 00h 	Check Acknowledge
Data/Address 12h Image: Comparison of the second sec	OK Cancel

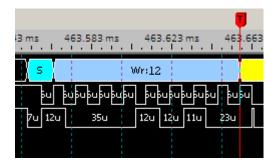
If Address is not checked, the data (Data 12h) will be analyzed.



Check Acknowledge: ACK (Acknowledge), NACK (Not Acknowledge). If the

Check Acknowledge is not checked, it can be either ACK or NACK.

Data/Address:



Data or Address can be in binary or hexadecimal code like 00010010b or 12h. Also, you can input X (Don't care) as the value; if the data is 10h, 20h, 30h, you can set X0h or 00XX0000b.

Cursor T will stay at the end of the condition as below if the trigger succeeds.

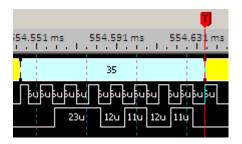
All Match: All input conditions must be satisfied to trigger.



I2C Trigger Settings				×
Channel : SCL 0	SDA 1	Trigger Method:	All Match	•
P1 Used 💌	P2 Used 🔻	P3 Unused	▼ P4 Unused	•
P5 Unused	P6 Unused 💌	P7 Unused	P8 Unused	•
P9 Unused	P10 Unused 💌	P11 Unused	P12 Unused	•
P13 Unused	P14 Unused	P15 Unused	P16 Unused	•
Timing Violation (Unit:ns / R				
🗖 tSU;STA 160	tsu;DAT 10	tsu;sto 160	🗌 tlow 🛛 160)
tHD;STA 160	tHD;DAT 5	tBUF 500	thigh 60	
P1 P2				
D D				
= = XXh XXh				
		E Page Court Trans	Data Caunt	
	ata match with P1 Address	Pass Councilype		0 🗄
Clear All Loa	d Save		ОК	Cancel

If P1 > 30h and P2 < 40, Cursor T will stay at the end of the condition as below if the

trigger succeeds.



Any Match: Any of input conditions is satisfied to trigger.

Timing Violation: There are eight timing values provided as the trigger condition. If

the timing of the signal is less than the input value, then the instrument will trigger.

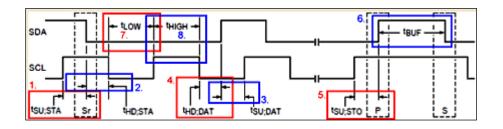
For this function, the 200MHz timing analysis is strongly recommended for better

resolution.



I2C Trigger Settings				×
Channel : SCL 0	SDA 1	Trigger Method:	Timing Violation	
P1 🔻	P2	P3	▼ P4	V
P5 💌	P6	P7	▼ P8	y
P9 🔽	P10	P11	▼ P12	_
P13	P14	P15	▼ P16	Y
Timing Violation (Unit:ns / F	Range:5~163840ns)			
tsu;sta 160	tsu;DAT 10	tsu;sto 160	🗖 tLOW 160	
tHD;STA 160	thd;dat 5	500 tBUF	thigh 60	
				1
tsu;sta sr the	STA ^t HD;DAT	tSU;DAT tSU;	STO P S	
Pre-Trigger	Data match with P1 Address	Pass Count Type	Pass Count 0 OK Cance	۲. ۲

About each:



Red 1: tSU;STA: The setup time of Re-Start, also the time when the clock (SCL) is from high to low.

Blue 2: tHD;STA: The hold time of Re-Start, also the time when the clock (SCL) is

from high to low.

Blue 3: tSU;DAT: The setup time of Data, also the time when the clock (SCL) is

from rising to falling.

Red 4: tHD;DAT: The hold time of Data, also the time when the clock (SCL) is from falling to rising.

Red 5: tSU; STO: The setup time of Stop, also the time when the clock (SCL) is from high to low.



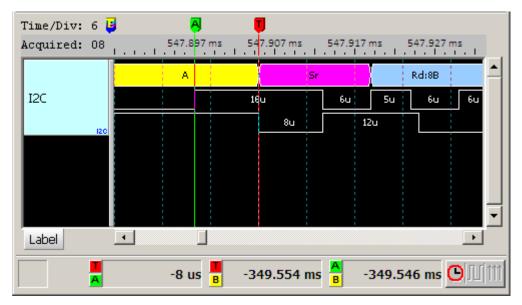
Blue 6: tBUF: Bus Free Time, that is between Start and Stop.

Red 7: tLOW: The time the clock (SCL) is low.

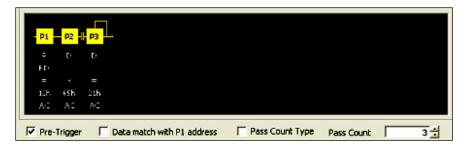
Blue 8: tHIGH: The time the clock (SCL) is high.

The following figure is an example to trigger the setup time (8005ns) of Re-Start (tSU;

STA), where the time between cursor T and cursor A is 8us (8000ns < 8005ns).



Pass Count: Pass Count will pass N times that triggers occurred in the non-sequential trigger condition. In the following example, the trigger will pass three triggers in P3 (non-sequential trigger condition) and trigger at the fourth time.



Pass Count Type: If Pass Count Type is checked, then the loop will start run from

the first trigger condition (P1).



P1 - P2 1 P3			
A D D RD			
= ; = Ch 68h 21h			
54 54 54			
Pre-Trigger 🔲 Data match with P1 address	Pass Count Type	Pass Count	3 👙

Data match with P1 address: P1 must be set as address and followed by data; this

function is only available in Match Sequentially. And the first level (P1) parameter

must be set the address (not data), the function will be open.

For more information of I^2C trigger, please refer to I^2C Application Note.

		and a second					405.04	4 ms	463.92				
		Addr:45		< I	01		A	<mark>sr</mark>	Addr:45		A 04	A 4D	
12C	o sa.	חמתחח	₅	40		1111	35u					[] ∏ ∏ ∏ ₃₃◡ ∏ ∏ ∏ [T
								יייי היור					H
120		35u	23u	12	9u		42u		35u	23u	42u 52u	35u 33u 24u	
									1				
.abel	Channel 💶												۲
CH-00 C		()											
CH-00 CH-01 C		2C(I2C)		-									
				D1	D2	D3	D4	D5	D6	D7	ASCII	Information	
ample	Status	Addr	DO	UT DI	DZ	100				D7	ASCII	Informacion	
-	Status Start	Addr Wr 45	4D	03	10	00	28			57	M(Información	
57550							28					Información	
.57550 .63551	Start	Wr 45	4D				28 09				M (Información	
.57550 .63551 .63857	Start Start	Wr 45 Wr 45	4D 01	03	10	00					M(
57550 63551 63857 69762	Start Start Repeat Start	Wr 45 Wr 45 Rd 45	4D 01 04	03 4D	10	00 4E	09				M(.M.N.		
57550 63551 63857 69762 75708	Start Start Repeat Start Start	Wr 45 Wr 45 Rd 45 Wr 45	4D 01 04 4D	03 4D	10	00 4E	09				M(.M.N. Ms		
57550 63551 63857 69762 75708 76018	Start Start Repeat Start Start Start Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45	4D 01 04 4D 01	03 4D 03	10 10 10	00 4E 00	<mark>09</mark> 73				M(.M.N. Ms		
57550 63551 63857 69762 75708 76018 82008	Start Start Repeat Start Start Start Repeat Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Rd 45	4D 01 04 4D 01 01 04	03 4D 03 4D	10 10 10 10	00 4E 00 4E	09 73 0A				M(.M.N. Ms .M.N.		
57550 63551 63857 69762 75708 76018 82008 88028	Start Start Repeat Start Start Repeat Start Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Rd 45 Wr 45	4D 01 04 4D 01 01 04 4D	03 4D 03 4D	10 10 10 10	00 4E 00 4E	09 73 0A				M(
157550 163551 163857 169762 175708 176018 182008 188028 188028 1880337	Start Start Repeat Start Start Repeat Start Start Start Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Wr 45	4D 01 04 4D 01 01 04 4D 01 04 01	03 4D 03 4D 03 03	10 10 10 10 10	00 4E 00 4E 00	09 73 0A 42				M(
157550 163551 163857 169762 175708 176018 182008 188028 188028 188028 188337 194304	Start Start Start Start Start Repeat Start Start Start Repeat Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Rd 45 Wr 45 Wd 45	4D 01 04 4D 01 04 4D 04 4D 01 01 01 04	03 4D 03 4D 03 4D 03 4D	10 10 10 10 10 10	00 4E 00 4E 00 4E	09 73 0A 42 0B				M(
157550 163551 169762 175708 176018 182008 188028 188337 194304 500190	Start Start Start Start Start Repeat Start Start Start Repeat Start Start Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Rd 45 Wr 45	4D 01 04 4D 01 01 04 4D 01 04 4D 01 04 4D	03 4D 03 4D 03 4D 03 4D	10 10 10 10 10 10	00 4E 00 4E 00 4E	09 73 0A 42 0B				M (.M.N. Ms .M.N. MB .M.N. M.N.		
Sample 157550 163551 169762 175708 175708 188028 188028 188337 194304 500190 500562 500562 5005481	Start Start Start Start Start Repeat Start Start Repeat Start Start Start Start Start Start	Wr 45 Wr 45 Rd 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Rd 45 Wr 45 Wr 45	4D 01 04 4D 01 01 04 4D 01 01 04 4D 01 04 01 01 01 01 01	4D 03 4D 03 4D 03 4D 03	10 10 10 10 10 10 10	4E 00 4E 00 4E 00	09 73 0A 42 0B 0F				M (
157550 163551 163857 169762 175708 182008 188028 188028 188028 188028 18837 194304 194304 1900562	Start Start Repeat Start Start Repeat Start Start Repeat Start Start Start Start Start Start Start	Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45	4D 01 04 4D 01 01 04 4D 01 04 4D 01 01 01 01 01	4D 03 4D 03 4D 03 4D 03 4D	10 10 10 10 10 10 10 10	4E 00 4E 00 4E 00 4E 00	09 73 0A 42 0B 0F				M(
157550 163551 163857 169762 175708 175708 182008 188028 188028 188337 194304 100190 100562 106481	Start Start Start Start Start Start Start Start Start Start Start Start Start Start Start Start Start Start Start	Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45 Wr 45	4D 01 04 4D 01 04 4D 01 04 4D 01 04 4D 01 04 4D 01 04 4D	4D 03 4D 03 4D 03 4D 03 4D	10 10 10 10 10 10 10 10	4E 00 4E 00 4E 00 4E 00	09 73 0A 42 0B 0F				M(

Result



I²S Trigger

Mode	Min. S/R	Max, S/R	Available ch.	Min. Mem.	Max. Mem.
🗐 400M	400MHz	400MHz	18	256	4M
+ 🧰 200M	1Hz	200MHz	Adjustable	256	Adjustable
🛨 🧰 UART Trigger	Baud Rate x 16	Baud Rate x 16	Adjustable	256	Adjustable
🛨 🧰 CAN Trigger	Data Rate × 10	Data Rate x 10	Adjustable	256	Adjustable
🛨 🧰 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
🖃 💼 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
—🗐 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
— Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
–≝ I2S Trigger-36	1Hz	200MHz	Adjustable	256	2M
-E I2S Trigger-18	1Hz	200MHz	Adjustable	256	4M
-E I2S Trigger-12	1Hz	200MHz	Adjustable	256	6M
–≝ I25 Trigger-9	1Hz	200MHz	Adjustable	256	8M
-🗐 I2S Trigger-6	1Hz	200MHz	Adjustable	256	12M
🖃 I2S Trigger-4	1Hz	200MHz	Adjustable	256	18M
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M

The settings dialog box below.

Trigger Setting

Select I²S Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button () on Toolbar (or Device menu) to show the I²S Trigger Settings dialog box below.

I2S Trigger Settings				x
Channel SCK 0	WS 1	SC	2	
Data Bits 8	▼ Bits F	-ull Scale Voltage	2000 mV	1
Method Data M	atch		•	
Channel 📀 Bo	oth O	Left 🤇) Right	
Pattern Unit 💿 Va		Voltage () dB	
Pattern A	00h	Pattern B	00h	
• = • • !=	0 < 0 >	🔿 In Range	C Out Range	
Duration(# of fram	ies) 1			
Timing Violation				1
Default Settings	🖲 Master	C Slave C	Custom	
SCK Period Min.	360 ns	SCK Period Max.	440 ns	
SCK High Duty Min.	160 ns	SCK Low Duty M	in, 160 ns	
Setup Time	0 ns	Hold Time	100 ns	
Pre-Trigger	· Pa	ass Count:	0 +	
	Load	Save	K Cancel	



Channel: There are three channels: Serial clock (SCK), word select (WS) and serial data (SDA).

Data Bits: 1-32 bits, normally it is 8, 12, 16, 24 or 32.

Channel: Both, Left or Right.

Pattern Unit: Value, Voltage or dB as the trigger codition. If it is Value, only

hexadecimal (xxxh) or decimal numbers are allowed.

Trigger method: = (is equal), !=(isn't equal), < (less than), >(more than), In Range

(between Pattern A and B), or Out Range (out of Pattern A and B)

Duration (# of frames): Continuous frames and trigger when the condition is matched.

Method:

Data Match: Trigger when the conditions matched.

Rising Edged: Trigger when it is a rising edge between two patterns.

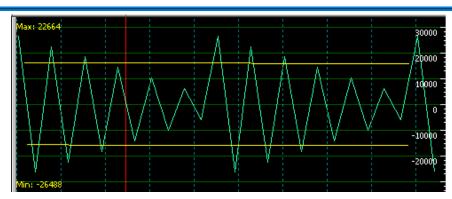
Falling Edged: Trigger when it is a falling edge between two patterns.

Glitch: Trigger when there is a glitch.



Mute: When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of -P < X < +P.





Clip: When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of $-P < X \cup +P > X$.

Timing Violation: There are two default (Master or Slave) and one custom types of timing violation triggers as below.

Master: select the default Master values as the trigger condition.

Slave: select the default Slave values as the trigger condition.

Custom: set trigger parameters manaully.

SCK Period Min.: Trigger when the value is less than the minimum SCK period.

SCK Period Max.: Trigger when the value is more than the maximum SCK period.

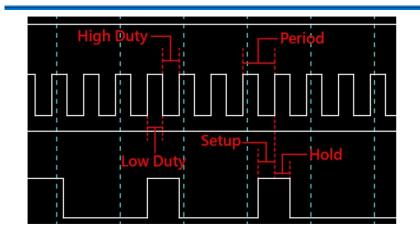
SCK High Duty Min.: Trigger when the value is less than the minimum SCK High Duty.

SCK Low Duty Min.: Trigger when the value is less than the minimum SCK Low Duty.

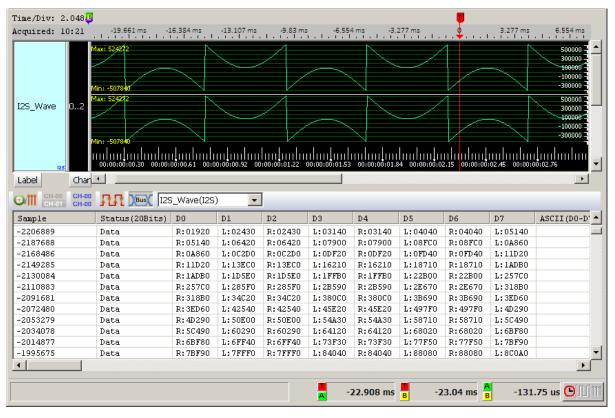
Setup Time: Trigger when the value is less than the Setup time.

Hold Time: Trigger when the value is less than the Hold time.





Result





Time/Div: 16 us 📮					Ţ				
Acquired: 10:21	-102.4 us	-76.8 us	-51.2 us	-25.6 us		25.6 us	51.2 us	76.8 us	102.4 us
	L:B2D40	R:B2D40	L:B67E0	R:B67E0	L:BA1B0	R:BA1B0	L:BDA90	R:BDA90	L:C1270
0 SCH I2S_Data									
1 WS	24u	24u	24u	24u	24u	24.01u	24u	24u	24u
2 SD	80 100		90	90	.	J)		
Label Char	•								
CH-00 CH-00 CH-00 CH-00									
Sample	I25_Data								-
25253	R:CB3B0								
27653	L:CE720								
30053	R:CE720								
32453	L:D1960								
34854	R:D1960								
37254	L:D4A40								
39654	R:D4A40								
42054	L:D79E0								
44454	R:D79E0								
46854	L:DA810								
49255	R:DA810								
51655	L:DD4D0								
					_				
					A -22.9	908 ms 📕	-23.04 n	ns <mark>A</mark> -1	.31.75 us 🕒 🔟 🗎



SPI Trigger

The settings dialog box below.

If need higher Sample rate for SPI, choose SPI-800M which is 800MHz Sample

Rate with 9 channels. In SPI-800M, you can only use the default parameter settings.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
+ 🧰 UART Trigger	Baud Rate × 16	Baud Rate × 16	Adjustable	256	Adjustable
+ 🧰 CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
+ 🧰 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
+ 🧰 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
– 🔄 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
— 🗐 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
—🗒 Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
—🗐 SPI Trigger-36	1Hz	200MHz	Adjustable	256	2M
—🗐 SPI Trigger-18	1Hz	200MHz	Adjustable	256	4M
-🗐 SPI Trigger-12	1Hz	200MHz	Adjustable	256	6M
🖃 SPI Trigger-9	1Hz	200MHz	Adjustable	256	8M
- E SPI Trigger-6	1Hz	200MHz	Adjustable	256	12M
🗐 SPI Trigger-4	1Hz	200MHz	Adjustable	256	18M
+ 🥅 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable

Trigger Setting

Select SPI Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button (.) on Toolbar (or Device menu) to show the SPI Trigger Settings dialog box below.

SPI Trigger Settings	×
Channel Chip Select CS 0 SCK 1 SDA 2 C Rising Edge C Falling Edge	Trigger Value IF After C5 OR IF After C5
Word Size Setup Word Size 8 MSB C LSB Pre-Trigger Pass Count 0	OR IF Then After C5 After C5 OR IF Then After C5 After C5
Check Load Save	OK Cancel



Channel: Select three channels for Chip Select (CH 0), serial clock (CH 1), and serial data (CH 2).

Chip Select: Select Active Low or Active High to enable Chip Select.

Clock Latch Data: Select Rising Edge or Falling Edge to latch data.

Word Size Setup: Select the number of data bits (4~24).

MSB/LSB: Select MSB first (MSB \rightarrow LSB) or LSB first (LSB \rightarrow MSB) to transmit the data.

Trigger Value: The SPI Trigger has four IF/Then triggers, but ONLY one will trigger when its condition is met first. The condition can be in characters, a string, decimal numbers or hexadecimal codes with no more than 16 characters and: Characters and the string MUST be within single or double quotation marks, e.g. 'A' or "Acute"; A string can be entered with characters, a string and hexadecimal code with a blank space between each two different inputs, 'A'_"cute" or 'A'_63h_'u'_'t'_65h e.g.

Pass Count: Pass Count will pass N times that triggers occurred. If the Pass Count is 5 as the dialog box below, all triggers in all IF/Then conditions are counted and the instrument will trigger at the 6th trigger.

SPI Trigger Settings	<u>×</u>
Channel Chip Select Chip Select Chip Select Chip Select Chip Select Chip Select Chip Select S	Trigger Value
SCK 1 SDA 2 Clock Latch Data © Rising Edge © Falling Edge	Image: Construction Image: Construction Image: Construction Image: Construction Image: Construction Image: Construction
Word Size Setup Word Size 8 C LSB	OR IF F Then After CS OR IF OR IF Then Then Then Then
Pre-Trigger Pass Count 5	After CS
C5 L SCK SDA DDH C5 L SCKSck SDA SDA	
Check Load Save	OK Cancel



Check Trigger: Check the validity of trigger conditions.

Result

Time/Div: 250 📮											
Acquired: 08:0	2.557 ms 2.557 r	ms I.I.	2.558 n	ms I.I	2.558	ms I	2.559	ms 	2.559 r	ms 2.559 ms 2.56	ms - I - I - I - I - J
SPI 1 CS) 00		00 00000000000000000000000000000000000		00 0 			dle 00 00 -
U 5DI —	150n	_				.9284				152	
2 SDO	172.5n							2.47u			
											-
Label Channel											•
CH-00 CH-00 CH-00 CH-00 CH-00	SPI(SPI)		-]							
Timestamp	Status(8 bits data)	DO	Dl	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Informati 🔺
2.5566025 ms	Unknown										
2.5567225 ms	Idle	0.0		DO	6.0	0.0	0.0			0	Duration:
2.5569075 ms 2.5582925 ms	Data Data	0B 00	00	B0 00	67 00	00	00	00	00	°g	
2.5596825 ms	Unknown	00	00	00	00	00	00	00	00		
2.5598 ms	Idle										Duration:
2.559985 ms	Data	OB	00	BO	74	00	00	00	00	°t	
2.561375 ms	Data	00	00	00	00	00	00	00	00		
2.5627625 ms	Data	00	00	00	00	00	00	00	00		
2.5641525 ms	Data	00	00	00	00	00	00				
2.5651925 ms	Unknown										
2.5653125 ms	Idle										Duration: 🖵
·											
						A	63	31 002	B	1855771 <mark>A</mark> 24	86773 🕒 🛙 🎁



SVID Trigger (Upon Request)

1ode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.
+ 🦲 CAN Trigger	Data Rate x 10	Data Rate x 10	Adjustable	256	Adjustable
+ 🧰 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable
+ 🧰 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable
🗐 SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M
+ 🧰 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable
- 💼 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable
–≝ Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto
—🗐 Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
–) SVID Trigger-36	1Hz	200MHz	Adjustable	256	2M
-) SVID Trigger-18	1Hz	200MHz	Adjustable	256	2M
-) SVID Trigger-12	1Hz	200MHz	Adjustable	256	2M
-) SVID Trigger-9	1Hz	200MHz	Adjustable	256	2M
-) SVID Trigger-6	1Hz	200MHz	Adjustable	256	2M
SVID Trigger-4	1Hz	200MHz	Adjustable	256	2M

The settings dialog box below.

If you have any issues with SVID protocol features, please contact your Intel

Field Representative.

Trigger Settings

Select SVID Trigger-36 where "-36" means 36 channels and click OK. Then click the

Trigger Settings button **U** on Toolbar (or Device menu) to show the SVID Trigger

Settings dialog box below.

SVID Trigger	Settings					×
Channel: SCLK 🚺	SDATA 1	ALERT 2	Trigge	er Method: Start		•
Address	Command	Master Payload	When Alert	АСК	Slave Payload	Trigger
P1 XXh Don't care 💌	XXh Don't care	▼ XXh	X Don't care 💌	X Don't care 🖉 💌	XXh	Then Trigger 🛛 🔻
P2 XXh Don't care	📃 😑 🕅 XXh Don't care	▼ XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger 📃 💌
P3 XXh Don't care 💌	XXh Don't care	▼ XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger 📃 💌
P4 XXh Don't care	📃 📃 XXh Don't care	▼ XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger 🗾 💌
✓ Pre-Trigger Pas	s Count 🛛 🔿 🗮		Load Sav	e Clear All		OK Cancel

Channel: Set the 2 channels (SCLK and SDATA) to form the trigger signal, ALERT



is option.

Trigger Mode:

Start: Trigger when the SVID packet is valid.

Frame Data: Trigger according to the frame data.

Parity Error: Trigger when the parity error happens.

Frame Data Settings:

svi	D Trigger S	ettings							×
Cha	nnel: SCLK 0	SDATA 1		ALERT 2	Trigge	r Method: Frame	Data		
	Address	Command		Master Payload	When Alert	ACK	Slave Payload	Trigger	
P1	XXh Don't care 💌	= XXh Don't care	-	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger	•
P2	XXh Don't care 💌	= XXh Don't care	7	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger	-
PЗ	XXh Don't care 💌	= XXh Don't care	-	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger	~
P4	XXh Don't care 💌	= XXh Don't care	-	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger	~
	Pre-Trigger Pass C	iount 0 🛋			Load Save	e Clear All		OK Canc	el

You can set 4 (most) frame data packets as trigger conditions. Each column in those frame data can be set as any value or Don't care (xxh) and set trigger condition equal to the command or not.

The Payload column is 1 byte only, can be character (like 'A'), decimal number (like

65) or hexa-decimal number (like 41h), but any input value over 1 byte will be

filtered.

The ALTER channel can be '0', '1' or don't care.

Trigger column includes:

Then Trigger: If conditions matched, trigger right away.

Then If: If conditions matched, wait for the next matched frame data.

Next: If conditions matched, wait for any next frame data.

Pass Count: The Pass Count function in the SVID Trigger is very unique. If you set the frame data conditions like P1 and P2 in the SVID Trigger Settings table below, the



pass count will only count 1 time when both P1 and P2 are matched. It will trigger

after 2 matches (P1 and P2).

SVI	D Trigger S	ettin	igs						×
Cha	nnel: SCLK 0		SDATA 1		ALERT 2	Trigge	r Method: Frame	Data	•
	Address	Co	ommand		Master Payload	When Alert	ACK	Slave Payload	Trigger
P1	XXh Don't care 💌	X	Xh Don't care	•	XXh	X Don't care 💌	X Don't care 💌	XXh	Next
P2	XXh Don't care 💌	×	Xh Don't care	•	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger 🗨
P3	XXh Don't care 💌	X	Xh Don't care	-	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger 🗾 👻
P4	XXh Don't care 💌	= X	Xh Don't care	-	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger 🗾 💌
	Pre-Trigger Pass C	iount	0 🗄			Load Sav	e Clear All		OK Cancel

If you set the frame data conditions like P1, P2 and P3 in the SVID Trigger Settings

table below, the pass count will only count 1 time when both P1 and P2 are matched

first and then P3 is matched. It will trigger after 2 matches (P3).

SVI	D Trigger S	ettings							×
Char	nnel: SCLK 0	SDATA 1		ALERT 2	Trigge	er Method: Frame	Data	¥	
	Address	Command		Master Payload	When Alert	ACK	Slave Payload	Trigger	
P1	XXh Don't care 💌	= XXh Don't care	•	XXh	X Don't care 💌	X Don't care 💌	XXh	Next	•
P2	XXh Don't care 💌	= XXh Don't care	•	XXh	X Don't care 💌	X Don't care 💌	XXh	Then If	-
P3	XXh Don't care 💌	= XXh Don't care	•	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger	•
P4	XXh Don't care 💌	= XXh Don't care	-	XXh	X Don't care 💌	X Don't care 💌	XXh	Then Trigger	~
▼ F	Pre-Trigger Pass C	iount 0 🕄			Load Sav	e Clear All		OK Ca	ncel



Result

	Idle Start	Addr:0 Cmd:GetR	<mark>eg(7)</mark> MA.PL:SR-slow(25) P:0 Er	nd Turn	SL.PL:02 P:1	Idle	
0 SCIk SVID		ΛΛΛΛΛΛΛ				340n	İ
1 SData	40n 40n	280n 120)n 80n #0n 80n #0n#0n#0n 80n	170n 280n	#0n/#0n		
2 Alert svid							
							•
Label Channel			* * * *			•	
Label Channel 3/111 CH-00 CH-00 CH-01 CH-00	-	SVID(SVID)	•				
	-	SVID(SVID) Command (h)	VA. Payload(h)	SL. Payload	l(h) Ack	• Error	
→ CH-00 CH-00 CH-01 CH-00				SL. Payload	l(h) Ack ACK(2)		
CH-00 CH-00 CH-01 CH-00 Fimestamp 0.06069 ms	Addr (h)	Command(h)	MA. Payload(h)	SL. Payload			
CH-00 CH-00 CH-01 CH-00 Fimestamp 0.06069 ms 0.06305 ms	Addr (h)	Command(h) SetRegDAT(6)	MA. Payload(h) 1.250V (C9)	SL. Payload	ACK(2)		
CH-00 CH-00 CH-01 CH-00 Fimestamp 0.06069 ms 0.06305 ms 0.06538 ms	Addr (h) 0 1	Command(h) SetRegDAT(6) SetRegADR(5)	MA. Payload(h) 1.250V (C9) Vout max(30)	SL. Payload	ACK(2) NAK(1)		
CH-00 CH-00 CH-01 CH-00 CH-01 CH-00	Addr (h) 0 1 1	Command(h) SetRegDAT(6) SetRegADR(5) SetRegDAT(6)	MA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9)		ACK(2) NAK(1) ACK(2)		
0/111 CH-00 CH-00 CH-01 CH-00 Fimestamp	Addr (h) 0 1 1 0	Command(h) SetRegDAT(6) SetRegADR(5) SetRegDAT(6) GetReg(7)	MA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9) SR-fast(24)	0A	ACK(2) NAK(1) ACK(2) ACK(2)		
CH-00 CH-00	Addr(h) 0 1 1 0 0	Command(h) SetRegDAT(6) SetRegADR(5) SetRegDAT(6) GetReg(7) GetReg(7)	MA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9) SR-fast(24) SR-slow(25)	0A	ACK(2) NAK(1) ACK(2) ACK(2) ACK(2)		
CH-00 CH-00	Addr (h) 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Command(h) SetRegDAT(6) SetRegDAT(5) SetRegDAT(6) GetReg(7) GetReg(7) GetReg(7)	MA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9) SR-fast(24) SR-fast(24) SR-slow(25) DC_LL(23) DC_LL(23)	0A	ACK(2) NAK(1) ACK(2) ACK(2) ACK(2) Rejet(3)		
CH-00 CH-00	Addr (h) 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Command(h) SetRegDAT(6) SetRegDAT(5) SetRegDAT(6) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7)	MA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9) SR-fast(24) SR-slow(25) DC_LL(23) DC_LL(23)	0A	ACK(2) NAK(1) ACK(2) ACK(2) ACK(2) Rejet(3) Rejet(3)		
CH-00 CH-00 CH-00 CH-01 CH-00 Ch-01 CH-00 Cimestamp 1.06069 ms 1.06059 ms 1.060538 ms 1.07253 ms 1.07253 ms 1.07263 ms 1.086472 ms 1.09868 ms 1.09689 ms	Addr (h) 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Command(h) SetRegDAT(6) SetRegADR(5) SetRegDAT(6) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7)	MA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9) SR-fast(24) SR-slow(25) DC_LL(23) DC_LL(23) DC_LL(23) DC_LL(23) DC_LL(23)	0A	ACK(2) NAK(1) ACK(2) ACK(2) ACK(2) Rejet(3) Rejet(3) Rejet(3)		
CH-00 CH-00 CH-00 CH-01 CH-00 Ch-01 CH-00 Ch-00 Ch-00 Ch-00 Ch-00 CH-00	Addr (h) 0 1 1 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 0	Command(h) SetRegDAT(6) SetRegDAT(5) SetRegDAT(6) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7) GetReg(7)	NA. Payload(h) 1.250V (C9) Vout max(30) 1.250V (C9) SR-fast(24) SR-slow(25) DC_LL(23) DC_LL(23) DC_LL(23) DC_LL(23)	0A	ACK(2) NAK(1) ACK(2) ACK(2) ACK(2) Rejet(3) Rejet(3) Rejet(3) Rejet(3)		



UART Trigger

The settings dialog box below.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max
🖺 800M	800MHz	800MHz	9	256	8M
🗐 400M	400MHz	400MHz	18	256	4M
+ 🧰 200M	1Hz	200MHz	Adjustable	256	Adju
- 🔄 UART Trigger	1Hz	200MHz	Adjustable	256	Adju
—🗐 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auti
— Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Aut
—🔳 UART Trigger-36	1Hz	200MHz	Adjustable	256	2M
────────────────────────────────────	1Hz	200MHz	Adjustable	256	4M -
────────────────────────────────────	1Hz	200MHz	Adjustable	256	6M
───── UART Trigger-9	1Hz	200MHz	Adjustable	256	8M
───── UART Trigger-6	1Hz	200MHz	Adjustable	256	12M
───── UART Trigger-4	1Hz	200MHz	Adjustable	256	18M
────────────────────────────────────	1Hz	200MHz	Adjustable	256	36M
□ UART Trigger-1	1Hz	200MHz	Adjustable	256	72M
🛨 🧰 CAN Trigger	1Hz	200MHz	Adjustable	256	Adju

Trigger Settings

Select UART Trigger-36 where "-36" means 36 channels and click OK. Then click the Trigger Settings button () on Toolbar (or Device menu) to show the UART Trigger Settings dialog box below.

UART Trigger Settings						
Trigger Channel: 🚺 💌 Baud Rate: 9600 💌 Data Bits: 8 💌	Polarity Idle High Start D0D7 Parity Stop Bit Idle Low					
Parity: NONE Stop Bits: 1 IF	Stop Bit D0D7 Parity Stop Bit D0D7 Parity Stop					
	Then Then Then					
	Then					
Check Load Save	Pass Count 0 *					



Trigger Channel: Only one channel can be selected. **Baud Rate:** The range is 110 ~ 2M bits per second (bps). Data Bits: 5, 6, 7, or 8.

Parity: EVEN, ODD, or NONE.

Stop Bits: 1 or 2.

Trigger Type: Falling Edge or Rising Edge.

IF/Then trigger: The UART Trigger has four IF/Then triggers, but ONLY one will trigger when its condition is met first. The condition can be in characters, a string, decimal numbers or hexadecimal codes with no more than 16 characters and: Characters and the string MUST be within single or double quotation marks, e.g. 'A' or "Acute"; A string can be entered with characters, a string and hexadecimal code with a blank space between each two different inputs, 'A'_"cute" or

'A'_63h_'u'_'t'_65h e.g.

Check Trigger Settings: Check the validity of trigger conditions.

Time/Div:	1.024 m	9																	
acquired:	15:07:5	1	. I . I	0.773 \$. I . I	00.774 S		00.776 S	3(00.778 S	. I . I	00.779 S	. I . I	0.781 S	. I . I	0.783 \$. I . I	00.784 S	
CH-00 VART(RS232	0 UART		Idle	55		33	01	00	02		17	01	02	J.	:		Break	X	
Label	Channe																	•	1
Э/ 111 сна Сна	00 CH-00 01 CH-00	J.J.	Bus	(Сн	DO(UAF	RT(RS23	32)) 💽	•											
Time	State	DO	Dl	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15		
300.7		55	33	01	00	02	17	01	02	10								Ū3	
300.7		55	33	01	00	02	17	01	02	10								U3	
800.7		55	33	01	00	02	17	01	02	10								U3	
800.8		55	33	01	00	02	17	01	02	10								U3	
300.8		55	33	01	00	02	17	01	02	10								U3	
800.8		55	33	01	00	02	17	01	02	10								U3	
300.8		55	33	01	00	02	17	01	02	10								U3	
800.8		55	33	01	00	02	17	01	02	10								U3	
800.8		55	33	01	00	02	17	01	02	10								U3	
00.8		55	33	01	00	02	17	01	02	10								U3	
300.8		55	33	01	00	02	17	01	02	10								U3	
300.9		55	33	01	00	02	17	01	02	10								U3	
800.9		55	33	01	00	02	17	01	02	10								U3	
300.9		55	33	01	00	02	17	01	02	10								U3	
300.9		55	33	01	00	02	17	01	02	10								U3	
300.9		55	33	01	00	02	17	01	02	10								U3	
300.9		55	33	01	00	02	17	01	02	10								U3	
300.9		55	33	01	00	02	17	01	02	10								U3	
•																			ьí
																		<u> </u>	-



Clause Trigger

LPC Trigger 🗐 ng	2	3 4 💌
Channel LFRAME# CH 0 LCLK CH 1 LAD[0] CH 2	$ \begin{array}{c} Run & \longrightarrow True \\ & State 1 & \longrightarrow False \\ & & Ti T2 \\ & State 2 & \longrightarrow Trigger \\ \end{array} $	State 1 Logic Condition © OR © AND Event 1 × Event 2 × + OR AND Timer 1 Cycle Type Memory Read Clk # If the condition is true, then
LAD[1] CH 3 LAD[2] CH 4 LAD[3] CH 5 LAD[3] CH 5		START 1 0000b Reset Counter 1 CT/DIR 1 010Xb Reset Counter 2 ADDR 8 7654XXXXh Image: Start Timer 1 from reset Image: Start Timer 2 from reset Image: Start Timer 2 from reset Image: Start Timer 2 from reset
Clock Edge Rising Edge	→ ▼ Trigger ×	TAR 2 Xxh SYNC 1 Xh DATA 2 ABh Xxh
Start Error CT/DIR Error (Bus Master) Channel Error (DMA)	+ State x 4 + Counter x 2	Data Offset
Size Error MSize Error Sync Error	Timer 1 Timer 2	
Undo Redo	Pre-Trigger Pass Count	重設 確定 取消

The Clause trigger settings dialog box is as below.

1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.

2. Flow chart

$ \begin{array}{c} Run \\ \hline \\ State 1 \\ \hline \\ \\ \hline \\ State 2 \\ \hline \\ \\ \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	$ \begin{array}{c} \text{Run} & \longrightarrow & \text{True} \\ \text{State 1} & \longrightarrow & \text{False} \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & & & & & & \\ & &$	Run State 1 State 1 State 2 State 2 State 2 Trigger Trigger Trigger
State 1 next State 2	State 1 then State 2	State 1 next State 2 then State 3 next State 4



$ \begin{array}{c} & \underset{\text{State 1}}{\overset{\text{WI}}{\longrightarrow}} & \underset{\text{False}}{\overset{\text{Trigger}}{\longrightarrow}} \\ & \underset{\text{T1}}{\overset{\text{State 2}}{\longrightarrow}} \\ & & \underset{\text{T1}}{\overset{\text{WI}}{\longrightarrow}} \\ & & \underset{\text{Trigger}}{\overset{\text{WI}}{\longrightarrow}} \\ \end{array} $	$ \begin{array}{c} \text{Run} & \longrightarrow & \text{True} \\ \text{State 1} & \longrightarrow & \text{False} \\ \text{State 2} & \longrightarrow & \text{Trigger} \\ \hline 1 & & & & \\ \end{array} $
State 1 (Active T1)	State 1 (Active T1)
next State 2 (Time >= T1)	next State 2 (Time < T1)

A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:

Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.

Double click any state, the state will branch to itself if it is false.

Click the state button and trigger button (**Trigger**): triggere when the state

conditions is satisfied.

Delete any state by clicking the cross sign on the state.

Clear the links to the trigger button by clicking on the trigger button (♥ Trigger))

Click + State x 4 and + Counter x 2 to add a new state.

Timer 1 : The timer ranges from 5 ns to 8 days.



3. State settings

,	Cycle Type Memory Read						
START	1	0000b					
CT/DIR	1	010Xb					
ADDR =	8	7654XXXXh					
TAR	2	XXh					
SYNC	1	Xh					
DATA	2	ABh XXh XXh XXh					
		4					

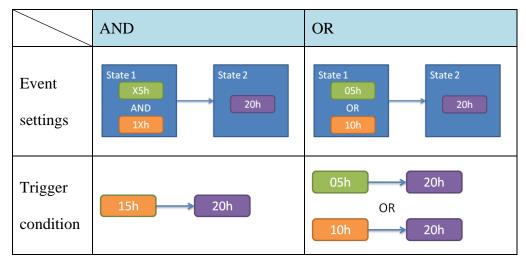
The trigger conditions of the state:

- 1. The current state index
- 2. Logic condition between every event in the state.
- 3. Switch between the tab windows to edit the trigger events . Click |+ OR | /

+AND to add new events (up to 8 events).

4. The bus trigger settings.

The relations between events and the trigger condition:





4. Timer and Counter settings

Press Advanced Setting >> button t	o edit the timer/counter reset settings of the state.
Timer Condition ▼ AND Timer 1 ▼ 5.000 ns ▼ AND Timer 2 >= ▼ 5.000 ns	
If the condition is true, then Reset Counter 1 Reset Counter 2	
Start Timer 1 from reset Start Timer 2 from reset	

The following table describes the state button icons:

	State 1	State 1	State 1	State 1 T1 T2 T1 T2 C1 C2 T1 T2
		State 1	State 1	State 1
Conditions	State 1	And	And	And
			timer < T1	T2 < timer <t1< td=""></t1<>
satisfied	Stort T1	V	Start T2	Start T1 and T2
condition	Start T1	X	Reset C2	Reset C1 and C2



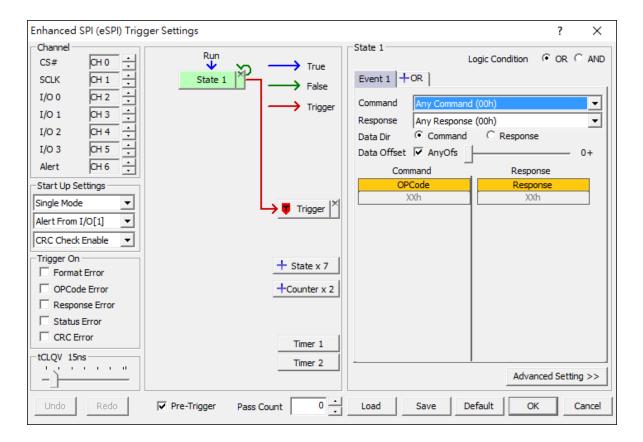
eSPI Trigger

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.	^
+ 🧰 200M	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 CAN Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🖃 🔄 eSPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
— Transitional Storage(400M)-16	400MHz	400MHz	Fixed	Auto	Auto	
eSPI Trigger (400M)-18	400MHz	400MHz	18	256	4M	
─	200MHz	200MHz	Fixed	Auto	Auto	
— Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto	
–≡ eSPI Trigger-36	1Hz	200MHz	Adjustable	256	2M	
–≝ eSPI Trigger-18	1Hz	200MHz	Adjustable	256	4M	
–≝ eSPI Trigger-12	1Hz	200MHz	Adjustable	256	6M	
- 🕮 eSPI Trigger -9	1Hz	200MHz	Adjustable	256	8M	
eSPI Trigger-6	1Hz	200MHz	Adjustable	256	12M	
+ 🧰 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🛨 🧰 LIN Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	~

Select eSPI Trigger in Hardware Settings.

Trigger Settings

Select "eSPI" in Trigger Settings.





Channel: Please refer to the Bus Decode of eSPI.

Start Up Settings: There are three modes including single, dual and quad mode. Set the current mode to be any of them and the setting would be automatically switched by monitoring the bus in hardware. Then choose the Alert signal and the CRC Check. Trigger On: Select any error of format, OP Code, Response, Status and CRC to trigger.

tCLQV: The delay time of I/O and Clock in Response. The incorrect setting may cause that Response cannot be triggered.

Trigger State Settings:

State 1	L	ogic Condition 💿 OR 🔿 AND					
Event 1 +	OR						
Command GET_CONFIGURATION (21h)							
Response	ACCEPT (x4 Da	ata) (08h) 🔹 💌					
Data Dir	C Command	Response					
Data Offset	AnyOfs	0+					
Com	mand .	Response					
Ade	dress	Data (D0+)					
)	0Xh	[]					
Ade	dress	Data (D1+)					
)	(Xh	11h					
C	RC	Data (D2+)					
)	0Xh	XXh					
		Status (D4+)					
		XXh					
		Status					
		XXh					
		Status					
		XXh					
		Advanced Setting >>					

eSPI Trigger offers many kinds of Command and Response. You may set "Any Command" to capture the signal, and choose the proper setting of trigger by the decode of eSPI.



Timestamp	OpCode/Response	СусТуре	Tag	LEN	Address	DO	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
-0.00000245 S	GET CONFIGURATION (21)				0010											58	
0.0000086 5	ACCEPT (08)					13	11	00	00						030F	95	
0.000003 5	SET_CONFIGURATION(22)				0010	01	11	00	00							F5	
0.000005935 S	ACCEPT (08)														030F	9B	
0.000008455 S	GET_STATUS(25)															FB	
0.000009365 S	ACCEPT (08)														030F	9B	
0.001601195 S	GET_CONFIGURATION(21)				0010											58	
0.001602795 S	ACCEPT (08)					13	11	00	00						030F	95	
0.001606635 S	SET_CONFIGURATION(22)				0010	01	11	00	00							F5	
0.001609575 S	ACCEPT (08)														030F	9B	

eSPI decode result

Data Dir: Trigger the data in the Command or Response.

Data Offset: Trigger the data from start of data frame without any offset. For example, setting D0 13h will check the first byte of data frame. With any offset, the siganl would be triggered by the byte pattern. For instance, setting D0+ XXh D1+ 11h, and the byte pattern of XXh and 11h will be triggered regardless of the position of the data.



LIN Trigger

Select LIN Trigger Settings.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max
+ 🦲 LPC Trigger	1Hz	200MHz	Adjustable	256	Adji
🛨 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adju
+ 🧰 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adju
+ 🧰 SMBus/PMBus Trigger	1Hz	200MHz	Adjustable	256	Adju
🛨 🧰 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adju
- 🔄 LIN Trigger	1Hz	200MHz	Adjustable	256	Adju
-🔳 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Aut
—🗐 Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Aut
—🗒 LIN Trigger-36	1Hz	200MHz	Adjustable	256	2M
—🗐 LIN Trigger-18	1Hz	200MHz	Adjustable	256	4M
—🗐 LIN Trigger-12	1Hz	200MHz	Adjustable	256	6M
—🗒 LIN Trigger-9	1Hz	200MHz	Adjustable	256	8M
— LIN Trigger-6	1Hz	200MHz	Adjustable	256	12M
🖃 LIN Trigger-4	1Hz	200MHz	Adjustable	256	18M
🕂 🧰 External Clock	1Hz	200MHz	Adjustable	256	Adiu

Trigger Settings

The LIN trigger settings dialog box is as below.

LIN Trigger So	ettings			? ×
LIN CH 0	Run → True	-State 1 -	Logic Condition	• OR C AND
Baud rate	State 1 False	Event 1	+or	
Trigger frame Break Sync Data End Wake up	→ ▼ Trigger ×	ID D0 D1 D2 D3	XXh Parit XXh D4 XXh D5 XXh D6 XXh D7	y Xh XXh XXh XXh XXh
Error Detect	+ State x 7 +Counter x 2			
Stop Error Checksum Error Classic mode	Timer 1 Timer 2		A	dvanced Setting >>
Undo Redo	✓ Pre-Trigger Pass Count	Load	Save Default	OK Cancel



Channel: Select channels.

Baud rate: Select baud rate.

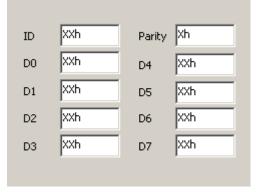
Trigger frame: Provide Break / Sync / Data / End / Wake up triggers.

Error Detect: Provide Sync / Parity / Stop / Checksum error triggers, checksum error

detect include "Classic" and "Enhanced" mode.

Redo / Undo: Click these buttons to redo/restore previous setting.

Trigger settings:



Provide the ID / Parity / Data triggers $\,\circ\,$



LPC Trigger

The LPC trigger settings dialog box is as below.

Mode	Min. S/R	Max. S/R	Available	Min. M	Max. Mem.	
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🚞 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🗏 Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🚞 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
- 🔄 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto	
─≡ Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto	
EPC Trigger-36	1Hz	200MHz	Adjustable	256	2M	
EPC Trigger-18	1Hz	200MHz	Adjustable	256	4M	
ELPC Trigger-12	1Hz	200MHz	Adjustable	256	6M	
EPC Trigger-9	1Hz	200MHz	Adjustable	256	8M	:
EPC Trigger-6	1Hz	200MHz	Adjustable	256	12M	
+ 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 External Clock	1Hz	200MHz	Adjustable	256	Adjustable	L

Trigger Settings

Select LPC Trigger Settings.

LPC Trigger Setting	0	3
Channel - LFRAME# CH 0 - LCLK CH 1 -	$\begin{array}{c} & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ &$	State 1 Logic Condition © OR © AND Event 1 × Event 2 × + OR Cycle Type Memory Read
LAD[0] CH 2 + LAD[1] CH 3 + LAD[2] CH 4 +	State 2 Trigger	START 1 0000b CT/DIR 1 010Xb
LAD[3] CH 5	→ ■ Trigger	ADDR = 8 7654XXXXh TAR 2 XXh SYNC 1 Xh
Error Detect	5 + State x 4	DATA 2 ABh XXh XXh XXh
Address Error (Bus Master)	+ State X4 + Counter x 2	Data Offset
Size Error MSize Error Sync Error	Timer 1 Timer 2	<< Advanced Setting ● ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■
Undo 6 Redo	▼ Pre-Trigger Pass Count 0	

1. Channel



Select channels

Clock Edge Rising Edge : Latch data when Clock Rising or Falling Edge

2. Clause trigger settings

Please refer to the Clause Trigger

3. Trigger settings

Cycle Type	'0 R	ead 💌	ſ		
(Clk #				
START	1	0000b	С	ycle Type	I/O Read 🗸
CT/DIR	1	000Xb			Start of Frame
ADDR =	4	0068h			I/O Read I/O Write
TAR	2	XXh			Memory Read Memory Write
SYNC	1	Xh			DMA Read DMA Write
DATA	2	00h XXh XXh XXh			Firmware Memory Read Firmware Memory Write
					Bus Master 0 - I/O Read Bus Master 0 - I/O Write Bus Master 0 - Memory Read Bus Master 0 - Memory Write
Data Offset	' 	1+			Bus Master 1 - I/O Read Bus Master 1 - I/O Write Bus Master 1 - Memory Read Bus Master 1 - Memory Write

The LPC trigger supports many cycle types. Please select "Start of Frame" and

capture, then choose the cycle type you need.

Sample	Field	#Clocks	LAD	Comment
7002909	START	1	0	Used for Memory or I/O or DMA cycles
7002917	CYCLETYPE+DIR	1	0	I/O Read
7002925	ADDR	4	0068	
7002959	TAR	2	FF	
7002975	SYNC	1	6	Long Wait
7002984	SYNC	1	6	Long Wait
7002992	SYNC	1	6	Long Wait
7003000	SYNC	1	0	Ready
7003009	DATA	2	00	
7003025	TAR	2	FF	
7082283	START	1	0	Used for Memory or I/O or DMA cycles.
7082291	CYCLETYPE+DIR	1	0	I/O Read
7082299	ADDR	4	0064	

LPC decoder result

Other settings :

Switch $=/\neq/>/\leq$ by click = buttonmn.

The input 'X' means don't care.



Data Offset	١.				,		1		1
Fix Offset		,	,	,	,	,		1	: Data offset setting

4. Timer and Counter

Please refer to the Clause Trigger

- Trigger when an error is detected based on the Intel® Low Pin Count Interface Specification.
- 6. Redo/Undo



MIPI SPMI Trigger

Select eSPI Trigger in Hardware Settings.

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max.
+ 🧰 LIN Trigger	1Hz	200MHz	Adjustable	256	Adju
+ 🧰 LPC Trigger	1Hz	200MHz	Adjustable	256	Adju
– 🔄 MIPI SPMI Trigger	1Hz	200MHz	Adjustable	256	Adju
─	200MHz	200MHz	Fixed	Auto	Auto
—I Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto
—≡ MIPI SPMI Trigger-36	1Hz	200MHz	Adjustable	256	2M
─	1Hz	200MHz	Adjustable	256	4M
────── MIPI SPMI Trigger-12	1Hz	200MHz	Adjustable	256	6M
— MIPI SPMI Trigger-9	1Hz	200MHz	Adjustable	256	8M
────────────────────────────────────	1Hz	200MHz	Adjustable	256	12M
MIPI SPMI Trigger-4	1Hz	200MHz	Adjustable	256	18M
+ 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adju
+ 🧰 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adju
🗐 Serial Flash Trigger (800M)-9	800MHz	800MHz	9	256	8M
+ 🧰 SMBus/PMBus Trigger	1Hz	200MHz	Adjustable	256	Adju
<					>

Trigger Settings

Select "MIPI SPMI" in Trigger Settings.

MIPI SPMI Trigger Settings		×
Channel SPMI CLK CH 0 · SPMI DAT CH 1 ·	$\begin{array}{c} \text{Run} \\ \checkmark \\ \text{State 1} \end{array} \text{True} \\ \end{array} \\ \begin{array}{c} \text{False} \end{array}$	State 1 Logic Condition • OR • AND Event 1 + OR
Trigger On	Trigger	Device Address
SSC Bus Timeout		Command XXh
No Response Frame		Data Address XXXXh
Error Check CMD Frame Format CMD Parity Data Address Parity Data Frame Parity Bus Park / Bus Handover	+ State x 7 + Counter x 2	Data XXh XXh XXh XXh XXh XXh
Bus Timeout 96 us	Timer 1 Timer 2	AUX Xh 💌 Advanced Setting >>
Undo Redo 🔽 Pre-Trigg	ger Pass Count 0	Load Save Default OK Cancel



Trigger On: Select Sequence Start Condition (SSC), Bus Timeout, or No Response

Frame to trigger.

Error Check: Check the error of Frame Format, Parity, and Bus Park / Bus

Handover.

Bus Timeout: Set the period of time to wait for SSC.

State Settings:

Device Address		5h					
Command		38h					
Data Address		XXXXh					
Data							
A3h	XXh	XXh	XXh				
XXh	XXh	XXh	XXh				
XXh	XXh	XXh	XXh				
XXh	XXh	XXh	XXh				
AUX	Xh		~				

MIPI SPMI Trigger offer Address, Command and Data parameter to trigger. You may capture the data with don't care (X). Trigger the specific address, command or data by the decode of MIPI SPMI.

Timestamp	A	SR	Device Address(Hex)	Command (Hex)	Data Address - High(Hex)	Data Address - Low(Hex)	Data Frame
-0.838595 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5C	46	00
-0.82933 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	5C	46	80
-0.02058 ms	MPL3		SA=05	38 (Extended Register Read Long: 1Bytes)	1D	40	00
-0.011155 ms	MPL3		SA=05	30 (Extended Register Write Long: 1Bytes)	1D	40	00
-0.00293 ms	MPL3		SA=05	38 (Extended Register Read Long: 1Bytes)	1D	41	A3
0.006135 ms	MPL3		SA=05	30 (Extended Register Write Long: 1Bytes)	1D	41	D2
3.5403 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	56	46	00
3.549725 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	56	46	80
4.058525 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	57	46	00
4.06811 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	57	46	80
4.343265 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5B	46	00
4.352585 ms	MPL3		SA=00	30 (Extended Register Write Long: 1Bytes)	5B	46	80
4.618265 ms	MPL3		SA=00	38 (Extended Register Read Long: 1Bytes)	5C	46	00

MIPI SPMI decode result



NAND Flash Trigger

The settings dialog box below.

Mode	Min. S/R	Max. S/R	Available	Min. M	Max. Mem.	
+ 🚞 CAN Trigger	Data Rate	Data Rate	Adjustable	256	Adjustable	
+ 🚞 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🖹 SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🧰 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	_
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 📄 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
- 🔄 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
- 🗐 NAND Flash Trigger(400M)-18	400MHz	400MHz	18	256	4M	_
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto	=
🖃 NAND Flash Trigger-36	1Hz	200MHz	Adjustable	256	2M	
🗏 NAND Flash Trigger-18	1Hz	200MHz	Adjustable	256	4M	
+ 🧰 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 External Clock	1Hz	200MHz	Adjustable	256	Adjustable	

Trigger Settings

Select NAND Flash trigger settings dialog box is as below.

NAND Flash Trigger Setting			<u>×</u>
Channel — © x 8 — © x	: 16	Run	State 1 Logic Condition ⓒ OR ⓒ AND
I/O Quick Setup		Run 🔶 🍌 True	
C I/O User Defined		State 1 - False	Event 1 +OR
I/O0 (LSB)	сно 🕂		Command
I/O [7:0]			XXh
CLE	сн 8 🕂		Address
ALE	сн 9 🖸		3-Byte Row Address C 4-Byte Row Address
RE	СН 10 🕂		Row XXXXXh
WE	СН 11 🕂	└─ <u></u> Trigger [×]	Column / Feature 🔽 XXXXh
Œ	СН 12 🕂		Data
R/B	СН 13 🕂	+ State × 7	Data Offset
DQS	CH 14 💌	+Counter x 2	
The Flash Startup mode	lode		xxh xxh
) >= 5,0ns		
	J - J - J - J - J - J - J - J - J - J -	Timer 1	XXh XXh
		Timer 2	
Cmds. accepted during bus	y		Advanced Setting >>
E Busy time check			<u> }</u>
Undo Redo	Pre-Trigger	Pass Count 0 · Load Sa	ave Default OK Cancel



Channel:

Select x8 or x16 to trigger 8 / 16 NAND Flash. Just set the I/O0 (LSB) channel

when check the I/O Quick Setup; pressing the button

when check the I/O User Defined will show the dialog below:

NAND Flas	sh I/O		×
I/O0	сно	I/O8 CH 8	3
I/O1	СН 1 :	I/09 CH 9	
I/02	сн 2 🔆	I/010 CH 3	10
I/03	снз 🗄	I/O11 CH	11 <u>-</u>
I/04	СН 4 .	I/012 CH 3	12 -
I/05	сн 5 🔆	I/013 CH 3	13 -
I/06	сн 6	I/014 CH	14 -
I/07	сн 7 🕂	I/015 CH 1	15 🐳
	OK	Can	cel

I/O Quick Setup:

I/00 (LSB)	I/O [14:7]	CH7 $\stackrel{\leftarrow}{\Rightarrow}$ Set LSB = CH 0, MSB = CH 7
I/O0 (LSB)	I/O [14:7]	CH7 \Rightarrow Set LSB = CH 7, MSB = CH 14

DQS: Check DQS pin to select the DDR (Double Data Rate) mode; SDR (Single

Data Rate) mode default.

The Flash Startup mode: Check DQS pin and Toggle / ONFI DDR Mode when

trigger NAND Command/Address/Data under NAND DDR mode.

tREA / tDQSQ:

tREA	>= 5	.Ons -		Г	tDQS	Q>=!	5.0ns		_
1			1		1			1	
			_					_	



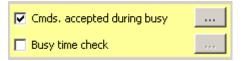
NAND will access data from the edge delay a period. This period call tREA under SDR mode and tDQSQ under DDR mode. The unit is 5 ns under 200 MHz sampling rate and 2.5 ns under 400MHz sampling rate of LA. The period between cursor T and cursor A is tREA.

Time/Div: '	7.5 ns			T .	Α.								
Acquired: .	11:47:26.693		-105 ns	97.5 ns	-90 ns	-82.5 ns	-75 ns	-67.5 ns	-60 ns	-52.5 ns	-45 ns	-37.5 ns	-301
		Idle		DO: O	00		İ	DO	00		1		DO:
	5 I/OO										1		
	6 I/O1												
	7 I/O2												
	8 I/O3												
	9 I/O4												
	10 I/O5						1		_	_	-		
NAND Flash	11 I/O6												
	12 I/O7					_							
	0 CLE					-	-					-	
	3 ALE					1				-		<u>.</u>	
	4 RE		10n		22.5n		7.5n		22.5n		12.	5n 🗌	
	2 WE												
	1 CE1												
Na	MFlark 13 R/B1												
Data Bus	125				00)a:	B <u>(</u>	49		

The period between cursor T and cursor A is tDQSQ.

Time/Div: 7.5	ns						Ą					
Acquired: 12:	07:49.63	-112.5 ns	-105 ns	-97.5 ns	-90 ns	-82.5 ns	-75 ns	-67.5 ns	-60 ns	-52.5 ns	-45 ns	-37.5 ns -3
		Idle		DO: 05	I	DO: 48		DO: E5	I	DO: C3	I	DO: C2
	0 DQO						Í	30n			15n	
	1 DQ1		17.5r			27.5r	<u> </u>			32.5n		
	2 DQ2		17.5r		12.5	n	17.	5n _		<u>27.5</u> n		
	3 DQ3			32.5r	۱					<u>57.5n</u>		
	4 DQ4											
	5 DQ5						17.	5n _		<u>27.5</u> n		
NAND Flash	6 DQ6									92.5n		
	7 DQ7								47.5	n		
	8 CLE											
	9 ALE		_	10 5		17.5		10 5-		17 5		10.5-
	13 W/R			<u>12.5n</u>		17.5n		12.5n		17.5n		12.5n
	12 CLK 14 CE1											
	14 CE1 10 R/B1											
	15 000		15n		15n		15n		15n		15n	⊨ ! .
NandFla	^w 13.0622										EOII	
Data Bus	70	00	OE	HE I	48	ED	E5	; 	C3		C2	

Commands accepted during busy / Busy time check:



The Command accepted during busy checked default, pressing _____ will show the



dialog below:

It means NAND commands still can be triggered while checking the Busy time check.

NAND command (70h/FFh/78h/7Bh) filled default.

Event 1 +0	DR											
	Comr	mand										
70h												
Commands a	ccepted d	uring busy		×								
Commands	accepted d	uring busy —										
1 70h		5 XXh										
2 FFh		6 XXh										
3 78h		7 XXh										
4 7Bh		8 XXh										
	<u> </u>	OK .	Cancel									
			_									
ime/Div: 60 n cquired: 16:3		-100 ns		100 m	s 200	ns 30	10 ns	400 ns	500	Ons	600 ns	
		-100 ns		AT. RÉG.(s 200 (0)	ns 30	0 ns	400 ns	500	0 ns	600 ns	_
	5:22.352 7 I/O0	_			_	ns 30	10 ns	400 ns	500	0 ns	600 ns	_
	5:22.352 7 I/O0 8 I/O1	_			_	ns 30	0 ns 	400 ns	500	0 ns 1 1	600 ns	_
	5:22.352 7 I/O0 8 I/O1 9 I/O2	_			_	ns 30	0 ns 1	400 ns	500	0 ns	600 ns	_
	5:22.352 7 I/O0 8 I/O1	_			_	ns	10 ns	400 ns	50	Dns	600 ns	_
cquired: 16:3	5: 22.352 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4 12 I/O5	_			_	ns 30	10 ns	400 ns	500	Dins	600 ns	_
cquired: 16:3	5: 22. 352 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4 12 I/O5 13 I/O6	_			_	ns 33	10 ns	400 ns	500	Dns I	600 ns	_
cquired: 16:3	5: 22. 352 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4 12 I/O5 13 I/O6 14 I/O7	_			_	ns 3	10 ns	400 ns	500	Dns 1 I	600 ns	_
	5: 22. 352 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4 12 I/O5 13 I/O6 14 I/O7 0 CLE	_			_	ns , , , , , , , , , , , , , , , , , , ,	10 ns	400 ns	500	D ns 1 I	600 ns	_
cquired: 16:3	5: 22. 352 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4 12 I/O5 13 I/O6 14 I/O7	_			_	ns 33	Nons 1	400 ns	500	0 ns	600 ns	
cquired: 16:3	5: 22. 352 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 5 RE 2 WE	_			_	ns 32	0 ns 1	400 ns	500	Dins I	600 ns	
cquired: 16:3	5:22.352 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 1 ALE 5 RE 2 WE 6 CE1	_			_	ns 3	ions 1	400 ns	500	2 ns 1	600 ns	
cquired: 16:3	5122.352 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 1 ALE 5 RE 2 WE 6 CE1	_			_	ns 3	0 ns	400 ns	500	Ons	500 ns	_
cquired: 16:3	5122.352 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 1 ALE 5 RE 2 WE 6 CE1	_			_	ns 3	NQ ns	400 ns		70	500 ns	Busy

Trigger Command 70h during busy time

Check the Busy time check function and pressing _____ will show the dialog below:



Busy time check
tBusy1 tBusy2 tBusy3 tBusy4 tB
-tBusy (Range: 0.1us - 250ms)
>= 25 us
Command
1 10h
2 XXh
3 XXh
4 XXh
OK Cancel

The Busy time check function provide 6 NAND Flash busy time to check and every busy time can be used by 4 commands. It will trigger when the busy time is more than or equal to the tBusy users filled.

Trigger the busy time >= 25 us after NAND command 10h

	_					 	 		
	7 I/OO	Idle	PAGE PROG. #2	(10)					Busy
	8 I/O1								-
	9 I/O2								
	10 I/O3								-
	10 I/O3 11 I/O4								
	11 I/O4 12 I/O5				1	-			-
	12 I/O5 13 I/O6				-				-
									-
	14 I/O7 0 CLE								
	1 ALE								
	I ALE 5 RE					_			
	2 WE								
	6 CE1				>=25 us				-
Nand Flazh	4 K/B1				2-20 US				
Data Bus	147							10	

PAGE PROGRAM #1(80)	0026B1	0000	7B	9D	ED	8A	C3	E7	00	30
	0026B1	0008	26	AO	71	CD	BC	57	EA	25
	0026B1	0010	61	66	31	77	58	AC	39	56
	0026B1	0018	07	BE	9B	63	74	36	C5	B8
	0026B1	0020	4D	C5	68	FO	3B	84	58	14

Trigger Command 80h



Event 1 +	OR							
	Com	mand						
80h								
	Add	ress						
③ 3-Byte R	low Address	C 4-Byte Row	Address					
Row XXX	xxxh							
Column / Fe	eature 🔽	XXXXh						
	Da	ata						
		Data Off						
XXh		XXh						
XXh		XXh						
Time/Div: 60	ns							
Time/Div: 60 Acquired: 13:		-100 ns		100 ns	200 ns	300 ns	4	100 ns
	48:23.961	-100 ns			200 ns	300 ns	4	100 ns
	48:23.961 7 I/O0	,		100 ns 6. #1(80)	200 ns	300 ns	4	100 ns
	48:23.961 7 I/O0 8 I/O1	,			200 ns	300 ns	4	100 ns
	48:23.961 7 I/O0 8 I/O1 9 I/O2	,			200 ns	300 ns	4	100 ns
	48:23.961 7 I/O0 8 I/O1 9 I/O2 10 I/O3	,			200 ns	300 ns	4	100 ns
	48:23.961 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4	,			200 ns	300 ns	4	100 ns
	48:23.961 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05	,			200 ns	300 ns	4	100 ns
Acquired: 13:	48:23.961 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4	,			200 ns	300 ns	4	100 ns
Acquired: 13:	48:23.961 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE	,			200 ns	300 ns	4	HOO ns
Acquired: 13:	48:23.961 7 I/00 8 I/01 9 I/02 10 I/03 11 I/04 12 I/05 13 I/06 14 I/07 0 CLE 1 ALE	,			200 ns	300 ns 1		400 ns
Acquired: 13:	48:23.961 7 I/O0 8 I/O1 9 I/O2 10 I/O3 11 I/O4 12 I/O5 13 I/O6 14 I/O7 0 CLE 1 ALE 5 RE	,			200 ns			100 ns , ,
Acquired: 13:	48: 23.961 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 5 RE 2 WE	,			200 ns	300 ns 		400 ns ,
Acquired: 13:	48: 23.961 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 1 ALE 5 RE 2 WE 6 CE1 2 WE 6 CE1	,			200 ns			100 ns
Acquired: 13:	48: 23.961 7 1/00 8 1/01 9 1/02 10 1/03 11 1/04 12 1/05 13 1/06 14 1/07 0 CLE 1 ALE 5 RE 2 WE 6 CE1 2 WE 6 CE1	,			200 ns			100 ns

Trigger Row Address: 0026B1h, Column Address: 0000h

Event 1 + OR	Time/Div: 250 ns	, and the second second second second second second second second second second second second second second se
	Acquired: 13:43:28.727 -2.8us -2.4us -2us -1.6us -1.2us -800 ns	-400 ns
Command	Idle Col.00 Col.00 Row B1	Row 26 Row OD
80h		1.68u
Address	81/01 7	20n 960r
		25n
③ 3-Byte Row Address ① 4-Byte Row Address	11 1/04	
Row 0026B1h	121/05 //20n	1.675u
Column / Feature 🔽 0000h	NAND Flash 13 I/O6 1.44u	960r
	14 I/07 720 n	2.39
Data		
Data Offset		
1	5 RE 2 WE 240n 480n 240n 480n 240n 480n 24	40n 480n 480r
	6 CE1	
XXh XXh	Nex/Flack 4 R/B1	
000		
XXh XXh	Data Bus 147 00 B1 2	26 00
pant pant		

Trigger Row Address: 02E200h, no Column Address



Event 1 +OR	Time/Div: 6								. •	l
	Acquired: 1	L6:33:09.274	-600 ns	-500 ns	-400 ns	-300 ns	-200 ns	-100 ns	🎗	
Command			Idle	R	ow 00		Row E2		Row 0	2
60h		0 I/OO								
Address		1 I/O1		<u> </u>						
③ 3-Byte Row Address 〇 4-Byte Row Address		2 I/O2 3 I/O3								
Row 02E200h		4 I/O4								
Column / Feature 🔲 XXXXh		5 I/O5			230n					
	NAND Flash	6 I/O6			230n					
Data		7 I/07			230n					
Data Offset —		13 CLE								
		12 ALE								
		15 RE								
		14 WE		120n	110n	110	n <u>1</u> .	20n		
XXh XXh		10 CE1								
	Har	9 R/B1								
XXh XXh						Y				
	Data Bus	70	00		E2					

Trigger the NAND Data

Event 1 +OR	Time/Div: 500 n							I
Command	Acquired: 13:37	:02.430	-3.2 us	-2.4 1 - 1 - 1 - 1	4 us -1.1	6us - Liilii	800 ns	
80h		7 1/00	Idle	DI: 7B	DI: 9D	DI: ED	DI: 8A	DI: C3
		3 I/O1			2.16u		720n	1.44u
Address		9 I/O2 🛏		720n	1.44			2.16u
③ 3-Byte Row Address ○ 4-Byte Row Address		10 I/O3 🛏			1.445 2.88u		<u> </u>	
Row XXXXXh		11 I/04		1.43				3.605u
Column / Feature 🔽 🛛 🛛 🗸		12 I/05 13 I/06		715n	725n	720n	1.44	
Data		14 I/07		715n	725n	720n	720n 3.605u	1.44u
Data Offset							5.0050	
		1 ALE						
		5 RE 2 WE 4	180n 480n	480)n 🗌 480r	480	n 🦳 480n	480n
9Dh EDh		5 CE1		400			1 4001	4001
	NandFlark	4 R/B1						
8Ah C3h	Data Bus	147	00	7B	9D	ED	84	C 3
					- 30			

Trigger the NAND Data (fixed offset)

Event 1 +OR	Time/Div: 50							U
Command	Acquired: 13	:32:54.430		.2 us -2.	4us Liilii	1.6 us	-800 ns	
80h		7 I/OO	Row 26	Idle	DI: 7	3 DI: 90) DI: ED	DI: 8A
		7 I/O0 8 I/O1				2.16u		720n
Address		9 I/O2		960n	720n	1.4	4u 🛛	2
💿 3-Byte Row Address 🔿 4-Byte Row Address		10 I/O3		1.675	u	1.44		<u>1.44</u> u
Row XXXXXXh		11 I/O4				2.8	Bu	
		12 I/05			1.43			3
Column / Feature 🔽 XXXXh	NAND Flash	13 I/06		960n	715n	725n	720n	1.44u
Data		14 I/07			715n	725n	720n	720n
		0 CLE						3.605u
Data Offset		1 ALE				-		
		5 RE						
		2 WE	- 490n	485n 47	5n 47	5n 🗌 480)n 🥅 480	n 🗍 480n
7Bh 9Dh		6 CE1						
0 1		4.0/04						
EDh BAh	NandF	larh			r	. – U		
2 3	Data Bus	147	26	00	7B	9D	ED	8A
J								



SD/eMMC Trigger

The settings dialog box below.

Mode	Min. S/R	Max. S/R	Available	Min. M	Max. Mem.	
+ 🚞 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🧰 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🗉 Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	
– 🔄 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
_	1.6GHz	1.6GHz	4	256	16M	
SD/eMMC Trigger(800M)-9	800MHz	800MHz	9	256	8M	
SD/eMMC Trigger(400M)-18	400MHz	400MHz	18	256	4M	
SD/eMMC Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto	Ξ
SD/eMMC Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto	
SD/eMMC Trigger-36	1Hz	200MHz	Adjustable	256	2M	
SD/eMMC Trigger-18	1Hz	200MHz	Adjustable	256	4M	
SD/eMMC Trigger-12	1Hz	200MHz	Adjustable	256	6M	
SD/eMMC Trigger-9	1Hz	200MHz	Adjustable	256	8M	
BD/eMMC Trigger-6	1Hz	200MHz	Adjustable	256	12M	
SD/eMMC Trigger-4	1Hz	200MHz	Adjustable	256	18M	
+ 🗀 LPC Trigger	147	200MH7	∆diuctable	256	Adjustable	Ŧ

Trigger Settings

Select SD/eMMC Trigger Settings dialog box below.

SD/eMMC 1 ger Settings 2	4
$\begin{array}{c c} Channel \bullet & & & \\ CLK & CH & 0 & \\ CMD & CH & 1 & \bullet \\ DATA0 & CH & 2 & \bullet \\ AUX & CH & 3 & \bullet \\ \end{array}$ $\begin{array}{c c} Frotocol \\ \hline \bullet & SD & \bullet eMMC \end{array}$	State 1 Logic Condition OR C AND Event 1 × Event 2 × + OR Image: Condition OR C AND © Command Response AND Timer 1 Image: Condition Image: Condition Cmd 13 - SEND_STATUS Image: Condition Image: Condition Image: Condition Image: Condition DATA0 = Image: Condition Image: Condition Image: Condition Image: Condition DATA0 = Image: Condition Image: Condition Image: Condition Image: Condition DATA0 = Image: Condition Image: Condition Image: Condition Image: Condition ST Command Image: Condition Image: Condition Image: Condition Image: Condition ST Command Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition Image: Condition
Idle Period > 20ms + State x 4 tODLY Time = 1.875ns + Counter x 2 Image: Check CRC Error Image: Check CRC Error Image: Active on Aux High	RCA[/:0] 24h Stuff Bits[15:8] 00h Stuff Bits[7:0] 00h CRC XXh 1
Undo Redo V Pre-Trigger Pass Count 0	Load Save Default OK Cancel

1. Channel



CLK: Clock signal.

CMD: Command signal.

Data0: eMMC only and judge response is R1 or R1b.

AUX: auxiliary CRC check.

Protocol-	
SD	C eMMC

select SD or eMMC trigger.

Idle Period:If clock keep idle and over the idle period value, then reset the state.

tODLY (Output delay) Time: When response, the delay time after clock edge

is the valid command data.

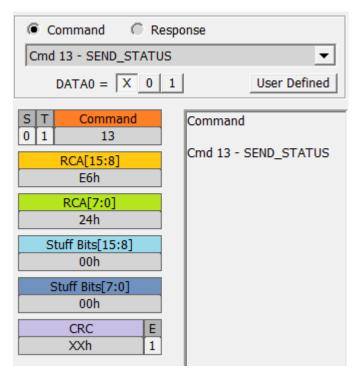
Check CRC Error: Trigger the CRC error, if "Active on AUX High" is

checked, the CRC check only when the AUX channel keeps high.

2. Clause trigger settings

Please reference Clause Trigger chapter

3. Trigger settings





Timestamp	Command	Response	Data	CRC7	Information
0.011239375 ms	CMD18:READ_MULTIPLE_BLOCK		0042 59C0h	6Ah	
0.011560625 ms		R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h	
0.413851875 ms	CMD12:STOP_TRANSMISSION		0000 0000h	30h	
0 414173125 mg		R1b.CMD12.STOP_TRANSMISSION	0000 0B00b	3Fh	
0.976969375 ms	CMD13:SEND_STATUS		E624 0000h	38h	
0.977285 ms		R1 :CMD13:SEND_STATUS	0000 0900h	1Fh	
0.98829625 ms	CMD18:READ_MULTIPLE_BLOCK		0042 5CC0h	4Dh	
0.9886175 ms		R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h	
1.330894375 ms	CMD12:STOP_TRANSMISSION		0000 0000h	30h	
1.331215625 ms		R1b:CMD12:STOP_TRANSMISSION	0000 0B00h	3Fh	
2.150086875 ms	CMD13:SEND_STATUS		E624 0000h	38h	
2.1504025 ms		R1 :CMD13:SEND_STATUS	0000 0900h	1Fh	
2.161419375 ms	CMD18:READ_MULTIPLE_BLOCK		0043 4000h	0Ah	
2.161740625 ms		R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h	

SD/eMMC decoder

Parameter :

DATO = X 0 1 : use Data0 to judge the R1 and R1b.

Input trigger value, input 'X' means don't care.

Append 'h' for HEX, 'b' for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

User Defined add the command reserved:

Command	Description
Imd 1	Test1
Imd 5	Test2
Double Click)	
	(OK) Cancel
ommand Des	cripti 🗙
Cmd 5 🗾 Test2	2
	Cancel

4. Timer and Counter

Please refer to the Clause Trigger



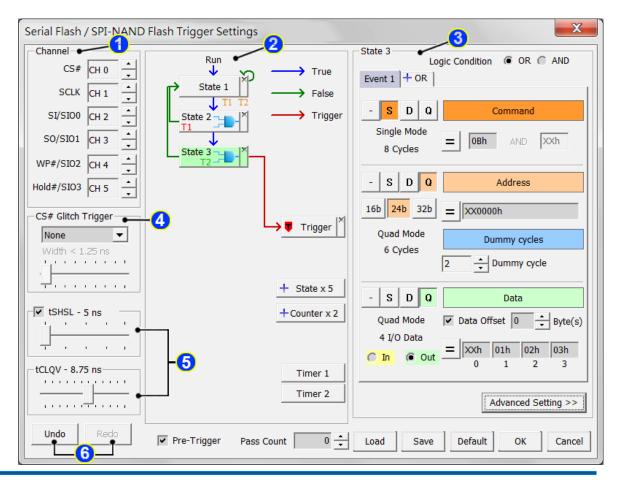
Serial Flash Trigger

Mode	Min. S/R	Max. S/R	Available	Min. M	Max. Mem.	-
🗏 800M	800MHz	800MHz	9	256	8M	
≝ 400M	400MHz	400MHz	18	256	4M	
+ 🧰 200M	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 UART Trigger	Baud Rat	Baud Rat	Adjustable	256	Adjustable	
+ 🧰 CAN Trigger	Data Rate	Data Rate	Adjustable	256	Adjustable	
+ 🧰 I2C Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 I2S Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
SPI Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🧰 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	_
🗏 Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	=
+ 🧰 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 External Clock	1Hz	200MHz	Adjustable	256	Adjustable	

The settings dialog box below.

Trigger Settings

Select Serial Flash Trigger Settings dialog box below.





1. Channel:

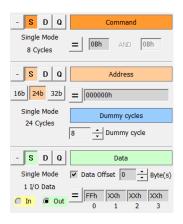
Select channels

2. Clause trigger settings

Please reference Clause Trigger chapter

3. Trigger settings

The setting result will show in the trigger flow chart.



Idle (0B)FAST_READ	Addr:00	Addr:00	Addr:00	DMY:00	DO:FF	
2.314u	972.5n		693.75n			1.4

Select the mode of command:

- S D Q	- S D Q	- S D Q	- S D Q
	Single Mode	Dual Mode	Quad Mode
	8 Cycles	4 Cycles	2 Cycles
Don't Care	Single Mode	Dual Mode	Quad Mode

Specified values in command, address and data fields, or input 'X' for don't care.

Check **Data Offset** to trigger on data at specified position.

EX: if Data Offset = 0, Data = FFh XXh XXh XXh. It will trigger on Data0= FFh and

Data1, 2, 3=any data.

Dummy cycles is needed when data field is specified, it could be 0 to 8 clocks wide



depends on the waveform.

Click \equiv button to switch NOT trigger \neq , it can have 2 input values when NOT trigger was selected.

4. CS Glitch Trigger

Trigger when CS glitch (High/Low/Either) pulse. The glitch pulse setting can be from 0.625ns to 80ns.

- 5. tSHSL and tCLQV.
- 6. Redo/Undo



SMBus/PMBus Trigger

Mode	Min. S/R	Max. S/R	Available ch.	Min. Mem.	Max. Mem.	
+ 🧰 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🗒 Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	
🛨 🧰 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🛨 🧰 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
🛨 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
- 🔄 SMBus/PMBus Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
—🗐 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto	
—🗐 Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto	
-🗐 SMBus/PMBus Trigger-36	1Hz	200MHz	Adjustable	256	2M	
—🗐 SMBus/PMBus Trigger-18	1Hz	200MHz	Adjustable	256	4M	
────────────────────────────────────	1Hz	200MHz	Adjustable	256	6M	
– SMBus/PMBus Trigger-9	1Hz	200MHz	Adjustable	256	8M	
–	1Hz	200MHz	Adjustable	256	12M	
🗐 SMBus/PMBus Trigger-4	1Hz	200MHz	Adjustable	256	18M	
+ 🧰 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	•

Select SMBus/PMBus Trigger Settings.

Trigger Settings

The SMBus/PMBus trigger settings dialog box is as below.

SMBus/PMBus Trigger Settings		×
Channel	Run	Logic Condition
SMB/PMBCLK CH 0	True	
SMB/PMBDAT CH 1	False	it 1 + OR
CH 2 📩	Trigger Fie	
Protocols Select	Addr	ess XXh
SMBus		
SMBus		X
O SBS	Comr	nand XXh
	→ ▼ Trigger	
C SPD SDRAM		
C PMBus	+ State × 7	
Triggers	+Counter x 2	
🗖 Repeat Start		x • x • x • x •
🗖 Stop	5	xxh Xxh Xxh
🗖 АСК		
	Timer 1	
Check PEC	Timer 2	Xh 💌
None Group Command		
C Group Command		Advanced Setting >>
Undo Redo V Pre-Trig	ger Pass Count 0 🔒 Loan	d Save Default OK Cancel

Channel: Select channels. AUX unchecked default.



Protocols Select: Select Protocols, it provides SMBus / PMBus trigger function.

Triggers: Provide the Repeat Start / Stop / ACK / NACK and Check PEC triggers.

Redo / Undo: Click these buttons to redo/restore previous setting.

Trigger settings:

Fields	
Address	Write X V
Command	ACK 🔽
Data	
ACK 2Ch	ACK V NACK X V 01h 8Eh XXh

Provide the Wr/Rd Address / Command / Data and Acknowledge triggers.



SVI2 Trigger

Mode	Min. S/R	Max. S/R	Available	Min. M	Max. Mem.	
+ 🚞 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🧰 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
- 🔄 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
- 🗏 Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto	
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto	
🗉 SVI2 Trigger-36	1Hz	200MHz	Adjustable	256	2M	
SVI2 Trigger-18	1Hz	200MHz	Adjustable	256	4M	
SVI2 Trigger-12	1Hz	200MHz	Adjustable	256	6M	Ξ
SVI2 Trigger-9	1Hz	200MHz	Adjustable	256	8M	
SVI2 Trigger-6	1Hz	200MHz	Adjustable	256	12M	
SVI2 Trigger-4	1Hz	200MHz	Adjustable	256	18M	
+ 🧰 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🚞 External Clock	1Hz	200MHz	Adjustable	256	Adjustable	

Trigger Settings

The SVI2 trigger settings dialog box is as below.

SVI2 Trigger Settings	X
Channel SVC CH 0 SVD CH 1	Run True State 1 False True False True Tr
SVT CH 2 . AUX CH 3 .	Trigger VD Packet VD VDDNB PSIO_L Xh Xh Xh Xh Xh V PSII_L TFN Xh Xh Xh Xh Xh
Frror Detect	xh xh Load Line Slope Trim xh Trigger Trigger
	+ State x 7 + Counter x 2 SVID AND AND SVID AUX AUX AUX
	Timer 1 VDD Voltage Timer 2 XXXh
Undo Redo	Image: Pre-Trigger Pass Count 0 Load Save Default OK Cancel



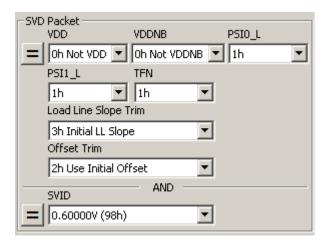
Channel: Select channels, SVT checked default.

Error Detect: Detect SVD / SVT packet error. It will check the size of packet.

Redo/Undo: Click these buttons to redo/restore previous setting.

Trigger settings: Trigger SVD / SVT packet.

SVD Packet:



Timestamp	VDD	VIDDNB	SVID Code	PSI	TFN	Slope Trim	Offset Trim	SVT	Volt	Volt/Current
-0.00144 ns	0	0	0.600007 (98)	3	1	Initial LL Slope(3)	Use Initial Offset(2))		
0.016945 ns	VDD(1)	0	1.30000V (28)	3	0	Initial LL Slope(3)	Use Initial Offset(2)			

SVT Packet:

SVT Packet	SVTO	
1h VDD Voltage	▼ 1h	-
= 1.33750V ((122h)	•
VDDNB Volt	age	
= 1.15625V ((13Fh)	•

Timestamp	VDD	VDDNB	SVID Code	PSI	TFN	Slope Trim	Offset Trim	SVT	Volt	Volt/Current
-0.001175 ms								3	1.33750V (122)	1.15625V (13F)
0.018485 ns								3	1.16250V (13E)	1.15000V (140)
0.038145 ns								3	0.97500V (15C)	1.15000V (140)

VOTF Complete + AUX High



SVT Packet SVT1 Ih VDD Voltage	SVTO Oh	AUX 1h
= xxxh	-	
VDDNB Voltage		
= XXXh	•	

Timestamp	Offset Trim	SVT	Volt	Volt/Current	Error	Description
-0.014045 ms		3	0.97500V (15C)	1.15000V (140)		Voltage Only
(-0.00029 ms		2				VOTF Complete)
0.00561 ms		3	0.75625V (17F)	1.15000V (140)		Voltage Only

Time/Div:	30 ns						P
Acquired:	10:59:2	-350 ns	-300 ns -	250 ns -200 ns	-150 ns -10	00 ns -50 ns	<mark>\$</mark>
SVC	•				30n 20n 30n	20n 30n	
SVD	1						
SVT	2			125n	50n	85n	
		Idle		S	SVT:	1: 1 SVTO: 0 P	
SVI2	o svc				30n 20n 30n	20n 30n	
	1 SVD						
s	2 SVT			125n	50n	85n	
AUX	3				370n		

Other settings: Switch $=/\neq$ by clicking = button when trigger VDD,

VDDNB...Offset Trim in SVD packet.

Switch	$=/\neq/>/\leq$	by clicking	button when trigger SVID in SVD packet.
Switch	$=/\neq$ by click	cing 📕 button	when trigger SVT1, SVT0 in SVT packet.

Switch $=/\neq/>/\leq$ by clicking = button when trigger VDD Voltage /

VDDNB Voltage in SVT packet.



USB1.1 Trigger

Mode	Min. S/R	Max. S/R	Available	Min. M	Max. Mem.	
+ 🚞 SPI Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVID Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
Serial Flash Trigger(800M)-9	800MHz	800MHz	9	256	8M	
+ 🧰 SD/eMMC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 LPC Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 NAND Flash Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
+ 🧰 SVI2 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
– 🔄 USB 1.1 Trigger	1Hz	200MHz	Adjustable	256	Adjustable	
Transitional Storage-32	200MHz	200MHz	Fixed	Auto	Auto	
Transitional Storage-8	200MHz	200MHz	Fixed	Auto	Auto	
USB 1.1 Trigger-36	1Hz	200MHz	Adjustable	256	2M	
USB 1.1 Trigger-18	1Hz	200MHz	Adjustable	256	4M	Ξ
USB 1.1 Trigger-12	1Hz	200MHz	Adjustable	256	6M	_
USB 1.1 Trigger-9	1Hz	200MHz	Adjustable	256	8M	
USB 1.1 Trigger-6	1Hz	200MHz	Adjustable	256	12M	
USB11 Trigger-4	1Hz	200MHz	Adjustable	256	18M	
+ 🧰 External Clock	1Hz	200MHz	Adjustable	256	Adjustable	_

Select USB1.1 Trigger Settings.

Trigger Settings

The USB1.1 trigger settings dialog box is as below.



USB1.1 Trigger Settings						x
Channel D+ CH 0 CH 0 CH 1 CH 1 CH 2 CH 2 CH 2 CH 2 CH 2 CH 2 CH 2 CH 2	State 1	True False Trigger	State 1 Event 1 + Fields PID	Logic Condition OR	© OR © AND	1
Speed Full speed C Low speed			Frame Number	XXXh		
Triggers Enter Suspend (Idle > 3 ms) Exit Suspend (Exit idle > 10 ms)		Trigger 🎽	Address	= XXh	_	
CRC-5 XXh			Endpoint	Xh		
CRC-16 XXXXh Frror Detect PID Error		tate x 7	Data		ata Offset	
CRC-5 Error			XXh	XXh XXh	XXh	
EOP Error Bit Stuffing Error		imer 1 imer 2	_AUX	Xh	V	
				(Ad	vanced Setting >>	
Undo Redo 🔽 Pre-Trig	ger Pass Count	0 -	Load S	5ave Default	OK Canc	el

Channel: Select channels. AUX unchecked default.

Speed: Speed mode. Select Full / Low speed.

Triggers: Trigger Enter Suspend / Exit Suspend / CRC-5 / CRC-16.

Error Detect: Trigger PID Error / CRC-5 Error / CRC-16 Error / EOP Error / Bit

Stuffing Error.

Redo/Undo: Click these buttons to redo/restore previous setting.

Trigger settings: Trigger PID:SETUP; Address = 01h; Endpoint = 0h



Fields	
PID	SETUP
Frame Number	xxxh
Address	= T
Endpoint	Oh
Data	Data Offset
XXh	XXh XXh XXh

Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC5	DATA	ASCII	CRC16	Packet Duration
-0.00591 ms	357	SOF (TOKEN)	0288			01				3 us(33 Bits)
-0.002245 ms	358	SETUP (TOKEN)		01	00	17				3 us(33 Bits)
0.00142 ms	359	DATAO (DATA)					CO OC 84 00 00 00 01 00		060E	8 us(96 Bits)
0.010425 ms	360	ACK (HANDSHAKE)								1 us(17 Bits)
1.009085 ms	361	SOF (TOKEN)	0289			1E				3 us(33 Bits)
1.012755 ms	362	OUT (TOKEN)		01	02	03				3 us(33 Bits)
1.01642 ms	363	DATAO (DATA)					5A OF 66 01	Z.f.	EC06	6 us(64 Bits)
1.022755 ms	364	ACK (HANDSHAKE)								l us(17 Bits)

Trigger PID:DATA0; Data: 5Ah, 0Fh, 66h, 01h

Fields									
PID	DATA0								
Frame Number	XXXh								
Address	= 💌 XXh								
Endpoint	Xh								
Data	Data Offset								
5Ah	0Fh 66h 01h								

Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC5	DATA	ASCII	CRC16	Packet Duration
-45.379 ms	1	SOF (TOKEN)	0289			1E				3 us(33 Bits)
-45.375335 ms	2	OUT (TOKEN)		01	02	03		_		3 us(33 Bits)
-45.371665 ms	3	DATAO (DATA)					5A OF 66 01	Z.f.	EC06	5 us(64 Bits)
-45.365335 ms	4	ACK (HAND SHAKE)								2 us(17 Bits)
-45.362915 ms	5	SOF (TOKEN)	0288			01				3 us(33 Bits)
-45.35925 ms	6	SETUP (TOKEN)		01	00	17				3 us(33 Bits)
-45.355585 ms	7	DATAO (DATA)					CO OC 84 00 00 00 01 00		060E	8 us(96 Bits)
-45.346585 ms	8	ACK (HAND SHAKE)								2 us(17 Bits)

Trigger PID:DATA0; 4 Byte Data(Fixed offset): C0h, 0Ch, 84h, 00h



Fields										
PID	DAT	'A0	-							
Frame Number	XXX	h								
Address	= XXh		•							
Endpoint	Xh									
Data		Data Off								
COh OCh 84h OOh										
0	1	2	3							
Timestamp	No.	PID	Frame Number	Address	Endpoint	CRC 5	DATA	ASCII	CRC16	Packet Duration
2.03475 ms	369	SOF (TOKEN)	0289			1E				3 us(33 Bits)
2.038415 ms	370	OUT (TOKEN)		01	02	03				3 us(33 Bits)
2.042085 ms	371	DATAO (DATA)					5A OF 66 01	Z.f.	EC06	5 us(64 Bits)
2.04842 ms	372	ACK (HAND SHAKE)								1 us(17 Bits)
2.050835 ms	373	SOF (TOKEN)	0288			01				3 us(33 Bits)
2.054505 ms	374	SETUP (TOKEN)		01	00	17				3 us(33 Bits)
2.05817 ms	375	DATAO (DATA)					CO OC 84 00 00 00 01 00		060E	8 us(96 Bits)
2.06717 ms	376	ACK (HAND SHAKE)								1 us(17 Bits)

Other settings: Select =, <, >, <=, >=, InRange, Not InRange in the Address field.