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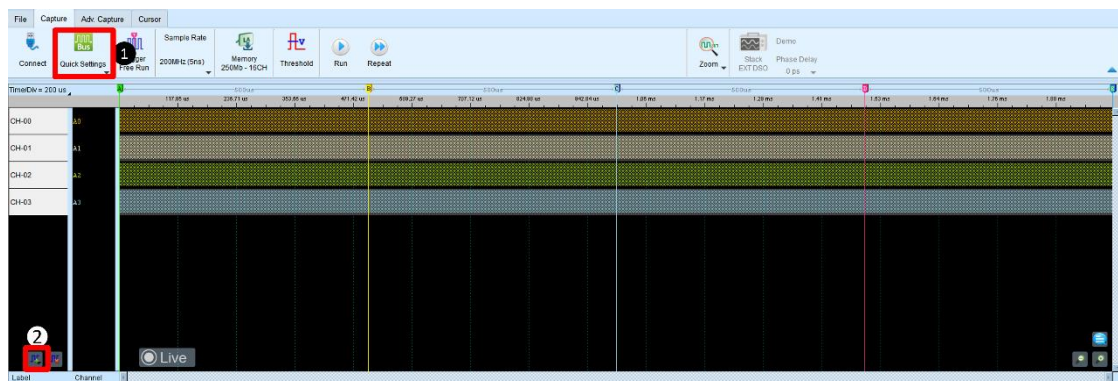
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Chapter 1 Bus Decode

Basic operation

Add a Bus Decode



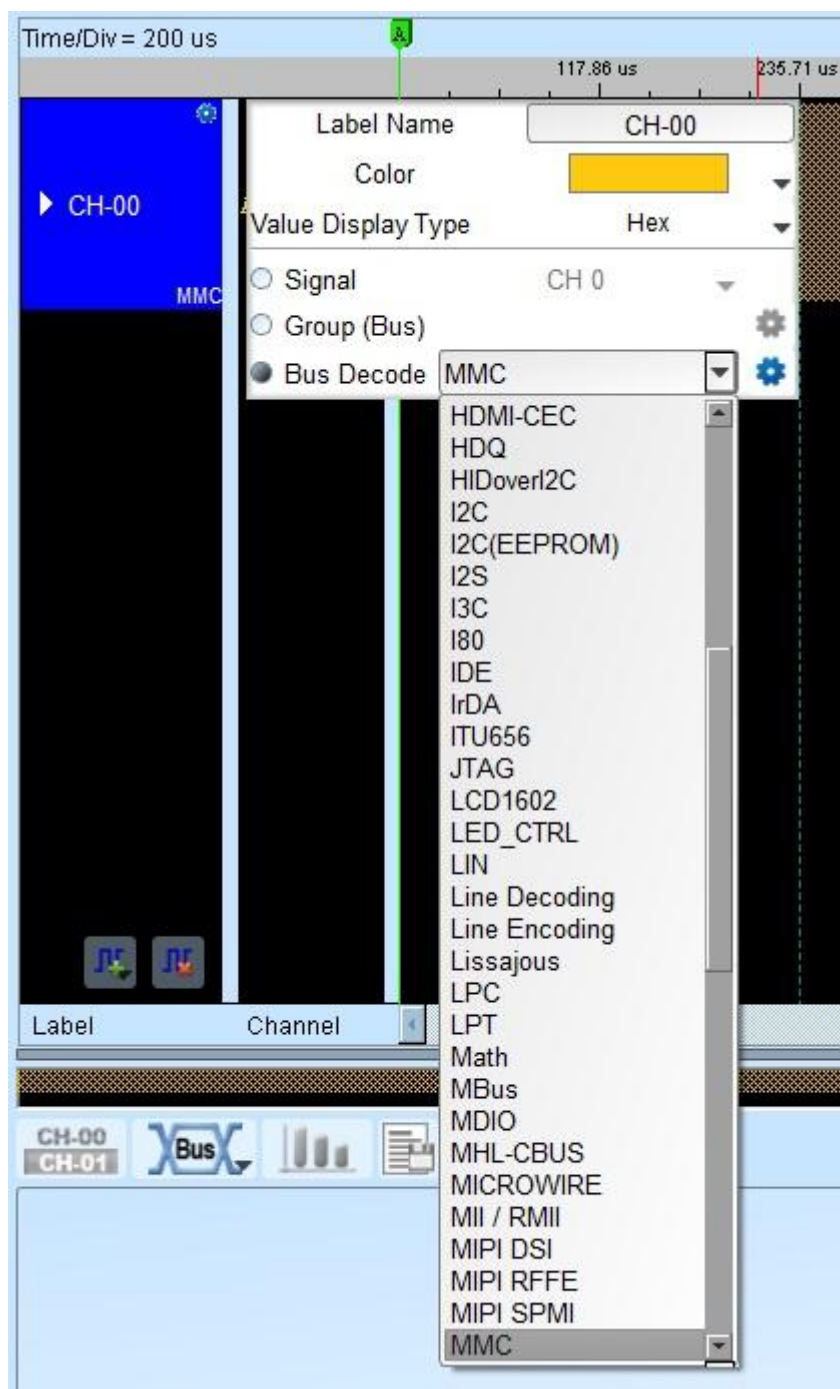
Method 1:

Click the Quick Setting in the menu (number 1 in the figure above), and select the bus decode.

Method 2:

Click Add Bus Decode (number 2 in the figure above) in the Label menu or right-click the label field to show the dialog box.

Advance channel setting



1. **Bus Name:** Enter the label name with 31 characters or less. (Chinese word expresses two characters.)
2. **Color:** Set the waveform color.
3. **Display the waveforms with decode**
4. **Display the waveforms with its decode together.**
5. **Advance:**

Set the decode parameters or press **OK** to use default settings. There are “Channel”/“Parameter”, “Color”, “Range” settings

The screenshot shows a software window titled "Parameters" with a close button (X) in the top right corner. The window is divided into three main sections:

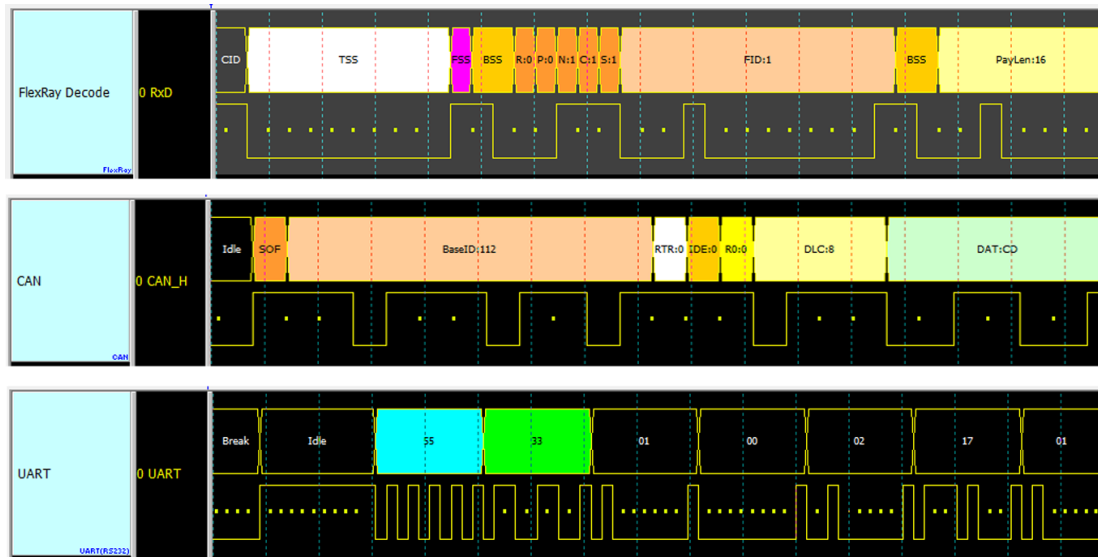
- Parameters:** Contains a small icon of a document with a pencil and a waveform diagram.
- Color:** Features a color bar with various colored squares. To the right of the color bar are four vertical dropdown menus with colored backgrounds (green, blue, yellow, and orange).
- Range:** Includes a section labeled "Decode Range" with a waveform icon. Below this are two dropdown menus labeled "From" and "To". The "From" dropdown is set to "Buffer Head" and the "To" dropdown is set to "Buffer Tail".

At the bottom of the window, there are three buttons: "Default" (with a blue circle icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

Specially Bus Decode

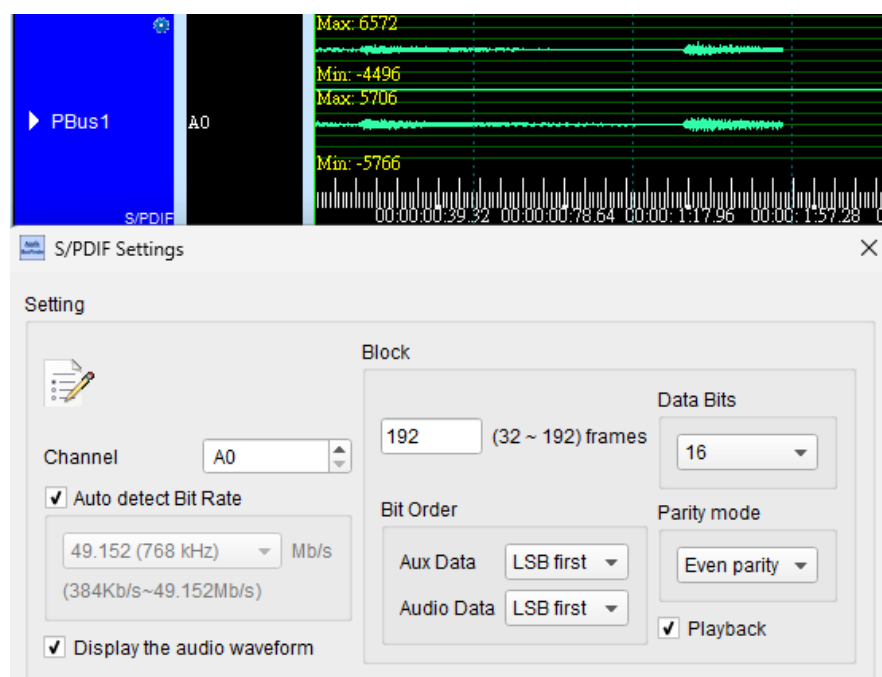
The bus decodes display the data in text format, but some decodes are able to show the original form for the data such as voice (I2S decode...), image, analog waveform (ADC decode) etc.

UART/CAN/FlexRay..bus decodes (released since 2009/9, LA Viewer Ver2.0):
The data is displayed according to bit points in order to calculate the bit number °



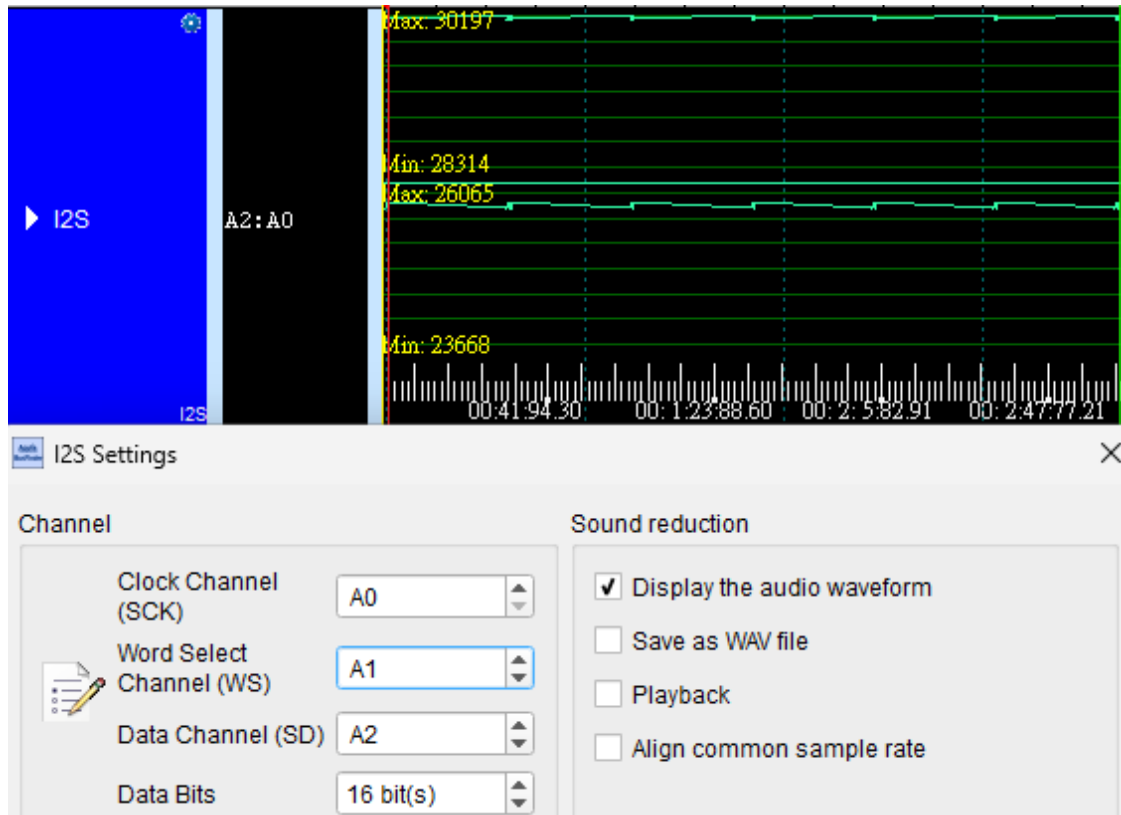
S/PDIF analysis (released since 2010/11, LA Viewer Ver2.5):

Display the data in sound waveform.



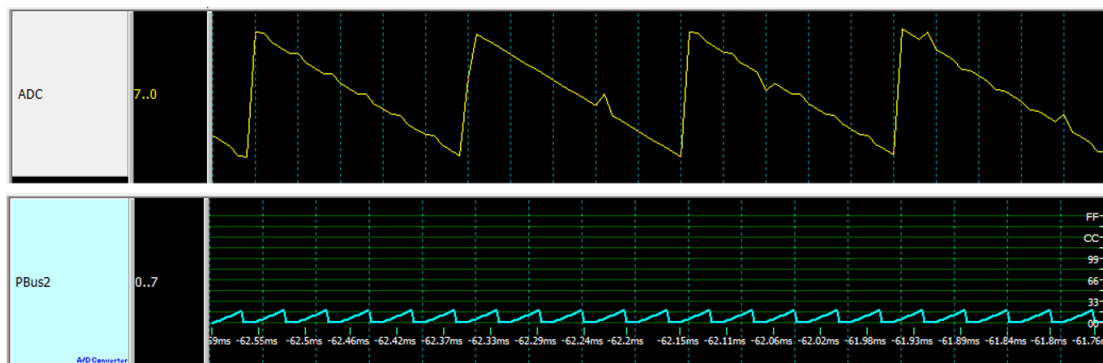
I²S analysis (released since 2011/9, LA Viewer Ver2.6.3):

Display the data in sound waveform ◦



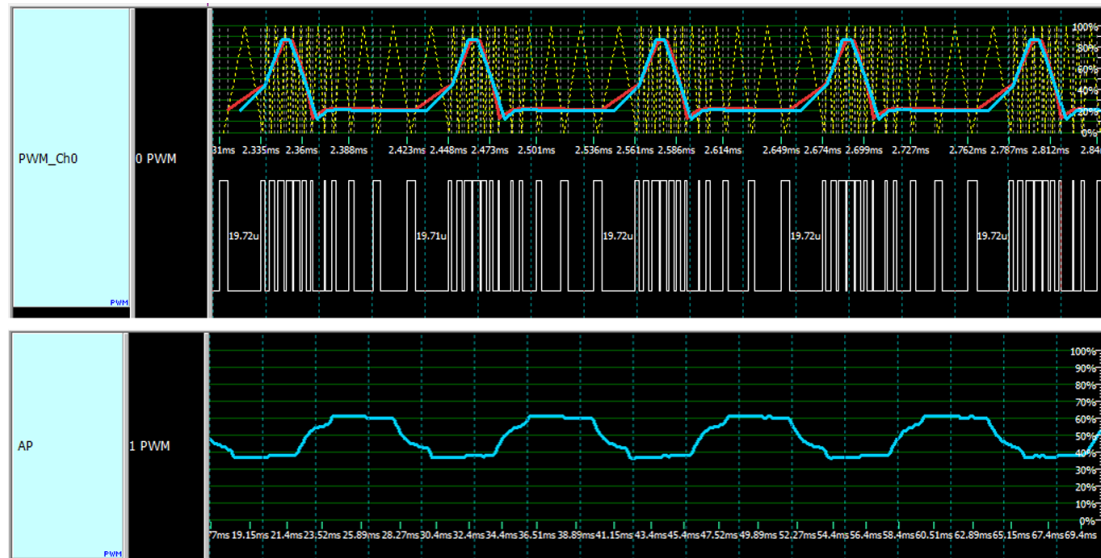
ADC bus decode:

Display the input data in graph ◦



PWM analysis (released since 2012/8, LA Viewer Ver2.7.3):

Restore and display the data in the waveform window as percentile or frequency °



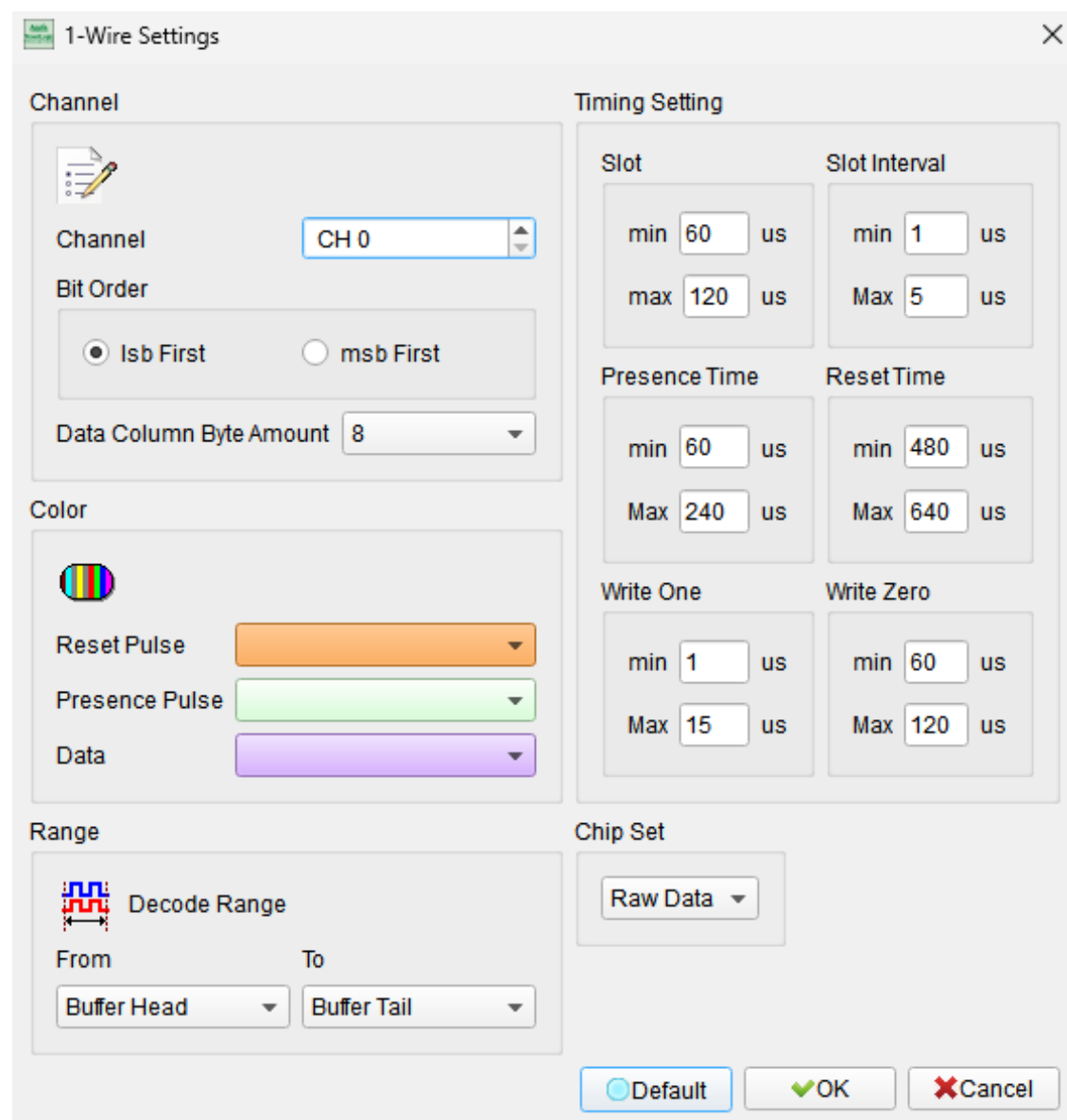
Bus Decode Settings Introduction

Please note: All are prefixed with 'Ch' except BusFinder or LA in the channel, which are prefixed with 'A'.

1-Wire

Developed by Dallas Semiconductor, the 1-Wire protocol defines several signal types such as Reset Pulse, Presence Pulse, Write 1, Write 0, Read 1, and Read 0, and combines these signal types into a command sequence. The transmission mode is LSB (Least-significant bit) to MSB (Most-significant bit), and the transmission speed is divided into Overdrive speed and Standard speed.

Settings



1-Wire Settings

Channel

Channel: CH 0

Bit Order: ☒ lsb First ☐ msb First

Data Column Byte Amount: 8

Timing Setting

Slot

min: 60 us
max: 120 us

Slot Interval

min: 1 us
Max: 5 us

Presence Time

min: 60 us
Max: 240 us

Reset Time

min: 480 us
Max: 640 us

Write One

min: 1 us
Max: 15 us

Write Zero

min: 60 us
Max: 120 us

Color

Reset Pulse: [Orange]

Presence Pulse: [Green]

Data: [Purple]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Chip Set

Raw Data

Default OK Cancel

Channel: Setting the Data Channel Source

Bit Order: Set whether the analyzed data is LSB first or MSB first.

Data Byte Column Amount: Set how many bytes of data are displayed in a row of the Data field in the Report area; user can select 8, 16, or 32.

Timing Setting: all unit is us.

1. Slot Time:

I. **Min:** Set the minimum length of time of a slot.

II. **Max:** Set the maximum length of time of a slot.

2. Slot Interval:

I. **Min:** Set the minimum length of time between each slot.

II. **Max:** Set the maximum length of time between each slot.

3. Reset Time:

I. **Min:** Set the minimum length of time that the waveform will be pulled down when is in Reset.

II. **Max:** Set the maximum length of time that the waveform will be pulled down when is in Reset.

4. Presence Time:

I. **Min:** Set the minimum length of time that the waveform will be pulled down when is in Presence.

II. **Max:** Set the maximum length of time that the waveform will be pulled down when is in Presence.

5. Write One:

I. **Min:** Set the minimum length of time that the waveform will be pulled down when 1 is written.

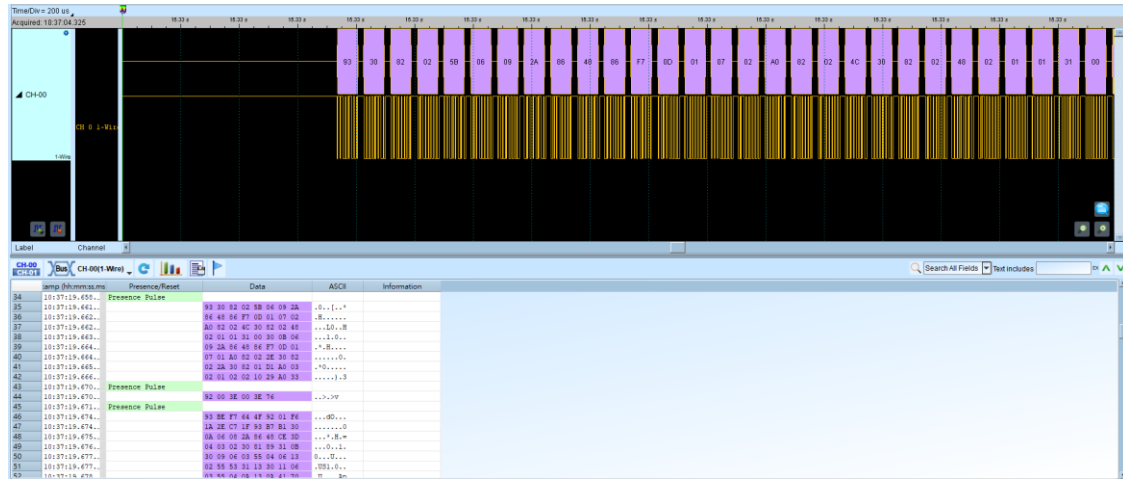
II. **Max:** Set the maximum length of time that the waveform will be pulled down when 1 is written.

6. Write Zero:

I. **Min:** Set the minimum length of time that the waveform will be pulled down when 0 is written.

II. **Max:** Set the maximum length of time that the waveform will be pulled down when 0 is written.

Result



10BASE-T1S

10Base-T1S uses Differential Manchester Encoding (DME). DME encodes data based on whether there is a transition within the clock period, indicating the logical state of the signal. If there is no transition within the clock period, the data state is logical 0. If transitions (either positive or negative) occur within the clock period, the data state is logical 1.

10BASE-T1S operates in a half-duplex bus configuration with a maximum length of 25 meters. It supports multipoint connections with two to eight nodes. The "S" in the standard name denotes short-range implementation. The intended use of 10BASE-T1S is to replace existing bus architectures that often result in "communication islands," such as CAN, CAN FD, LIN, and RS-485.

Settings:

10BASE-T1S Settings

Channel

Data: A0

Option

☐ Show Sync Code ☐ Hide BEACON ☐ FCS in Byte Order

☐ Display 5B Code ☐ Show MAC for Each Row

☒ Show MAC Data

Transport Layer Data

☐ Data Filter: 20 bytes

Report Data: 8 Byte

Color

SYNC_COMMIT: Preamble/SFD

SSD: MAC Data

BEACON

ESDHB

ESDBRS

ESDJAB

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Show Sync Code: Show Commit, SSD in report; enabled when checked.

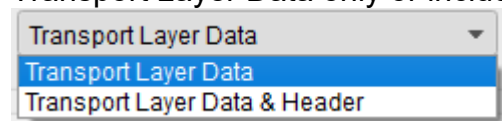
Hide BEACON: Hide Beacon data is not shown; enabled when checked.

FCS in Byte order: Present FCS in report in byte order; enabled when checked.

Display 5B Code: Show special code value

Show MAC Data: Show MAC Packet.

In IPv4(0800h), there will be 20bytes header. The Data column is able to show Transport Layer Data only or including the header.



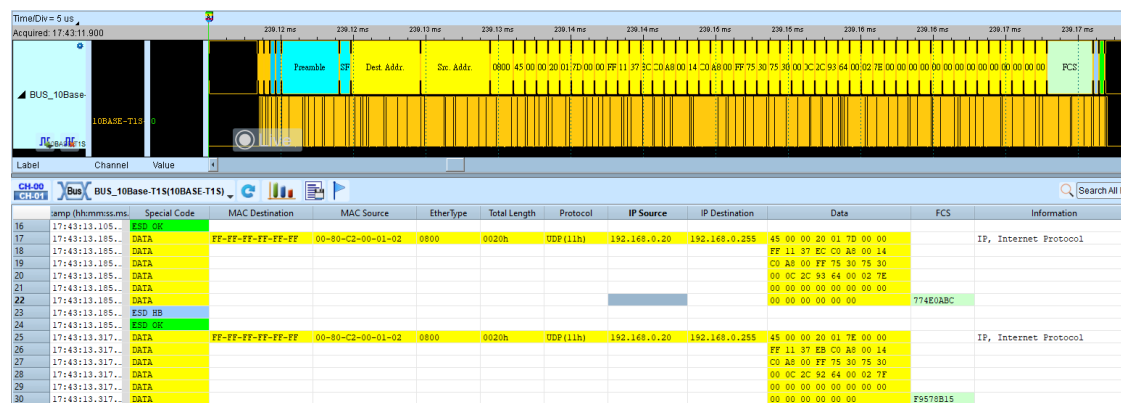
Transport Layer Data:

Total Length	Protocol	IP Source	IP Destination	Data
0020h	UDP (11h)	192.168.0.20	192.168.0.255	75 30 75 30 00 0C 2C 93 64 00 02 7E 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Transport Layer Data & Header:

Total Length	Protocol	IP Source	IP Destination	Data
0020h	UDP (11h)	192.168.0.20	192.168.0.255	45 00 00 20 01 7B 00 00 FF 11 37 EE C0 A8 00 14 C0 A8 00 FF 75 30 75 30 00 0C 2C 95 64 00 02 7C 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Results:



3-Wire

3-Wire protocol is established by HOLTEK SEMICONDUCTOR INC. It's Applied to control LED/LCD driver IC or EEPROM.

Settings

3-Wire(HOLTEK) Settings

Parameters

Channel

CS: A0

WR: A1

☒ RD: A3

DATA: A2

Application

☒ LED Drive IC

☐ LCD Drive IC

☐ EEPROM

HT 1620x

HT93LC46

x8

Color

OPERATION: [Blue]

ADDRESS: [Cyan]

COMMAND: [Green]

DATA: [Yellow]

START: [Purple]

Latch

Chip Select Edge

☐ Active High ☒ Active Low

Data Edge

☒ Rising ☐ Falling

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Show the selected channels (CS:CH0, WR:CH1, DATA:CH2, RD:CH3)

LED Driver IC: Select LED driver IC application.

LCD Driver ID: Select LCD driver IC application.

EEPROM: Select EEPROM application.

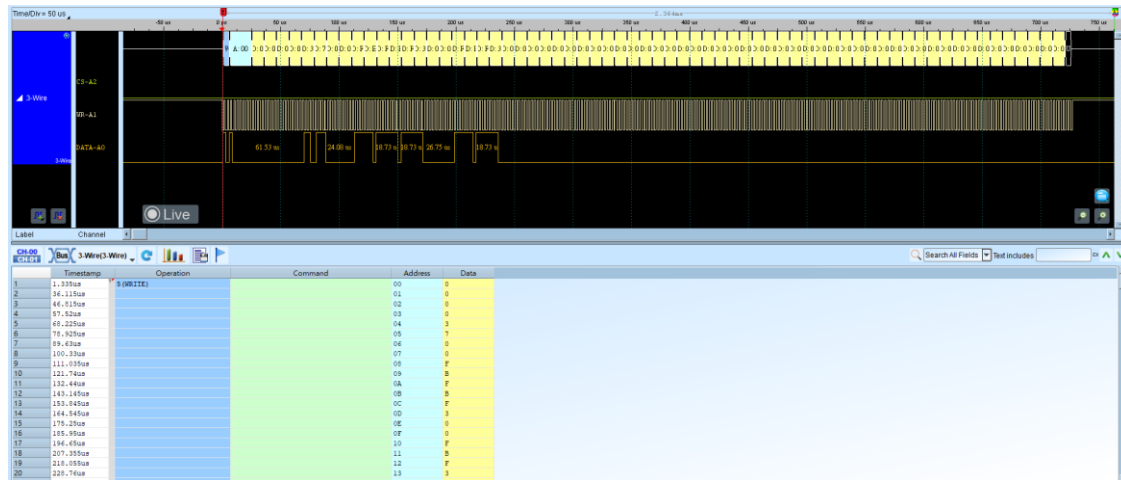
Active High: Select Active High.

Active Low: Select low chip select (CS).

Rising: Select Rising Data Edge.

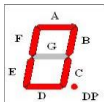
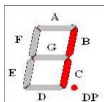
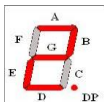
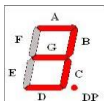
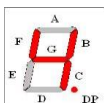
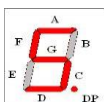
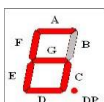
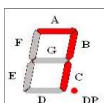
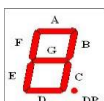
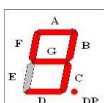
Falling: Select Falling Data Edge.

Result

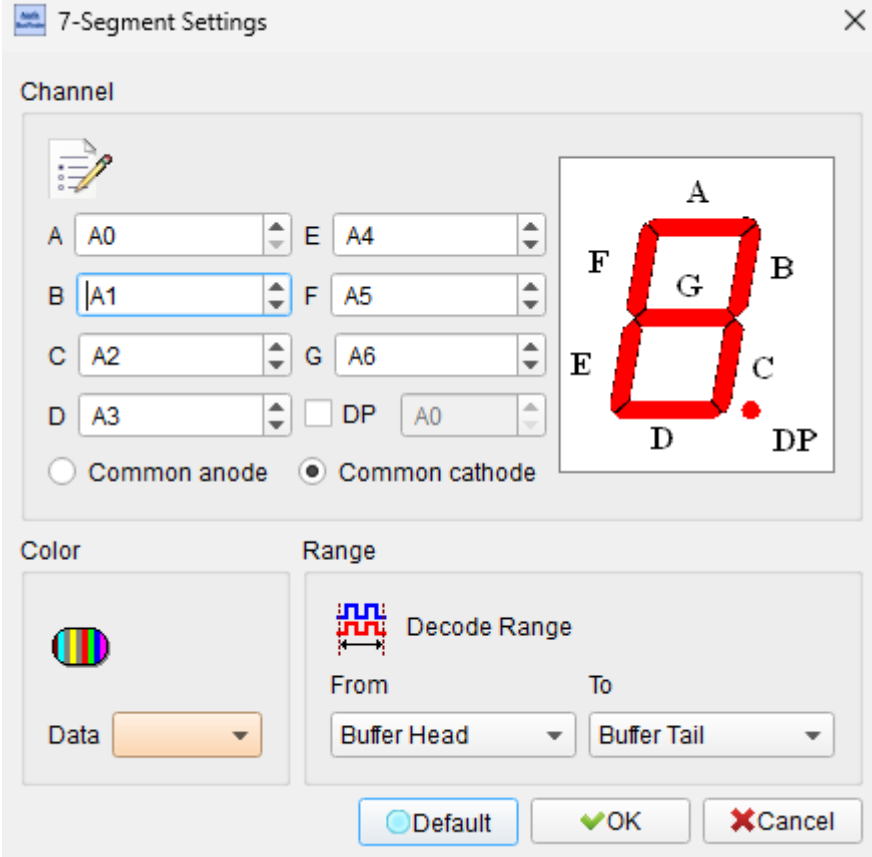


7-Segment

A seven-segment display, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.

Digit	LED	A	B	C	D	E	F	G
0		ON	ON	ON	ON	ON	ON	OFF
1		OFF	ON	ON	OFF	OFF	OFF	OFF
2		ON	ON	OFF	ON	ON	OFF	ON
3		ON	ON	ON	ON	OFF	OFF	ON
4		OFF	ON	ON	OFF	OFF	ON	ON
5		ON	OFF	ON	ON	OFF	ON	ON
6		ON	OFF	ON	ON	ON	ON	ON
7		ON	ON	ON	OFF	OFF	OFF	OFF
8		ON	ON	ON	ON	ON	ON	ON
9		ON	ON	ON	ON	OFF	ON	ON

Settings



7-Segment Settings

Channel

A A0 E A4

B A1 F A5

C A2 G A6

D A3 DP A0

☐ Common anode ☒ Common cathode

Color

Data

Range

Decode Range

From To

Buffer Head Buffer Tail

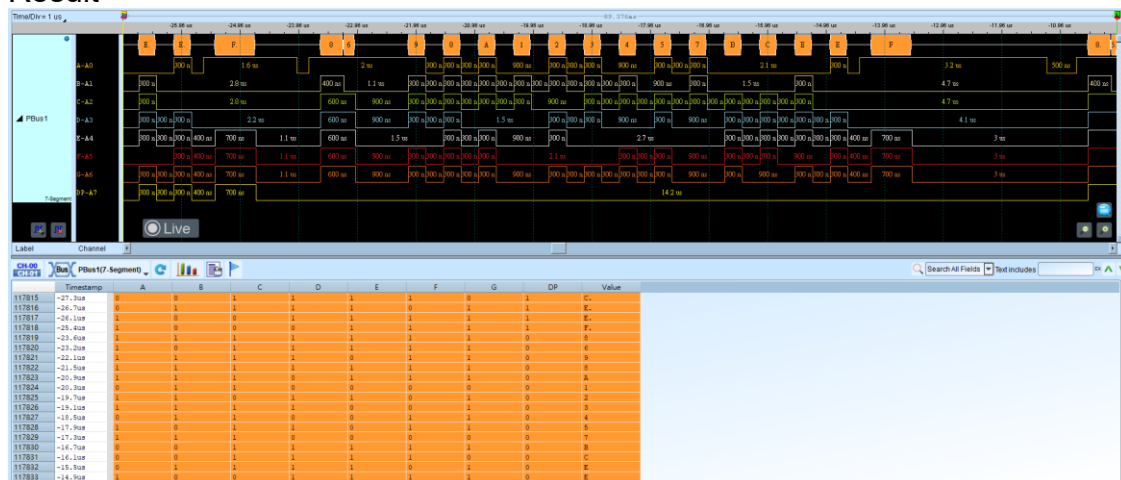
The dialog box shows settings for a 7-segment display. The Channel section has dropdowns for segments A through G and a DP (decimal point) setting. The Common cathode option is selected. The Color section has a Data dropdown. The Range section has a Decode Range dropdown and From/To dropdowns for Buffer Head and Buffer Tail. Buttons for Default, OK, and Cancel are at the bottom.

Channel: Show the selected channel (CH 0).

DP: to analysis decimal point.

Common cathode/anode: Show the same cathode or anode.

Result



8b10b Decoding

8b/10b encoding is a coding technique commonly used in high-speed digital communications to convert every 8 bits of data into a 10 bits format. It was first invented by IBM in the 1980s to improve the reliability and stability of data transmission.

Setting

Data Channel: Set the signal on the DUT to the channel number of the logic analyzer.

(LVDS signals need to be converted into single-ended signals or use LVDS probes)

Data Rate: User can set the data rate manually, or choose the 'Auto', let software calculate the data rate automatically.

Option:

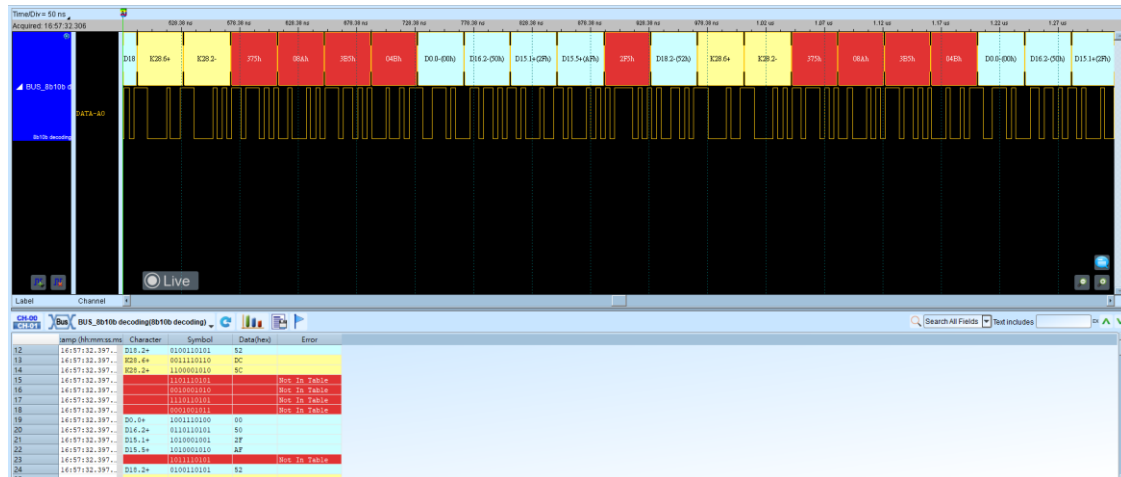
Invert Value: Invert the waveform.

Little Endian: The data would be sorted follow Little Endian when

checked.

Sync Symbol: Choose which k-code for syncing.

Result



A/D Converter

A/D Converter (Analog-To-Digital Converter), is a device that uses sampling to convert a continuous quantity to a discrete time representation in digital form.

Settings

Data Channel Start From: ADC data channel start from

CLK Channel: CLK IN channel of ADC, enable CLK channel and Data Edge option when checked.

CS(OE) Channel: Chip Select channel of ADC, enable CS channel and Chip Select Edge option when checked.

Data Width: ADC data width, range: 4Bit ~ 32Bit

MSB First: Data bit starts form MSB; LSB defaulted

Chip Select Edge: Set the chip select edge; Active Low defaulted

Data Edge: Set the Data Edge; Falling Edge defaulted

Curve: Time(X)-Data(Y) Show the diagram in form of time as X axis; data as Y axis.

Ramp/Step Function: Select Ramp/Step curve, Ramp Function defaulted

Color: Select the curve color

Bound Value Range:

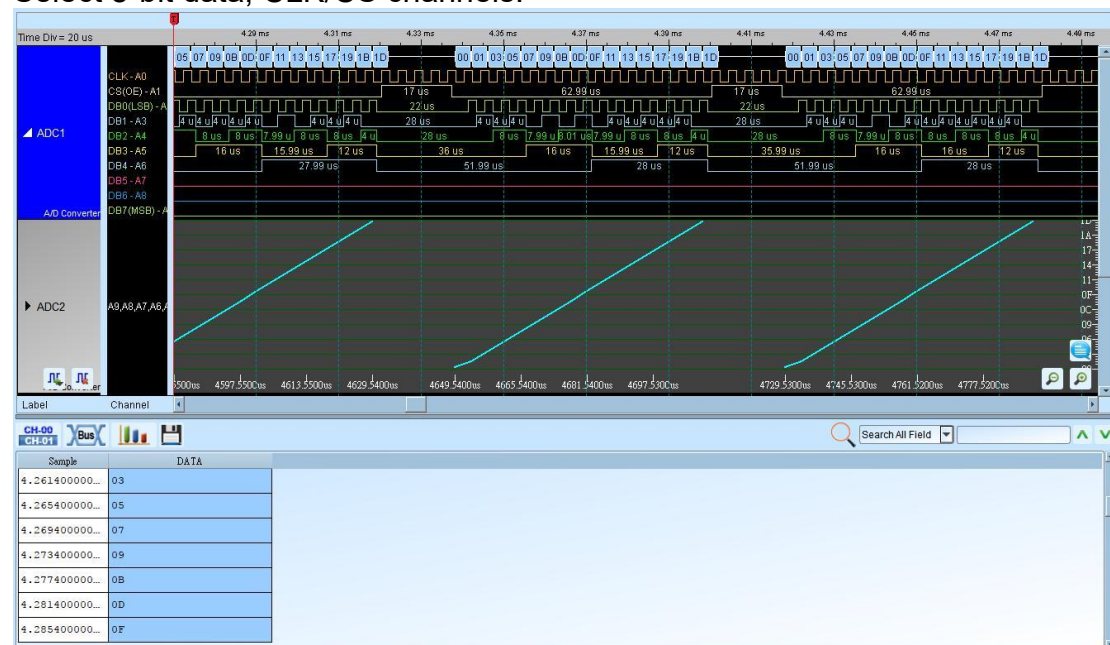
Default: The maximum value that can be represented using the data width is the upper bound.

Use the maximum and minimum as the bound of Y axis: Use the maximum data as the top bound of Y axis and minimum data as the bottom bound of Y axis.

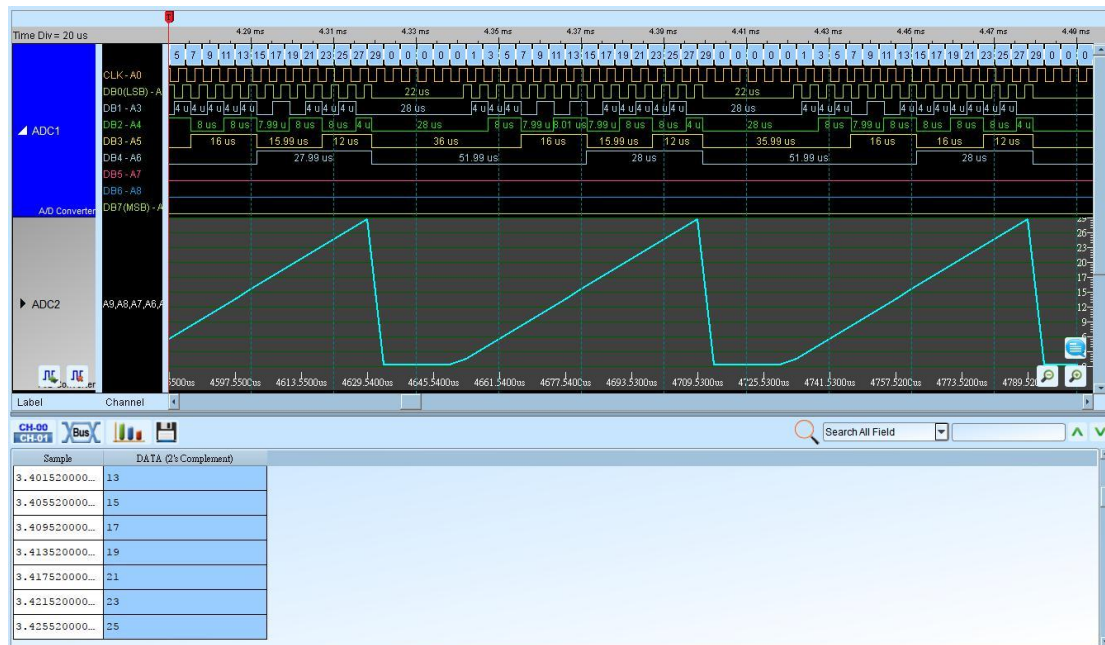
Insert Y axis bound: Set the maximum and minimum bounds of Y axis.

Result

Select 8-bit data, CLK/CS channels:



Select 8-bit data, CLK:



Accelerometer

Accelerometer (AccMeter) decoder is the SPI interfaced accelerometer data decoder, which provides bus value to acceleration value conversion and curve drawing function.

Settings

AccMeter Settings

Parameter Settings

Channels Settings

CS: A0
CLK: A1
SDI: A2
SDO: A3

Edge Select

CS: Activate Low
SDI: Rising
SDO: Rising

Model: AIS326DQ

Initial Full-Scale: 2 G

Delay Settings

☐ Plot Time (X) - Data (Y) ☐ X ☐ Y ☐ Z

☐ Advanced Decode

☐ Calculate Average: (N - 0) to (N + 0)

Color

R / W: M / S:

Address: Data:

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel Setting:

CS: Chip Select, must specified the active state of the CS pin.

CLK: Clock

SDI: Data Input Pin, must specified the data sampling edge.

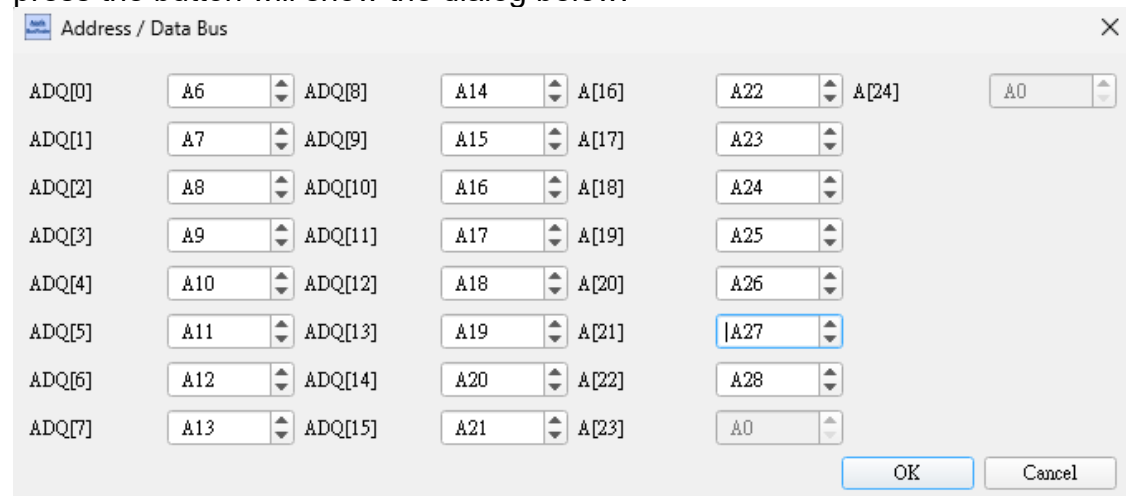
AD-Mux Flash

AD-Mux Flash is one kind of parallel flash that utilize an Address and Data multiplexed interface.

Settings

Amax: Setting the number of address pin.

Quick Setup/User Defined: Only set ADQ[0](LSB) when select the Quick Setup, other channels will be set automatically. When check User Defined and press the button will show the dialog below:



The dialog box titled "Address / Data Bus" contains a grid of address pins and their values. The pins are arranged in two columns: ADQ[0] to ADQ[7] on the left and ADQ[8] to ADQ[15] on the right. Each pin has a corresponding value field. The values range from A6 to A28, with A0 appearing in the top right and bottom right fields. The A27 field is highlighted with a blue border. At the bottom right, there are "OK" and "Cancel" buttons.

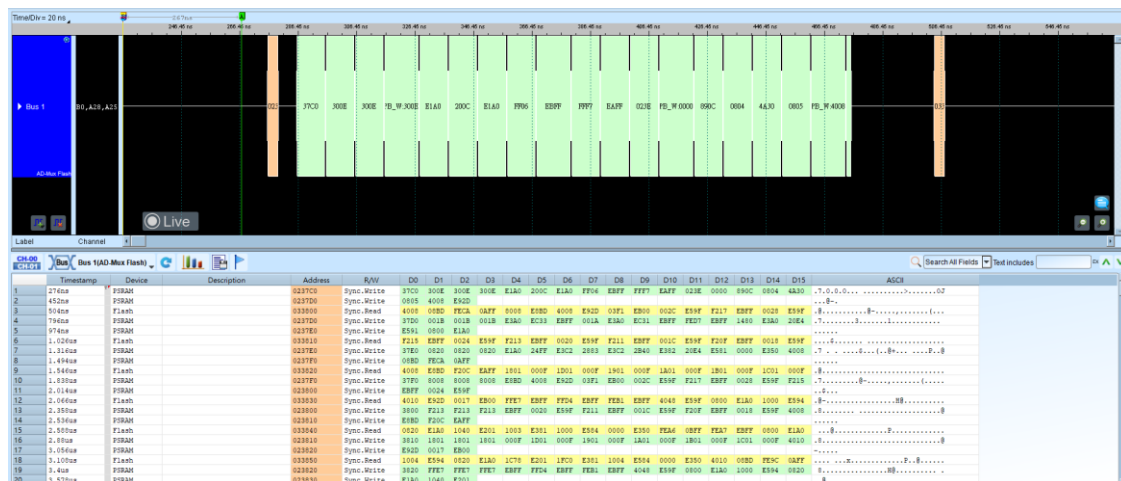
Pin	Value	Pin	Value
ADQ[0]	A6	ADQ[8]	A14
ADQ[1]	A7	ADQ[9]	A15
ADQ[2]	A8	ADQ[10]	A16
ADQ[3]	A9	ADQ[11]	A17
ADQ[4]	A10	ADQ[12]	A18
ADQ[5]	A11	ADQ[13]	A19
ADQ[6]	A12	ADQ[14]	A20
ADQ[7]	A13	ADQ[15]	A21

Flash: Control pins of flash.

PSRAM: Control pins of PSRAM. Some MCP include Flash and PSRAM in one package. It will decode PSRAM at the same time when "has PSRAM" is checked.

Configuration: The default setting of configuration register. User must set here to make a correct analysis.

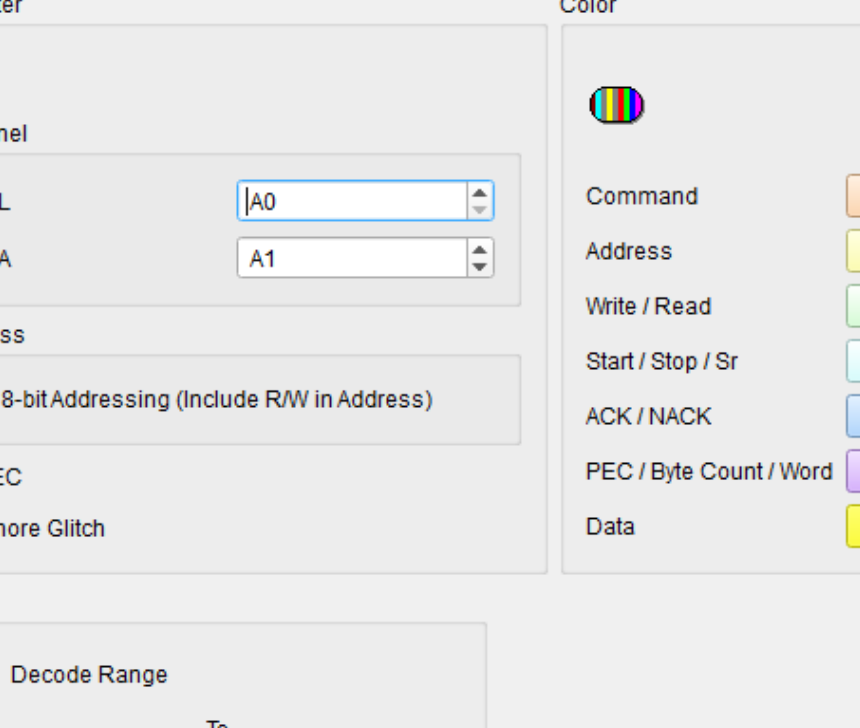
Result



APML

APML protocol is established by AMD for it's Opteron CPU platform.

Settings



Settings

APML Rev. 1.06 Settings

Parameter

Channel

SCL A0

SDA A1

Address

☐ 8-bit Addressing (Include R/W in Address)

☐ PEC

☐ Ignore Glitch

Color

Command

Address

Write / Read

Start / Stop / Sr

ACK / NACK

PEC / Byte Count / Word

Data

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

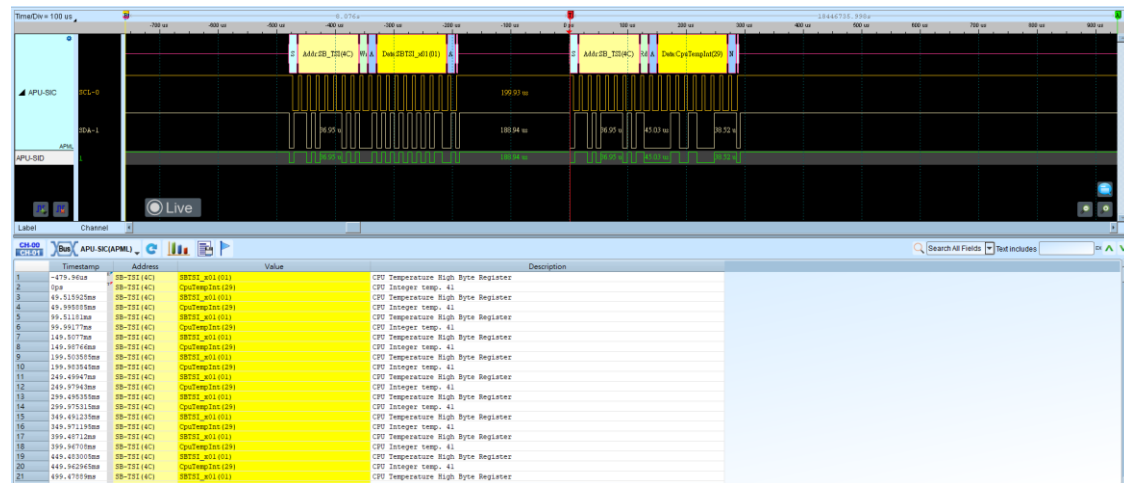
8-bit addressing (Include R/W in Address): Show 8-bit addressing (include

7-bit addressing and 1-bit R/W). Enable when checked.

PEC: Packet Error Check. Enable when checked.

Ignore glitch: Ignore the glitch when the slow transitions. Enable when checked.

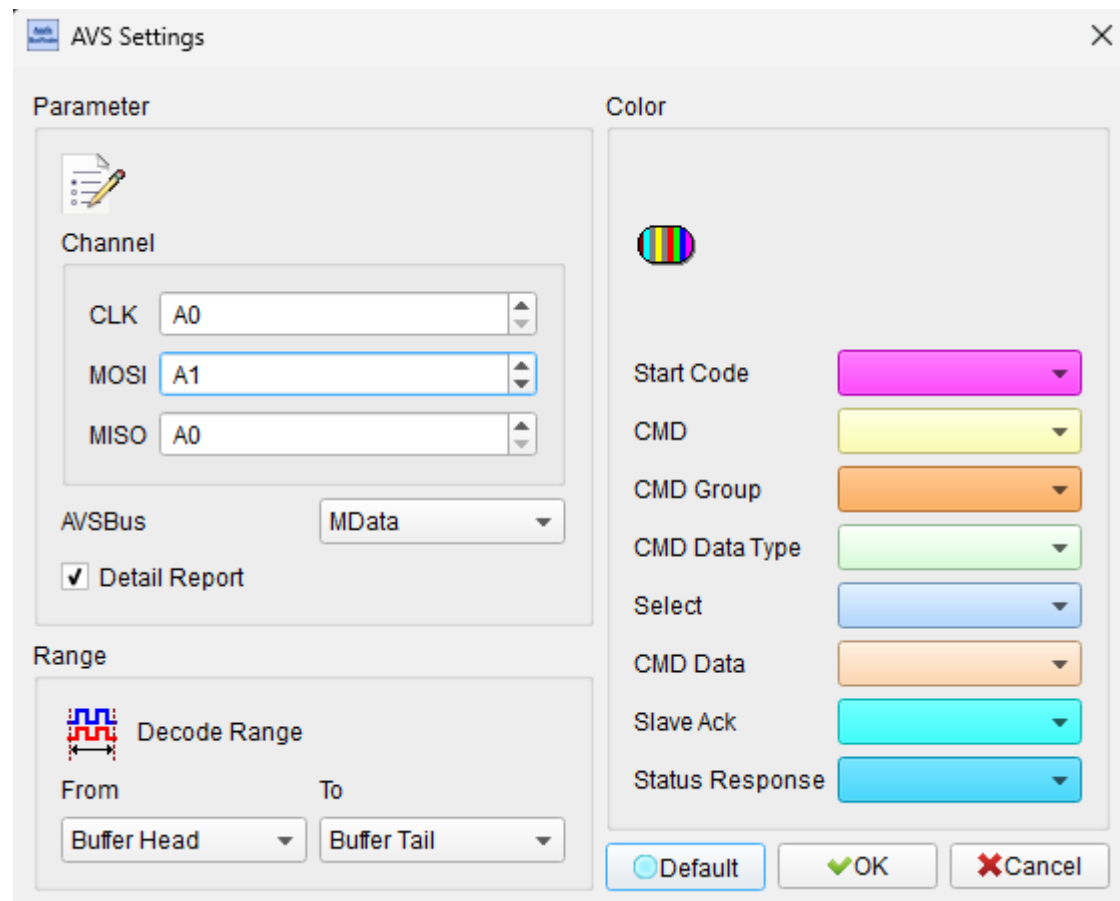
Result



AVSBus

AVS stands for Audio-Visual Coding Standard, which is a video and audio coding standard used to compress, transmit and decode digital video and audio data.

Settings

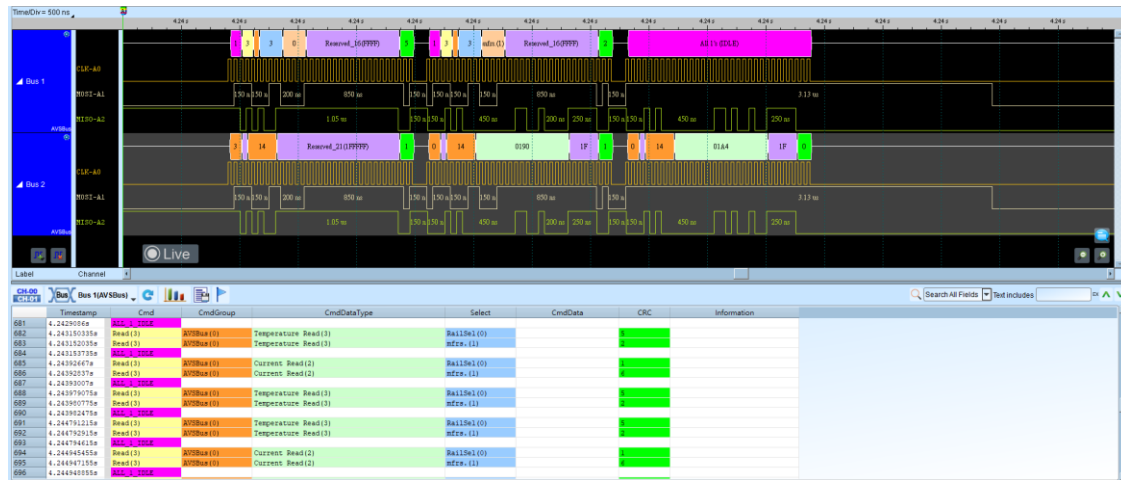


Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

AVSBus: Set the decoded data type to SData or MData.

Detail Report: Show details in report area, enabled when checked.

Result



BiSS-C

BiSS-C (Bidirectional Synchronous Serial C-mode) designed by Ic-Haus. The BiSS Interface is based on a protocol which implements a real time interface. It enables a digital, serial and secure communication between controller, sensor and actuator. It is used in industrial applications which require transfer rates, safety, flexibility and a minimized implementation effort.

Settings

BiSS-C Rev.C6 Settings

Channel

MA: A0 SLO: A1

Type of Data: Single Cycle Data

Serial Data Length (bits): 12 (Range: 1 ~ 64)

Data Channel: 1

SLO Phase: 0 samples

Range

Decode Range

From: Buffer Head To: Buffer Tail

Color

Ack / ADR: [Orange]

Start: [Orange]

CDS / CTS: [Yellow]

Data / Cmd: [Green]

Flag / IDL / ID: [Cyan]

CRC: [Blue]

Stop / Ex: [Purple]

Read / IDS: [White]

Write / IDA: [Magenta]

[Default] [OK] [Cancel]

MA/SLO: Setting the channel of MA and SLO.

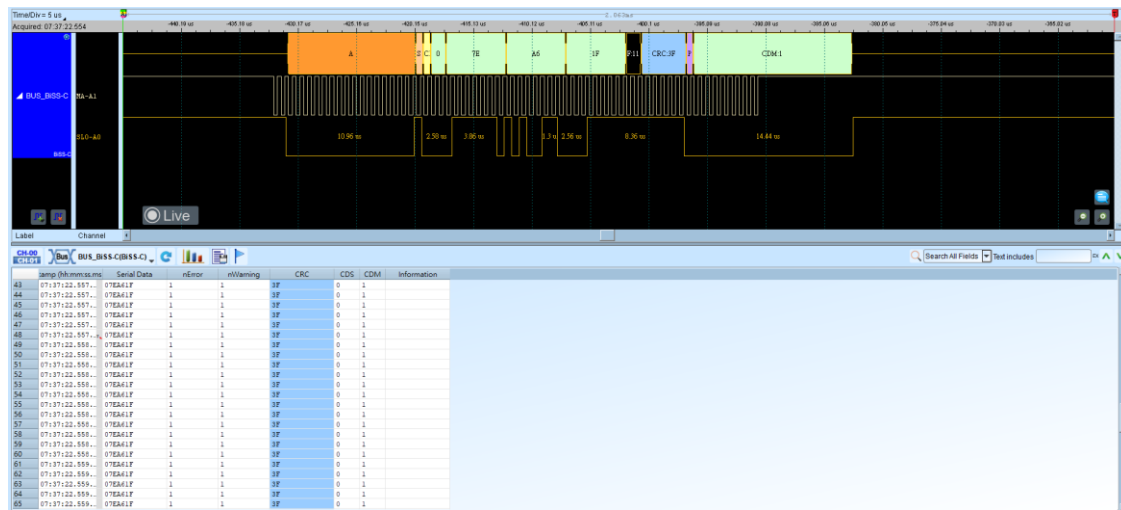
Type of data: Setting the type you want to decode. It include “Register Data-CDM”, “Register Data-CDS”, “Single Cycle Data”.

Serial data length(bits): Setting the data length when Single Cycle Data mode.

Data Channel: Startup setting, users need to provide the number of slaves as the base information for decoding.

SLO Phase: Sets the delay phase of the SLO.

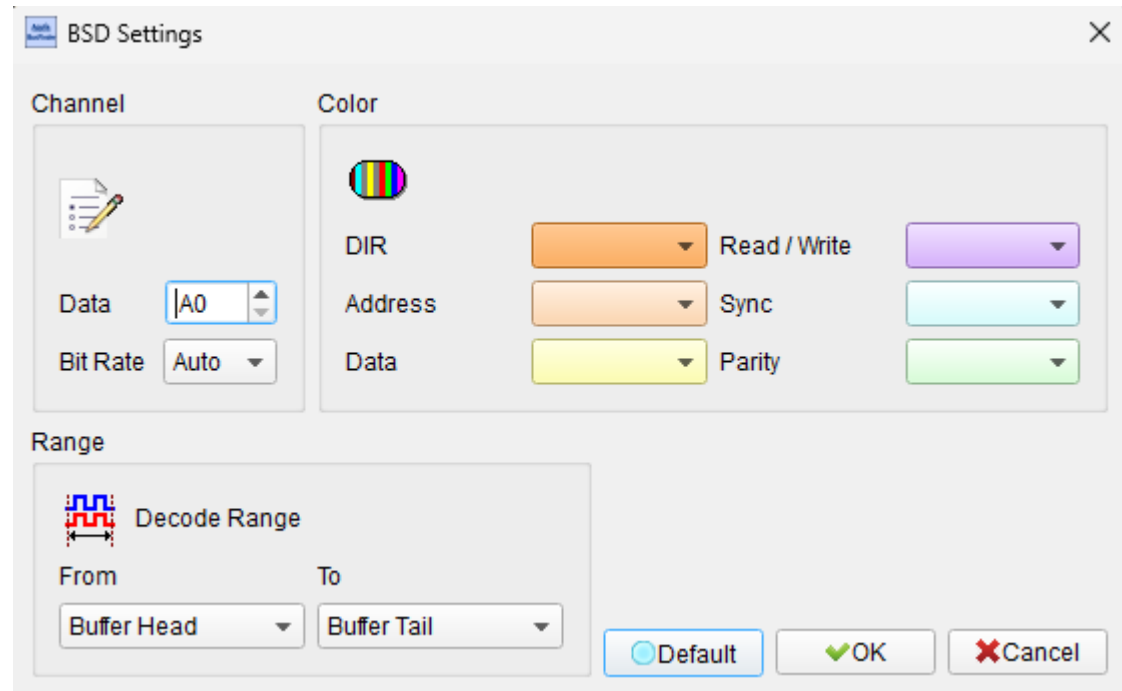
Result



BSD

BSD(Bit Serial Device) is a serial communications protocol for battery monitoring in automotive application.

Settings



The BSD Settings dialog box is used to configure the communication parameters for the Bit Serial Device. It includes sections for Channel, Color, Range, and buttons for Default, OK, and Cancel.

Channel

- Data: A0
- Bit Rate: Auto

Color

- DIR: Read / Write
- Address: Sync
- Data: Parity

Range

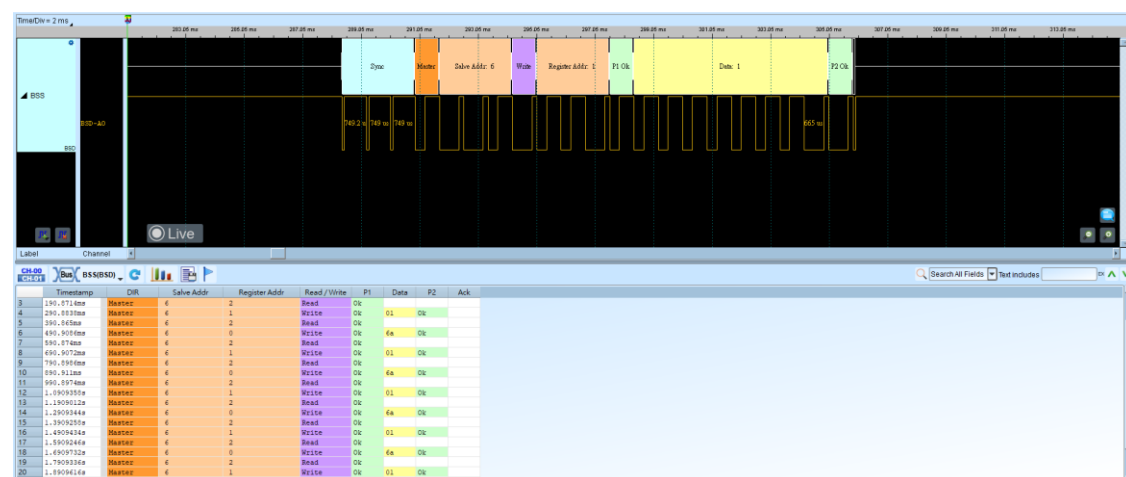
- Decode Range: From Buffer Head To Buffer Tail

Buttons: Default, OK, Cancel

Data: The BSD data.

Bit rate: The bit rate of the BSD data

Result



BSS

Bit Synchronous Single-wire interface (BSS), direct link with the onboard Engine Control Unit (ECU). Aim of the BSS is real time control (through digital protocol) of main electrical parameters, such as voltage regulation and load response timing.

Settings

BSS Settings

Channel

Channel: CH 0

☐ Detail Report

Startup Setting

Time Scale Select: 0

Color

Direction: [Orange] Read: [Blue]

Address: [Cyan] Write: [Purple]

Register: [Green] Data: [Yellow]

ChipSet

STL9910

Range

Decode Range

From: Buffer Head To: Buffer Tail

☐ Default

OK Cancel

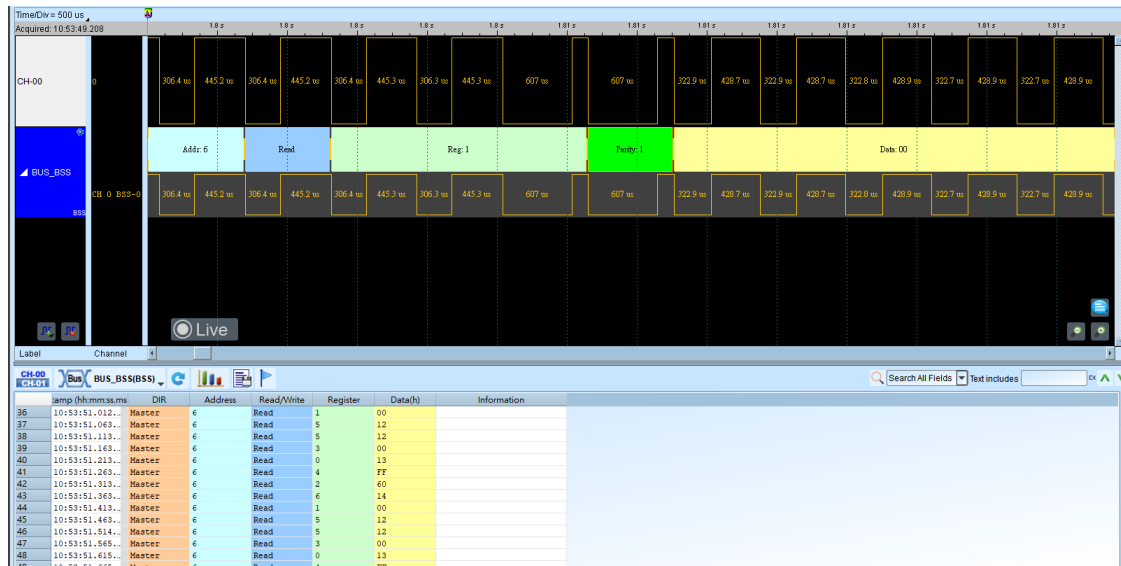
Channel: Set the signal channel of BSS.

Detail Report: Detailed analysis of the byte content. Enable when checked.

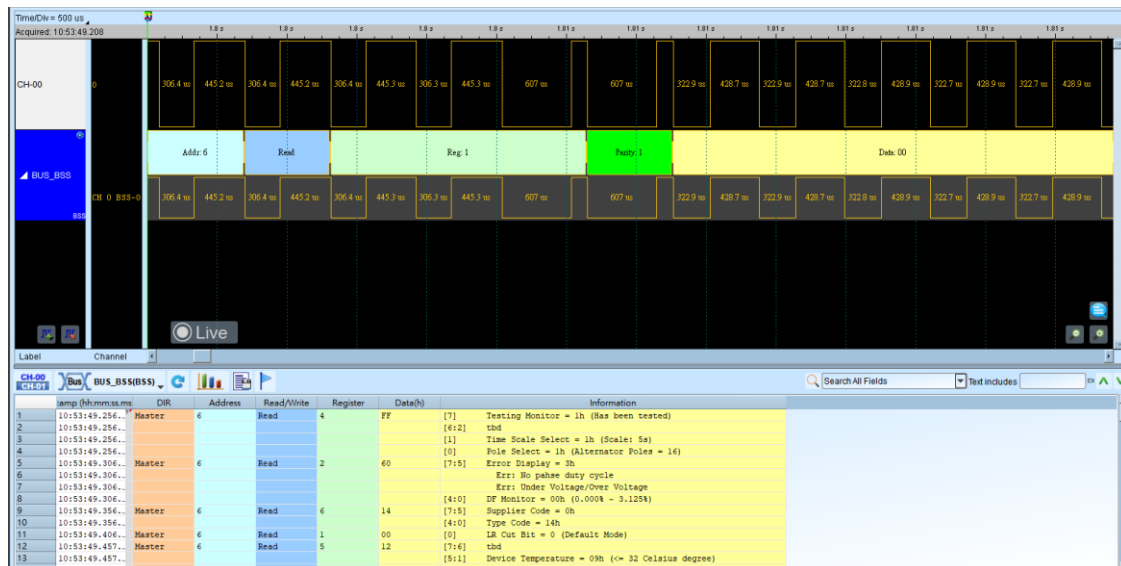
Startup Setting: Set the value of the Time Scale Select Bit

ChipSet: Set the Chipset that are going to be analyzed.

Result



Detail Report



BT1120

Digital interfaces for HDTV studio signals

The BT1120 is used for bit serial port transmission of HDTV signals. It mainly provides image format parameters and data transmission signals for HDTV production and international program exchange, and is backward compatible with old image frequencies of 60, 50, 30, 25 24Hz (progressive, interlaced, frame segmentation), total line number 1125, valid line number 1080 to cover both commercial and developing products. This interface will include all equipment necessary for broadcast and industrial applications.

Settings

BT1120 Settings

Parameter

Channel

CLK |A0|

Data 0 |A1| ☒ Quick Setting

Data 1 |A2|

Data 2 |A3|

Data 3 |A4|

Data 4 |A5|

Data 5 |A6|

Data 6 |A7|

Data 7 |A8|

Stream |Y Stream|

Color

SAV

YA/CA

YD/CRD

CBD

YCR/CCR

LN

EAV

Range

Decode Range

From To

|Buffer Head| |Buffer Tail|

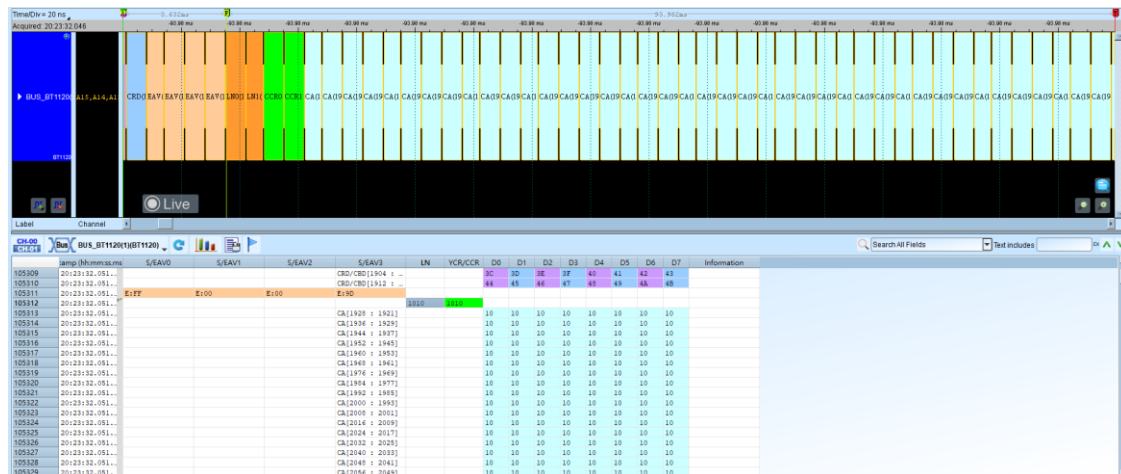
☐ Default ☒ OK ☒ Cancel

Channel setting: Set the object to be tested, CLK, each Data 0-7, the channel number connected to the logic analyzer,

Quick Setting: the Data channel setting will be automatically incremented.

Stream: Y, CB/CR stream

Result



CAN 2.0B/ CAN FD

The Controller Area Network (CAN) protocol has version 2.0A (Basic CAN, 11 bits) and version 2.0B (Extended CAN or Peli CAN, 29 bits); both versions have four message types: Data Frame, Remote Frame, Error Frame and Overload Frame as the diagrams below. The CAN Bus has two kinds of data output: CAN High (CAN_H) and CAN Low (CAN_L).

The data rate is flexible in CAN FD (CAN with Flexible Data-Rate). When CAN FD is transferring, it is 64 (bytes/per data) and including CRC17/CRC21.

Settings

Setting

Channel: CAN_L(Rx) CAN_L: A0

Color

Start of Frame	[Orange]	RTR bit	[White]
Identifier	[Light Orange]	SRR bit	[Pink]
Data length code	[Yellow]	IDE bit	[Gold]
Data	[Light Green]	Reserved bit	[Yellow]
CRC	[Light Blue]	Delimiter bit	[Green]
ACK Slot	[Blue]	Error Frame	[Cyan]
End of Frame	[Purple]	Error State	[Red]

Range

Decode Range: From [Buffer Head] To [Buffer Tail]

[Default] [OK] [Cancel]

Channel Settings:

CAN_H/CAN_L(RX): Can directly measure the stabilized physical layer or the

logic signal converted by the transceiver, the best signal to measure is the logic signal Rx.

Auto Detect Data Rate:

- I. When checked, the program assists in calculating the data rate.
- II. When unchecked, user can choose the built-in Data Rate setting or input Data Rate by yourself.
- III. The allowable input data rate range is 5Kbps-1Mbps.
- IV. If CAN FD function is checked, this function will be disabled automatically because the Data Rate will be changed.

Show Scale in Waveform: When the box is checked, a scale point is displayed on the top of the waveform, which is convenient to check the bit cutting status. This function is not available if CAN FD is checked.

CAN FD Setting:

ISO CRC/Non ISO CRC: User can adjust the rules of ISO CRC analysis and calculation.

Data Only:

- I. When checked, this function enables you to set the amount of data to be displayed in the analysis report, which can be set from 8 bytes to 60 bytes, and the data outside the set range will be deleted and not be displayed in the report, which is convenient for you to use when you view the report quickly.
- II. When unchecked, all Data will be displayed.

Report Format: Check this box to set the width of the data fields to be displayed in the analysis report, which can be set to 8, 16, or 32 bytes. 8 bytes will be displayed when the box is unchecked, and the following is an example of the application:

Data field width set to 8 bytes.

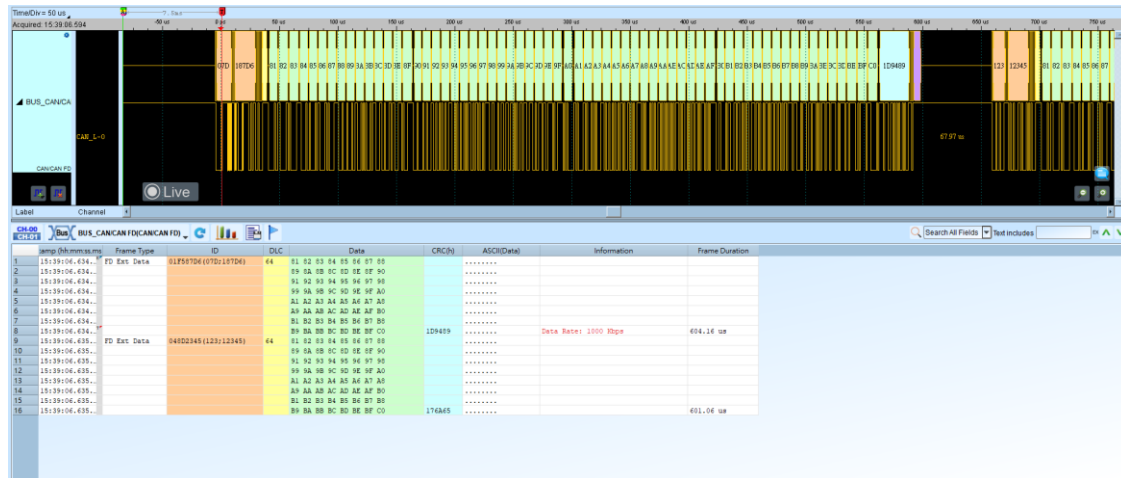
Frame Type	ID	DLC	Data	CRC(h)
FD Ext Data	01F587D6 (07D;187...	64	81 82 83 84 85 86 87 88	
			89 8A 8B 8C 8D 8E 8F 90	
			91 92 93 94 95 96 97 98	
			99 9A 9B 9C 9D 9E 9F A0	

Data field width is set to 16 bytes.

Frame Type	ID	DLC	Data
FD Ext Data	01F587D6 (07D;187...	64	81 82 83 84 85 86 87 88 89 8A 8B 8C 8D 8E 8F 90
			91 92 93 94 95 96 97 98 99 9A 9B 9C 9D 9E 9F A0
			A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD AE AF B0

Result

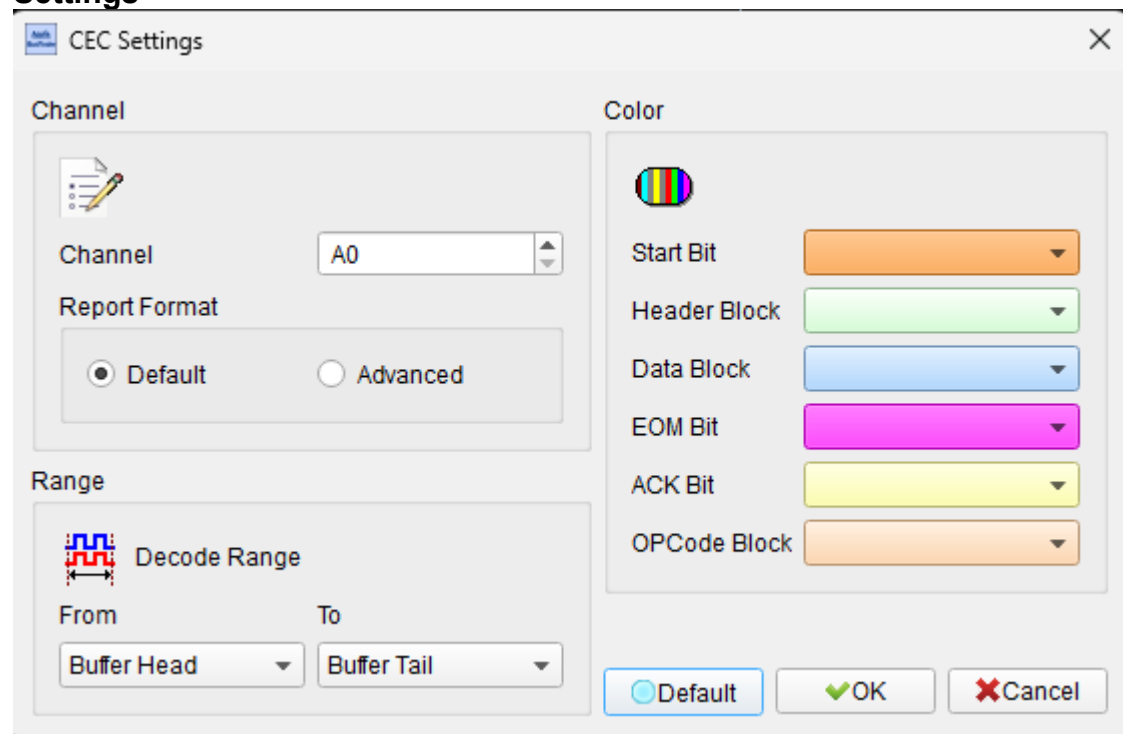
Use the CAN_L(Rx) signal for analysis.



CEC

Consumer Electronics Control, used for transmitting industrial specification AV Link protocol signals to support a single remote control to operate multiple AV machines, is a single-core, bi-directional serial bus.

Settings

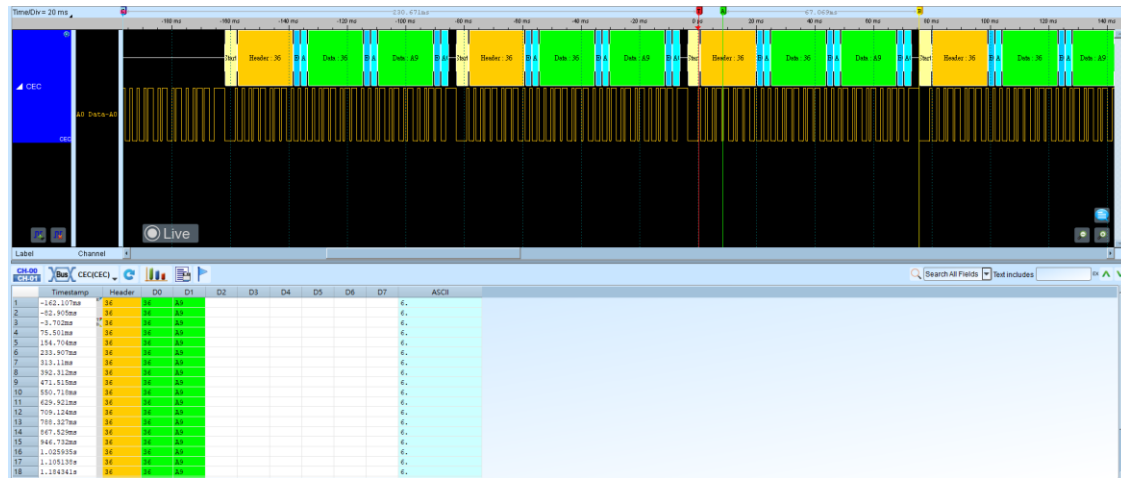


Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

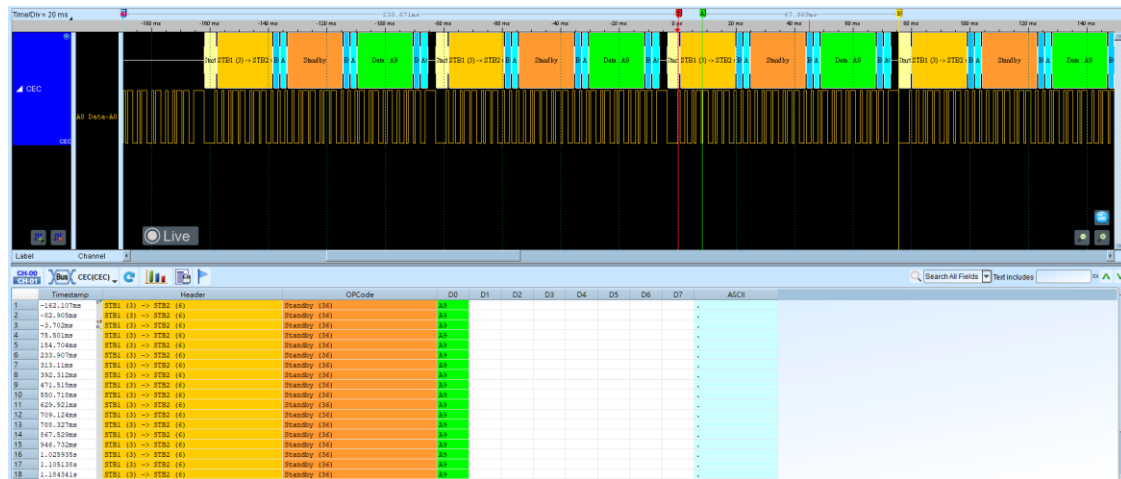
Report Format: There are two types of settings, Advanced and Default. The Advanced mode explains the meaning of the Header and OPCode of the waveform.

Result

Normal



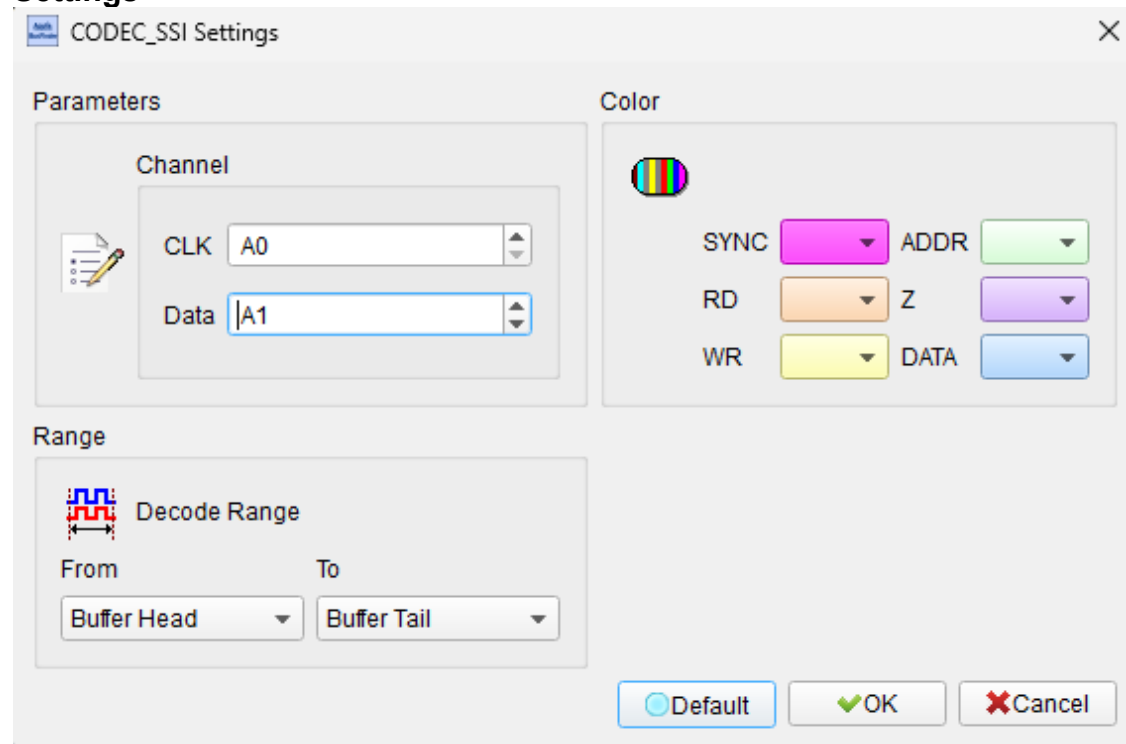
Advanced



Codec SSI

Serial Synchronous Interface (SSI) signal used by the codec (CODEC) inside the phone

Settings



The dialog box is titled "CODEC_SSI Settings" and contains three main sections: Parameters, Color, and Range.

Parameters: A "Channel" section with a notepad icon. It contains two dropdown menus: "CLK" set to "A0" and "Data" set to "A1".

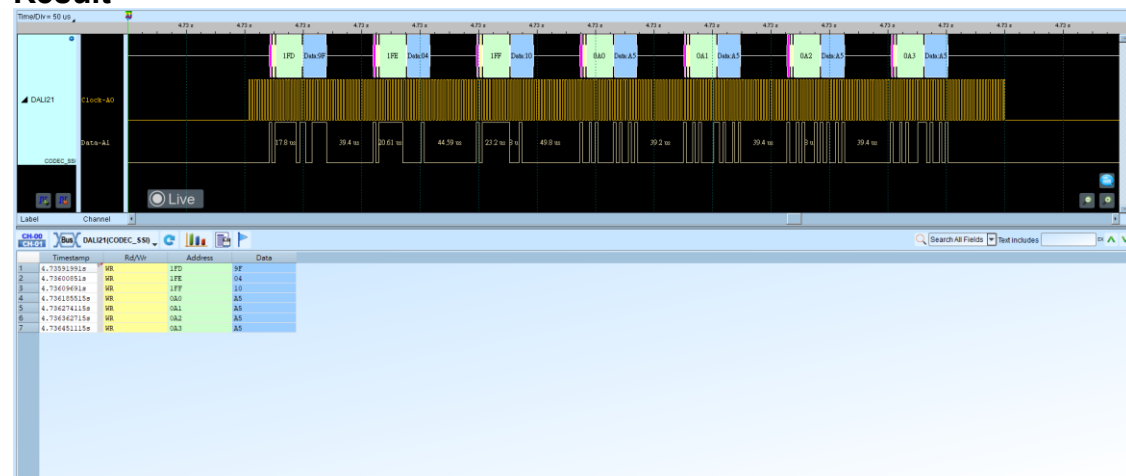
Color: A section with a color wheel icon. It contains six color-coded dropdown menus: "SYNC" (pink), "ADDR" (light green), "RD" (orange), "Z" (purple), "WR" (yellow), and "DATA" (blue).

Range: A section with a waveform icon and the text "Decode Range". It contains two dropdown menus: "From" set to "Buffer Head" and "To" set to "Buffer Tail".

At the bottom right are three buttons: "Default" (with a blue circle icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

Channel: Set the signal on the DUT to the channel number of the logic analyzer.

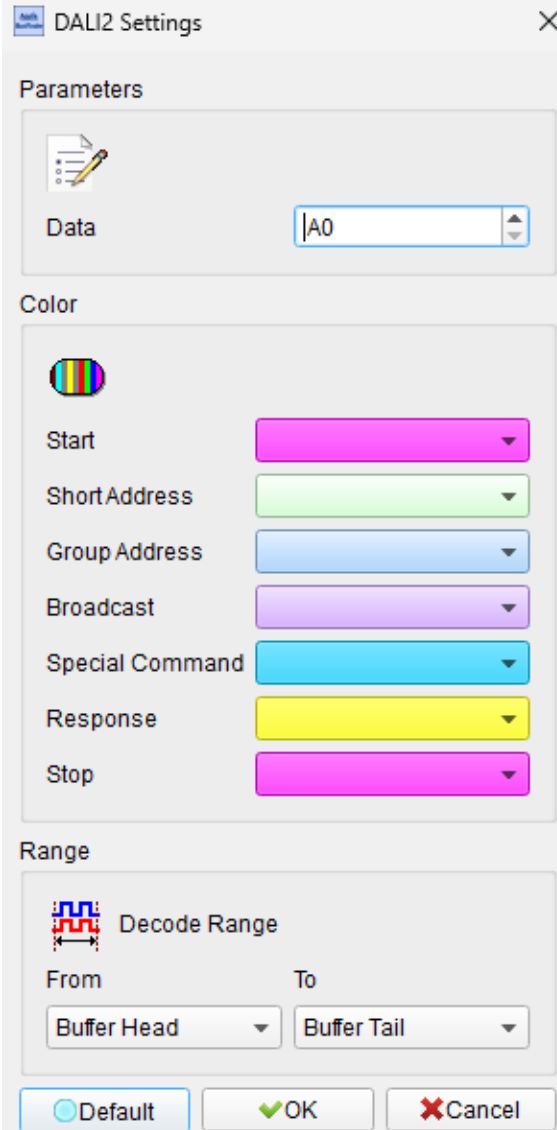
Result



DALI

Digital Addressable Lighting Interface (DALI) is a technical standard for network-based systems that control lighting in buildings. The DALI standard, which is specified in the IEC 60929 standard for fluorescent lamp ballasts, encompasses the communications protocol and electrical interface for lighting control networks.

Settings



The image shows a software dialog box titled "DALI2 Settings". It is divided into three main sections: "Parameters", "Color", and "Range".

- Parameters:** Contains a "Data" field with a dropdown menu currently showing "A0".
- Color:** Features a color selection icon (a circle with vertical rainbow bars) and seven color-coded dropdown menus: "Start" (magenta), "ShortAddress" (light green), "Group Address" (light blue), "Broadcast" (light purple), "Special Command" (cyan), "Response" (yellow), and "Stop" (magenta).
- Range:** Includes a "Decode Range" icon (a red and blue waveform) and two dropdown menus labeled "From" and "To", both of which are set to "Buffer Head" and "Buffer Tail" respectively.

At the bottom of the dialog are three buttons: "Default" (with a blue circle icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

Data Channel: Show the selected channel.

DDC (EDID)

EDID (Extended Display Identification Data) is I2C protocol base on DDC wire and transmitted monitor information. Now, HDMI, DVI and VGA are support this protocol.

Settings

DDC(EDID) Settings

Parameter Setting

Channel Setting


SCL SDA

Address Mode

☒ 7-Bit Addressing
☐ 8-Bit Addressing (Include R/W in address)


☐ Ignore glitch ☐ Statistics Mode

Color



Start Read / Write
 Stop ACK
 Address NACK
 Data

Range

 Decode Range

From To

SCL: CLK of I²C.

SDA: Data of I²C.

Address Mode:

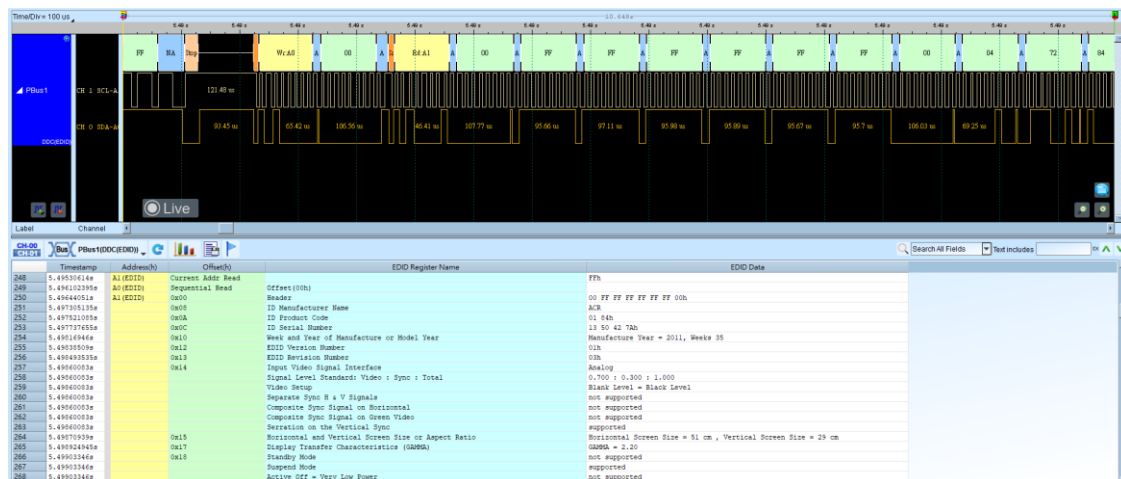
7-bit addressing: Show 7-bit addressing

8-bit addressing(Include R/W in Address): Show 8-bit addressing(include 7-bit addressing and 1-bit Rd/Wr).

Ignore glitch: Ignore the glitches occurred due to the slow transitions.

Statistic Mode: Collect all the data frames into one report by register address order.

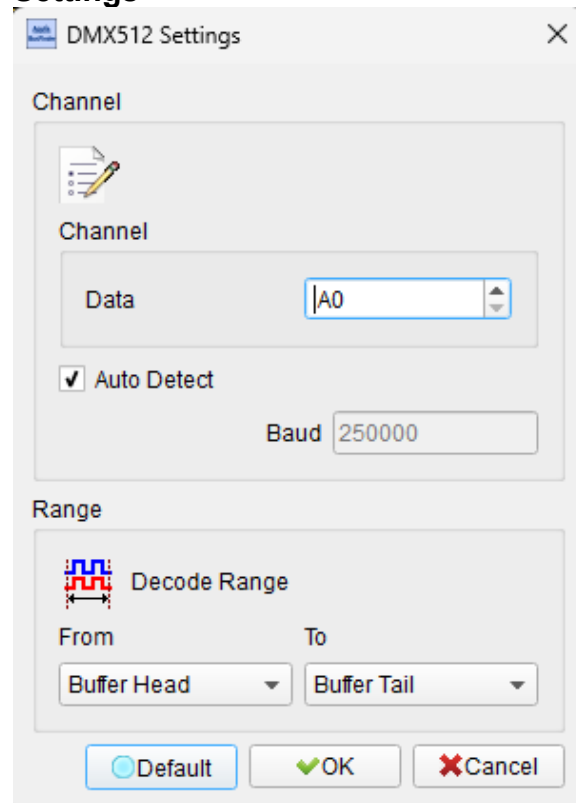
Result



DMX512

DMX512 is a standard for digital communication networks that are commonly used to control stage lighting and effects..

Settings



The DMX512 Settings dialog box contains the following elements:

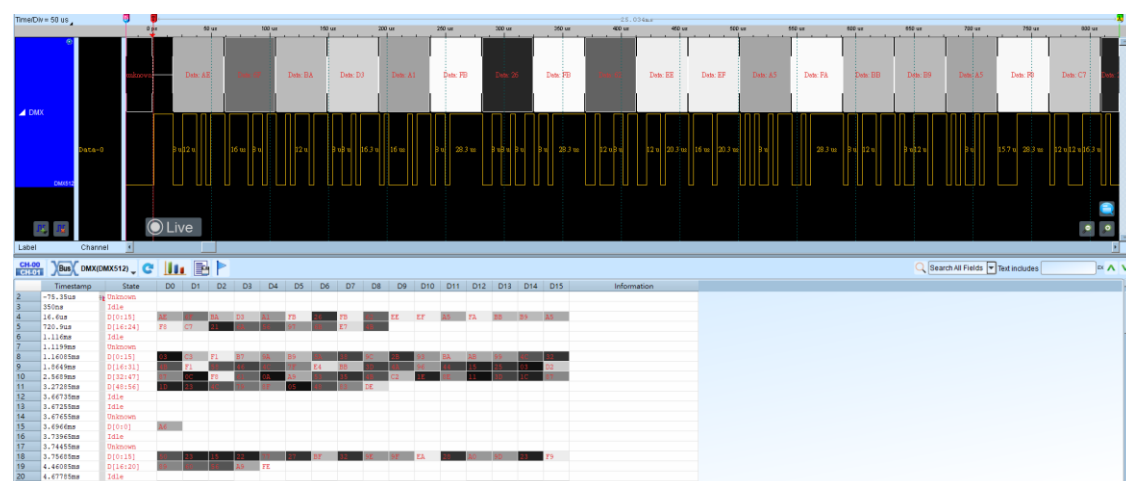
- Channel** section:
 - A 'Channel' label with a pencil icon.
 - A 'Data' dropdown menu currently showing 'A0'.
 - A checked 'Auto Detect' checkbox.
 - A 'Baud' text field set to '250000'.
- Range** section:
 - A 'Decode Range' label with a waveform icon.
 - 'From' and 'To' dropdown menus, both set to 'Buffer Head' and 'Buffer Tail' respectively.
- Buttons at the bottom: 'Default' (with a circular arrow icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

Data: Show the selected channel (CH0).

Auto Detect: Set the Baud Rate manually if not selected.

Result

Use grayscale to display the decode results.



DP Aux Ch

The DP Aux Ch is to detect the link, configuration and status of the Display Port source. The Display Port is the digital display interface that is specified in the VESA standard. (Support DP 2.1, eDP 1.5)

Settings

DP AUX CH Settings

Settings

Channel

Aux: A0

Analysis Mode

Mode: DP_Aux

Aux Option

Startup Transaction: Request

☐ Show DPCD

- ☒ DP Version: 1.4a
- ☐ eDP Version: 1.2
- DPCD 00108h: 8b/10b

☐ Show EDID

Color

Request: [Orange]

Reply: [Orange]

CMD: [Yellow]

Address: [Green]

Data: [Cyan]

Stop: [Blue]

Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Set the channel to decode

Show DPCD: Show the Display Port Configuration data. Enable when checked.

- I. DP Version supported to 2.1
- II. eDP Version supported to 1.5
- III. DPCP 00108h: 8b/10b or 128b/132b encoding options are available.

Mode: Choose the mode DP_Aux / HPD / PWR

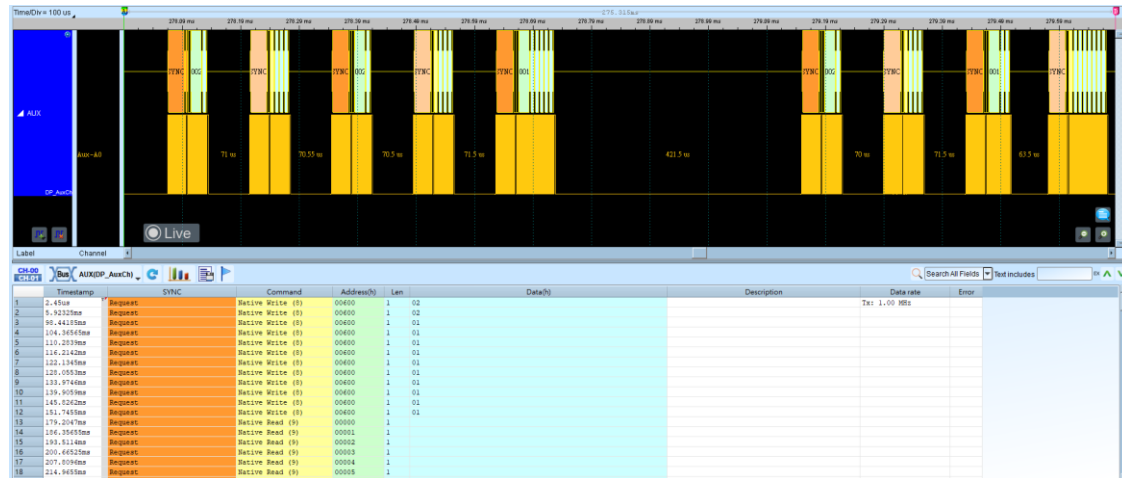
Show EDID: Show the EDID information. Enable when checked.

Startup transaction: Set the transaction type of the first frame

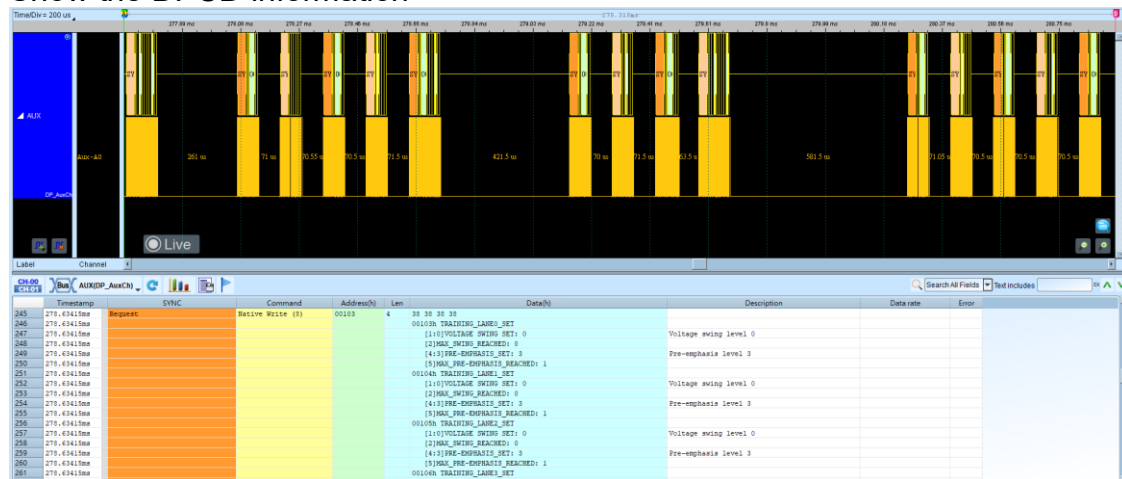
Reply Timeout: Set the value of timeout

Result

Without the DPCD information



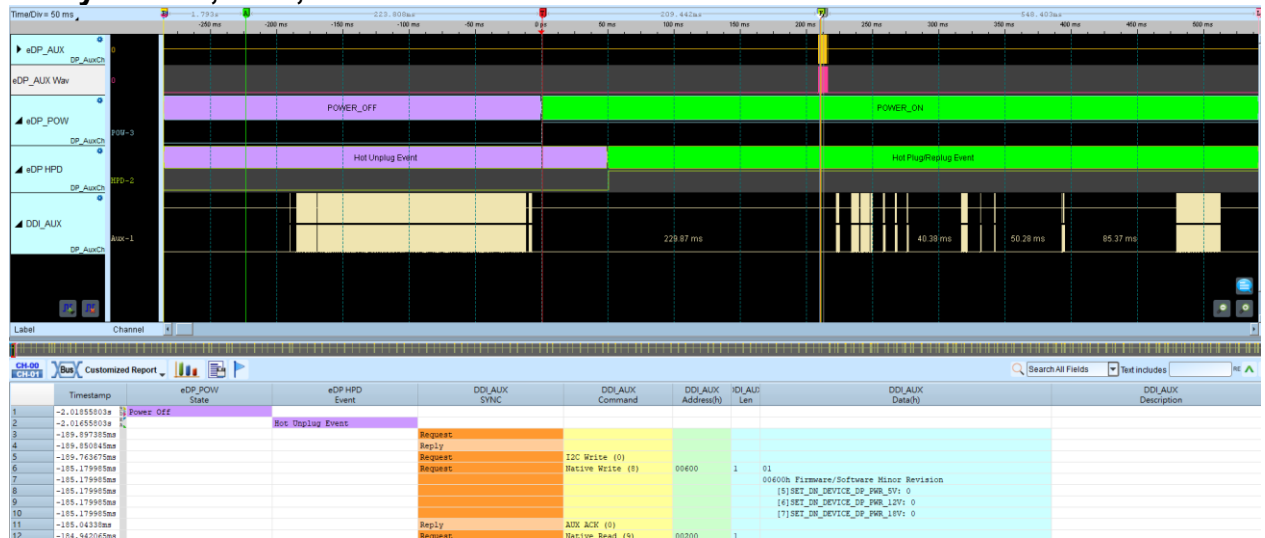
Show the DPCD information



Accessories:

<https://www.acute.com.tw/en/product/detail143>

Analysis Aux, HPD, PWR



eSPI

eSPI is the transmission protocol used in new generation baseboard of Intel, and its specification is to integrate SMBus / LPC / SPI Flash interface to simplify bus and increase transmission efficiency. Source of specification is based on Enhanced Serial Peripheral Interface (eSPI) Interface Base Specification (for Client and Server Platforms) June 2013, Revision 0.75.

Settings

Enhanced SPI (eSPI) Parameter Settings

Channel Settings

CS # SCK

I/O 0 I/O 1

I/O 2 I/O 3

☐ Alert ☐ Reset #

☒ Enable Glitch Filter

CS Work Mode

Response latched on

Startup Settings

I/O Mode Setting

Default Alert Mode

☒ Auto-select protocol timing by clock speed

Command deselect time

Clock LOW to output valid

☒ Pop-up MessageBox when found CRC mismatch(es)!

Advanced Decode Settings

☐ Show RAW Byte Only

☐ Show Configuration Detail

☐ Show Status Bit Def.

☐ Show VWire Detail

☐ Show EC/KBC Command

☐ Show OOB detail

☐ Show RPMC Detail

☐ Reduced Report

Default Display

Color

OpCode

Cycle Type

Tag

Length

Address

Data

Response

Status

Range

Decode Range

From To

Channel:

CS#: Chip Select (Active Low)

SCK: Clock
I/O0 – I/O3: Data input / output
Alert: Alert signal (Optional)
Reset: Reset signal (Optional)

Startup Settings:

I/O Mode Setting: Set the initial I / O state to be Single / Dual / Quad, and I / O state would be switched automatically by the content of the waveform.

Default Alert Mode: Set the channel of Alert signal.

Command deselect time: Set tSHSL, Chip Select# Deassertion Time.

Clock LOW to output valid: Set tCLQV, Output Data Valid Time.

Advanced Decode Setting:

Show Configuration Detail: Show details of SET_CONFIG / GET_CONFIG.

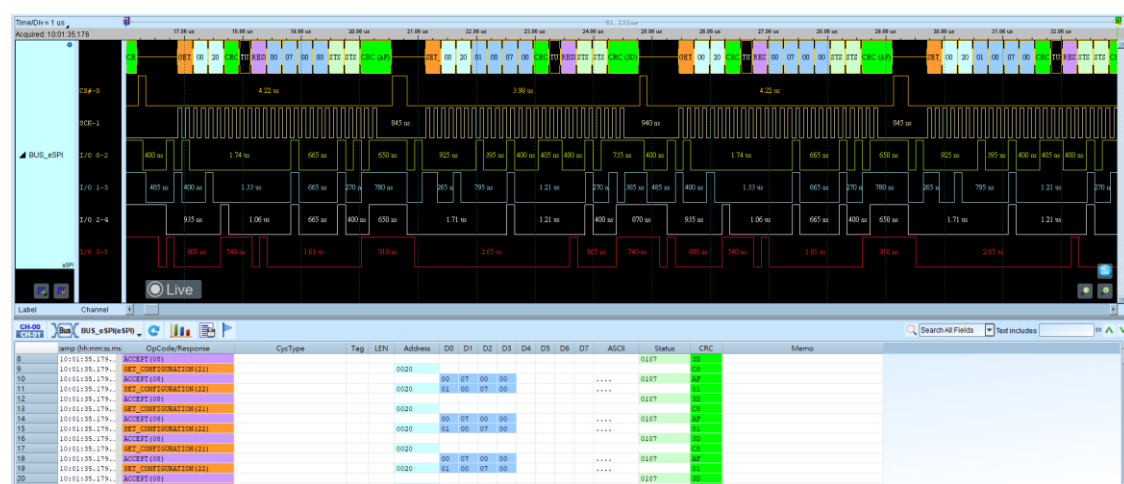
Show Status Bit Def.: Show details of Status.

Reduced Report: Reducing the report is easy to check the Command Flow.

Filter Setting: To show or hide the specific OP Code / Cycle Type or Address range in the report.

Note: The setting of Address Filter would be saved as LAleSPI\leSPIFilterX.bin in the work directory.

Result



FlexRay

FlexRay is an in-vehicle communication network standard that supports two communication channels, each with a speed of up to 10 Mbps.

Settings

FlexRay Settings

Setting

Channel

Communication Data (Rx/D) ☐ RxEN ☐ Rx/D A0 A1

Auto detect Data Rate ☒ 0.00 Mbps (1 Mbps ~ 20 Mbps)

FlexRay Channel Channel A

☐ Show scale in the waveform

Color

Indicator Bits	Color
TSS	White
FSS	Magenta
BSS	Yellow
FES	Yellow
DTS	Green
WUS	Cyan
CAS/MTS	Blue
Error	Red

Range

Decode Range

From Buffer Head To Buffer Tail

Channel: Set the channel, Communication Data (Tx/D)

Communication Data (Tx/D): The Tx/D data is from the Tx/D and TxEN of the FlexRay transceiver.

Communication Data (Rx/D): The Rx/D data is from the Rx/D and RxEN of the FlexRay transceiver.

Auto detect Data Rate: Default is Auto Bit Rate. If disabled, you may use built-in Bit Rate 10/5/2.5 Mbps or input manually, ranges from 1Mbps-20Mbps.

FlexRay Channel: Channel A or B, for Frame CRC checking.

Errors are:

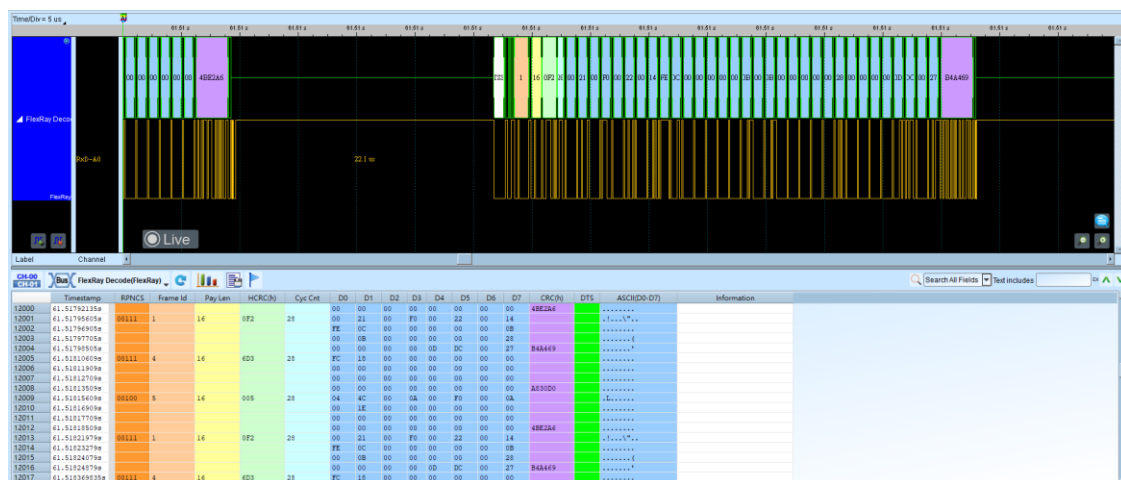
Error	Description
TSS Error	Unable to detect TSS
FSS Error	Unable to detect FSS
BSS Error	Unable to detect BSS
FES Error	Unable to detect FES
Header CRC Error	The header CRC value is incorrect
Frame CRC Error	The frame CRC value is incorrect

Abbreviations are:

Abbreviation	Description
TSS	Transmission start sequence
FSS	Frame start sequence
BSS	Byte start sequence
FES	Frame end sequence
DTS	Dynamic trailing sequence
CAS	Collision Avoidance Symbol
MTS	Media Access Test Symbol
WUP	Wakeup Pattern
CID	Channel Idle Delimiter

Result

10Mbps FlexRay Communication Data(RxD)



HD Audio

High Definition Audio, also known as HD Audio or by its codename, Azalia, is an audio standard created by Intel to be used on their chipsets, i.e., it is a standard for high-quality on-board audio. In this tutorial we will explain more about this feature.

Settings



HD Audio Settings

Setting

SYNC CH 0 I/O 0 CH 3

BCLK CH 1

Direction

☐ SDO ☒ SDI

Color

Stream Data

Preamble Stream ID

Length Sample

Response (SDI)

Valid UnSol

Reserved Response

Command (SDO)

Reserved CAd

NID Verb ID

Payload

Range

Decode Range

From To

Buffer Head Buffer Tail

☐ Default

Channel: Show the selected channel.

HDLC

HDLC (High-level Data Link Control) is the default synchronous data link layer protocol used in the equipment of Cisco.

Settings

HDLC Settings

Parameters

Channel Setting

Data: A0

Option

Mode: NRZI-0

Parity: Low

Baud Rate: 9600

Address Bits: 8

Control Bits: 8

FCS Bits: 16

Order: LSB

Color

Flag: [Blue]

Address: [Cyan]

Control: [Purple]

I-Frame: [Yellow]

S-Frame: [Green]

U-Frame: [Red]

Information: [Light Blue]

FCS: [Magenta]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

HDLC: Set the channel of the signal.

Option: Start up Setting of signal analysis

- I. **Mode:** Choose the analysis method.
- II. **Parity:** Set Parity (High / Low)
- III. **Baud Rate:** Set Baud rate

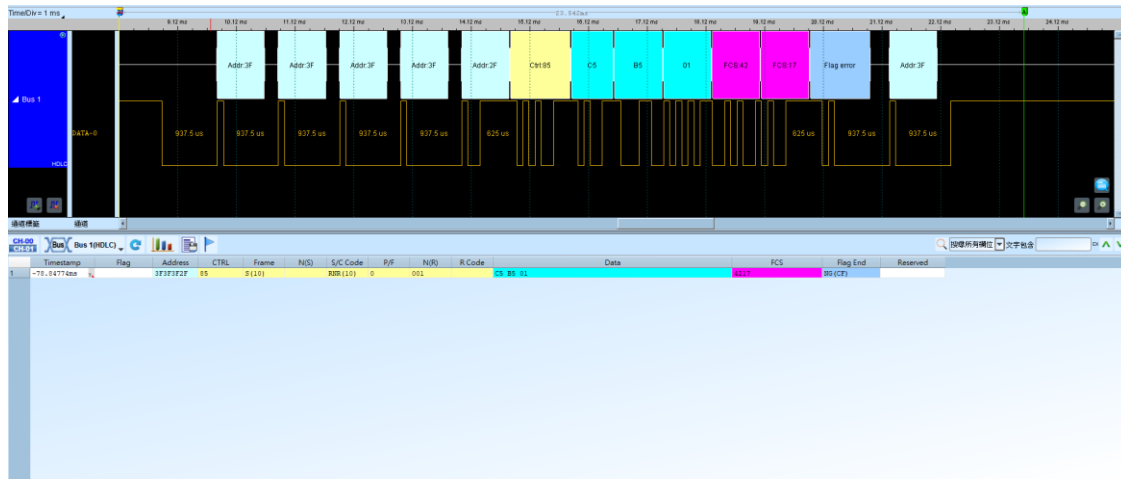
IV. **Address Bits:** Set the length of Address Bits.

V. **Control Bits:** Set the length of Control Bits.

VI. **FCS Bits:** Set the length of FCS (Frame Check Sequence) Bits.

VII. **Order:** Bit order of transmission.

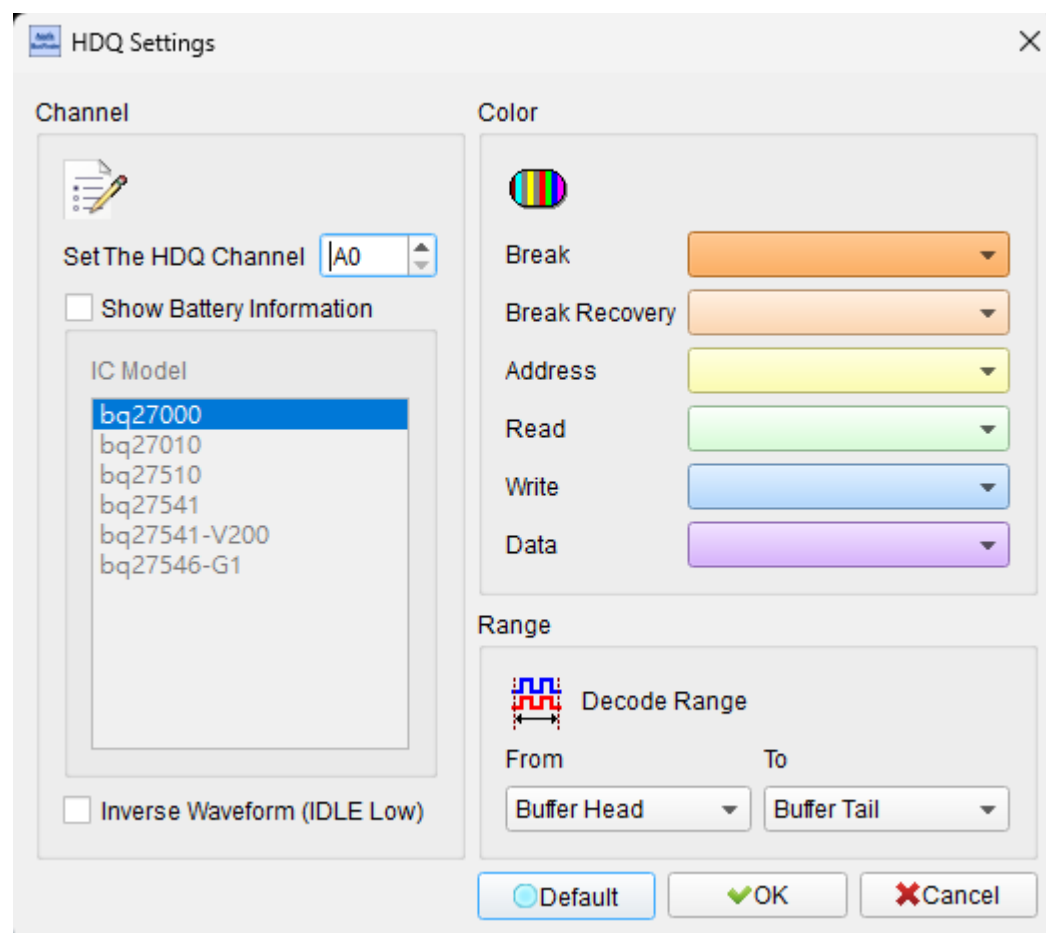
Result



HDQ

Developed by TEXAS INSTRUMENTS for battery management display applications, primarily in consumer electronics, HDQ is available in two data width formats, 8-bit and 16-bit, with a fixed 7-bit address. An HDQ packet mainly consists of Break, 7 bits Address, 1 bit R/W and 8 bits Data or 16 bits Data. The transmission method is LSB (Least-significant bit) to MSB (Most-significant bit), and the maximum transmission rate is 5 Kbit/s. The maximum transmission rate is 5Kbit/s.

Settings



Channel: Set the HDQ channel: Show the selected channel (CH 0).

Show Battery Information: monitor the command between battery and IC.

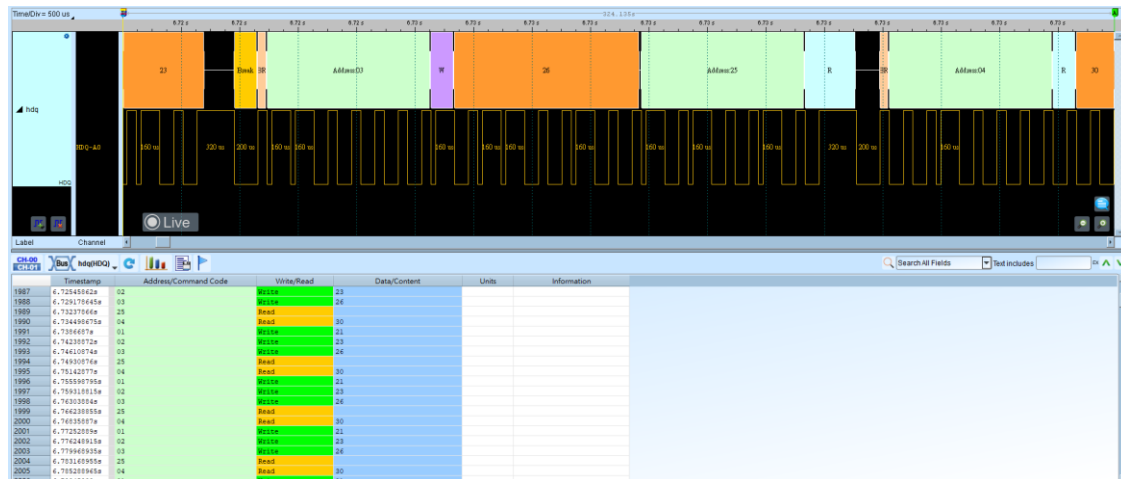
Invese Waveform (IDLE Low): Invert the waveform. Enabled when

checked.

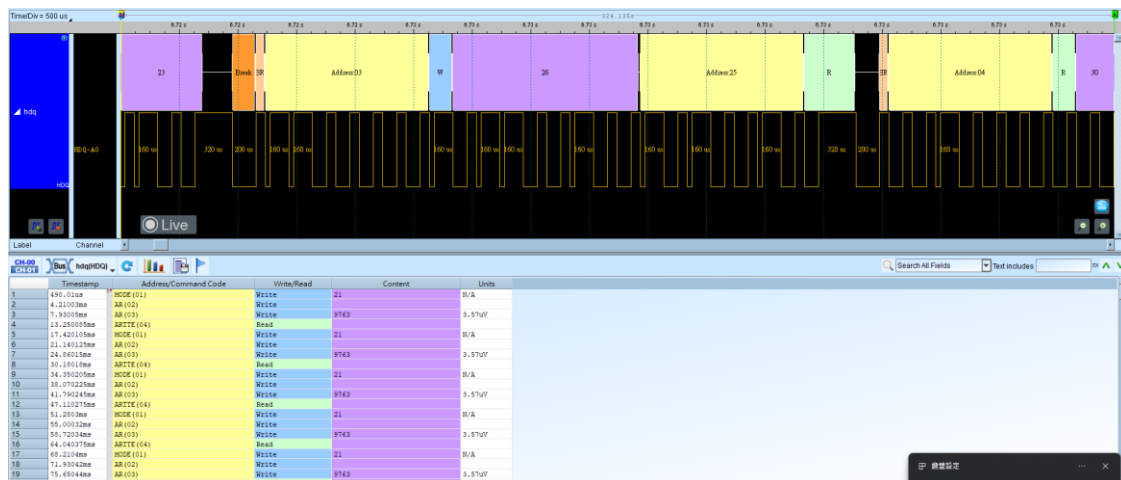
Result

Write: Indicates that the data is written and followed by the data.

Read: Read Indicates that the data is read, followed by the data.



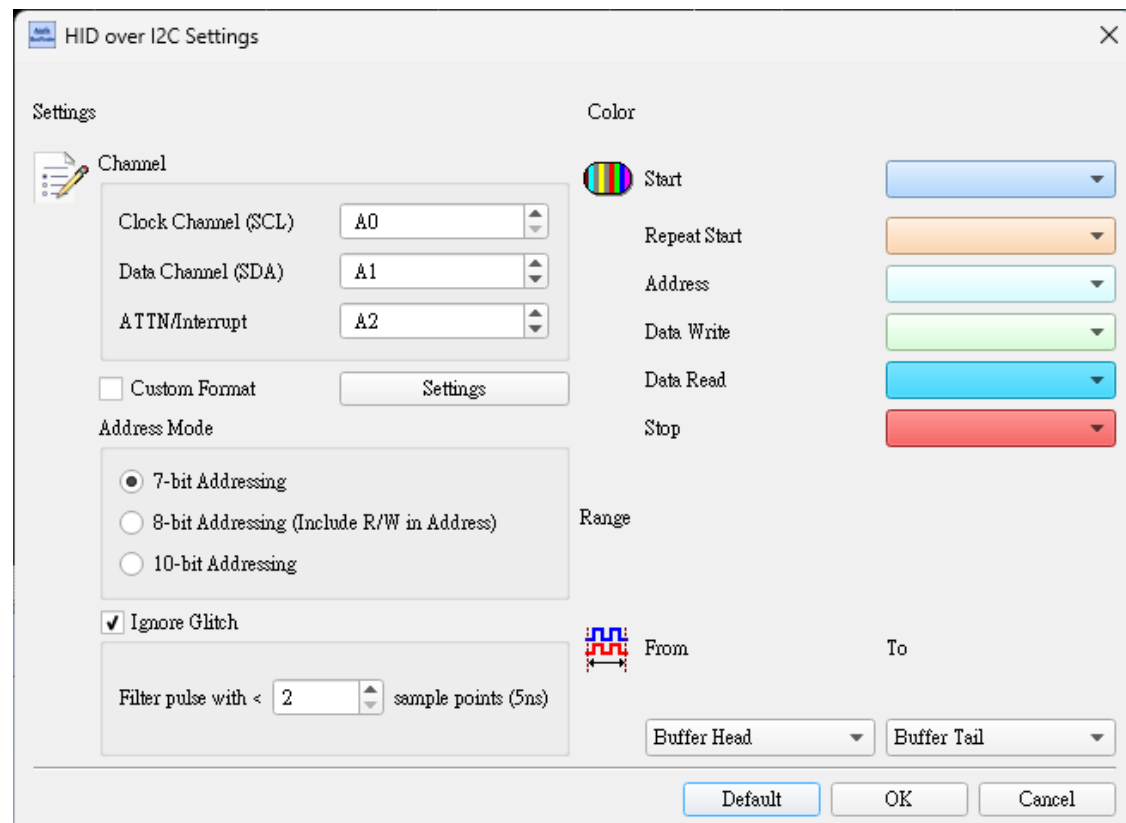
Show the battery information



HID Over I²C

HID Over I2C (Human Interface Device Over I2C) is mainly used in Windows 8, ARM platform architecture; the other is HID Over USB is used in x86 system, in Windows 8 common support for HID Over I2C bus protocol device is touch pad.

Settings



Channel: Show the selected channels (SCL:CH0, SDA:CH1, ATTN:CH2).

Custom Format: Customizable partial analysis content.

Setting: Click on it to bring up Notepad to edit the decoding format, the format is as follows: CMD, {Name of parse field 1, Number of bytes in parse field 1, Arrangement of parse field 1},

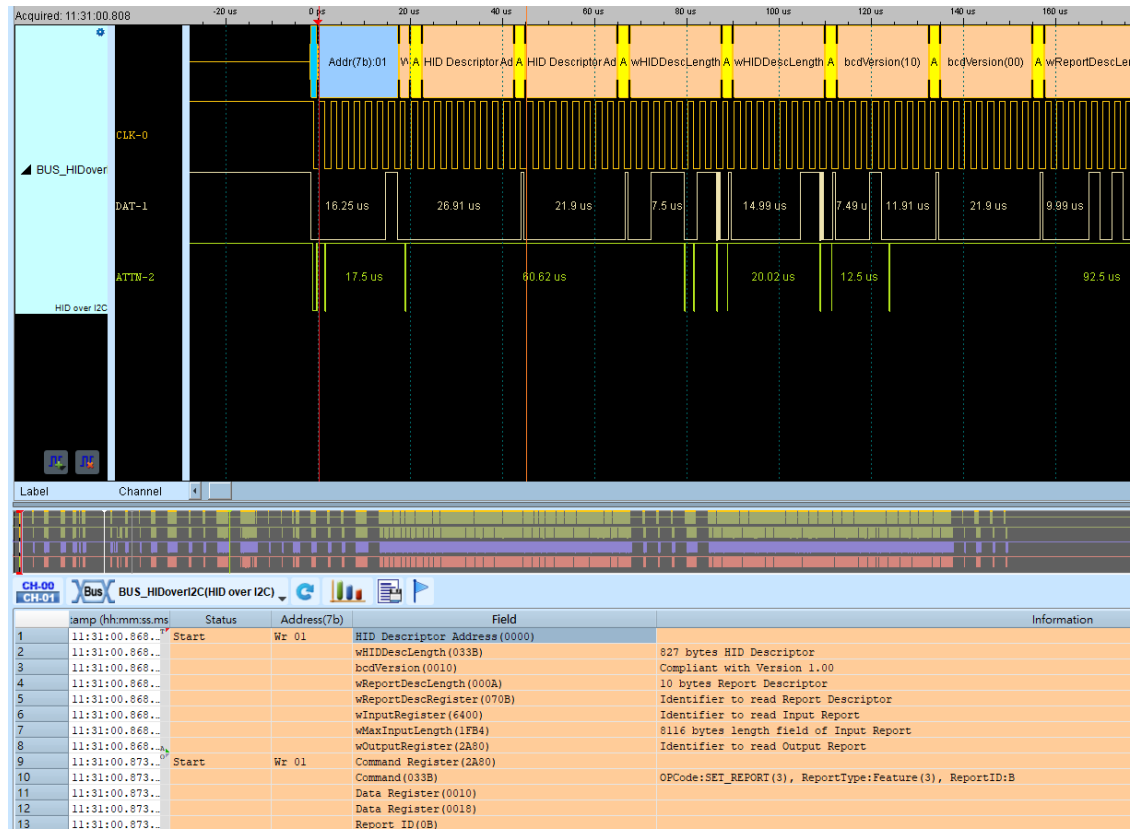
7-bit addressing: Show 7-bit addressing.

8-bit addressing (Include R/W in Address): Show 8-bit addressing (include 7-bit addressing and 1-bit Rd/Wr).

10-bit addressing: show 10-bit addressing.

Ignore glitch: Ignore the glitches occurred due to the slow transitions. Enabled when checked.

Result



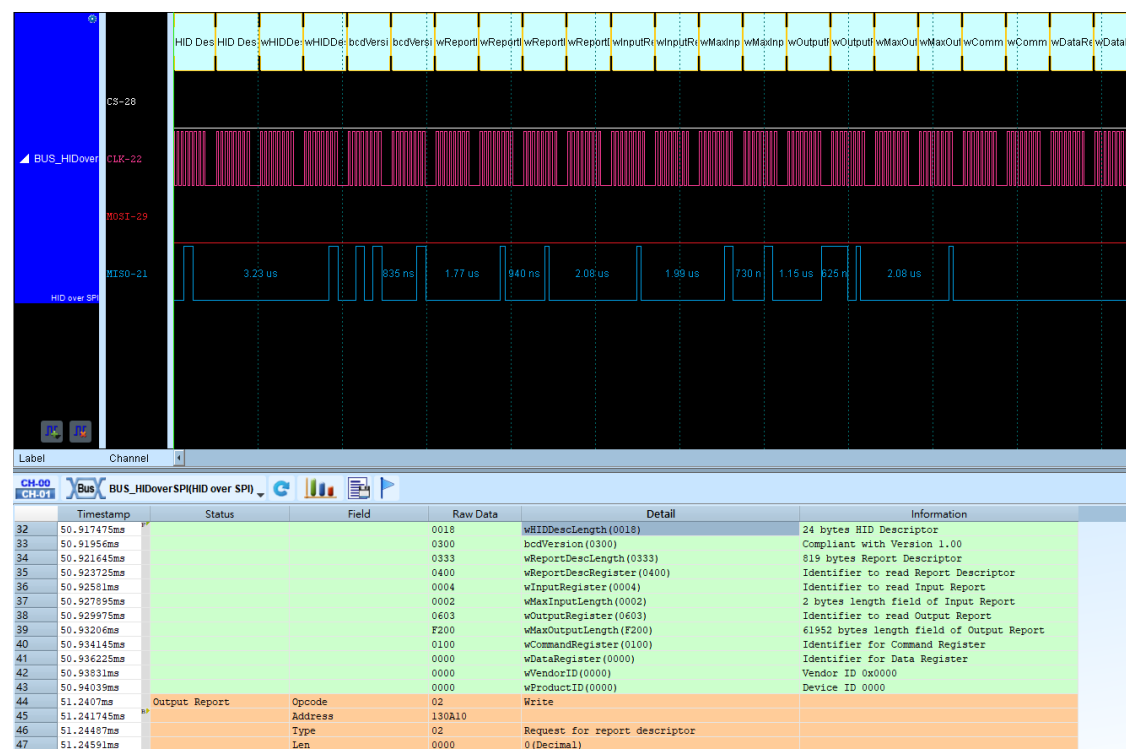
HID Over SPI

HID Over SPI (Human Interface Device Over SPI) protocol is established by Microsoft. It's applied for Windows 8 ARM platform.

Settings

Channel: Show the selected channels (CS, CLK, MOSI, MISO).

Result



HTSensor

An HTSensor is a sensor designed to measure and monitor environmental conditions. It typically measures environment-related parameters such as temperature and humidity and provides the corresponding data to a system or device for processing or control. These sensors are widely used in a variety of devices and systems, such as smart homes, automation systems, climate control systems, medical devices, and so on.

Setting

HTSensor Settings

Channel

Data: A0

Color

Humidity: Start

Temperature: Echo

Check Digits: End

Chip Settings

Model: AM2120 Tolerance: 0%

Parameter	Min	Max	Unit
Start Low	1000	20000	us
Echo Low	75	85	us
Logic 0 High	22	30	us
Logic 0&1 Low	48	55	us
Start High	10	200	us
Echo High	75	85	us
Logic 1 High	68	75	us
End Low	45	55	us

Display: Celsius (°C) Calculate Type: (High Low) / 10

Range

Decode Range

From: Buffer Head To: Buffer Tail

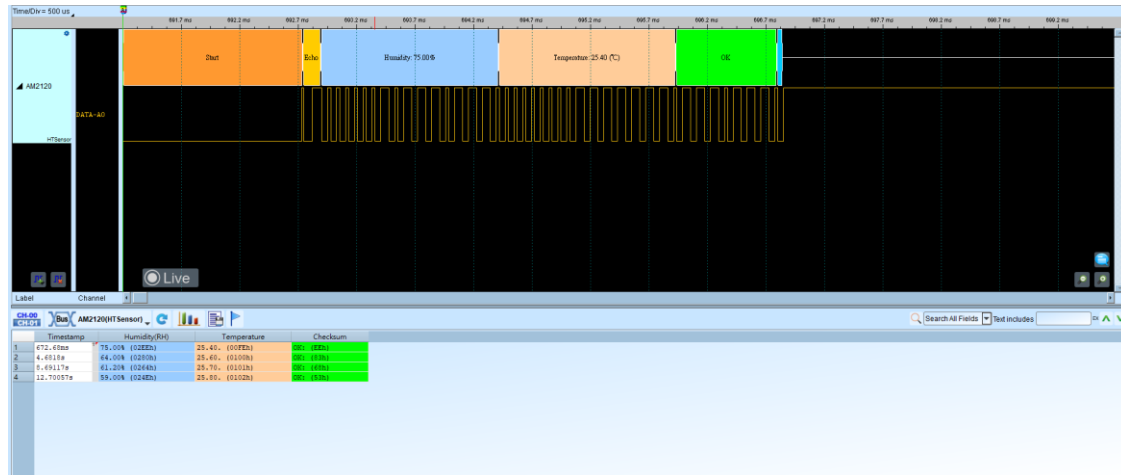
Default OK Cancel

Data: Set the channel number of the Logic Analyzer to which each signal end is

connected on the object to be tested.

Chip Setting: Configure supported chip models or user-defined chip parameter details.

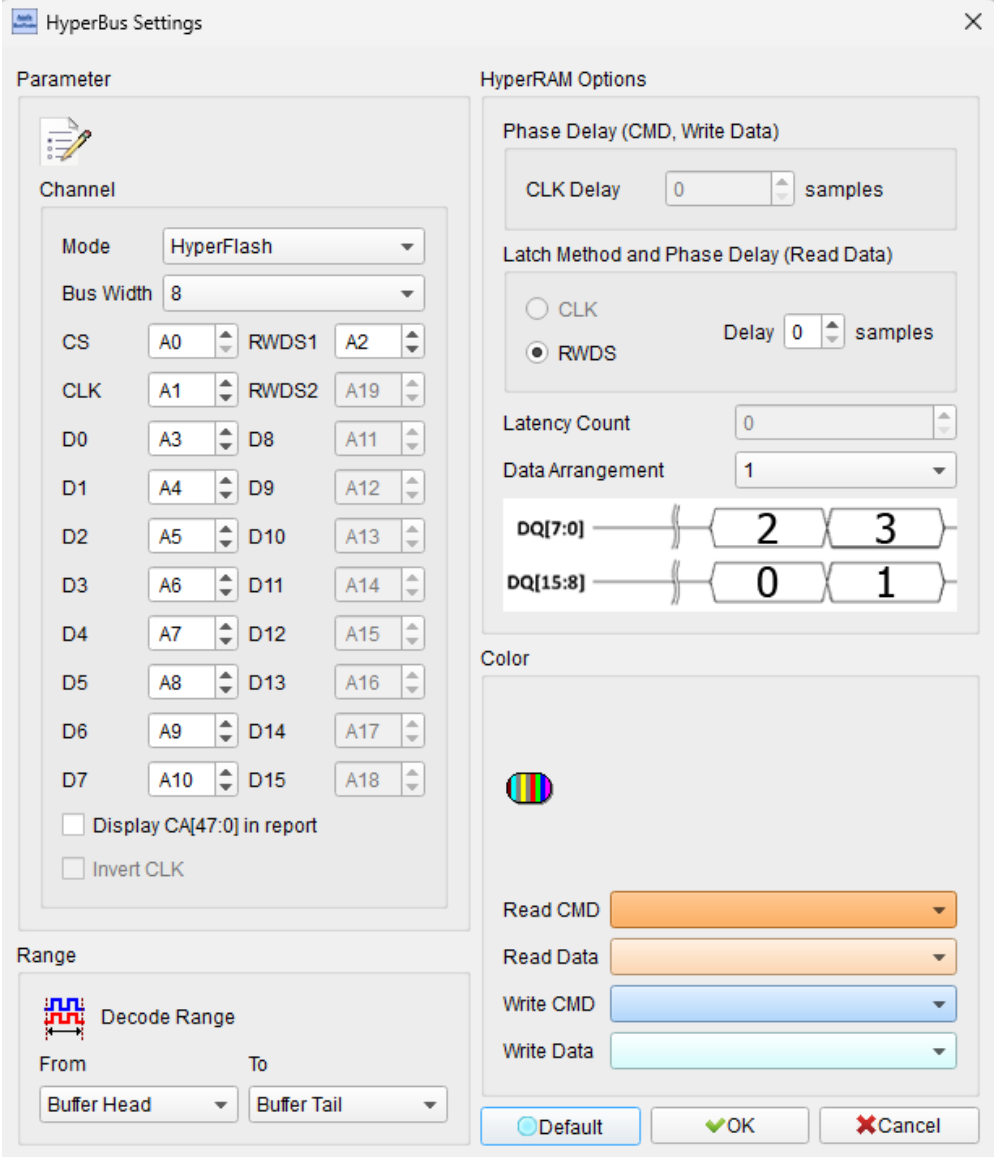
Result



HyperBus

HyperBus is a high-performance memory interface technology designed to increase data transfer rates, especially in embedded systems such as smartphones, tablets, and IoT devices. Proposed by Micron Technology and adopted by several device manufacturers, HyperBus technology can support many different types of memory, most commonly used for connecting Flash memory and DRAM (Dynamic Random Access Memory), while providing faster data read and write speeds than traditional SPI and parallel memory interfaces.

Settings



The HyperBus Settings dialog box is divided into several sections:

- Parameter**:
 - Channel**:
 - Mode: HyperFlash
 - Bus Width: 8
 - CS: A0, RWDS1, A2
 - CLK: A1, RWDS2, A19
 - D0: A3, D8, A11
 - D1: A4, D9, A12
 - D2: A5, D10, A13
 - D3: A6, D11, A14
 - D4: A7, D12, A15
 - D5: A8, D13, A16
 - D6: A9, D14, A17
 - D7: A10, D15, A18
 - ☐ Display CA[47:0] in report
 - ☐ Invert CLK
 - Range**:
 - Decode Range: From Buffer Head To Buffer Tail
- HyperRAM Options**:
 - Phase Delay (CMD, Write Data)**:
 - CLK Delay: 0 samples
 - Latch Method and Phase Delay (Read Data)**:
 - ☐ CLK
 - ☒ RWDS Delay: 0 samples
 - Latency Count: 0
 - Data Arrangement: 1
 - Data Diagram**:
 - DQ[7:0]: 2, 3
 - DQ[15:8]: 0, 1
 - Color**:
 - Read CMD: Orange
 - Read Data: Orange
 - Write CMD: Blue
 - Write Data: Light Blue
- Buttons**: Default, OK, Cancel

Mode: Switching mode, can be set to Hyper Flash or Hyper Ram.

Bus Width: Setting the bus width, can be set to 8 or 16.

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

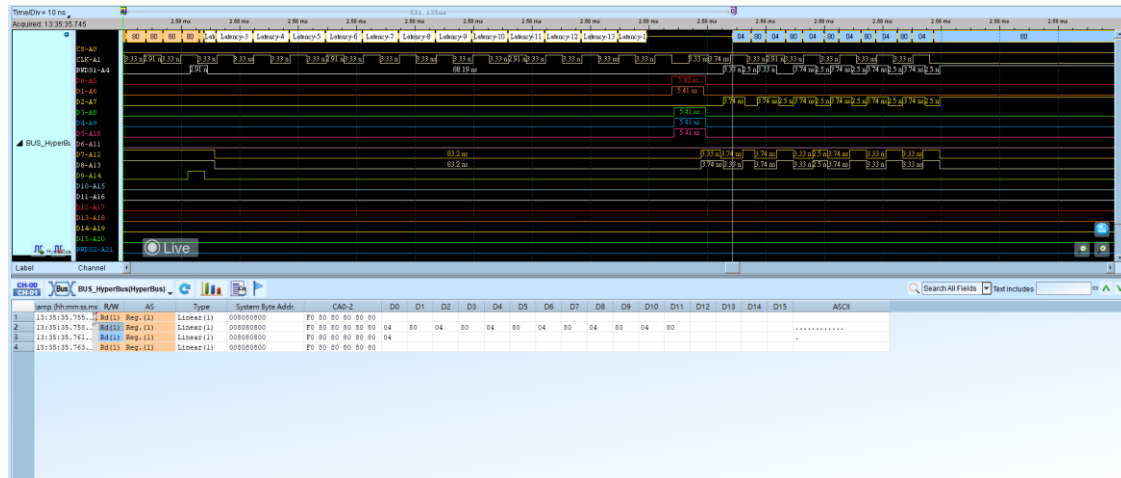
Display CA[47:0] in report: Displays CA[47:0] total 48bit information in the report. Available only when the mode is switched to HyperFlash. Enabled when checked.

Invert CLK: Invert CLK: Available only when mode is switched to HyperRam. Enabled when checked.

HyperRAM Options:

- I. **Phase Delay (CMD, Write Data):** Sets the number of sample points for Delay, valid only when the mode is switched to HyperRam.
- II. **Latch Method and Phase Delay (Read Data):** Set the number of sample points for CLK (valid only when mode is switched to HyperRam) or RWDS Delay.
- III. **Latency Count:** Sets the number of Delay CLKs, valid only when the mode is switched to HyperRam.
- IV. **Data Arrangement:** Sets the mode of the Data Arrangement to one of two modes.

Result



I²C

I²C is a two-wire serial communications bus, using a multi-slave architecture, developed by Philips in the 1980s to enable motherboards, embedded systems, or cell phones to connect to low-speed peripheral devices, and is a commonly used type of electronic circuit system. I²C uses only two bi-directional signal lines, one clock line (SCL) and one data line (SDA). Signal content has a total of start (Start), address (Address), data (Data), read/write (Read/Write), etc., the transmission method is bidirectional, the data format is divided into two kinds of 8 bits and 10 bits. The transmission rate is 100kbit/s-3.4Mbit/s. The data format is divided into 8 bits and 10 bits.

Settings

I2C Settings

Settings

Channel

Clock Channel (SCL)

Data Channel (SDA)

Address Mode

☒ 7-bit Addressing

☐ 8-bit Addressing (Include R/W in Address)

☐ 10-bit Addressing

Report

Show data in report

☐ Show NACK ☐ Unwrap the ASCII frame

☐ Clock Stretching

Timeout Check us

☒ Ignore Glitch

Filter pulse with < sample points

Color

Start

Repeat Start

Address

Data Write

Data Read

Stop

Range

Decode Range

From To

Clock Channel (SCL): Transfer clock of I²C.

Data Channel (SDA): Transfer data of I²C.

Address Mode:

- I. **7-bit addressing:** Displays the address in 7-bit width and Rd/Wr in 1-bit width.
- II. **8-bit addressing(Include R/W in Address):** Displays an 8-bit width address (7-bit width address plus 1-bit Rd/Wr).
- III. **10-bit addressing:** Displays a 10-bit width address.

Report:

- I. **Show data in report:** Displays the data in the report area with a choice of 8 or 16 fields.
- II. **Show NACK:** Marks the Byte as NACK in the field. enabled when checked.
- III. **Unwrap the ASCII frame:** Add “ASCII” field in the report area.
Enabled when checked.

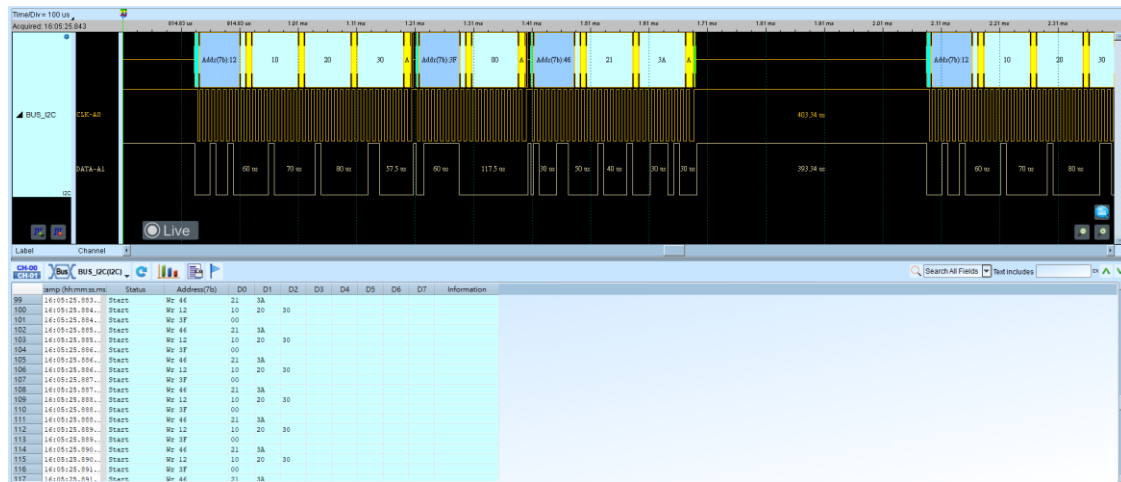
Clock Stretching: Set the length of time for Clock Streching. Enabled when checked.

Ignore Glitch: Ignore glitch caused by slow transitions when analyzing.
Enabled when checked.

Result

Wr: Indicates that the data is written.

Rd: Indicates reading data.



I²C EEPROM

EEPROM, or E²PROM, is known as Electrically-Erasable Programmable Read-Only Memory, and the interface of EEPROM components can be classified into serial and parallel, with I²C EEPROM belonging to the 2-wire serial EEPROM, and its model is a series starting with 24. I²C EEPROM belongs to the 2-wire serial EEPROM, and its model number is a series starting with 24.

Settings

I2C(EEPROM 24 Series) Settings

Parameters

Channel

Clock Channel (SCL) A0

Data Channel (SDA) A1

Device Address

☒ Control Code

☐ 7-bit Addressing

☐ 8-bit Addressing (Include R / W in Address)

Word Address

Address Width 8

☐ 24LCS61 / 24LCS62

☒ Ignore Glitch

Color

Start Output Enable

Control Device ID

Address Command Select

Read Data

Write Stop

ACK

NACK

Chip

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Clock Channel (SCL): Transfer clock of I²C.

Data Channel (SDA): Transfer data of I²C.

Device Address:

1. **Control Code:** Display Control Code.

IV. **7-bit Addressing:** Displays the address in 7-bit width and Rd/Wr in 1-bit width.

2. **8-bit Addressing (Include R/W in Address):** Displays an 8-bit width address (7-bit width address plus 1-bit Rd/Wr).

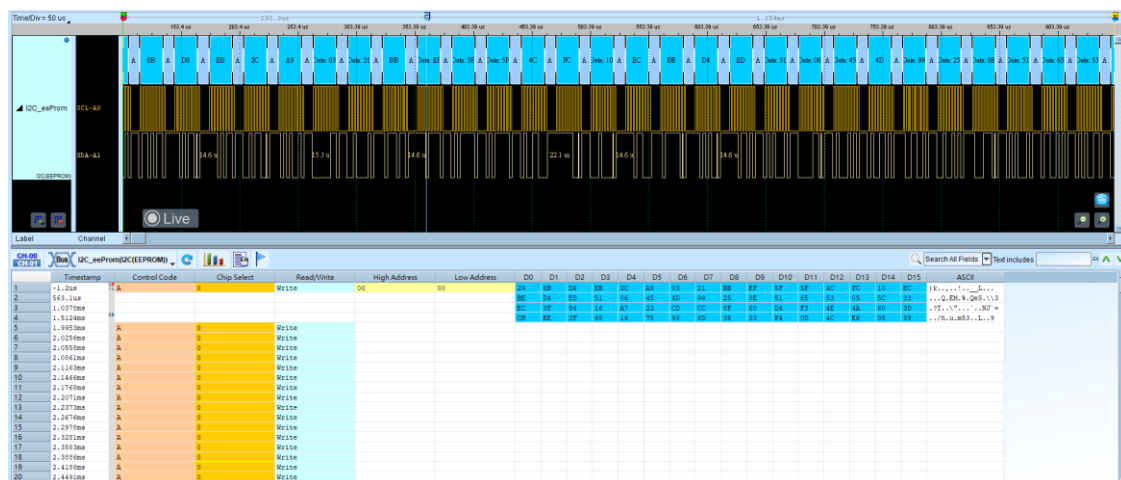
Word Address: Set the number of valid bits of I2C EEPROM address, the default value is 8.

24LCS61 / 24LCS62: Select whether to analyze 24LCS61 / 24LCS62. enabled when checked.

Ignore Glitch: Ignore glitch caused by slow transitions when analyzing.

Enabled when checked.

Result



I²S

I²S is an interface standard for transferring digital audio data between ICs. It is a bus standard developed by Philips for transferring audio data between digital audio devices, and is often used for transferring PCM audio from a CD to a DAC in a CD player. The I²S standard specifies the hardware interface specifications and the format of the digital audio data, and uses a sequential approach to transmit two groups (left and right channels) of data. It consists of three transmission lines, a clock line (SCK), a word selection line (WS), and a data line (SD). The data format is up to 32 bits.

Settings

I2S Settings

Channel

Clock Channel (SCK) A0

Word Select Channel (WS) A1

Data Channel (SD) A2

Data Bits 16 bit(s)

Sound reduction

☐ Display the audio waveform

☐ Save as WAV file

☐ Playback

☐ Align common sample rate

Config

☐ Enable meet full scale

Mode I2S Mode

Report 8 Columns

TDM Settings

Channel Size 16

Channel Length 16

Word Length 8

Channel Offset 8

Latch Rising

Color

R. Channel

L. Channel

Range

Decode Range

From Buffer Head To Buffer Tail

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Data Bits: The number of bits of analyzed data ranges from 1 to 32 Bits; the default value is 16 Bits.

Sound reduction:

1. **Display the audio waveform:** User can draw the waveform of the sound in the Waveform area. Enabled when checked.
2. **Save as WAV file:** All Data can be saved as a sound file (.WAV) and saved in the working directory. Enabled when checked.
3. **Playback:** The default setting is off. This function collects all the data and plays it back after analyzing it. This is the fastest way to confirm that the sound is being transmitted correctly without having to go through the data one by one. Since the length of playback time depends on the depth of data that the Logic Analyzer can record, it is recommended that you increase the Logic Analyzer's data depth and reduce the number of channels used by the Logic Analyzer. Enabled when checked.
4. **Align common sample rate:** Automatically archives the sound waveforms with the sampling rate closest to the commonly used ones (44.1KHz, 48KHz). Enabled when checked.

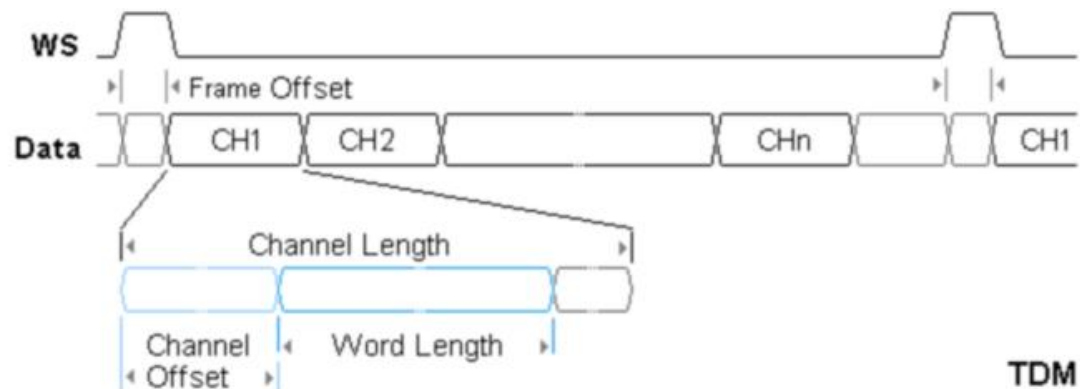
Config:

1. **Mode:** switch mode base on the needs.
 - i. I²S Justified
 - ii. MSB Justified
 - iii. LSB Justified
 - iv. PCM

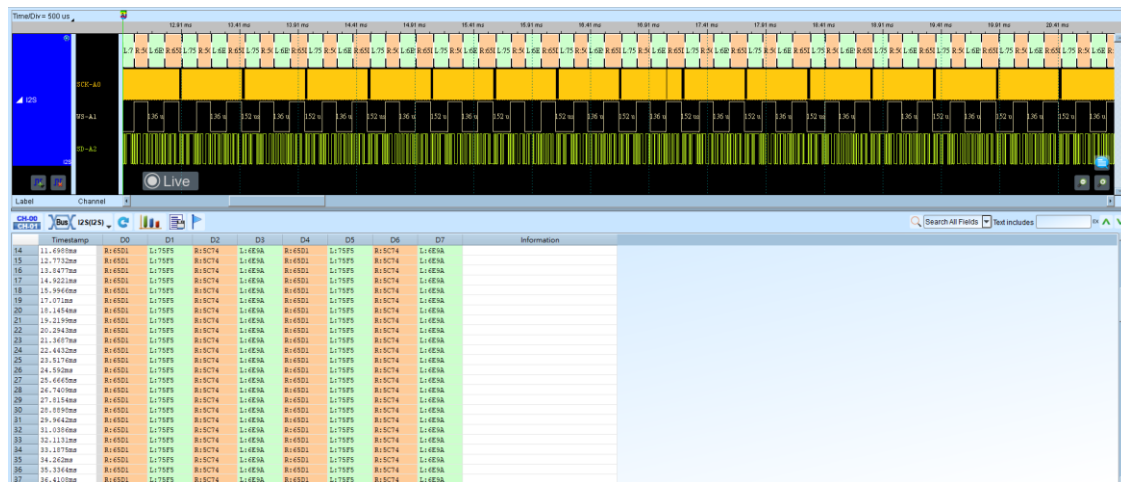
v. TDM

2. **Enable meet full scale:** Auto-completes missing bits in multiples of 8, e.g., 15 bits to 16 bits, 17 bits to 24 bits, enabled when checked.
3. **Report:** User can select the number of columns displayed in the report area.

TDM Setting Parameter Definitions:



Result

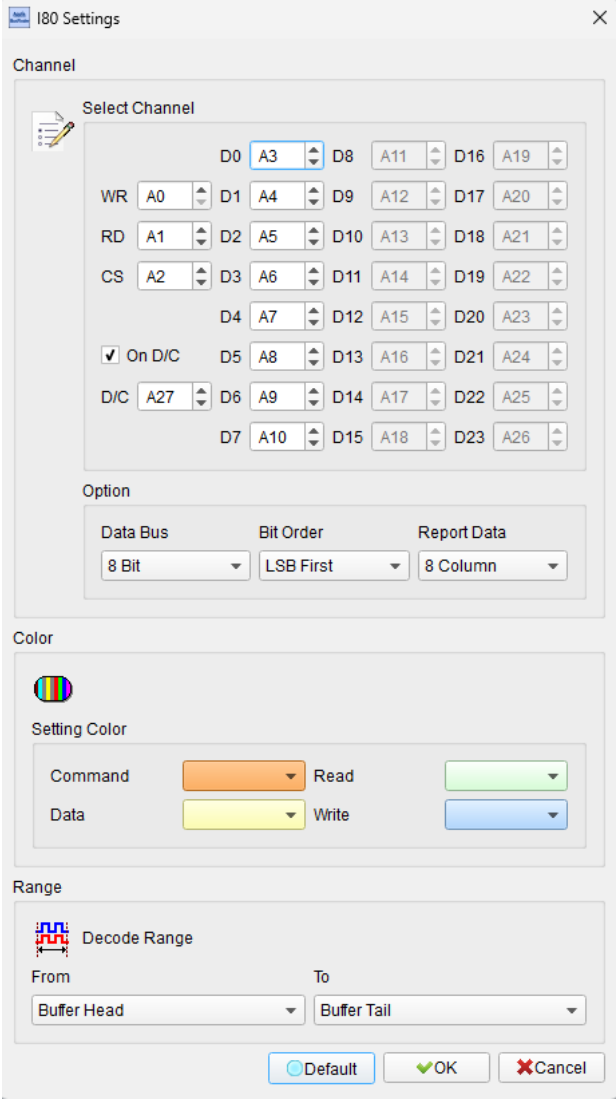


I80

The Inter 8080-series interface is mainly used for LCM data transfer.

It is simply called I80 interface. To analyze the 8080-series, 3 or 4 Ctrl Buses (WR, RD, CS, and D/C) are required, and the Data Bus requires at least 4 bits depending on the user's definition, so at least 7 channels are required: WR, RD, CS, D0-D3, and 8 channels if there is a D/C Pin. The channel numbers of these signals can be adjusted. The channel numbers of these signals can be adjusted. The 8 bits Data bus requires 11 signals: WR, RD, CS, D0-D7, and so on... WR to CH0, and so on.

Settings



I80 Settings

Channel

Select Channel

D0	A3	D8	A11	D16	A19
WR	A0	D1	A4	D9	A12
RD	A1	D2	A5	D10	A13
CS	A2	D3	A6	D11	A14
		D4	A7	D12	A15
<input checked="" type="checkbox"/> On D/C		D5	A8	D13	A16
D/C	A27	D6	A9	D14	A17
		D7	A10	D15	A18
				D23	A26

Option

Data Bus: 8 Bit
Bit Order: LSB First
Report Data: 8 Column

Color

Setting Color

Command	Read
Data	Write

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

IDE

IDE (Integrated Device Electronics) is a standard interface for hard disks, solid-state drives, CD-ROMs, etc. IDE was first used by Western Digital in the U.S. for its hard disk sales business. The name IDE was first used by Western Digital in the United States for their hard disk sales business. The official specification name is ATA/ATAPI (Advanced Technology Attachment/AT Attachment Packet Interface). The ATA specification has continued to be added to due to the increased capacity of hard disks, the need for higher transfer speeds, and the constant evolution of storage devices. In 1998, the ATAPI specification was added to ATA-4, allowing ATA to connect to optical drives and other storage media. In 2003, the SATA (Serial ATA) specification was released, which retroactively renamed the original Parallel ATA to PATA (Parallel ATA) to differentiate it.

To analyze IDE, because it is a parallel transmission, it needs to use more channels, so we have to divide it into three types.

Normal channel (11 pin): Its signals are DASP-, DIOR-:HDMARDY-:HSTROBE, DIOW-:STOP, DMACK-, DMARQ, INTRQ, IORDY:DDMARDY-:DSTROBE, PDIAG-:CBLID-, RESET-, CSEL and IOCS16. -.

Register channel (5 pin): its signals are CS(0:1)- and DA(2:0).

Data channel (16 pin): its signal is DD(15:0).

We recommend that IDE bus of the target system to be connected to the instrument as the following table:

IDE Pin No.	IDE Pin name	IDE Pin Description	LA default Channel No.
Pin1	Reset-	Hardware reset	Channel 0
Pin2	Ground		
Pin3	DD7	Device data	Channel 1
Pin4	DD8	Device data	Channel 2
Pin5	DD6	Device data	Channel 3
Pin6	DD9	Device data	Channel 4

Pin7	DD5	Device data	Channel 5
Pin8	DD10	Device data	Channel 6
Pin9	DD4	Device data	Channel 7
Pin10	DD11	Device data	Channel 8
Pin11	DD3	Device data	Channel 9
Pin12	DD12	Device data	Channel 10
Pin13	DD2	Device data	Channel 11
Pin14	DD13	Device data	Channel 12
Pin15	DD1	Device data	Channel 13
Pin16	DD14	Device data	Channel 14
Pin17	DD0	Device data	Channel 15
Pin18	DD15	Device data	Channel 16
Pin19	Ground		
Pin20	Key pin		
Pin21	DMARQ	DMA request	Channel 17
Pin22	Ground		
Pin23	DIOW-:STOP	Device I/O write: Stop Ultra DMA burst	Channel 18
Pin24	Ground		
Pin25	DIOR-:HDMAR DY- :HSTROBE	Device I/O read: Ultra DMA ready: Ultra DMA data strobe	Channel 19
Pin26	Ground		
Pin27	IORDY:DDMAR DY- :DSTROBE	I/O channel ready: Ultra DMA ready: Ultra DMA data strobe	Channel 20
Pin28	CSEL	Cable select	Channel 21
Pin29	DMACK-	DMA acknowledge	Channel 22
Pin30	Ground		
Pin31	INTRQ	Device interrupt	Channel 23
Pin32	Obsolete (see note)	Device 16-bit I/O in ATA-2	Channel 24

Pin33	DA1	Device address	Channel 25
Pin34	PDIAG-:CBLID-	Passed diagnostics: Cable assembly type identifier	Channel 26
Pin35	DA0	Device address	Channel 27
Pin36	DA2	Device address	Channel 28
Pin37	CS0-	Chip select	Channel 29
Pin38	CS1-	Chip select	Channel 30
Pin39	DASP-	Device active, device 1 present	Channel 31
Pin40	Ground		

Settings

IDE Settings

Channel

General

Register

Data Bus

DIOR-:HDMARDY:HSTROBE

A20

PDIAG-:CBLID-

A24

DIOW-:STOP

A17

DASP-

A28

DMARQ

A18

RESET-

A19

IORDY:DDMARDY-DSTROBE

A22

CSEL

A23

DMACK-

A26

IOCS16-

A0

INTRQ

A31

Color and Setting

Transferring mode

Register Color

Analysis Report

Transferring Mode	Max Transferring Rate	Standard
<input type="radio"/> ULTRA DMA Mode 1	25MByte/sec	ATA-4
<input type="radio"/> ULTRA DMA Mode 2	33MByte/sec	ATA-4
<input type="radio"/> ULTRA DMA Mode 3	44MByte/sec	ATA-5
<input type="radio"/> ULTRA DMA Mode 4	66MByte/sec	ATA-5
<input checked="" type="radio"/> ULTRA DMA Mode 5	100MByte/sec	ATA-6

Range

Decode Range

From

Buffer Head

To

Buffer Tail

Default

OK

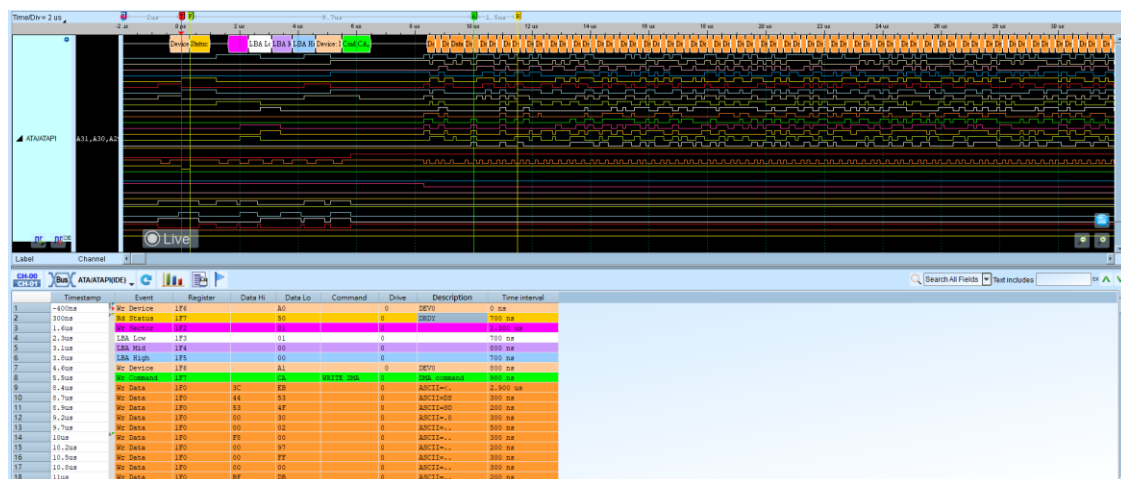
Cancel

Channel: Set channel number for General, Register, and Data Bus.

Transferring Mode: User can specify which specification will be used by the device to be tested so that commands can be interpreted correctly during IDE analysis. If it is not specified correctly, the analysis can be performed.

Analysis Report: User can specify that only those registers are displayed in the Display Report window. For example, if the Data Register is unchecked, data about the data register will not appear in the Report window. In this way, the contents of the data registers are filtered out when viewing the analysis results.

Result



IO-Link

IO-Link is a communication system that connects smart sensors and actuators to automation systems, in accordance with the Single-drop digital communication interface for small sensors and actuators (SDCI) in the IEC 61131-9 standard. This specification includes electrical connections and digital communication protocols through which smart sensors and actuators can interact with automation systems.

Settings

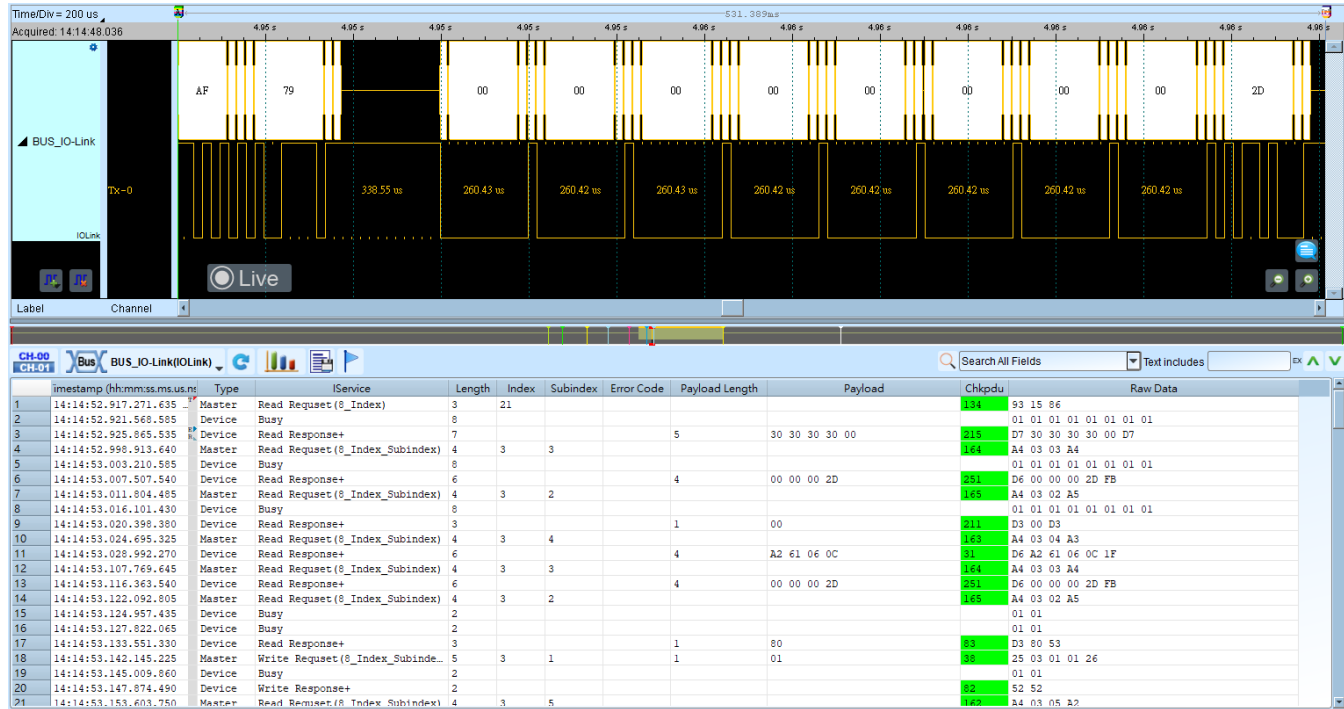
Channel: Set the C/Q signal terminal on the object under test to be connected to the channel number of the logic analyzer.

Timing Constraints:

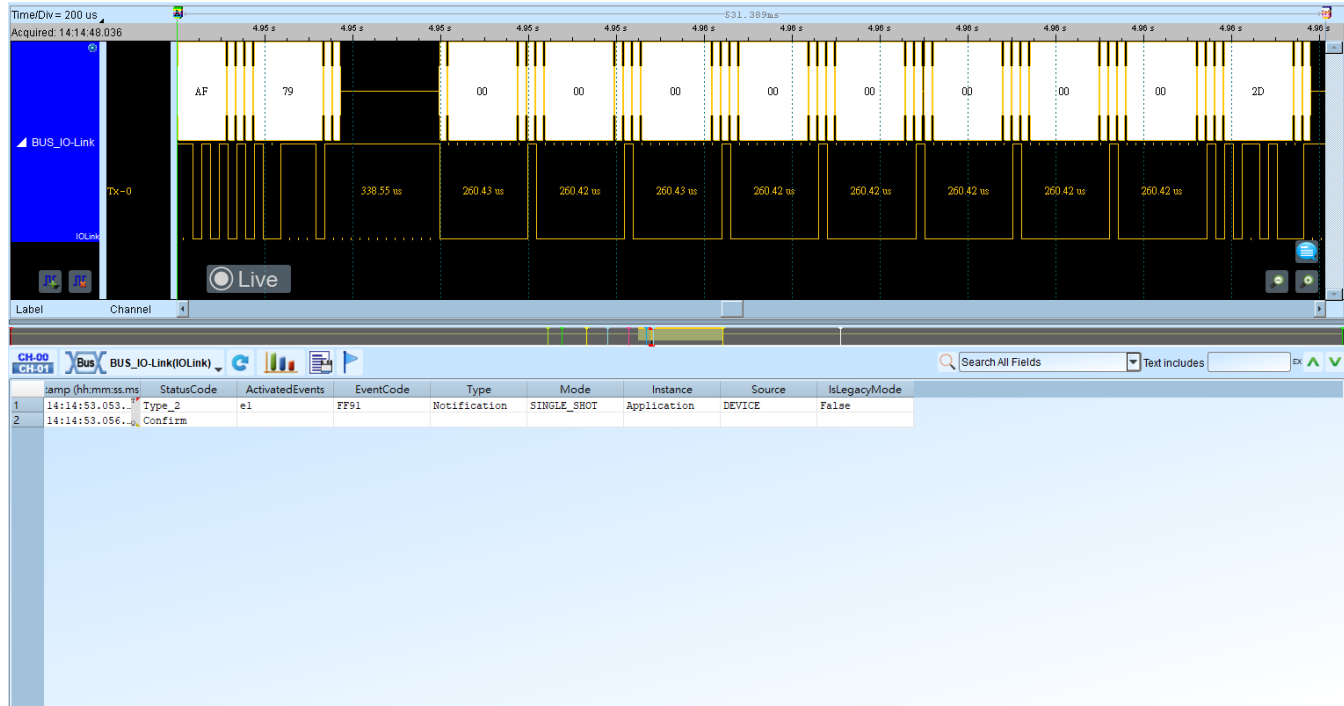
- **Transmission Timeout:** The default is 30 TBIT. If IDLE is larger than this value, the next data will be decoded and analyzed by the Master.
- **Response Time:** The default is 10 TBIT. If IDLE is less than this value and greater than 3 TBIT, the next data will be decoded and analyzed by Device.

Analysis Mode: The report will be analyzed in the selected mode (Overview, Frame, ISDU, Event).

ISDU



Event



IrDA

The Infrared Data Association (IrDA) was formed in 1993. The IrDA is point to point user model for a wide range of appliances and devices.

Settings

IrDA Settings

Channel

LA Channel: A0

☐ Invert Waveform

Color

Start: [Orange]

Data: [Light Orange]

Stop: [Yellow]

Address: [Light Green]

CRC: [Light Blue]

Mode

☐ SIR Transfer Rate: [] Kbps (2.4Kbps ~ 115.2Kbps)

☐ HDLC Transfer Rate: [] Mbps (0.576Mbps ~ 1.152Mbps)

☒ 4PPM(FIR)

Range

Decode Range

From: Buffer Head To: Buffer Tail

[Default] [OK] [Cancel]

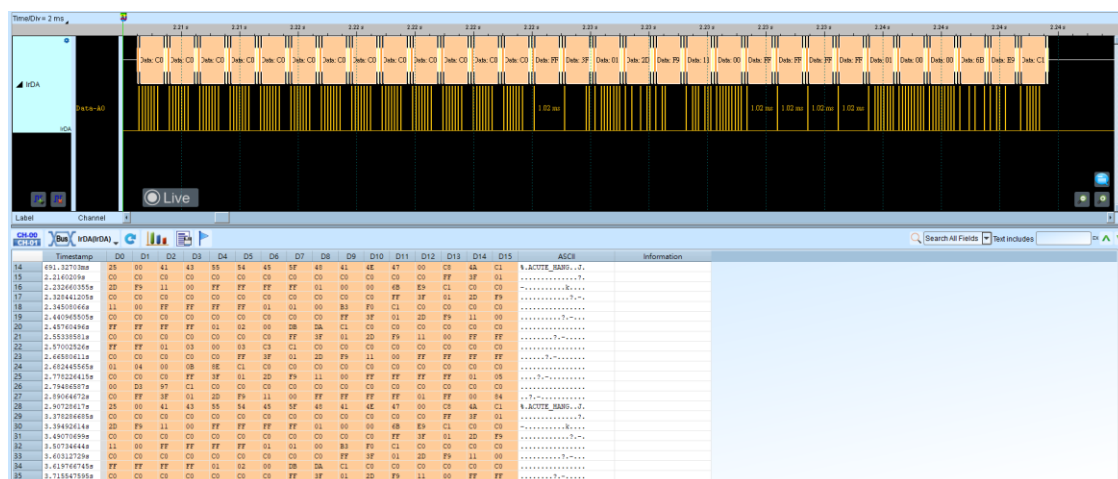
Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Invert Waveform: Invert the waveform before analysis. Enabled when checked.

Mode:

1. **SIR:** After switching to SIR mode, enter the transfer rate to complete the setting.
2. **HDLC:** After switching to HDLC mode, enter the input rate to complete the setting.
3. **4PPM (FIR):**

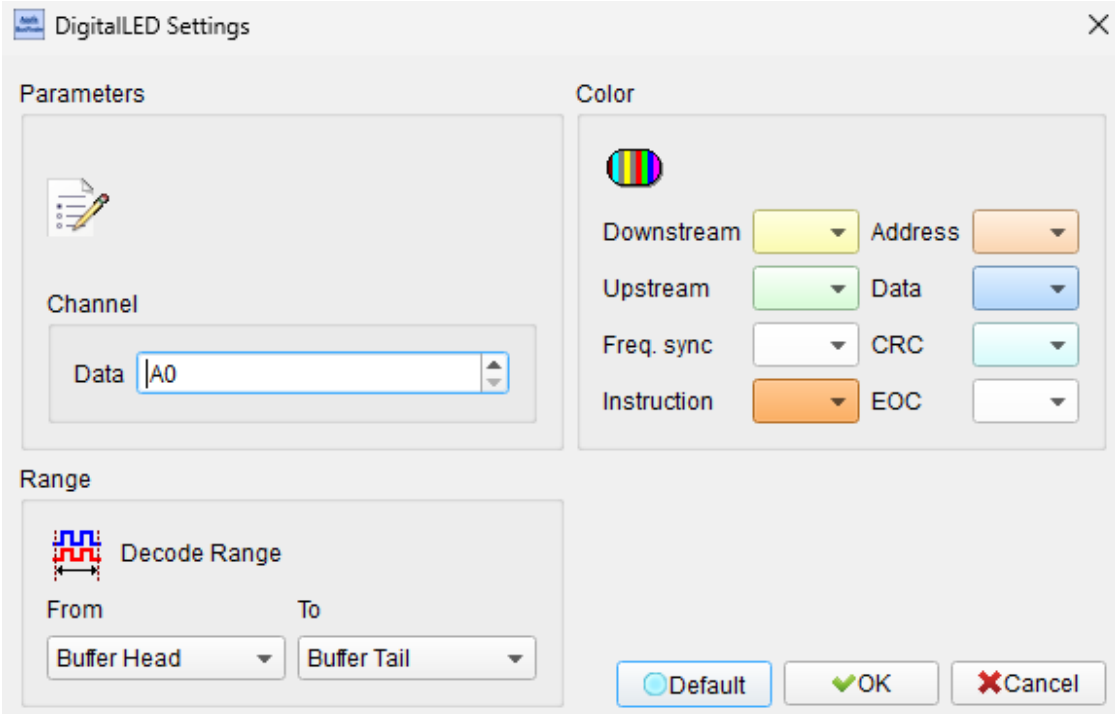
Result



ISELED

ISELED (Integrated Smart Embedded LED) is a new smart embedded LED technology designed to provide more efficient and intelligent control of LED lighting systems. It combines the luminous performance of LEDs with integrated circuit (IC) technology to enable more precise and flexible control for a wide range of application scenarios, especially in automotive, architectural and consumer electronics.

Settings



The **DigitalLED Settings** dialog box is divided into three main sections: **Parameters**, **Color**, and **Range**.

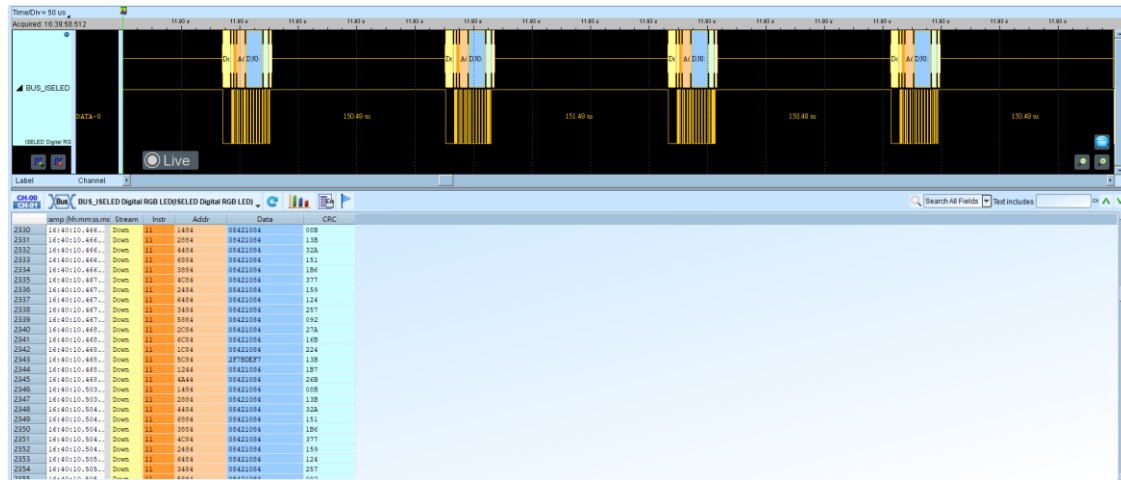
- Parameters:** Contains a 'Channel' section with a 'Data' field set to 'A0'.
- Color:** Contains a color selection icon and a table of settings:

Setting	Value	Setting	Value
Downstream	Yellow	Address	Orange
Upstream	Green	Data	Blue
Freq. sync	White	CRC	Cyan
Instruction	Orange	EOC	White
- Range:** Contains a 'Decode Range' section with 'From' and 'To' dropdowns, both set to 'Buffer Head' and 'Buffer Tail' respectively.

At the bottom right, there are three buttons: **Default** (with a blue circle icon), **OK** (with a green checkmark icon), and **Cancel** (with a red X icon).

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Result



ITU656 (CCIR656)

ITU656 describes a simple digital video protocol for streaming uncompressed PAL or NTSC Standard Definition TV (525 or 625 lines) signals. The protocol builds upon the 4:2:2 digital video encoding parameters defined in ITU-R Recommendation BT.601, which provides interlaced video data, streaming each field separately, and uses the YCbCr color space and a 13.5 MHz sampling frequency for pixels.

Settings

ITU-R BT.656 (CCIR656) Settings

Channel

Channel

CLK: A0 Data 5: A6 Data Bits: 8 Bits

Data 0: A1 Data 6: A7

Data 1: A2 Data 7: A8

Data 2: A3 Data 8: A9

Data 3: A4 Data 9: A10

Data 4: A5

☐ Save Raw Data

Color

SAV: CR

EAV: CB

Blanking: Y

Range

Decode Range

From: Buffer Head To: Buffer Tail

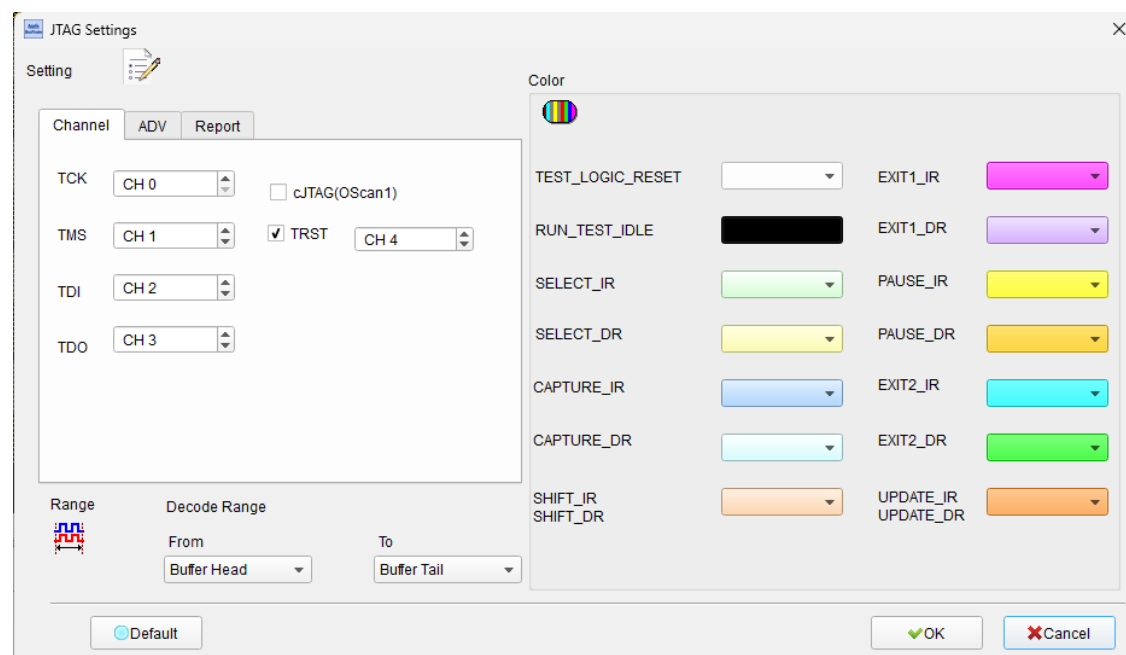
Default OK Cancel

JTAG

JTAG (Joint Test Action Group) is an international standard test protocol (IEEE 1149.1), mainly used for on-chip internal testing, and nowadays most advanced components support JTAG protocol, such as DSPs, FPGAs, etc. The standard JTAG consists of five signal interfaces: TCK, TMS, TDI, TDO and TRST, four of which are input signal interfaces and the other one is output signal interface.

The standard JTAG consists of five signal interfaces: TCK, TMS, TDI, TDO and TRST, four of which are input signal interfaces and the other one is an output signal interface. The basic principle is to define a TAP (Test Access Port) inside the device and test the internal nodes with a dedicated JTAG test tool.

Settings



Channel: Specify the channel number of the Logic Analyzer to be connected with the object to be tested, the TRST pin can be decided by the user, if you are going to use the function of interpreting commands, then the system will decide whether to use the TRST pin or not according to the data of the commands that you have selected, and the user can decide whether to turn on the cJTAG or not, if you turn on the cJTAG option, the TDI/TDO channels are displayed in If

cJTAG is enabled, the TDI/TDO channels will be grayed out, and the TCK/TMS channels will be treated as TCKC/TMSC channels in cJTAG OScan1 mode.

Advanced:

The screenshot shows the 'Report' tab in the Acute JTAG software. It features a table of JTAG instructions with columns for ID, Name, and Len. Below the table are controls for showing test data (TDI or TDO) and selecting the bit order (LSB or MSB).

ID	Name	Len
1 000	ARM7~ARM9	4
2 001	ARM10	4
3 002	ARM11	5
4 003	Xilinx	5

☐ Interpreter instruction
 Show the test data is
☐ Test Data Input (TDI)
☒ Test Data Output (TDO)
 Test Data Bit Order: LSB

I. Show the test data is: User can select the state of TAP state as Shift-IR, Shift-DR. TDI or TDO data will be displayed in hexadecimal.

II. Test Data Bit Order: The length of data may vary during data transmission by JTAG. Therefore, the user can specify whether the data is LSB First or MSB First when interpreting TDI/TDO.

III. Interpreter Instruction: If you open the Explain Command function, you will see a list of commands, and the JTAG protocol analyzer will display the commands in the Instruction register during Update-IR. Users can select "Edit..." function to add and modify the instruction list file (JtagInst.txt) by themselves using the editor. After finishing the modification, click "Refresh" again to update the instruction list.

IV. Acute Jtag Instruction table(JtagInst.txt): This file is provided by Jtag DLL, users can re-edit this file according to their own needs. We

also supports BSDL format, user can directly add the BSDL file, user can save the time of editing instruction data, please see the last appendix of this unit Acute Jtag Instruction table syntax description.

Report: To enable report filtering, simply check the items to be displayed in the report window.

Channel
ADV
Report

Show the state in the report

☒ Test-Logic-Reset
☒ Exit1-DR

☒ Run-Test/Idle
☒ Exit1-IR

☒ Select-DR-Scan
☒ Pause-DR

☒ Select-IR-Scan
☒ Pause-IR

☒ Capture-DR
☒ Exit2-DR

☒ Capture-IR
☒ Exit2-IR

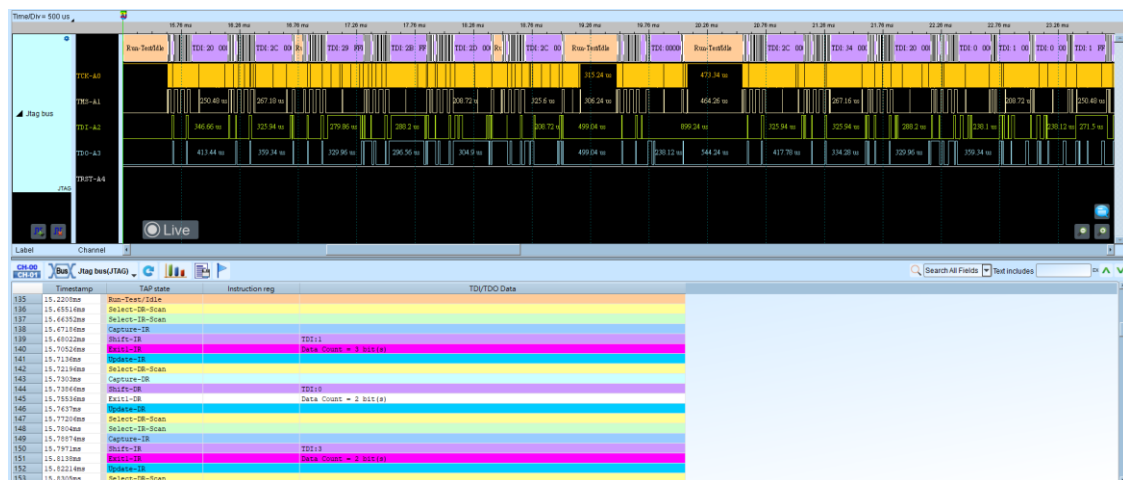
☒ Shift-DR
☒ Update-DR

☒ Shift-IR
☒ Update-IR

☒ Show TDI or TDO
☐ Show TDI and TDO

I. Show TDI or/and TDO: If choose “Show TDI and TDO”, the report area will show the TDI and TDO at the same time.

Result



Acute JTAG Instruction table Syntax Description (JtagInst.txt):

The numbers used in this file are hexadecimal.

##: is comment.

#ID: Command list number; the range is 00 - FF and , MUST be entered in order or will be seen as the end of commands.

#NAME: Command Name, 32 bytes most will be shown in the command list.

#LENGTH: Command length, unit in bits.

#CAPTURE: Command Capture Code, is stored in Instruction Register..

#INST: Command List, listed by Command Code and Command Name or will be seen as the end of commands..

#TRST: Enter 1 if TREST is needed or enter 0 or nothing if TREST is not needed.

#BSDL: Load the BSDL file. Use the BSDL file as step 1-6.

Example:#ID:00

#NAME:ARM7-ARM9

#LENGTH:4

#CAPTURE:1

#INST:0, EXTEST

#INST:2, SCAN_N

#INST:3, SAMPLE/PRELOAD

#INST:4, RESTART

#INST:5, CLAMP

#INST:7, HIGHZ

#INST:9, CLAMPZ

#INST:C, INTEST

#INST:E, IDCODE

#INST:F, BYPASS

#INST:

#ID:01

#BSDL:C:\3256at144_1532.bsd

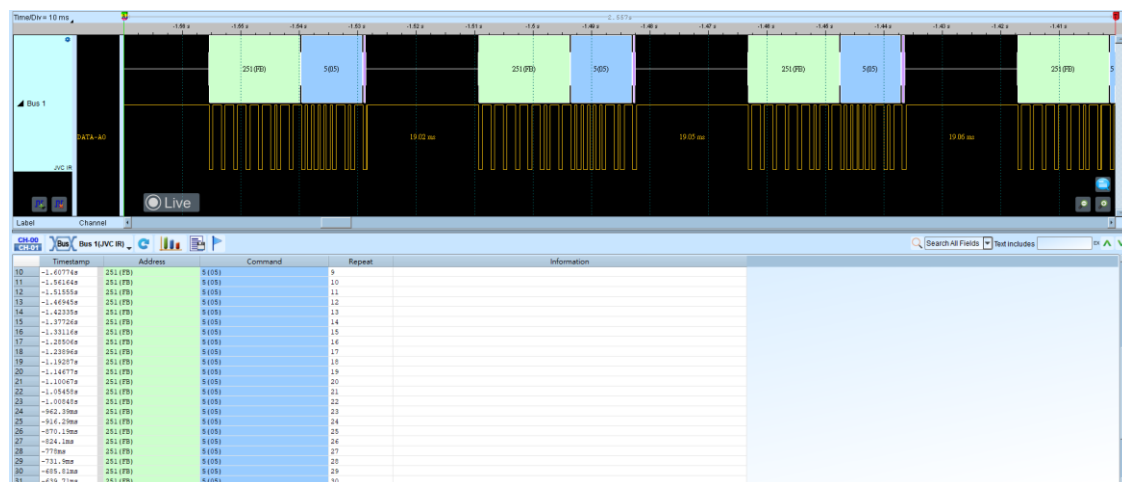
JVC IR

JVC IR refers to products or systems related to infrared (IR) technology introduced by JVC (Japan Victor Company).

Settings

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Result



LCD1602

The Liquid Crystal Display 1602 (LCD1602) bus has 11 data bits:

Instruction/Data Register Select (RS), Read/Write Select (RW), Enable Select (E) and 8 bits or 4 bits Data Input/Output lines (DB0~DB7/DB0~DB3).

Settings

LCD1602 Ver.1.0 Settings

Parameters

Channel

RS	A0	DB0	A3	DB4	A7
RW	A1	DB1	A4	DB5	A8
E	A2	DB2	A5	DB6	A9
		DB3	A6	DB7	A10

Data Mode

☒ 8 Lines ☐ 4 Lines

☒ To merge the same command

Color

SCREEN CLEAR: [Yellow]

CURSOR RETURN: [Cyan]

INPUT SET: [Purple]

DISPLAY SWITCH: [Magenta]

SHIFT: [Yellow]

BUSY/AD READ CT: [Light Green]

CGRAM AD SET: [Red]

DDRAM AD SET: [Orange]

FUNCTION SET: [Cyan]

DATA WRITE: [Blue]

DATA READ: [Yellow]

Range

Decode Range

From: [Buffer Head] To: [Buffer Tail]

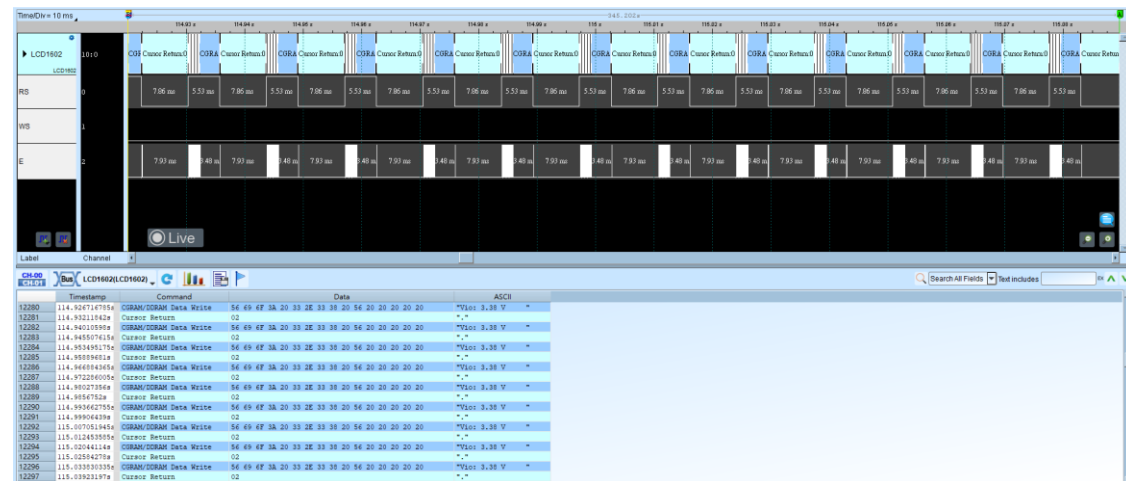
☐ Default

Channel: Show the selected channels (RS: CH0, RW: CH1,..., DB0: CH10).

Data Mode: 8 lines or 4 lines.

To merge the same command: Merge data with its command.

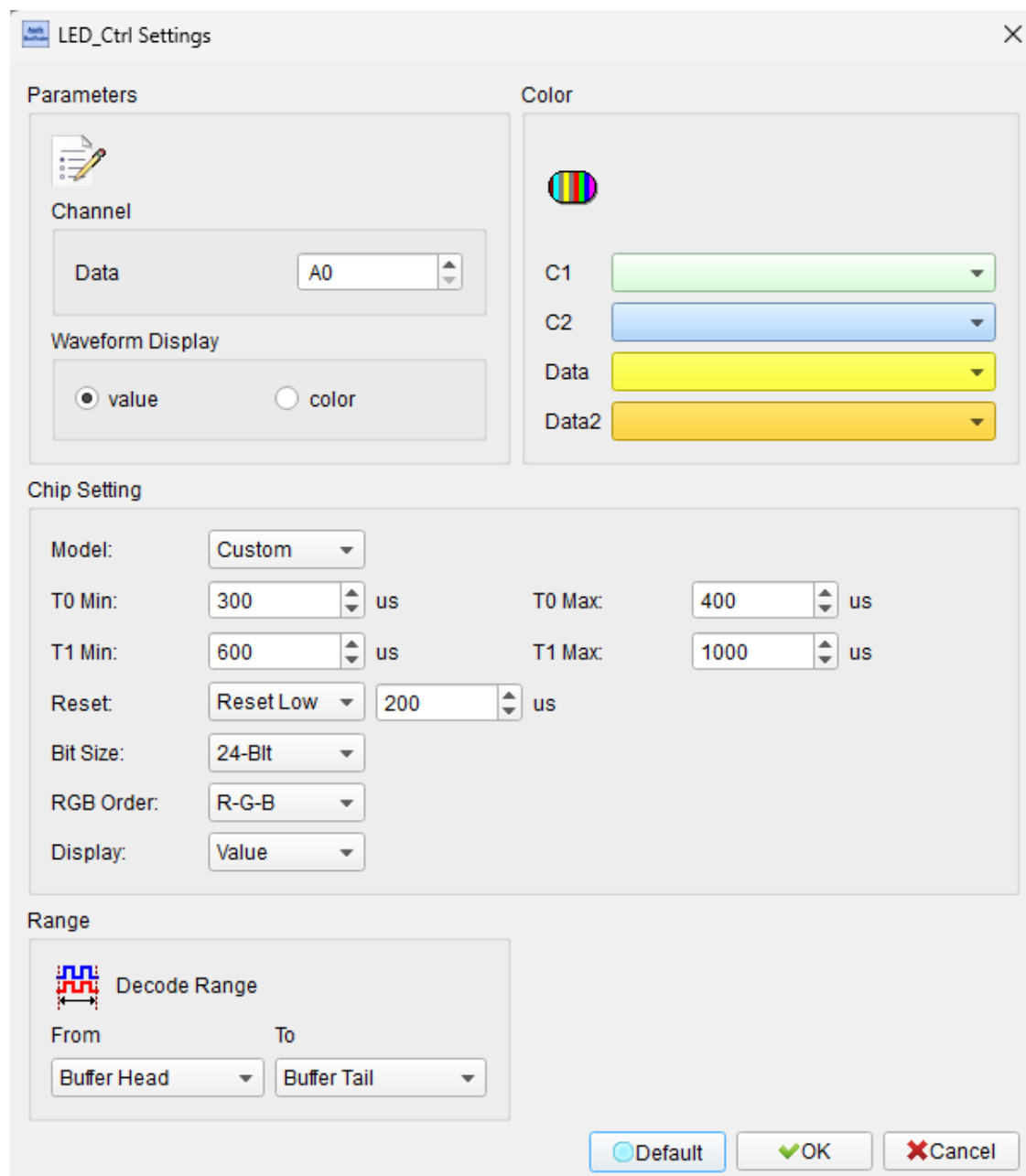
Result



LED_Ctrl

LED Controls are made specifically for digital type LEDs. These LEDs contain a special IC chips that allow the user to control each LED or section of LEDs.

Settings



The LED_Ctrl Settings dialog box is divided into several sections:

- Parameters:**
 - Channel:** A dropdown menu showing "Data" and a text box with "A0".
 - Waveform Display:** Two radio buttons, "value" (selected) and "color".
- Color:**
 - A color selection icon (rainbow bar).
 - Four color bars with dropdown arrows: C1 (green), C2 (blue), Data (yellow), and Data2 (orange).
- Chip Setting:**
 - Model:** A dropdown menu showing "Custom".
 - T0 Min:** A text box with "300" and a unit dropdown with "us".
 - T0 Max:** A text box with "400" and a unit dropdown with "us".
 - T1 Min:** A text box with "600" and a unit dropdown with "us".
 - T1 Max:** A text box with "1000" and a unit dropdown with "us".
 - Reset:** A dropdown menu showing "Reset Low" and a text box with "200" and a unit dropdown with "us".
 - Bit Size:** A dropdown menu showing "24-Bit".
 - RGB Order:** A dropdown menu showing "R-G-B".
 - Display:** A dropdown menu showing "Value".
- Range:**
 - A waveform icon and the text "Decode Range".
 - From:** A dropdown menu showing "Buffer Head".
 - To:** A dropdown menu showing "Buffer Tail".

At the bottom right, there are three buttons: "Default" (with a blue circle icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

Channel: Show the selected channels.

Waveform display: show value or RGB color in waveform area.

Chip setting:

Model: User can select the IC model. We now support TM1814 、WS2811 、WS2812 、RT7905 、HZ0028 and Custom 。

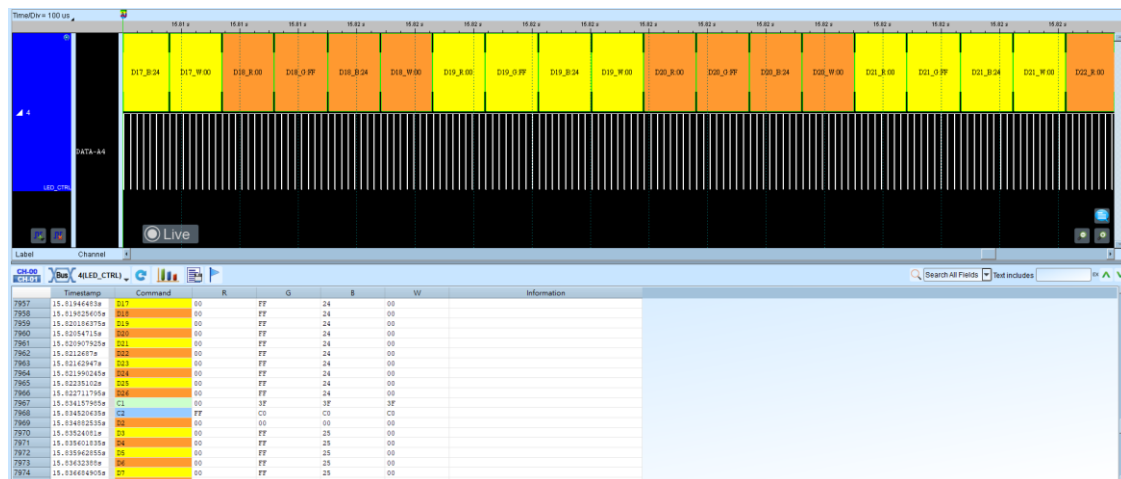
Condition: Idle high

If the time that waveform goes to low between T0 min and T0 max, the bit will decode as zero. If it's between T1 min and T1 max, the bit will decode as one.

Reset: if the waveform keeps at high potential over the time, the decoder will reset the start bit.

Bit size: choose 32-bit (WRGB) or 24-bit (RGB).

Result



LIN

LIN (Local Interconnect Network) is a serial network protocol used for communication between components in vehicles. LIN may be used also over the vehicle's battery power-line with a special LIN over DC powerline (DC-LIN) transceiver.

Settings

LA Channel: Show the selected channel.

Show Scale: It will show the scales according to the bit width on the waveform.
Enabled when checked.

Import LDF File: Enable users to import the LIN Description File. Click on Add

and select LDF file.

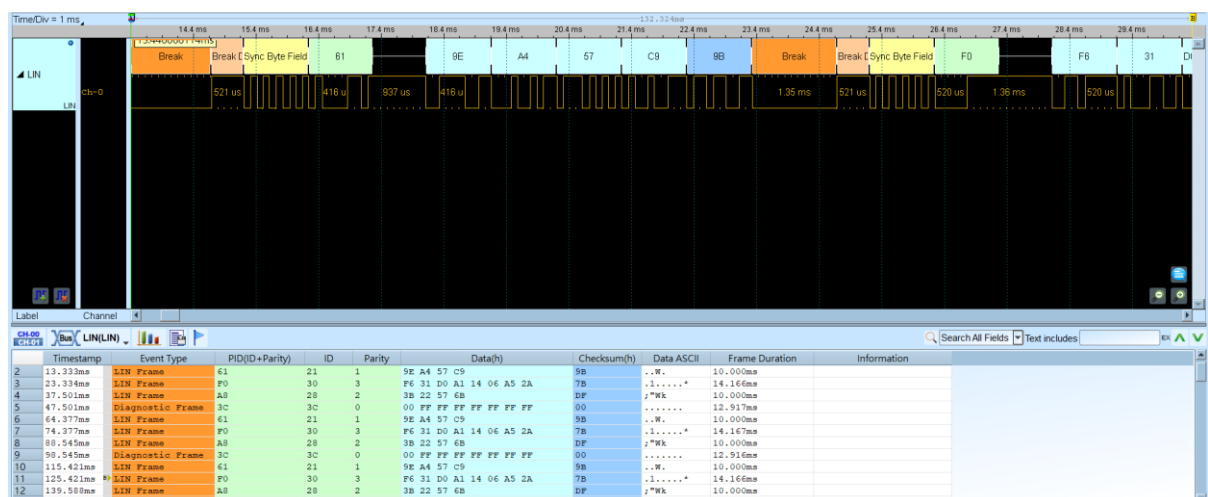
Version: Different versions can be selected for LIN analysis. The Checksum verification after Lin version 2.0 has changed to two modes. If user need to use the enhanced verification below, user should select the version after 2.0 to use it.

Baud rate: Show the selected baud rate.

Checksum Mode: Select the proper baud rate of the signal before the analysis.

When set to auto, it will automatically detect the baud rate that matches the signal to be analyzed.

Result



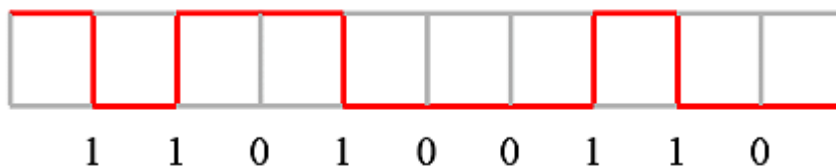
The decoder with LDF



Line Decoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

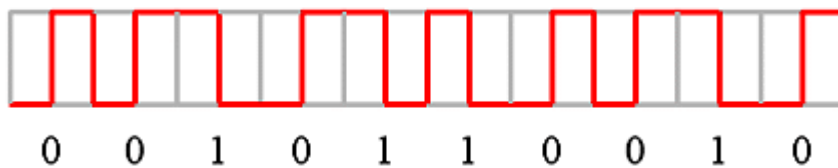


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.

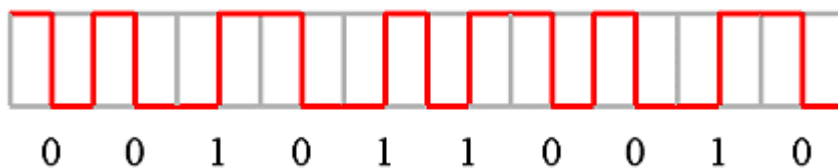


Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.

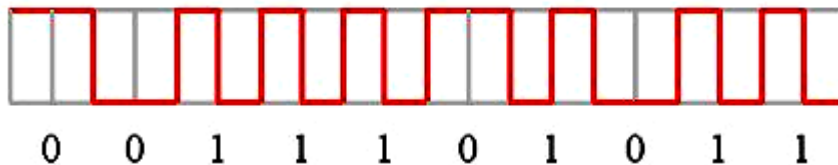


Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit's signal i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.



Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions which makes clock recovery and synchronization difficult.

When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that together form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

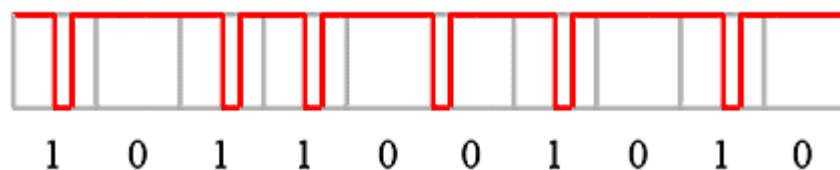
Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.



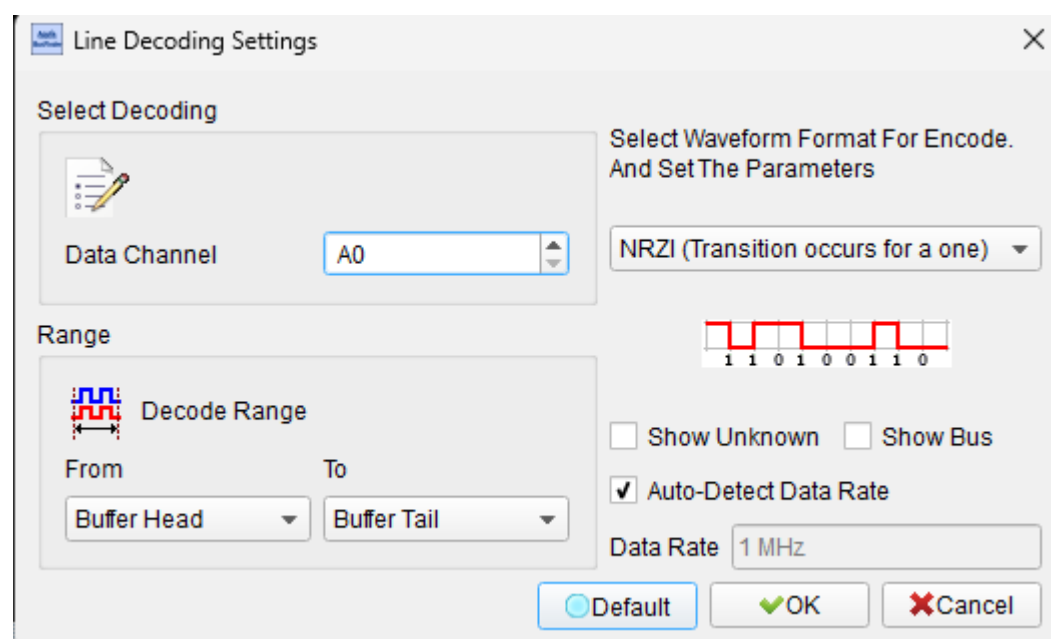
Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation

data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit.

This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Decoding: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Select the line code that user want to decode:

- I. NRZI (Transition occurs for a one)
- II. NRZI (Transition occurs for a zero)
- III. Manchester (Thomas)

IV. Manchester (IEEE802.3)

V. Differential Manchester

VI. Biphase Mark Decode

VII. Miller

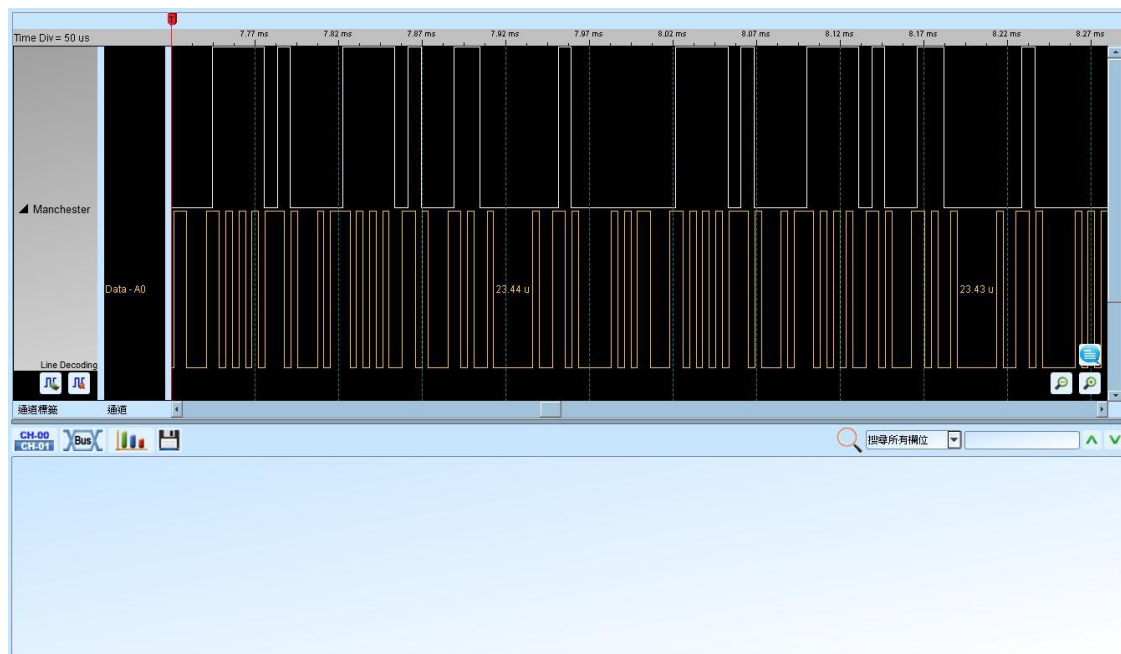
VIII. Modified Miller

Show Unknown: Display unknown data.

Show Bus: Display bus data.

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Data Rate is not selected.

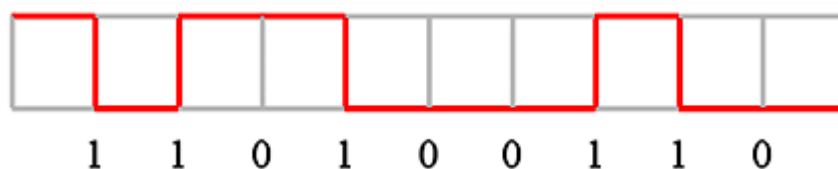
Result



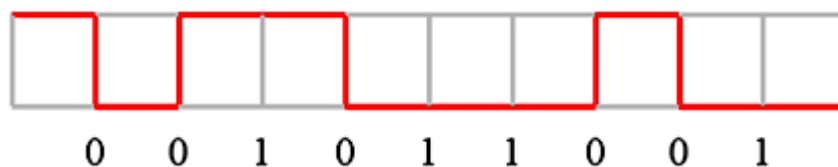
Line Encoding

NRZI (Non return to zero, inverted): Non return to zero, inverted (NRZI) is a method of mapping a binary signal to a physical signal for transmission over some transmission media. The two level NRZI signal has a transition at a clock boundary if the bit being transmitted is a logical one, and does not have a transition if the bit being transmitted is a logical zero. There are two modes:

NRZI (Transition occurs for a one): A 1 is represented by a transition of the physical level, a 0 has no transition.

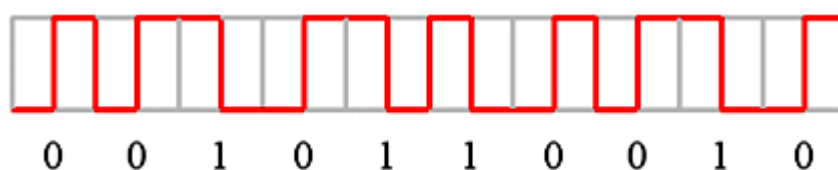


NRZI (Transition occurs for a zero): A 0 is represented by a transition of the physical level, a 1 has no transition.



Manchester: In telecommunication, Manchester code is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It is, therefore, self-clocking, which means that a clock signal can be recovered from the encoded data. There are three modes:

Manchester (Thomas): A 0 is expressed by a low-to-high transition, a 1 by high-to-low transition.



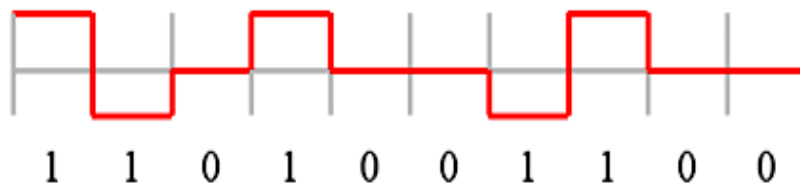
Manchester (IEEE802.3): A 1 is expressed by a low-to-high transition, a 0 by high-to-low transition.



Differential Manchester: A 1 bit is indicated by making the first half of the signal equal to the last half of the previous bit, i.e. no transition at the start of the bit-time. A '0' bit is indicated by making the first half of the signal opposite to the last half of the previous bit's signal i.e. a zero bit is indicated by a transition at the beginning of the bit-time. In the middle of the bit-time there is always a transition, whether from high to low, or low to high. A reversed scheme is possible, and no advantage is given by using either scheme.

AMI (Alternate Mark Inversion): There are four modes:

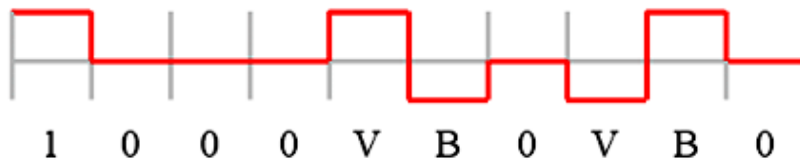
AMI (Standard): AMI (Alternate Mark Inversion) is a synchronous clock encoding technique that uses bipolar pulses to represent logical 1 value. It is therefore a three level system. A logical 0s is represented by no symbol, and a logical 1 is represented by alternating-polarity pulses.



AMI (B8ZS): Bipolar-8-Zero Substitution

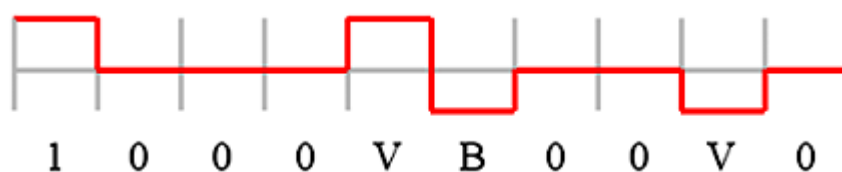
If 1 is +, 00000000 is represented to 000+-0-+

1 is -, 00000000 is represented to 000-+0+-



AMI (HDB3): High Density Bipolar 3

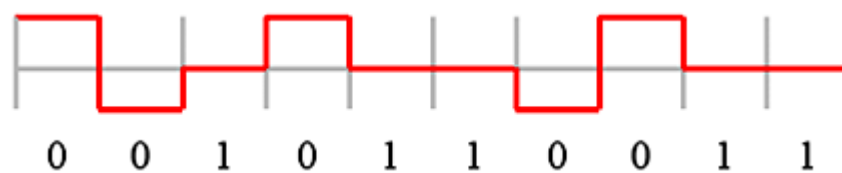
The HDB3 code is a bipolar signaling technique (i.e. relies on the transmission of both positive and negative pulses). It is based on Alternate Mark Inversion (AMI), but extends this by inserting violation codes whenever there is a run of 4 or more 0's. This and similar (more complex) codes have replaced AMI in modern distribution networks. The encoding rules follow those for AMI, except that sequences of four consecutive 0's are encoding using a special "violation" bit. This bit has the same polarity as the last 1-bit which was sent using the AMI encoding rule. The purpose of this is to prevent long runs of 0's in the data stream that may otherwise prevent a DPLL from tracking the center of each bit. Such a code is sometimes called a "run length limited" code, since it limits the runs of 0's that would otherwise be produced by AMI. One refinement is necessary, to prevent a dc voltage being introduced by excessive runs of zeros. This refinement is to encode any pattern of more than four bits as B00V, where B is a balancing pulse. The value of B is assigned as + or -, so as to make alternate "V"s of opposite polarity. The receiver removes all Violation pulses, but in addition a violation preceded by two zeros and a pulse is treated as the "B00V" pattern and both the violation and balancing pulse are removed from the received bit stream. This restores the original bit stream.



MLT-3: Multilevel Transmission 3: A 0 means no transition happens, a 1 is represented by a transition (0, +, 0, -).



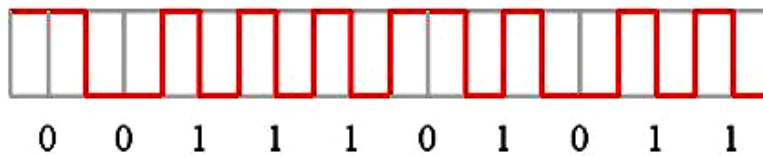
Pseudoternary: A 1 is always zero, a 0 is represented by a transition (+, -).



CMI (Coded Mark Inversion): A zero is sent as a low to high [01] transition, while a one is sent as either a one [1] or zero [0] depending on the previous state. If the previous state was high the one is sent as a zero [0], if it was low the one is sent as a one [1].



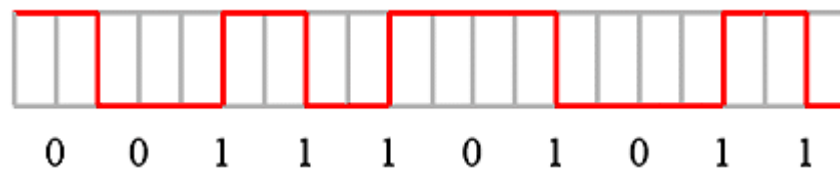
Bi-phase Mark: The bi-phase mark code (also called FM1 code) is a type of encoding for binary data streams. When a binary data stream is sent without modification via a channel, there can be long series of logical ones or zeros without any transitions that make clock recovery and synchronization difficult. When encoding, the symbol rate must be twice the bitrate of the original signal. Every bit of the original data is represented as two logical states that form a bit.



Miller: Delay encoding is also known as Miller encoding.

In telecommunications, delay encoding is the encoding of binary data to form a two-level signal such that (a) a "0" causes no change of signal level unless it is followed by another "0" in which case a transition to the other level takes place at the end of the first bit period; and (b) a "1" causes a transition from one level to the other in the middle of the bit period.

Delay encoding is used primarily for encoding radio signals because the frequency spectrum of the encoded signal contains less low-frequency energy than a conventional non-return-to-zero (NRZ) signal and less high-frequency energy than a bi-phase signal.

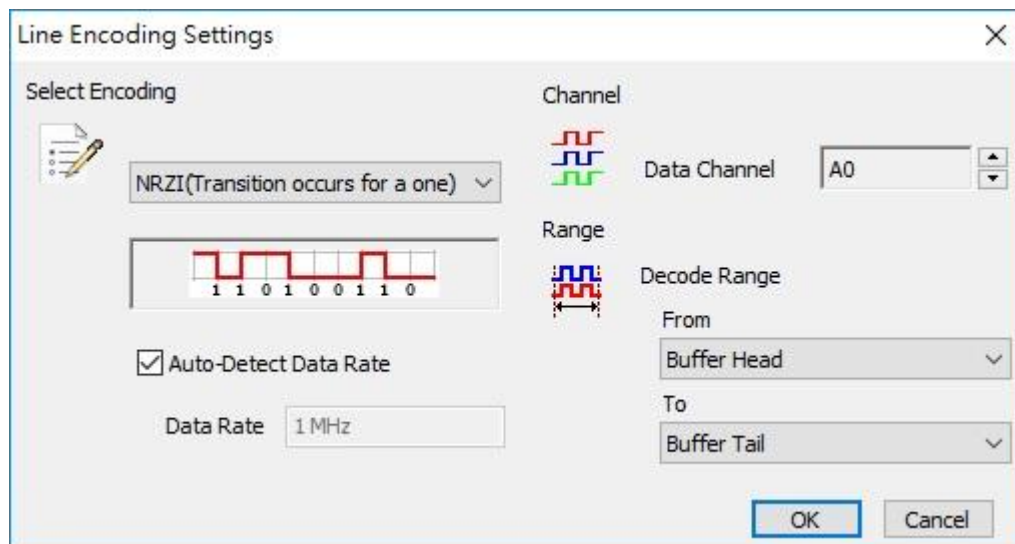


Modified Miller: The Modified Miller (M 2) demodulator facilitates demodulation of M 2 modulation data to NRZ-L (non-return-to-zero-level) data, composed of a data separation circuit for producing synchronizing clock pulses from the M 2 modulation data which is reproduced by a data recording device and separating the M 2 modulation data into clock bits and data bits, and an M 2 modulation data demodulation circuit for producing NRZ - L data by utilizing the clock bits, data bits and synchronizing clock pulses which are output from the data separation circuit.

This structure enables the M 2 modulation data which is input to the M 2 demodulation circuit to be easily demodulated to an NRZ - L type data signal by means of a very simple circuit structure. An example is as below:



Settings



Select Encoding: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Select the line code you want to encode:

- I. NRZI (Transition occurs for a one)
- II. NRZI (Transition occurs for a zero)
- III. Manchester (Thomas)
- IV. Manchester (IEEE802.3)
- V. Differential Manchester
- VI. AMI (Standard)
- VII. AMI (B8ZS)

VIII. AMI (HDB3)

IX. Pseudoternary

X. MLT-3

XI. CMI

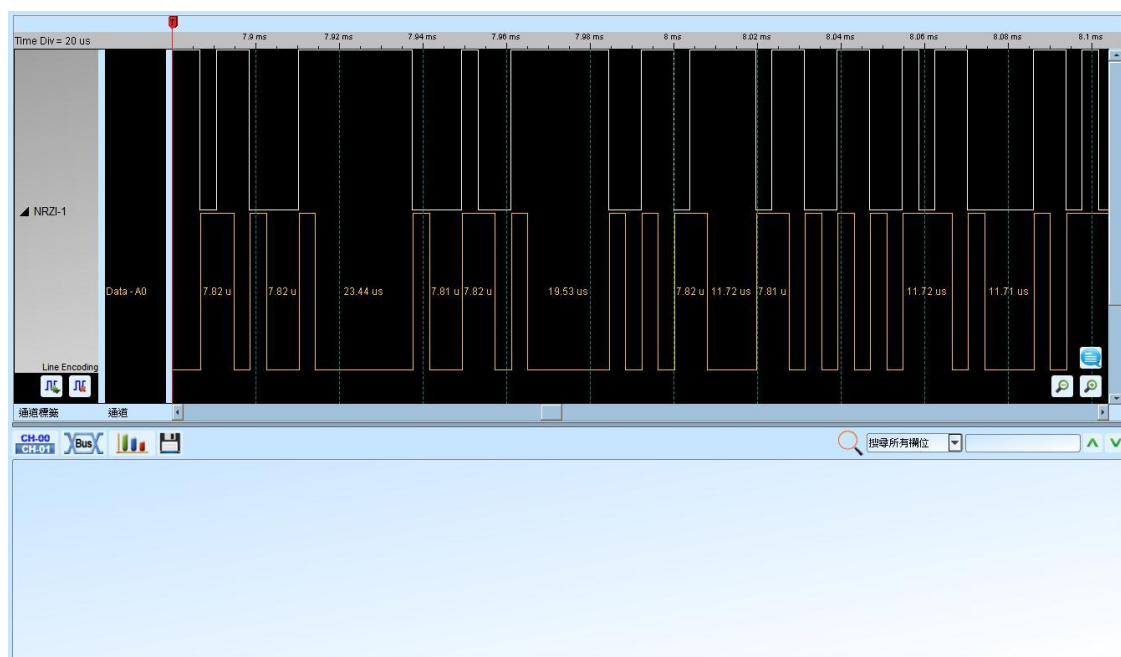
XII. Biphas Mark Encode

XIII. Miller

XIV. Modified Miller

Auto-Detect Data Rate: Enter the Data Rate manually if the Auto-Detect Data Rate is not selected.

Result



LPC

The LPC bus, for the data transmissions, was developed by Intel to replace the ISA bus.

Settings

LPC Settings

Setting

LFRAME# A1 LAD[2] A4 LCLK A0

LAD[0] A2 LAD[3] A5 Data Edge Rising

LAD[1] A3

Show the field in report

- ☒ START
- ☒ CYCLETYP+DIR
- ☒ SIZE
- ☒ TAR
- ☒ ADDR
- ☒ CHANNEL
- ☒ DATA
- ☒ SYNC
- ☒ STOP

Color

START ADDR

CYCLETYP+DIR DATA

CHANNEL SYNC

TAR IDSEL

SIZE/MSIZE STOP

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

LCLK: Transfer clock of LPC.

Data Edge: Latch the data to be analyzed when the LCLK is rising or falling.

LFRAME#: Marks the start of each Frame transfer cycle or is used to interrupt

LPT

LPT is a universal parallel interface that use in PC since 1980's. It was primarily designed to operate a line printer, but could also be used to adapt other peripherals. This decode only support EPP Mode.

Settings

LPT(EPP) Setting

Channel

Data0(LSB) CH 0

Data[7:0] => [CH 7: CH 0]

/nWrite CH 8

/nWait CH 9

/nDStrb CH 10

/nAStrb CH 11

☐ /nInit CH 0

☐ /nIntr CH 0

☐ Address Table Report

Color

Read Address

Write Address

Read Data

Write Data

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Data0(LSB): There are 8 data channel. Only set Data0(LSB) here, other channel will be set automatically.

/nWrite: Indicates the direction of transfer.

/nWait: To acknowledge that a transfer has finished.

/nDStrb: Indicates the data cycle.

/nAStrb: Indicates the address cycle.

/nInit: Indicates a termination cycle in order to return the interface to the

LTPI

LTPI (LVDS Tunneling Protocol & Interface) is an interface protocol designed for transmitting low-speed signals between the HPM (Host Processor Module) and SCM (Server Control Module). It supports multiple channels such as GPIO, I2C/SMBus, and UART, utilizing time-division multiplexing (TDM) over LVDS links to achieve multi-channel transmission. The GPIO channel includes both low-latency and normal-latency types. The I2C/SMBus channel handles single-controller communication links. The UART channel supports flow control. Additionally, an OEM channel is provided for proprietary interfaces, and a data channel supports memory image data transfers

Parameters

Tx Clock: Transfer Clock of Tx.

Tx Data: Transfer Data of Tx

Rx Clock: Transfer Clock of Rx

Rx Data: Transfer Data of Tx

SDR: The transmission method is SDR ◦

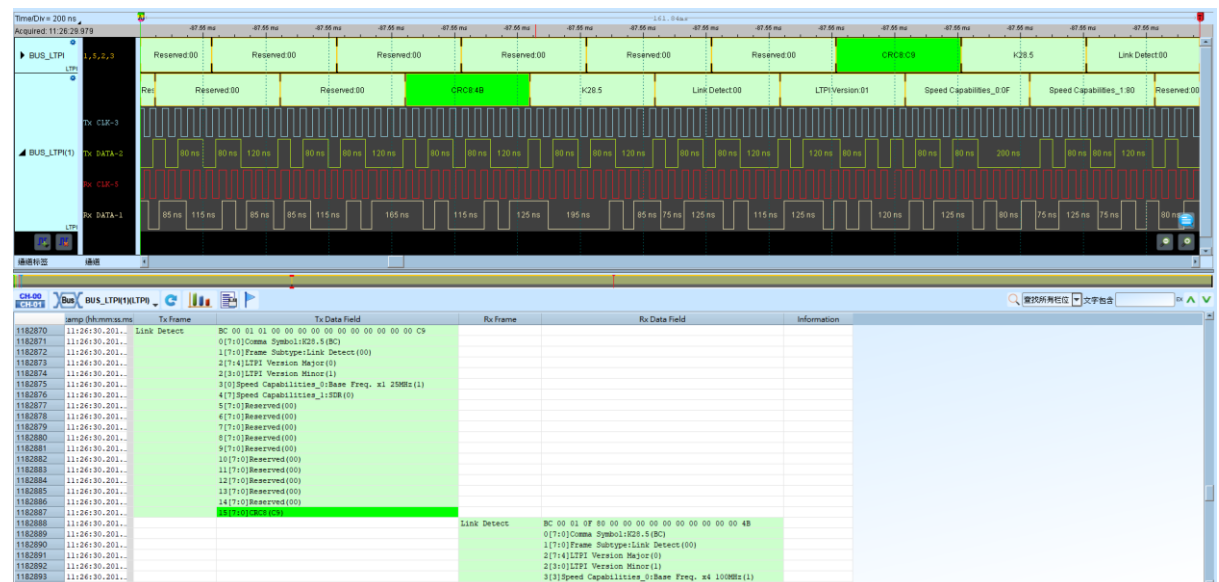
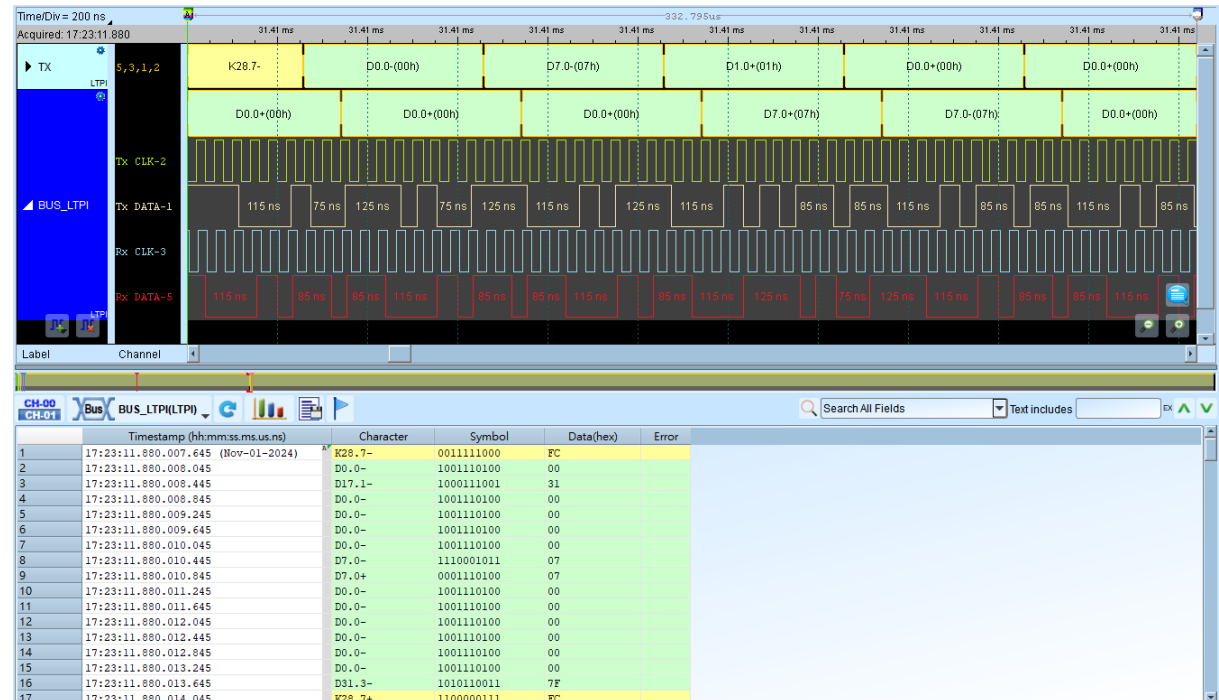
DDR: The transmission method is DDR ◦

Waveform: The direction (Transmit / Receive) and decoded content displayed in the waveform area (8b10b / LTPI / GPIO / UART / I2C)

Detail Report: Whether to enable detailed reporting

Import GPIO CSV: Whether to import the GPIO bit name

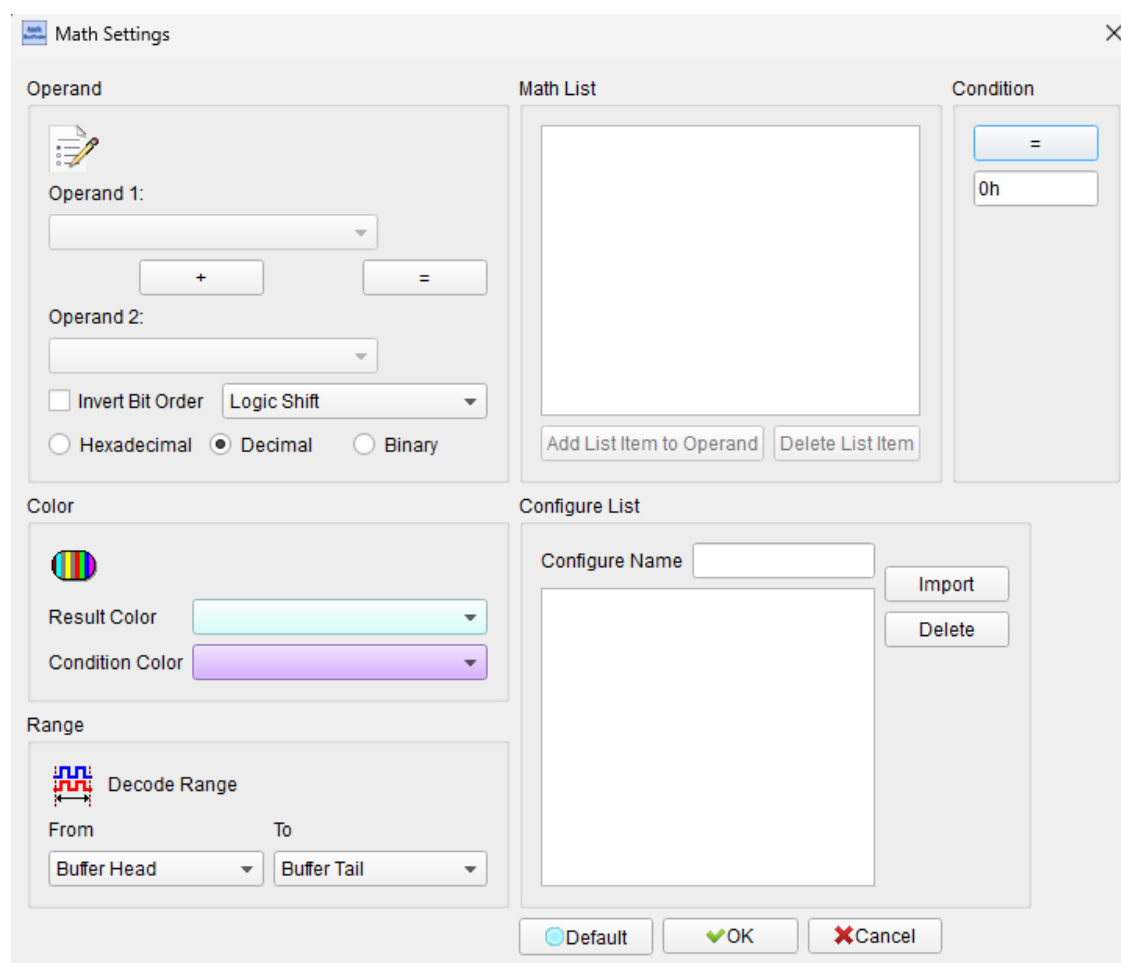
Result



Math

Math is used to conduct addition, subtraction, multiplication, division, AND, XOR, OR, NAND, NOR, XNOR, Bit Shift operation for the combined value of channel or bus.

Parameters Settings



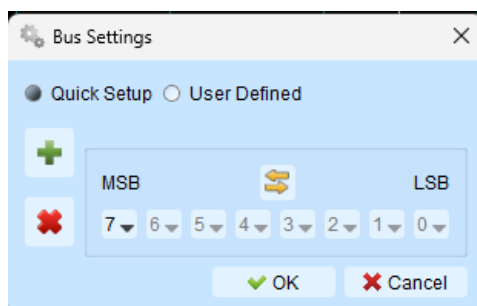
The **Math Settings** dialog box is used to configure mathematical operations. It includes sections for Operand, Math List, Condition, Color, and Range.

- Operand:** Contains dropdowns for Operand 1 and Operand 2, a plus sign (+) button, an equals sign (=) button, a checkbox for **Invert Bit Order**, a **Logic Shift** dropdown, and radio buttons for **Hexadecimal**, **Decimal** (selected), and **Binary**.
- Math List:** A large empty box for listing mathematical operations, with **Add List Item to Operand** and **Delete List Item** buttons below it.
- Condition:** Includes an equals sign (=) button and a text input field containing **0h**.
- Color:** Includes a color selection icon, **Result Color** (light blue), and **Condition Color** (purple).
- Range:** Includes a **Decode Range** icon, **From** and **To** dropdowns (both set to **Buffer Head** and **Buffer Tail** respectively).
- Configure List:** Includes a **Configure Name** text input, **Import** and **Delete** buttons, and a large empty box for the list.
- Buttons:** **Default** (with a blue circle icon), **OK** (with a green checkmark icon), and **Cancel** (with a red X icon).

1. Channels Settings

- i. **Operand:** The channel or bus for which the calculation is to be performed is automatically listed with the labeled name of the channel or bus in the current waveform window.

- ii. **Operator: We support**
 - 1. **Arithmetic operator:** + 、 - 、 × 、 /
 - 2. **Logic operator:** AND 、 XOR 、 OR 、 NAND 、 NOR 、 XNOR 、 >> 、 <<
- iii. **「=」 button: Add the equation to the Math List**
- iv. **Invert Bit Order: By default, when adding a new bus, the smaller channel number is lsb and the larger channel number is msb. Users can reverse the order of lsb and msb by setting this option.**



- v. **Bit Shift Method: We support (i)Arithmetic Shift 、 (ii)Logic Shift 、 (iii) Rotate Circular Shift and (iv)Rotate through Carry Shift. Use with >> and << in logical operators.**
- vi. **Numeric Display: We support Hexadecimal 、 Decimal 、 Binary.**
- vii. **Math List: Displaying the equations added by the user, up to a limit of 8.**
- viii. **「Add List Item to Operand」 button: Adding the selected item from *Math List* to operand for user to select for further operating with other channel or bus. Those item that was added to operand is enclosed in a set of parentheses when it operates with other operand. Up 2 levels of parentheses are supported.**
- ix. **「Delete List Item」 button: Deleting the selected item from *Math List*.**

2. Waveform Settings:

- i. **Setting the color of frame that represents the calculated result.**
- ii. **Setting the comparison condition and the frame color that matches the condition.**

3. Case Settings:

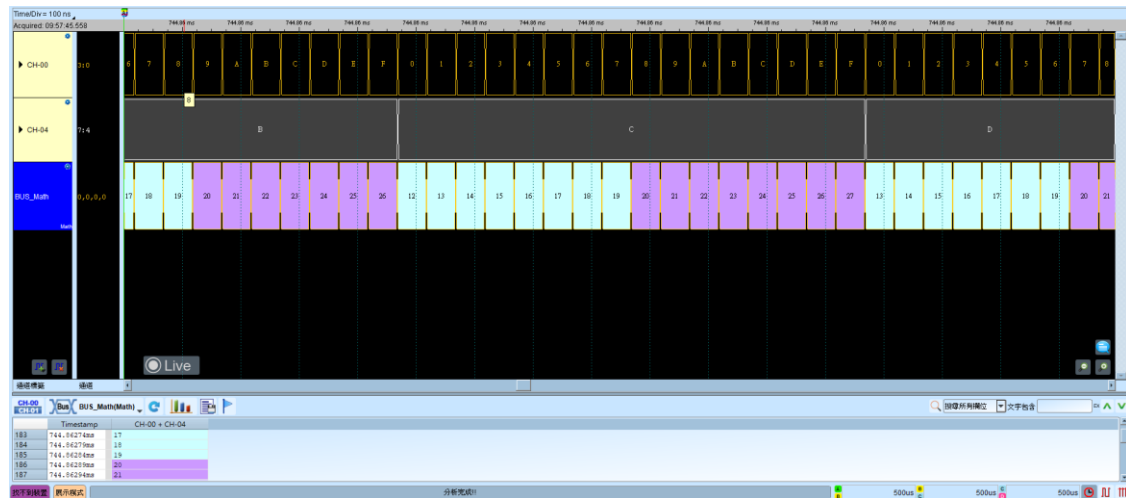
- i. **Comparison Condition: We support \geq 、 $>$ 、 $=$ 、 \leq 、 $<$.**
- ii. **Comparison Value: Entering the value of the condition to be compared. Supports hexadecimal and decimal representation.**

4. Configure: Lists all the configure names so that users can quickly switch between different configures. The configure records a list of different equations.

Operating Methods

- 1. After selecting the operand and operator, click “=” to add the equation to the *Math List*.**
- 2. Choosing the equations to be operated on.**
- 3. Setting the color of frame that represents the calculated result.**
- 4. Setting the comparison condition and entering the comparison value, also setting the color for displaying the matches frame.**

Result



Note: After setting, press OK to write all the settings to a file and save it to the working directory (AqMath.bin). The file will be overwritten every time user press OK, so when user save the file, user need to save a copy of AqMath.bin in addition to the waveform file. When user open the waveform file, user need to place AqMath.bin in the working directory before opening the waveform file.

M-Bus

M-Bus (Meter-Bus) is for remote reading of heat meters and other types of consumption meters.

Settings

MBus Settings

Channel

Channel

Master: A0

Polarity: Auto

☐ Slave: A1

Polarity: Idle Low

☒ Auto Detect

Baud Rate: 9600

Detail

Parity: None

☐ MSB First

☐ Adv. Report

Color

Start / Stop: [Orange]

CI Field: [Cyan]

L Field: [Orange]

Data: [Blue]

C Field: [Yellow]

Check Sum: [Purple]

A Field: [Green]

Range

Decode Range

From: Buffer Head

To: Buffer Tail

Default OK Cancel

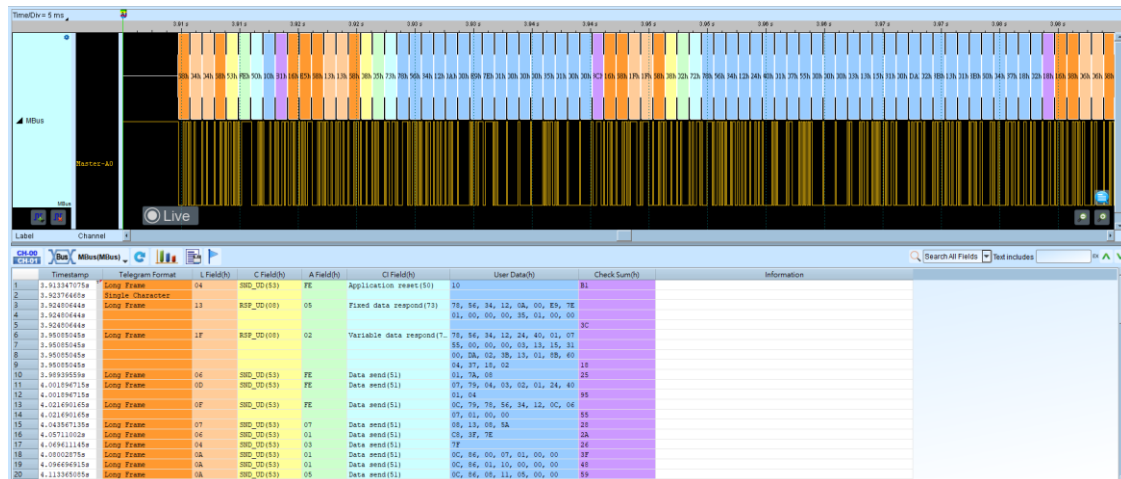
Channel: Set the signal channel and polarity. If there is a Slave on the bus, user can set up additional Slave channels. Enable when checked.

Baud Rate: The transmission speed of the signal. Checking Auto Detection will detect the baud rate by itself.

Detail:

- I. **Parity:** Parity error detect.
- II. **MSB First:** Displayed in MSB first format. Enabled when checked.
- III. **Adv. Report:** Advanced report. Enabled when checked.

Result



MCTP over I²C

MCTP (Management Component Transport Protocol) over I²C is a transport binding that enables communication between management controllers and other components in a system using I²C as the physical layer.

MCTP is a transport-independent protocol, meaning it can work over various underlying buses like PCIe, SMBus/I²C, UART, and Ethernet. When MCTP operates over I²C/SMBus, it follows the I²C/SMBus protocol for message passing between MCTP endpoints.

Settings:

MCTP over I²C Settings

Channel

SCL A0

SDA A1

Destination Address Configuration ...

Advanced Decode Setting

- ☐ Control
- ☐ PLDM
- ☐ NCSI
- ☐ Ethernet

Color

DestinationAddress NVME

MCTP SPD

Control Vendor PCI

PLDM Vendor IANA

NCSI Message

Ethernet

Range

Decode Range

From To

Buffer Head Buffer Tail

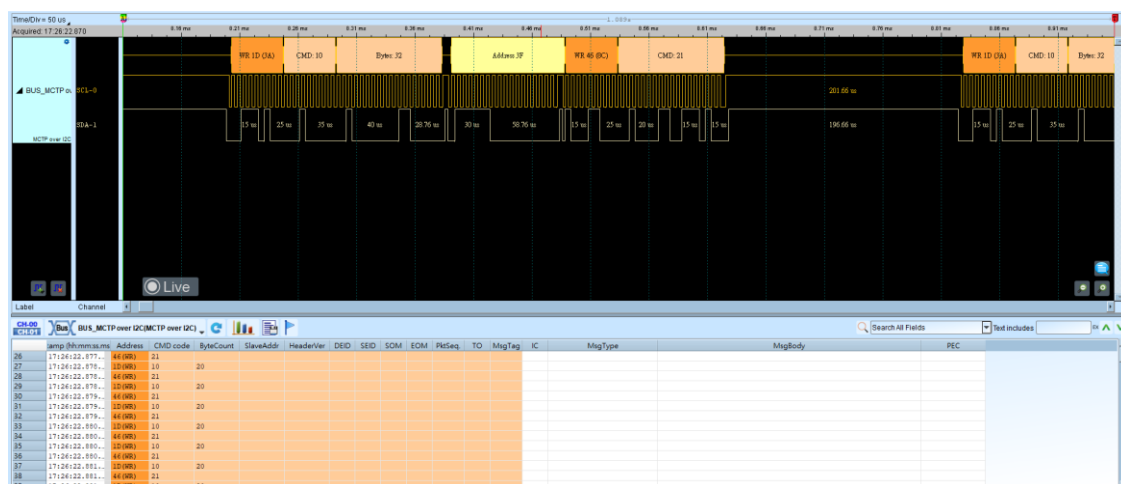
Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Destination Address Configuration: Set the device address and its corresponding protocol.

Advanced Decode Setting: Show the detail meaning of the raw data.

Result:



MCTP over I3C

MCTP (Management Component Transport Protocol) over I3C is a transport binding that enables standardized communication between system management controllers and peripherals using the MIPI I3C (Improved Inter-Integrated Circuit) bus.

MCTP is a transport-agnostic protocol, meaning it can operate over various physical layers like PCIe, SMBus/I²C, UART, and Ethernet. When using I3C, MCTP benefits from its higher speed, dynamic addressing, and in-band interrupt support, making it a more efficient alternative to I²C/SMBus.

Settings:

MCTP over I3C Settings

Channel

SCL A0

SDA A1

Destination Address Configuration ...

Advanced Decode Setting

- ☐ Control
- ☐ PLDM
- ☐ NCSI
- ☐ Ethernet

Color

DestinationAddress NVME

MCTP SPDM

Control

PLDM Vendor PCI

NCSI Vendor IANA

Ethernet Message

Range

Decode Range

From To

Buffer Head Buffer Tail

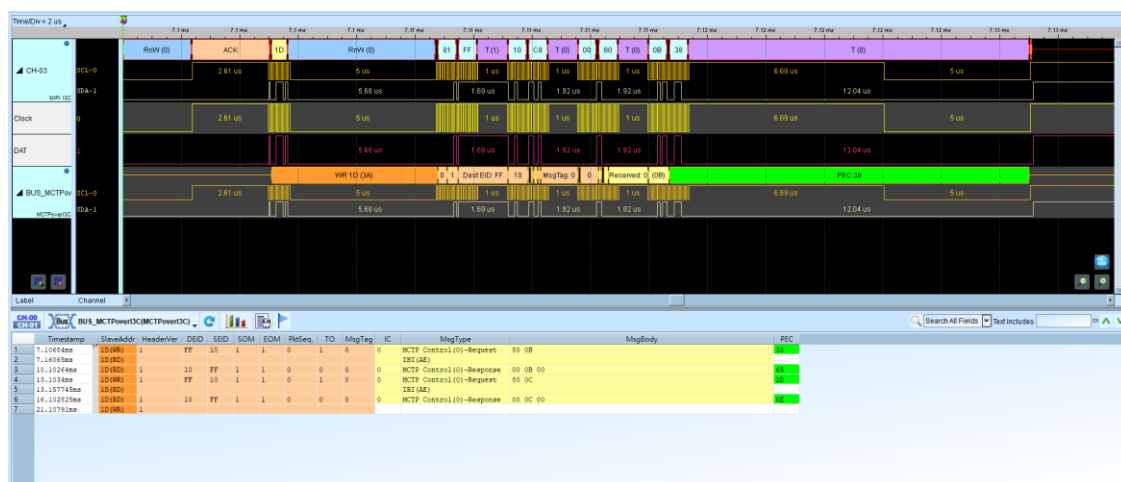
Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Destination Address Configuration: Set the device address and its corresponding protocol.

Advanced Decode Setting: Show the detail meaning of the raw data.

Result:



MCTP over SMBus

MCTP (Management Component Transport Protocol) over SMBus is a transport binding that enables communication between management controllers and other components in a system using SMBus as the physical layer.

MCTP is a transport-independent protocol, meaning it can work over various underlying buses like PCIe, SMBus/I²C, UART, and Ethernet. When MCTP operates over I²C/SMBus, it follows the I²C/SMBus protocol for message passing between MCTP endpoints.

Settings:

MCTP over SMBus Settings

Channel

SCL A0

SDA A1

Destination Address Configuration ...

Advanced Decode Setting

☐ Control

☐ PLDM

Color

DestinationAddress NVME

MCTP SPDM

Control

PLDM Vendor PCI

NCSI Vendor IANA

Ethernet Message

Range

Decode Range

From To

Buffer Head Buffer Tail

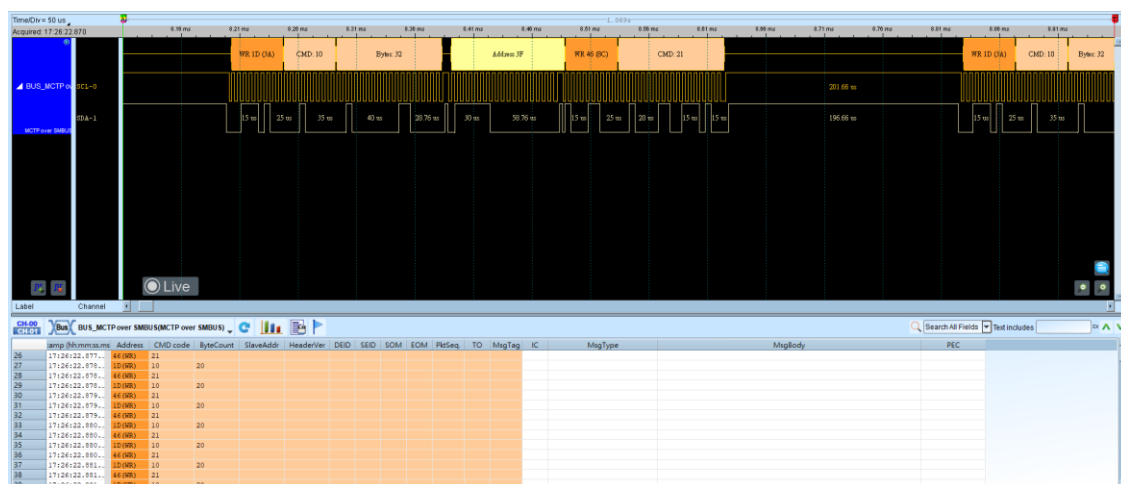
Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Destination Address Configuration: Set the device address and its corresponding protocol.

Advanced Decode Setting: Show the detail meaning of the raw data.

Result:



Mobile Display Digital Interface (MDDI)

The Mobile Display Digital Interface (MDDI) is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link for connecting portable computing, communication, and entertainment devices to wearable micro displays. This decoder is based on VESA Mobile Display Digital Interface Standard Version 1.2, only Type I communication is supported in this decoder.

Settings

MDDI Settings

Channel

Channel icon: ☐ MDDI STB: A0 ☒ MDDI D0 + A0 ☐ MDDI D0 - A0

Color

Color bar icon: Packet Length: [Yellow] Packet Header: [Green] Packet Data: [Cyan]

Range

Decode Range icon: From: Buffer Head To: Buffer Tail

Buttons: Default OK Cancel

Channel Settings

MDDI STB: MDDI Strobe

MDDI D0+/-: MDDI Data 0 +/-

Configure the Channel setup for the decoder, and choose the data source from Data 0+ or Data 0-.

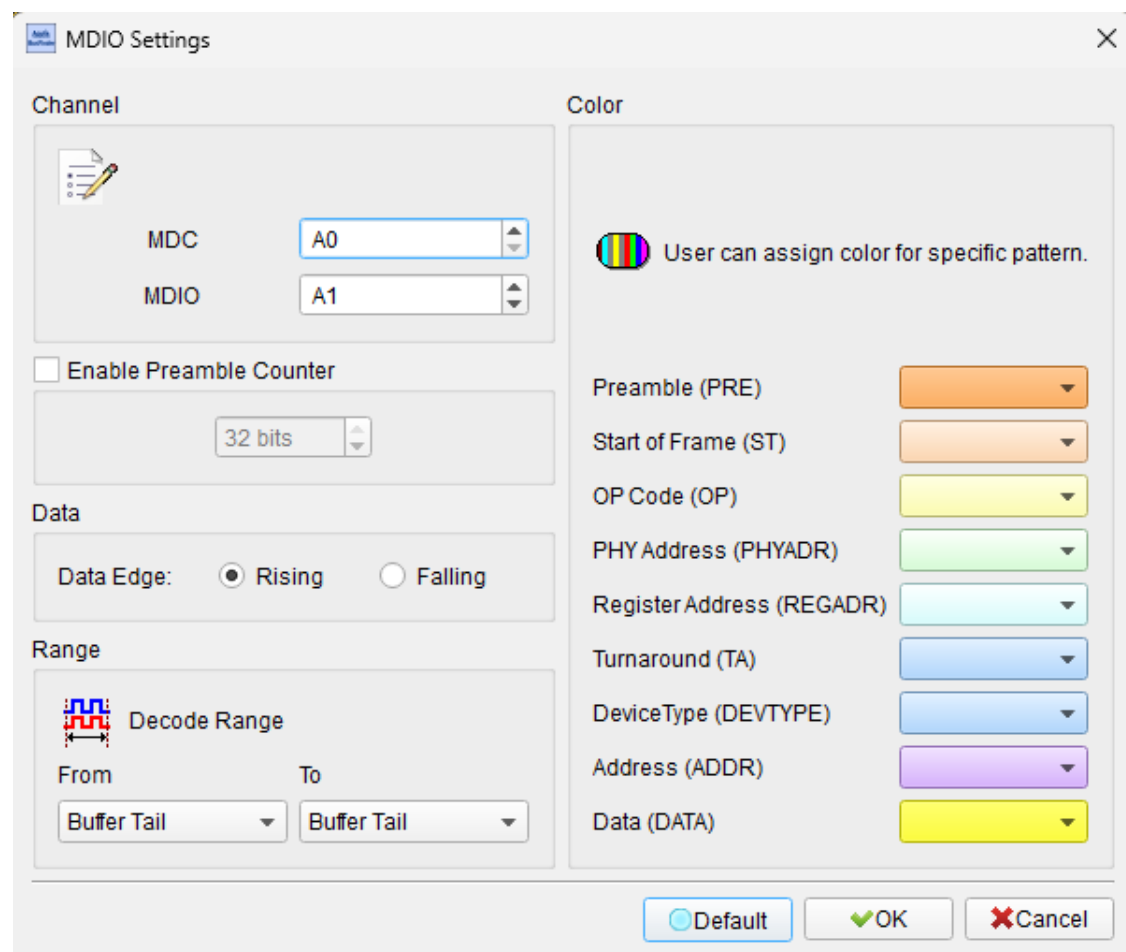
Result



MDIO

MDIO, also known as Serial Management Interface (SMI), is a serial bus defined for the Ethernet IEEE 802.3 specification for Media Independent Interface, or MII.

Settings



The MDIO Settings dialog box is divided into several sections:

- Channel:** Contains dropdown menus for MDC (set to A0) and MDIO (set to A1).
- Enable Preamble Counter:** A checkbox that is currently unchecked. Below it is a dropdown menu set to 32 bits.
- Data:** Contains a 'Data Edge' section with radio buttons for 'Rising' (selected) and 'Falling'.
- Range:** Contains a 'Decode Range' section with a waveform icon. Below it are 'From' and 'To' dropdown menus, both set to 'Buffer Tail'.
- Color:** A section with a color wheel icon and the text 'User can assign color for specific pattern.' Below this is a list of MDIO fields with corresponding color selection dropdowns:
 - Preamble (PRE): Orange
 - Start of Frame (ST): Light Orange
 - OP Code (OP): Yellow
 - PHY Address (PHYADR): Light Green
 - Register Address (REGADR): Light Blue
 - Turnaround (TA): Blue
 - DeviceType (DEVTYPE): Light Blue
 - Address (ADDR): Purple
 - Data (DATA): Yellow

At the bottom of the dialog are three buttons: 'Default' (with a circular arrow icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

MDC: Transfer clock of MDIO.

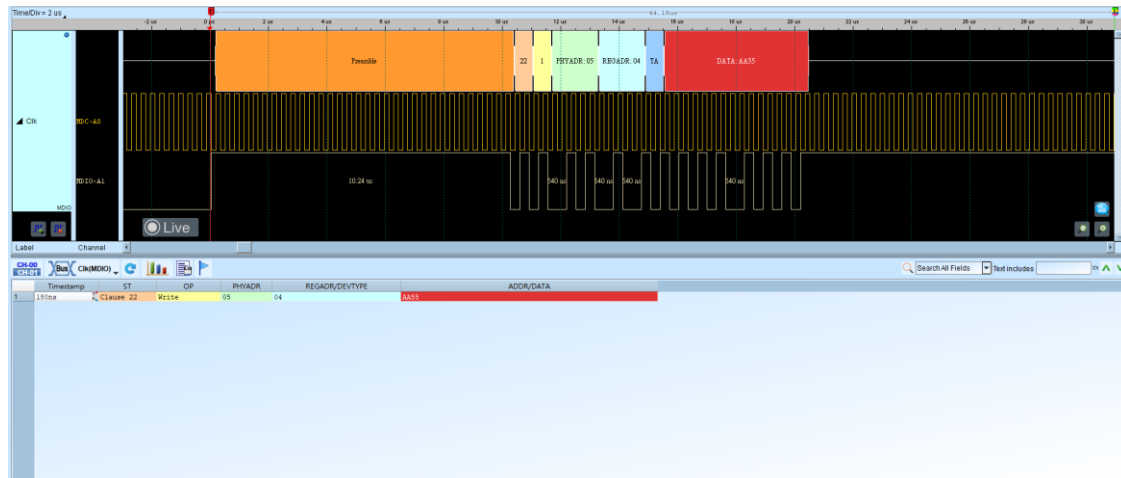
MDIO: Transfer data input/output of MIDO.

Data Edge: Set the MDC Rising/Falling edge to latch the data field, Rising Edge default.

Enable Preamble Counter: Configurable MDIO Preamble width, 4 - 32 Bit,

default is 32 Bit. Enabled when checked.

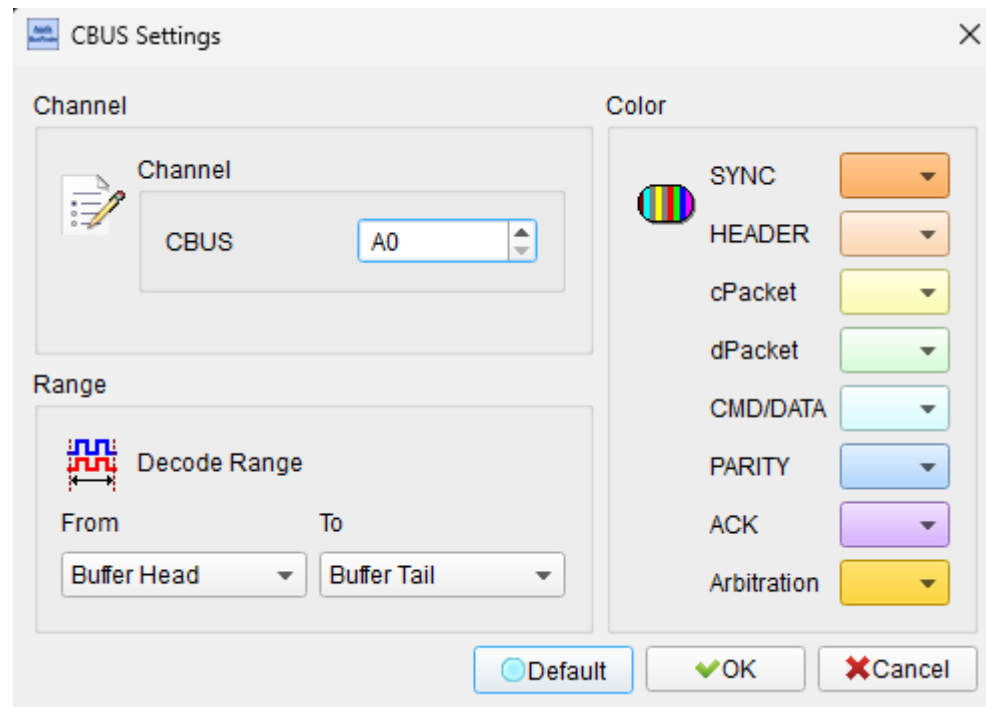
Result



MHL-CBUS

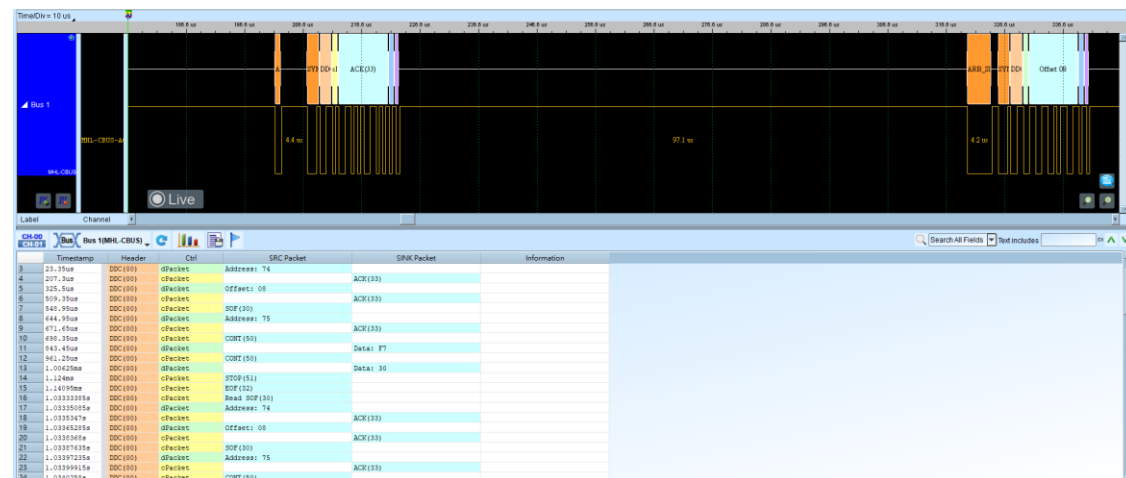
Mobile High-definition Link (MHL) is an HD audio and video interface, Control Bus (CBUS) is used to control it.

Settings



Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

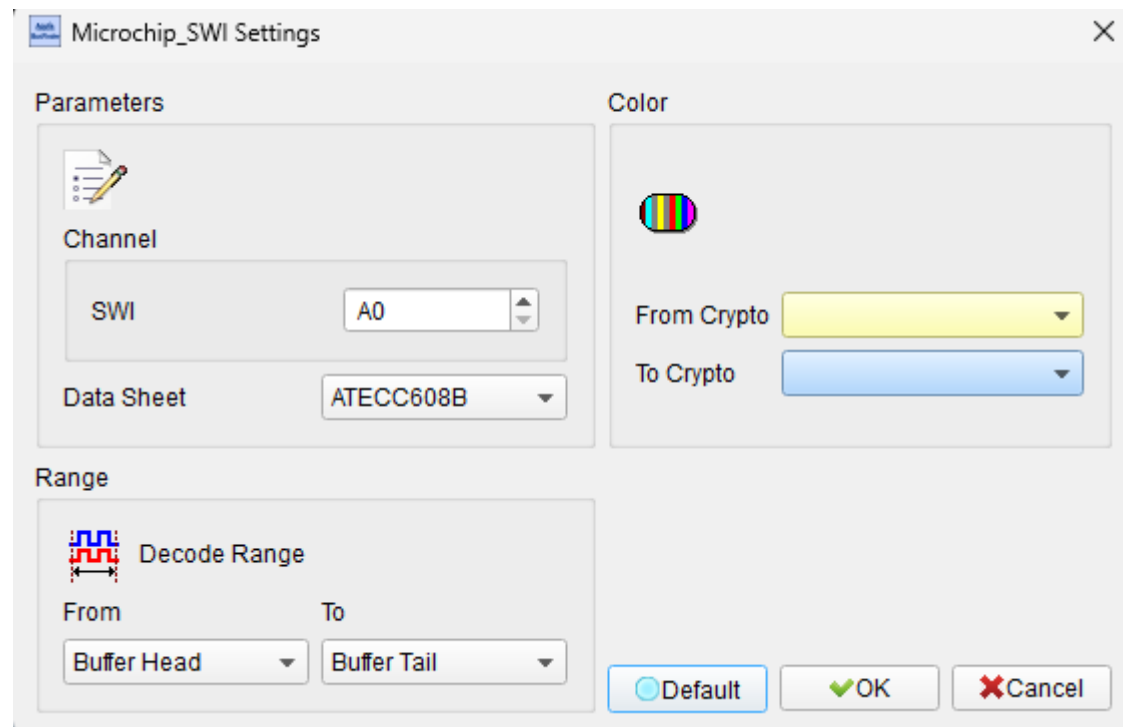
Result



Microchip SWI

SWI usually refers to Single Wire Interface, a communication protocol provided by Microchip Technology to simplify communication between devices.

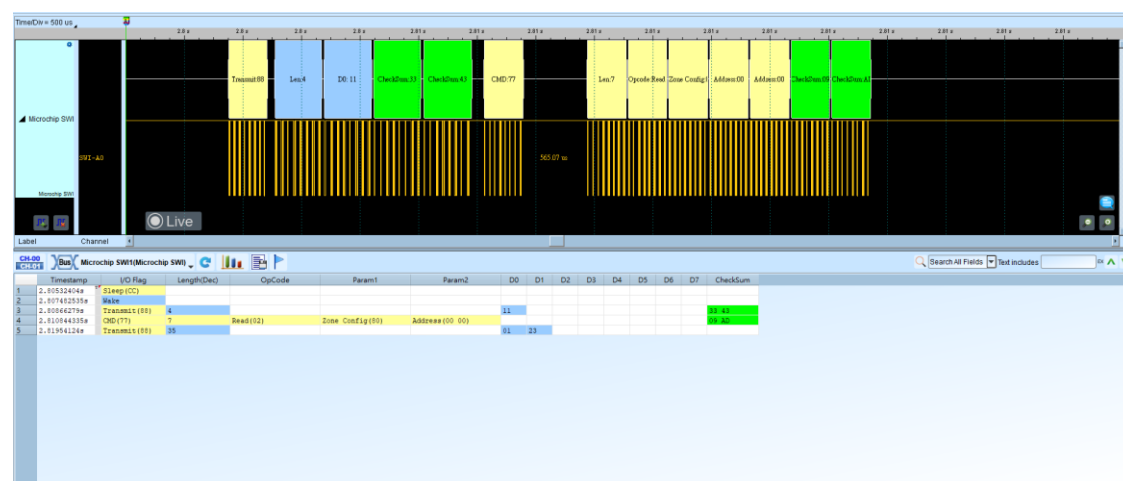
Setting



Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Data Sheet: Choose the supported IC model. We now support ATECC608B.

Result



Microwire

A serial signal format developed by National Semiconductor, the hardware structure and signal operation are the same as SPI (Serial Peripheral Interface). In the line structure, there are device selection line (CS: Chip Select), clock line (SK: Serial Clock) and data input/output line (DI: Data Input/DO: Data Output).

Settings

Microwire Settings

Channel

Channel

Chip Select Channel (CS) CH 0

Clock Channel (SK) CH 1

Data In Channel (DI) CH 2

Data Out Channel (DO) CH 3

EEPROMs

93xx46 A 8 Bits

Data

Chip Select Edge

☒ Activate High ☐ Activate Low

Data Edge (DI)

☒ Rising ☐ Falling

Data Edge (DO)

☒ Rising ☐ Falling

Report

Show Data in Report 8 Columns

Color

ERASE / WRITE ENABLE

ERASE / WRITE DISABLE

ERASE

WRITE

READ

ERASE ALL

WRITE ALL

Range

Decode Range

From To

緩衝區開頭 緩衝區結尾

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

Chip Select Edge: Active Low or Active High.

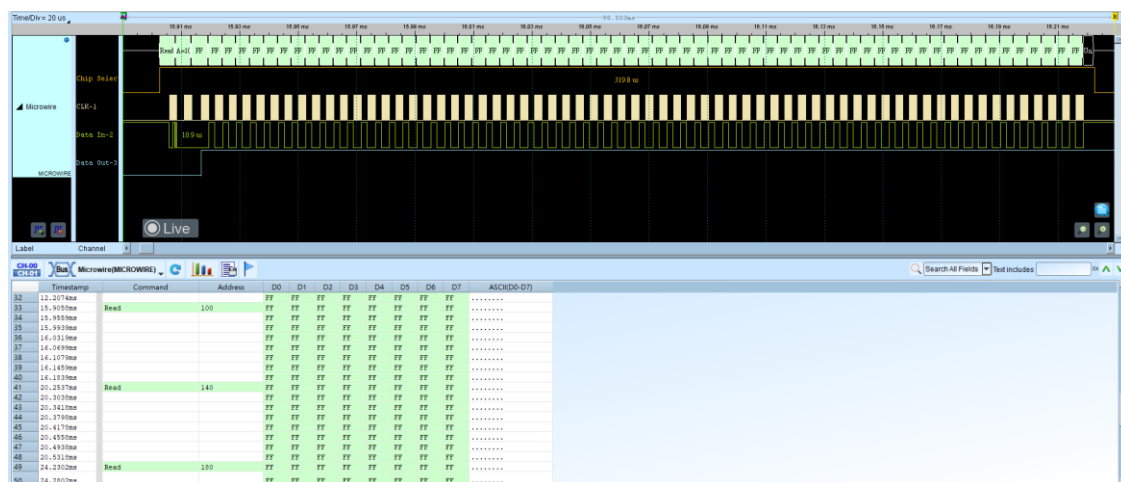
Data Edge: Rising or Falling.

EEPROMs: Select EEPROMs.

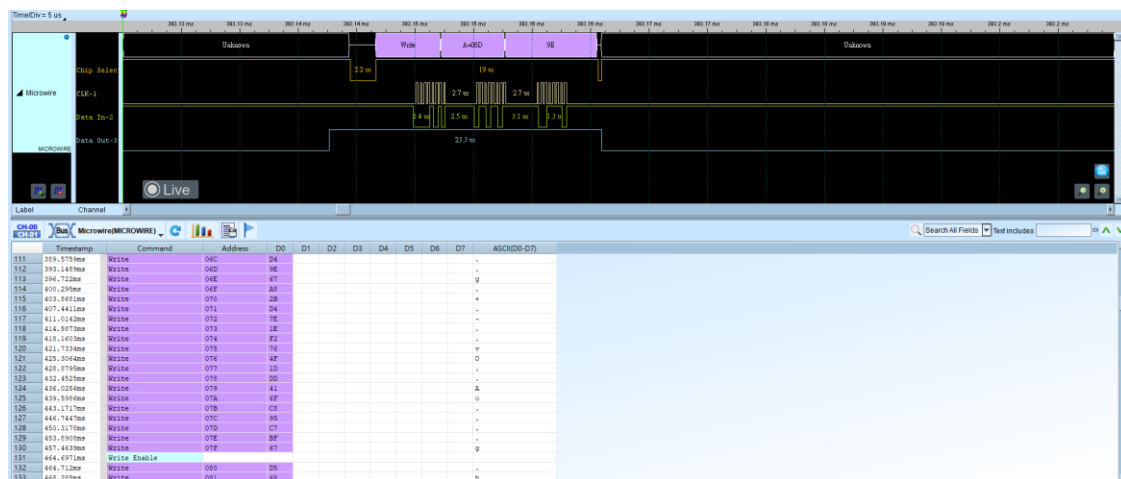
Report: Show data in report.

Result

Read



Write



MII / RMII / RGMII / GMII

MII: Media Independent Interface

RMII: Reduced Media Independent Interface

RGMII: Reduced Gigabit Media Independent Interface

GMII: Gigabit Media Independent Interface

Formulated by 802.3u that applied to Fast Ethernet, connecting MAC of Data Link Layer and PHY layer. Its clock frequency is either 25MHz or 2.5MHz (Ethernet); they are TX_CLK and RX_CLK. TX [0:3], RX [0:3] are 4-bit-width bus and TX_EN, RX_EN enable the IN/OUT; TX_ER, RX_ER can detect the errors on the bus; RX_DV inform bus the data received is valid or not; COL can detect the collision on the bus. **Serial Management Interface (SMI), also known as MDIO, is also an important part of MII.**

Settings

MII / RMII / GMII / RGMII Settings

Settings

- Protocol: MII
- Mode: Transmit (TX)
- Data Edge: Rising
- Report Columns: 8 columns
- RGMII Speed: 1 Gbps
- RGMII Clock: Normal
- ☒ Decode Ethernet Packet (MAC)

Timing Specifics

- ☐ Ts skew = 0.000 ns

Color

User can assign color for specific pattern.

- Data: [Yellow] Error: [Red]
- Collision: [Purple] Idle: [Black]
- Preamble/SFD: [Cyan] Others: [Blue]

Channel

Transmit(TX)		Receive(RX)	
TX_CLK	A0	RX_CLK	A0
TX_D0	A1	RX_D0	A0
TX_D1	A2	RX_D1	A0
TX_D2	A3	RX_D2	A0
TX_D3	A4	RX_D3	A0
TX_D4	A8	RX_D4	A0
TX_D5	A9	RX_D5	A0
TX_D6	A10	RX_D6	A0
TX_D7	A11	RX_D7	A0
TX_EN	A5	RX_DV	A0
TX_ER	A6	RX_ER	A0
TX_COL	A7		

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Protocol: MII / RMII / GMII / RGMII can be selected. except BusFinder / LA, TravelLogic and MSO do not support GMII.

Mode: Transmit (Tx) or Receive (Rx) mode can be selected.

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Data Edge:

Rising: Latch data when Clock edge is rising.

Falling: Latch data when Clock edge is falling.

Report Column:

8 Columns: Set the data fields of the report window to be displayed in 8 columns.

16 Columns: Set the data fields of the report window to be displayed in 16 columns.

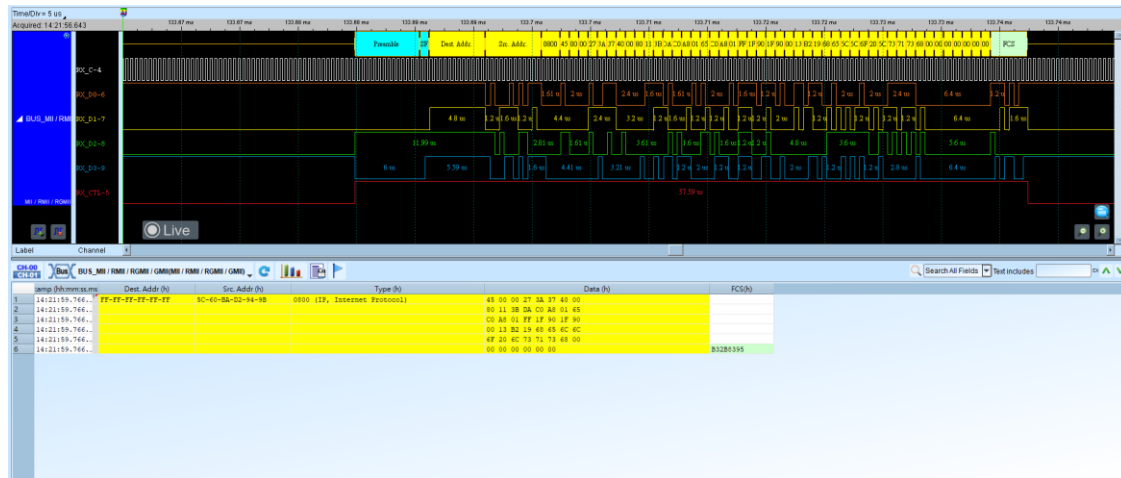
RGMII Speed: Set the speed of RGMII to 1Gbps or 100/10Mbps, valid only when MII is set to RGMII.

RMII Clock: Set the RMII Clock to Normal or Decrease Latch Frequency (x10). Only available when MII is set to RMII.

Decode Ethernet Packet (MAC): Decode MAC packets. Enabled when checked.

Timing Specifics: Sets the delay or advance of the Data Latch. Available only when MII is set to GMII. Enabled when the check box is selected.

Result



Mini / Micro-LED

The die positioning of display panel in Mini LED is 100 ~ 200 μ m, and Micro LED is below 50 μ m.

Parameter Settings

MiniLED Settings

Parameters

Channel

DCLK: A0

LE: A1

Data: A2

Color

CMD: [Orange Bar]

Data Line 1: [Yellow Bar]

Data Line 2: [Blue Bar]

Range

Decode Range

From: Buffer Head To: Buffer Tail

IC Setting

Model: User Defined

Option

Mode: Data

Word Size: 8

Bit Order: LSB First

GCLK x: 1 ☐ DDR

Data Edge: Rising

☒ Skip Data Bit: 0

(Skip Data Bit After CMD)

Delay Time: 0 ns

SDR max range is -GCLK / 2 to +GCLK / 2

DDR max range is -GCLK / 4 to +GCLK / 4

(Unit: sample point)

Default OK Cancel

Channel

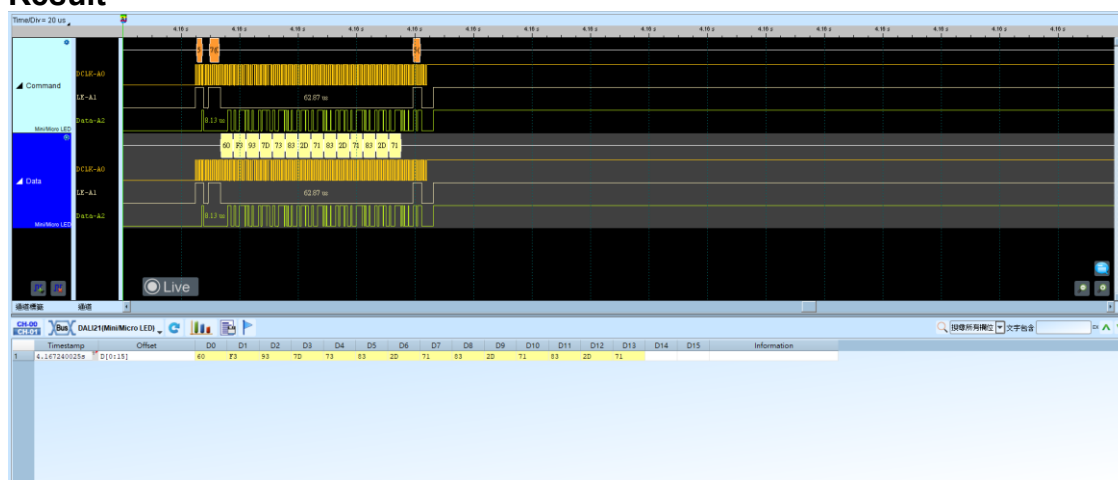
1. **DCLK:** Default CLK channel
2. **Data:** Data channel
3. **LE:** The channel that can switch CMD or DATA

IC Setting:

1. **Model:** Setting the IC model number, currently supports ICND, MBI and User Defined; after selecting the model number, user can select the IC number again.

2. **Mode:** Set the Mode of the IC to Data or Command.
3. **Word size:** The number of the data bits.
4. **Bit order:** MSB/LSB first.
5. **GCLK:** The magnification of DCLK.
6. **DDR:** DDR mode. Enabled when checked.
7. **Data Edge:** Rising/falling latch.
8. **Skip Data Bit:** Set the number of skip data bit after LE falling
9. **Delay Time:** Set the time lead / delay in data line.

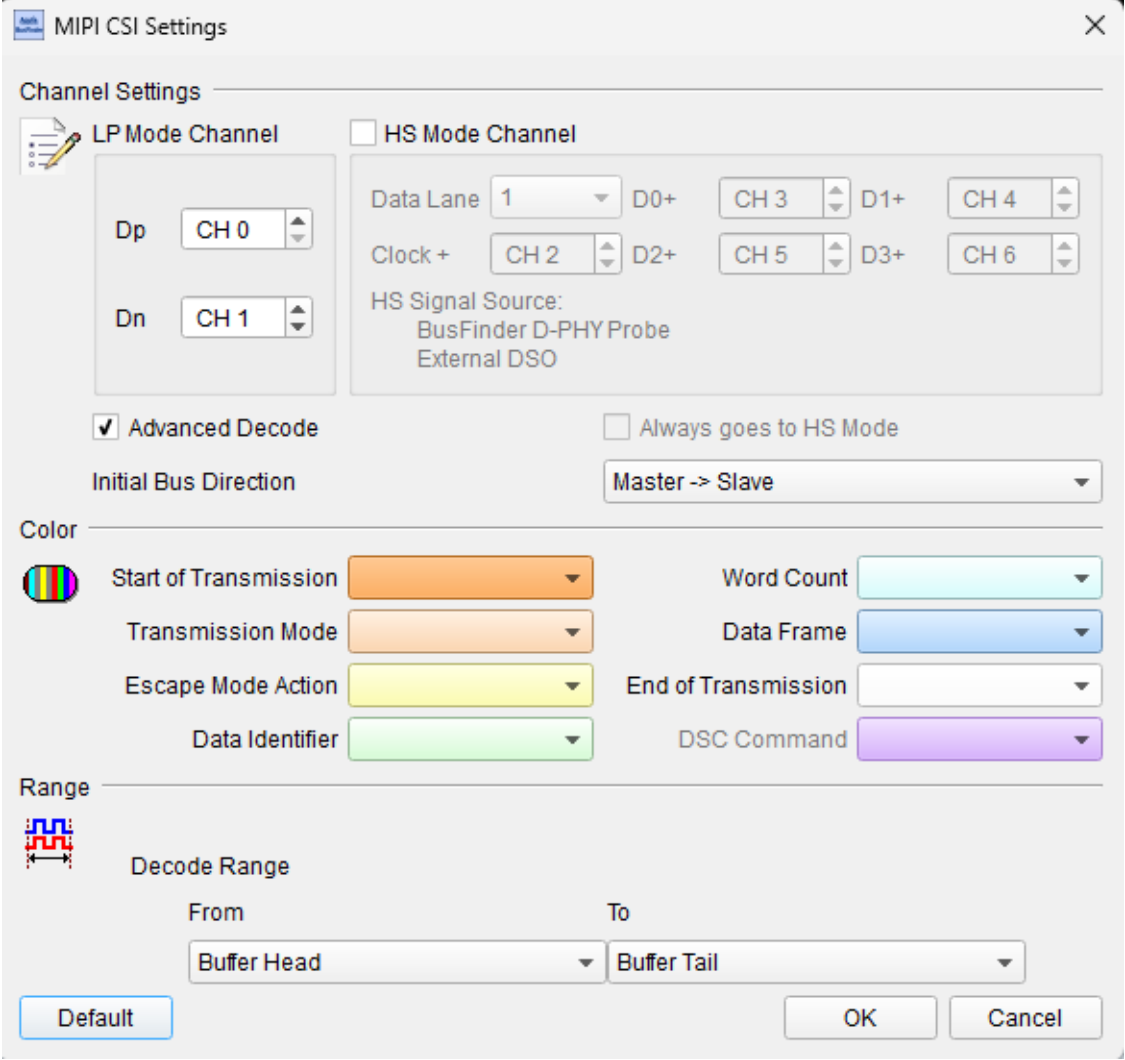
Result



MIPI CSI

MIPI CSI (Mobile Industry Processor Interface Camera Serial Interface) is a standardized data transfer protocol specifically designed to connect image sensors (such as camera modules) to processors (such as mobile phones, tablets or embedded devices). It was developed by the MIPI Alliance (Mobile Industry Processor Interface Alliance) to provide an efficient, low-power and high-speed data transfer channel.

Settings



The image shows the 'MIPI CSI Settings' dialog box. It has a title bar with a close button. The main area is divided into several sections:

- Channel Settings:**
 - LP Mode Channel:** Includes 'Dp' (set to CH 0) and 'Dn' (set to CH 1) dropdowns.
 - HS Mode Channel:** A checkbox that is currently unchecked.
 - Data Lane:** A dropdown set to '1'.
 - D0+:** A dropdown set to 'CH 3'.
 - D1+:** A dropdown set to 'CH 4'.
 - Clock +:** A dropdown set to 'CH 2'.
 - D2+:** A dropdown set to 'CH 5'.
 - D3+:** A dropdown set to 'CH 6'.
 - HS Signal Source:** A text area containing 'BusFinder D-PHY Probe' and 'External DSO'.
- Advanced Decode:** A checkbox that is checked.
- Always goes to HS Mode:** A checkbox that is unchecked.
- Initial Bus Direction:** A dropdown menu set to 'Master -> Slave'.
- Color:**
 - Start of Transmission:** A color picker set to orange.
 - Transmission Mode:** A color picker set to light orange.
 - Escape Mode Action:** A color picker set to yellow.
 - Data Identifier:** A color picker set to light green.
 - Word Count:** A dropdown menu set to '1'.
 - Data Frame:** A dropdown menu set to 'Data'.
 - End of Transmission:** A dropdown menu set to 'End of Frame'.
 - DSC Command:** A dropdown menu set to 'DSC Command'.
- Range:**
 - Decode Range:**
 - From:** A dropdown menu set to 'Buffer Head'.
 - To:** A dropdown menu set to 'Buffer Tail'.

At the bottom, there are three buttons: 'Default', 'OK', and 'Cancel'.

Dp, Dn: The signal channel for DSI-LP mode.

Data Lane: The lane amount under DSI-HS mode.

Clock+, D0+, D1+, D2+, D3+: The signal channel under DSI-HS mode.

Enabled when checked.

Advanced Decode: Decodes the data in CSI format. Enabled when checked.

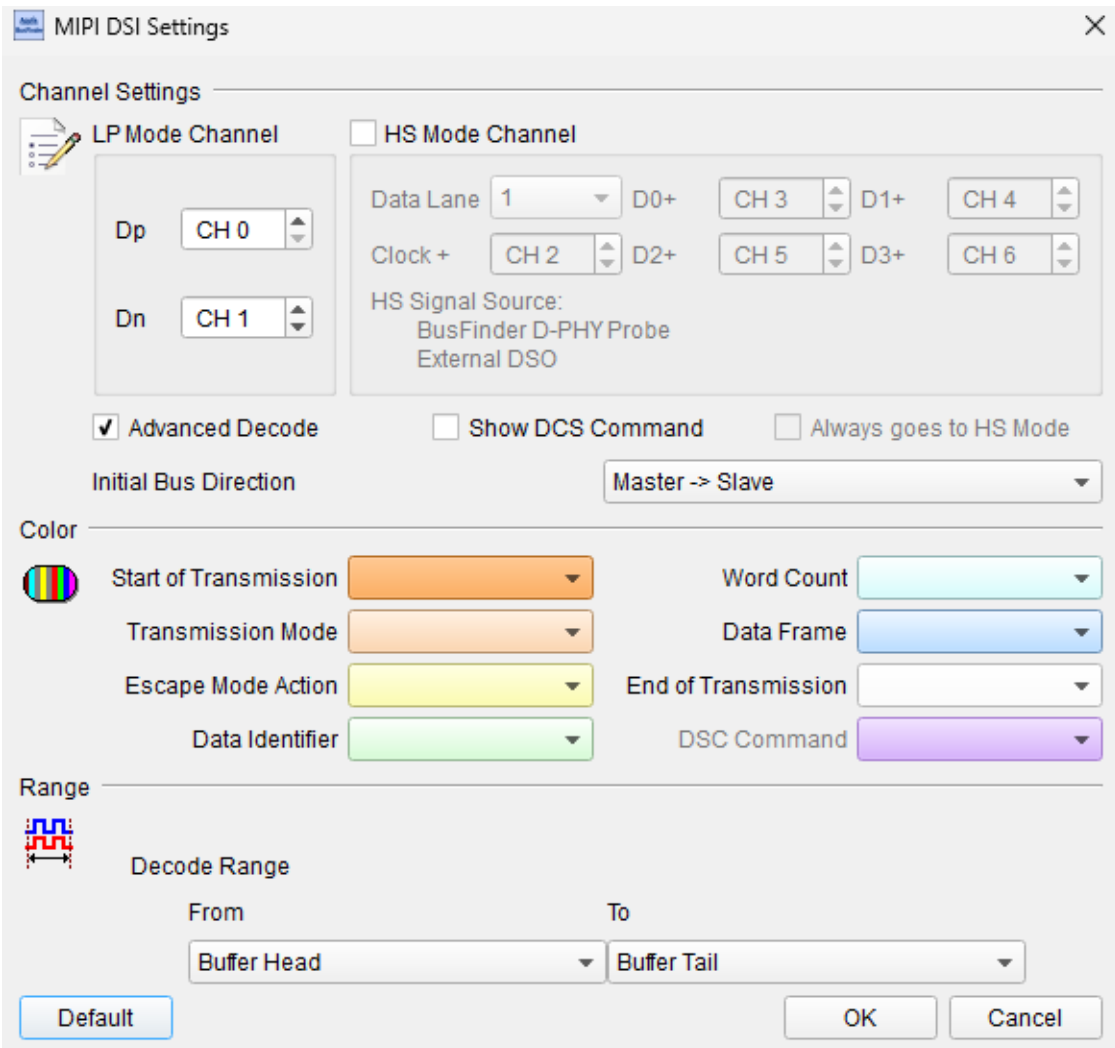
Always goes to HS Mode: Ignore the status of Dp and Dn in DSI-LP mode, and always read the data as HS-Mode, enabled when checked.

Initial Bus Direction: Select the data transmission direction of the bus in the initial state.

MIPI DSI

MIPI Display Serial Interface (DSI) designed by MIPI alliance for the protocols between a host processor and peripheral devices using a D-PHY physical interface. The operation mode includes High Speed Mode and Low Power Mode (LPM).

Settings



The image shows the 'MIPI DSI Settings' dialog box. It is divided into several sections: 'Channel Settings', 'Color', and 'Range'.
Channel Settings: Includes 'LP Mode Channel' (with Dp set to CH 0 and Dn set to CH 1) and 'HS Mode Channel' (unchecked). The HS Mode Channel section shows Data Lane 1, Clock +, D0+, D1+, D2+, D3+, D4+, D5+, and D6+ channels. The HS Signal Source is set to 'BusFinder D-PHY Probe' and 'External DSO'. There are checkboxes for 'Advanced Decode' (checked), 'Show DCS Command' (unchecked), and 'Always goes to HS Mode' (unchecked). The 'Initial Bus Direction' is set to 'Master -> Slave'.
Color: Includes color selection icons and dropdowns for 'Start of Transmission' (orange), 'Transmission Mode' (orange), 'Escape Mode Action' (yellow), 'Data Identifier' (green), 'Word Count' (cyan), 'Data Frame' (blue), 'End of Transmission' (white), and 'DSC Command' (purple).
Range: Includes a 'Decode Range' section with 'From' (Buffer Head) and 'To' (Buffer Tail) dropdowns. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

Dp, Dn: DSI-LP signal lines

Data Lane: DSI-HS mode Data Lane number

Clock+, D0+, D1+, D2+, D3+: DSI-HS signal lines

Advanced Decode: Enable DSI format decode and display.

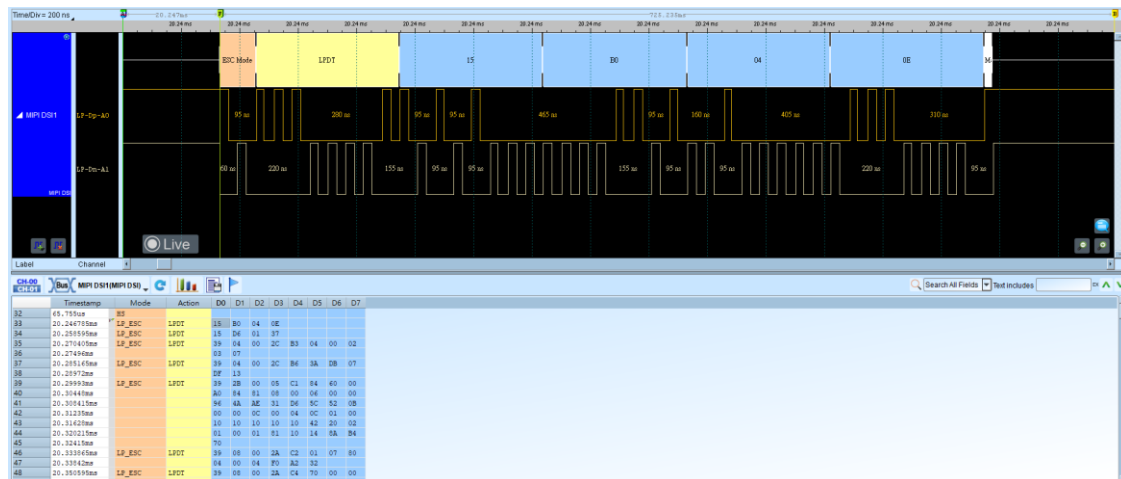
Show DCS Command: Enable DCS Command decode and display.

Always goes to HS Mode: Ignore the Dp and Dn status and decode all the data frame in HS mode

Initial Bus Direction: Select the Initial direction of the bus transmission.

Result

Advanced Decode Disabled:



Advanced Decode Enabled:



MIPI I3C

MIPI I3C is an extension of I2C interface, so it still maintains the two-wire SCL (clock), SDA (data) as I2C. The frequency of MIPI I3C SCL clock is defined in spec. up to 12.9 MHz, and generally it is 12.5 MHz. It supports three operating voltages, 1.2 V / 1.8 V / 3.3 V. The MIPI I3C is a new generation of sensor interface specification, which integrates multiple sensor interfaces in one unified specification, mainly for simplifying the application of smart phone, smart phone, and sensor interface.

MIPI I3C is a new generation sensor interface specification that integrates multiple sensor interfaces in a unified specification, with the main application being to simplify sensor integration in smart phones, IoT devices, and automotive systems.

Settings

MIPI I3C Ver. 1.1.1 Settings

Channel

SCL: A0
SDA: A1

Startup

Mode: I3C SDR Mode

Extended Specification

☐ MIPI Debug Over I3C

Report Detail Options

☒ Show CCC Detail
☒ Show Tenary Symbol

Range

Decode Range
From: Buffer Head To: Buffer Tail

Color

S / Sr / P: [Orange] RnW: [Blue]
ACK / NACK: [Orange] T / PAR: [Purple]
Address: [Yellow] HDR Restart: [White]
Command: [Green] HDR Exit: [Pink]
Data: [Cyan] HDR Flow Control: [Blue]

Device Configuration

☐ DDR5 Serial Presence Detect (SPD)

☐ Custom Device Settings [Add] [Delete] [Edit]

Device Type	Static Address	Dynamic Address

Default OK Cancel

Channel:

1. **Clock Channel (SCL):** Transfer clock of I3C.
2. **Data Channel (SDA):** Transfer data of I3C.

Startup: Specifies the mode that is currently running on the bus. User can set the mode to:

1. I3C SDR Mode
2. I2C Mode
3. I3C HDR-DDR Mode
4. I3C HDR-TSP Mode
5. I3C HDR-TSL Mode

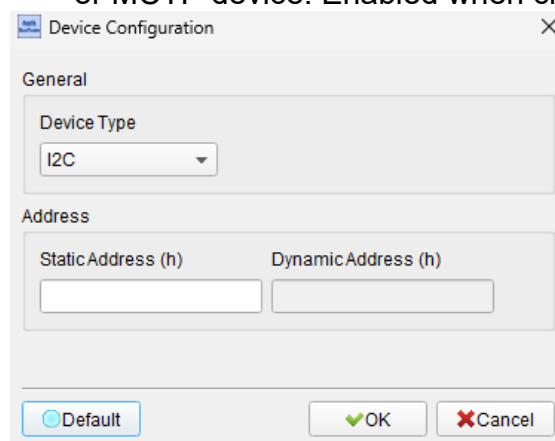
Extended Specification—MIPI Debug Over I3C: The command for debugging I3C. Enabled when checked

Report Detail Options:

1. **Show CCC Detail:** Show the CCC(Common Command Code) information in report. Enabled when checked.
2. **Show Ternary Symbol:** Show the Ternary Symbol in report. Enabled when checked.

Device Configuration:

1. **DDR5 Serial Presence Detect (SPD):** SPD function. Enabled when checked.
2. **Custom Device Settings:** Add user-defined device. User can add I²C or MCTP device. Enabled when checked.



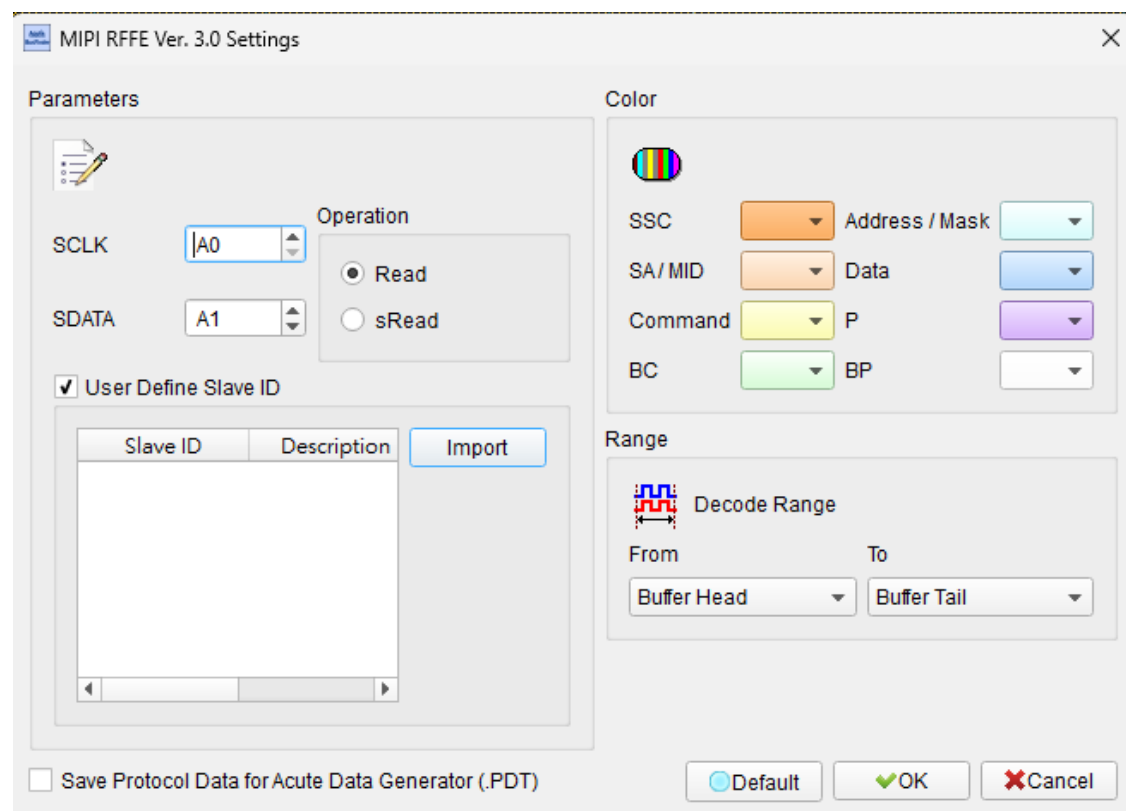
Result



MIPI RFFE

MIPI RFFE (RF Front-End Control Interface) designed by MIPI alliance is for controlling RF front-end devices including Power Amplifiers, Low-Noise Amplifiers, filters, switches, power management modules, antenna tuners and sensors.

Settings



Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Operation: Set to Read or sRead.

User Define Slave ID: Add used-defined Slave ID. Enabled when checked.

Save Protocol Data for Acute Data Generator (.PDT): Save the analyzed result as .PDT file for the usage of Acute Data Generator. Enabled when checked.

MIPI SoundWire

Soundwire is a hardware interface and transport protocol developed by MIPI. It provides an expandable, simple, low-power, low-latency, dual-lead (clock and data) bus that can be used to transfer multiple audio streams such as amplifiers and microphones and embedded control commands.

Max Clock Rate:12.288MHz

Settings

MIPI SoundWire Settings

Channel

Clock: A0
Data: A1

Startup Setting

Delay: 40 ns
Current Bank: ☒ Bank 0 ☐ Bank 1
Initial Frame Shape

Bank 0		Bank 1	
Row	Column	Row	Column
48	2	48	2

Report Settings

☐ Show Packet Table
☐ Hide all Ping OpCode
☐ Ignore SCP Frame Ctrl CMD

Range

Decode Range
From: Buffer Head To: Buffer Tail

☐ Enable PayLoad

Type: PCM
Bank: Bank 0
Device: Device 0
DPn: DP0
HStart: 0
HStop: 0
Block Packing Mode: Block-per-Port
Port Flow Mode: Normal (isochronous)

Sample Interval: 96
Offset 1: 0
Offset 2: 0
Word Length: 0
Audio Sample Rate: 4000 Hz
PDM Sample Rate: 4800 KHz

☐ CH1 ☐ CH2 ☐ CH3 ☐ CH4
☐ CH5 ☐ CH6 ☐ CH7 ☐ CH8

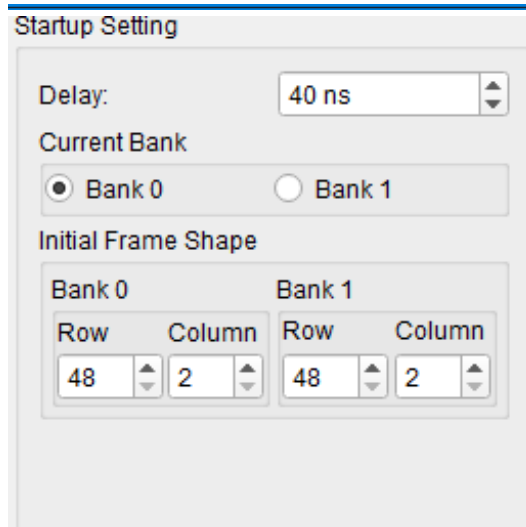
☐ Save as .wav ☐ Save as .bit
☐ Playback
☐ Full Scale ☒ All
☐ Display Audio ☐ 5 Sec
☐ Full Scale ☐ 3 Sec
☒ Original

☒ Default

OK Cancel

CLK: Transfer clock of SoundWire.

Data: Transfer data of SoundWire.



Startup Setting

Delay: 40 ns

Current Bank
☒ Bank 0 ☐ Bank 1

Initial Frame Shape

Bank 0		Bank 1	
Row	Column	Row	Column
48	2	48	2

Delay: Fix the position of latching data.

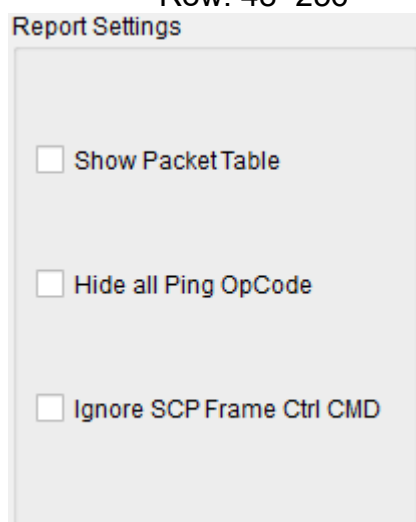
Bank: There are two types of parameters setting files, Bank0 and Bank1.

The Data port (DP) is the source or sink of the Payload Stream on the SoundWire bus, and the DP also divides the Payload Stream into one or more channels for each audio channel.

Initial Frame Shape: set the row and column of each setting file.

Column: 2~16(Only even)

Row: 48~256



Report Settings

☐ Show Packet Table

☐ Hide all Ping OpCode

☐ Ignore SCP Frame Ctrl CMD

Show Packet Table: Show Packet Table (in 2-Dimension). Enabled when checked.

Hide all Ping OpCode: Hide all the Ping OpCode in report. Enabled when checked.

Ignore SCP Frame Ctrl CMD: Hide all SCP CMD in report for easy reading.

Enabled when checked.

☒ Enable PayLoad

Type:	PCM	Sample Interval:	96	<input type="checkbox"/> Save as .wav	<input type="checkbox"/> Save as .txt
Bank:	Bank 0	Offset 1:	0	<input type="radio"/> Full Scale	<input type="checkbox"/> Playback
Device:	Device 0	Offset 2:	0	<input checked="" type="radio"/> Original	<input checked="" type="radio"/> All
DPn:	DP0	Word Length:	0	<input type="checkbox"/> Display Audio	<input type="radio"/> 5 Sec
HStart	0	Audio Sample Rate:	4000 Hz	<input type="radio"/> Full Scale	<input type="radio"/> 3 Sec
HStop	0	PDM Sample Rate:	4800 KHz	<input checked="" type="radio"/> Original	
Block Packing Mode:	Block-per-Port	<input type="checkbox"/> CH1 <input type="checkbox"/> CH2 <input type="checkbox"/> CH3 <input type="checkbox"/> CH4			
Port Flow Mode:	Normal (isochronous)	<input type="checkbox"/> CH5 <input type="checkbox"/> CH6 <input type="checkbox"/> CH7 <input type="checkbox"/> CH8			

DPn amount: 1~16, No. DP0~DP15

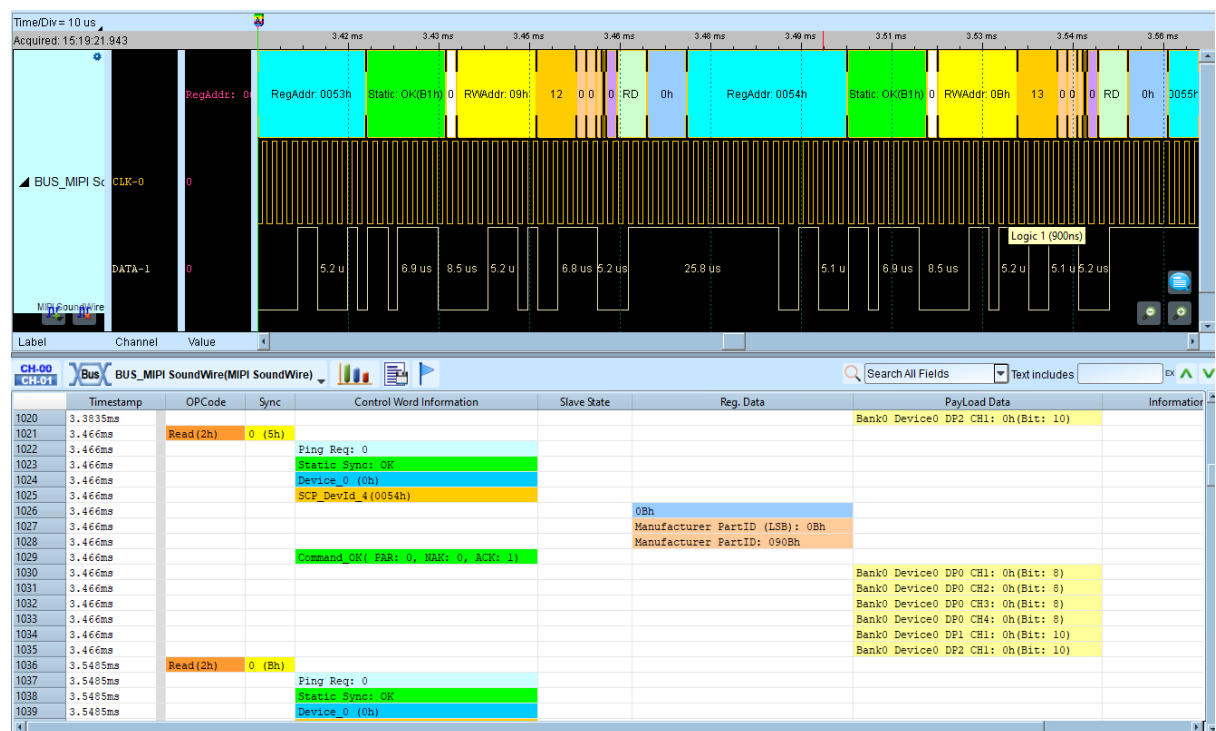
1. **HStart:** The start position of data in Frame Shape.
2. **HStop:** The stop position of data in Frame Shape.
3. **Word Length:** Data length of each channel in DPn.
4. **Sample Interval:** DPn sample interval.
5. **Block Package Mode:**
 - i. **Block per port:** Block Offset = Offset1 + (256 * Offset2)
 - ii. **Block per channel:** Block Offset = Offset1 , Sub-Block Offset = Offset2.
 - iii. ***Block Offset range :** 0 ~ 65535
 - iv. ***Sub-Block Offset range:** 0 to 255
 - v. ***Offset1 range:** 0~65535
 - vi. ***Offset2 range:** 0~255
6. **Channel:** Divide a Data Port into different parts, commonly used in the left channel, right channel and so on for data distribution, user can choose up to 8 channels to use, and do not need to follow the order of selection.
7. **Port Flow Mode:** it has four mode, Isochronous, Tx-Controlled, Rx-Controlled & Full-Asynchronous
 - i. ***Isochronous:** 'Normal' mode, there is no valid data in each Payload Data Block.
 - ii. ***Tx-Controlled:** 'Push' mode, whether the flow-control bit driven by the

Source Data Port transmits valid data in the Payload Data Block.

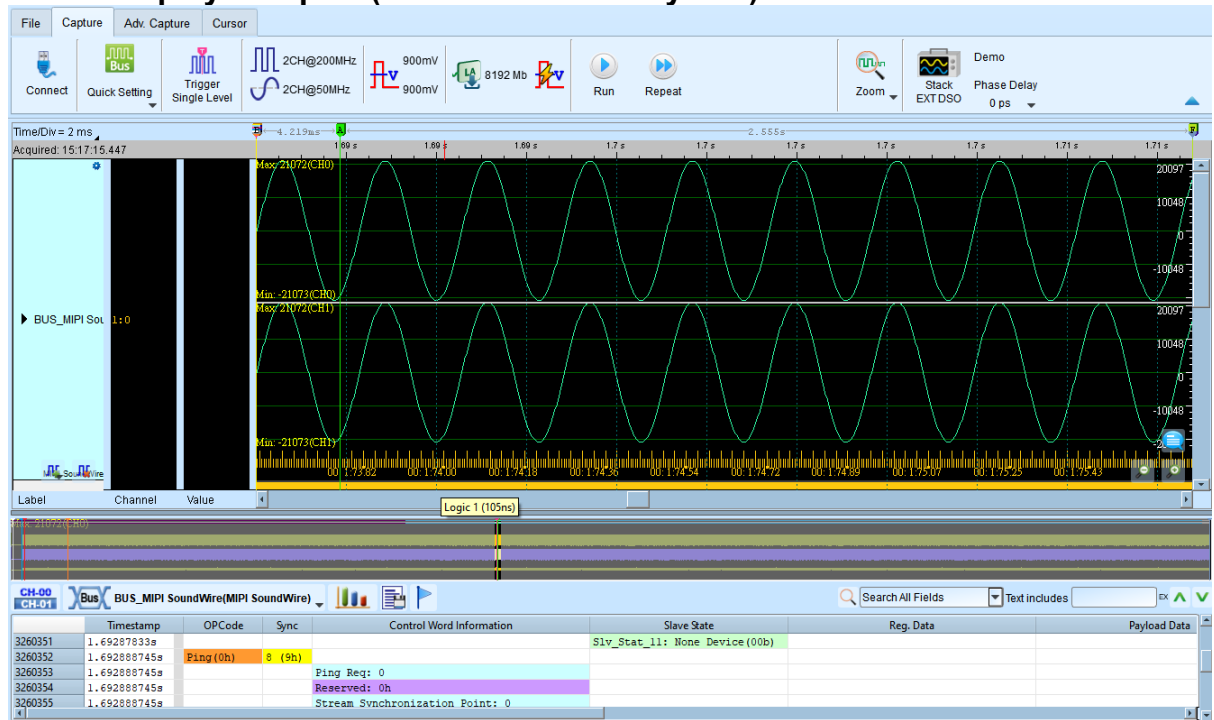
- iii. *Rx-Controlled: 'Pull' mode, whether the flow-control bit driven by the Sink Data Port transmits valid data in the Payload Data Block.
- iv. *Full-Asynchronous: Whether the flow-control bit driven by the Sink and Source Data Port transmits valid data in the Payload Data Block.

Result:

Control Word + Report (Control Word & Payload):



Audio Display + Report (Control Word & Payload)



MIPI SPMI

MIPI SPMI(System Power Management Interface) designed by MIPI alliance.

SPMI is a serial interface that connects the integrated Power Controller(PC) with Power management Integrated Circuits(PMIC).

Settings

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

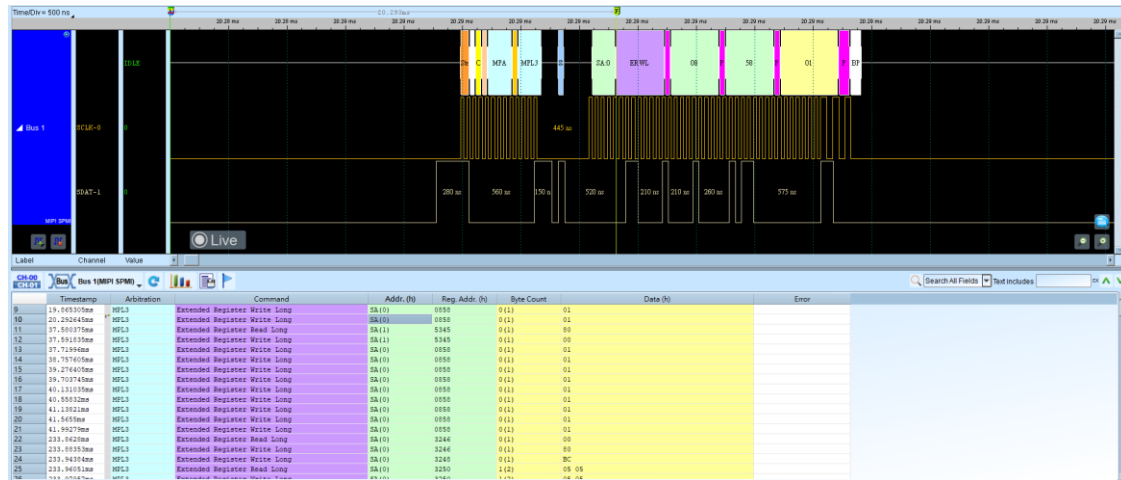
Options:

Version: Choose the version of MIPI SPMI. V2.0 and V1.0 are allowed to be chosen.

Arbitration OFF: Means there is no arbitration on the bus. Enabled when checked.

Report Options: Split register address into higher and lower address in report. Enabled when checked.

Result



MMC

The Multi Media Card (MMC) or the Embedded Multi Media Card (eMMC) version 5.1 is a flash memory card standard.

Settings

Channel:	Set the used LA Channels which are connected with DUT.
Analysis:	(Combine with the feature – Customized Report)
Command:	Analysis Command only.
Data:	Analysis Data only.
Command:	Adv. feature
Adv. Report:	Advance report on CMD, DATA argument.
3Pin mode:	Decode with CLK, CMD, D0
No CLK mode:	Only use the CLK to decode
Startup mode:	When start to decode, set the DUT. status
	Need to set the DUT. Status. Including 1-8 bit data, DDR mode, Data Strobe and no BOOT ACK.

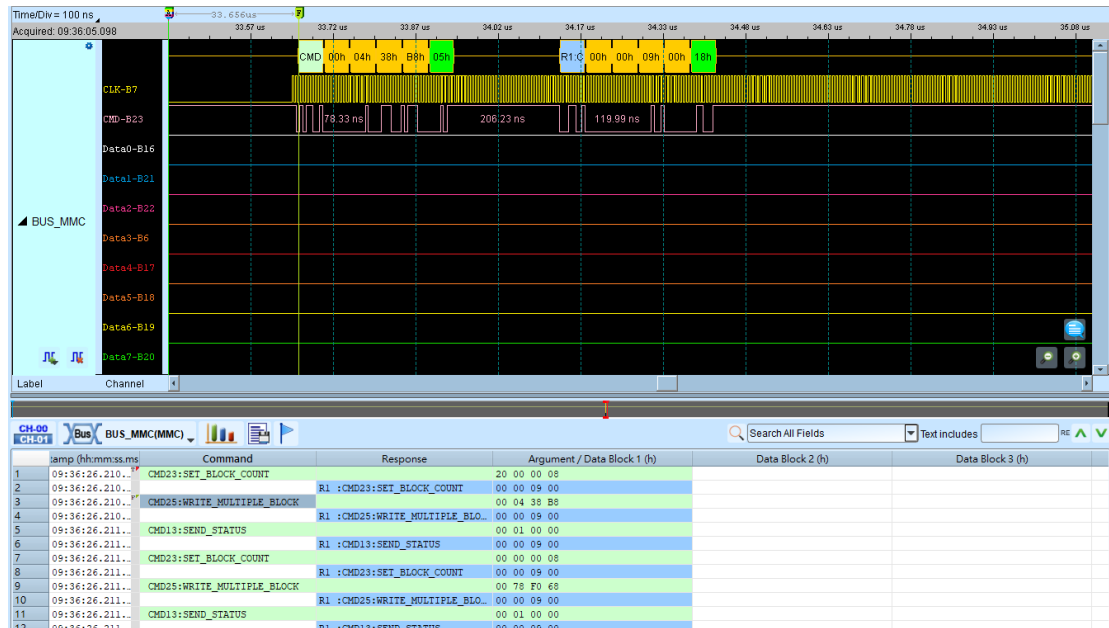
Auto Phase

Correction:

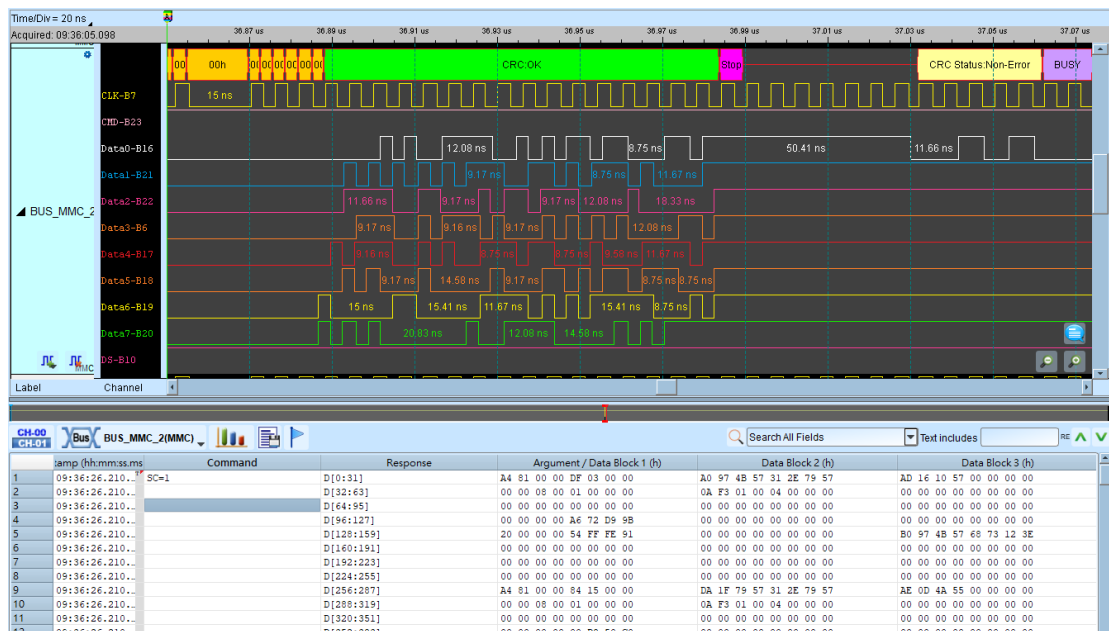
Result

Command:

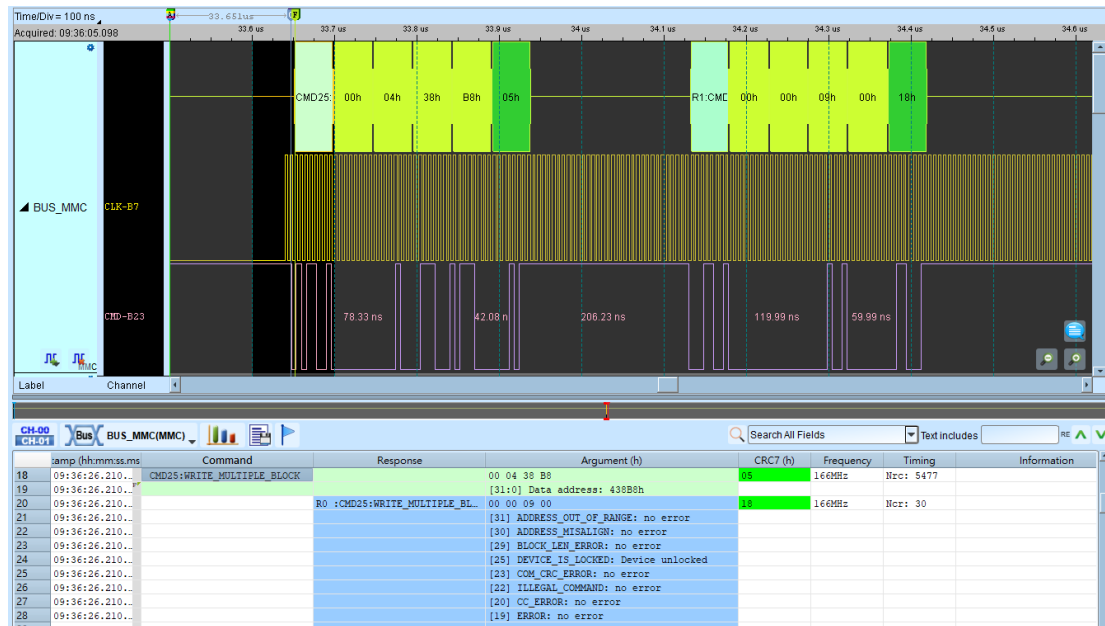
If it's checked, the decoder will auto adjust the phase of LA when measure the DUT..



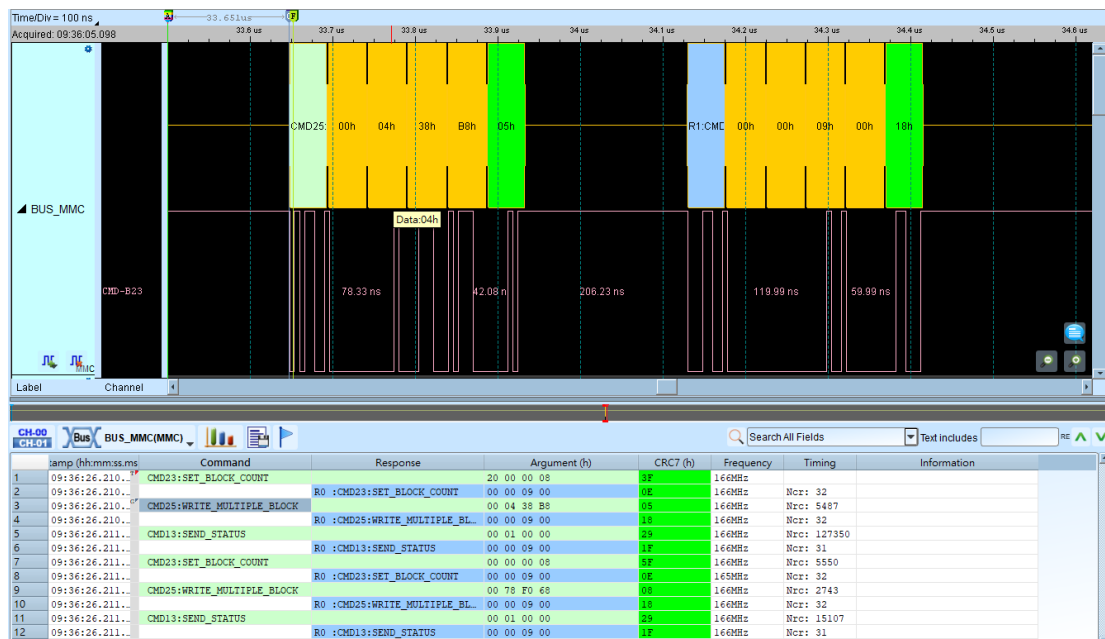
Data:



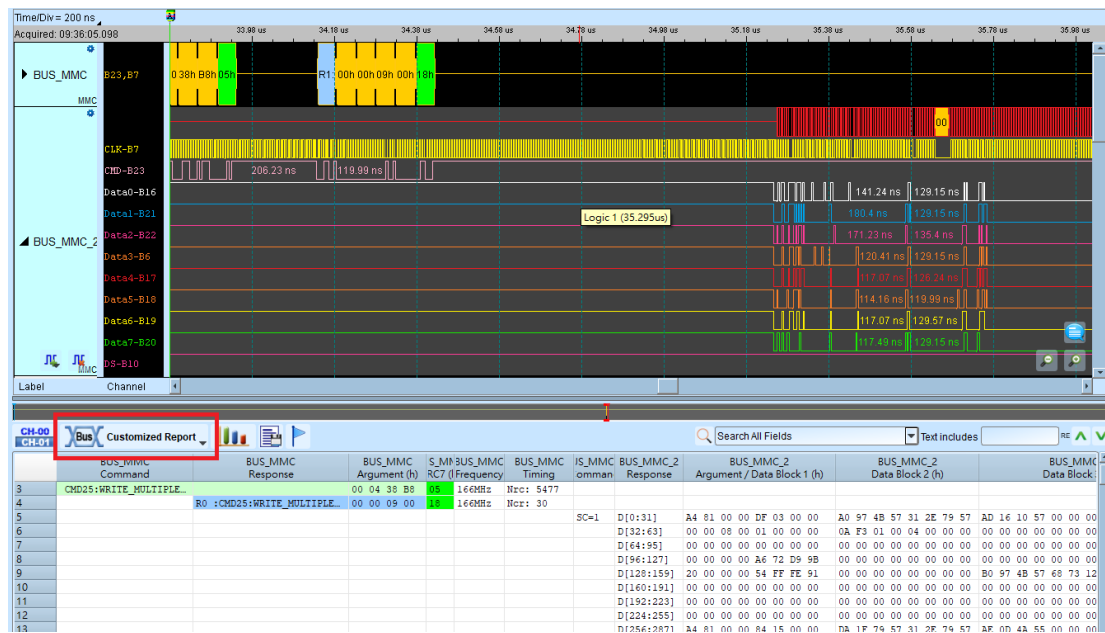
Adv. Report:



No CLK mode



Command + Data: (Customized Report)



M-PESTI

M-PESTI stands for "Modular Peripheral Sideband Tunneling Interface". It is an IP (Intellectual Property) core designed for early detection and attribute collection of peripheral devices before system boot.

M-PESTI supports bidirectional communication based on an initiator-command and target-response structure.

Settings

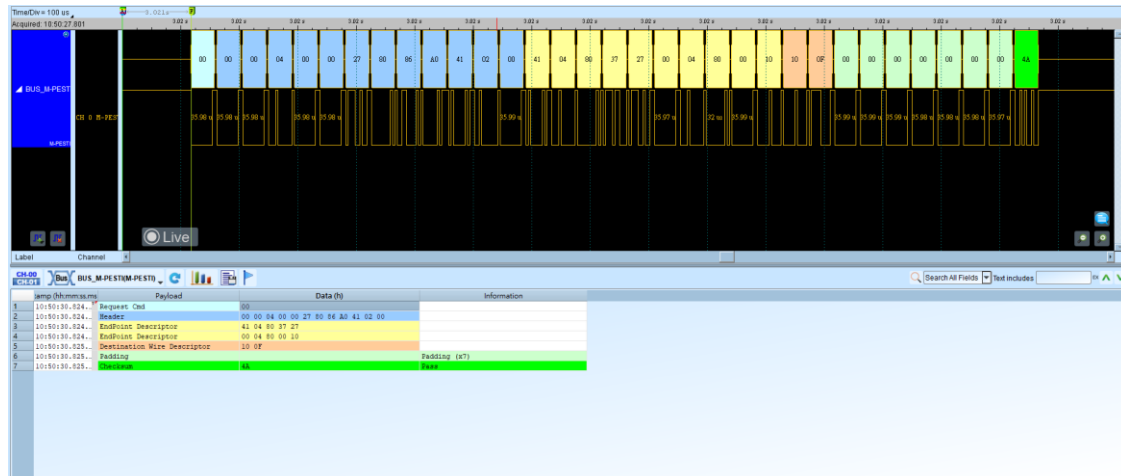
Channel: Set the signal channel of M-PESTI.

Virtual Wire Startup Setting:

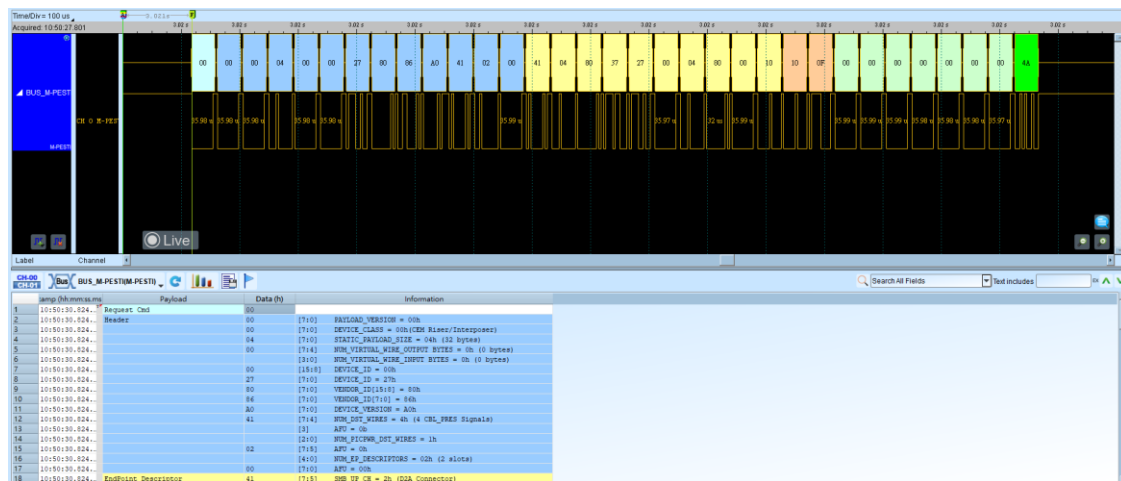
1. **Initiator to Target:** Configure the number of bytes to be sent from the Initiator to the Target, excluding the Virtual Wire Command.
2. **Target to Initiator:** Configure the number of bytes to be returned from the Target to the Initiator.

Detail Report: Detailed analysis of the byte content. Enable when checked.

Result



Detail Report



ModBus

Modbus is a serial communications protocol published by Modicon in 1979 for use with its programmable logic controllers (PLCs). Simple and robust, it has since become one of the standard communications protocols in the industry, and it is now amongst the most commonly available means of connecting industrial electronic devices.

Settings

Modbus Settings

Settings

Channel

Tx: A0 Rx: A1

If the frame gap > 1000 ms, return to Tx state (When Tx = Rx)

Transmission Mode

☐ ASCII ☒ RTU

Format

☒ Auto Detect

☐ Manual

Baud Rate: 9600 Polarity: Idle Low

Parity: None Data Bits: 8

☒ CRC Check

☐ Adv. Report

☐ Big-Endian

Waveform Area Settings

Decode: Tx ☒ Show Scale

Color

Tx/Rx: [Purple]

Address: [Orange]

Function: [Yellow]

Data: [Green]

Header: [Light Blue]

End: [Bright Green]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel:

1. **Tx:** Signal channel of Modbus Tx.
2. **Rx:** Signal channel of Modbus Rx.

Transmission Mode: It has ASCII and RTU mode.

Format:

1. **Auto Detect:** Auto detect the value of all the options that can adjust by user if it was checked.
2. **Manual:** User can manually adjust the options below:
 - I. **Baud Rate:** Data rate (bits per second), and the range is 110 ~ 2M (bps).
 - II. **Polarity:**
 - ◆ **Idle high:** Idle condition shows High.
 - ◆ **Idle low:** Idle condition shows Low.
 - III. **Parity:** N-None Parity, O-Odd Parity, E-Even Parity.
 - IV. **Data Bits:** Set the data bits. User can set to 7, 8 or 9.

CRC Check: Do CRC check. Enabled when checked.

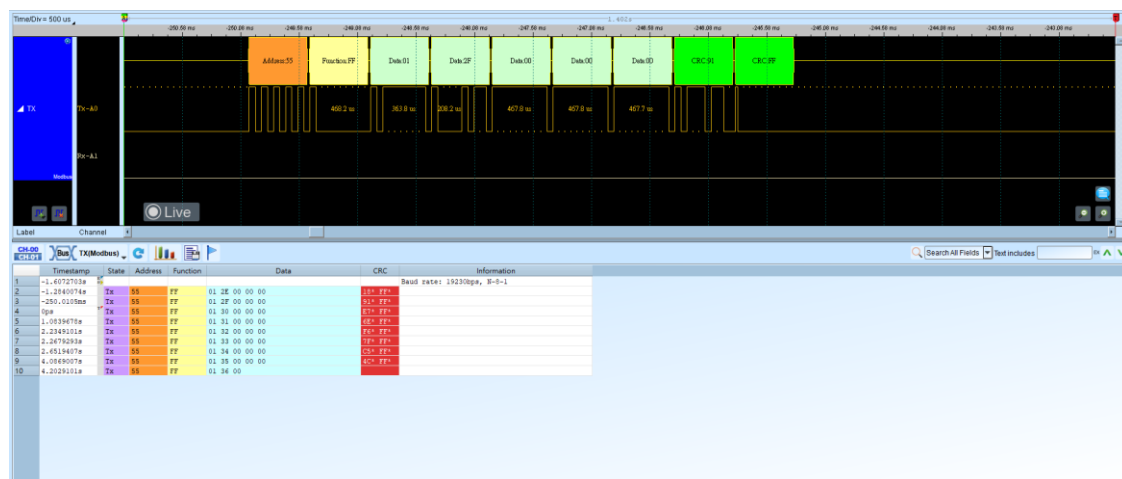
Adv. Report: Show the detail report in the report area. Enabled when checked.

Big-Endian: Data is arranged in Big-Endian style. Enabled when checked.

Waveform Area Settings:

1. **Decode:** Display the analyzed result of Tx or Rx in waveform area. Rx option only available when Rx is activated.
2. **Show Scale:** Display the waveforms with scales.

Result



NAND Flash

NAND flash uses tunnel injection for writing and tunnel release for erasing.

NAND flash memory forms the core of the removable USB storage devices known as USB flash drives, as well as most memory card formats and solid-state drives available today.

Settings

Channel:

Async	Ssync	Description
I/Ox	DQx	NAND Flash data channels
CLE	CLE	Command Latch Enable channel
ALE	ALE	Address Latch Enable channel
RE	W/R	Read Enable and Write/Read channel
WE	CLK	Write Enable and Clock channel
RB#	RB#	Ready/Busy channel

CE#	CE#	Chip Enable channel
---	DQS	Data Strobe channel

Device Width: Select 8/16 bits device width.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

I/O Quick Setup / I/O User Defined: Only set I/O0 (LSB) when select the I/O Quick Setup, other channels will be set automatically. when check the I/O User Defined and press the button will show the dialog below:

The dialog box is titled "NAND Flash I/O" and contains two columns of channel selection controls. Each control consists of a label (I/O0 through I/O15) followed by a dropdown menu showing a channel number. The channels are set as follows: I/O0 to I/O7 are set to CH 0 through CH 7 respectively; I/O8 to I/O13 are set to CH 0; I/O14 is set to CH 14; and I/O15 is set to CH 15. At the bottom, there are two buttons: "OK" with a green checkmark icon and "Cancel" with a red X icon.

User can set NAND I/O channel by channel.

The Flash Startup mode: Check Toggle /ONFI DDR Mode to run synchronous data interface.

tREA / tDQSQ: Set the delay time to access the NAND data under SDR / DDR. To adjust the tREA/tDQSQ when the data out value of NAND Flash is invalid.

Save the NAND Flash Data: Save the read/write data. Program will save the NAND Flash read/write data as a file when check Save the NAND Flash Data. It will be saved into the LA work directory.

mode.

Don't show BUSY State: Show/hide the BUSY state information (e.g. BUSY START / BUSY END) in the report window.

Erase Count: Show/ hide NAND Erase command/address statistics.

Show/Hide Items: Show/hide the items in the report window.

Invert RE# (W/R#) / Invert DQS: check this item when connect the RE/DQS# pin under DDR mode.

Not Filled the address field of report: Filled the NAND write/Read address column in the report window or not.

Invert RE# (W/R#) / Invert DQS: Check this when connect the RE / DQS# under DDR mode.

Don't care ALE/RB#/CE# signal: Ignore the signal selected when decode.

Description of file name as following (**Save the NAND Flash Data function**):

File Name	Description
NF_DI/NF_DO	NAND Flash Data In / Data Out
_Rowxxxxxxh	Row Address
_Colxxxxh	Column Address
CEx	Active CEx
_1, _2, _3	File Order

Ex:NF_DI_Row017821h_Col0000h_CE1_1.bin

NF_DO_Row017821h_Col0000h_CE1_2.bin

NF_DO_Row_Col_CE1_3.bin

Compare the content of file with the one of report.

D0	D1	D2	D3	D4	D5	D6	D7
5A	A6	6F	36	B2	38	B8	B7
06	8A	B7	0B	B1	19	C8	21
7E	CE	58	EF	BD	18	47	7C
5E	DD	9A	E3	A5	E4	02	11
E9	2D	96	14	86	32	CE	F4
53	10	60	79	EA	B6	D6	CE
5A	22	53	A5	F1	9E	DB	58
8A	73	B3	B1	82	19	B9	46
92	25	76	EA	E4	CE	74	A7
1C	E5	20	3D	9F	74	BB	E5
55	54	68	4C	69	86	AC	0F

```

000000 5A A6 6F 36 B2 38 B8 B7 06 8A B7 0B B1 19 C8 21
000010 7E CE 58 EF BD 18 47 7C 5E DD 9A E3 A5 E4 02 11
000020 E9 2D 96 14 86 32 CE F4 53 10 60 79 EA B6 D6 CE
000030 5A 22 53 A5 F1 9E DB 58 8A 73 B3 B1 82 19 B9 46
000040 92 25 76 EA E4 CE 74 A7 1C E5 20 3D 9F 74 BB E5
000050 55 54 68 4C 69 86 AC 0F F1 A2 47 FA 37 4B 04 0D

```

Device information

Vendors: Select the NAND Flash Vendor. Please refer to the following details when select the **Custom** item.

Model: Select the NAND Flash device type.

Custom: Users create a **AqNFCustom.txt** file into the LA work directory when select the **Custom** vendor item and edit NAND Flash Command set.

```

Manufacturer=Samsung
PartNo=K9XXXXXXXX
#CE/RB=1
X16=N
SyncMode=Y
Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30
Cmd=Read Status, Read Stat., , , , Y, N, Y, 70
Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000, N, Y, N, 80, 11, 81, 10

```

Manufacturer, PartNo, #CE/RB, X16, SyncMode, Cmd are keywords.

Keyword	Description
Manufacturer	NAND Flash Vendor.
PartNo	NAND Flash IC Model.
#CE/RB	Number of targets, only 1/2/4 acceptable.
X16	8/16 bits device width, only Y/N acceptable.
SyncMode	Only Y/N acceptable, Y: Synchronous data interface

	supported; N: Not supported.
Cmd	Cmd is composed of several parts, it's divided with comma.
	1. Complete command name.
	2. Abbreviation of command.
	3. Name of first busy time check. Put a space and add a comma if unused.
	4. Value of first busy time check. Its unit is micro seconds. Put a space and add a comma if unused.
	5. Name of second busy time check. Put a space and add a comma if unused.
	6. Value of second busy time check. Its unit is micro mseconds. Put a space and add a comma if unused.
	7. First flag. It's acceptable command during busy.
	8. Second flag. It can be inserted by some command or not.
	9. Third flag. It can insert into some multi plane command or not.
	10. Command.

Ex: Cmd=Read, Read, tR, 60, , , N, N, N, 00, 30

Cmd=Read Status, Read Stat., , , , Y, N, Y ,70

Cmd=Two-Plane Page Program, TPP Prog., tDBSY, 1, tPROG, 5000,
N, Y, N, 80, 11, 81, 10

Read Status / Two-Plane Page Program : complete command.

Read Stat. / TPP Prog. : abbreviation of command.

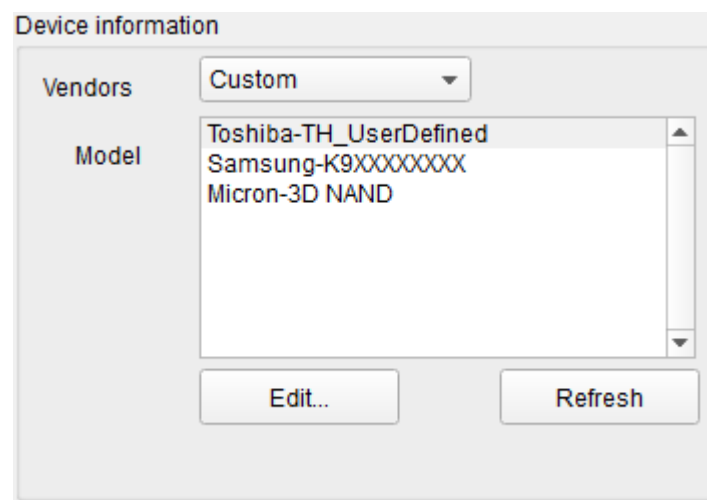
Busy Time Check(tDBSY, 1, tPROG, 5000) : tDBSY is 1us; tPROG is 5000 us. It will show some information when violation of busy time.

3 Flags: 1st flag of "Read Status" is Y means it's acceptable command

During busy; 2nd flag of "Two-Plane Page Program" and 3rd flag of "Read

Status” means any command between 11h and 81h is prohibited except “Read Status (70h)”.

Perform NAND Flash bus analysis, select Custom, the manufacturer name and model entered in the AqNFCustom.txt file will be displayed in the model; the analysis result will also be displayed according to the input command.



NAND Bus Decode Timing Check function description

When using this function, please add the following description in the first paragraph of the content of the custom file AqNFCustom.txt.

```
Manufacturer=Samsung
PartNo=K9XXXXXXXX
Spec=Toggle
Version=2.0
#CE/RB=1
X16=N
SyncMode=Y
TimingCheck=Y
StartupDDR=Y
...
```

1. Spec=Toggle

Only ONFI or Toggle can be filled in.

2. Version=2.0

ONFI fill in SDR/NV-DDR/NV-DDR2-3; Toggle fill in Legacy/1.0/2.0.

3. TimingCheck=Y

Only Y/N can be filled in, Y means the Timing Check function is enabled.

If you turn on the Timing Check function, please fill in the items that need

Timing Check, the format:

Item Name, Minimum Time, Maximum Time

The unit of time value is ns, and for the Timing Check item provided by the software, please fill in the item name specified in the appendix below according to the Spec/Version you set. These are the standard time check items listed in ONFI and Toggle NAND Flash. All other project names will be ignored.

If the time value check item of a certain item is not needed, please fill in X. If the two time values are both X, the item will also be ignored.

The time values listed in the appendix can be adjusted according to the actual NAND Flash specifications during use.

```
TimingParam=tADL, 300, X
TimingParam=tAR, 10, X
TimingParam=tCALH, 5, X
TimingParam=tCALS, 15, X
TimingParam=tCAH, 5, X
TimingParam=tCAS, 5, X
TimingParam=tCDQSH, 100, X
TimingParam=tCH, 5, X
TimingParam=tCLR, 10, X
```

The results will be displayed in the Information field of the report window, and those that violate the set time range will be displayed in red font.

Normally, it will be displayed in black font.

The displayed information will include:

1. Time test item
2. Measurement time
3. Set time range.

Appendix

ONFI								
SDR			NV-DDR			NV-DDR2-3		
tADL	400	X	tAC	3	25	tAR	10	X
tALH	20	X	tADL	400	X	tCAH	5	X
tALS	50	X	tCADf	25	X	tCAS	5	X
tAR	25	X	tCADs	45	X	tCALH	5	X
tCEA	X	100	tCAH	10	X	tCALS	15	X
tCEH	20	X	tCALH	10	X	tCEH	20	X
tCH	20	X	tCALS	10	X	tCH	5	X
tCLH	20	X	tCAS	10	X	tCS	20	X
tCLR	20	X	tCEH	20	X	tCSD	10	X
tCLS	50	X	tCH	10	X	tCLR	10	X
tCOH	0	X	tCK	50	X	tCR	10	X
tCR	10	X	tCKH(abs)	0.43	0.57	tDBS	5	X
tCS	10	X	tCKL(abs)	0.43	0.57	tRHW	100	X
tDH	20	X	tCKWR	0.43	X	tWC	25	X
tDS	40	X	tCS	35	X	tWH	11	X
tITC	X	1000	tDH	5	X	tWHR	80	X

tRC	100	X	tDQSCK	3	25	tITC	X	1000
tREH	30	X	tDQSH	0.4	0.6	tRR	20	X
tRHOH	0	X	tDQSL	0.4	0.6	tWB	X	100
tRHW	X	200	tDQSQ	X	5	tADL	400	X
tRLOH	0	X	tDSC	50	X	tDQSH	0.43	X
tRP	50	X	tDSH	0.2	X	tDQSL	0.43	X
tRR	40	X	tDSS	0.2	X	tWPRE	15	X
tWB	X	100	tHP	0.43	X	tWPST	6.5	X
tWC	100	X	tWPRE	1.5	X	tWPSTH	15	X
tWH	30	X	tWPST	1.5	X	tDH	0.3	X
tWHR	120	X	tWHR	80	X	tDS	0.3	X
tWP	50	X	tFEAT	X	1000	tDSC	3.75	X
tFEAT	X	1000	tRST	X	500000	tAC	3	25
tRST	X	500000				tDQSRE	3	25
						tQSH	0.37	X
						tQSL	0.37	X
						tREH(abs)	0.43	X
						tRP(abs)	0.43	X
						tWP	11	X
						tRPRE	15	X
						tRPST	4.875	X
						tRPSTH	15	X
						tDQSRH	5	X
						tRC	3.75	X
						tCD	3.75	X

						tFEAT	X	1000
						tRST	X	500000

Note: Some Timing Check items will be multiplied by the average value of certain time items, including:

1. tDQSH/tDQSL: $0.45 \times \text{tDSC}(\text{avg})$
2. tQSH/tQSL: $0.37 \times \text{tRC}(\text{avg})$
3. tREH/tRP: $0.43 \times \text{tRC}(\text{avg})$

If the above Timing calculation method is used, the following description must be added to the front end of the file:

```
Manufacturer=Micron
PartNo=3D NAND
Spec=ONFI
Version=NW-DDR2-3
#CE/RB=1
X16=N
SyncMode=Y
TimingCheck=Y
UsedtRCavg=Y
UsedtDSCavg=Y
```

Then check the item input value at that time:

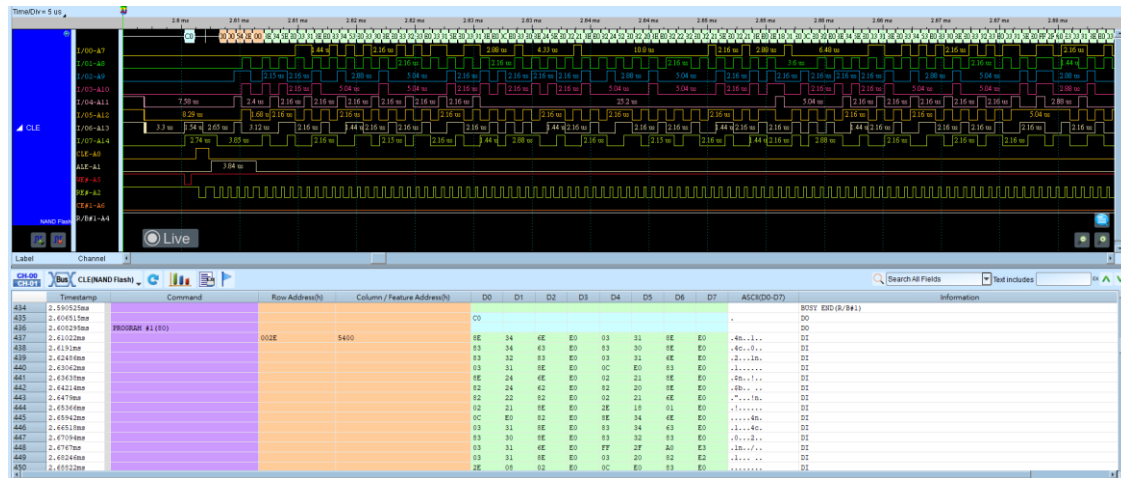
```
TimingParam=tQSH, 0.37, X
TimingParam=tQSL, 0.37, X
TimingParam=tREH(abs), 0.43, X
TimingParam=tRP(abs), 0.43, X
```

If you do not use the above Timing calculation method, you only need to enter UsedtRCavg=N, UsedtDSCavg=N in the file header or remove this description completely, and the value entered for the time check item will be the minimum/maximum value of the time deal with.

Toggle								
Legacy			1.0			2.0		
tCLS	10	X	tADL	300	X	tADL	300	X
tCLS2	40	X	tAR	10	X	tAR	10	X
tCLH	5	X	tCALH	5	X	tCALH	5	X
tCS	15	X	tCALS	15	X	tCALS	15	X
tCH	5	X	tCAH	5	X	tCAH	5	X
tWP	10	X	tCAS	5	X	tCAS	5	X
tALS	10	X	tCDQSH	100	X	tCDQSH	100	X
tALH	5	X	tCH	5	X	tCH	5	X
tDS	5	X	tCLR	10	X	tCLR	10	X
tDH	5	X	tCOH	5	X	tCOH	5	X
tWC	10	X	tCR	10	X	tCR	10	X
tWH	10	X	tCRES	10	X	tCRES	10	X
tADL	300	X	tCS	20	X	tCS	20	X
tRR	10	X	tDH	0.9	X	tDH	0.4	X
tRP	10	X	tDQSH	4	X	tDQSH	2	X
tRC	20	X	tDQSL	4	X	tDQSL	2	X
tCR	9	X	tDQSRE	X	25	tDQSRE	X	25
tCLR	10	X	tDSC	10	X	tRC	5	X
tAR	10	X	tDS	0.9	X	tREH	2	X
tRHOH	25	X	tRC	10	X	tRP	2	X
tRLOH	5	X	tREH	4	X	tRPP	30	X
tREH	7	X	tRP	4	X	tRPRE	15	X
tWHR	30	X	tRPP	30	X	tRPST	27.5	X

tWHC	30	X	tRPRE	15	X	tRPSTH	25	X
tWHR1	180	X	tRPST	27.5	X	tRR	5	X
tWHR2	300	X	tRPSTH	25	X	tWB	X	100
tWB	X	100	tRR	20	X	tWC	25	X
tFEAT	X	1000	tWB	X	100	tWH	11	X
tRST	X	100000	tWC	25	X	tWHR	120	X
			tWH	11	X	tWHR2	300	X
			tWHR	120	X	tWP	11	X
			tWHR2	300	X	tWPRE	15	X
			tWP	11	X	tWPST	6.5	X
			tWPRE	15	X	tWPSTH	25	X
			tWPST	6.5	X	tFEAT	X	1000
			tWPSTH	25	X	tRST	X	500000
			tFEAT	1000	X			
			tRST	500000	X			

Result



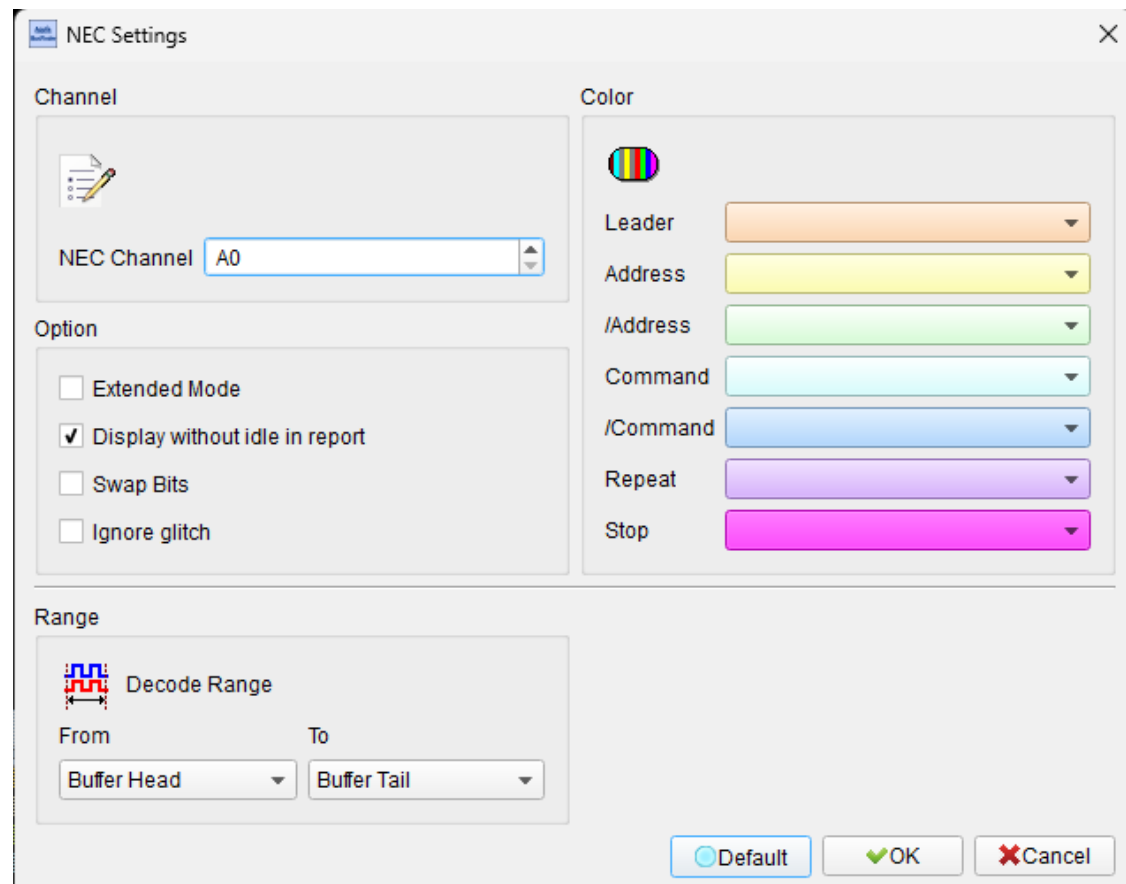
Timing Check

	Timestamp (hh:mm:ss.ms.us.ns)	Command	Row Address(h)	Column / Feature Address(h)	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
29	09:25:05.440.234.699													tWC (152.08 ns):Min(25 ns)
30	09:25:05.440.234.891													tWC (152.50 ns):Min(25 ns)
31	09:25:05.440.235.085													tAR (102.50 ns):Min(10 ns)
32	09:25:05.440.235.085													tWHR (234.17 ns):Min(80 ns)
33	09:25:05.440.235.186													tRPRE (100.83 ns):Min(15 ns)
34	09:25:05.440.235.186													tRP (abc) (100.83 ns):Min(0.43 ns)
35	09:25:05.440.235.189													tRC (103.75 ns):Min(3.75 ns)
36	09:25:05.440.235.189													tWHR (337.92 ns):Min(80 ns)
37	09:25:05.440.235.192													tWPRE (97.08 ns):Min(15 ns)
38	09:25:05.440.235.192													tDQSR (3.33 ns):Min(8 ns)/Max(25 ns)
39	09:25:05.440.235.192													tQSL (97.08 ns):Min(0.37 ns)

NEC IR

NEC IR (NEC Infrared) is a company that specializes in infrared technology and solutions, often referred to as NEC (Nippon Electric Company) products or services in the field of infrared technology.

Settings



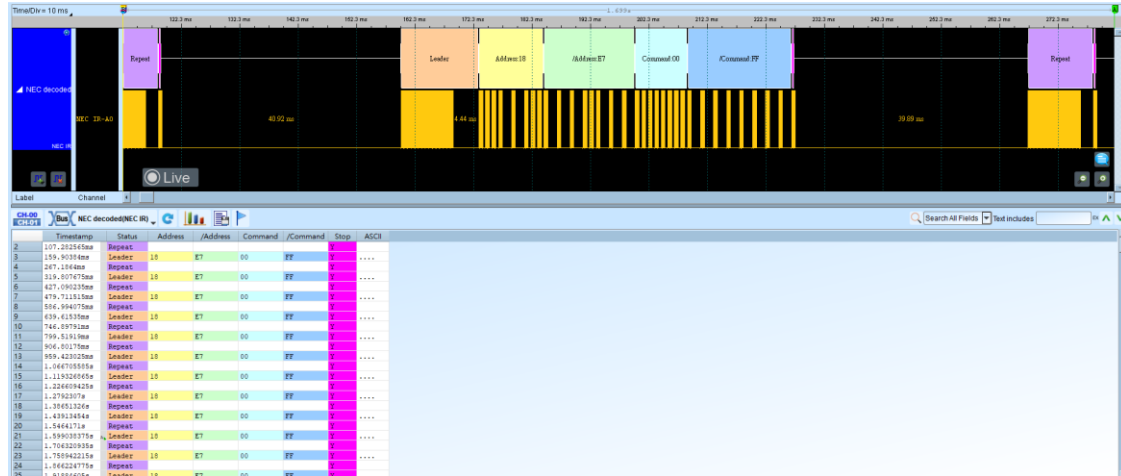
Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Options: Enabled when checked.

1. **Extended Mode:** It integrates /Address and Address into 16 Bits Address, /Command and Command into 16 Bits Command.
2. **Display without idle in report:** It will not idle on the Report Window for the user to observe and analyze data.

3. **Swap Bits:** Switch LSB First to MSB First.
4. **Ignore glitch:** Ignore glitch while analysis. Enabled when checked.

Result



OA3p(PMD)

OA3p (OPEN Alliance 3-pin) is an important protocol in automotive Ethernet testing that defines the requirements for Physical Layer (PHY) testing in automotive environments to ensure the consistency, reliability and stability of the equipment under different operating conditions.

Settings

OA3p (PMD) Settings

Channel

TX: A0
RX(MDC): A1
ED(MDO): A2

Ethernet Settings (10BaseT1S)

☐ Show Sync Code ☐ Show Single BEACON ☐ FCS in Byte Order
☐ Display 5B Code ☐ Show MAC to Each Row
☒ Show MAC Data

Transport Layer Data: [Dropdown]

☐ Data Filter: 20 bytes
 Report Data: 8 Byte

OA3p Settings

Display Mode: TX Data + Config
☐ Show RX Data in NORMAL State

Range

Decode Range
 From: Buffer Head To: Buffer Tail

MDIO Settings (Config State)

☐ Enable Preamble Counter
 32 bits

Data

Data Edge: ☒ Rising ☐ Falling

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

OA3p settings:

- Display Mode:** Display TX Data / RX Data + Config result in waveform area.
- Show Rx Data in NORMAL State:** Show RX analyzed result even the Bus goes into Normal State. Enabled when checked.

OATC6 over SPI

OPEN Alliance Technical Committee 6 (TC6) focuses on improving the media-independent communication interface (xMII) to enhance its use in automotive networks. TC6 develops recommendations for automotive xMII standards and defines related improvements.

Settings

OATC6 over SPI Settings

Channel

CLK: A0
CS: A1
SDI: A2
SDO: A3

Startup Settings

☐ Protected Mode
☐ Enable Timestamp: 64-bit (Default)
Block Payload Size: 64-Byte (Default)
☐ Transmit FCS Validation Enable

Report Settings

☒ Show Ctrl Detail
Waveform Display: SDI

Ethernet Settings

☐ FCS Byte Order
☐ Data Filter: 20 bytes
Report Data: 8 Byte
☒ Show Ethernet Packet

Range

Decode Range
From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Report Settings:

1. **Show Ctrl Detail:** Show the Ctrl detail information in report area.
Enabled when checked.

2. **Waveform Display:** Display the SDI or SDO result in waveform area.

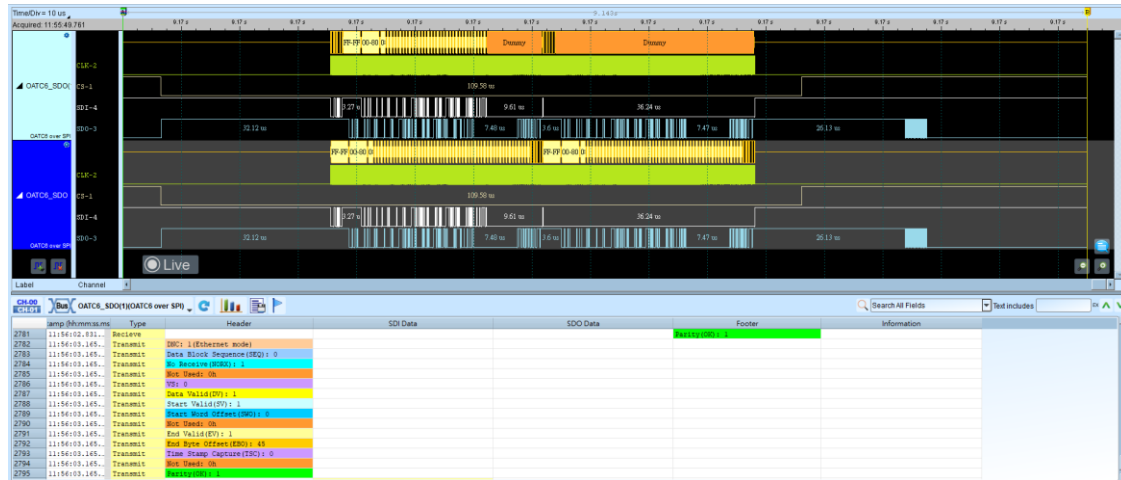
Startup Settings, enabled when checked:

1. **Protected Mode:** Enable or disable the protected format in the control frame.
2. **Enable Timestamp:** Set the output timestamp format. User can choose 64 bit (default value) or 32 bit format.
3. **Block Payload Size:** Assign the Block Payload Size. User can choose 64 bit (default value) or 32 bit format.
4. **Transmit FCS Validation Enable:** Enable Frame Check Sequence (FCS) validation during transmission to ensure data integrity.

Ethernet Settings:

1. **FCS Byte Order:** Present the FCS in Byte order in the report.
2. **Data Filter:** Only how many bytes of data are displayed (at least 20 bytes).
3. **Report Data:** Limits the maximum number of bytes of data that can be displayed in the Data field; the portion that exceeds the setting continues to be displayed on a new line.
4. **Show Ethernet Packet:** Displays Ethernet data such as Address, Data, and FCS.

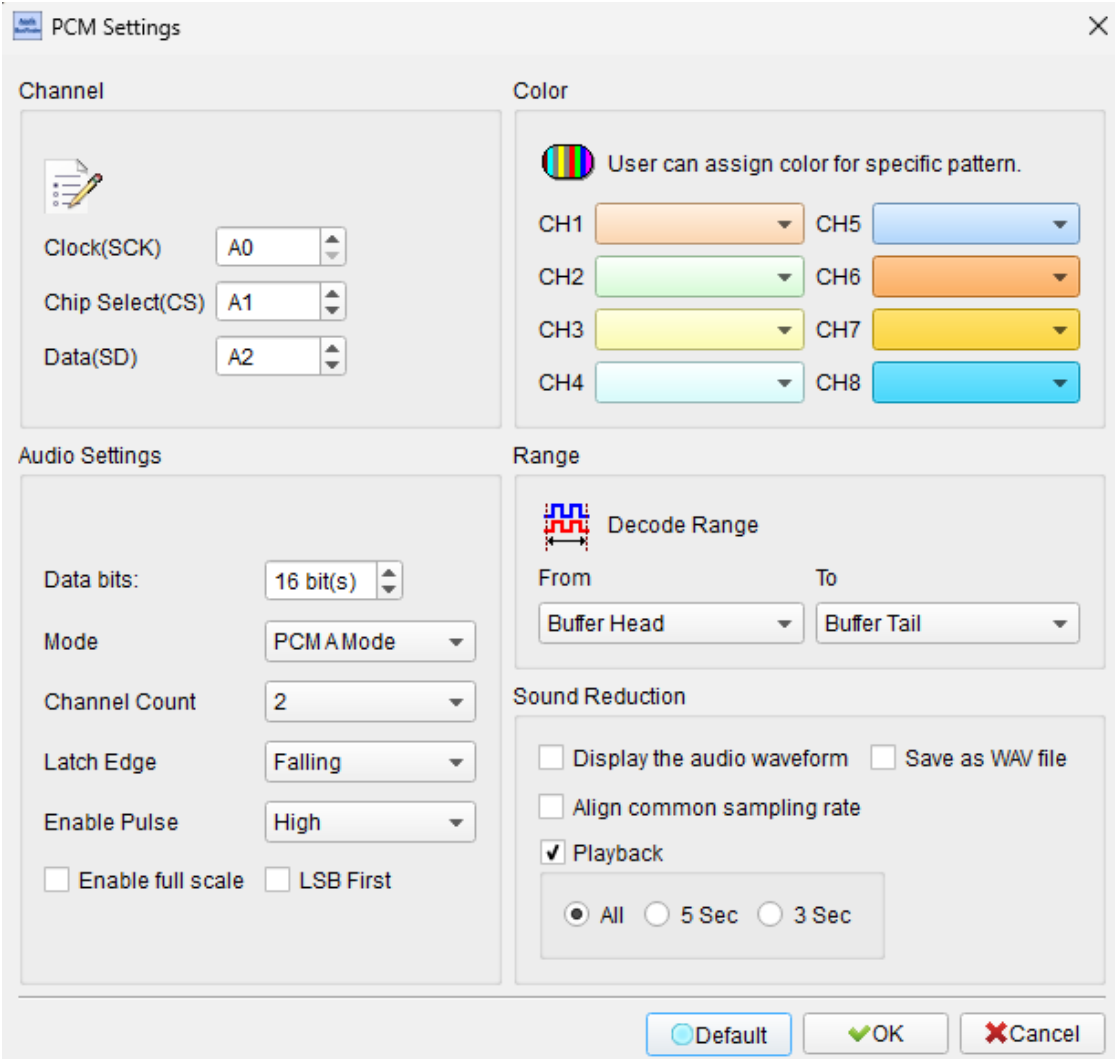
Result



PCM

The format that describes sound as a series of numbers is often referred to as a raw audio file, and the term for it is PCM (Pulse-code modulation). Examples of this format include WAV files on Microsoft Windows (sound files recorded using the "Sound Recorder" software) and AIFF files on Apple platforms. These files belong to this format, typically with a header added at the beginning.

Settings



The PCM Settings dialog box is divided into four main sections: Channel, Color, Audio Settings, and Range.

- Channel:** Contains three dropdown menus for signal assignment: Clock(SCK) set to A0, Chip Select(CS) set to A1, and Data(SD) set to A2.
- Color:** Features a color selection icon and a text prompt: "User can assign color for specific pattern." Below this are eight color-coded dropdown menus for channels CH1 through CH8, each with a unique color (e.g., CH1 is orange, CH2 is green).
- Audio Settings:** Includes several configuration options:
 - Data bits: 16 bit(s)
 - Mode: PCM A Mode
 - Channel Count: 2
 - Latch Edge: Falling
 - Enable Pulse: High
 - Enable full scale: ☐
 - LSB First: ☐
- Range:** Contains a "Decode Range" section with "From" (Buffer Head) and "To" (Buffer Tail) dropdowns.
- Sound Reduction:** Includes checkboxes for "Display the audio waveform", "Save as WAV file", and "Align common sampling rate". The "Playback" checkbox is checked, and below it are radio buttons for "All", "5 Sec", and "3 Sec".

At the bottom of the dialog are three buttons: "Default", "OK", and "Cancel".

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

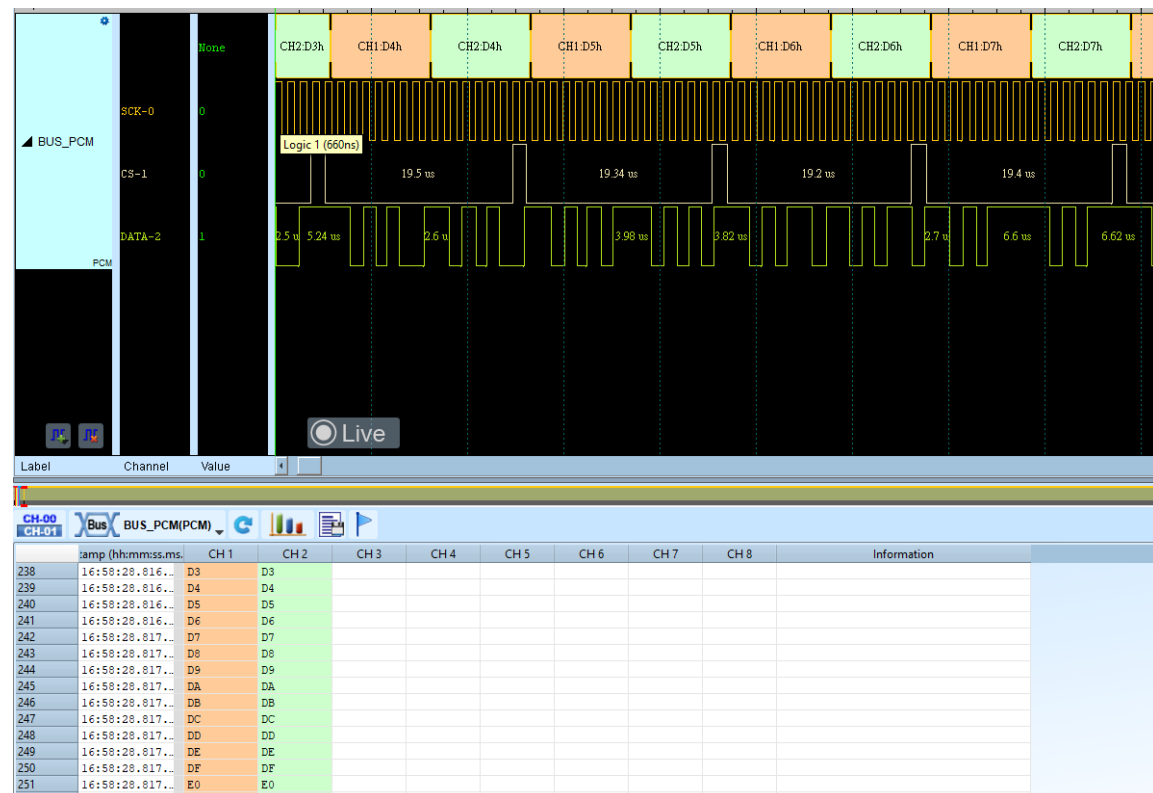
Audio Settings:

1. **Data bits:** Set the PCM Data bit amount.
2. **Mode:** PCM mode settings. User can set to PCM A Mode, PCM B Mode, PCM Multi Mode.
3. **Channel Count:** PCM Channel Number Adjustment
4. **Latch Edge:** Latch data at the clock rising or falling edge.
5. **Enable Pulse:** CS operation settings, can be set to High or Low.
6. **Enable full scale:** Full scale function. Enabled when checked.
7. **LSB First:** Data is arranged in LSB first. Enabled when checked.

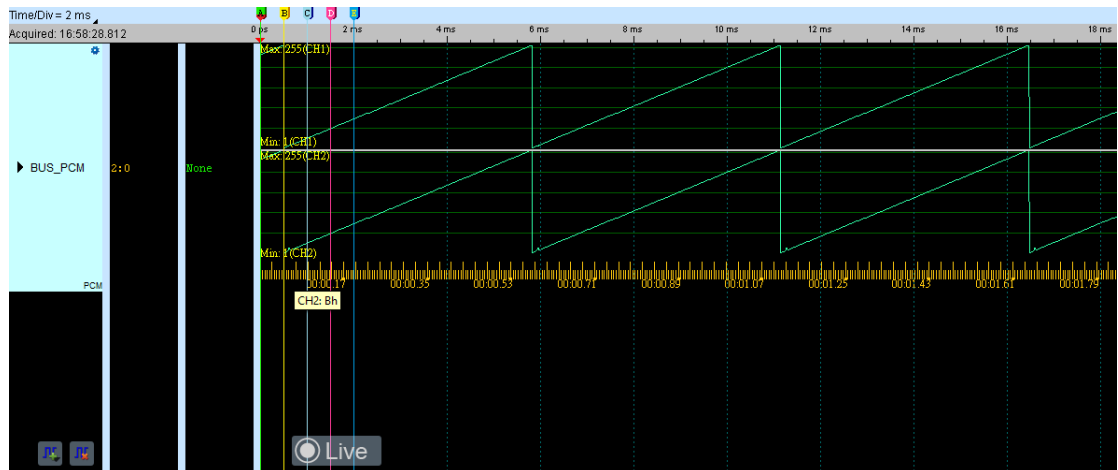
Sound Reduction: Display, playback or save the sound waveform. Enabled when checked.

Result

Packet



Audio



PDM

PDM (Pulse Density Modulation) is a digital signal modulation technique primarily applied in the digitization and transmission of audio signals.

Settings

PDM Settings

Parameter Settings

Clk Channel: A0
Data Channel: A1

Color

L.Channel: [Orange]
R.Channel: [Green]

Detail

☒ Mono: Latch on Rising
☐ Stereo: LCH: Rising RCH: Falling

☐ Show bit stream only

Audio Information

☒ Decimation Parameter: x64
☐ Audio Frequency: 192kHz

☒ Auto Detect Sample Rate
PDM Sample Rate: 4800kHz

Sound reduction

☒ Playback
☐ Display audio waveform

☐ All
☐ 5 sec
☒ 3 sec

☐ Full Scale
☒ Original

☐ Save as WAV file

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Detail:

1. **Mono & Stereo:** Audio mono or stereo selection.

2. **PDM Sample Rate:** PDM Clock Speed
3. **Decimation Parameter:** Calculation parameter for PDM to PCM
4. **Audio Frequency:** PCM audio frequency

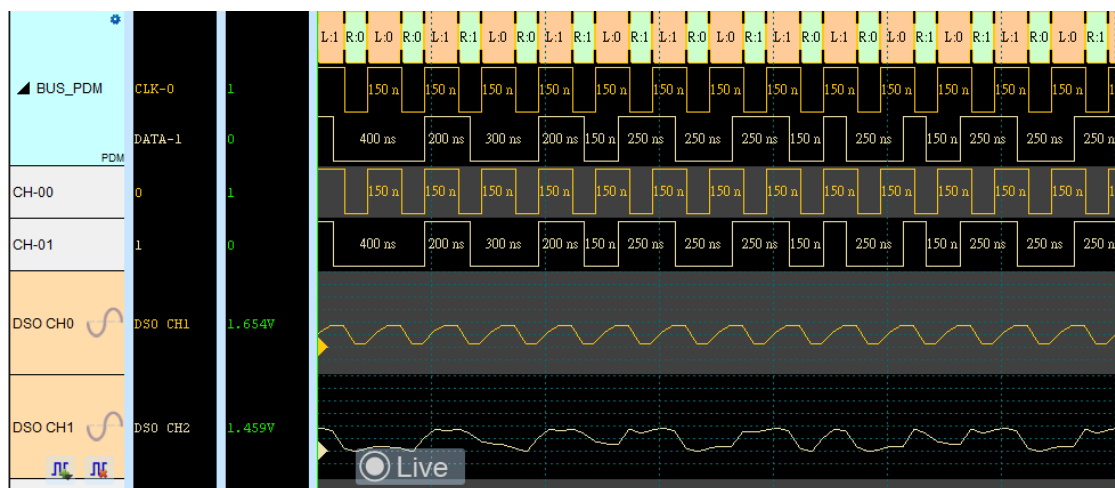
Sound reduction:

1. **Playback:** Set the playback time duration.
2. **Display audio waveform:** Use Full Scale or Original to draw sound waveform in waveform area.

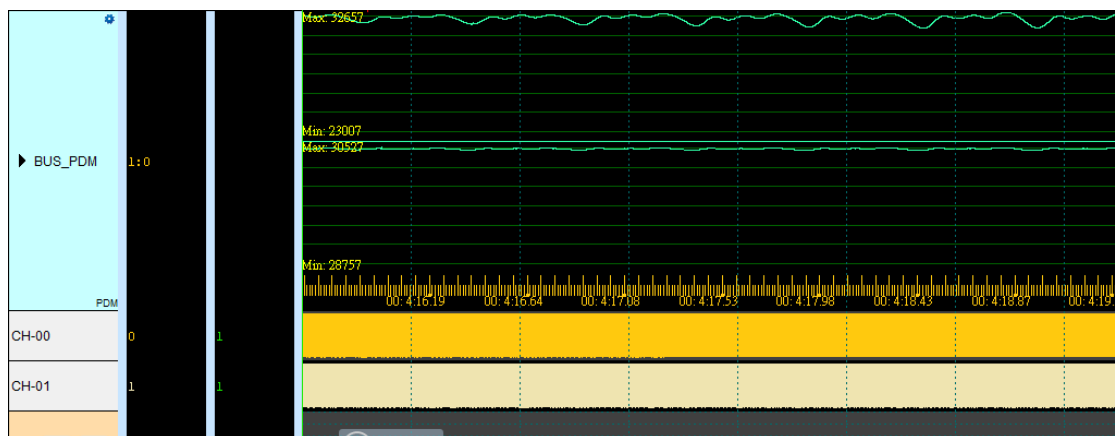
Save as WAV file: Saves the restored sound waveform as a .wav. Enabled when checked.

Result

Normal mode



Audio mode



PECI

Platform Environment Control Interface, Platform management include thermal, power and electrical error monitoring.

Settings

PECI Settings

Parameter

Channel: Data | A0

Report Mode: ☒ Normal ☐ Advance

☐ Do not detect SYNC frame

☐ Do not compare SYNC packets

Color

Sync: [Magenta]

Address: [Orange]

WL / RL: [Yellow]

FCS: [Light Green]

Data: [Light Blue]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

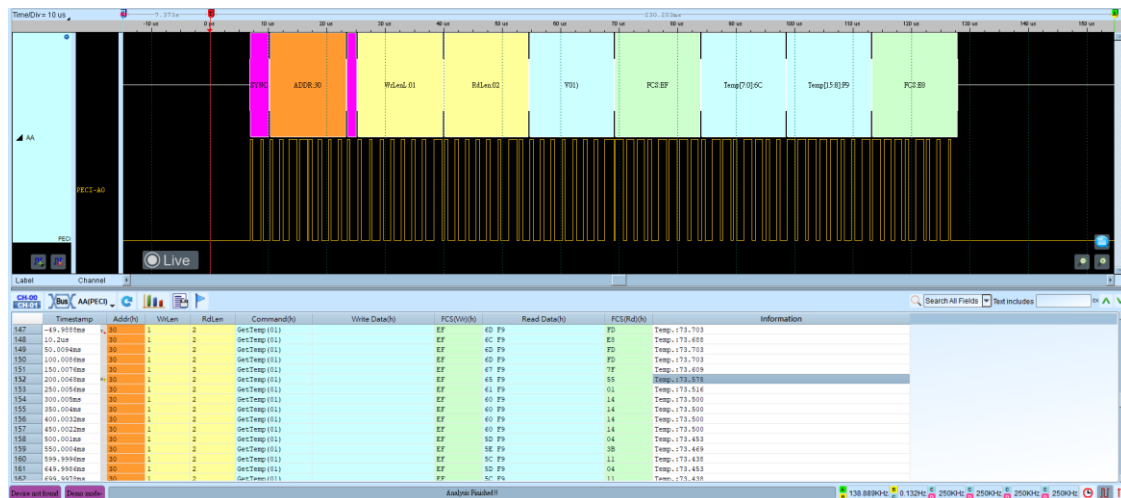
Report Mode: User can choose between Normal and Advanced modes, and the Advanced mode displays more detailed information.

Do not detect SYNC frame: Do not detect SYNC frame. Enabled when checked.

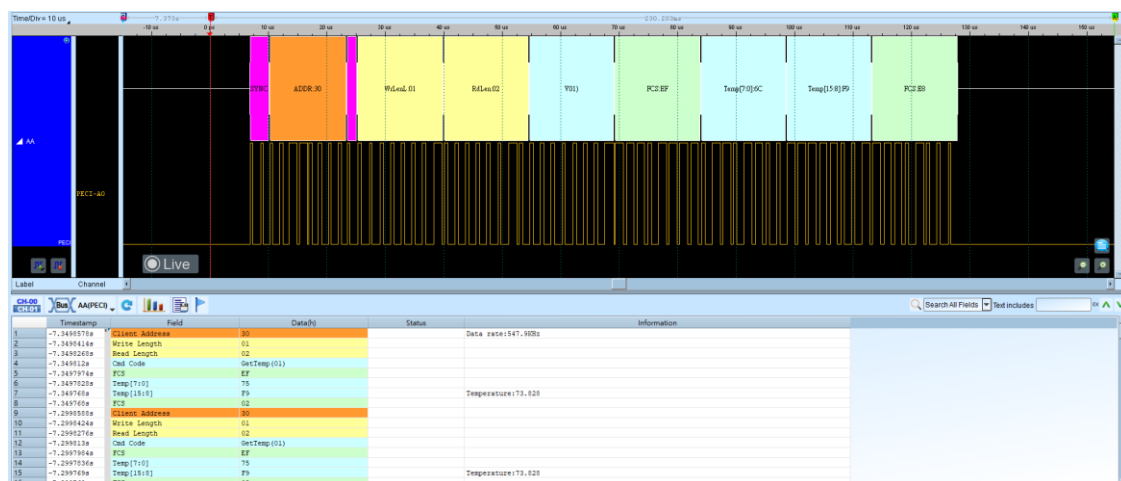
Do not compare SYNC packets: Do not compare SYNC packets. Enabled when checked.

Result

Normal mode



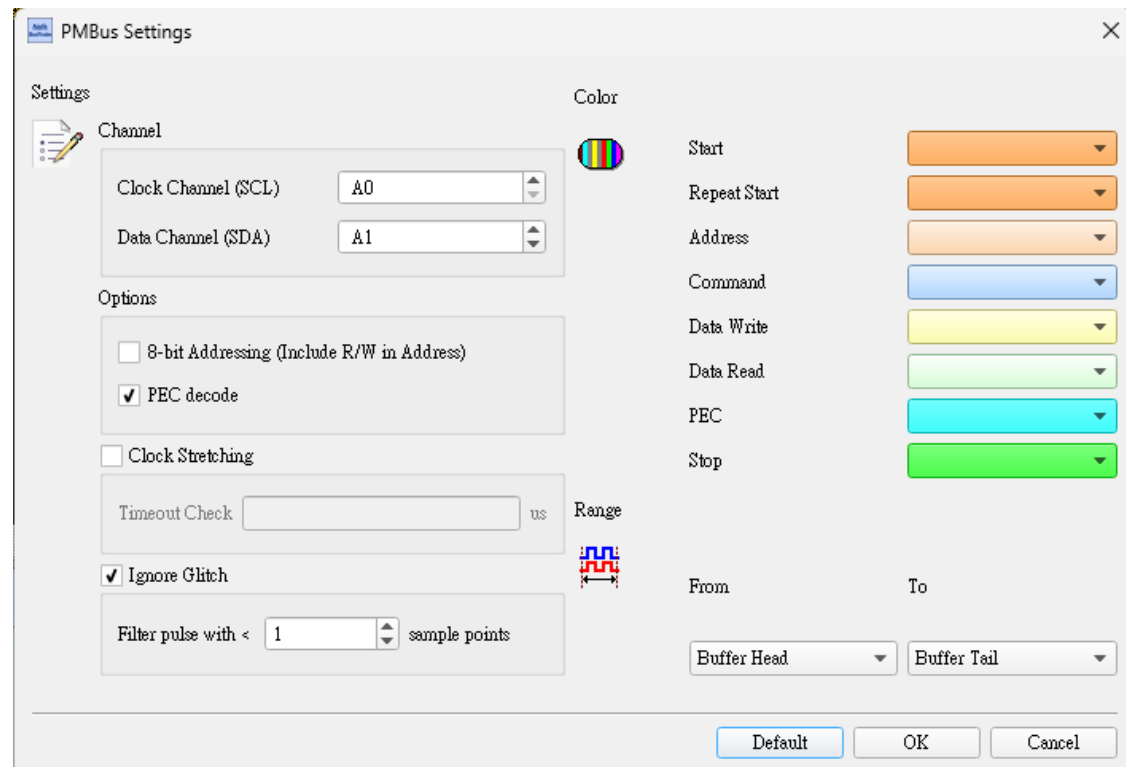
Advance mode



PMBus

The Power Management Bus (“PMBus”) is an open standard protocol that defines a means of communicating with power conversion and other devices.

Settings



Channel:

1. **Clock Channel (SCK):** Transfer clock of PMBus.
2. **Data Channel (SDA):** Transfer data of PMBus.

Options:

1. **8-bit addressing (Including R/W in Address):** Displays an 8-bit width address (7-bit width address plus 1-bit Rd/Wr).
2. **PEC decode:** Set whether the analyzed data contains PEC.

Clock Stretching: Set the time of Clock Stretching. Enabled when checked.

Ignore Glitch: Ignore noise caused by slow transitions when analyzing.

ProfiBus

ProfiBus (PROcess Field Bus) was developed in 1987 by Siemens and other 14 companies and 5 research institutes in Germany, and is widely used in industrial control automation, transportation and power automation, etc.

ProfiBus consists of 3 parts, PROFIBUS FMS (Fieldbus Message Specification), PROFIBUS DP (Decentralized Peripherals), and PROFIBUS PA (Process Automation). Currently, PROFIBUS DP and PROFIBUS PA are the most commonly used.

Settings

ProfiBus Settings

Channel

Configuration Channel

Channel: CH 0

Option

☒ Auto Detect

9600 bps

Start bit: Low

☐ MSB first

☐ Show scale in the waveform

Color

User can assign color for specific pattern.

LE / LRr	SD
SA	DA
DSAP	FC
DU	SSAP
ED	FCS
START	STOP
PARITY	

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal

end is connected on the object to be tested.

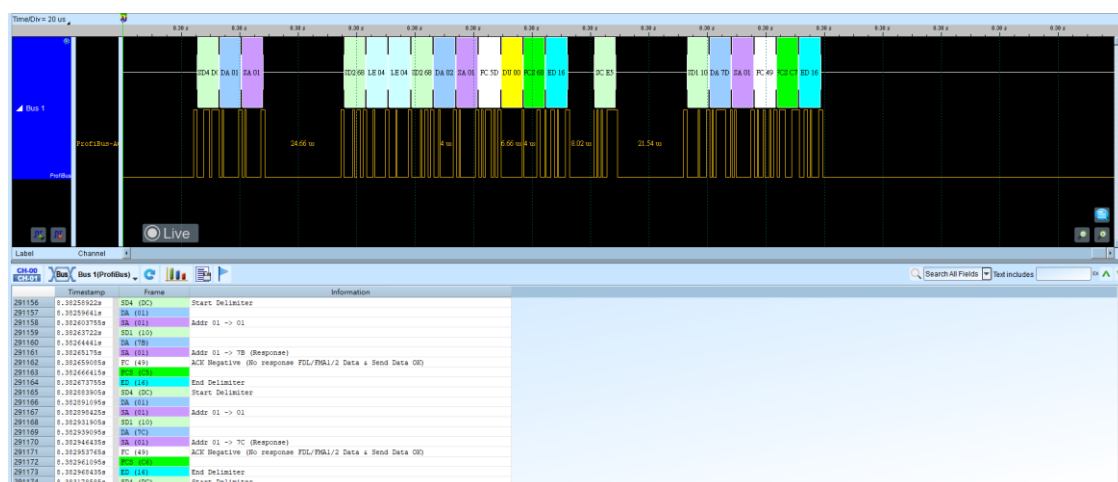
Baud Rate/Auto Detect: Set the baud rate manually or auto detect

Start bit: Set the Start bit to be High or Low.

MSB First: The default is LSB first; click it to change to MSB first.

Show scale in the waveform: Show the scale in the waveform section

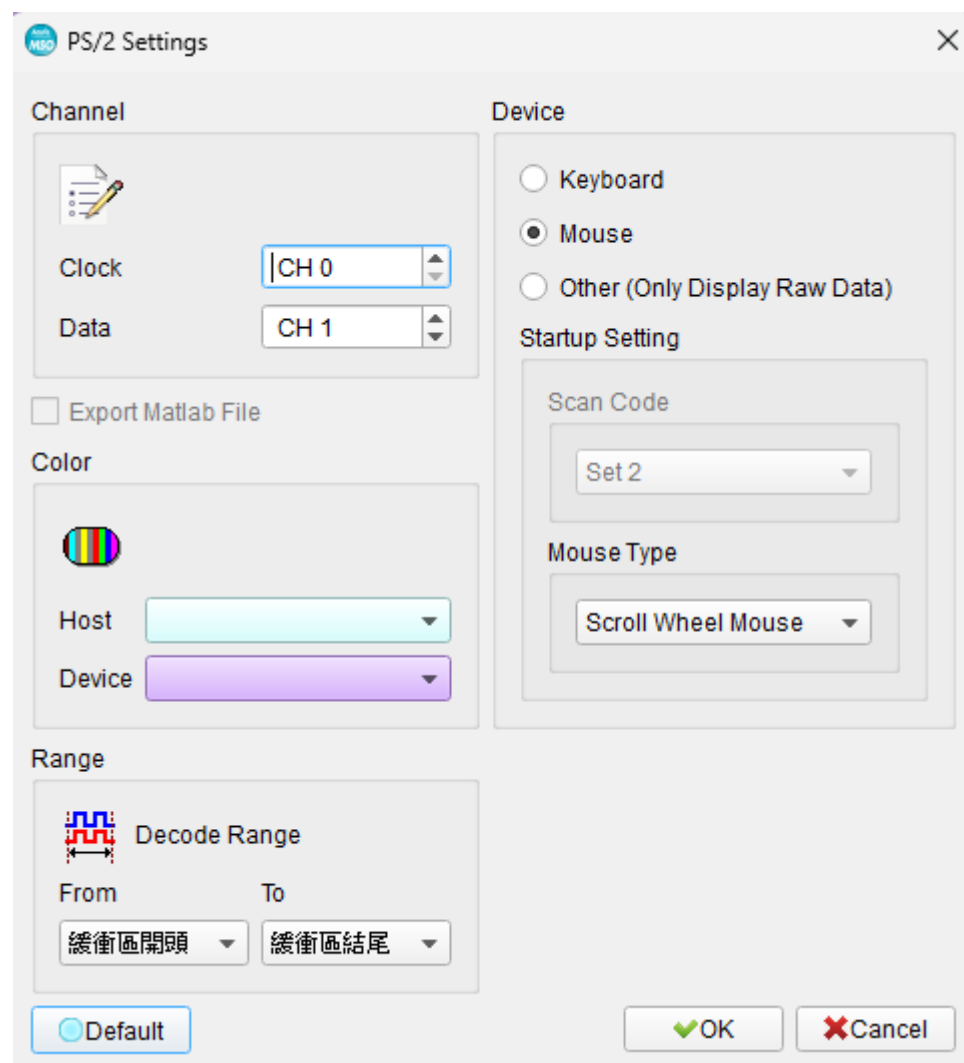
Result



PS/2

PS/2 is a bi-directional synchronous serial protocol for communication between a keyboard or mouse and a PC, developed by IBM, it consists of six pins, namely Clock, Data, +5v, Ground and two blank pins. PS/2 uses a bi-directional synchronous transmission method, whereby data is exchanged between the two ends of the communication via Clock and Data.

Settings



The image shows a 'PS/2 Settings' dialog box with the following sections:

- Channel:** Contains two dropdown menus. 'Clock' is set to 'CH 0' and 'Data' is set to 'CH 1'.
- Device:** Contains three radio buttons: 'Keyboard' (unselected), 'Mouse' (selected), and 'Other (Only Display Raw Data)' (unselected).
- Startup Setting:** Contains a 'Scan Code' dropdown menu set to 'Set 2' and a 'Mouse Type' dropdown menu set to 'Scroll Wheel Mouse'.
- Export Matlab File:** A checkbox that is currently unchecked.
- Color:** Contains a color selection icon (a circle with vertical bars of different colors) and two dropdown menus: 'Host' (set to a light blue color) and 'Device' (set to a light purple color).
- Range:** Contains a 'Decode Range' section with a waveform icon and two dropdown menus: 'From' (set to '緩衝區開頭') and 'To' (set to '緩衝區結尾').
- Buttons:** At the bottom, there is a 'Default' button (with a blue circle icon), an 'OK' button (with a green checkmark icon), and a 'Cancel' button (with a red X icon).

Channel: Show the selected channels.

Export MATLAB file: Export the data with MATLAB format as the following:

Time = [25.78484 25.785985 ...]

Description = [DH DH ...] DH = Device to Host, HD = Host to Device

Data = [58 FA 02 FA C4 ...]

The file (PS2_Matlab.m) will be saved at work directory

Device:

Keyboard: Assign the current device is PS/2 keyboard.

Mouse: Assign the current device is PS/2 mouse.

Other (Only Display Raw Data): Other PS/2 device, only display raw data in this mode.

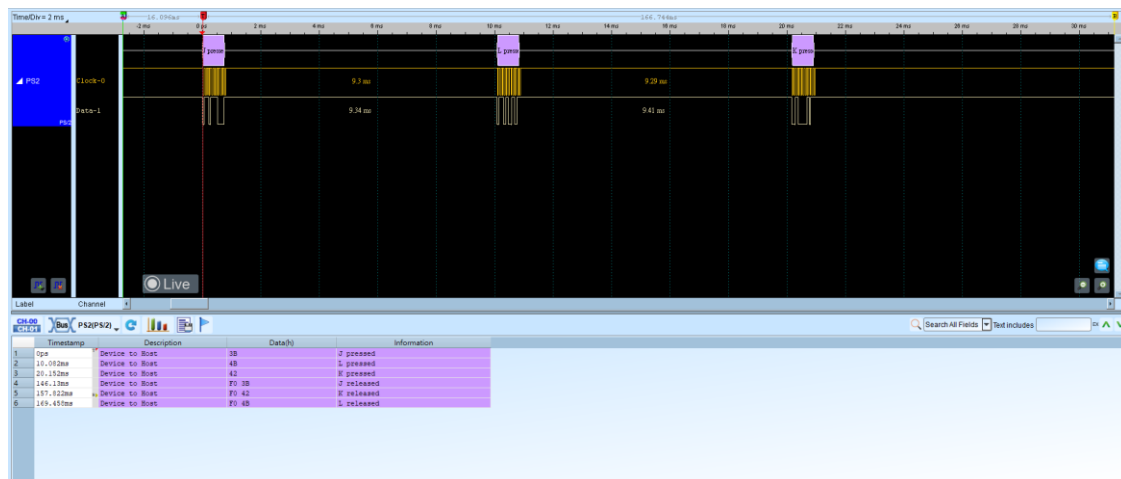
Startup Setting:

Scan Code: Set the Scan Code Set of PS/2 keyboard.

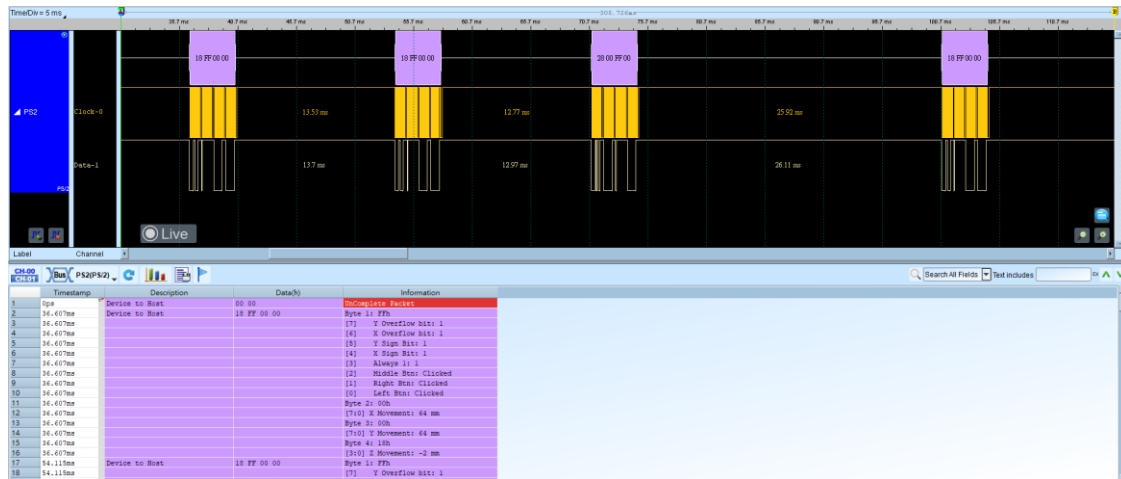
Mouse Type: Set the Type of the PS/2 mouse.

Result

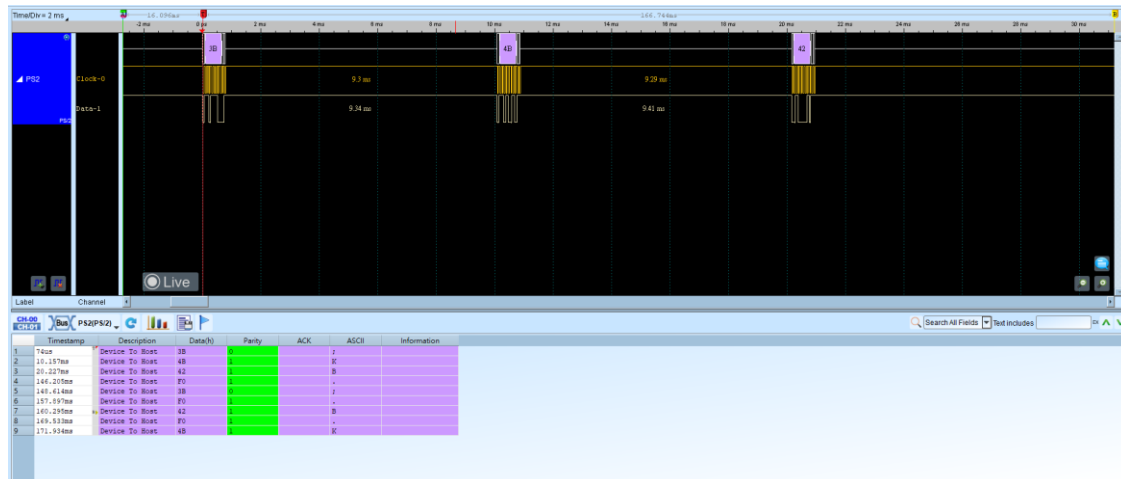
Keyboard:



Mouse:



Other (Only Display Raw Data):



PWM

PWM (Pulse Width Modulation), called pulse width modulation, it is not a bus analysis protocol. It is a very effective technique to control analog circuits by utilizing the pulse width cycle, which is widely used in some rotational speed control, brightness control and temperature control.

Settings

PWM Channel

A0

Option

RPM Conversion(cycles/1 revolution)

1

☐ Show 0%/100% Duty Cycle

Unit of Period Frame

s

☐ Draw PWM Curve

☐ Source

☒
☐
☐

Color

☒ Time(X) - Duty(Y)

☐ Time(X) - RPM(Y)

☐ Time(X) - Freq.(Y)

☐ Draw 0 Hz
 ☐ Speed Curve
 ☐ Encoder

Color

Color

User can assign color for specific pattern.

90% ~ 100%

80% ~ 89%

70% ~ 79%

60% ~ 69%

50% ~ 59%

40% ~ 49%

30% ~ 39%

20% ~ 29%

10% ~ 19%

0% ~ 9%

Range

Decode Range

From

To

Buffer Head

Buffer Tail

Default

OK

Cancel

PWM Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Option:

1. **RPM Conversion (cycles/1 revolution):** Set the number of PWM cycles.
2. **Show 0% and 100% Duty Cycle:** When Time (X)-Period (Y) is selected for plotting, check the box to draw 0% and 100% periods, then the curve will be drawn; otherwise, the curve will not be drawn. If 0% follows 100% or 100% follows 0%, the curve of the two periods will not be drawn.
3. **Unit of Period Frame:** Set the unit of time, user can set s, ms, us.

Draw PWM curve:

1. **Source:** Show the source waveform of the PWM.
2. **Time(X)-Duty(Y):** Show the curve diagram with Time(X) and Duty(Y)
3. **Time(X)-Freq.(Y):** Show the curve diagram with Time(X) and Freq.(Y)
4. **Time(X)-RPM(Y):** Show the curve diagram with Time(X) and RPM(Y)
5. **Draw 0 Hz:** When select the Time(X)-Freq.(Y) drawing and check the item Draw 0 Hz, will show the Frequency from 0 Hz at Y axis.
6. **Speed Curve:** Supports up to three Curves for overlay drawing.

Speed Curve

Curve1

Pulse: A0 Color: Yellow

Direction: A1 Direction Message: H(1):Positive

☐ **Curve2**

Pulse: A2 Color: Green

Direction: A3 Direction Message: H(1):Positive

☐ **Curve3**

Pulse: A4 Color: Cyan

Direction: A5 Direction Message: H(1):Positive

☐ Draw Composed Curve

☐ Red line to draw 0 speed axis

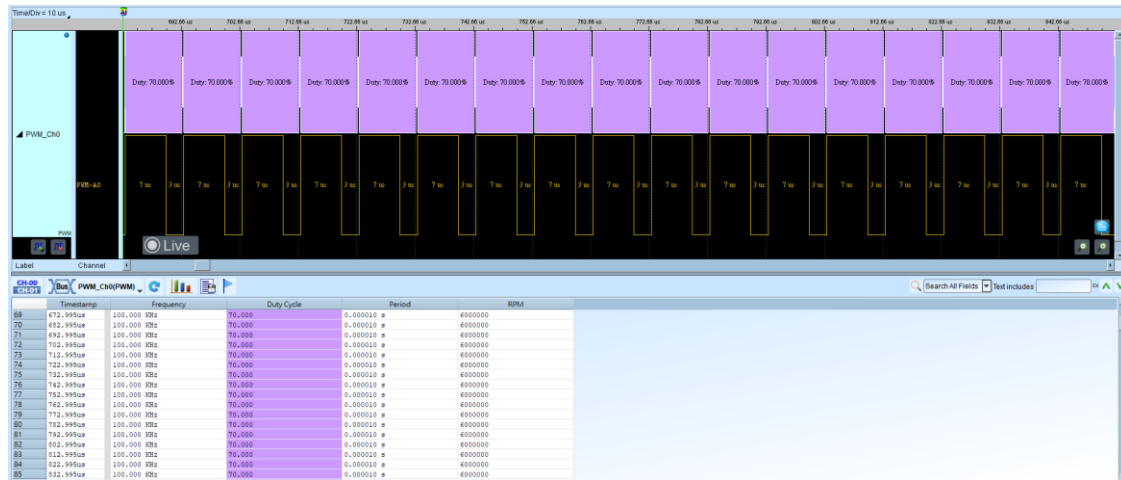
OK Cancel

Pulse/Direction: Setting the pulse and direction of the signal channel on the instrument.

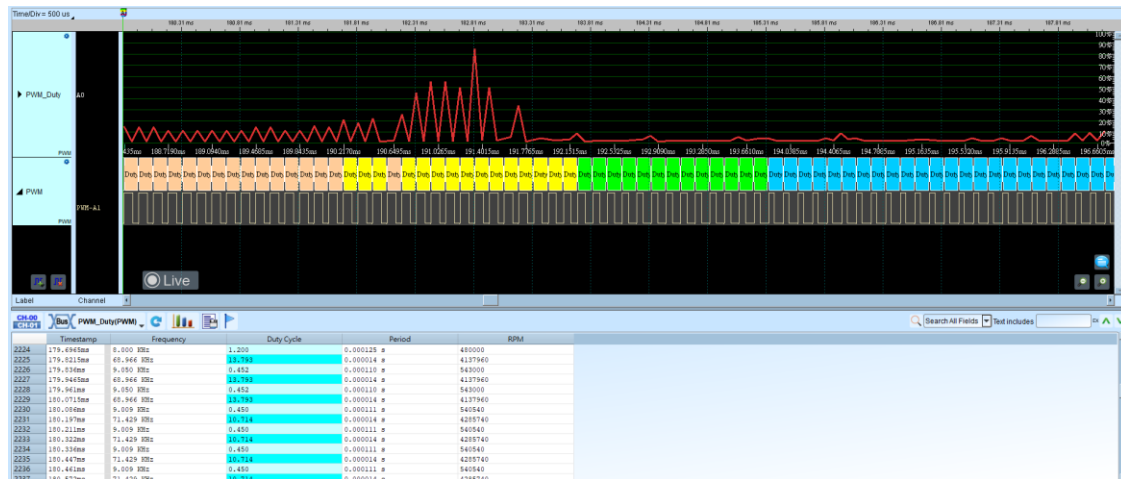
Direction Message: Set the direction source to H(1): Positive or L(0): Positive.

- Encoder:** Encode the PWM parsing result, enabled when checked.

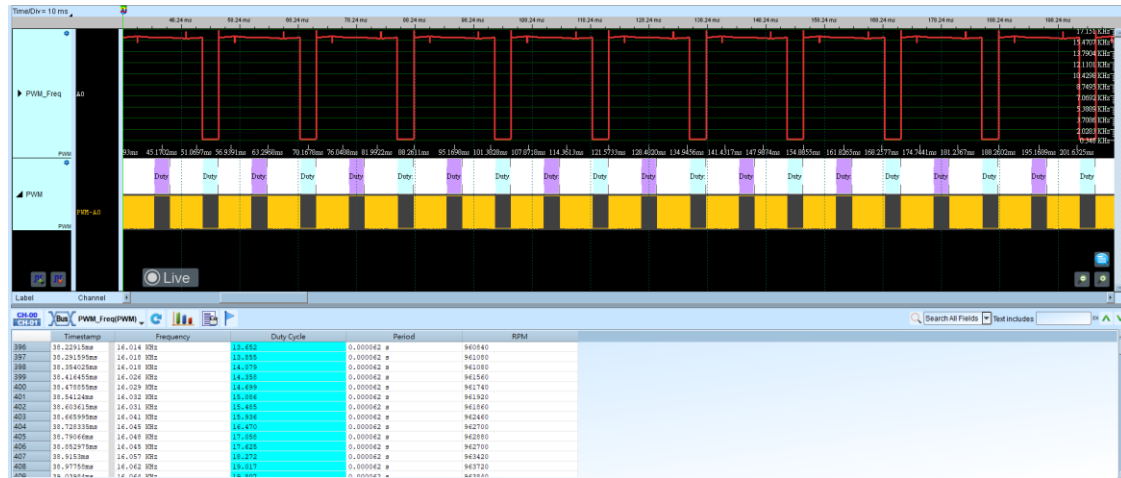
Result



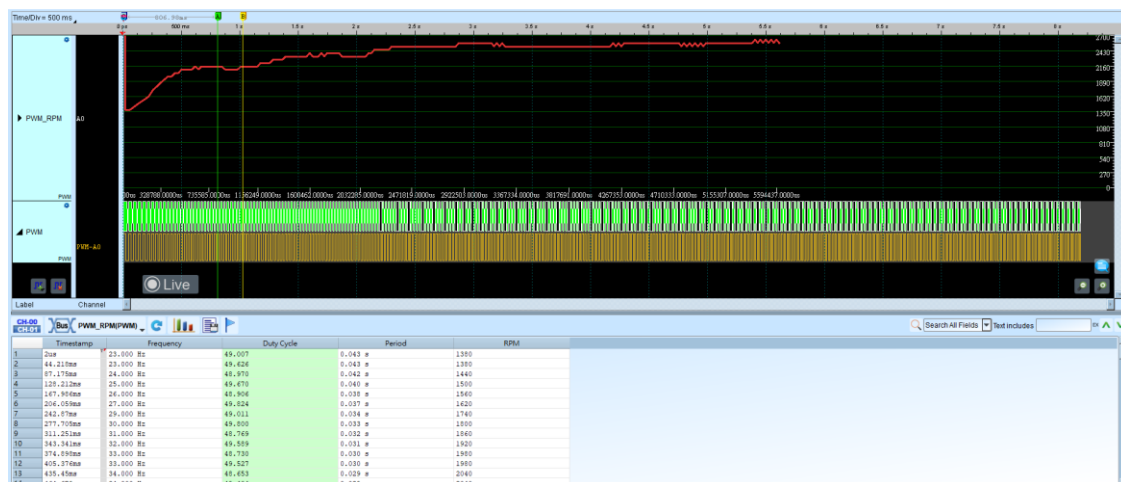
Select Time(X)-Duty(Y)



Select Time(X)-Freq.(Y)



Select Time(X)-RPM(Y)



QEI

QEI (Quadrature Encoder Interface) is a feedback signal (encoder) for small motor control. The QEA/QEB signal is used to obtain the RPM of the motor, and the INDX signal can be used to obtain the angle of rotation of the motor.

Settings

The screenshot shows the 'QEI Settings' dialog box. It is divided into three main sections: 'Setting', 'Color', and 'Range'.
 - The 'Setting' section on the left contains a 'Channel' sub-section with three dropdown menus: 'QEA' set to 'A0', 'QEB' set to 'A1', and 'INDX' set to 'A2' (with a checked checkbox). Below these is a 'Pulse/Rotation' text box containing the value '400'. At the bottom of this section are two unchecked checkboxes: 'Start 0 degree at Rising Edge' and 'Draw Curve'.
 - The 'Color' section on the top right features a color wheel icon and two dropdown menus labeled 'Angle' and 'Speed'.
 - The 'Range' section on the bottom right includes a 'Decode Range' icon and two dropdown menus labeled 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail').
 - At the bottom of the dialog are three buttons: 'Default' (with a blue circle icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

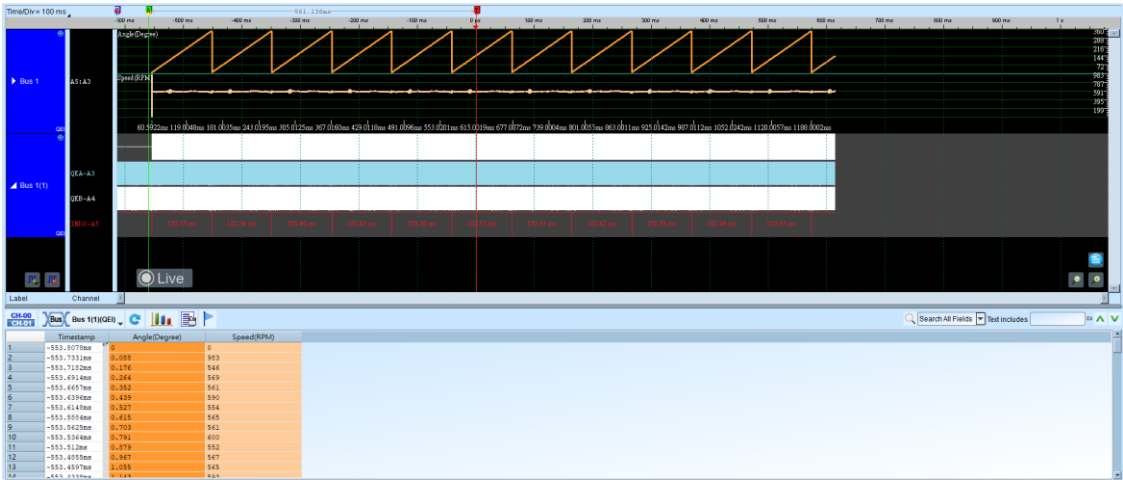
Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Pulse/Rotation: Set the number of lines of the encoder, the default is 400 lines.

Start 0 degree at Rising Edge: Sets the rising edge of the INDX signal to an angle of 0 degrees; the default is for the falling edge to be at an angle of 0 degrees. Enabled when checked.

Draw Curve: Whether draw the angle/speed curve. Enabled when checked.

Result



QI

QI is a contactless power transfer protocol published by Wireless Power Consortium (WPC). It is a method of contactless power transfer from a Base Station to a Mobile Device, which is based on near field magnetic induction between coils.

Settings

QI Parameter Settings

Setting

QI Channel: A0 ☐ Advanced Decode

Color

Preamble: [Orange] Start [Blue]

Head: [Light Orange] Parity [Purple]

Message: [Yellow] Stop [White]

Checksum: [Green]

Range

Decode Range

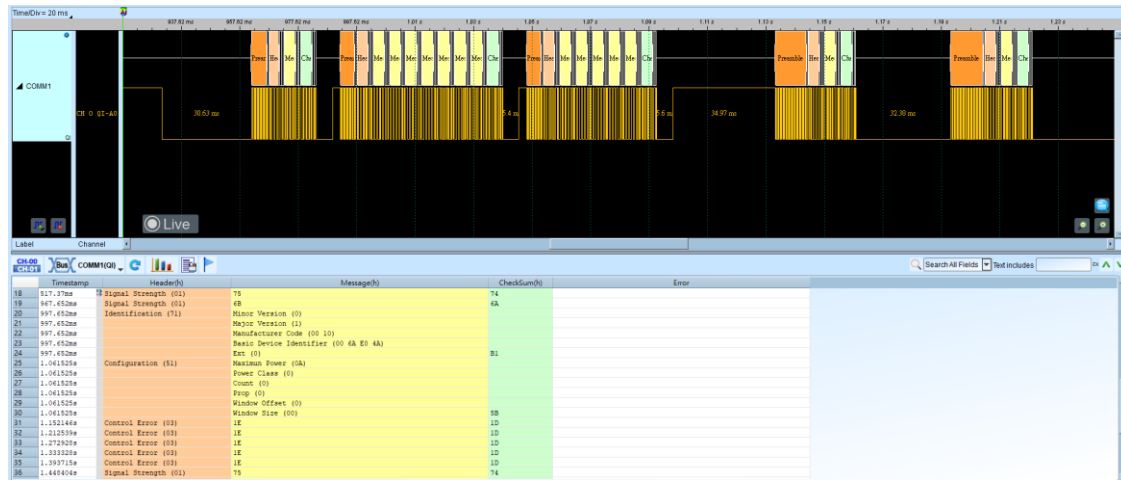
From: Buffer Head To: Buffer Tail

☐ Default

QI Channel: Show the selected channel.

Advance Decode: show detail message decode

Result



QSPI

QSPI is an enhanced version of SPI, which uses additional data lines to increase throughput in DATA; The data line of QSPI is bidirectional and belongs to parallel transmission

Settings

QSPI Settings

Settings

Channel

☒ CS A0 Low Active

CLK A1

D0 A2 D4 A6

D1 A3 D5 A7

D2 A4 D6 A8

D3 A5 D7 A9

Mode CMD+ADDR MSB

Significant Bit (D0) MSB

Latch Edge Rising

Bus Width 4

Report Column 8

☐ Image Restoration Settings

☐ User Define Format Settings 0

Color

CMD

Address

Data

Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Channel:

CS: Capture data when CS edge is falling.

CLK: Clock channel.

D0-D7: Customizable data channel.

Mode: Set the mode of QSPI. It can be set to CMD+ADDR, CMD or DATA, and it can be set to MSB first or LSB first.

Significant Bit(D0): D0 is the MSB or LSB of the data arrangement,

- Take Bus Width = 4 MSB as an example, the Byte combination is D0 D1 D2 D3 D0 D1 D2 D3
- Take Bus Width = 4 LSB as an example, the Byte combination is D3

D2 D1 D0 D3 D2 D1 D0

Latch Edge: Rising/Falling/Both can be selected as the data collection location

Bus Width: Optional data 1, 2, 4, 8 lines

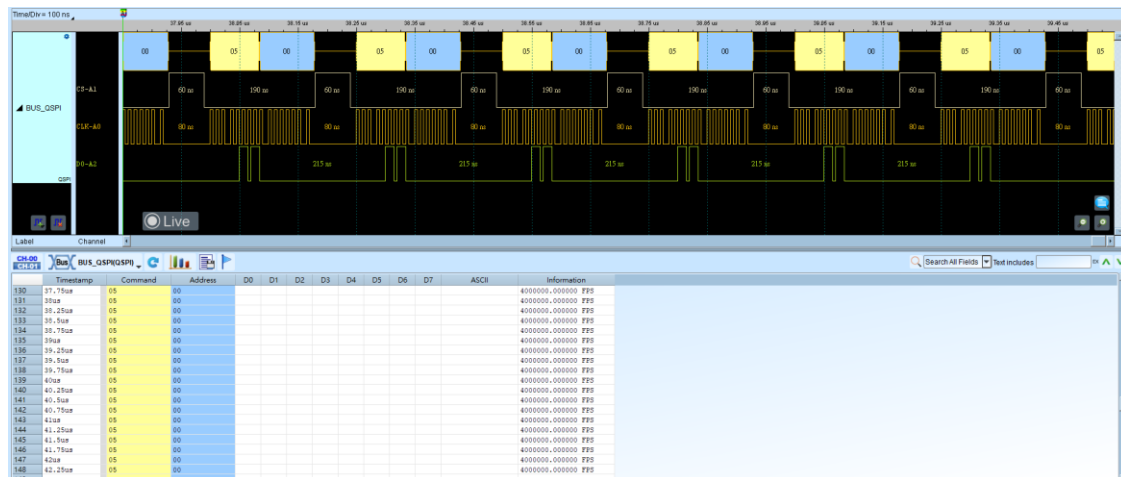
Report Column: Report presentation mode, 8/16 fields can be selected

Image Restoration: Save the parsed waveform as a picture for additional reading of the configuration file. Enabled when checked.

User Defined Format: User-defined parsing format, which can read additional configure files. Enabled when checked.

**** Please note that Image Restoration and User Define Format cannot be enabled at the same time **.**

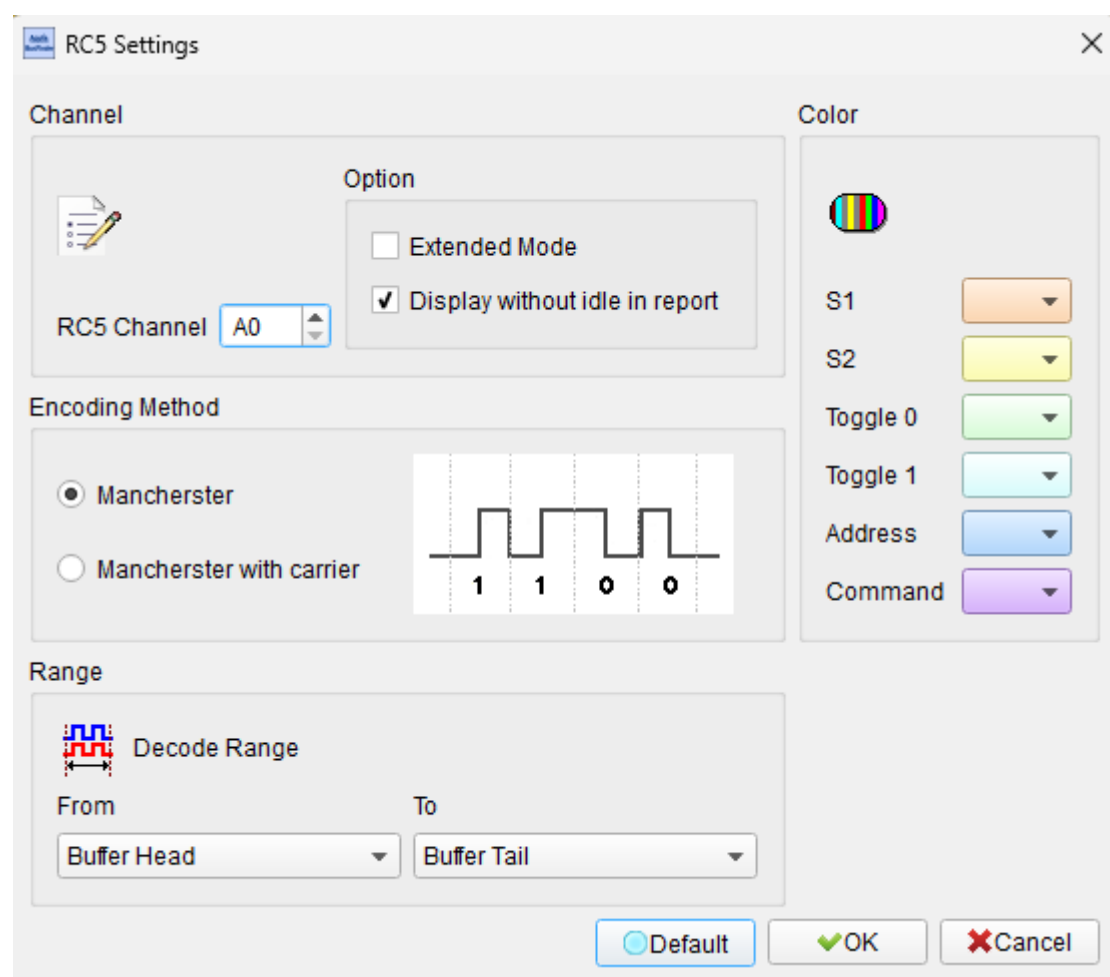
Result



RC-5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. The protocol is well defined for different device types ensuring compatibility with your whole entertainment system.

Settings



The RC5 Settings dialog box is divided into several sections:

- Channel:** Includes a document icon, a dropdown menu for 'RC5 Channel' set to 'A0', and an 'Option' section with checkboxes for 'Extended Mode' (unchecked) and 'Display without idle in report' (checked).
- Encoding Method:** Features two radio buttons: 'Manchester' (selected) and 'Manchester with carrier'. To the right is a timing diagram showing a square wave for the binary sequence 1 1 0 0.
- Range:** Contains a 'Decode Range' section with 'From' and 'To' dropdown menus, both set to 'Buffer Head' and 'Buffer Tail' respectively.
- Color:** A vertical panel on the right with a color bar icon and six color-coded dropdown menus: S1 (orange), S2 (yellow), Toggle 0 (green), Toggle 1 (cyan), Address (blue), and Command (purple).

At the bottom right, there are three buttons: 'Default' (with a blue circle icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Option:

1. **Extended mode:** When the Extended enabled, the S2 will be converted

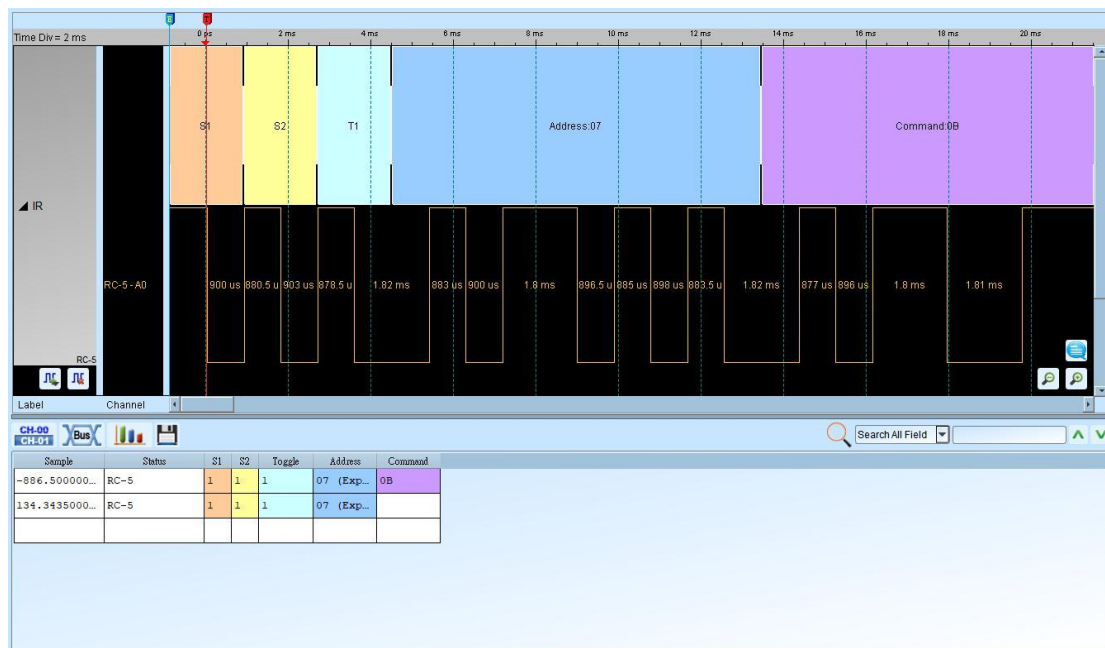
into seventh bit of the Command. There is an Extend Command on the Waveform Window.

2. **Display without idle in report:** It will not idle on the Report Window for the user to observe and analyze data.

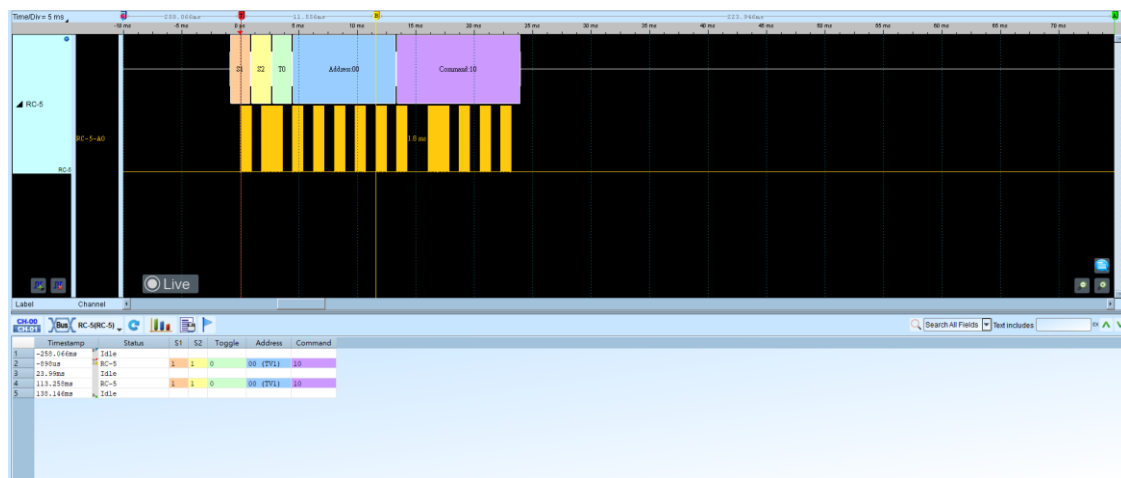
Encoding Method: Manchester mode and Manchester with carrier mode.

Result

RC5 without carrier



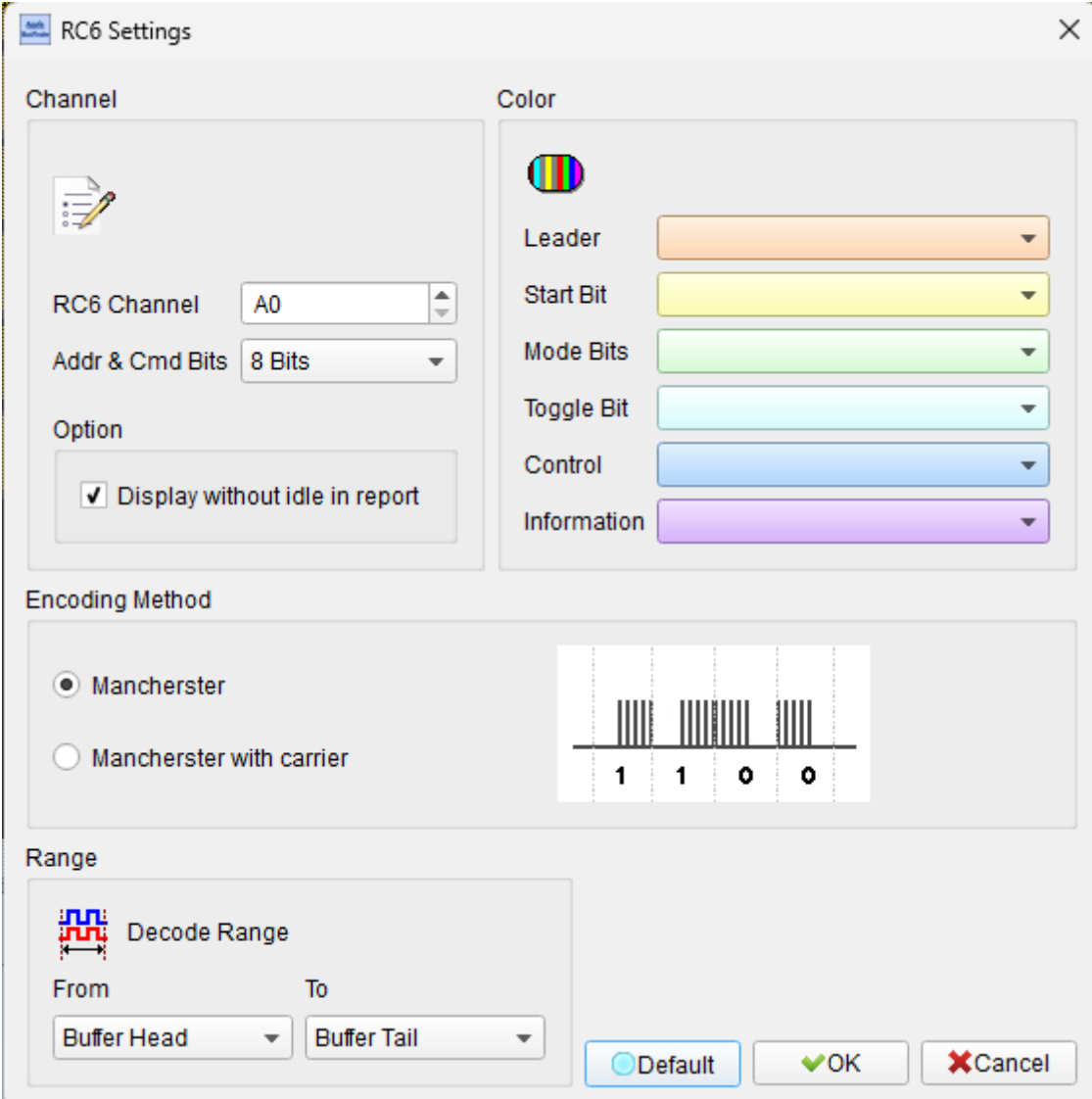
RC5 with carrier



RC-6

RC-6, like RC-5, is also developed by Philips. But, RC-6 has more features of remote controls than RC-5.

Settings



The RC6 Settings dialog box is divided into several sections:

- Channel:**
 - RC6 Channel: A0
 - Addr & Cmd Bits: 8 Bits
 - Option: ☒ Display without idle in report
- Color:**
 - Leader: [Orange dropdown]
 - Start Bit: [Yellow dropdown]
 - Mode Bits: [Light Green dropdown]
 - Toggle Bit: [Light Blue dropdown]
 - Control: [Blue dropdown]
 - Information: [Purple dropdown]
- Encoding Method:**
 - ☒ Manchester
 - ☐ Manchester with carrier

Timing diagram showing four pulses corresponding to the binary sequence 1 1 0 0.
- Range:**
 - Decode Range: [Icon]
 - From: Buffer Head
 - To: Buffer Tail

Buttons at the bottom: Default, OK, Cancel.

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

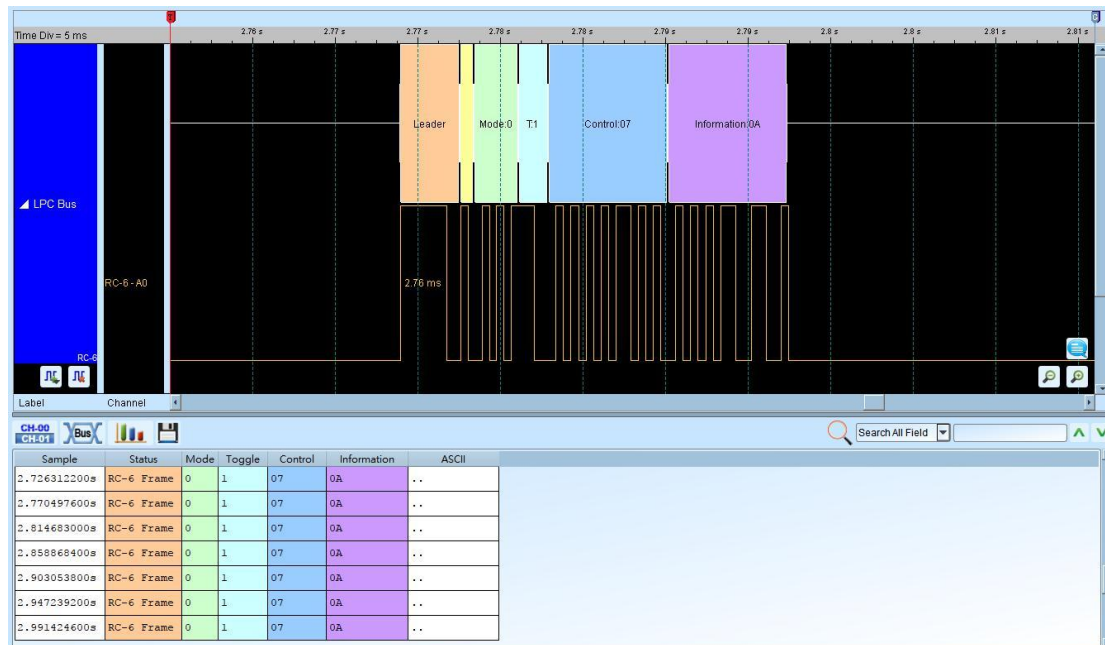
Add & Cmd Bits: Show commands in 8 bits or 16 bits of address and information in the control label.

Display without idle in report: Do not display any idle in the Report Window.

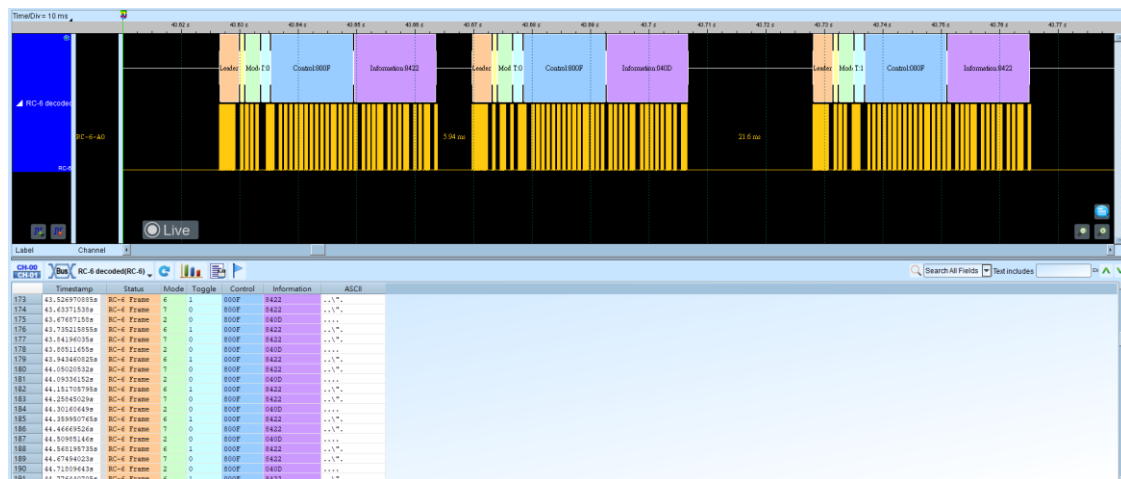
Encoding Method: Manchester mode, Manchester with carrier mode.

Result

RC6 without carrier



RC6 with carrier



RGB Interface

RGB Interface is for data transmission between MCU and LCD. LCD Panel can be driven by LCD controller. RGB data would be written in memory and can be transmitted to LCD controller. It is able to show the picture of LCD Panel by reading the data from the interface.

Settings

RGB_IF Settings

Channel

SCLK

A0

R0

A4

G0

A12

B0

A20

DE

A1

R1

A5

G1

A13

B1

A21

HSYNC

A2

R2

A6

G2

A14

B2

A22

VSYNC

A3

R3

A7

G3

A15

B3

A23

R4

A8

G4

A16

B4

A24

R5

A9

G5

A17

B5

A25

R6

A10

G6

A18

B6

A26

R7

A11

G7

A19

B7

A27

Format

RGB888

Save as JPG File

A (Alpha)

R (Red)

G (Green)

B (Blue)

L (Luminance)

0 bits

8 bits

8 bits

8 bits

0 bits

Color

HSYNC

VSYNC

DATA

Range

Decode Range

From

To

Buffer Head

Buffer Tail

Default

OK

Cancel

Channel

SCLK: The Clock pin.

DE: The Data Enable pin.

Hsync: The Horizontal synchronization pin.

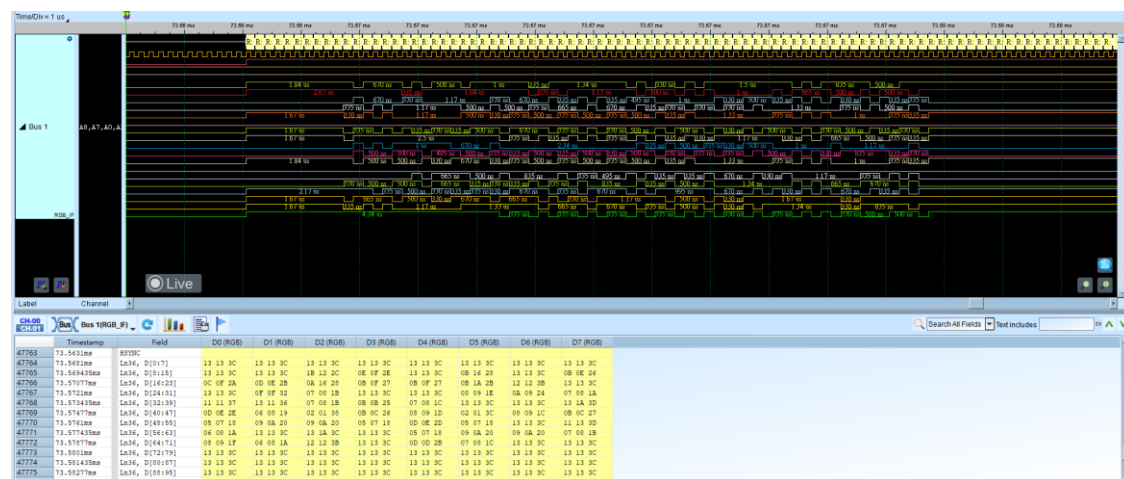
Vsync: The Vertical synchronization pin.

R0 – 7, G0 – 7, B0 – 7: RGB data pins.

Format: Select one of RGB formats or User defined.

Save as JPG file: Generate the JPG file with RGB data in the work directory of LA.

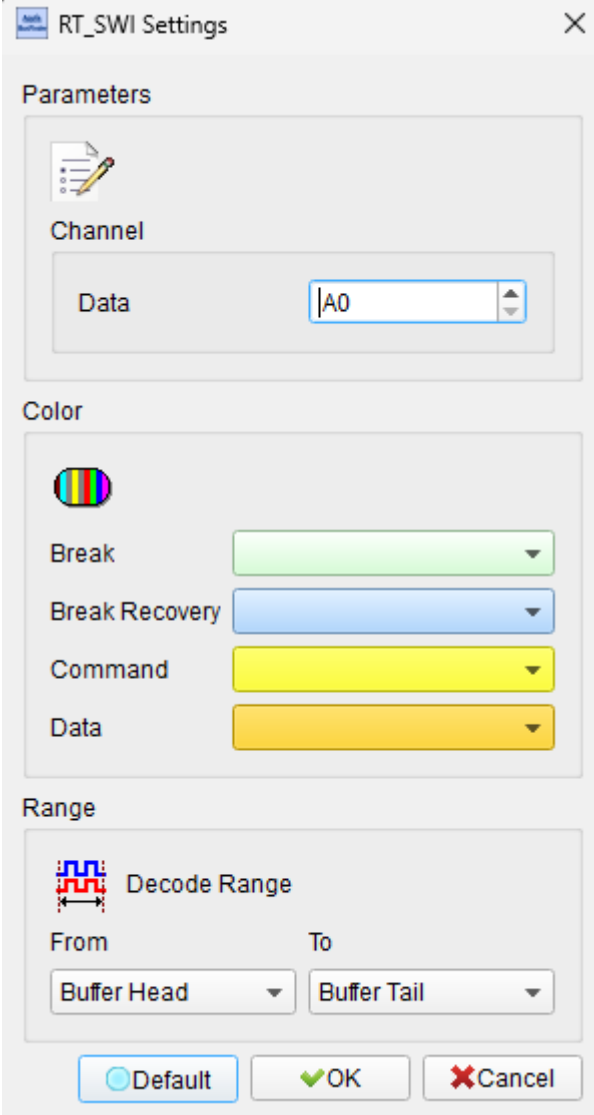
Result



RT_SWI

Realtek Single Wire Interface (SWI) is a communication protocol provided by Realtek. It is an interface designed for data transfer over a single data wire. This interface can help simplify hardware design, reduce wiring complexity, and effectively save space and cost.

Settings



The image shows the 'RT_SWI Settings' dialog box. It has a title bar with a close button. The dialog is divided into three main sections: 'Parameters', 'Color', and 'Range'. The 'Parameters' section contains a 'Channel' label and a text box with 'A0'. The 'Color' section has a color selection icon and four dropdown menus labeled 'Break' (green), 'Break Recovery' (blue), 'Command' (yellow), and 'Data' (orange). The 'Range' section has a 'Decode Range' label with a waveform icon, and two dropdown menus labeled 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail'). At the bottom are three buttons: 'Default' (with a blue circle icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

RT_SWI Settings

Parameters

Channel

Data A0

Color

Break

Break Recovery

Command

Data

Range

Decode Range

From To

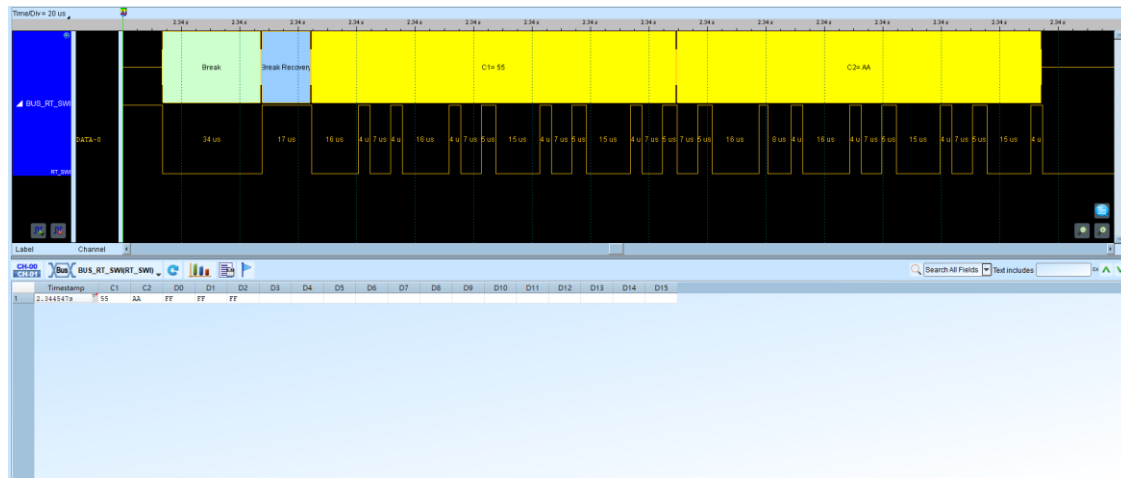
Buffer Head Buffer Tail

Default OK Cancel

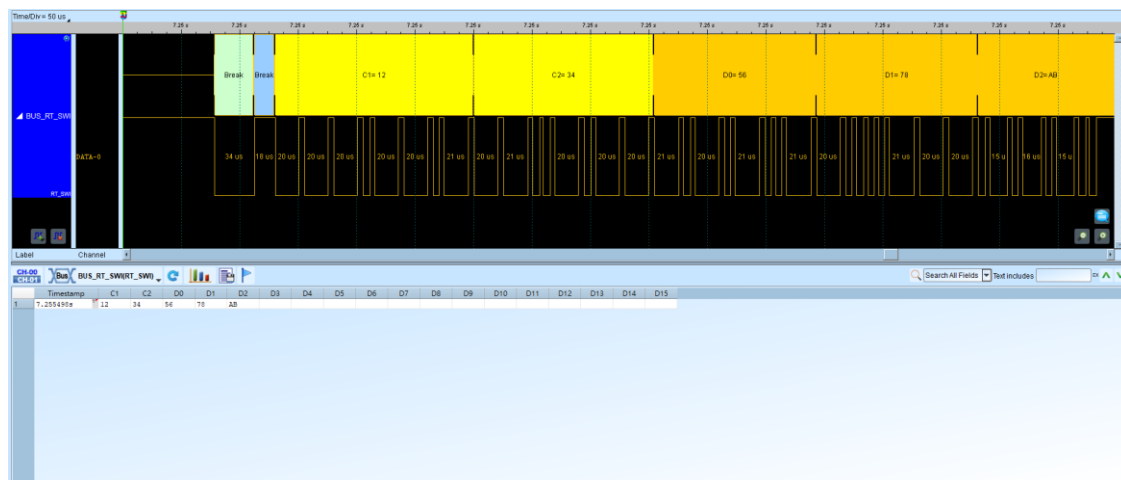
Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Result

Read



Write



SAE J1850

SAE J1850 is an automotive communication protocol used primarily for on-board diagnostics (OBD) and in-vehicle networking. It was widely used in vehicles before CAN (Controller Area Network) became the standard. J1850 allows different electronic control units (ECUs) to communicate within a vehicle.

Settings

J1850 Settings

Parameter

Channel: A0

Bit Order: ☐ LSB First ☒ MSB First

☐ Invert Waveform

Manufacture: GM

Color

SOF: [Color Picker] IFR: [Color Picker]

DATA: [Color Picker] EOF: [Color Picker]

EOD: [Color Picker] IFS: [Color Picker]

NB: [Color Picker] BRK: [Color Picker]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Transfer Method

☐ PWM ☒ VPW

PWM Parameters:

- Active Phase "1": 8 us
- Active Phase "0": 16 us
- Bit Time: 24 us
- SOF/EOD Time: 48 us
- EOF Time: 72 us
- IFS Time: 96 us
- Active SOF: 32 us
- Active BRK: 40 us
- BRK to IFS Time: 120 us

VPW Parameters:

- Short Pulse: 64 us
- Long Pulse: 128 us
- SOF/EOD Time: 200 us
- EOF Time: 280 us
- BRK Time: 300 us
- IFS Time: 300 us

Buttons: Default OK Cancel

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Bit Order: Select the transferred bit order. Default is MSB first.

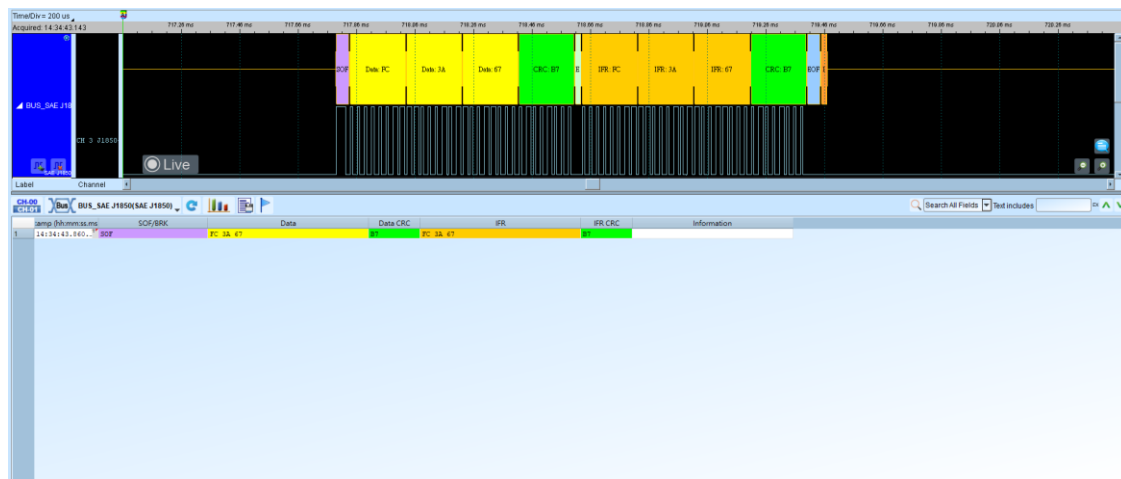
Invert Waveform: Invert the waveform for analyzing. Enable while checking.

Manufacture: Select the Manufacture. Due to different manufacture defined different NB value to indicate enable CRC or not. Please note that, this combo box can only be accessed when the transferred method had been adjusted to VPW. We only support GM and Chrysler now, if user need more manufacture candidate, please contact us.

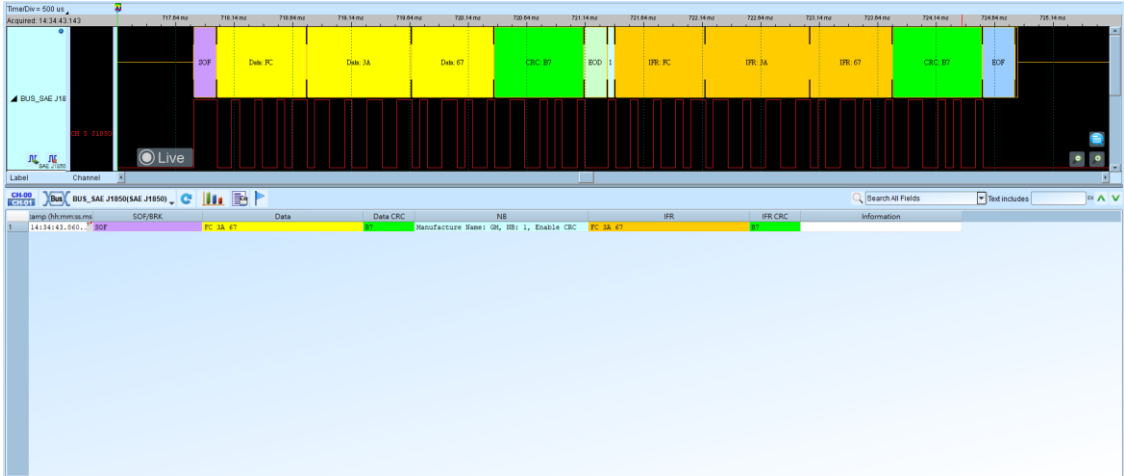
Transfer Method: Select the transferred method. Default is VPW. PWM and VPW has different timing parameters. User can adjust the value manually.

Result:

PWM:



VPW:



S/PDIF

It is a digital audio interface that can be transmitted using either wire or fiber optics. It is called the Sony/Philips Digital Interconnect Format (also known as Sony Philips Digital InterFace). These two companies are the primary specification developers, and the specification is derived from the AES/EBU professional digital audio interface, with some modifications for use in lower-cost hardware.

Settings

S/PDIF Settings

Setting

Channel: A0

☒ Auto detect Bit Rate

49.152 (768 kHz) Mb/s
(384Kb/s~49.152Mb/s)

☐ Display the audio waveform

Block

192 (32 ~ 192) frames

Data Bits: 16

Bit Order

Aux Data: LSB first

Audio Data: LSB first

Parity mode

Even parity

☒ Playback

Color

Preamble: [Cyan]

Aux Data: [Orange]

Audio Data: [Yellow]

Validity bit: [Light Yellow]

User bit: [Light Green]

Channel Status bit: [Light Blue]

Parity Bit: [Purple]

Range

Decode Range

From: Buffer Head To: Buffer Tail

☐ Default ☒ OK ☐ Cancel

Channel: The default is Channel 0.

Auto detect Bit Rate: Turned on by default.

Num of frame: 192 frames within each block by default, used to analyze each sub-frame order User bit and Channel status bit.

Bit Order (Aux. Data): The default is the LSB first for the Aux. data.

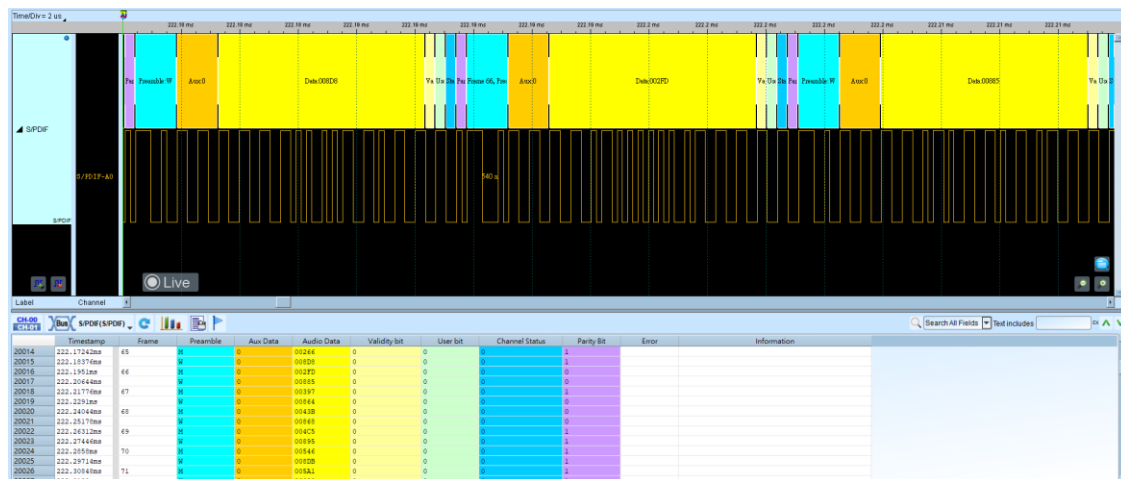
Bit Order (Audio Data): The default is the LSB first for Audio data.

Data format: The default is 16 bits.

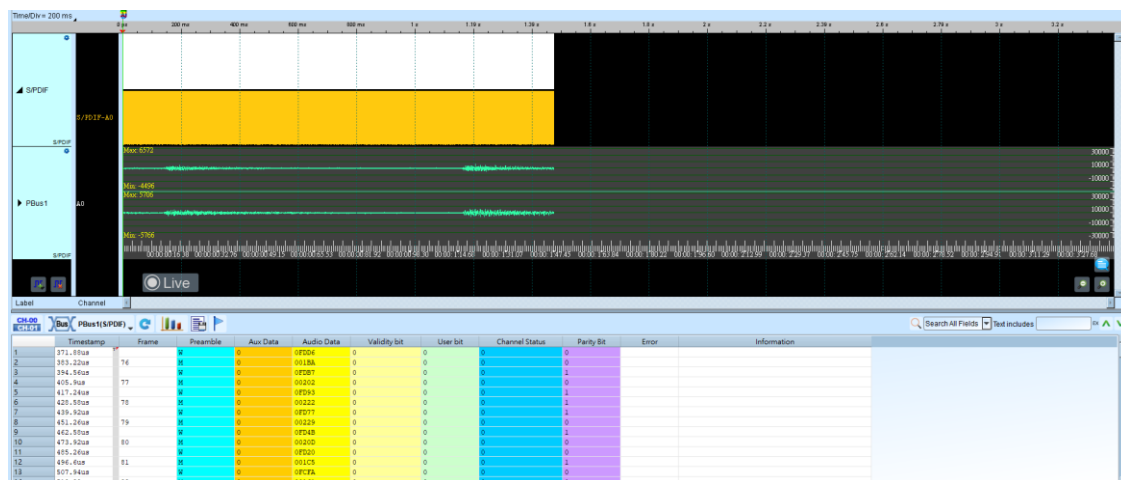
Parity mode: The default is even parity.

Display the audio waveform: Click to display the audio waveform in the Waveform Window.

Result



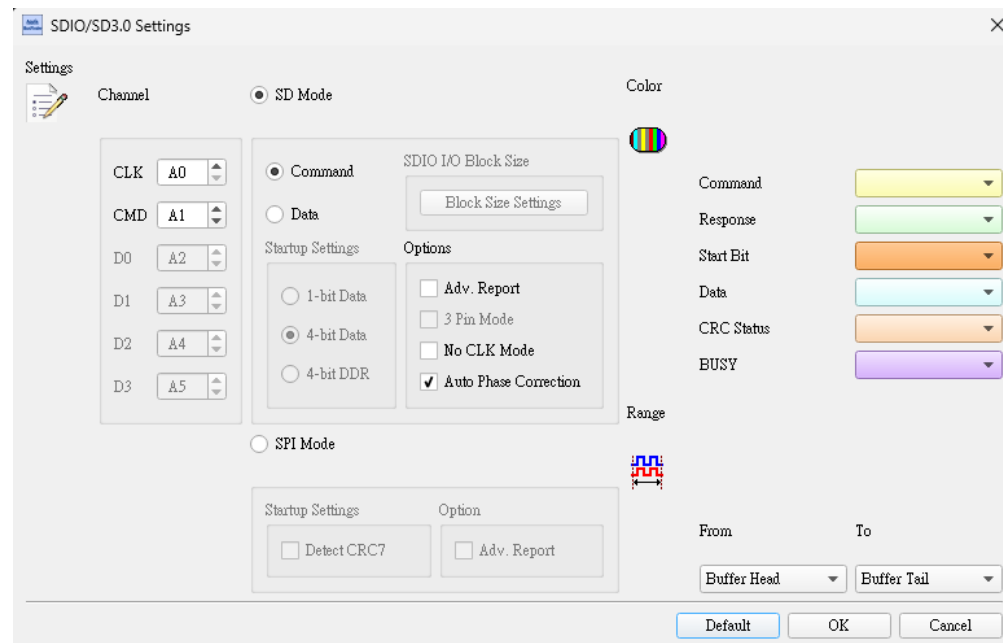
Show wave:



SDIO

The SD3.0/SDIO3.0 Protocol is a high speed serial protocol used primarily for interfacing with SD (Secure Digital) Flash memory cards.

Settings



The SDIO/SD3.0 Settings dialog box is used to configure the SDIO interface. It includes sections for Channel, SD Mode, SPI Mode, Color, and Range. The Channel section shows signal assignments for CLK, CMD, D0, D1, D2, and D3. The SD Mode section includes Command and Data options, SDIO I/O Block Size settings, and Startup Settings. The SPI Mode section includes Startup Settings and Option settings. The Color section shows color assignments for Command, Response, Start Bit, Data, CRC Status, and BUSY. The Range section shows the range of the signal, with From and To fields and Buffer Head and Buffer Tail dropdowns. The dialog box has Default, OK, and Cancel buttons.

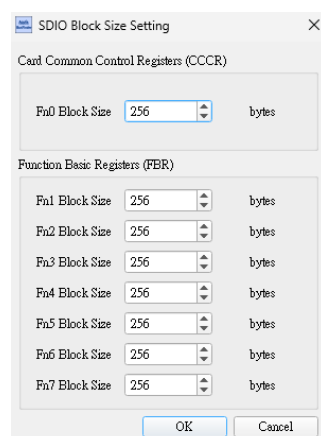
Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

SD Mode, analyzed in SPI mode:

Command: Analyze Command.

Data: Analyze Data.

SDIO I/O Block Size: Set the block size of CCCR and FBR of SDIO.



The SDIO Block Size Setting dialog box is used to set the block size of CCCR and FBR of SDIO. It includes sections for Card Common Control Registers (CCCR) and Function Basic Registers (FBR). The CCCR section shows the Fn0 Block Size set to 256 bytes. The FBR section shows the block size for Fn1 through Fn7, all set to 256 bytes. The dialog box has OK and Cancel buttons.

Options:

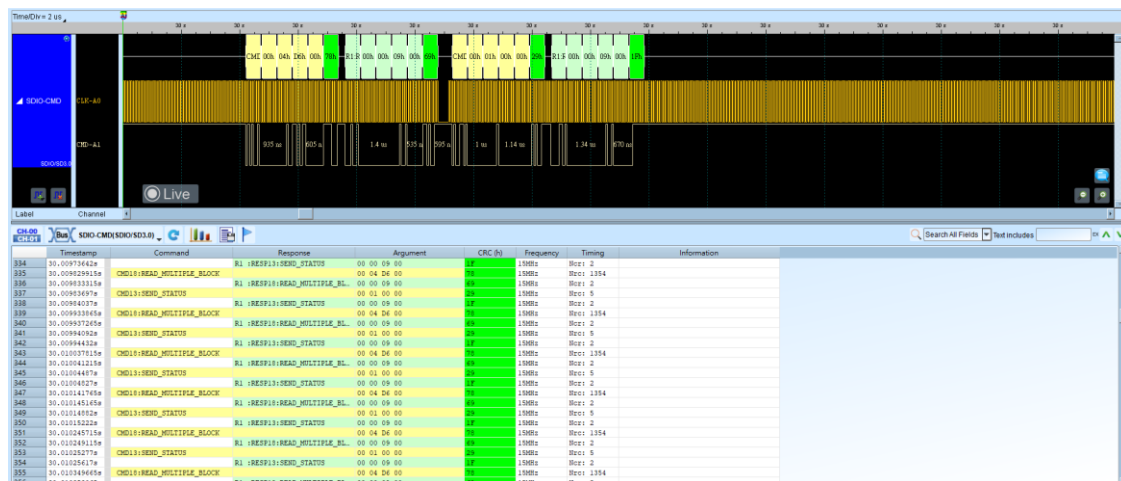
1. **Adv. Report:** Show details. Enabled when checked.
2. **3 Pin Mode:** Analyze the data using CLK, CMD, and D0.
3. **No CLK Mode:** Analyze the data using CMD line only.
4. **Auto Phase Correction:** Automatically adjusts the phase of measurement.

SPI Mode, analyzed in SPI mode:

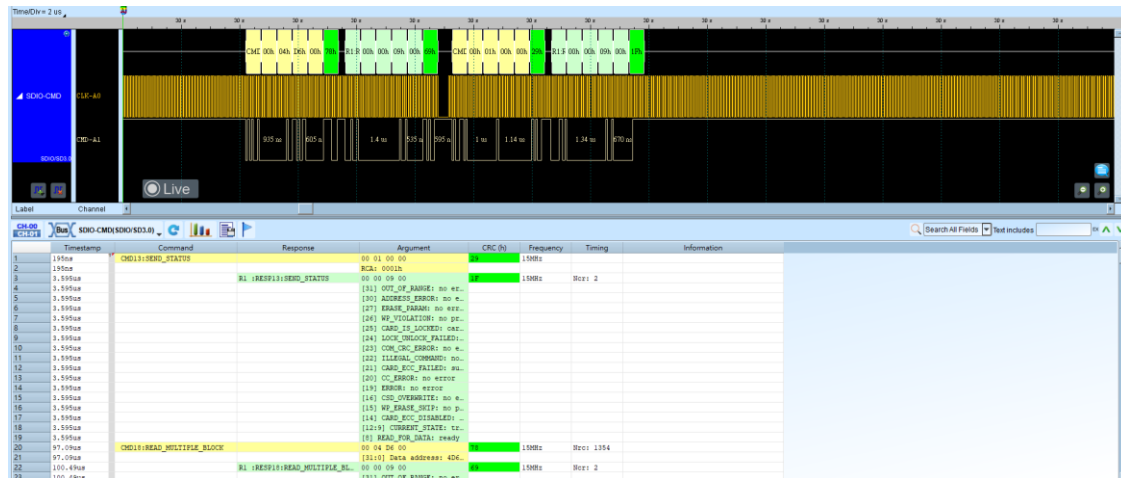
1. **Detect CRC7:** Detect CRC 7 or not. Enabled when checked.
2. **Adv. Report:** Show details. Enabled when checked.

Result

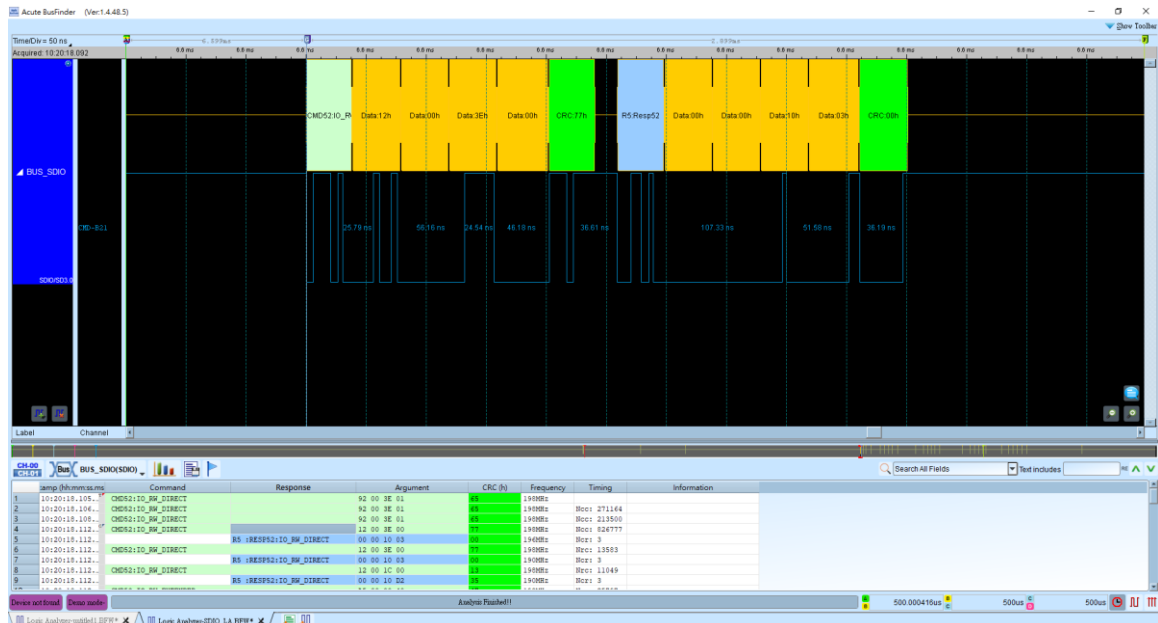
CMD mode



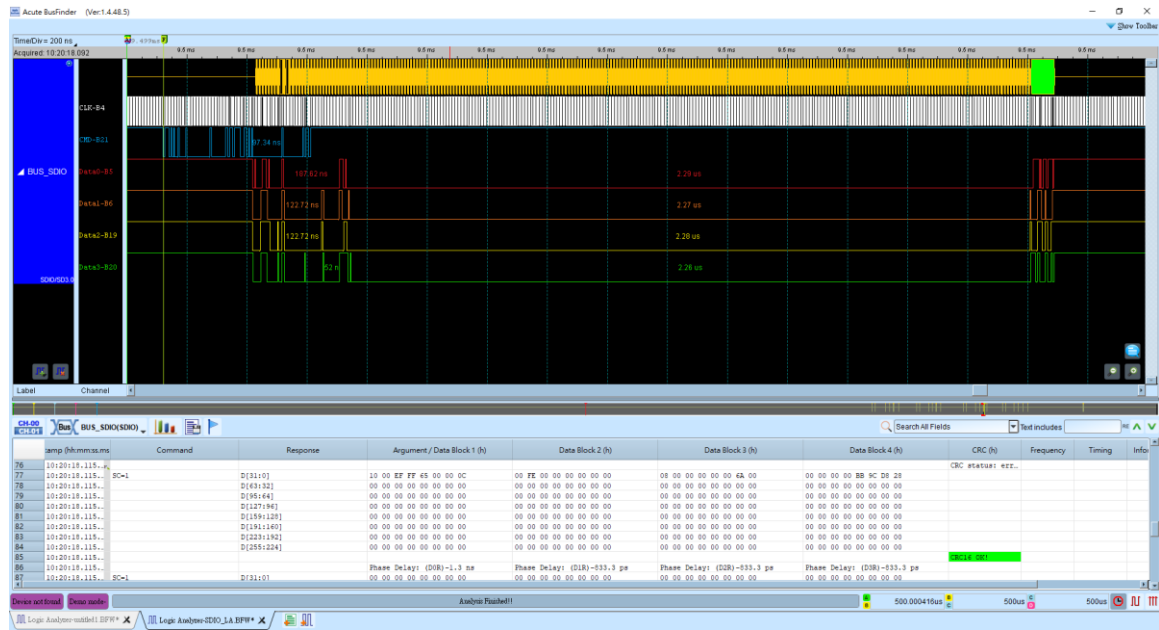
Adv. Report



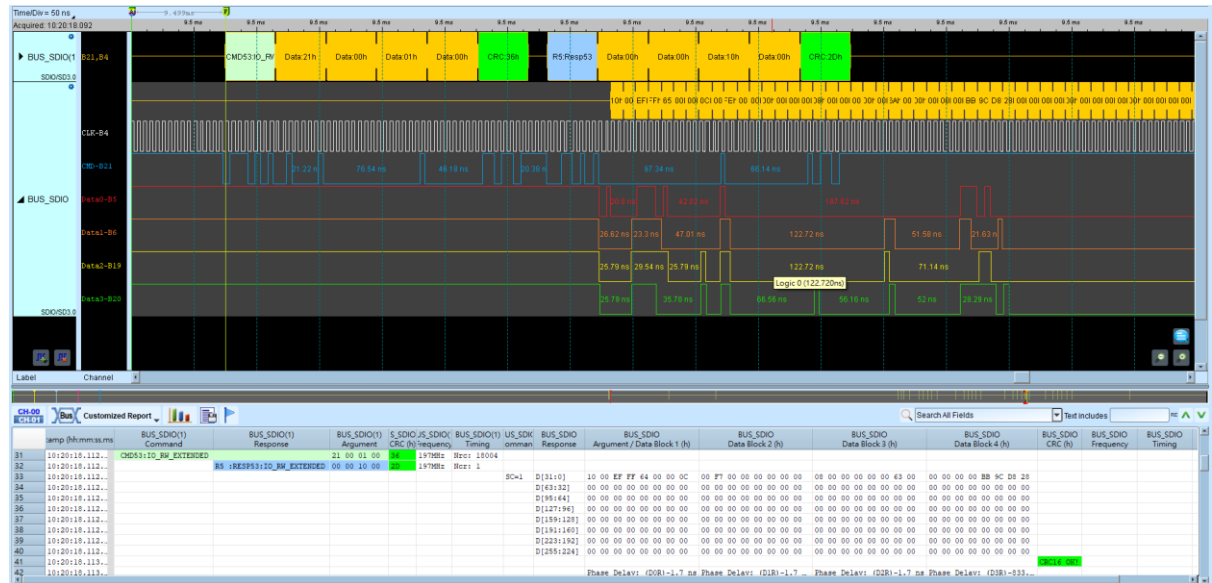
No CLK mode:



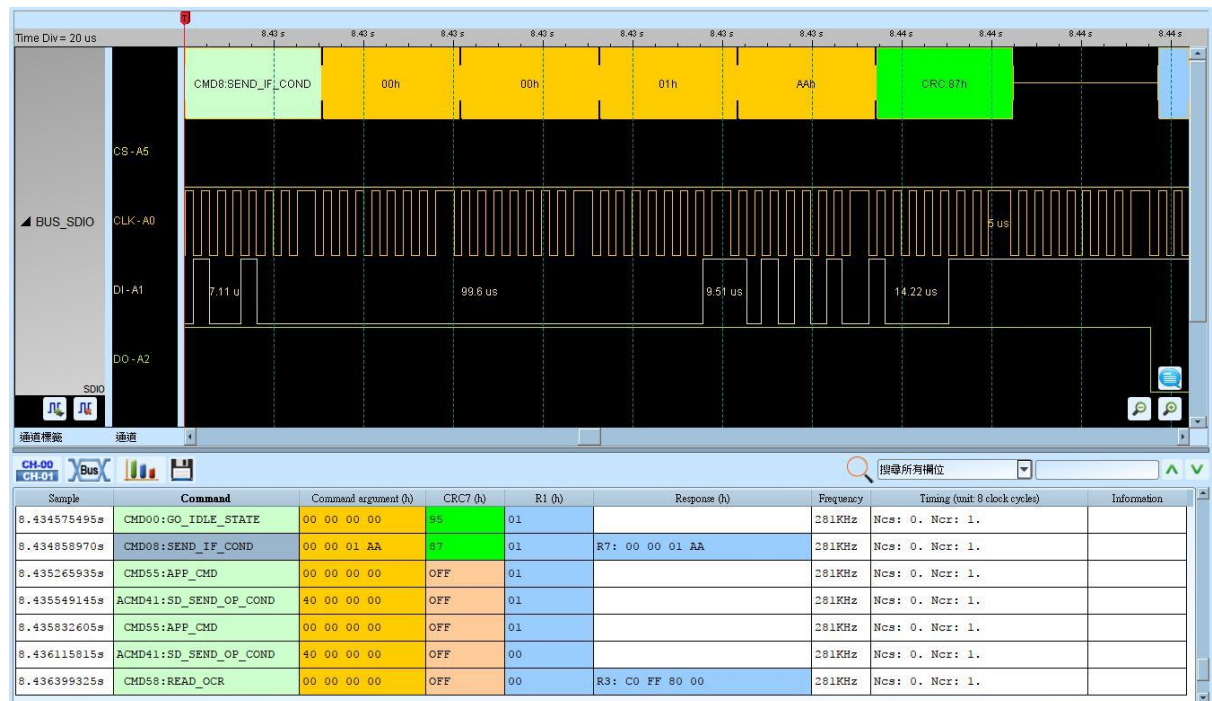
Data:



Command + Data mode:



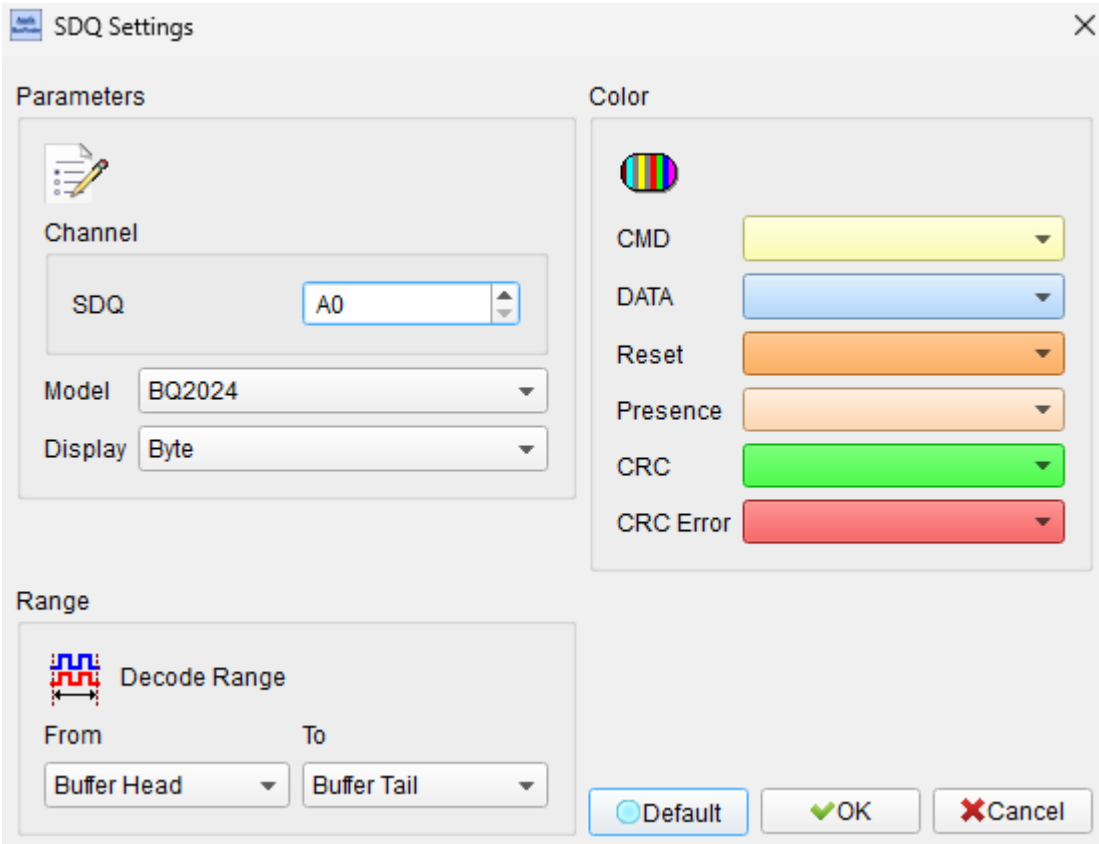
SPI mode:



SDQ

SDQ (Serial Data Quality) interface is an interface standard designed to improve the quality of data transmission, primarily in digital signal processing and communication systems. The SDQ interface is designed to improve data accuracy, reduce miscoding and interference, and ensure signal quality during high-speed data transmission.

Settings



The SDQ Settings dialog box is divided into three main sections: Parameters, Color, and Range.

- Parameters:**
 - Channel:** A dropdown menu showing 'SDQ' and a text box with 'A0'.
 - Model:** A dropdown menu showing 'BQ2024'.
 - Display:** A dropdown menu showing 'Byte'.
- Color:**
 - A color selection icon (a circle with vertical bars of different colors).
 - CMD:** A dropdown menu with a yellow background.
 - DATA:** A dropdown menu with a blue background.
 - Reset:** A dropdown menu with an orange background.
 - Presence:** A dropdown menu with a light orange background.
 - CRC:** A dropdown menu with a green background.
 - CRC Error:** A dropdown menu with a red background.
- Range:**
 - Decode Range:** A section with a waveform icon and a double-headed arrow.
 - From:** A dropdown menu showing 'Buffer Head'.
 - To:** A dropdown menu showing 'Buffer Tail'.

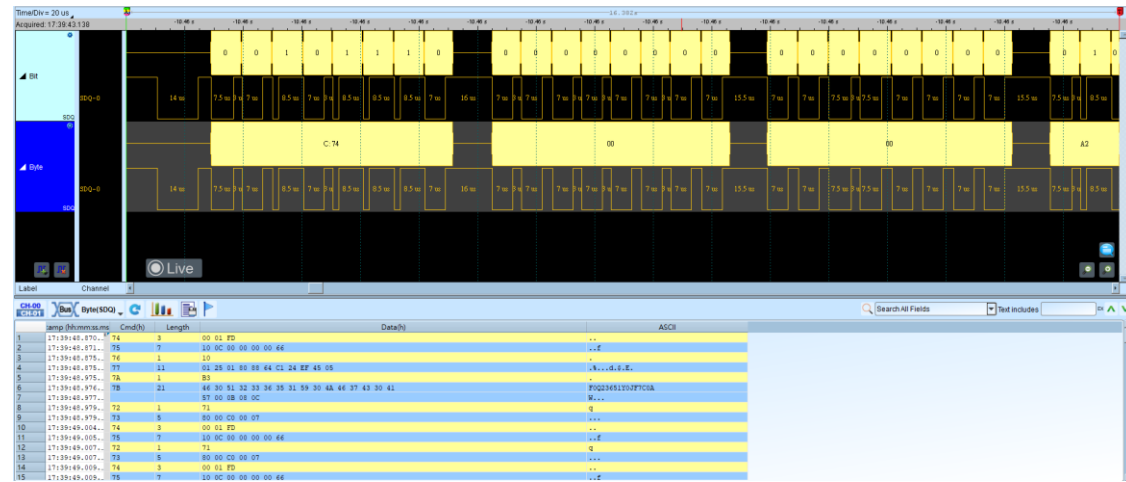
At the bottom right, there are three buttons: 'Default' (with a blue circle icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Model: Set the IC model number. Currently supports BQ2024, BQ2025, BQ2026.

Display: The result of waveform resolution is displayed in Bit or Byte format.

Result



SDR SDRAM

SDRAM (Synchronous Dynamic Random Access Memory) is a synchronous dynamic random access memory. Its characteristic is that it can synchronize the clock pulse of the memory with the host. Because it can only transmit data at the Rising edge, SDRAM can also be called SDR SDRAM (Single Data Rate SDRAM) .

SDRAM is different from the DDR SDRAM structure used in current computers. DDR (Double Data Rate) actually refers to DDR SDRAM (Double Data Rate SDRAM), which means that Rising/Falling edge can transmit data.

Due to the large number of channels required and the high signal speed, this decode is only available on LA3000+, LA4000+ or BusFinder models.

In addition, this decode only supports SDR SDRAM analysis, not DDR SDRAM.

Settings

Channel

#CAS: A3 Address: x12

CKE: A5

CLK: A0

#CS: A1

#RAS: A2

#WE: A4

DQM: x4

DQM0: A6

DQM1: A7

DQM2: A8

DQM3: A9

Bank Address

BA0: A10

BA1: A11

Data

DQ0: A25 DQ8: B1 DQ16: B9 DQ24: B17

DQ1: A26 DQ9: B2 DQ17: B10 DQ25: B18

DQ2: A27 DQ10: B3 DQ18: B11 DQ26: B19

DQ3: A28 DQ11: B4 DQ19: B12 DQ27: B20

DQ4: A29 DQ12: B5 DQ20: B13 DQ28: B21

DQ5: A30 DQ13: B6 DQ21: B14 DQ29: B22

DQ6: A31 DQ14: B7 DQ22: B15 DQ30: B23

DQ7: B0 DQ15: B8 DQ23: B16 DQ31: B24

☒ Parsing include Address and Data

Start Up

#CAS Latency

☒ Non

☐ 3 clocks

☐ 2 clocks

Decode display in waveform area

☒ Command

☐ Address

☐ Data

☐ BankAddress

☐ A10

Color

DESL: [Orange]

NOP: [Orange]

BST: [Yellow]

READ / A: [Light Green]

WRITE / A: [Light Blue]

ACT: [Blue]

PRE: [Purple]

CBR_AREF: [White]

MRS: [Pink]

PALL: [Yellow]

SELF: [Yellow]

Address: [Green]

Data: [Cyan]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Set the channel number of logic analyzer

Parsing include Address and Data:

When this item is not checked:

Only for simple analysis of SDRAM Command, just connect #CAS, CKE, #CS,

#RAS, the 6 channels of #WE, A10 can be analyzed. In this way, the number of

wiring can be reduced, but because it cannot knowing the status of Address, Data, etc., is only suitable for primary analysis. Please see Figure 1 below for the analysis results.

When checked:

Including all SDRAM pins for a complete analysis, the analysis results are shown in Figure 2 below

Startup:

#CAS Latency:

Set the delay time for SDRAM read operation

Decode display in waveform area

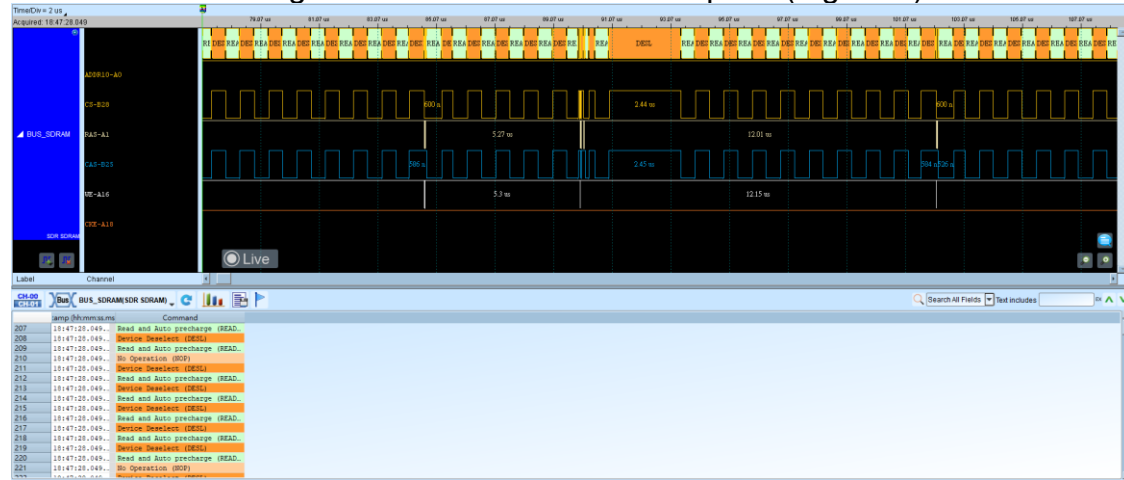
Because there are many states to be displayed by SDRAM, they cannot be displayed all at once in the waveform area.

Therefore, it is necessary to select the item to be viewed in the waveform area.

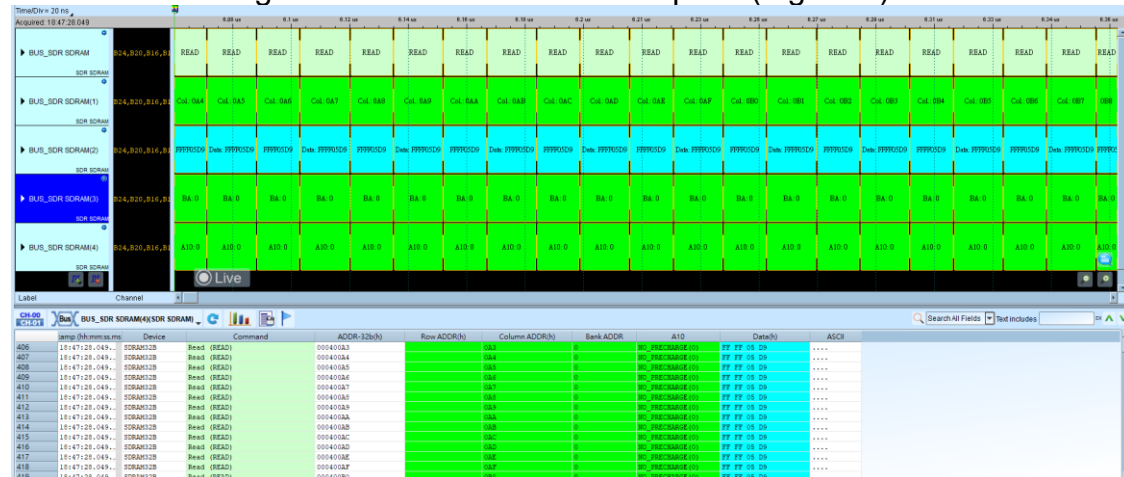
If there are many items to be viewed at the same time, you can add multiple groups of the same SDRAM decoding, then set different decoding and display modes of the waveform area respectively. As shown in Figure 2 below, the left side multiple groups of channels have been added to distinguish the display.

Result

Uncheck the Parsing include Address and Data option (Figure 1)



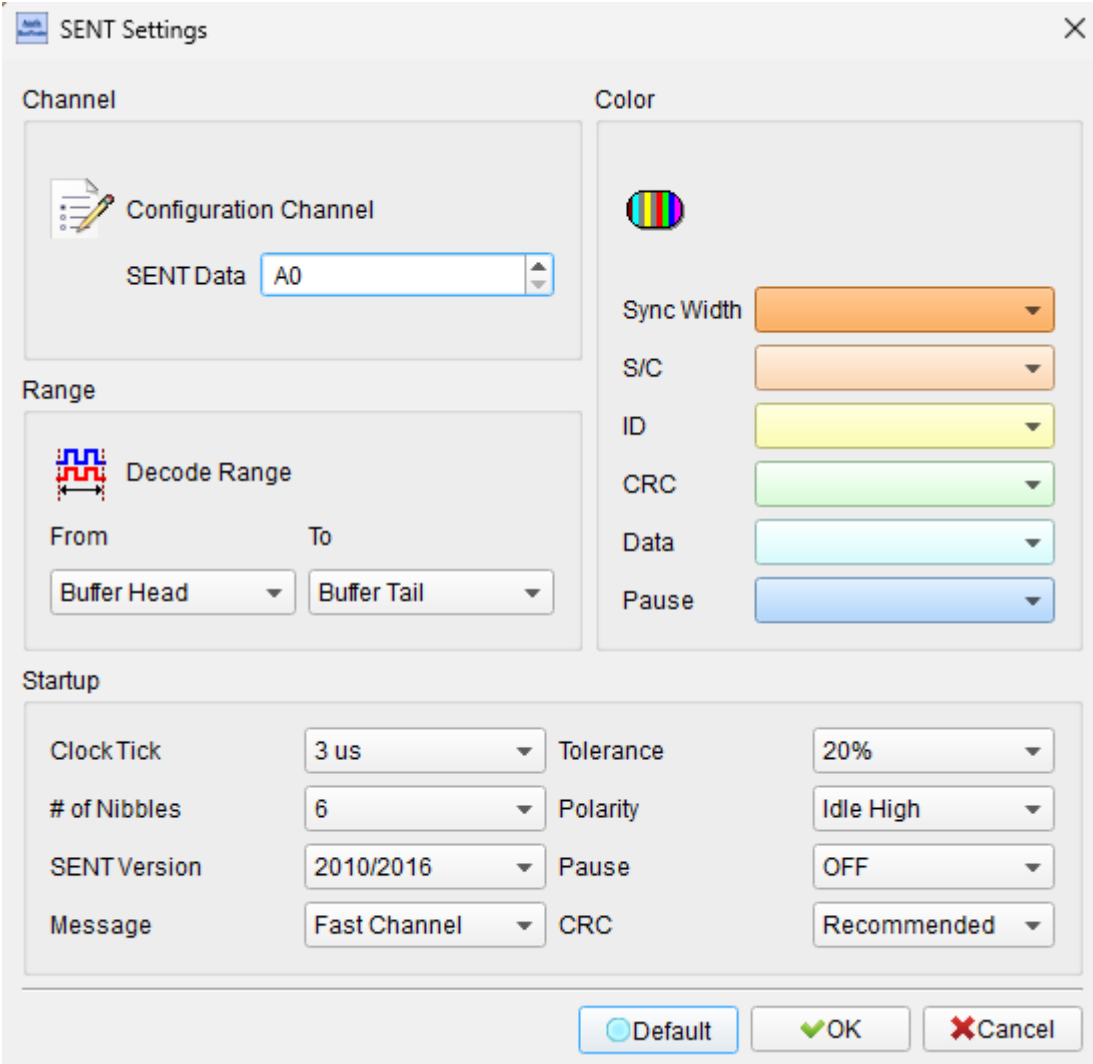
Check the Parsing include Address and Data option (Figure 2)



SENT

The SENT (Single Edge Nibble Transmission) protocol is a communication protocol used in the field of automotive electronics, especially for data transmission between sensors and control units (ECUs) in the vehicle's internal electronic system. The SENT protocol is widely used in high-performance in-vehicle sensors such as wheel speedometers, position sensors, etc. It enables efficient data transfer with limited bandwidth and guarantees high-precision data transfer.

Settings

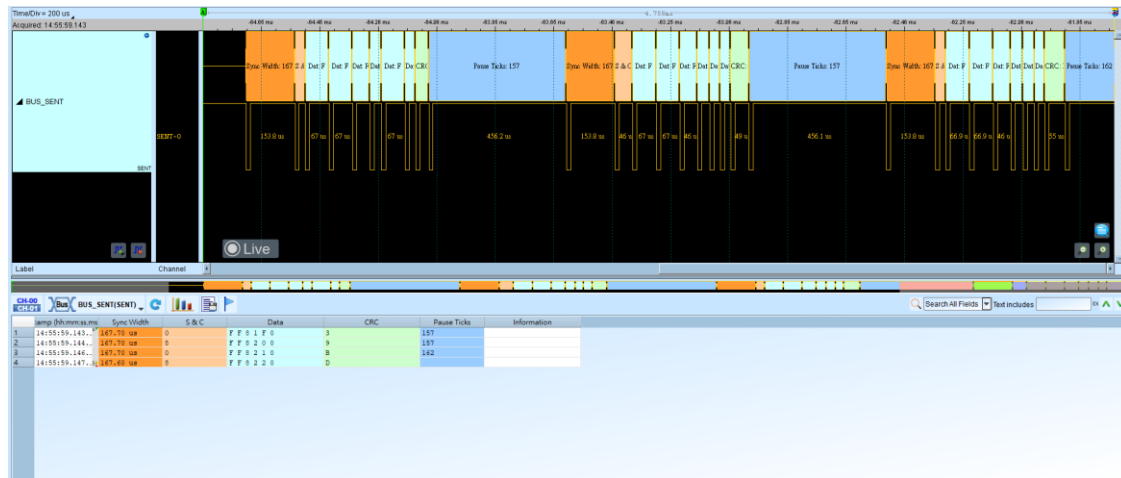


The image shows the 'SENT Settings' dialog box. It is divided into three main sections: Channel, Range, and Startup. The Channel section includes a 'Configuration Channel' icon and a 'SENT Data' dropdown menu set to 'A0'. The Range section includes a 'Decode Range' icon and two dropdown menus for 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail'). The Startup section includes several settings: 'Clock Tick' (3 us), '# of Nibbles' (6), 'SENT Version' (2010/2016), 'Message' (Fast Channel), 'Tolerance' (20%), 'Polarity' (Idle High), 'Pause' (OFF), and 'CRC' (Recommended). There is also a 'Color' section with a color bar icon and dropdown menus for 'Sync Width', 'S/C', 'ID', 'CRC', 'Data', and 'Pause'. At the bottom, there are buttons for 'Default', 'OK', and 'Cancel'.

Channel: Set the channel number of the Logic Analyzer to which each signal end is connected on the object to be tested.

Startup: Sets the startup setting for SENT before analysis.

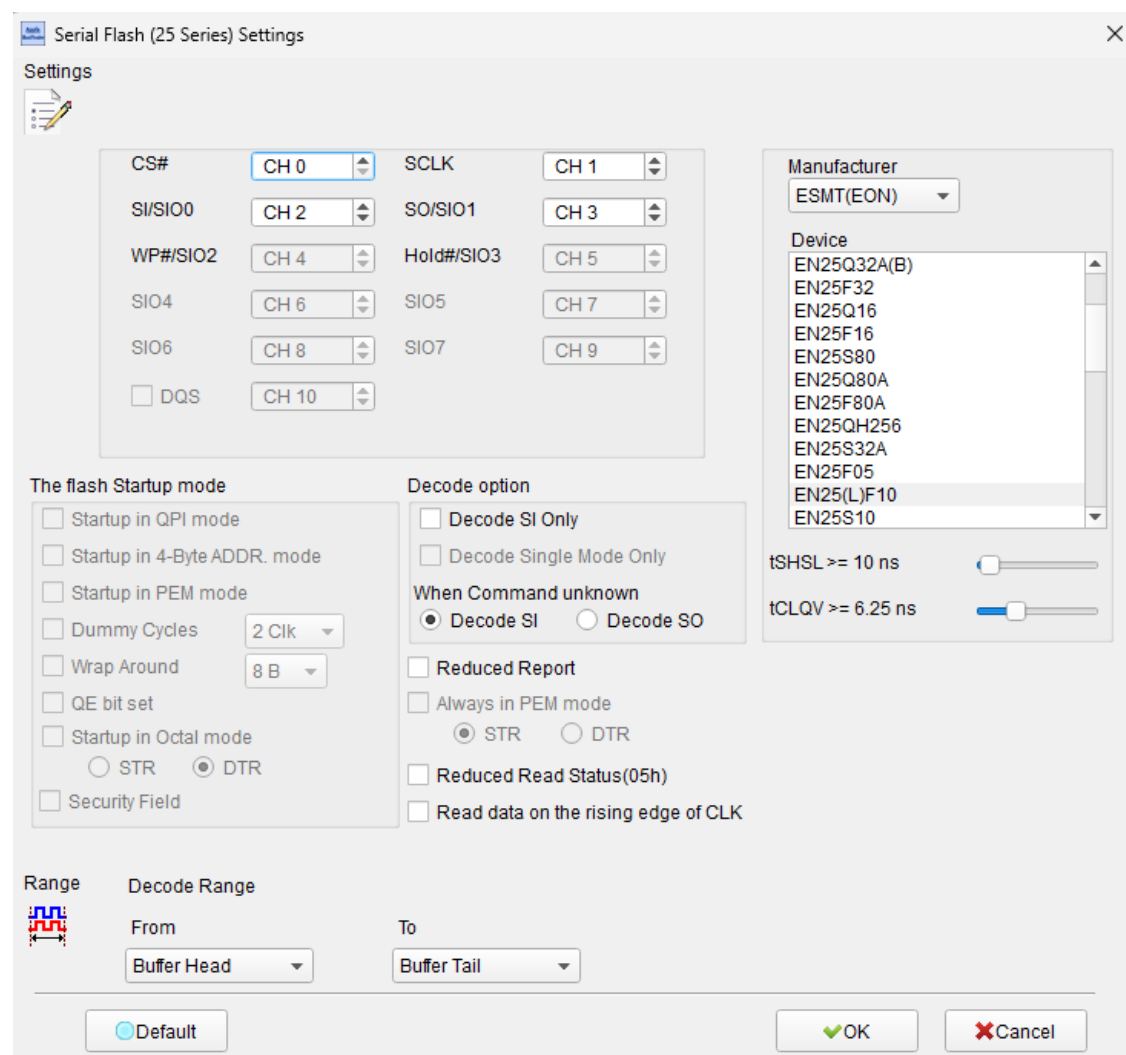
Result



Serial Flash

Serial flash (SPI Flash) 25, 35, etc. series use SPI/QPI/OPI protocol as their data transfer communication method. Serial flash bus analysis provides users with the ability to view commands and input/output bus messages at the same time when viewing signals, saving users the time of analyzing waveforms using the SPI bus.

Settings



The image shows the 'Serial Flash (25 Series) Settings' dialog box. It contains several sections for configuring the serial flash analysis. The 'Settings' section at the top left has dropdown menus for CS# (CH 0), SCLK (CH 1), SI/SIO0 (CH 2), SO/SIO1 (CH 3), WP#/SIO2 (CH 4), Hold#/SIO3 (CH 5), SIO4 (CH 6), SIO5 (CH 7), SIO6 (CH 8), SIO7 (CH 9), and a checkbox for DQS (CH 10). The 'Manufacturer' dropdown is set to 'ESMT(EON)'. The 'Device' list includes EN25Q32A(B), EN25F32, EN25Q16, EN25F16, EN25S80, EN25Q80A, EN25F80A, EN25QH256, EN25S32A, EN25F05, EN25(L)F10, and EN25S10. The 'The flash Startup mode' section has checkboxes for Startup in QPI mode, Startup in 4-Byte ADDR. mode, Startup in PEM mode, Dummy Cycles (2 Clk), Wrap Around (8 B), QE bit set, Startup in Octal mode (STR or DTR), and Security Field. The 'Decode option' section has checkboxes for Decode SI Only, Decode Single Mode Only, When Command unknown (Decode SI or Decode SO), Reduced Report, Always in PEM mode (STR or DTR), Reduced Read Status(05h), and Read data on the rising edge of CLK. The 'Range' section has a 'Decode Range' with 'From' (Buffer Head) and 'To' (Buffer Tail) dropdowns. At the bottom are 'Default', 'OK', and 'Cancel' buttons.

CS#: Chip Select of transfer signal.

SCLK: Clock of transfer signal.

SIO0-SIO7: Data pin of transfer signal.

Manufacturer: The main purpose of this function is to select the correct Flash model, tCLQV and tSHSL for command parsing. If no exact model is found, the user can also select a model that is compatible with the command format.

The Flash Startup Mode: Since the Serial Flash can switch the operation mode with commands, the Logic Analyzer does not know the current operation mode of the actual Serial Flash when it captures the waveforms. Therefore, the user should be informed if necessary. When the user selects a Flash model that does not support mode switching, the relevant option will be disabled and cannot be set.

QPI Mode: Refers to Quad Peripheral Interface Mode or Quad SPI Mode.

4-Byte Mode: Refers to the 4-Byte Address Mode.

PEM Mode: Refers to the Performance Enhancement Mode.

Dummy Cycles: Some Read instructions wait for Dummy cycles, and the number of cycles they wait for can be preset.

Wrap Around: The value of Wrap around can be preset.

QE bit: QE bit in the status register, which can be used for QPI mode enable/disable control.

Startup in Octal Mode: Refers to the OPI mode.

Security Field: We provide Flash with AES encryption and decryption function, please contact us if user need to use it.

Decode SI Only: When checked, the program will use Single mode to analyze the waveforms in 3-line mode. These 3 lines are CS# / SCLK / SI.

Decode Single Mode Only: When this option is selected, the program will use Single mode to analyze the waveform in 4-line mode. These 4 lines are CS / Clock / SI / SO. In this case, the program will ignore the command to switch to

multi-line mode. If unchecked, the program will analyze the waveform in 4-wire or 6-wire mode according to the selected Flash model.

When Command Unknown: Decoded for SO or SI only.

Always in PEM Mode: When checked, the analyzer will maintain the PEM mode regardless of the command setting, and you can choose to maintain in STR or DTR mode.

Reduce Read Status(05h): When checked, the Read Status (05h) command that repeats the unchanged data will be combined into a single command when generating an analysis report, and the number of repetitions will be displayed, thus reducing the number of reports and making it easier to view.

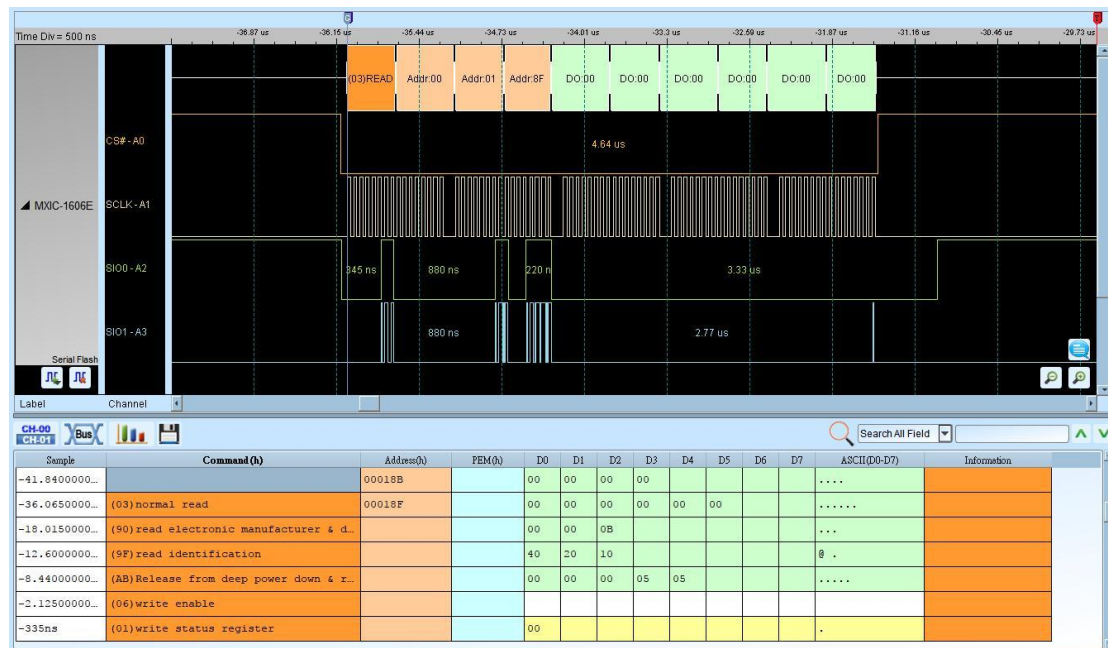
As you can see from the example below, the Read status data = 01 is repeated 1817 times.

(01)Write Status Register	00	02	..	x1
(05)Read Status Register-1	01			Repeat: CMD 1817 Times, DAT 1817 B
(05)Read Status Register-1	00			x1
(35)Read Status Register-2	02			x1
(06)Write Enable				x1

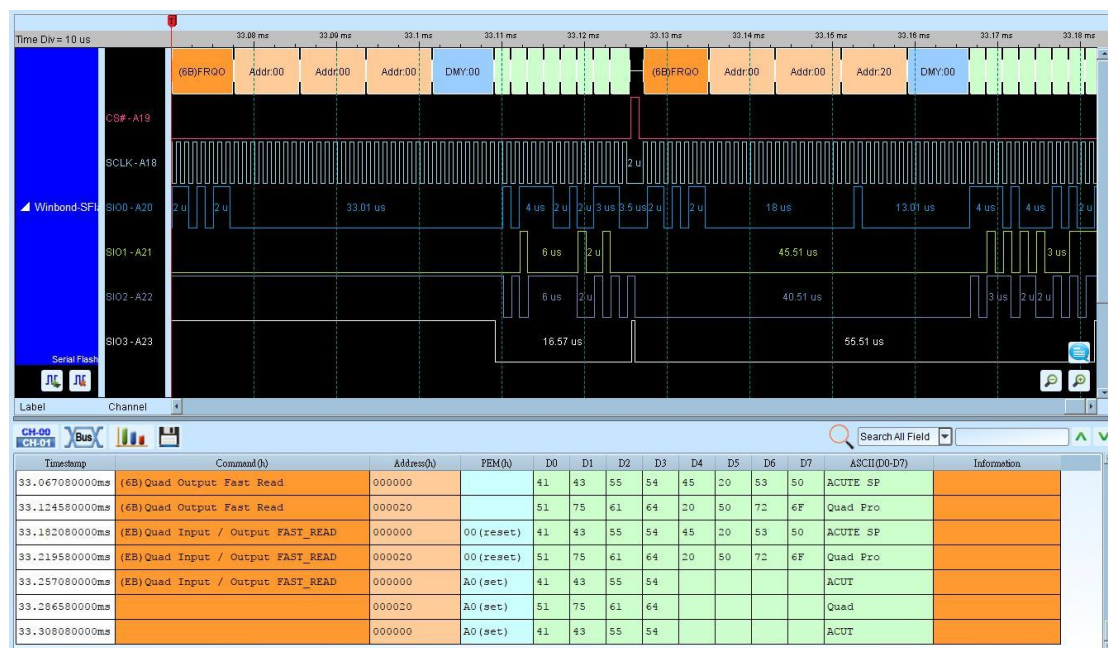
Read data on the rising edge of CLK: For SDR Read Data mode, if the Clock signal Duty is not stable enough and the Latch Data out cannot be correct after setting tCLQV value, the Latch bit can be set to Next rising edge.

Result

Using SPI Mode Serial Flash Decoding Situation

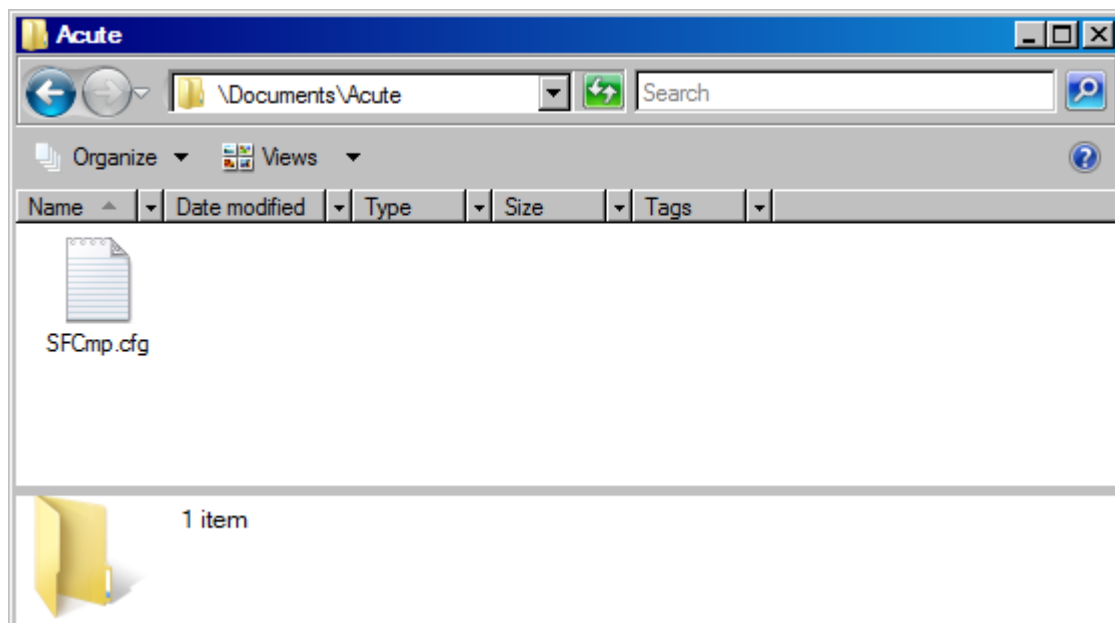


Using QPI Mode Serial Flash Decoding Scenario

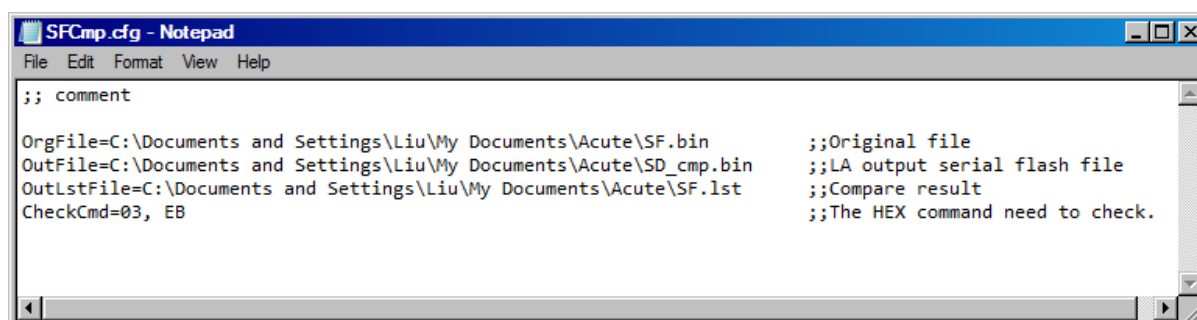


Serial Flash data Comparison : Compare the Serial Flash data by the waveform files.

Method: Create a file by text editor and save it as SFCmp.cfg in order to compare with the real Serial Flash waveform to find the bug, the default path is "My Documents\Acute"



SFCmp.cfg information:



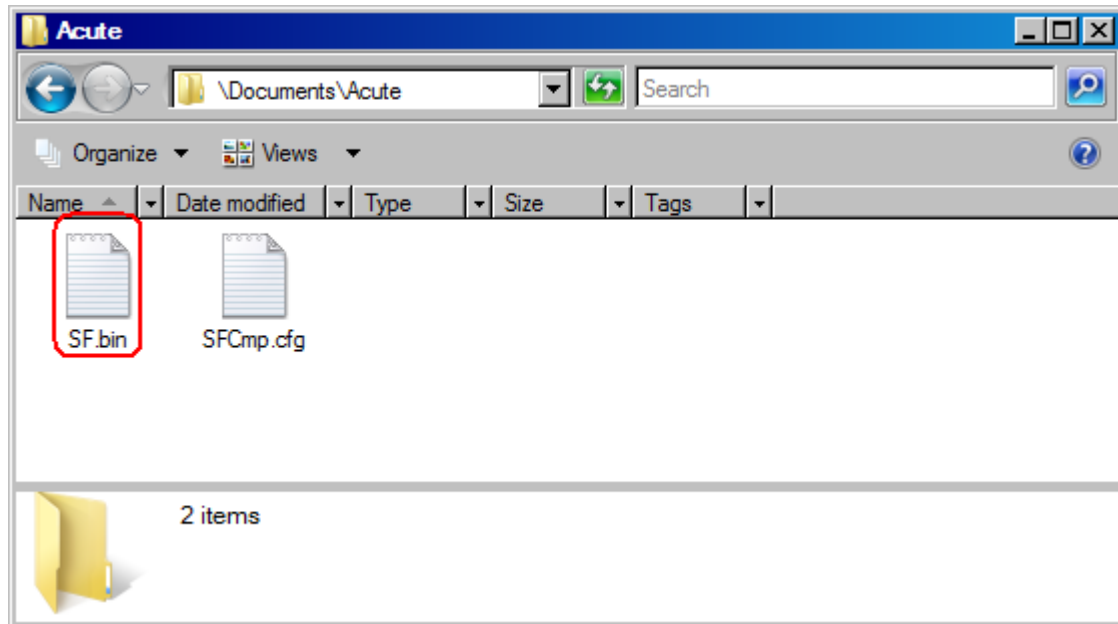
OrgFile=File_Path: Key in the file path of the original Serial Flash data file (.bin).

OutFile=File_Path: Key in the file path of the Serial Flash output file.

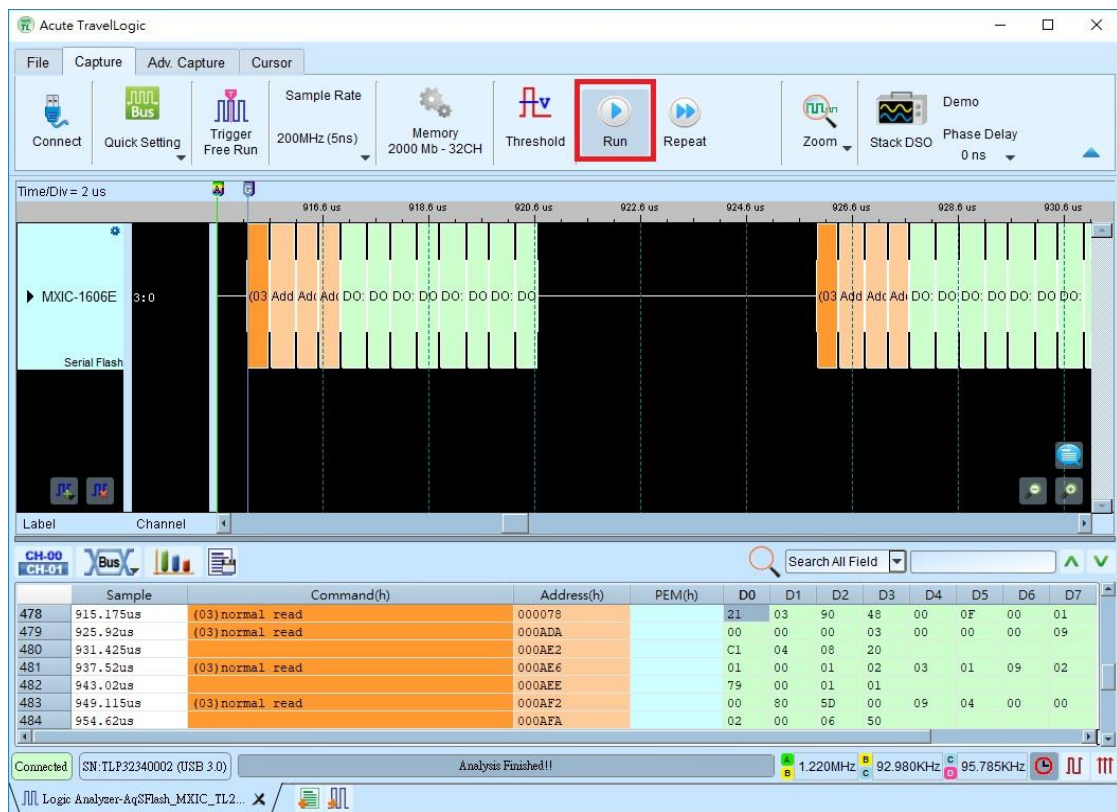
OutLstFile=File_Path: Key in the file path of the comparison result. The file name will has extension “.lst”.

CheckCmd=Serial Flash command: Key in the command in Hex that are separated by commas.

Save the OrgFile to the OrgFile file path.

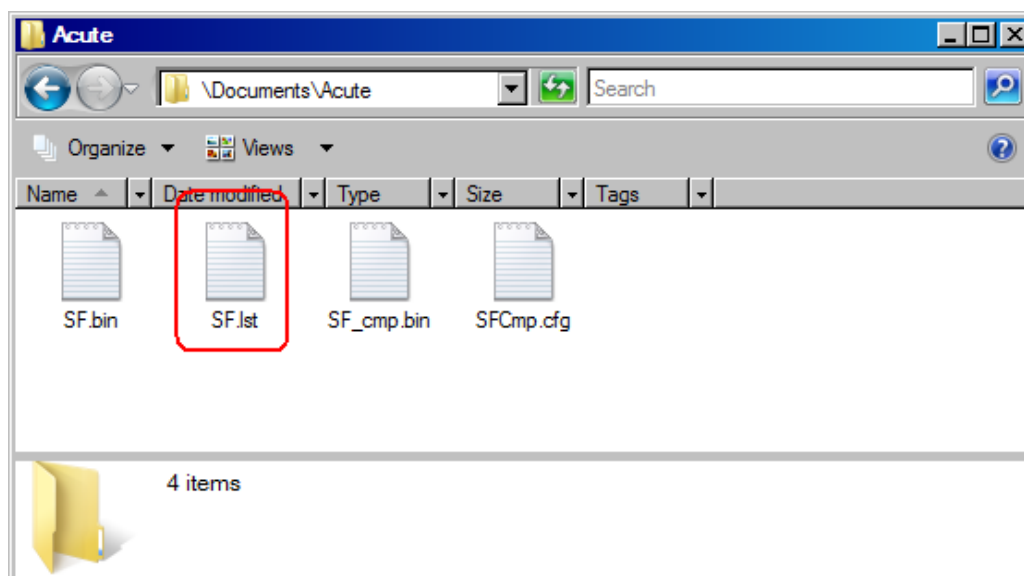


Run the Serial Flash Bus Decode to capture the Serial Flash signal.

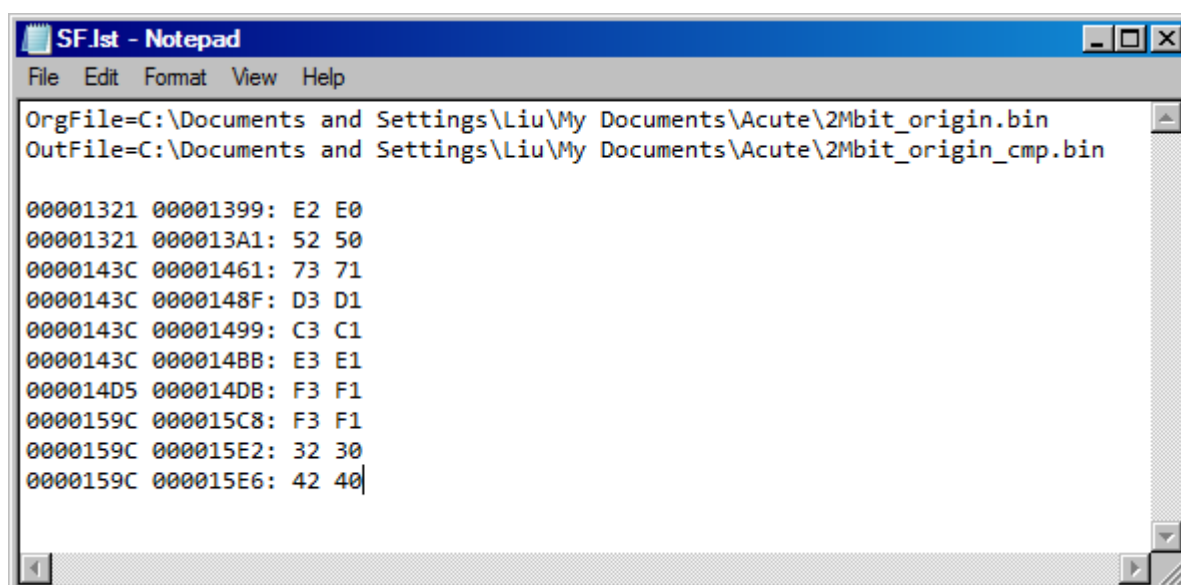


If the OutFile does not exist, it will copy the OrgFile to the OutFile and write the data to it according to the CheckCmd.

Compare result:



The OutLstFile:

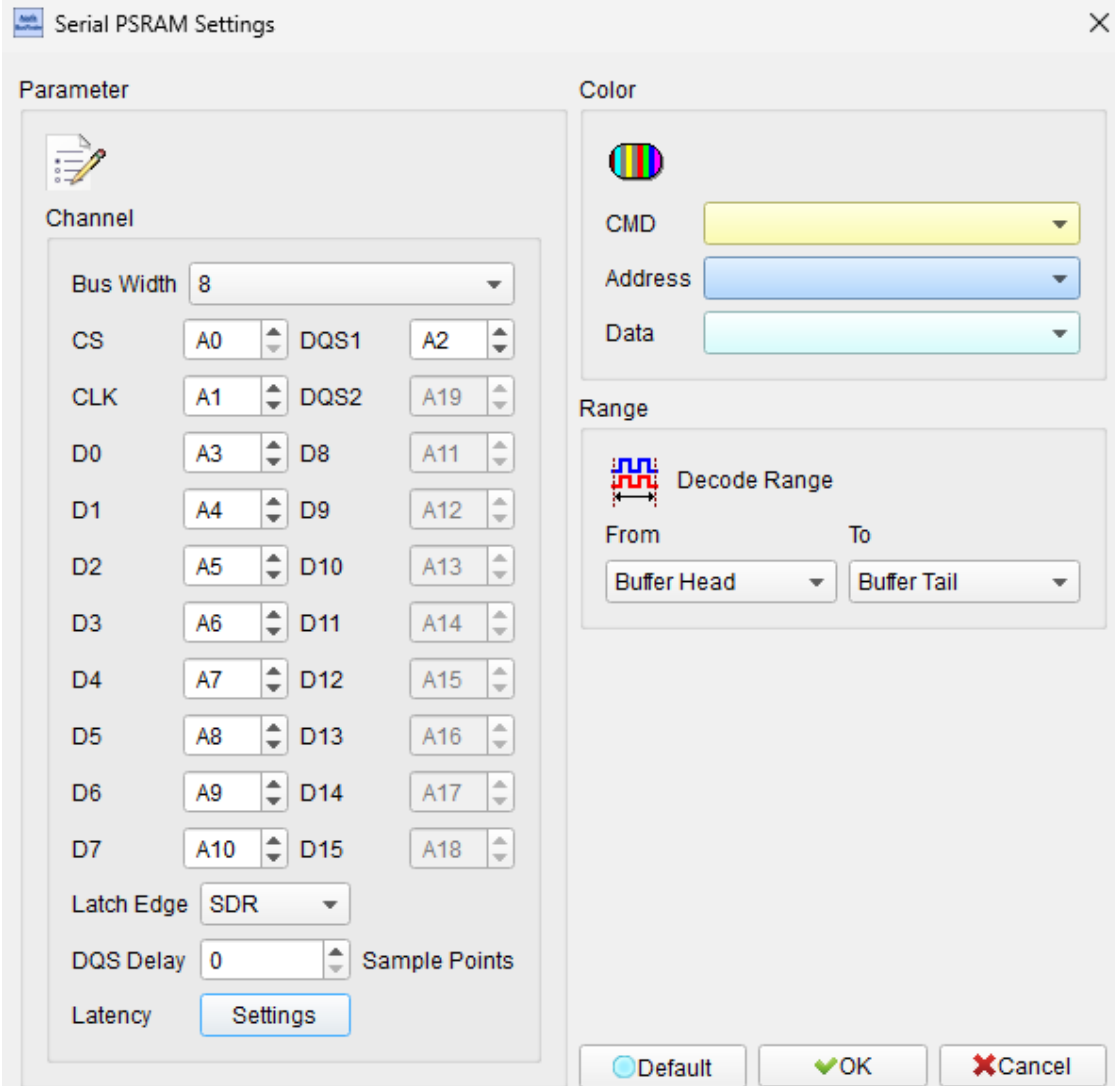


The first column is the compared address from OrgFile, the second column is the different address from OutFile.

Serial PSRAM

Serial PSRAM is a special form of PSRAM (Pseudostatic RAM) that uses a serial interface to communicate with a microprocessor or other system. PSRAM is a type of memory that is intermediate between Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). It has the advantages of high density of DRAM, but similar to SRAM, it offers relatively simple operation and simplifies memory control to some extent.

Settings



The dialog box is titled "Serial PSRAM Settings" and contains two main sections: "Parameter" and "Color".

Parameter Section:

- Channel:** Includes a "Bus Width" dropdown set to 8.
- CS:** A0 (up/down arrows) and DQS1 (A2, up/down arrows).
- CLK:** A1 (up/down arrows) and DQS2 (A19, up/down arrows).
- D0:** A3 (up/down arrows) and D8 (A11, up/down arrows).
- D1:** A4 (up/down arrows) and D9 (A12, up/down arrows).
- D2:** A5 (up/down arrows) and D10 (A13, up/down arrows).
- D3:** A6 (up/down arrows) and D11 (A14, up/down arrows).
- D4:** A7 (up/down arrows) and D12 (A15, up/down arrows).
- D5:** A8 (up/down arrows) and D13 (A16, up/down arrows).
- D6:** A9 (up/down arrows) and D14 (A17, up/down arrows).
- D7:** A10 (up/down arrows) and D15 (A18, up/down arrows).
- Latch Edge:** SDR (dropdown).
- DQS Delay:** 0 (up/down arrows) and Sample Points.
- Latency:** Settings (button).

Color Section:

- CMD:** Yellow (dropdown).
- Address:** Blue (dropdown).
- Data:** Cyan (dropdown).

Range Section:

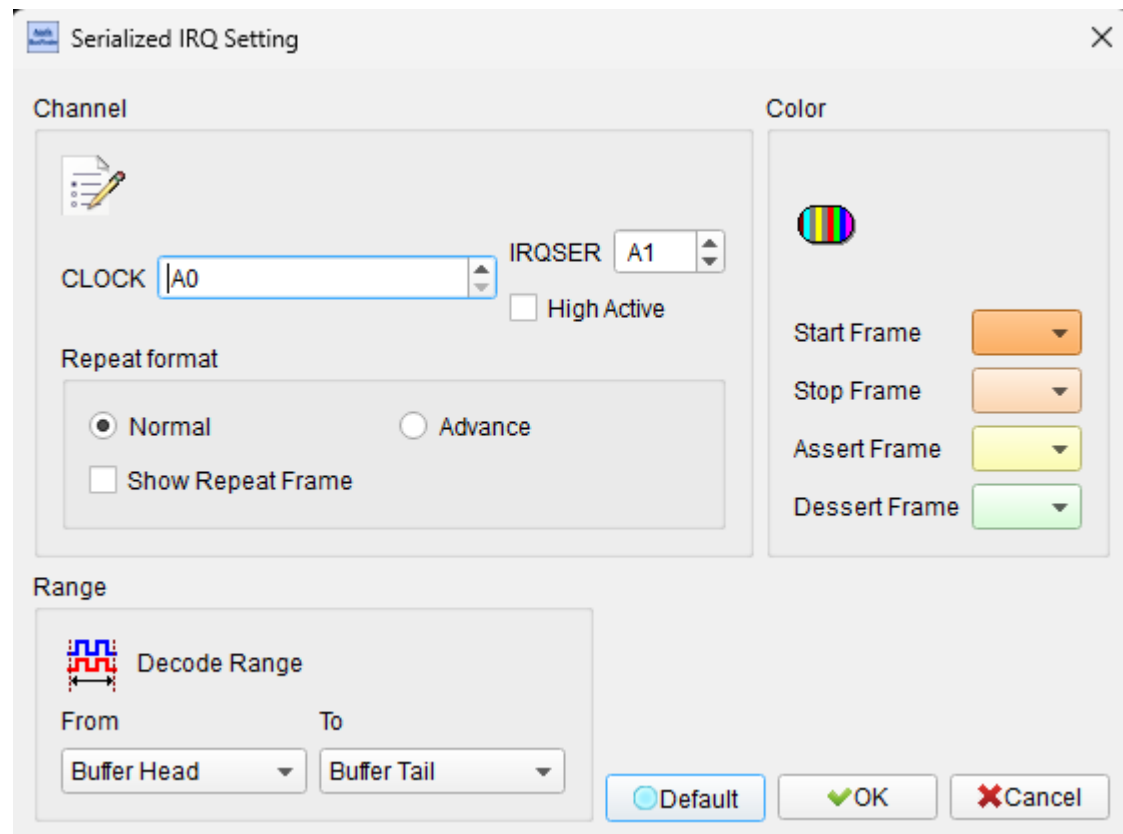
- Decode Range:** Includes a diagram of a memory buffer with a range indicated by a red arrow.
- From:** Buffer Head (dropdown).
- To:** Buffer Tail (dropdown).

Buttons: Default (radio button), OK (green checkmark), and Cancel (red X).

Serial IRQ

Serial IRQ/Data is a communication protocol composed of two lines, PCI-Clock and IRQSER, used to transmit interrupt status. An IRQSER cycle essentially consists of three parts: Start, IRQ/Data, and Stop Frame. The operating modes are divided into Continuous mode and Quiet mode. In Continuous mode, the source of the Start Frame is not restricted, but in Quiet mode, only the Host can generate the Start Frame signal.

Settings



CLOCK: PCI Clock channel

IRQSER; IRQSER channel

Normal: Not show repeat frame

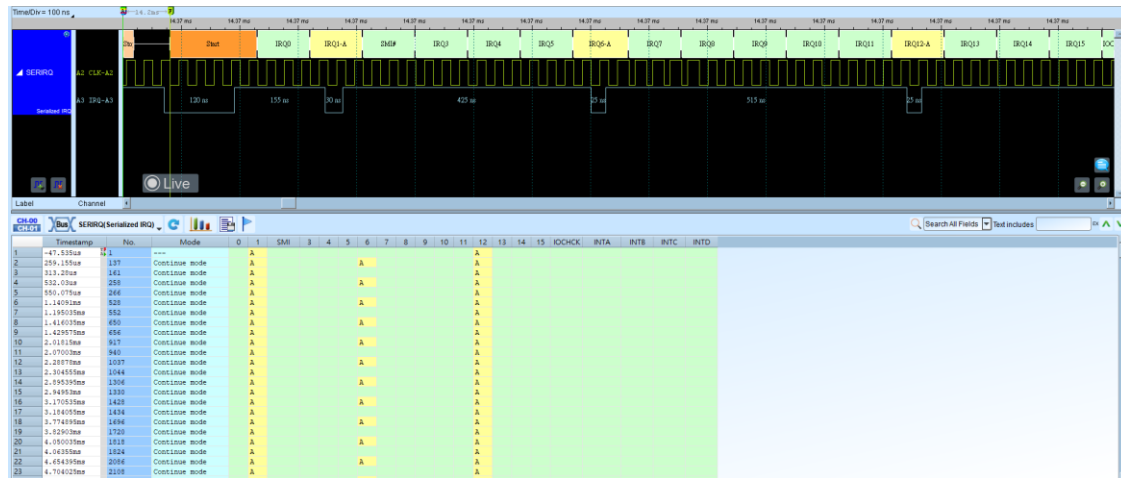
High Active: Enables the user to adjust the numeric judgment conditions.

Advance: Spread all IRQ/Data in a frame on different lines.

CH-00 CH-01 Bus SERIRQ(Serialized IRQ)				
	Timestamp	IRQ/Data Frame	Signal Sampled	# of clocks past Start
1	-47.38us	1	IRQ0	2
2	-47.29us	2	IRQ1	5
3	-47.2us	3	SMI#	8
4	-47.11us	4	IRQ3	11
5	-47.02us	5	IRQ4	14
6	-46.93us	6	IRQ5	17
7	-46.84us	7	IRQ6	20
8	-46.75us	8	IRQ7	23
9	-46.66us	9	IRQ8	26
10	-46.57us	10	IRQ9	29
11	-46.48us	11	IRQ10	32
12	-46.39us	12	IRQ11	35
13	-46.3us	13	IRQ12	38
14	-46.21us	14	IRQ13	41
15	-46.12us	15	IRQ14	44

Result

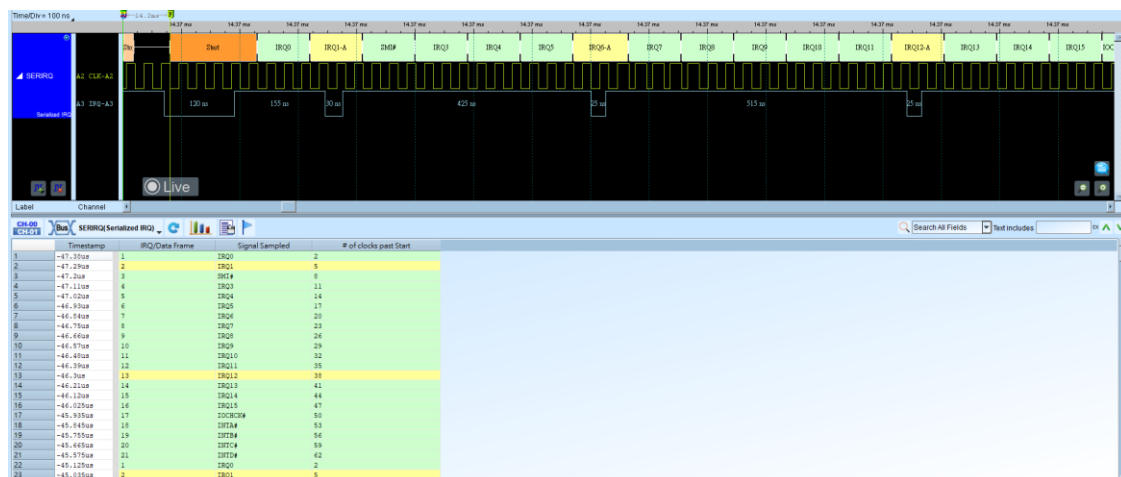
Normal mode (Hide Repeat Frame)



Normal mode(Show repeat frame)



Advance mode



SGPIO

SGPIO (Serial General Purpose Input Output Serial) is a general-purpose input/output that can be controlled by the user.

Settings

SGPIO Settings

Channel

Startup Settings

Mode: 3-bit Driver

Byte per column: 16-bits

Packets Starts From: Low

Load Latch On: Rising

SGPMO Latch On: Falling

SGPMI Latch On: Rising

Display: DataOut

Significant Bit: LSB

Channel

Clock: A0

Load: A1

☒ DO: A2

☒ DI: A3

Color

Load / Start: [Green]

DO: [Orange]

DI: [Cyan]

Range

Decode Range

From: Buffer Head To: Buffer Tail

Default OK Cancel

Channel: Set the channel number of each signal on the object to be tested that is connected to the Logic Analyzer. These are Clock, Load, Data Out, and Data In. User can choose to have only Data Out, Data In, or both.

Startup Settings:

Mode:

1. **3-Bit Driver:**
2. **User Defined Data**, the following settings are valid only when the mode is switched to this item:

Byte per Column: Sets the Data-Size.

Packets Starts From: Set the Packet to start from Low or High.

Load Latch On: Latch data on rising or falling edge of Load Pin.

SGPMO Latch On: Latch data on rising or falling edge of SGPMO Pin.

SGPMI Latch On: Latch data on rising or falling edge of SGPMI Pin.

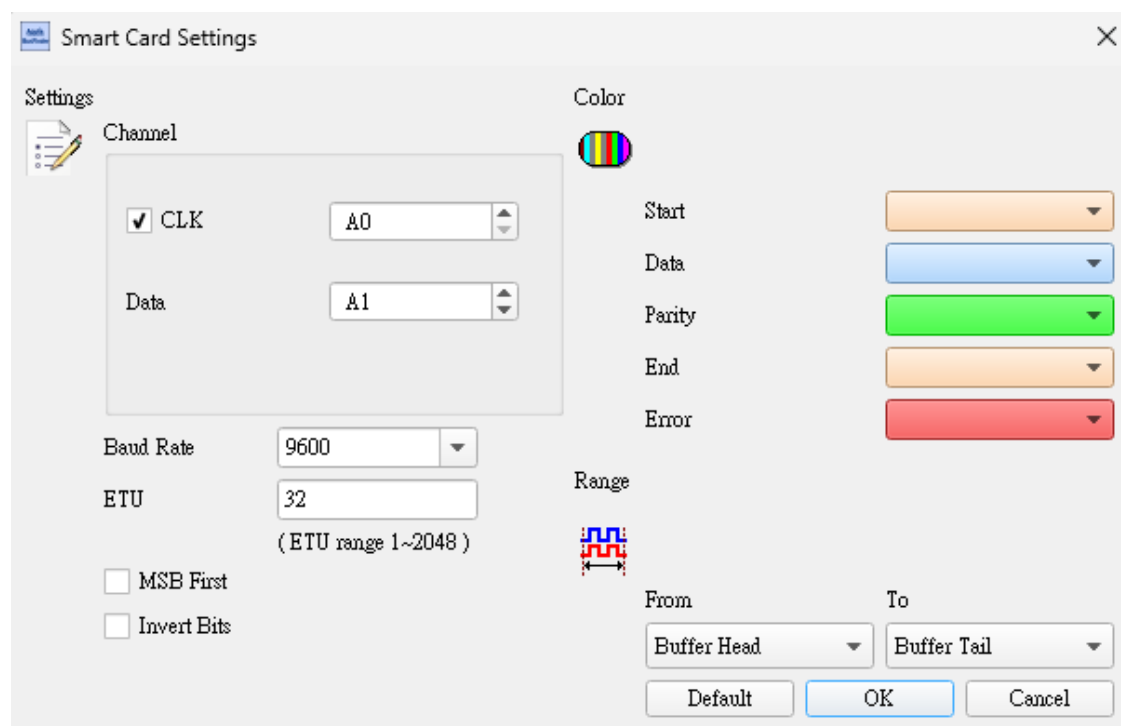
Result:



Smart Card (ISO7816)

Smart Card is a communication protocol based on ISO 7816 specification, generally used in IC card or IC chip card, different IC chips have different functions and applications. It is mainly used for identification, recording and encoding/decoding.

Settings



The image shows a 'Smart Card Settings' dialog box. It is divided into several sections: 'Settings' (containing 'Channel' and 'Baud Rate' settings), 'Color' (containing a color selection icon and a list of color-coded fields: Start, Data, Parity, End, Error), and 'Range' (containing a range selection icon and 'From'/'To' dropdowns). The 'Channel' section has a 'CLK' checkbox checked and a 'Data' checkbox unchecked. The 'Baud Rate' is set to 9600 and 'ETU' is set to 32. The 'Color' section has a rainbow color icon and five color-coded dropdowns: Start (orange), Data (blue), Parity (green), End (orange), and Error (red). The 'Range' section has a range icon and two dropdowns: 'From' (Buffer Head) and 'To' (Buffer Tail). At the bottom are 'Default', 'OK', and 'Cancel' buttons.

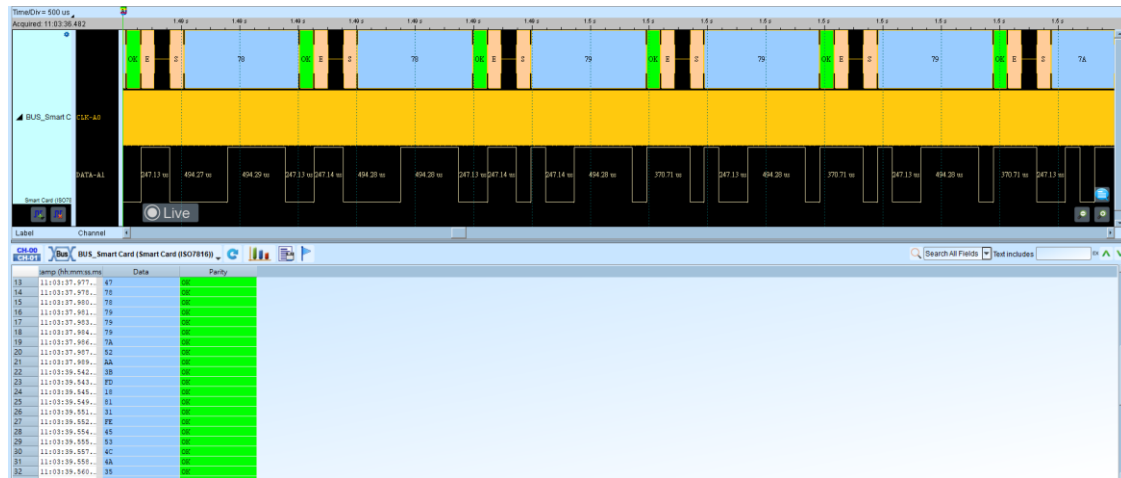
Channel

CLK: Clock of transfer signal.

Data: Data of transfer signal.

ETU(Elementary Time Unit): The number of Clocks in each Bit.

Result



SMBus

The full name System Management Bus (SMBus) is derived from I²C bus, which is a bus consisting of two signals. SMBus was defined by Intel in 1995, and contains Clock, Data, and commands based on Philips' I²C serial bus protocol. The clock frequency ranges from 10KHz to 100KHz.

Settings

Channel:

SMBCLK: Clock of transfer signal.

SMBDATA: Data of transfer signal.

Startup: PEC analysis. Enabled when checked.

8-bit addressing (Include R/W in Address): Displays the 8-bit width address (7-bit width address plus 1-bit Rd/Wr). Enabled when checked.

Device, by default, the report window displays the SMBus analysis result.

Enabled when checked:

1. **MCTP:** Display MCTP analysis result in report area.
2. **Show SBS:** The report window displays the Smart Battery System analysis, which shows the status of the battery and information such as voltage, current, or manufacturer information.
3. **Show SPD(Serial Presence Detect):** The report window displays the EEPROM analysis content, which shows the configuration information of memory modules (DDR3, DDR2, DDR, SPD SDRAM), such as the number of P-Banks, voltage, the number of row addresses/column addresses, the bit-widths, and the timing of each major operation (e.g., CL, tRCD, tRP, tRAS, etc.).

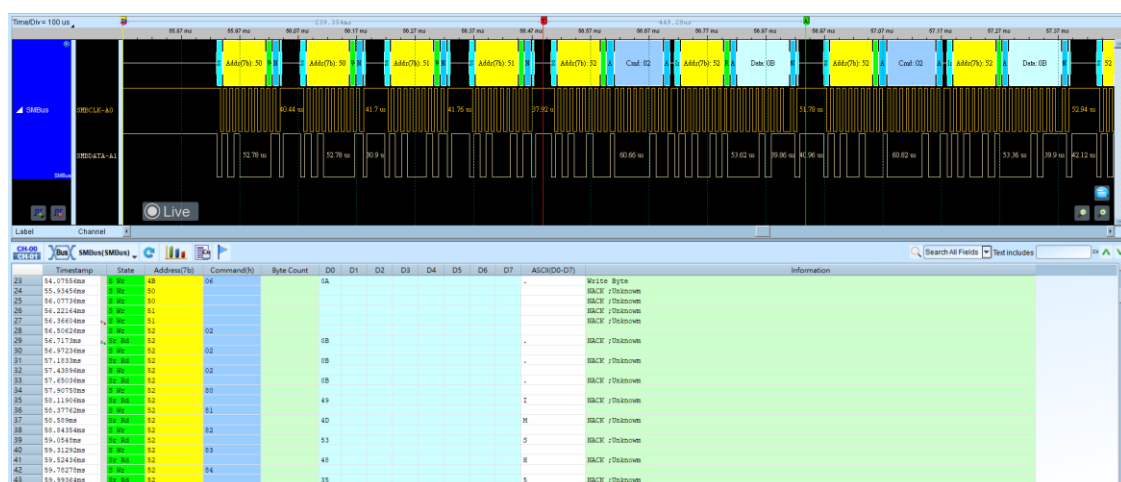
Clock Stretching: Set the time for Clock Stretching. Enabled when checked.

Ignore Glitch: Ignore noise caused by slow transitions when analyzing.

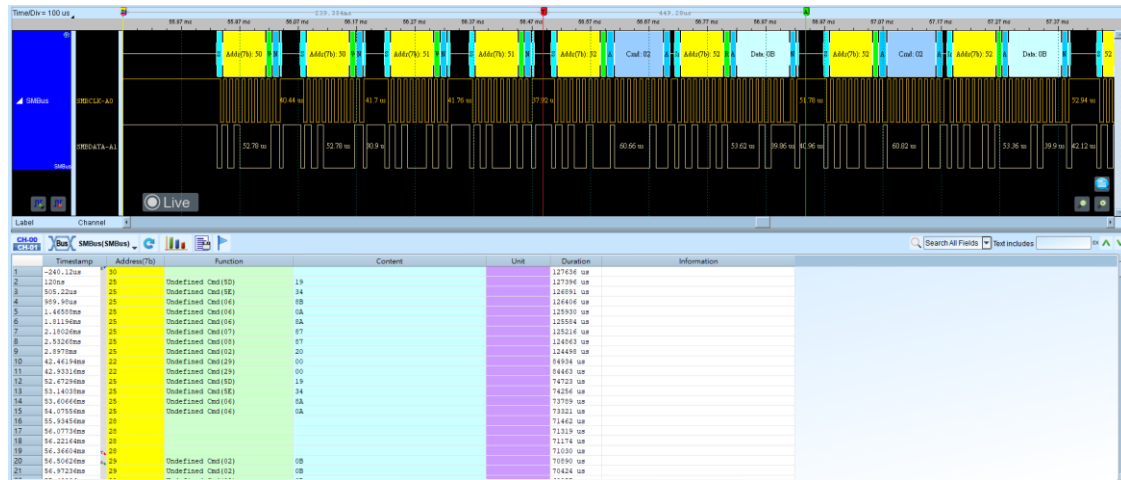
Enabled when checked.

Result

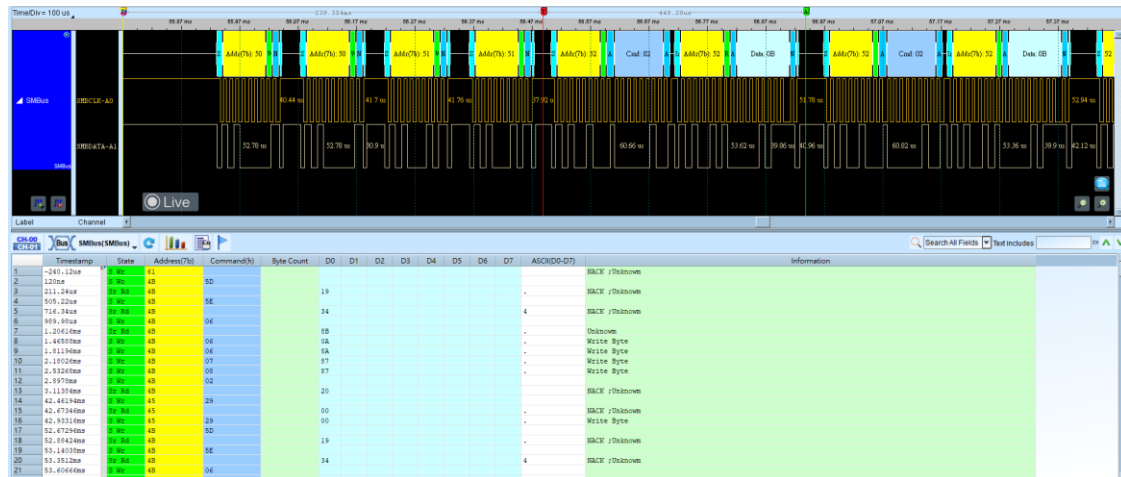
SMBus



Show SBS (Smart Battery System)



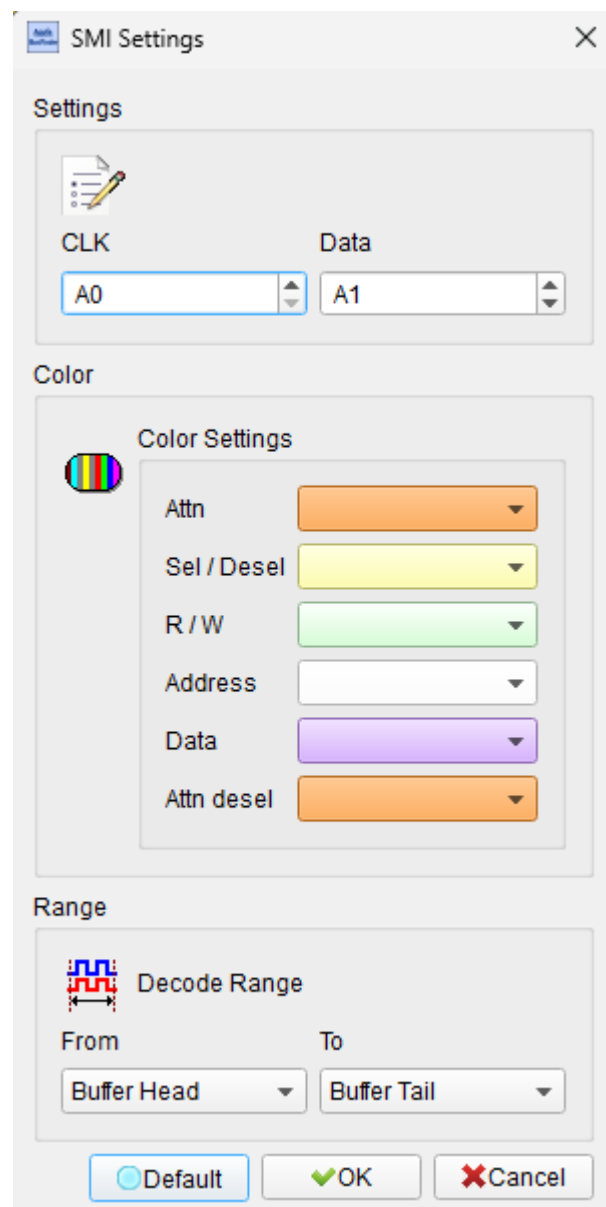
Show SPD (Serial Presence Detect)



SMI

SMI (Serial Microprocessor Interface) was developed by BDNC and consists of a Clock and Data.

Settings



SMI Settings

Settings

CLK Data

A0 A1

Color

Color Settings

Attn

Sel / Desel

R / W

Address

Data

Attn desel

Range

Decode Range

From To

Buffer Head Buffer Tail

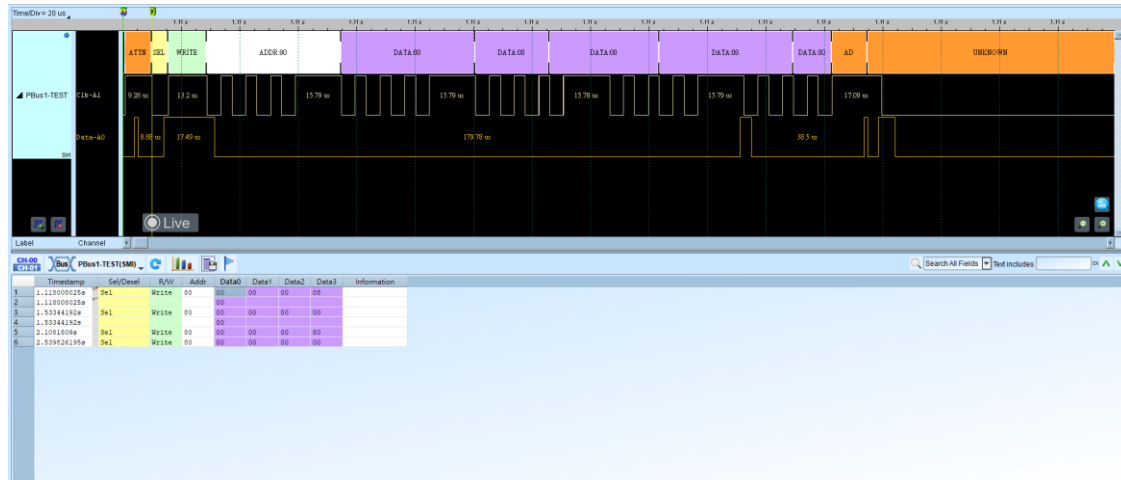
Default OK Cancel

Channel:

CLK: Clock of transfer signal.

Data: Data of transfer signal.

Result



SPI

The Serial Peripheral Interface Bus (SPI) is a 4-wire synchronous sequential data protocol for portable device platform systems. Serial peripheral interfaces are generally 4-wire, and can sometimes be 3-wire or 2-wire.

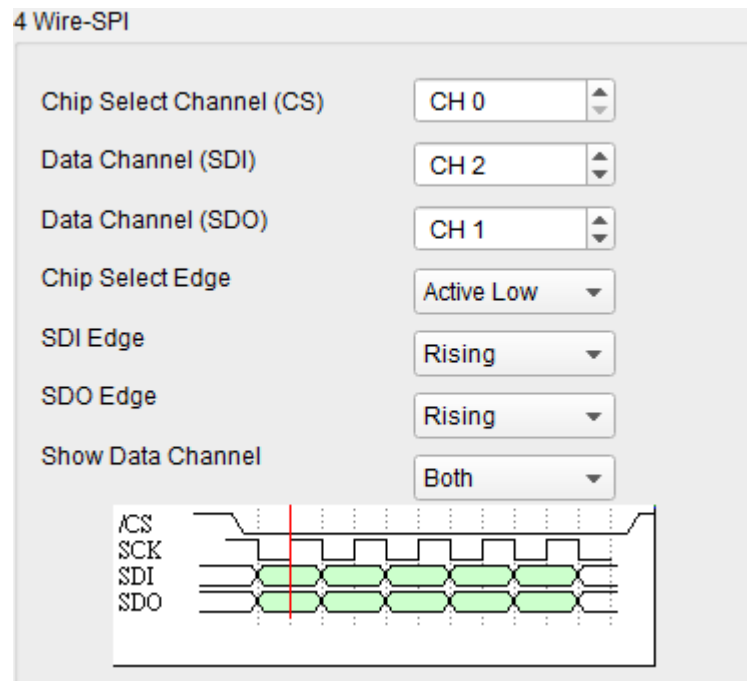
Settings

Type: Select the SPI type, the default is 3-wire-SPI, which is included:

4 Wire-SPI dialog box → CS, SCK, SDI, SDO

User can set the trigger edge of CS, SDI and SDO respectively, the default setting of CS is Active Low, and the default setting of SDI/SDO is Active High,

because the SDI and SDO data will be displayed at the same time. User can select the last data to be displayed in the display data channel as SDI only, SDO only or both, and the default is Both.



3 Wire-SPI dialog box → CS, SCK, SDA

In 3-wire Slave select mode, only 1 data channel (either SDI or SDO) is required. User can set the triggering edge of CS and Data respectively, the default setting of CS is Active Low, and the default setting of Data is Active High, for general application, the data channel is a single line and unidirectional way to transfer data.

3 Wire-SPI

Chip Select Channel (CS)

Data Channel (SDA)

Chip Select Edge Data Edge

☐ SDI(Write)-Latency-SDO(Read)

Write Length Latency

Read Length (Bits)

We also provide a one-line bidirectional transmission mode. As shown in the figure below

☒ SDI(Write)-Latency-SDO(Read)

Write Length Latency

Read Length (Bits)

User only need to check “SDI(Write)-Waiting-SDO(Read)”, then user can set the bit number of bidirectional transmission. Let's take Master as our point of view, the write length is the number of bits that Master puts into the data channel, the minimum is 1. The number of bits that wait for Slave to process is the minimum is 0. Then the data is collected according to the read length, the minimum is 1. The maximum value of these 3 parameters is 65535.

3 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDI, SDO

Since CS is not used, user has to set the Idle time of SCK as the frame separating time. In 3-wire without Slave select mode, user need to set the channel where SDI/SDO is located and its trigger edge to Active High. In the 3-wire non-slave select mode, user need to set the channel where SDI/SDO is located, and set the trigger edge of SDI/SDO to Active High, and set the time to wait for Clock Idle to separate the frames. The SDI and SDO data will appear at the same time. User can select the last data to be displayed in SDI only, SDO only or both in the display data channel, and the default is Both.

3 Wire-SPI(Unused Chip Select)

Data Channel (SDI)

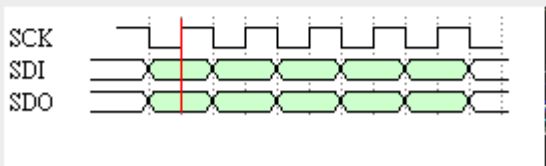
Data Channel (SDO)

SDI Edge

SDO Edge

Frame guard time ns

Show Data Channel



2 Wire-SPI (Unused Chip Slave) dialog box → SCK, SDA

Since CS is not used, user has to set the Idle time of SCK as the frame separating time. In 2-wire without Slave select mode, user need to set the channel where the data is located and its trigger edge to Active High. The trigger edge of the data channel and the trigger edge of the data channel should be set to Active High, and set the time to wait for the Clock Idle as the Frame Separation. In general application, the data channel is a single line and

unidirectional way to transfer the data.

2 Wire-SPI(Unused Chip Select)

Data Channel (SDA) CH 0

Data Edge Rising

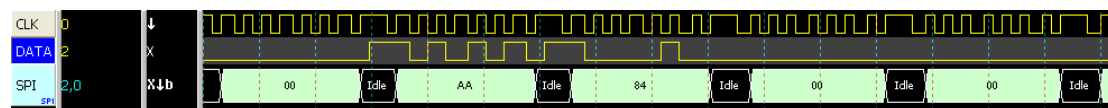
☐ SDI(Write)-Latency-SDO(Read)

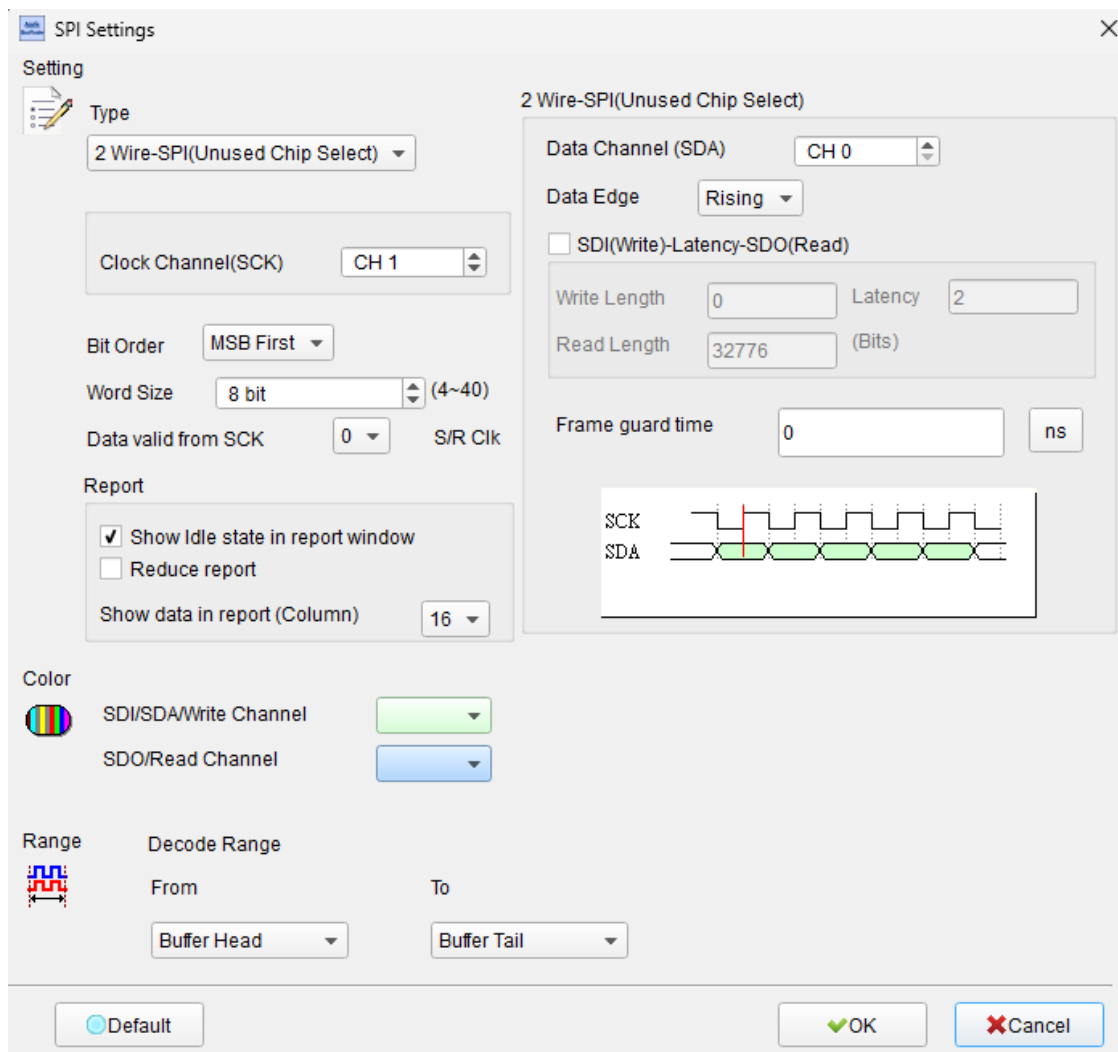
Write Length 0 Latency 2

Read Length 32776 (Bits)

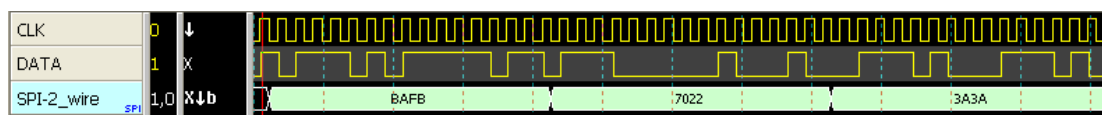
Frame guard time 0 ns

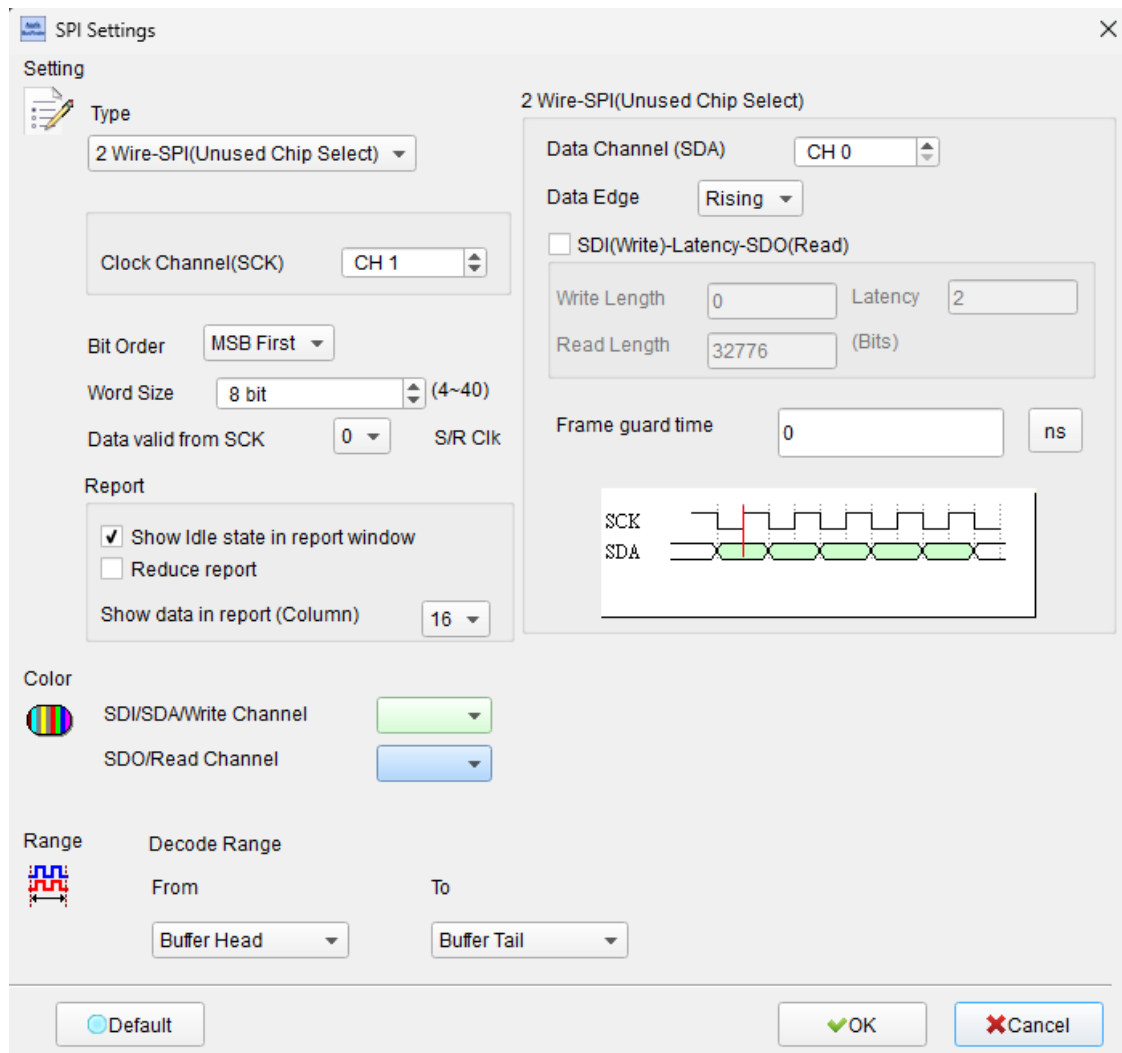
If Slave select is not used, and the time between frames is not 0, the application example is as follows. The signals are only CLK, DATA, Frame is separated by 6 us, and the data trigger edge is Rising. it can be seen that if the Clock pause interval is more than 6 us, it will be recognized as Idle.





When Slave select is not used, and the Frame separation time is 0, it can be another kind of continuous data analysis, as shown in the following figure. The signal is only CLK, DATA, and the time between frames is 0, the data trigger is in Falling.





Bit Order: You can configure the SPI data interpretation as either MSB first or LSB first. The default setting is LSB first.

Word Size: You can set the data word size in bits. During SPI analysis, this value will define the number of bits for each data word. The minimum value is 4, and the maximum value is 40. The default value is 8.

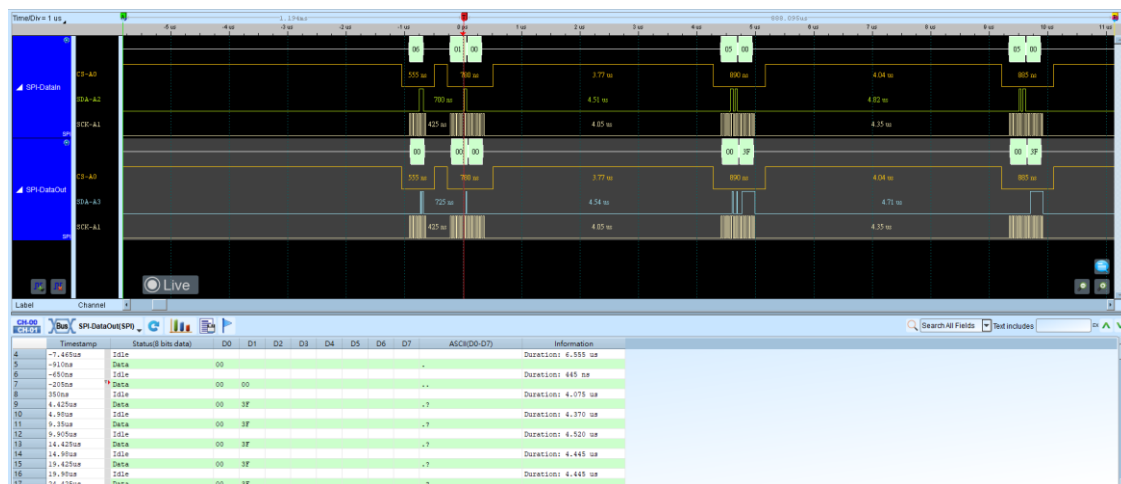
Report:

Show Idle state in report window: In SPI applications, there may be intervals with the Idle State between each data capture. To make data review easier, you can configure the report window to hide the Idle State. By default, the Idle State is shown.

Reduce report: You can configure consecutive SPI data to be displayed in the report window in a format ranging from 1 to 16 columns. The default setting is 16 columns, and the ASCII-encoded results can be viewed on the far right side of the report window.

Data Valid from SCK: In certain devices using SPI transmission, there is a delay between the data output and the valid data, which does not align with the clock's edge. To accommodate such devices, you can configure the "Data Valid from SCK" to delay this time. You can input the delay time in terms of the sampling rate, with a range of 0-3. By default, there is no delay. If set to 1, with a sampling rate of 200 MHz, the actual delay time will be 5 ns.

Result



SPI NAND

The SPI NAND Flash Memory series uses the SPI/QPI transmission protocol for data communication. The SPI NAND bus analysis allows users to view both command and input/output bus information simultaneously, saving time when using the SPI bus analysis waveform.

Settings

SPI NAND Settings

Parameter Settings

CS# A0 SCK A1 Micron

SI / SO0 A2 SO / SO1 A3 MT29FXG01AAADD

WP / SO2 A4 HOLD# / SO3 A5

☐ Refer to #Hold Status

Start up reading mode Continuous Read

Command deselect time 100 ns

☐ Latch IC output data on SCK rise edge

Clock LOW to output valid 15 ns

☒ Show Calculated Physical Address From Page Address

☐ Show all repeated Get/Set Feature Data

Color

Op Code Dummy

Address Data In

Data Out

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

CS#: Chip Select of transferred signal.

SCLK: Clock of transferred signal.

SIO0 – SIO3: Data pins for data transfer.

Start up reading mode: Enables selection of the read state during initial analysis.

Command deselect time: Adjustable hold time for determining CS# inactivity during analysis.

Clock LOW to output valid : Adjustable setting for determining the actual data position during analysis.

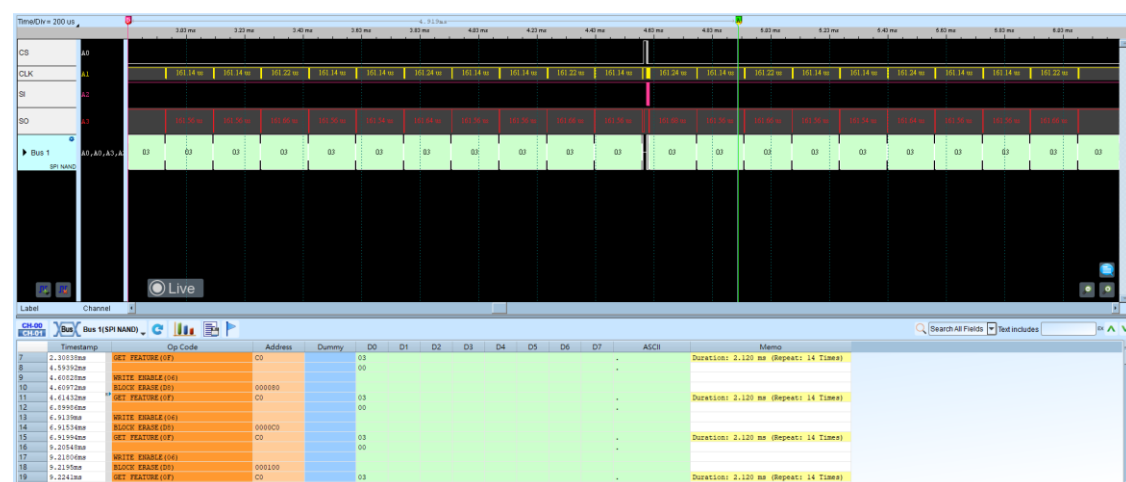
Refer to #Hold Status: Decode based on the state of the #Hold pin. Enabled when checked.

Latch IC output data on SCK rise edge: Latch Data on the rising edge of SCK for analysis. Enabled when checked.

Show Calculated Physical Address From Page Address: Display the full address. Enabled when checked.

Show all repeated Get/Set Feature Data: Fully display repeated Get or Set Feature data. Enabled when checked.

Result



The report will delete the repeated value while Op Code = Get Feature (0F).

And mark its duration time °

SSI

The Synchronous Serial Interface (SSI) protocol has four kinds of signals:

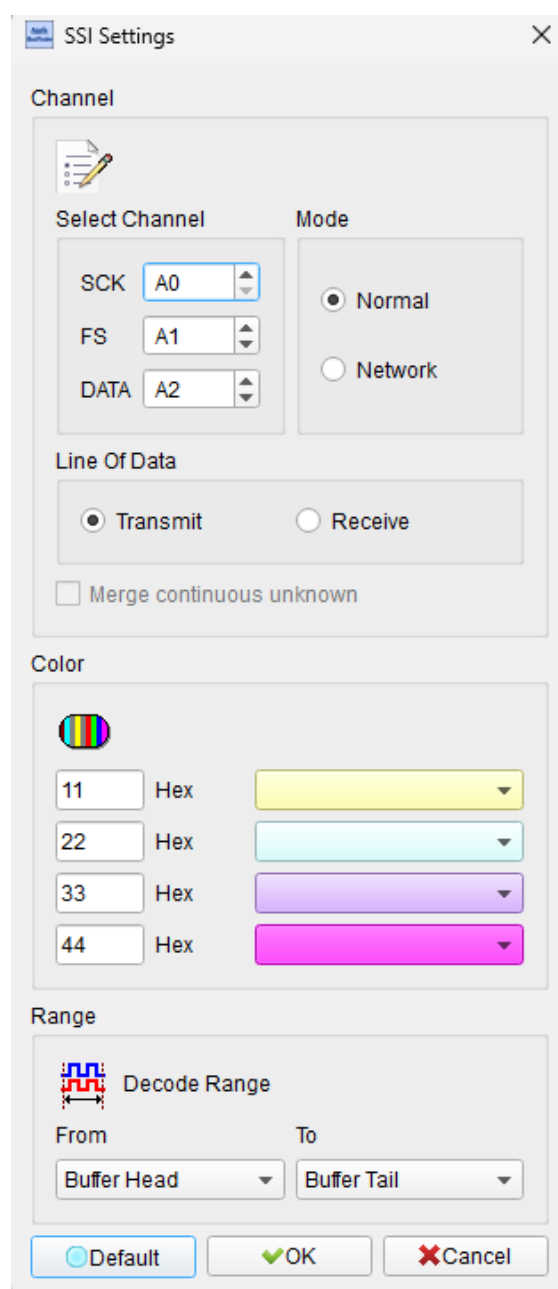
Serial Clock (SCK), Transmit Data, Receive Data and Transmit/Receive Frame

Synchronous (FS). The SSI protocol supports either the Normal or Network

mode that is independent of whether the transmitter and the receiver are

synchronous or asynchronous.

Settings



SSI Settings

Channel

Select Channel

SCK A0

FS A1

DATA A2

Mode

☒ Normal

☐ Network

Line Of Data

☒ Transmit

☐ Receive

☐ Merge continuous unknown

Color

11 Hex

22 Hex

33 Hex

44 Hex

Range

Decode Range

From To

Buffer Head Buffer Tail

Default OK Cancel

Select Channel: Assign the signal pins of the Device Under Test (DUT) to the corresponding channel numbers of the logic analyzer

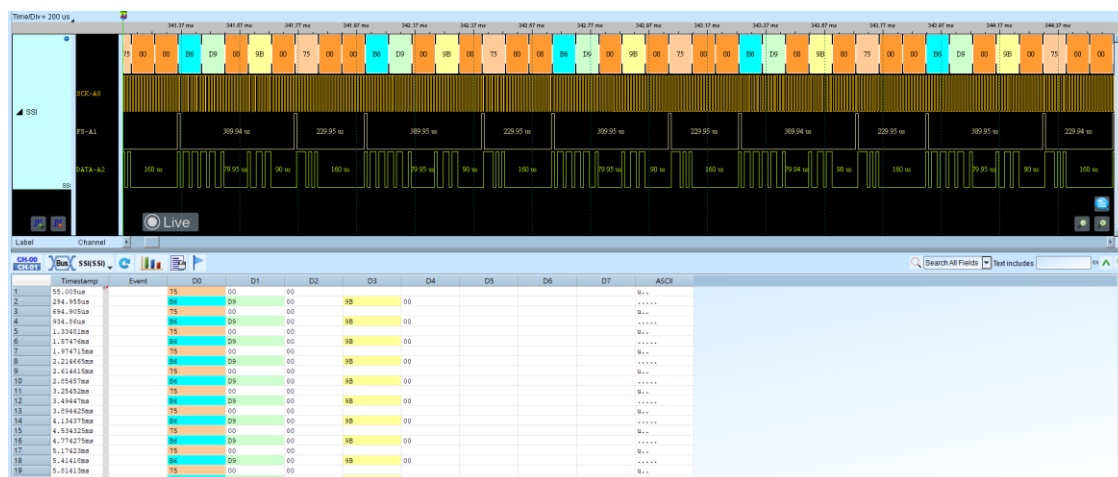
Mode: Normal or Network.

Line Of Data: Transmit or Receive.

Merge continuous unknown: Combine the unknown data only in Network mode.

Result

Click **OK** to run SSI decode and see the result on the Report Window below.



ST7669

ST76669 was developed by Sitronix to interface with the LCD module.

Settings

ST7669 Ver. 1.3a Settings

Parameter

Type: 8-bit Serial Interface

Channel

Chip Select Channel (/CS): A0

Clock Channel (SCL): A1

Serial Data Input (MPU SI): A2

Serial Data Input (LCD SI): A0

A0: A3

Range

Decode Range

From: Buffer Head To: Buffer Tail

Color

D/C: [Dropdown]

Command: [Dropdown]

Data: [Dropdown]

Read: [Dropdown]

Default OK Cancel

Type, selectable options:

1. 8-bit Serial Interface
2. 8-bit Serial Interface + LCD SI
3. 9-bit Serial Interface
4. 9-bit Serial Interface + LCD SI

Chip Select Channel (/CS): CS for ST7669 data transmission.

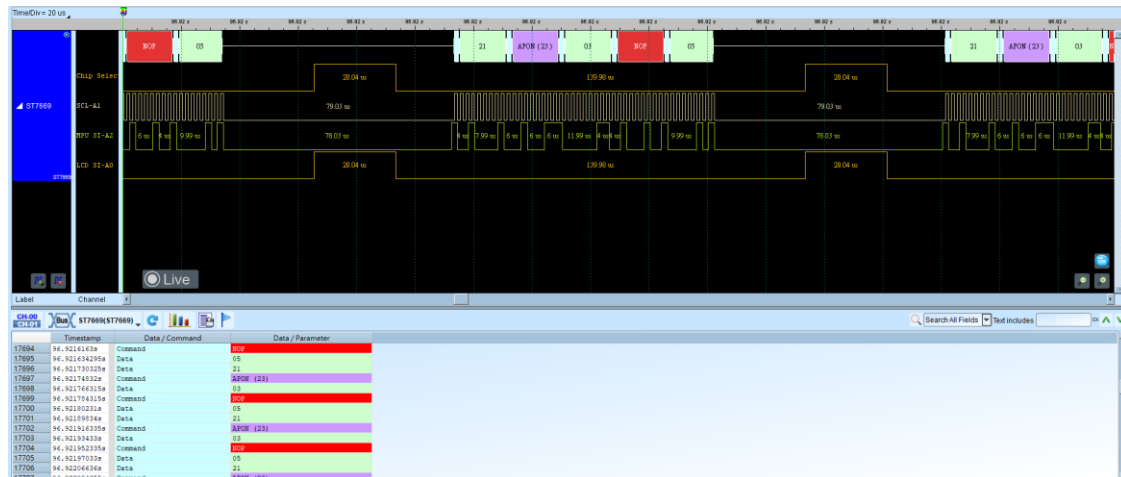
Clock Channel (SCL): Clock for ST7669 data transmission.

Serial Data Input (MPU SI): MPU Data Input for ST7669 data transmission.

Serial Data Input (LCD SI): LCD Data Input for ST7669 data transmission.

A0: A0 for ST7669 data transmission.

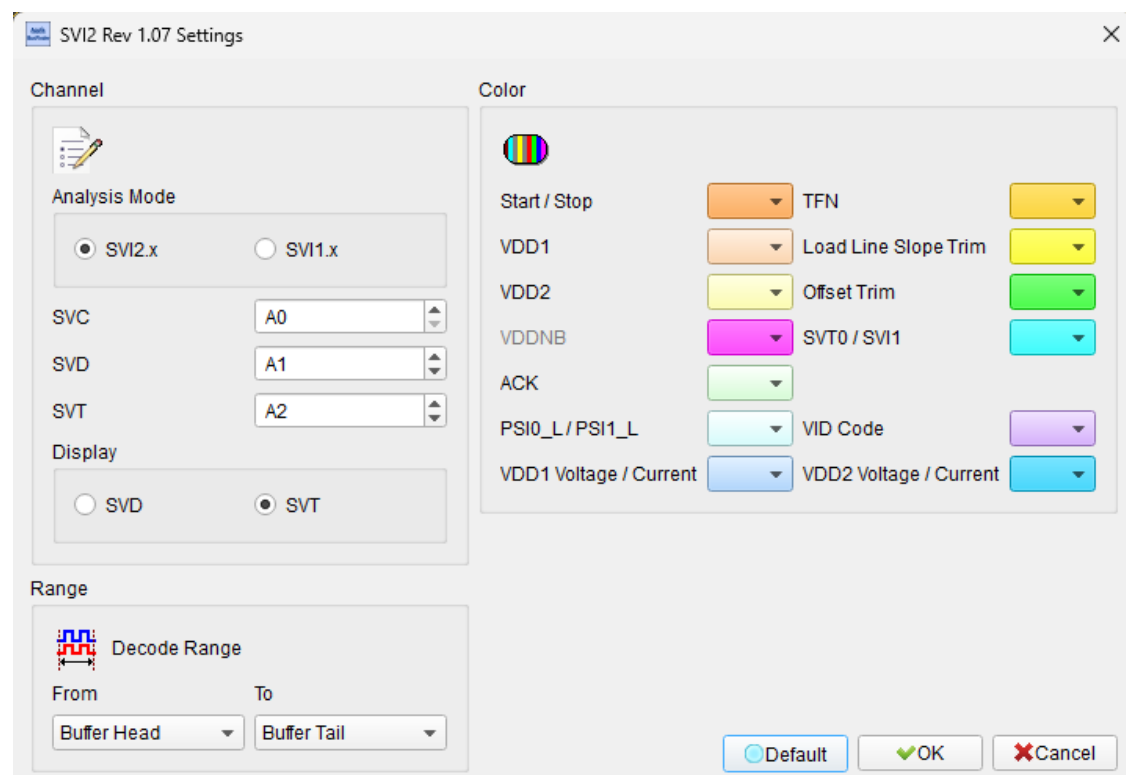
Result



SVI2

The SVI2 (Serial VID Interface 2.0) bus is a communication protocol used by AMD for power management control data transmission, typically applied in voltage control. SVI2 bus analysis allows users to view transmitted signal packets, reducing the time needed for waveform interpretation. It operates with a voltage range of 1V to 1.8V and a maximum frequency of 20MHz. The interface consists of three signal channels: SVC, SVD, and SVT. When measuring signals, it is important to set the trigger level between 0.6V and 0.9V to ensure stable signal triggering.

Settings



Analysis Mode:

SVI2.x / SVI1.x: Select SVI2 / SVI decoding.

Channel:

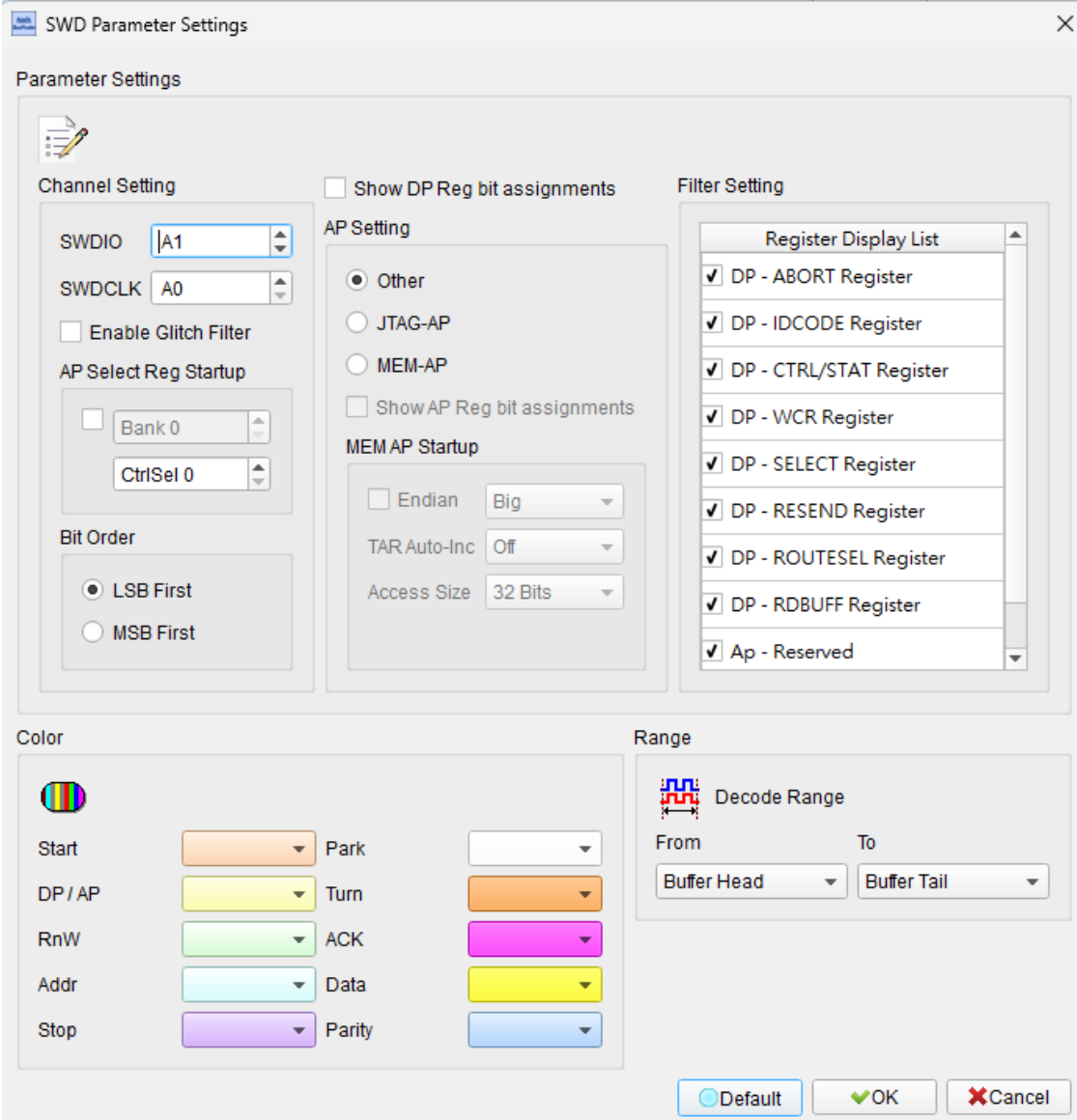
SVC: Clock for transferred signal.

SVD: Data for transferred signal.

SWD

SWD (Serial Wire Debug) is a test protocol defined by ARM, consisting of two signal lines: SWDIO and SWDCLK. It serves as a debug access protocol for CoreSight™ Debug Access Port and is an alternative to JTAG when there are pin count limitations.

Settings



The image shows the 'SWD Parameter Settings' dialog box. It is divided into several sections: 'Channel Setting', 'AP Setting', 'Filter Setting', 'Color', and 'Range'. The 'Channel Setting' section includes dropdowns for SWDIO (A1) and SWDCLK (A0), a checkbox for 'Enable Glitch Filter', and a section for 'AP Select Reg Startup' with a checkbox and dropdowns for 'Bank 0' and 'CtrlSel 0'. The 'AP Setting' section has radio buttons for 'Other', 'JTAG-AP', and 'MEM-AP', a checkbox for 'Show AP Reg bit assignments', and a 'MEM AP Startup' section with a checkbox for 'Endian' (Big), a dropdown for 'TAR Auto-Inc' (Off), and a dropdown for 'Access Size' (32 Bits). The 'Filter Setting' section contains a 'Register Display List' with a list of registers and checkboxes: DP - ABORT Register, DP - IDCODE Register, DP - CTRL/STAT Register, DP - WCR Register, DP - SELECT Register, DP - RESEND Register, DP - ROUTESEL Register, DP - RDBUFF Register, and Ap - Reserved. The 'Color' section has a color palette icon and a table of color-coded fields: Start (orange), DP / AP (yellow), RnW (green), Addr (cyan), Stop (purple), Park (white), Turn (orange), ACK (magenta), Data (yellow), and Parity (blue). The 'Range' section has a 'Decode Range' icon and dropdowns for 'From' (Buffer Head) and 'To' (Buffer Tail). At the bottom are buttons for 'Default', 'OK', and 'Cancel'.

SWDIO: I/O data.

SWDCLK: Clock.

AP Select Reg Startup						
<input type="checkbox"/>	Bank = 0	Time	Select	RnW	Address (h)	ACK Data
	CtrlSel = 0	-0.0003 ms	AP	Write	0	OK 23 00 00 52

AP Select Reg Startup						
<input checked="" type="checkbox"/>	Bank = 0	Time	Select	RnW	Address (h)	ACK Data
	CtrlSel = 0	-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	OK 23 00 00 52

Bit Order: LSB or MSB.

Show DP Reg bit assignments: Show the DP register information.

Select	RnW	Address (h)	ACK	Data
DP	Write	SELECT Register (8)	OK	00 00 00 00
				APSEL [31:24] 00
				APBANKSEL [7:4] 0
				CTRLSEL [0] 0

AP Setting: You can select between MEM-AP and JTAG-AP for AP Register decoding. If the user selects Other, the AP data will only display as Bank X Register X without further interpretation.

JTAG-AP: Show the JTAG AP decode.

MEM-AP: Show the MEM AP decode.

Other: Show Bank X Register X.

<input checked="" type="radio"/> Other	Time	Select	RnW	Address (h)	ACK	Data
<input type="radio"/> JTAG-AP	-0.0003 ms	AP	Write	Bank 0 Register 0 (0)	OK	23 00 00 52
<input type="radio"/> MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	Bank 0 Register 1 (4)	OK	00 00 02 68
<input type="radio"/> Other	Time	Select	RnW	Address (h)	ACK	Data
<input checked="" type="radio"/> JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
<input type="radio"/> MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	PSEL Register (4)	OK	00 00 02 68
<input type="radio"/> Other	Time	Select	RnW	Address (h)	ACK	Data
<input type="radio"/> JTAG-AP	-0.0003 ms	AP	Write	CSW Register (0)	OK	23 00 00 52
<input checked="" type="radio"/> MEM-AP	0.0308 ms	DP	Read	RDBUFF Register (C)	OK	00 00 00 00
	2.9998 ms	AP	Write	TAR Register (4)	OK	00 00 02 68

Show AP Reg bit assignments: Display the AP register information if JTAG-AP or MEM-AP checked.

MEM-AP	Select	RnW	Address (h)	ACK	Data
<input checked="" type="checkbox"/> Show AP Reg bit assignments	AP	Read	BASE Register (8)	OK	00 00 00 00
					BASEADDR [31:12] E00FF
					Format [1] 1
					Entry present [0] 1

MEM AP Startup: When selecting MEM-AP, the contents of MEM-AP can be initialized. During data capture, if a corresponding register address is encountered, the data will be updated according to the bus content. Enabling the Endian checkbox activates the display of data along with the corresponding read/write addresses.

<div>MEM-AP</div> <div><input checked="" type="checkbox"/> Show AP Reg bit assignments</div> <div>MEM AP Startup</div> <div><input checked="" type="checkbox"/> Endian<div>Big</div></div> <div>TAR Auto-Inc<div>Single</div></div> <div>Access Size<div>16 Bits</div></div>		AP		Read	DRW Register	(C)	OK	00 00 00 0D	TAR Address = E000EFF0
								Big-Endian	
								000D Access to E000EFF0	
								0000 Access to E000EFF2	
		AP		Read	DRW Register	(C)	OK	00 00 00 E0	TAR Address = E000EFF2
								Big-Endian	
								00E0 Access to E000EFF2	
								0000 Access to E000EFF4	

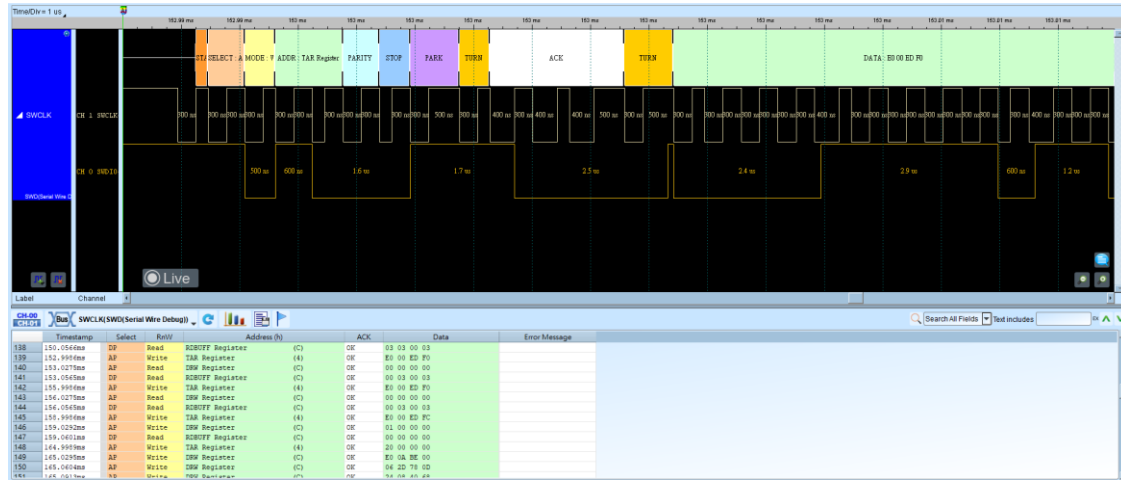
Filter Setting: Filter the unwanted Registers.

Filter Setting

Register Display List

- ☒ DP - ABORT Register
- ☒ DP - IDCODE Register
- ☒ DP - CTRL/STAT Register
- ☒ DP - WCR Register
- ☒ DP - SELECT Register
- ☒ DP - RESEND Register
- ☒ DP - ROUTESEL Register
- ☒ DP - RDBUFF Register
- ☒ Ap - Reserved

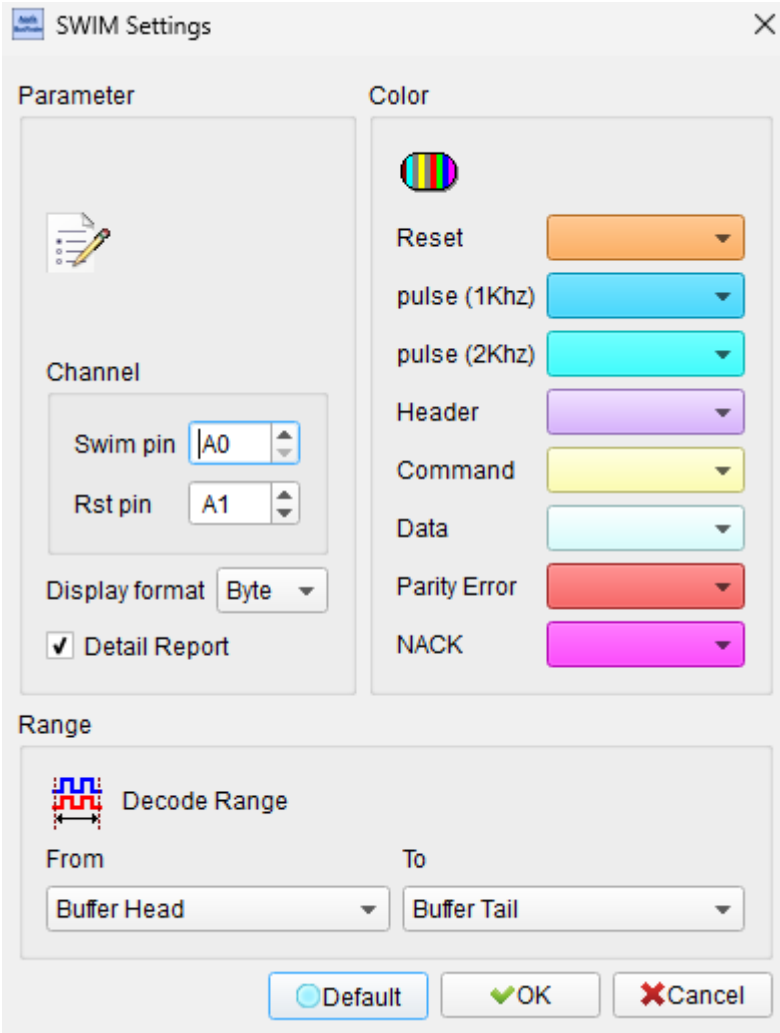
Result



SWIM

SWIM is the single wire interface module of STM8 8-bit MCUs family. While the CPU is running, the SWIM allows a non-intrusive read/write accesses to be performed on-the-fly to the RAM and peripheral registers, for debug purposes.

Settings



The SWIM Settings dialog box is divided into several sections:

- Parameter Section:**
 - Channel:** Contains two spinners: "Swim pin" set to "A0" and "Rst pin" set to "A1".
 - Display format:** A dropdown menu currently set to "Byte".
 - Detail Report:** A checked checkbox.
- Color Section:**
 - A color selection icon (a circle with vertical rainbow bars).
 - A list of color-coded items with dropdown arrows:
 - Reset (Orange)
 - pulse (1Khz) (Light Blue)
 - pulse (2Khz) (Cyan)
 - Header (Purple)
 - Command (Yellow)
 - Data (Light Cyan)
 - Parity Error (Red)
 - NACK (Magenta)
- Range Section:**
 - Decode Range:** A section with a waveform icon and a double-headed arrow.
 - From:** A dropdown menu set to "Buffer Head".
 - To:** A dropdown menu set to "Buffer Tail".
- Buttons:** At the bottom, there are three buttons: "Default" (with a blue circle icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

Swim pin: set the Swim Channel.

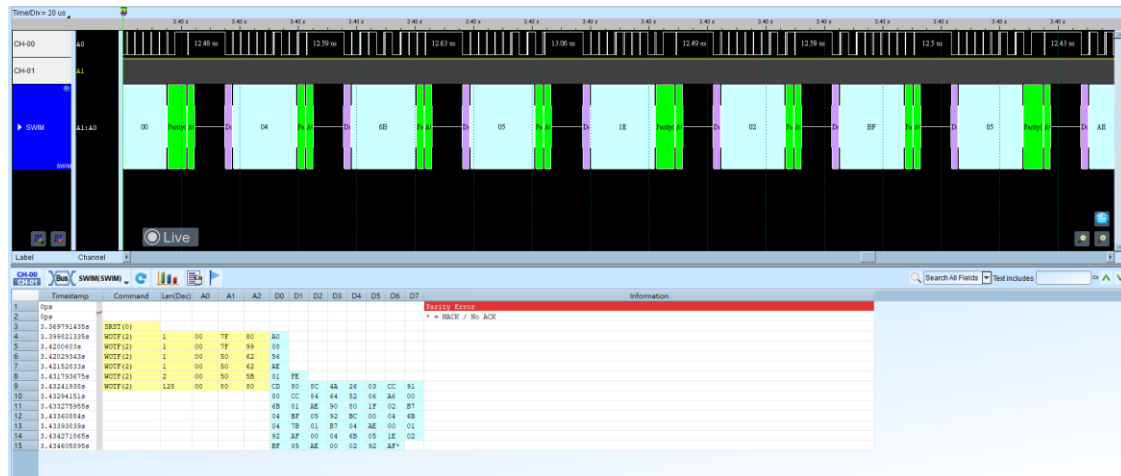
Rst pin: set the Reset Channel.

Display format: the display method of waveform decode (Byte, Bit).

Detail Report: show the detail information of SWIM decode.

Result

Normal



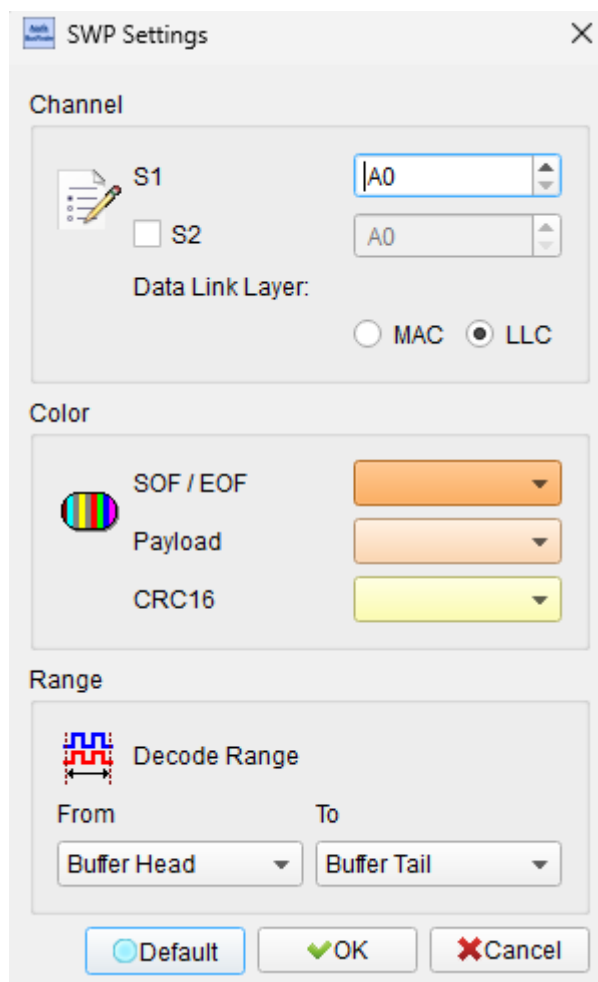
Detail Report



SWP

The Single Wire Protocol (SWP) is a single-wire connection between the SIM card and a NFC chip in a cell phone.

Settings



The image shows the 'SWP Settings' dialog box. It has three main sections: 'Channel', 'Color', and 'Range'.
 - **Channel**: Contains two checkboxes, 'S1' and 'S2'. 'S1' is checked and has a dropdown menu set to 'A0'. 'S2' is unchecked and has a dropdown menu set to 'A0'. Below these is the 'Data Link Layer' section with two radio buttons: 'MAC' and 'LLC'. 'LLC' is selected.
 - **Color**: Contains three color selection buttons. The first is labeled 'SOF / EOF' with a rainbow icon. The second is labeled 'Payload' with an orange icon. The third is labeled 'CRC16' with a yellow icon.
 - **Range**: Contains a 'Decode Range' section with a red and blue icon. Below it are two dropdown menus: 'From' (set to 'Buffer Head') and 'To' (set to 'Buffer Tail').
 At the bottom are three buttons: 'Default' (with a blue circle icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

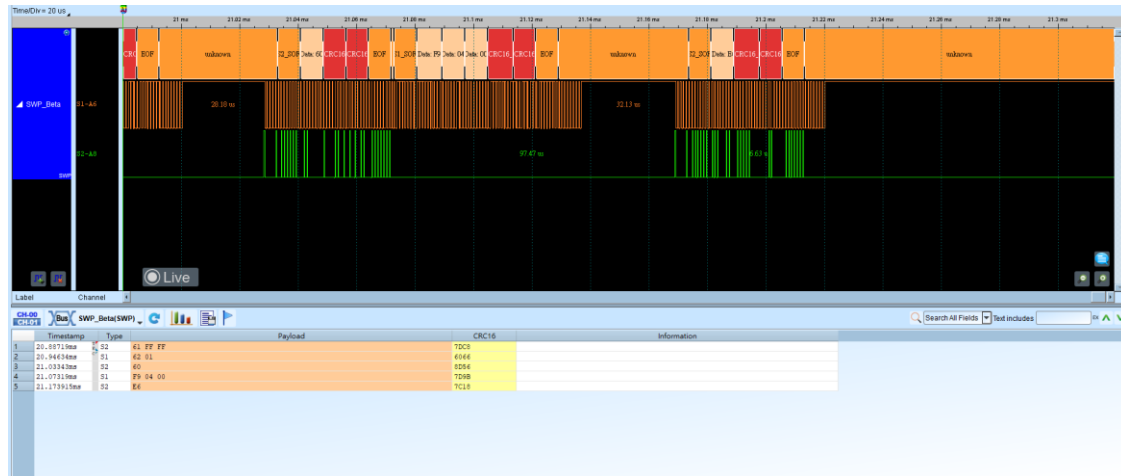
S1: I/O data.

S2: I/O data in current domain and it need convert to voltage domain.

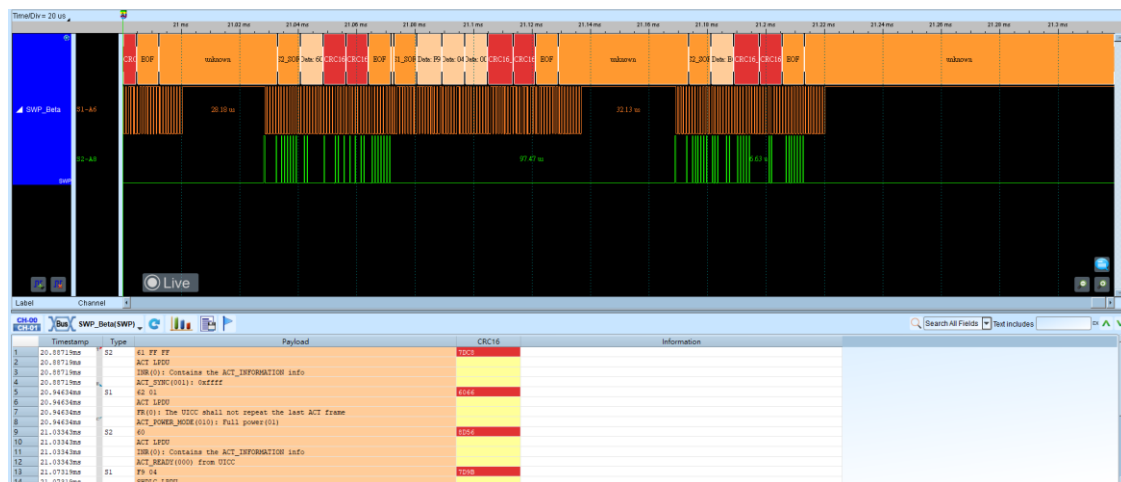
Data Link Layer: Supported MAC and LLC layers

Result

MAC



LLC



TDM

TDM Audio (Time Division Multiplexing Audio) is a method for transmitting multiple audio channels over a single data line (or a pair of data lines) by dividing the transmission content into multiple time slots. This technique is widely used in digital audio systems to efficiently manage and transmit multiple audio streams, particularly in professional audio, consumer electronics, and automotive applications.

Settings

TDM Settings

Channel

Clock(SCK) | A0

Word Select(WS) | A1

Data(SD) | A2

Mode Select

Slot Width Mode

Audio Settings

Slot bits | 16 bit(s)

Audio bits: | 16 bit(s)

Channel Count | 2

Latch Edge | Falling

Enable Pulse | High

Data Offset | 0 bit(s)

☐ LSB First

☐ Save as CSV file

Range

Decode Range

From | Buffer Head | To | Buffer Tail

Sound Reduction(Max Ch. = 8)

☐ Display the audio waveform ☐ Save as WAV file

☐ Align common sampling rate ☐ Enable full scale

☐ Playback

☒ All ☐ 5 Sec ☐ 3 Sec

Channel: The signal pins of the Device Under Test (DUT) are assigned to the channel numbers of the logic analyzer.

Option: Adjust the detailed settings of the audio signal.

Slot bits: Data width of an audio channel.

Audio bits: Valid bits in the slot bits.

Channel Count: Number of audio channels (e.g., 2, 4, 8)

Latch Edge: Choose which clock edge to latch data (Rising or Falling)

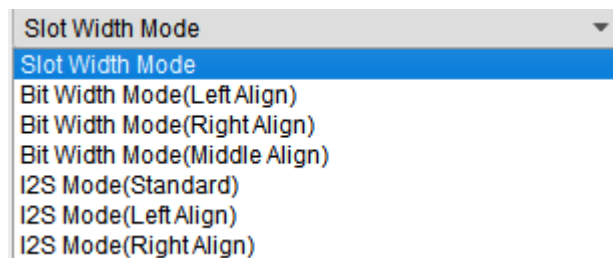
Start Pulse: Set the polarity of the active pulse (High or Low)

Data Offset: Bit offset before starting data capture

LSB First: Check this if the data is transmitted with LSB first

Save as CSV file: Save the decoded result as a .CSV file

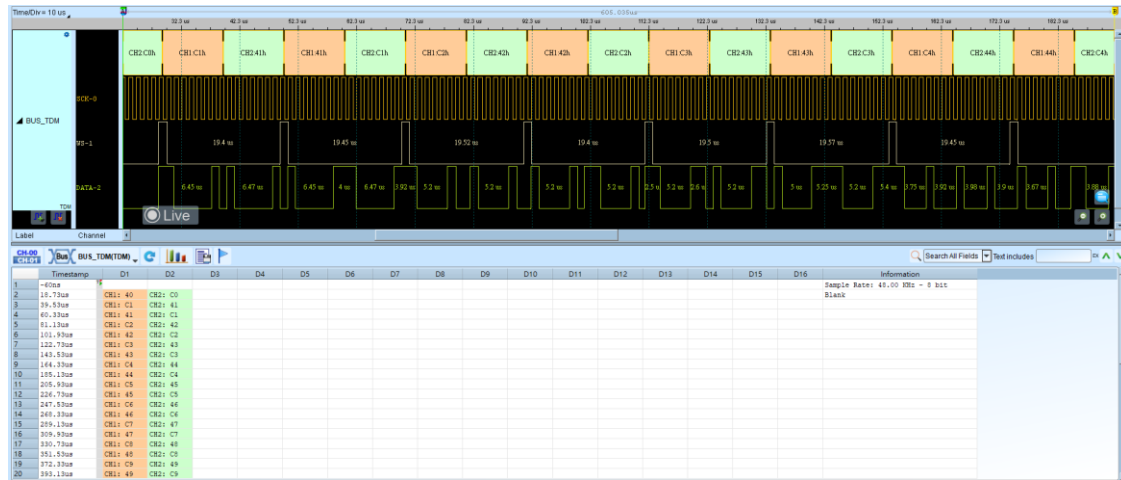
Mode: Set the data arrangement format. The following formats are currently supported:



Sound Reduction: Set whether to save, replay, or visualize the audio waveform based on the analysis results after decoding. Enabled when selected.

- **Display the audio waveform**
- **Enable meet full scale**
- **Save as WAV file**
- **Align common sampling rate**
- **Playback: Choose to play all, 5 seconds, or 3 seconds**

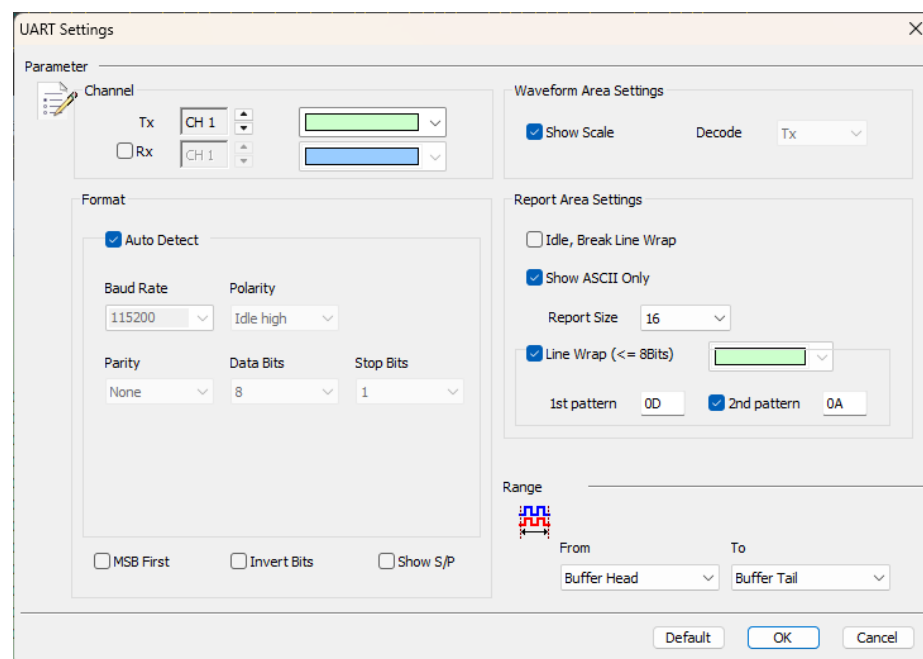
Result



UART(RS-232, RS485)

It is a serial data communication interface standard established by the Electronic Industries Alliance (EIA) in the United States. In the RS-232 and RS-485 standards, characters are transmitted sequentially as a series of bits in a serial manner. The advantages of this method include fewer transmission lines, simpler wiring, and longer transmission distances. Since RS-485 uses differential signaling, the signal must be converted into a logic signal before measurement. The logic analyzer (LA) cannot directly measure differential signals.

Settings



Channel:

Tx: Assign the Tx signal pin to the corresponding channel number of the logic analyzer.

Rx: Assign the Rx signal pin to the corresponding channel number of the logic analyzer. Enabled when selected.

Auto: Automatically detect the settings for the following options. Enabled when selected.

Baud Rate: The data transmission speed, measured in bits per second (bps). The supported range is 110 to 2M bps.

Polarity: Includes Idle High and Idle Low formats.

Parity: Includes N - None Parity (No parity bit), O - Odd Parity, and E - Even Parity.

Data Bits: Can be set between 4 to 16 bits.

Stop Bits: Can be set to 1, 1.5, 2, 2.5, 3, 3.5, 4, or 4.5 bits.

MSB First: When selected, the Most Significant Bit (MSB) comes after the Start Bit. When not selected, the Least Significant Bit (LSB) is used.

Invert Bits: Reverses High and Low levels. Enabled when selected.

Show S/P: Displays Start and Stop in the waveform area. Enabled when selected.

Waveform Area Settings:

Decode: Select whether to display the Rx or Tx decoding results in the waveform area. The Rx option is only effective when the Rx channel is enabled.

Show Scale: Displays the scale in the waveform area. Enabled when selected.

Report Area Settings, enabled when selected:

Idle, Break Line Wrap: When the bus Idle/Break, the report is displayed on a new line.

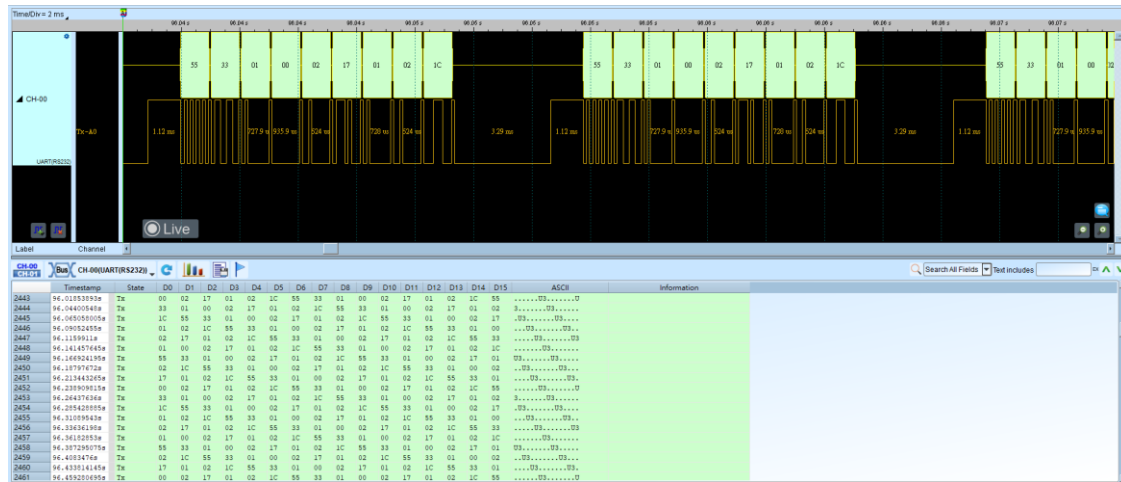
Show ASCII Only: Show only ASCII reports.

Report Size: Sets the number of Data fields in the report area. Can be set to 16 or 32.

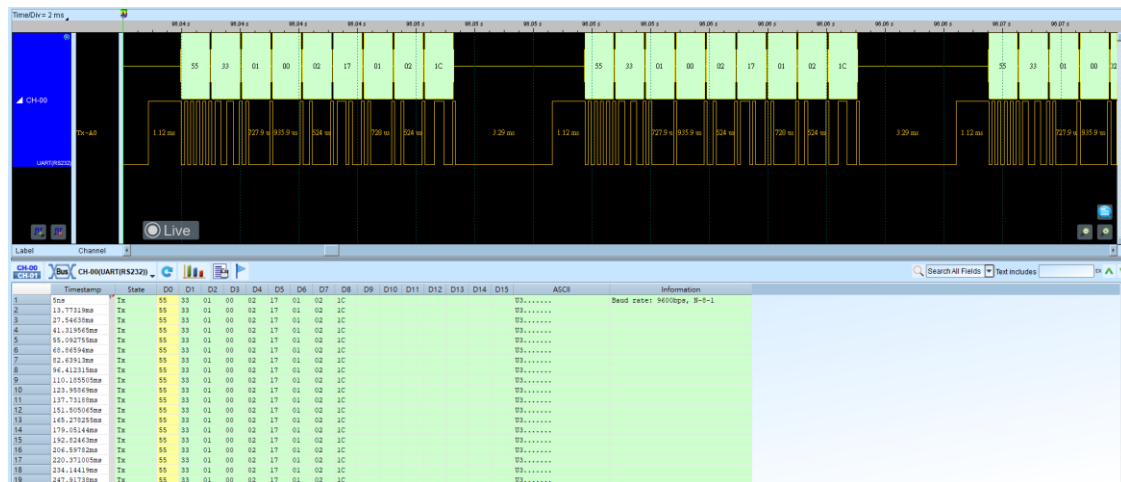
Line Wrap Data: Allows setting two values as the primary order for decoding, making it easier to view analysis results.

Result

Normal Data Analysis Displaying



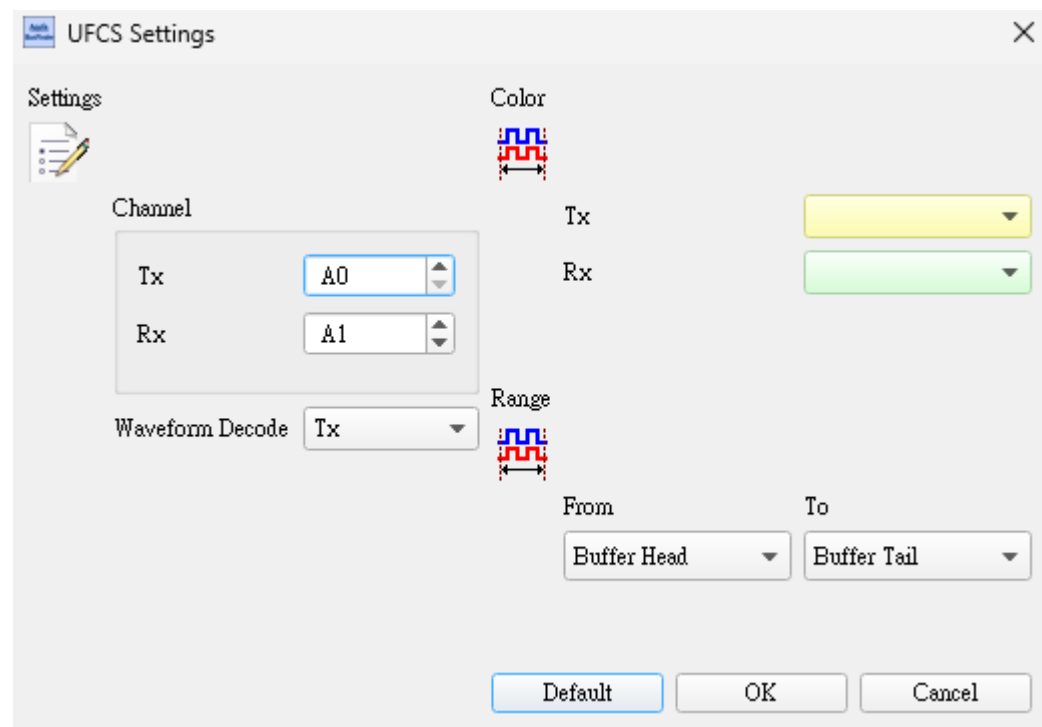
Enable Line Wrap Data Analysis Displaying



UFCS

UFCS(Universal Fast Charging Specification) formulate integrated fast charging standards for mobile terminals to solve the problem of incompatibility between fast charging and create a fast, safe and compatible charging environment for end users. The power supply port of UFCS adopts USB Type-A charging port, and the signal transmission is based on USB D+/D-.

Settings



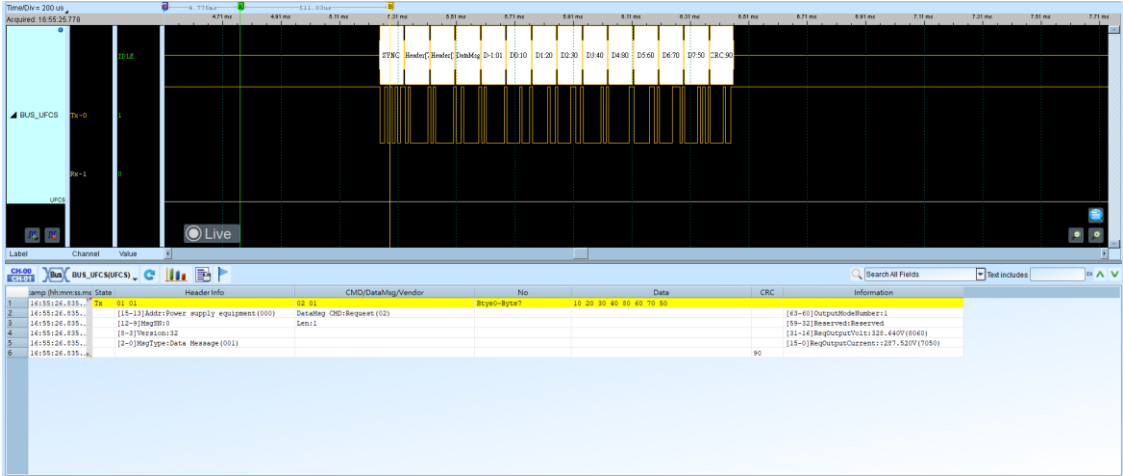
Channel: Set the Tx/Rx channel of UFCS.

Waveform Decode: Tx/ Rx.

(Multiple sets of waveform area decoding cannot be displayed on a single decoder. If you need to view multiple sets at the same time, please add an additional set of decoders.)

Result

UFCS



ULPI

UTMI + Low Pin Interface. ULPI is the Low Pin version of UTMI. UTMI (USB2.0 Transceiver Macrocell Interface) is a protocol for USB controller and USB PHY communication. Compared with ULPI, UTMI has more control signals and supports 8bit / 16bit data interface.

Parameter:

ULPI Settings

Parameter

Channel

CLK A0

DIR A1

STP A2

NXT A3

D0 A4 ☒ Quick Setting

D1 A5

D2 A6

D3 A7

D4 A8

D5 A9

D6 A10

D7 A11

Decode ULPI

Color

TURN

TxCMD

TxData

RxCMD

RxData

Range

Decode Range

From To

Buffer Head Buffer Tail

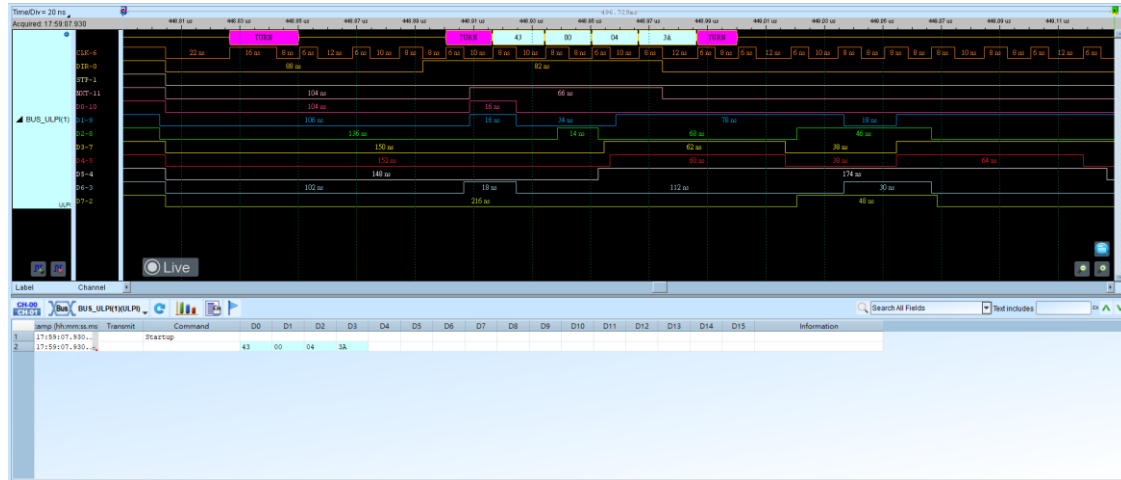
Default OK Cancel

Channel setting: Set the ULPI channel. And you can use Quick Setting to quickly set the data pin.

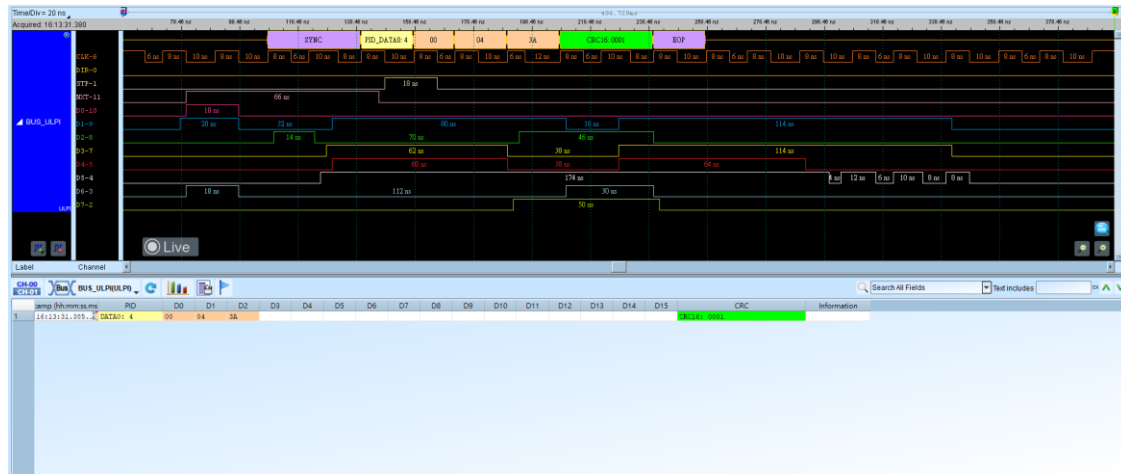
Decode: Set the decoding method of ULPI, optional ULPI / USB (analog timing).

Result

ULPI



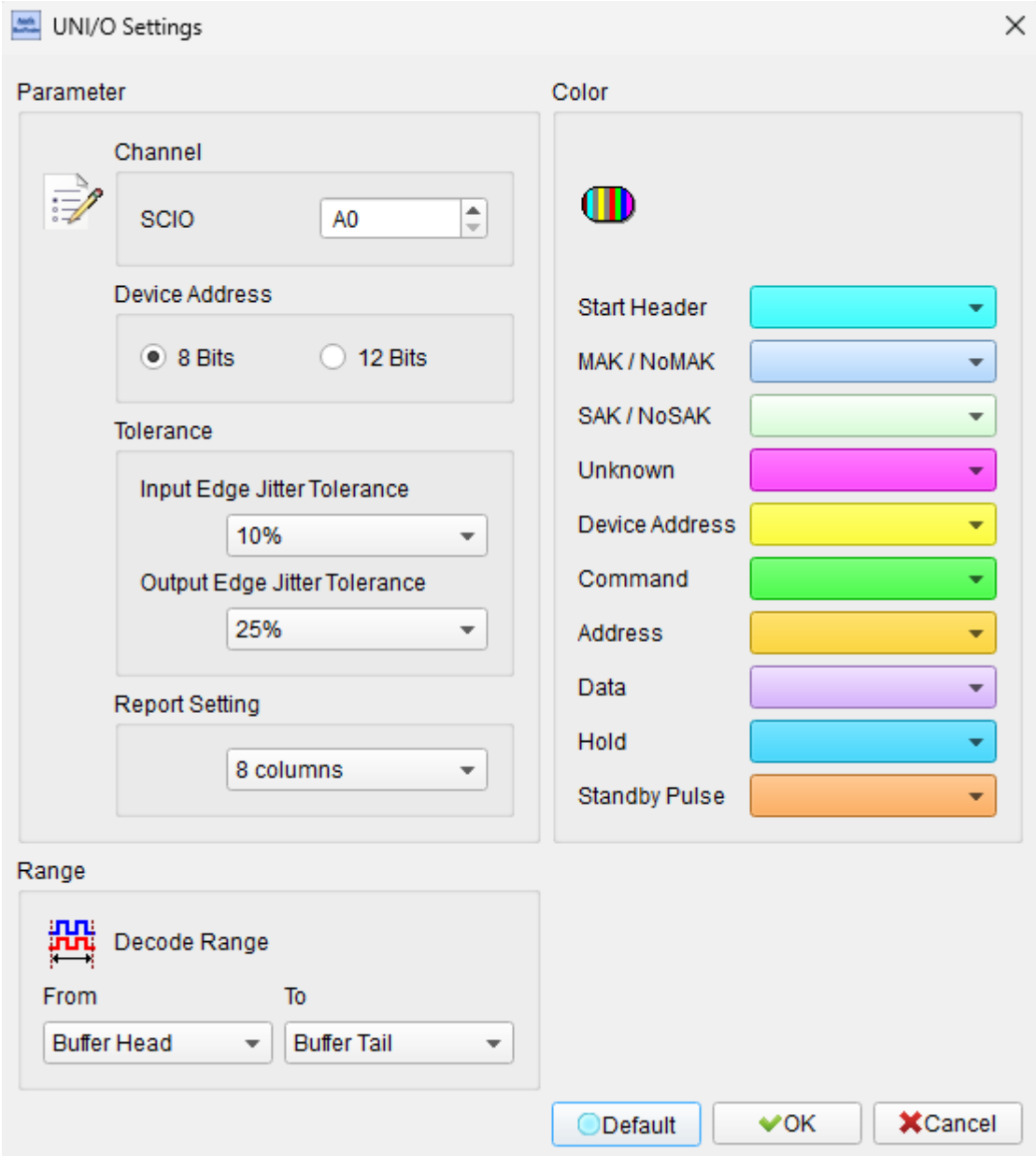
USB



UNI/O

UNI/O is a communication protocol developed by Microchip, primarily used in EEPROM applications. It was designed to meet the growing demand for fewer I/O pins in miniaturized embedded systems, while also providing a low-cost and easy-to-use single-wire bus solution. UNI/O utilizes Manchester Encoding and supports data transmission rates ranging from 10Kbps to 100Kbps

Settings



The image shows a software dialog box titled "UNI/O Settings". It is divided into several sections for configuring the communication protocol.

- Parameter Section:**
 - Channel:** A dropdown menu showing "SCIO" and a text box with "A0".
 - Device Address:** Two radio buttons: "8 Bits" (selected) and "12 Bits".
 - Tolerance:**
 - Input Edge Jitter Tolerance:** A dropdown menu showing "10%".
 - Output Edge Jitter Tolerance:** A dropdown menu showing "25%".
 - Report Setting:** A dropdown menu showing "8 columns".
- Color Section:** A list of color-coded items with corresponding dropdown menus:
 - Start Header (Cyan)
 - MAK / NoMAK (Light Blue)
 - SAK / NoSAK (Light Green)
 - Unknown (Magenta)
 - Device Address (Yellow)
 - Command (Green)
 - Address (Orange)
 - Data (Purple)
 - Hold (Blue)
 - Standby Pulse (Dark Orange)
- Range Section:**
 - Decode Range:** A section with a waveform icon and two dropdown menus: "From" (set to "Buffer Head") and "To" (set to "Buffer Tail").
- Buttons:** At the bottom right, there are three buttons: "Default" (with a blue circle icon), "OK" (with a green checkmark icon), and "Cancel" (with a red X icon).

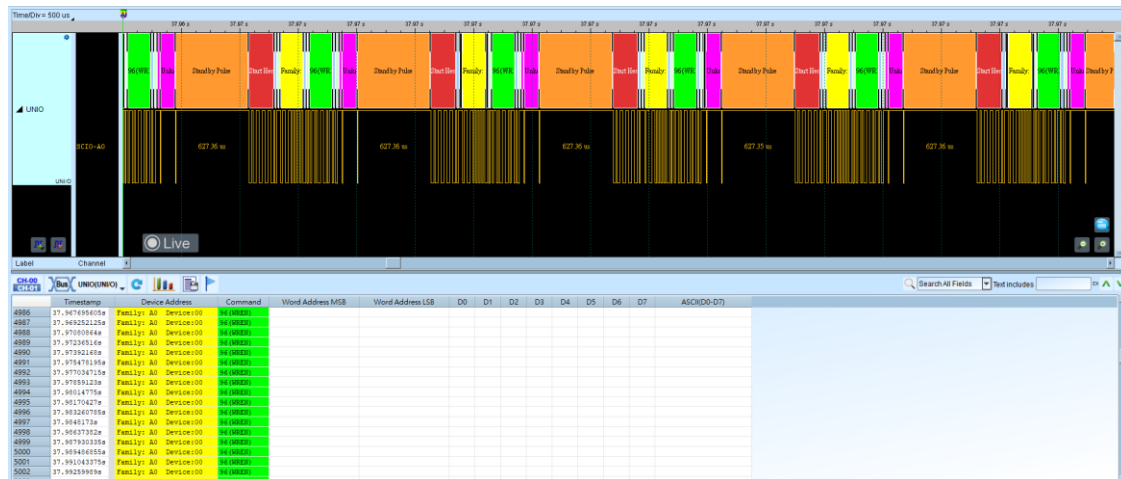
Channel: Show the selected channels (SCIO CH0).

Device Address: Set data bits for the device address.

Tolerance: Set the Input / Output Edge Jitter Tolerance, $\pm 10\%$ / $\pm 25\%$ default.

Report Setting: To show the data by 8 or 16 columns in the Report Window.

Result



USB PD

USB PD (Power Delivery) 2.0/3.0 is the protocol based on BMC (Biphase Mark Coding) and can be applied to Laptops / Tablets / Mobile phones / Power banks or other devices with USB Type-C for power supplying or charging. The maximum power offered by USB Type-C can be 240W, and the users can charge the device by supporting USB Type-C connector, current version is Revision 3.1, Version 1.0.

Settings

USB PD Settings

Channel

Configuration Channel

CC1 A0 CC2 A1

Color

User can assign color for specific pattern.

Preamble SOP/EOP

Header Extended Header

Data Object(s) CRC

☐ VDM

Acute USB PD VDM v1.01
All the number is HEX mode
Format = VDM Header + VDO(s)
Maximum VDM size is 32 (e.g. VDM 1 ~ VDM 32)
Support Header Structured VDM only (SVID / Command Items)
Each Vendor-defined command has a corresponding VDO(s). e.g. 10.DISCOVER_BUTTONS command

Default Reload Edit in text editor

Range

Decode Range

From To

Buffer Head Buffer Tail

Display Settings

☐ Detail Report

☐ Show 5b value in waveform window

Default OK Cancel

Channel: Set Configuration Channel (CC) CC1 & CC2.

VDM: Use the vendor defined message function when checked; users could define the SVID/Command of the Structured VDM by Edit/Refresh.

Content of the configure file as the following:

```
=====
Acute USB PD VDM v1.01
All the number is HEX mode
Format = VDM Header + VDO(s)
Maximum VDM size is 32 (e.g. VDM 1 ~ VDM 32)
Support Header Structured VDM only (SVID / Command Items)
Each Vendor-defined command has a corresponding VDO(s), e.g. 10,DISCOVER_BUTTONS command and VDO 1
=====

##VDM 1
#Header
Bits<31:16>,8087,Intel Vendor-defined message
Bits<4:0>,10,DISCOVER_BUTTONS
#Header
#VDO 1
VDO<23:9>, ,reserved
VDO<8>,1,Sleep button
VDO<7>,1,Eject button
VDO<6:1>, ,reserved
VDO<0>,1,Power chassis button
#VDO 1

#VDO 2
#VDO 2

##VDM 1
=====

##VDM 2
#Header
Bits<31:16>,8087,Intel Vendor-defined message
Bits<4:0>,1C, Vendor-defined command
#Header
#VDO 1
VDO<23:9>, ,reserved
VDO<0>,1, Vendor-defined function ON
#VDO 1
```

VDM (Vendor defined message)

Maximum quantity: 32 (##VDM1 ~ ##VDM32)

The ##XXX at the beginning of each column is a keyword and don't use it at other position in the file. Each VDM is composed of a header and its corresponding VDO (VDM Object), and the header is the first Data Object of VDM; the rest is VDO(s), which is the response message according to the Command.

The header part uses the keyword #Header to include the definition of SVID / Command:

SVID (Standard/Vendor ID):

Bits<31:16>,8087,Intel Vendor-defined message

When the value of Header bit 31 ~ bit 16 is 8087h, the Intel Vendor-defined message is displayed.

Command:

Bits<4:0>,10,DISCOVER_BUTTONS

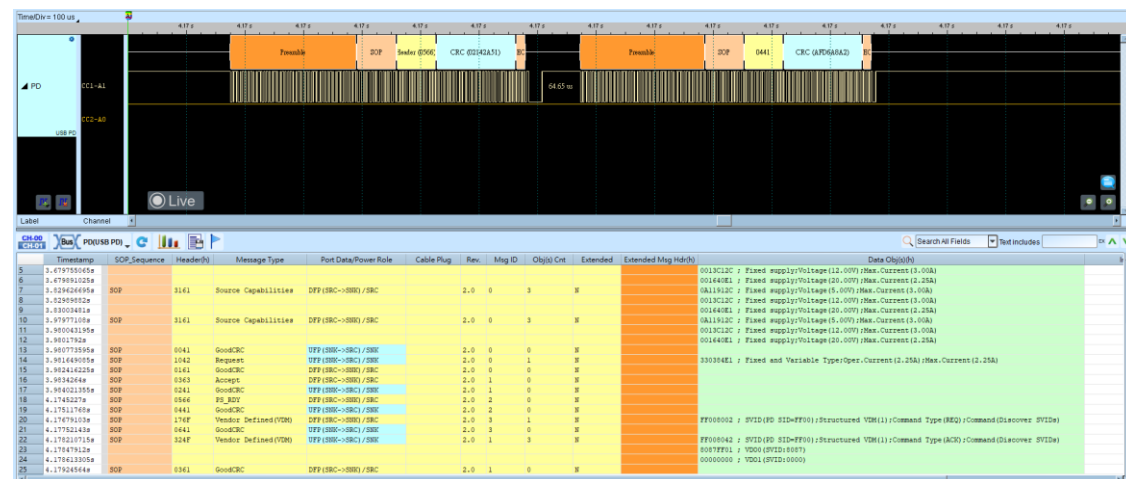
When the value of Header bit 4 ~ bit 0 is 10h, it's command is DISCOVER_BUTTONS.

Show 5b value in waveform window: Show 5b value in the waveform.

Details Report: Show the details of bit parsing for the Data Obj(s) frame.

Show 5b value in waveform window: Show 4b or 5b value in the waveform.

Result



Accessories:

<https://www.acute.com.tw/en/product/detail142>

USB1.1

USB (Universal Serial Bus), known as the "Universal Serial Bus", was initially developed by seven companies: Intel, Microsoft, National Semiconductor, Compaq, Northern Telecom, NEC, and AT&T. The development of USB began in 1994, with version 1.0, followed by version 1.1 in 1998, and later USB 2.0 in 2000. The data transfer speed evolved from 12 Mbps in USB 1.1 to 480 Mbps in USB 2.0.

In the USB protocol, communication between the host and device is primarily established through two differential signal lines, D+ and D-.

Settings

Setting

Channel

D- |A1
D+ A0

USB 1.1 Setting

☒ Auto Detect
☐ Low speed
☐ Full speed

☐ Decode USB standard request & descriptor

Report Setting

Mark PID SOF

Show Data 8 Columns

PID Filter

☐ SOF
☐ DATA1
☐ SETUP
☐ ACK
☐ IN
☐ NACK
☐ OUT
☐ STALL
☐ DATA0
☐ PRE

☐ Show scale in the waveform

Range

Decode Range

From To

Buffer Head Buffer Tail

Color

Sync
Packet ID
Frame No. / Address / Endpoint/ Data
CRC5/CRC16
EOP
Transfer Direction
Type
Recipient
bRequest
wValue
wIndex
wLength
Descriptor

Default OK Cancel

D+: D+ line for USB 1.1 data transmission.

D-: D- line for USB 1.1 data transmission.

USB1.1 Settings: Configure the USB 1.1 signal as Low-Speed or Full-Speed, and determine whether to decode USB standard requests and descriptors.

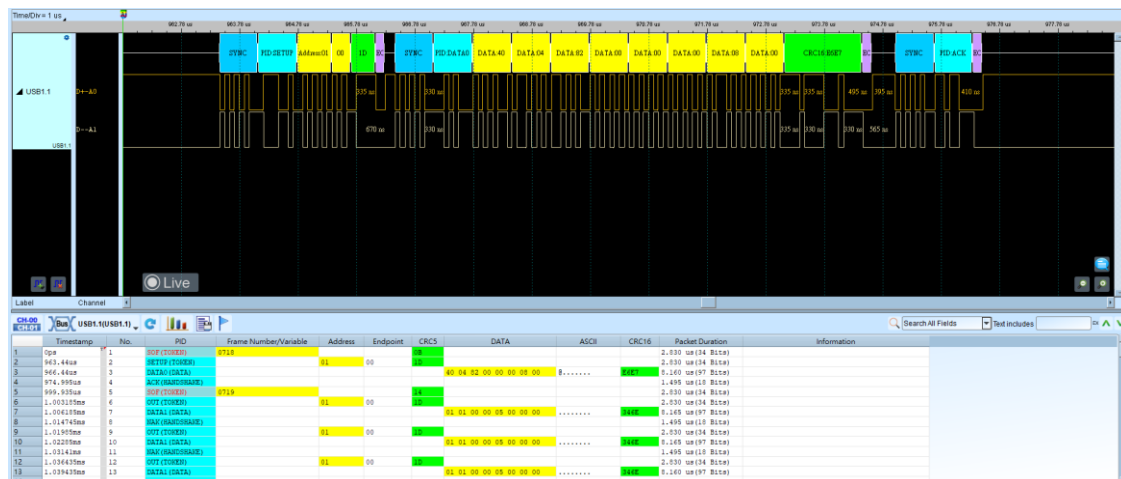
Mark PID: Allows marking selected PID types with specific colors in the report window.

Show Data: Sets the data display in the report window to 8 columns or 16 columns.

PID Filter: Allows hiding specific data from display.

Show Scale in Waveform: Displays scale markings on the waveform.

Result.



USB4/TBT3 SB

USB4 can simultaneously transmit DisplayPort video and PCIE signals through Intel Tunneled technology, and also support PD (Power Delivery) fast charging technology.

USB4 is backward compatible with USB 2.0 and USB 3.2 Gen1/Gen2 and supports Thunderbolt 3/4. The sideband channel (SB) was originally defined as a channel for video protocol communication after entering the Alt-Mode (Alternate Mode) in USB 3.2 (for example: DP Alt-Mode transmits AUX signals through the Sideband channel...etc.). In the USB4 specification, new features of Sideband channel are added to confirm whether the USB4 interface is connected, start and close the channel, initialize the channel, and enter or leave the sleep mode. Thunderbolt Alt-Mode will be enabled when connecting to the device via Thunderbolt 3.

1. Settings:

SBChannel Settings

Settings

Channel

Sideband TX: A0

Sideband RX: A1

Waveform Area

☒ TX

☐ RX

Options

☐ Show Scale

☐ Detail Report

Version

☒ USB4 1.0

☐ USB4 2.0

☐ TBT3

Range

From: Buffer Head

To: Buffer Tail

Color

Data Link Escape (DLE)

Lane State Event (LSE) / ELSE

Complement LSE (CLSE) / ECLSE

Start Transaction (STX) - AT

Start Transaction (STX) - RT

Data Symbols / Link Parameters

LCRC / HCRC

End of Transaction (ETX) Symbol

No Meaning Byte

Default Cancel OK

a. Channel:

Sideband TX: Show the selected channel.

Sideband RX: It is checked by default, and the dual-channel analysis mode can be enabled by checking Sideband RX.

Data Convert: TX is checked by default, and the TX/RX channel can be selected for analysis in the data convert field.

Show on Report: TX and RX is checked by default. Choose which channel to display in the report area, and both channels can be displayed at the same time.

b. Others:

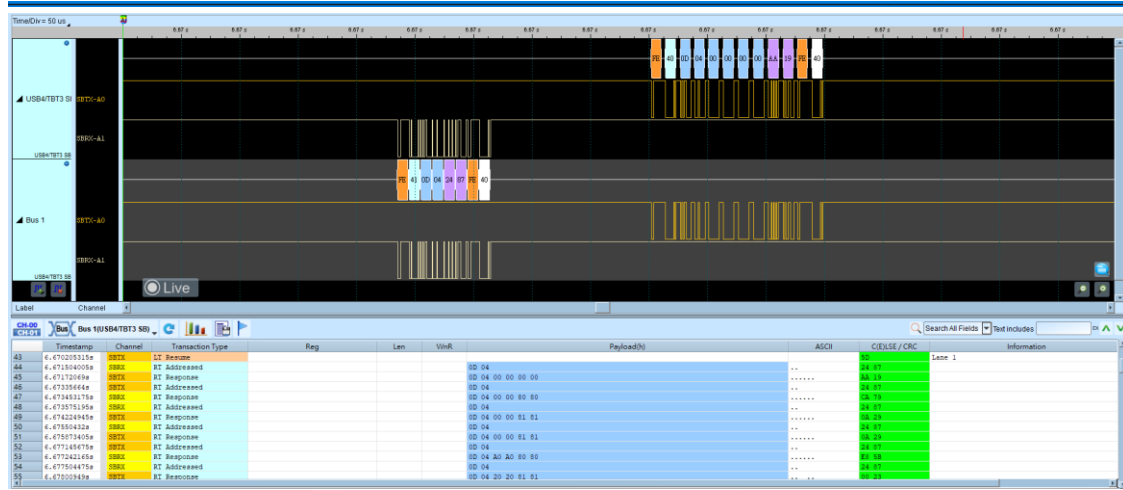
Version: USB4 2.0 is checked by default, and different versions can be selected for USB4/TBT3 SB signal analysis.

Show scale on data convert: The default is off. Show the scale on data convert field.

Show data detail on report: The default is off. If checked, additional data information will show on report as shown below.

Channel	Transaction Type	Reg	Len	WnR	Data Symbols / Link Parameters payload(H)
SBTX	RT Addressed	vendor specific (15h)	35	Read	
SBRX	AT Command	Link Configuration(0Ch)	3	Read	
SBTX	AT Response	Link Configuration(0Ch)	3	Read	03 F3 03
					Byte0 [0]Enabling Decision (Lane 0): 1
					[1]Enabling Decision (Lane 1): 1
					[2]Asymmetric Decision (Tx): 0
					[3]Asymmetric Decision (Rx): 0
					Byte1 [0]Enabling Request (Lane 0): 1
					[1]Enabling Request (Lane 1): 1
					[4]Bonding Support: 1
					[5]Gen 3 Support: 1
					[6]RS-FEC Request (Gen 2): 1
					[7]RS-FEC Request (Gen 3): 1
					Byte2 [0]USB4 Sideband Channel Support: 1
					[1]TBT3-Compatible Speeds Support: 1
					[2]Gen 4 Support: 0
					[3]Asymmetric Support 3 Tx: 0
					[4]Asymmetric Support 3 Rx: 0
					[5]Request Asymmetric Tx: 0

2. Result:



Wiegand

It is commonly used to connect a card swipe mechanism to the rest of an electronic entry system.

Settings

Wiegand Settings

Channel

Data 0

A0

Data 1

A1

Color

Data

Parity

Range

Decode Range

From

To

Buffer Head

Buffer Tail

Default

OK

Cancel

Data 0: Wiegand data 0 ◦

Data 1: Wiegand data 1 ◦

Result

The screenshot displays the Acute software interface. The top section shows a waveform for 'Bus 1' (Wiegand) with a time scale of 10 ns. The waveform shows a series of pulses corresponding to the data bits. Below the waveform, a table lists the captured data points.

Timestamp	D0	D1	D2	D3	D4	D5	D6	D7	Even parity	Odd parity	Information
1. 0.0000000	04	95	04	95					11: OK	01: OK	
2. 204.522302aa	04	95	04	95					11: OK	01: OK	
3. 13.7405962da	04	95	04	95					11: OK	01: OK	
4. 9122404659											End of capture

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Chapter 2 Bus Trigger

Bus Trigger

Introduction of trigger

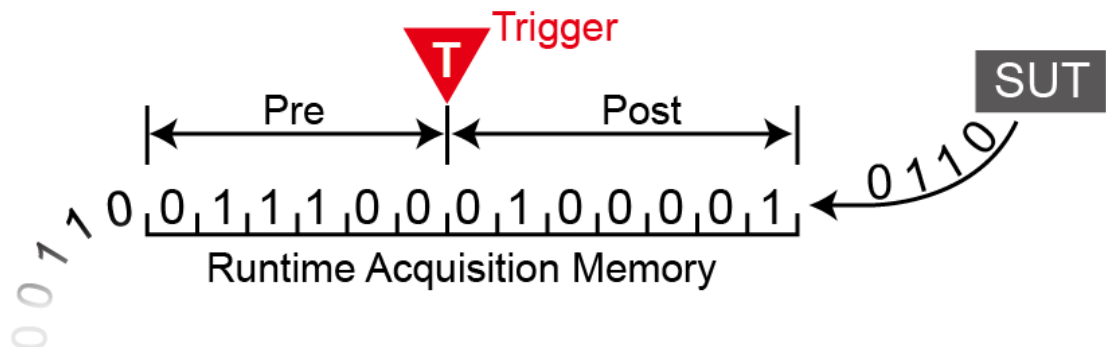
Trigger function is to utilize the logic analyzer's hardware circuitry to check whether the signal to be tested meets the trigger conditions within a limited period of time by using parallel processing techniques, and then carry out the signal acquisition work. Ideal logic analyzer trigger function, in addition to the basic must be accurate, but also as much as possible can be varied. The hardware of logic analyzer takes the signal acquisition function and then performs the signal acquisition work.

The hardware of logic analyzer take the parallel processing technology to check the signal.

Trigger Mode

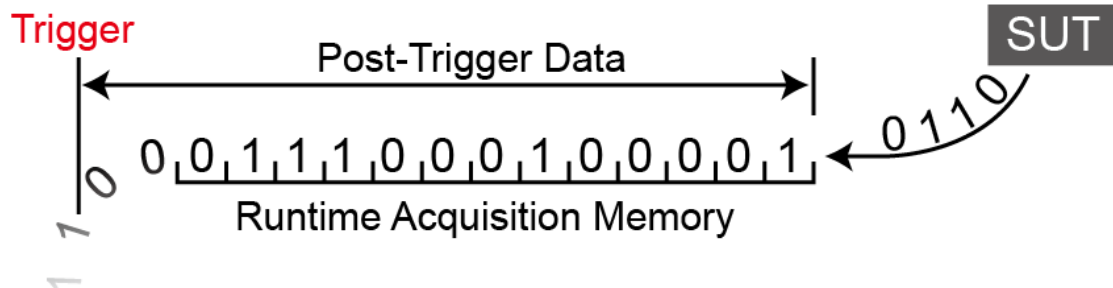
1. Pre-Trigger

In certain applications, when the user wants to capture signals before the trigger point, the Pre-Trigger function must be enabled. After pressing the 'Start Capture' button, the logic analyzer will wait until the data fills the memory from the beginning of the buffer to the trigger cursor before allowing the trigger circuit to start operating (it starts operating, not issuing the trigger signal). Therefore, before the logic analyzer has filled the data between the buffer and the trigger cursor, any signal that meets the trigger condition will not cause the trigger circuit to issue a trigger signal.



2. Post-Trigger

This is the most basic triggering method. After pressing the 'Start Capture' button, the logic analyzer will wait for the trigger to occur and then start capturing data from the position specified by the trigger cursor. Once the memory is fully filled with data, the capture will stop.



3. Delay-Trigger

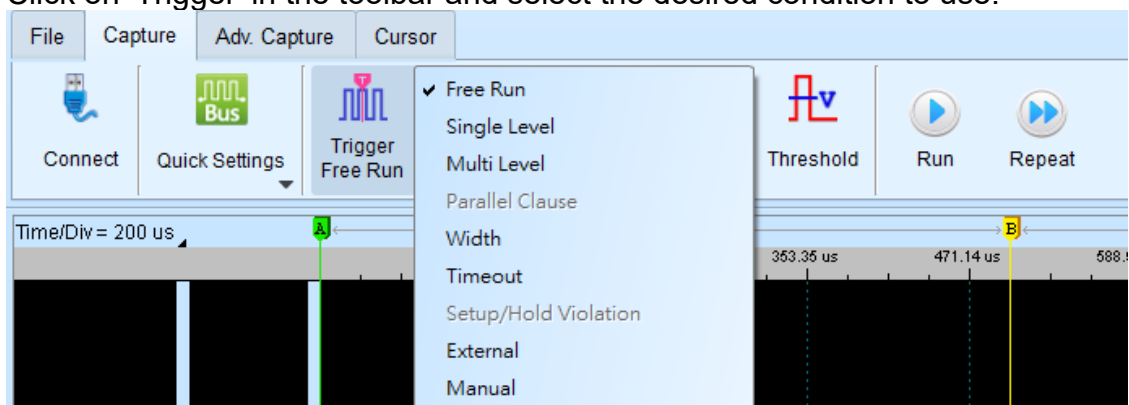
In certain applications, when the user wants to capture signals after the trigger point and with a delay, the trigger delay function can be used to set the desired delay time. After the signal capture is successful, the trigger cursor will stop at the position where the data capture started.

4. Pass Count

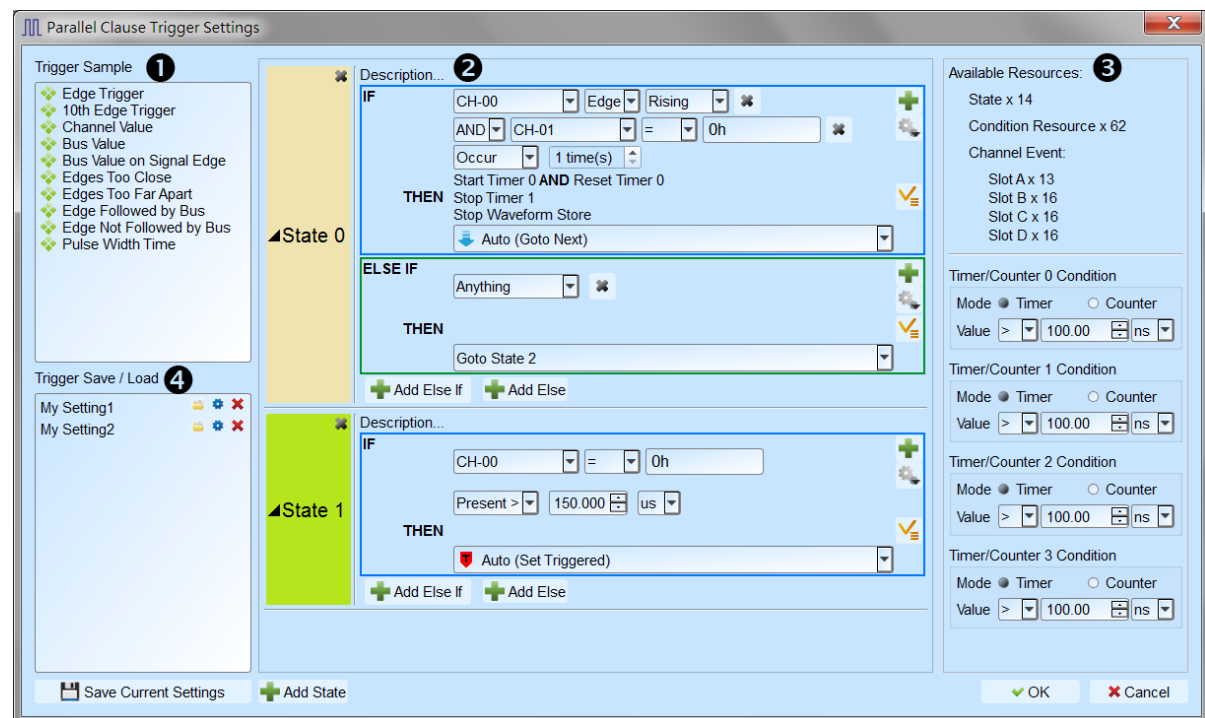
Pass Count represents the number of times the set trigger parameters should be ignored. Under normal conditions, Pass Count is set to 0, which means data capture will start as soon as the trigger parameters are met. If set to N times, it means the trigger parameters must be met N+1 times before data capture begins. The maximum value of Pass Count will be automatically adjusted based on the specific model.

5. Choose to Trigger

Click on 'Trigger' in the toolbar and select the desired condition to use.

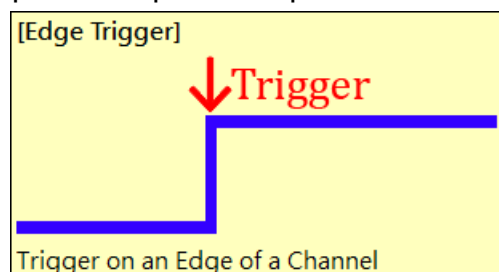


Parallel Clause Trigger



Parallel Clause Trigger feature provides 16 States, 64 Condition Resources and 4 Timer/Counter conditions(1) to help user locate the target waveform, it is also available to set State branch control flow for each IF Clause and decide whether to store waveform or not.

1. Trigger Sample: Provides several Trigger Samples for user's reference, users may also combine multiple trigger samples together for more complex trigger condition. Holding mouse cursor on each Sample for a while will pop up the sample description with schematic picture.



2. Trigger condition settings:


The screenshot displays the Acute software's trigger condition configuration window. It features a sidebar on the left with buttons for 'State 0' (yellow) and 'State 1' (green). The main area is divided into two sections, one for each state. Each section has a 'Description...' field (labeled 2) and a logic editor. The logic editor for State 0 (labeled 1) includes an 'IF' clause (labeled 3) with conditions on CH-00 (Edge, Rising) and CH-01 (=, 0h), and a 'THEN' clause (labeled 4) with actions like 'Start Timer 0 AND Reset Timer 0'. The logic editor for State 1 includes an 'IF' clause with a condition on CH-00 (=, 0h) and a 'THEN' clause with the action 'Auto (Set Triggered)'. At the bottom, there is an 'Add State' button (labeled 6) and 'Add Else If'/'Add Else' buttons (labeled 5).


- ① State button: Click to switch between Text Read Only mode and Edit mode.
- ② State description: Click to edit a short user description for the State, maximum input text length is 80 characters.
- ③ IF Clause: Setup trigger conditions for Label selected in waveform area, and it is also available to setup AND/OR logic combination for multiple IF conditions.
 - i. Channel Logic/Edge/Pattern compare: Specify value or edge condition for each channel label, it is also available to input X as don't care value for the comparison. Input value ended with h for hexadecimal value; input value ended with b for binary value; input value not ended with b or h for decimal value.


Bus_[A7:A0]	=	ABh	✕
AND	Bus_[A7:A0]	=	10101011b
AND	Bus_[A7:A0]	=	171
AND	Bus_[A7:A0]	=	XBh
AND	Bus_[A7:A0]	=	AXh


- ii. Timer/Counter condition check: Check Timer/Counter conditions, condition will be set as True if the Timer/Counter value is matched, otherwise the condition is be set as False.
- iii. Occur and Present time check: Additional Occur times check or Present time check when the all conditions are set to True in the IF Clause.

iv. Control buttons

 Add new condition: Click to add new AND/OR IF condition, the new IF condition will consume 1 Condition Resource.

 Advanced control button, including:

 Get Value From: Set IF condition value by all Label value from selected Cursor position in the waveform area.

 Copy: Copy all IF conditions of current IF Clause.

 Paste: Paste the copied IF conditions into current IF Clause.

- ④ THEN Branch: Select the Branch or Trigger control flow when the IF Clause is matched (2). When select Auto, the Branch or Trigger control will be determined by current State order in the setting, the Action will be set as Trigger if current State is the last State in the setting; the Action will be set as Goto Next State if current State is NOT the last State in the setting.

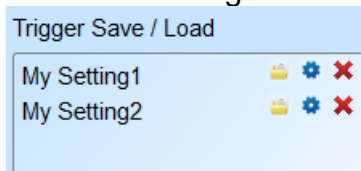
THEN	
	Auto (Set Triggered)
Add Else	Auto (Set Triggered)
	Goto Next
	Set Triggered
	Goto State 0
	Goto State 1
	Goto State 2
	Goto State 3
	Goto State 4
	Goto State 5
	Goto State 6

✓ Additional Then action: Setup Timer/Counter Start/Stop/Reset actions or Waveform Store Suspend/Resume for each IF Clause when condition matched.

- ⑤ Add new ELSE IF / ELSE Clause: Click to add new ELSE IF / ELSE Clause, each clause condition will be checked from top to bottom, and perform the specified Action and Branch if the clause condition is matched. New clause conditions will consume Condition Resources. ELSE Clause condition will be set as “Anything” and Branch to current State by default if the user didn’t assign ELSE Clause.
- ⑥ Add new State: Click to add new State Clause, the new State Clause will consume both State and Condition Resources.

3. Available Resources and Timer/Counter settings: Display remain available resource number and Timer/Counter settings.
Timer / Counter: Parallel Clause trigger provides 4 independent Timer/Counter resources, each resource could be selected to work in Timer or Counter mode. The minimum Timer interval is 12 Sample clock intervals (i.e. 60ns when working in 200MHz sampling mode), and the maximum Timer interval is 0x3FFFFFFF (i.e. 5s when working in 200MHz sampling mode). The minimum Counter value is 1, and the maximum Counter value is 0x3FFFFFFF.

4. Trigger Save/Load: Users may save their current trigger settings with maximum 20 characters description, or load previous saved trigger settings from the list, the saved settings will be stored into Working Directory with file name PClauseUserSetting.aqr. Copy and share the .aqr file in order to share the settings to other user.



📁 Load selected Trigger settings, it's also available to select 🔄 to overwrite current Trigger settings, or select + to append the selected settings to the end of current Trigger settings.

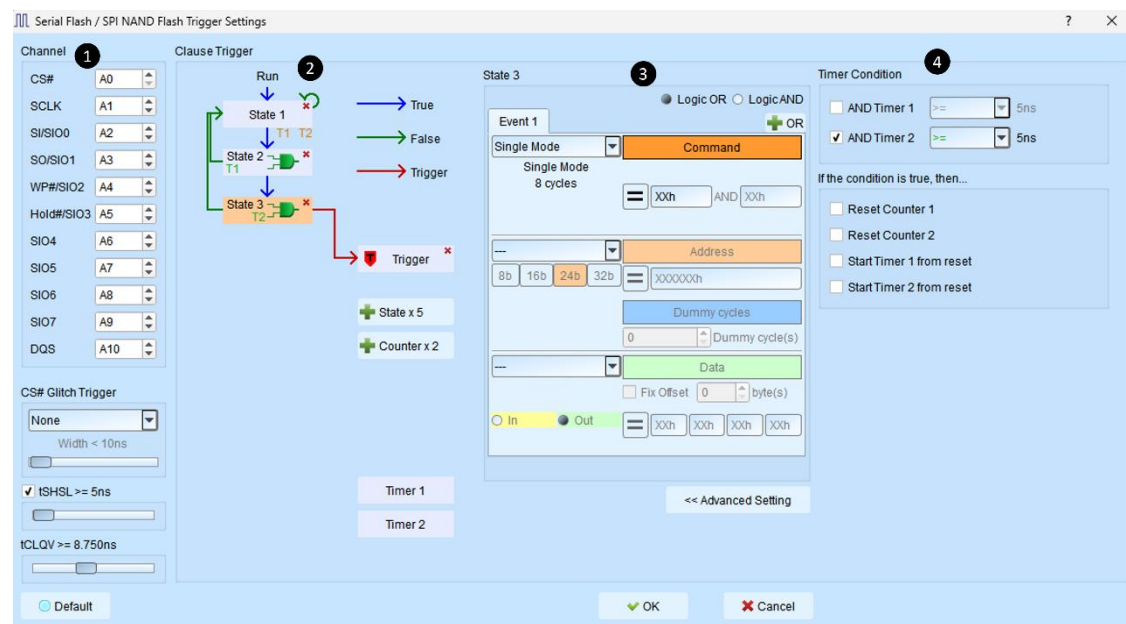
⚙️ Edit the display name for the selected Trigger settings.

❌ Delete the selected Trigger settings.

- (1) Timer / Counter features are provided in 300MHz, 250MHz, 200MHz and below sampling rate mode only.
- (2) If these not valid trigger setting, system will be hold and the status bar will display “Wait for Trigger”, and must press Stop Capture manually in order to retrieve the waveform.

Clause Trigger

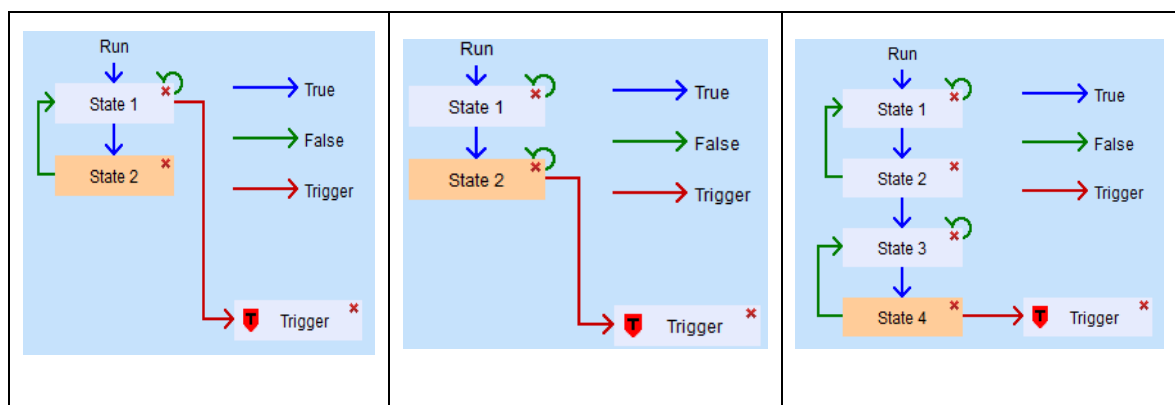
The Clause trigger settings dialog box is as below.

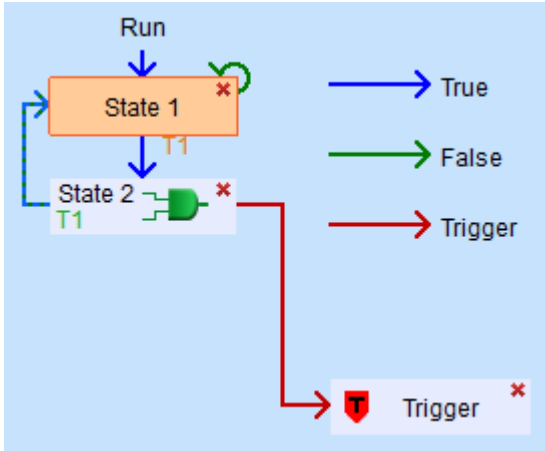
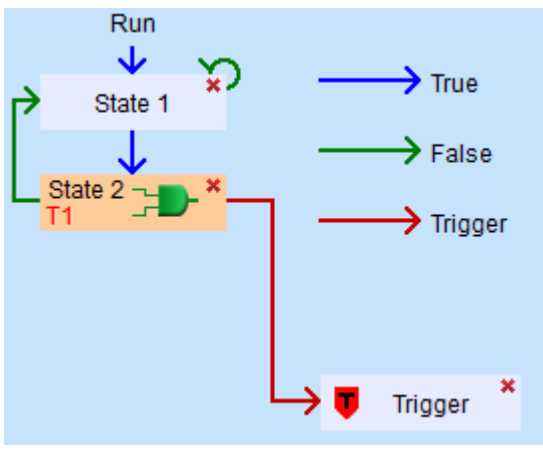


1. Channel and bus trigger settings:

Please refer to the descriptions in each bus trigger settings section.

2. Flow chart





State 1 next State 2	State 1 then State 2	State 1 next State 2 then State 3 next State 4
		
State 1 (Active T1) next State 2 (Time \geq T1)	State 1 (Active T1) next State 2 (Time $<$ T1)	

A state button represents a trigger state. The true state condition will only lead the branch to the next state, on the other hand, the false state condition could lead the branch to any state as below:

Click state 1 and state 2, then state 1 will branch to state 2 while state 1 is false.



Double click any state, the state will branch to itself if it is false.

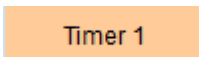
Click the state button and trigger button ( Trigger ): trigger when the state conditions is satisfied.

Delete any state by clicking the cross sign on the state.

Clear the links to the trigger button by clicking on the trigger button

( Trigger )

Click  State x 6 and  Counter x 2 to add a new state.


 Timer 1 : The timer ranges from 5 ns to 8 days.



3. State settings

This area displays the detailed trigger conditions for each level in the triggering process on the left:

The State 1 text in the upper left indicates the currently displayed state number.

☒ Logic OR ☐ LogicAND User can set the logic operation rules between events.




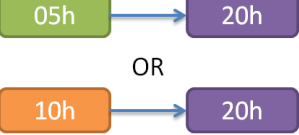
Event 1 ✖ Event 2 ✖ Event 3 ✖  OR User can switch/view the number of combinations of OR/AND conditions currently in this hierarchy.

Choose  OR /  AND tab to add up to 8 OR/AND triggers.

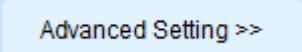
The center parameter setting area varies according to the selected trigger type.

The input values support 2 /10/16 progress, binary code (followed by b, such as 01000001b), decimal code (followed by no b, such as 65), hexadecimal code (followed by h, such as 41h).

The relationship between events and triggering signals within each level can be seen in the following table:

	AND	OR
Event settings		
Trigger condition		

4. Timer and Counter settings

Press  button to edit the timer/counter reset settings of the state.

Timer Condition

☒ AND Timer 1 < 5ns

☒ AND Timer 2 >= 5ns

If the condition is true, then...

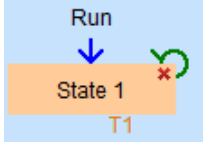
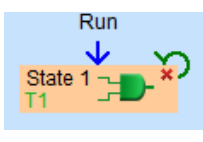
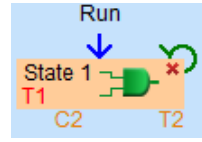
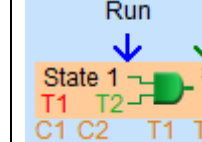
☒ Reset Counter 1

☒ Reset Counter 2

☒ Start Timer 1 from reset

☒ Start Timer 2 from reset

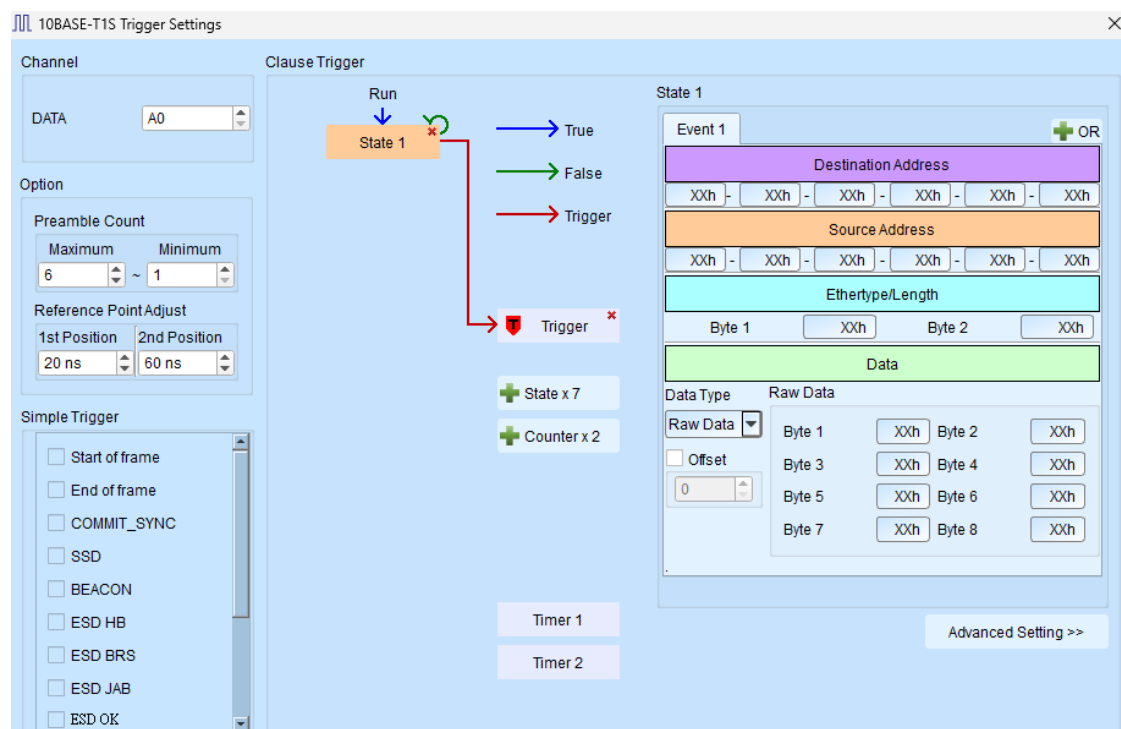
The following table describes the state button icons:

				
Conditions	State 1	State 1 And timer > T1	State 1 And timer < T1	State 1 And T2 < timer < T1
satisfied condition	Start T1	X	Start T2 Reset C2	Start T1 and T2 Reset C1 and C2

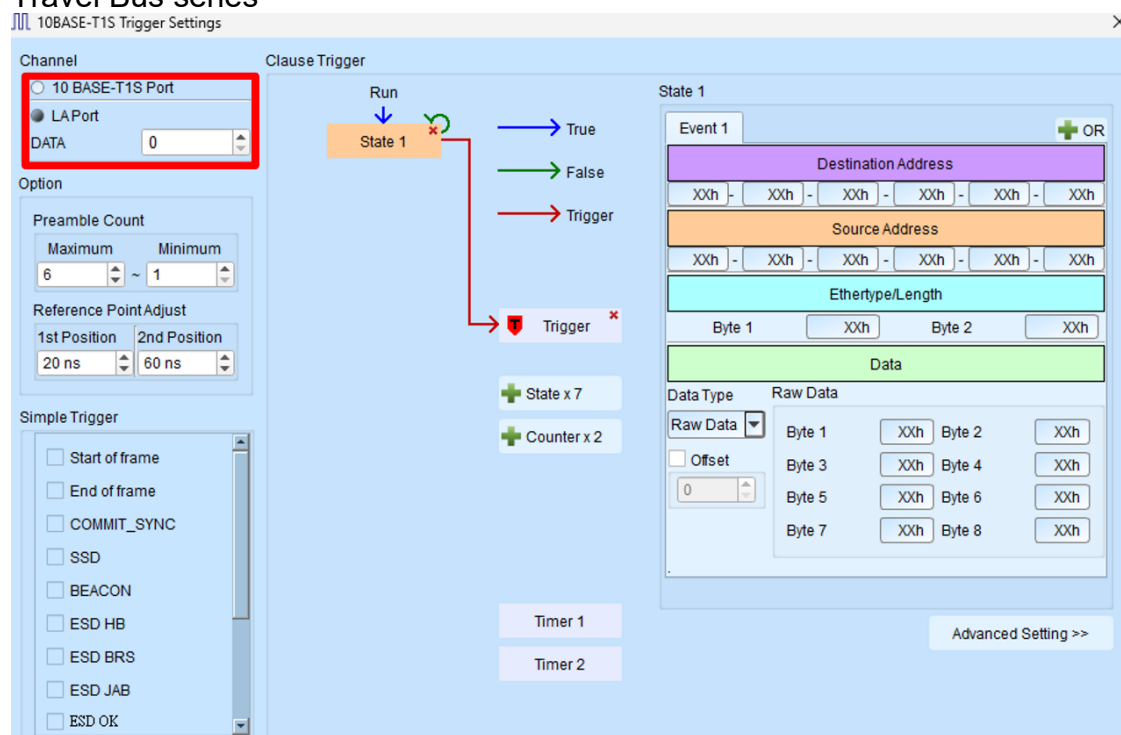
10BASE-T1S Trigger

Trigger Parameter Settings

Click on the "10BASE-T1S Trigger Settings" in the toolbar, and the following window will appear.



Travel Bus series



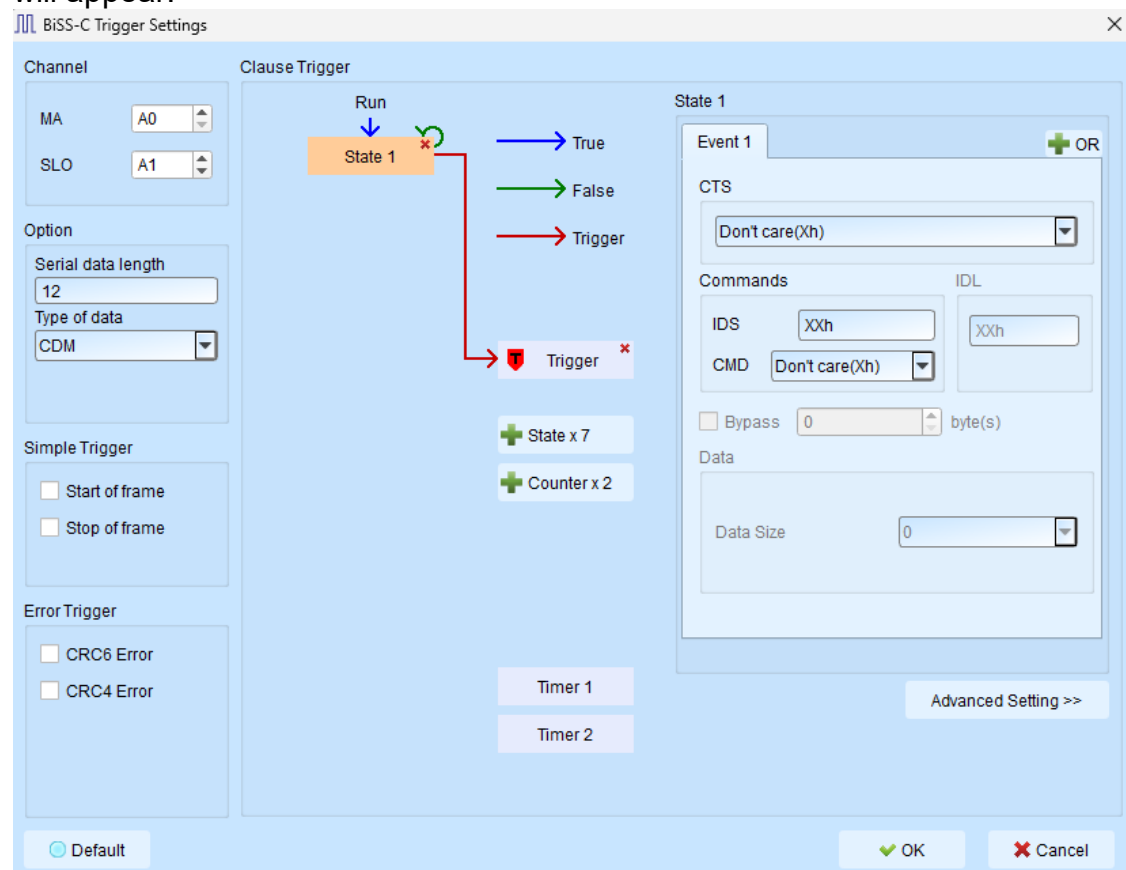
Since TravelBus has specially designed channels for 10BASE-T1, the 10BASE-T1S trigger settings in the TravelBus software will include additional channel source options.

1. **Channel:** Configure the Data channel.
2. **Option**
 - Preamble Count:** Set the number of Preamble bits.
 - Reference Point Adjust:** Adjusts the reference point for logic level determination.
3. **Simple Trigger:** Configure the trigger packet.
4. **Clause Trigger:** Please refer to the Parallel Clause Trigger description for details.
5. **State:** This section displays the detailed trigger conditions within each level of the trigger process on the left. Users can specify values for Destination Address, Source Address, Ethertype/Length, or Data, or leave 'X' as a wildcard for any value.

BiSS-C Trigger

BiSS-C Trigger Parameter Settings

Click on the " BiSS-C Trigger Settings" in the toolbar, and the following window will appear.



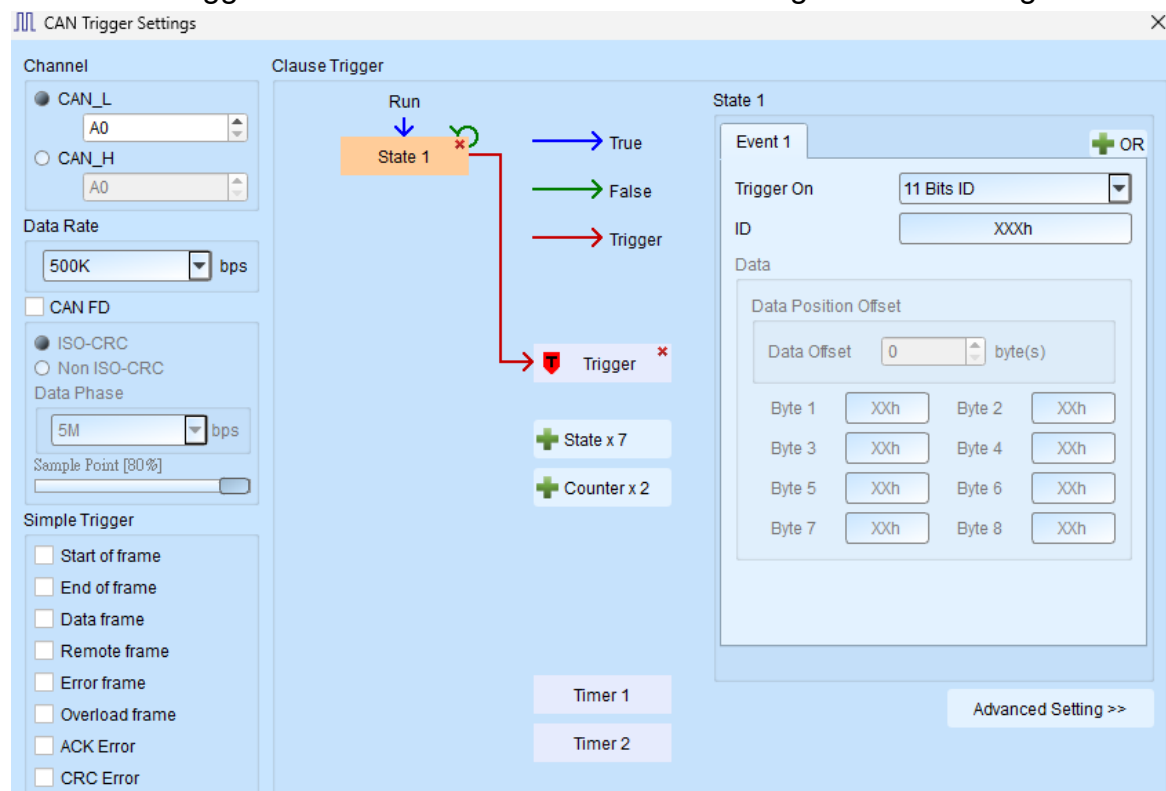
1. **Channel:** Select channels.
2. **Option:**
 - I. Serial data length: Set SCD packet length, the default is 12 bits, 255 bits is the maximum.
 - II. Type of data: Select the CDM or CDS packet.
3. **Simple Trigger:** Specific trigger function of BiSS-C.
4. **Error Trigger:**

CRC6 Error/CRC4 Error: Trigger CRC6 or CRC4 error of BiSS-C.
5. **Clause Trigger:** Please reference Clause Trigger chapter.
6. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the CTS, Commands, IDL and Data fields, default value is XX means "don't care".

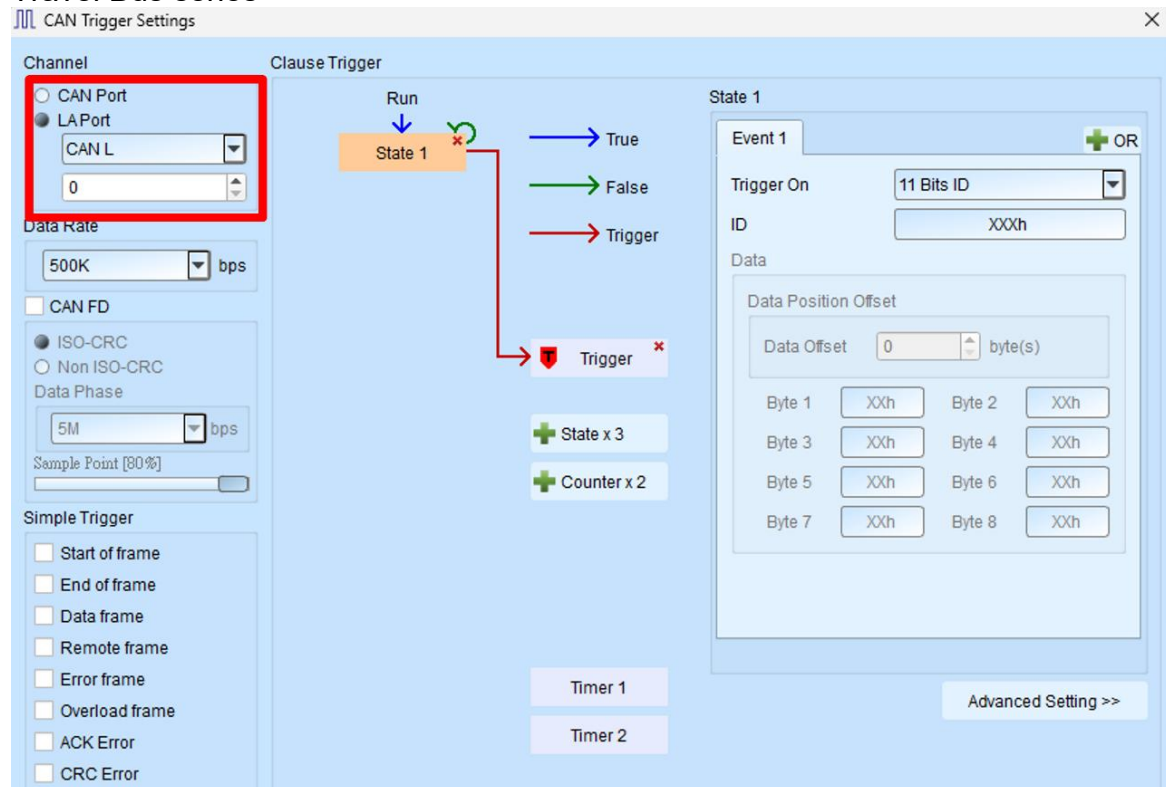
CAN Trigger

CAN Trigger Settings

Click CAN Trigger in the toolbar and will show the dialog as the following °



Travel Bus series



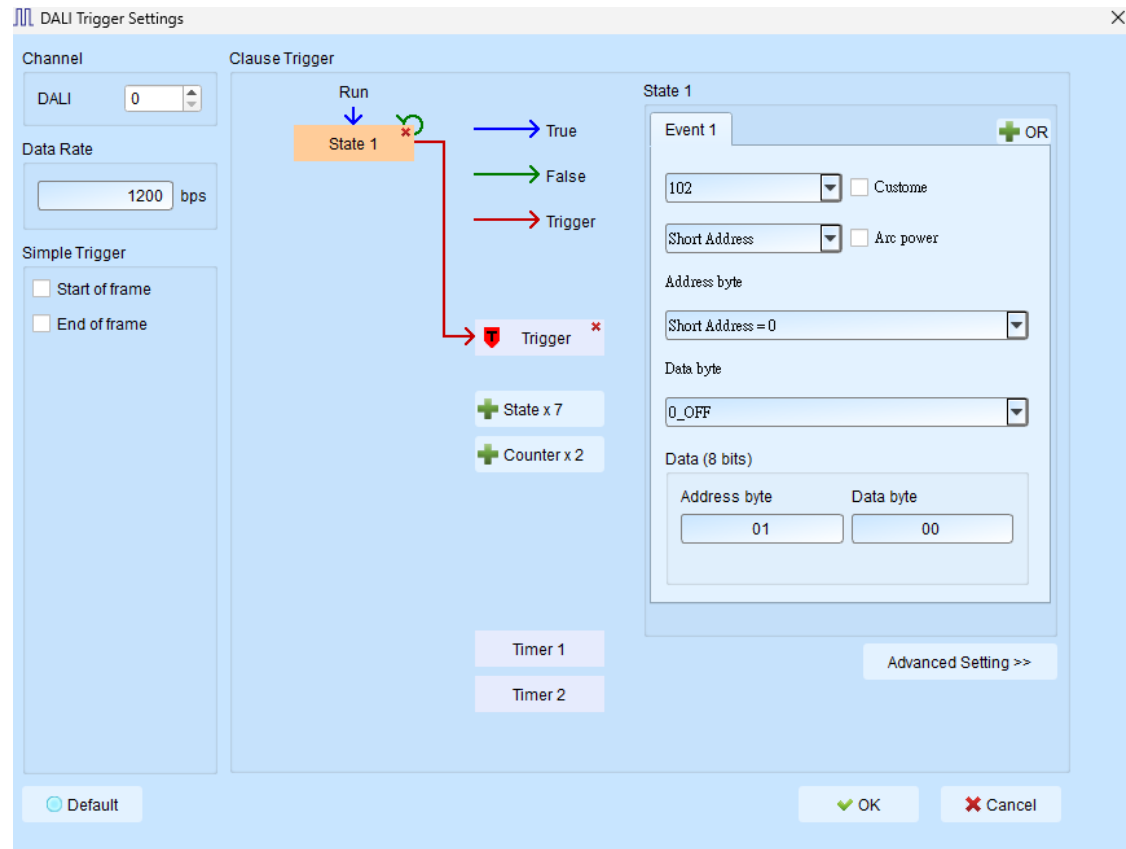
Since TravelBus has specially designed channels for CAN, the CAN trigger settings in the TravelBus software will include additional channel source options.

- 1. Channel:** Configure the CAN interface (supported only on TravelBus B series models) or set to LA channels.
- 2. Data Rate:** CAN data rate. Users could type the data rate if no data rate is available.
- 3. Simple Trigger:** Specific trigger function of CAN.
- 4. Clause Trigger:** Please reference Clause Trigger chapter.
- 5. State:** Show the details of trigger condition in every state as left side; there are 11 Bits ID, 29 Bits ID, Data, 11 Bits ID + Data and 29 Bits ID + Data selections in the Trigger On; selecting one of them and typing the trigger values in the ID or Data fields, default value is XX means “don’t care”.

DALI2 Trigger

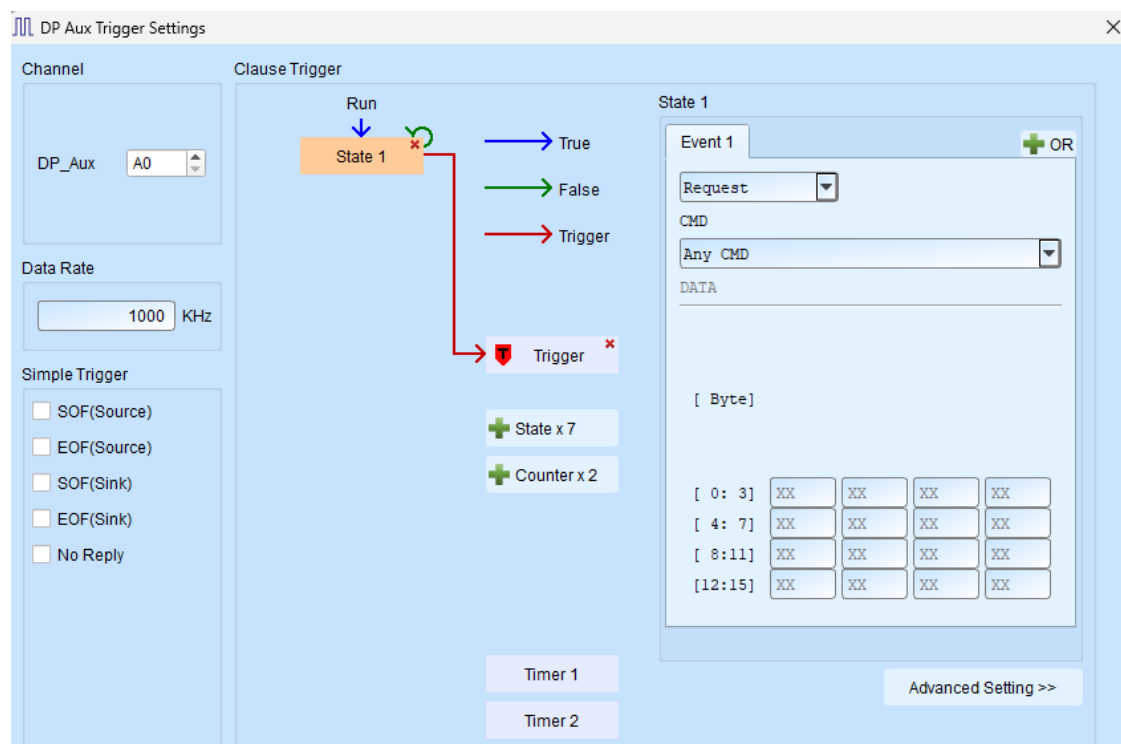
DALI Trigger Settings

Click DALI Trigger in the toolbar and will show the dialog as the following.

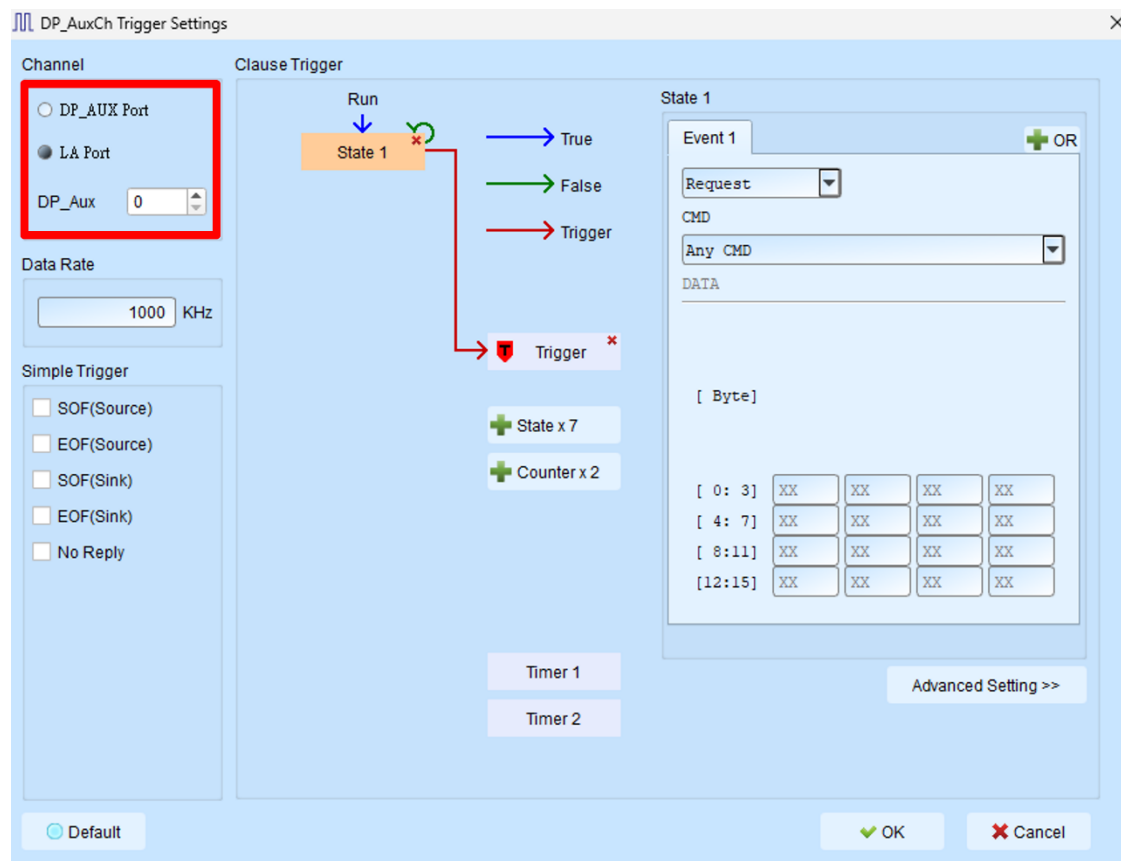


1. **Channel:** Select channels.
2. **Simple Trigger:** Trigger specific of DALI.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side;
selecting the trigger type of DALI (102, 103), command type (short address, group address, broadcast, response, special command), or custom cmd.

DPAux Ch Trigger



Travel Bus series



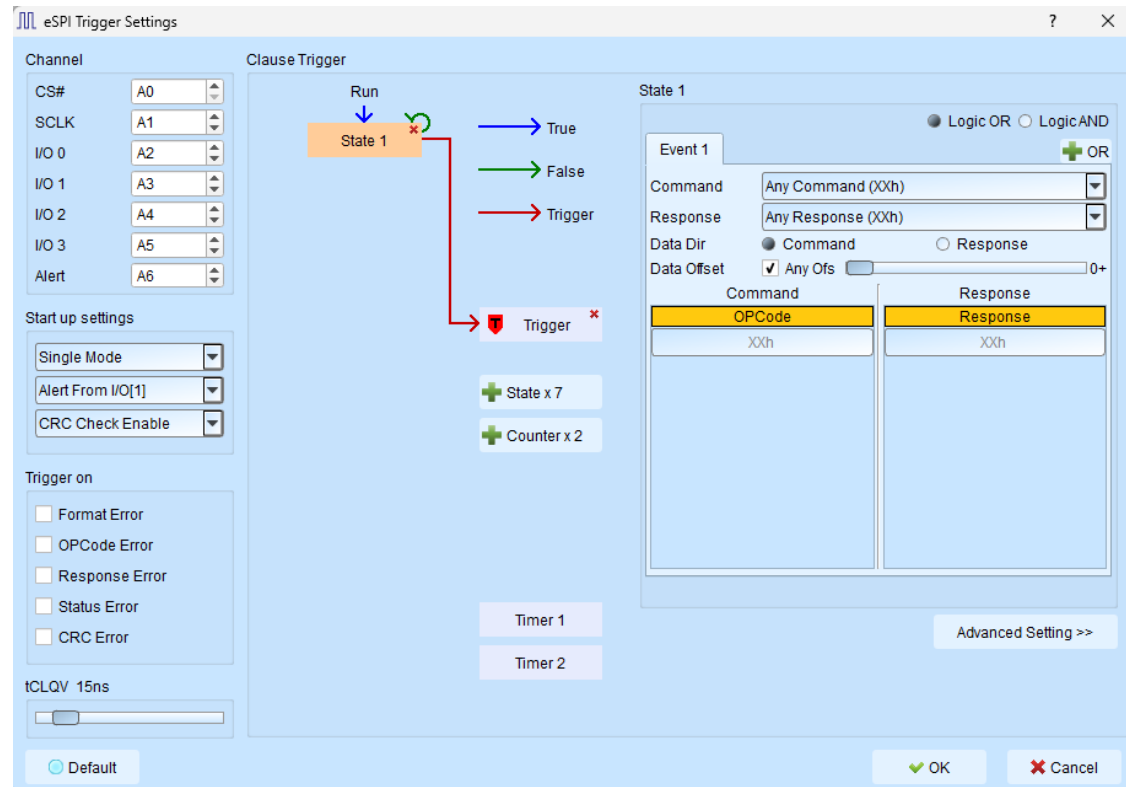
Since TravelBus has specially designed channels for DP Aux, the DP Aux trigger settings in the TravelBus software will include additional channel source options.

1. **Channel:** Configure the DP Aux channel
2. **Data Rate: Configure the DP Aux data rate**
3. **Simple Trigger:** Triggers on common basic packets. Enabled when selected.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** This section displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the packet as Request or Reply, fine-tune Command settings, or specify trigger values for the Data packet content. Alternatively, 'X' can be used as a wildcard to represent any value.

eSPI Trigger

eSPI Trigger Settings

Click eSPI Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Startup settings:** Set the initial parameters of eSPI.
3. **Trigger on:** Trigger specific error of eSPI.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Response fields, default value is 00h.
 - I. **Data Dir:** Trigger the data in the Command or Response.

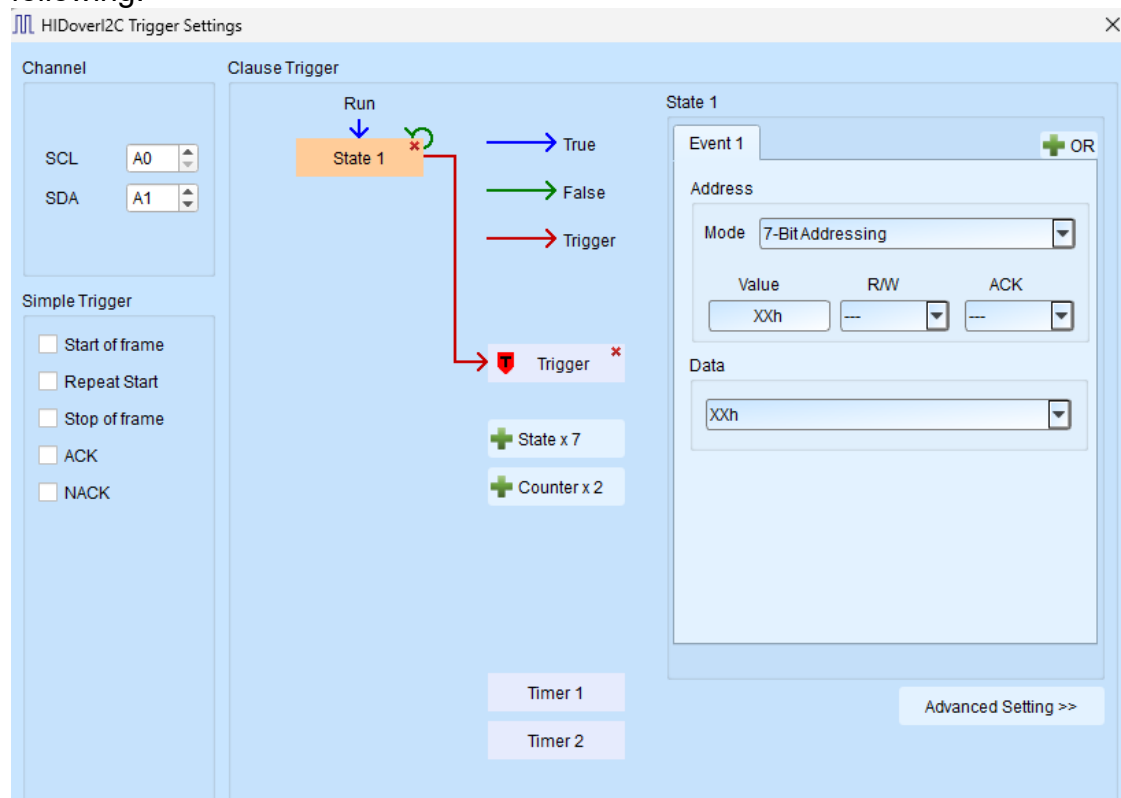
Timestamp	OpCode/Response	CycType	Tag	LEN	Address	D0	D1	D2	D3	D4	D5	D6	D7	ASCII	Status	CRC	Memo
0.00000245 S	SET_CONFIGURATION(21)				0010											33	
0.00000086 S	ACCEPT(08)					13	11	00	00					030F	95	
0.000003 S	SET_CONFIGURATION(22)				0010	01	11	00	00							75	
0.000005935 S	ACCEPT(08)														030F	90	
0.000008455 S	SET_STATUS(25)														030F	70	
0.000009365 S	ACCEPT(08)														030F	90	
0.001601195 S	SET_CONFIGURATION(21)				0010											55	
0.001602795 S	ACCEPT(08)					13	11	00	00					030F	95	
0.001604635 S	SET_CONFIGURATION(22)				0010	01	11	00	00						75	
0.001609575 S	ACCEPT(08)														030F	90	

- II. **Data Offset:** Trigger the data from start of data frame without any offset. For example, setting D0 13h will check the first byte of data frame. With any offset, the signal would be triggered by the byte pattern. For instance, setting D0+ XXh D1+ 11h, and the byte pattern of XXh and 11h will be triggered regardless of the position of the data.

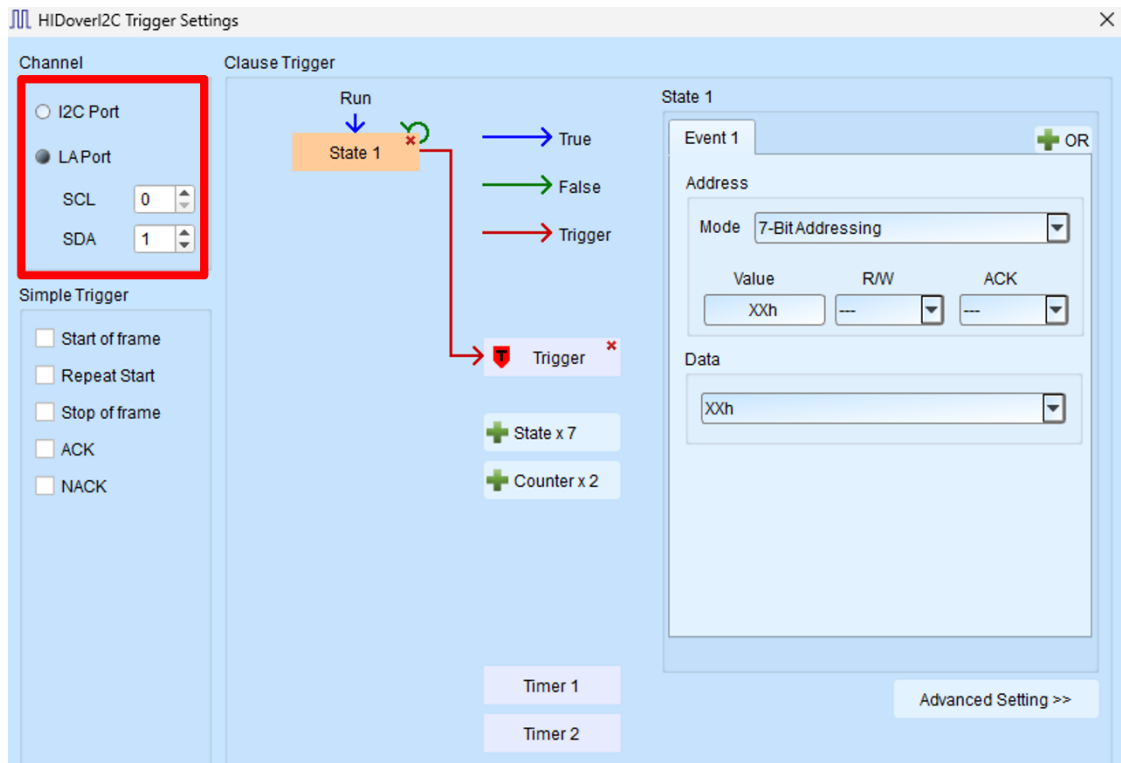
HIDoverI2C Trigger

HIDoverI2C Trigger Settings

Click HIDoverI2C Trigger in the toolbar and will show the dialog as the following.



Travel Bus series



Since TravelBus has specially designed channels for I2C, the HID Over I2C settings in the TravelBus software will include additional channel source options.

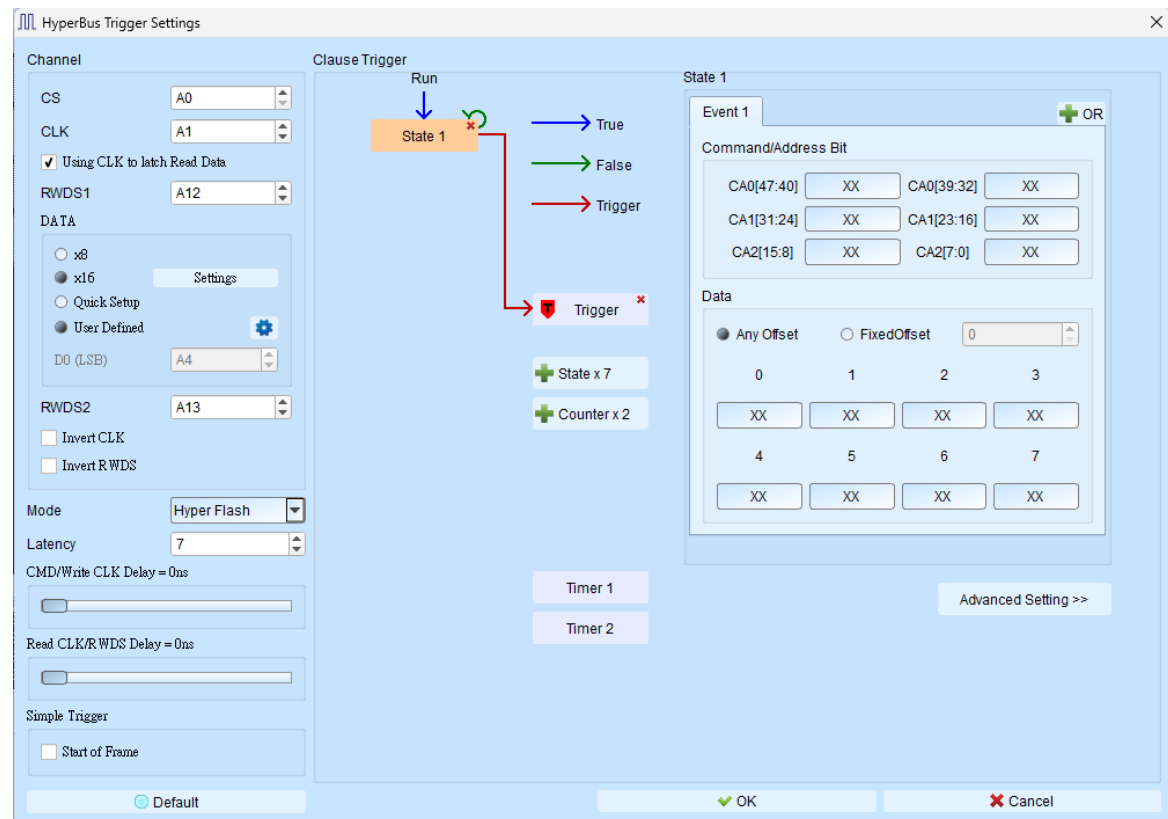
1. **Channel:** Available only on TravelBus B series models, or set to LA channels.
2. **Simple Trigger:** Configure I2C Specific Frame Trigger.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** This section displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values in the Value, R/W, ACK, and Data fields, or use 'X' as a wildcard for any value.

The Data field can be set to HID descriptor as a trigger condition. When the trigger item is set to descriptor, the R/W field will automatically switch to Read mode.

HyperBus Trigger

HyperBus Trigger Settings

Click HyperBus Trigger in the toolbar and will show the dialog as the following.



1. Channel:

- I. **CS、CLK、RWDS1、RWDS2:** Configure HyperBus Channel.
- II. **Using CLK to latch Read Data:** Uses CLK to latch Read Data. Enabled when selected.
- III. **DATA:**
 - ◆ **x8、x16:** Configure the Data Bus Width.
 - ◆ **Quick Setup、User Defined:** Users can either use the Quick Setup function to batch-configure DATA channels or manually define each DATA bit channel.
 - ◆ **Settings:** Configure the Data Arrangement format.
- IV. **Invert CLK:** Reverses the CLK signal. Enabled when selected.
- V. **Invert RWDS respectively:** Independently inverts the RWDS1 & RWDS2 signals. Enabled when selected.

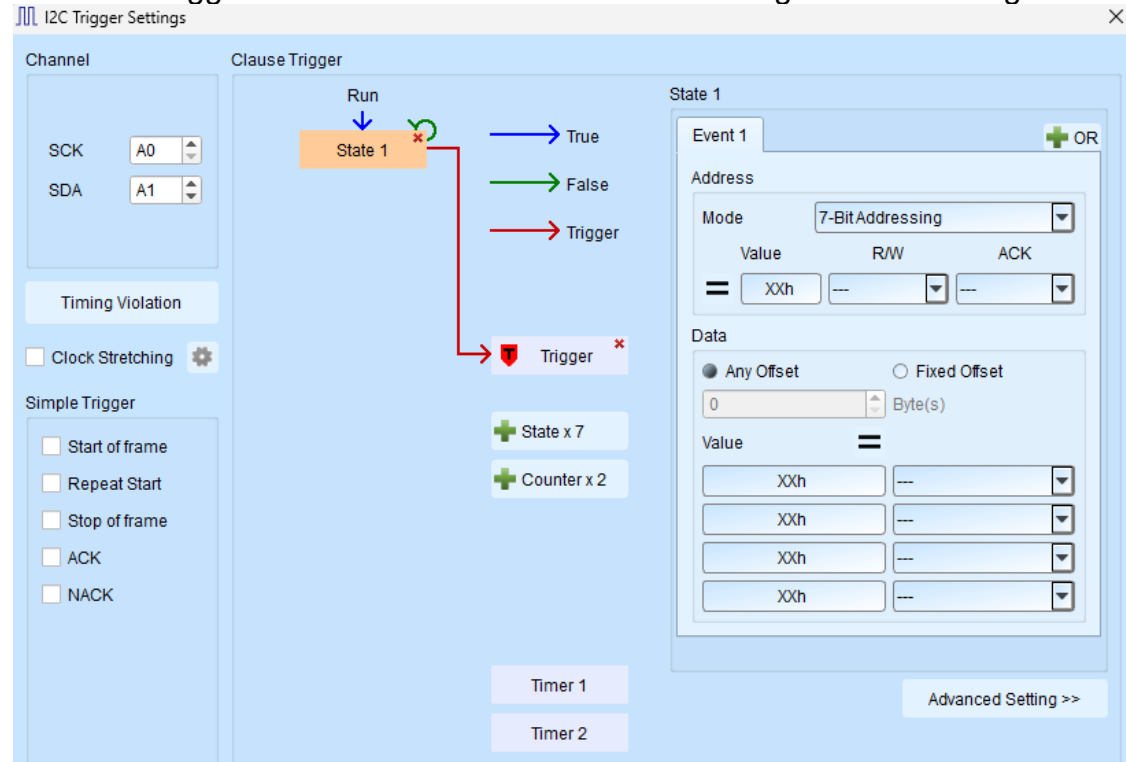
2. Mode: Can be set to HyperFlash or HyperRAM.

3. **Latency:** Sets the number of Sample Points for latency.
4. **CMD/Write CLK Delay 、 Read CLK/RWDS Delay:** Configures the delay time for commands, write clock, read clock, and RWDS.
5. **Clause Trigger:** Please reference Parallel Clause Trigger chapter.
6. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values in the Command/Address Bit and Data fields, or use 'X' as a wildcard for any value.

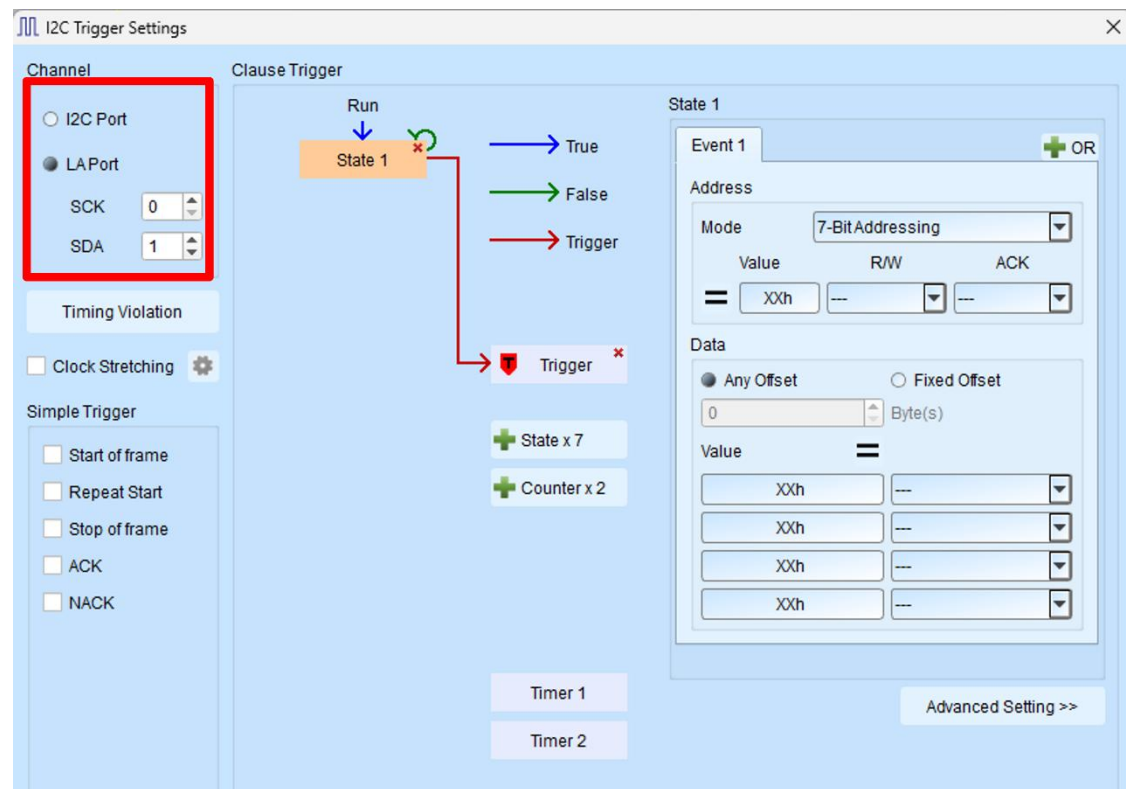
I²C Trigger

I2C Trigger Settings

Click I2C Trigger in the toolbar and will show the dialog as the following.

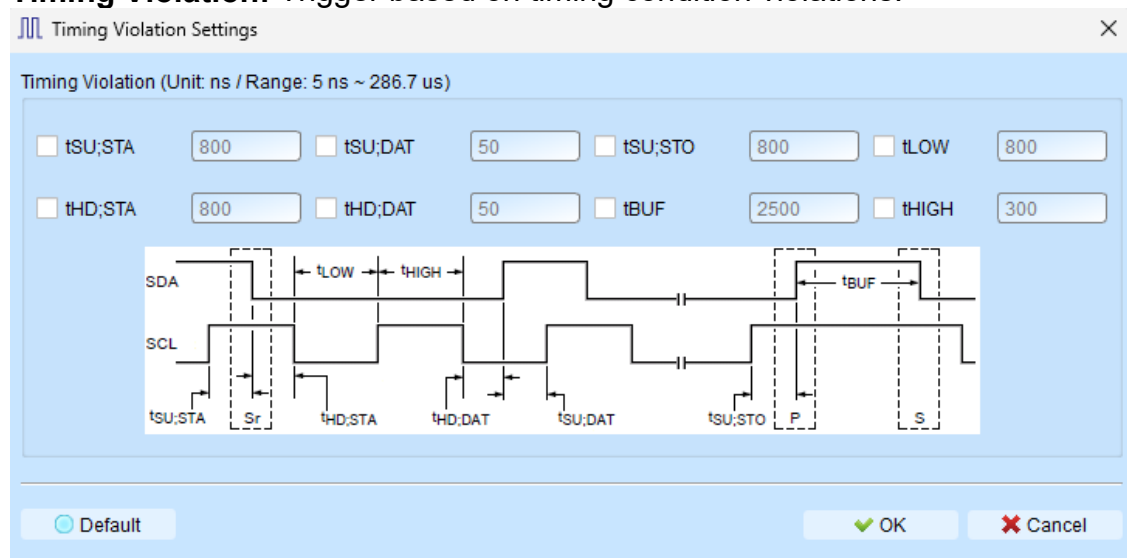


Travel Bus series

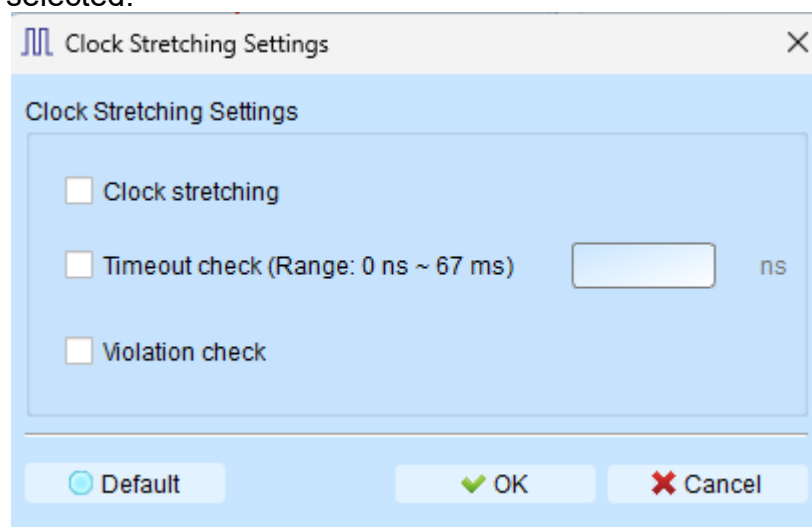


Since TravelBus has specially designed channels for I2C, the I2C settings in the TravelBus software will include additional channel source options.

1. **Channel:** Configure the I2C interface (supported only on TravelBus B series models) or set to LA channels.
2. **Simple Trigger:** Configure I2C specific frame trigger.
3. **Timing Violation:** Trigger based on timing condition violations.



4. **Clock Stretching:** Triggers on Clock Stretching events. Enabled when selected.



- I. **Clock Stretching:** Triggered when slave stretching clock.
 - II. **Timeout Check:** Set the amount of time after which the timeout is determined and triggered.
 - III. **Violation Check:** In HS mode, triggered at the illegal SCL width.
5. **Clause Trigger:** Please reference Parallel Clause Trigger chapter.

- 6. State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can specify trigger values for Value, R/W, ACK, and Data fields or use 'X' as a wildcard for any value.
- I.** The Data field allows up to 4 Bytes to be set. Unused fields should be filled with XXh to indicate any value. Additionally, users can click the equal sign ("=") next to the set value to modify the trigger condition to "not equal to" the specified value.
- II.** The input field can contain the required trigger Data or 'X' to represent any value. When entering values:
- Hexadecimal values should end with 'h'.
 - Binary values should end with 'b'.
 - Decimal values do not require a suffix.
- III.** Trigger Data Offset (Offset):
- i. Any Offset: Triggers when valid **Data** that meets the set conditions appears anywhere in the **Data** field, regardless of offset.
 - ii. Fixed Offset: Triggers only when valid Data that meets the set conditions appears at the specified offset.

I²S Trigger

I2S Trigger Settings

Click I2S Trigger in the toolbar and will show the dialog as the following.

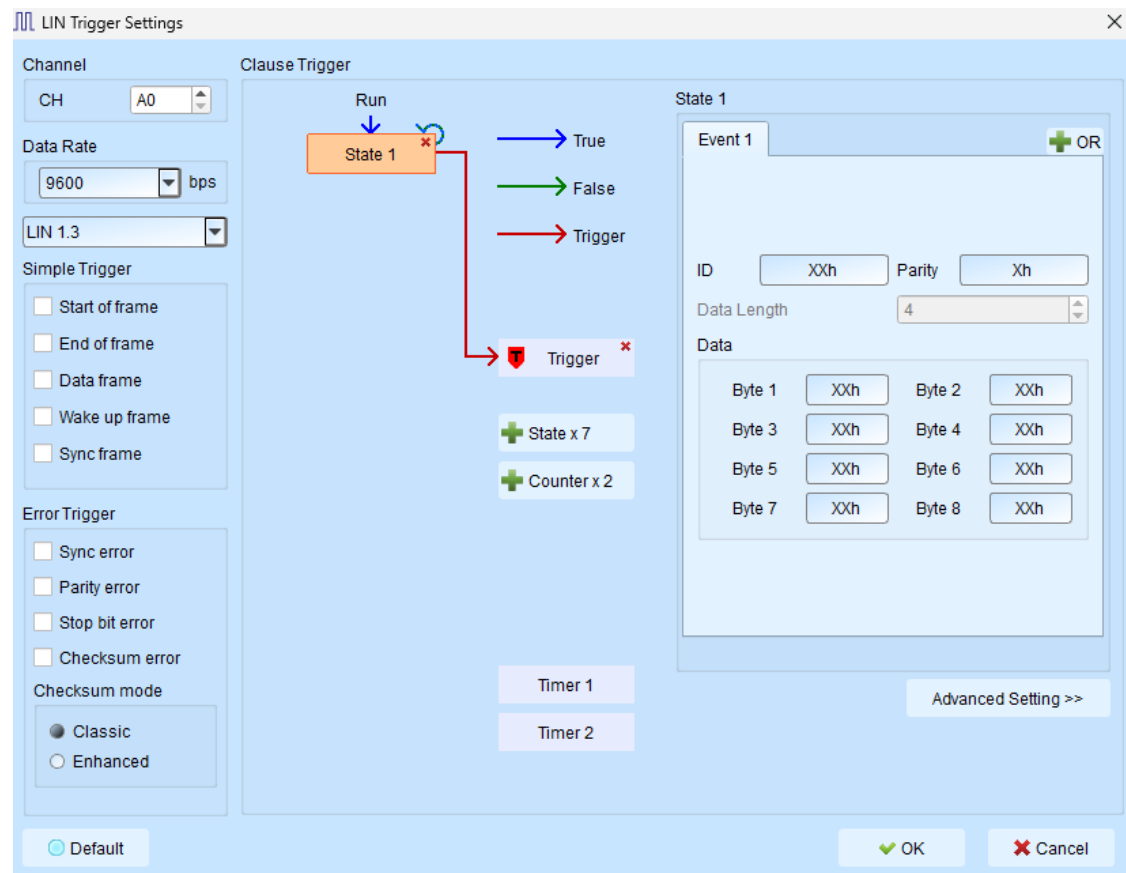
The screenshot shows the 'I2S Trigger Settings' dialog box. It has a title bar with a close button. The main area is divided into sections. The 'Channel' section has three dropdown menus: 'SCK' with value 'A0', 'WS' with value 'A1', and 'SD' with value 'A2'. Below this is 'Data Bits' set to '8' and 'Method' set to 'Data Match'. The 'Data Trigger' section contains two rows of radio buttons: 'Channel' with options 'Both' (selected), 'Left', and 'Right'; and 'Pattern Unit' with options 'Value' (selected), 'Voltage', and 'dB'. Below these is a 'Pattern' dropdown set to '=' and a text box containing '00h'. At the bottom is a 'Duration (# of frames)' text box set to '1'. The bottom of the dialog has three buttons: 'Default' (with a blue circle icon), 'OK' (with a green checkmark icon), and 'Cancel' (with a red X icon).

1. **Channel:** Select Serial clock (SCK), word select (WS) and serial data (SD).
2. **Data Bits:** 1-32 bits, normally it is 8, 12, 16, 24 or 32.
3. **Method:**
 - Data Match : Trigger when the conditions matched.
 - Rising Edge : Trigger when it is a rising edge between two patterns.
 - Falling Edge : Trigger when it is a falling edge between two patterns.
 - Glitch : Trigger when there is a glitch.
 - Mute : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of $-P < X < +P$.
 - Clip : When the duration (or number of frames) is p, the instrument will trigger when the signal is within the range of $-P < X \cup +P > X$.
 - Timing Violation : Provide 6 trigger conditions and this function will be enabled at 200 MHz sampling rate.
4. **Data Trigger:** Select Both, Left, Right channel and pattern unit.

LIN Trigger

LIN Trigger Settings

Click LIN Trigger in the toolbar and will show the dialog as the following.

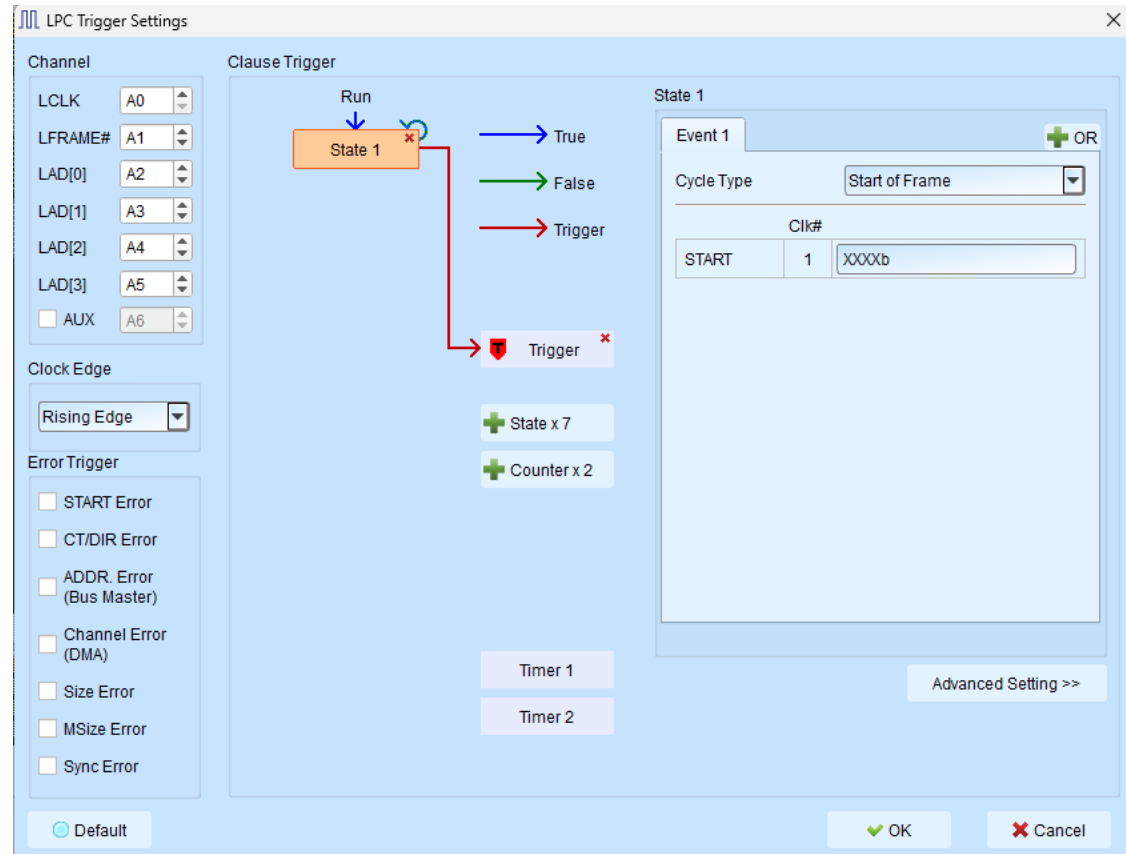


1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of LIN.
3. **Error Trigger:** Trigger specific error of LIN.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ID, Parity, Data Length and Data fields, default value is XX means “don’t care”. When select the LIN 2.2, Data Length field will be enabled.

LPC Trigger

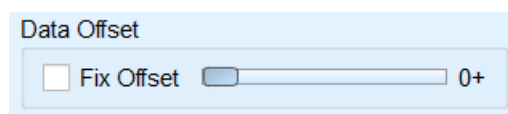
LPC Trigger Settings

Click LPC Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select LPC channels.
2. **Clock Edge:** Select Rising/Falling clock edge.
3. **Error Trigger:** Trigger specific error of LPC.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Cycle Type and its parameters, default value is XX means “don’t care”. Switch $=$ / \neq / $>$ / \leq by click $=$ button.

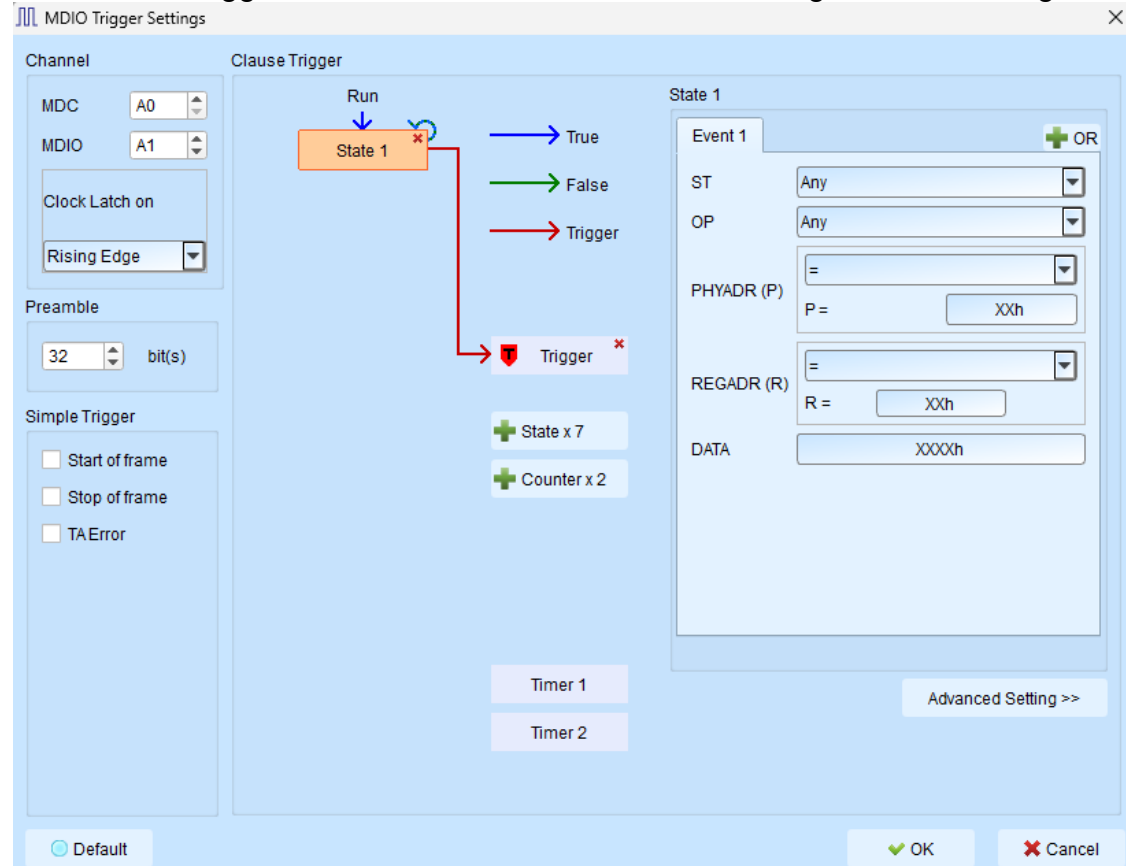
Data offset setting:



MDIO Trigger

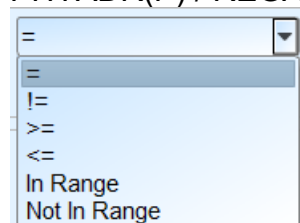
MDIO Trigger Settings

Click MDIO Trigger in the toolbar and will show the dialog as the following.



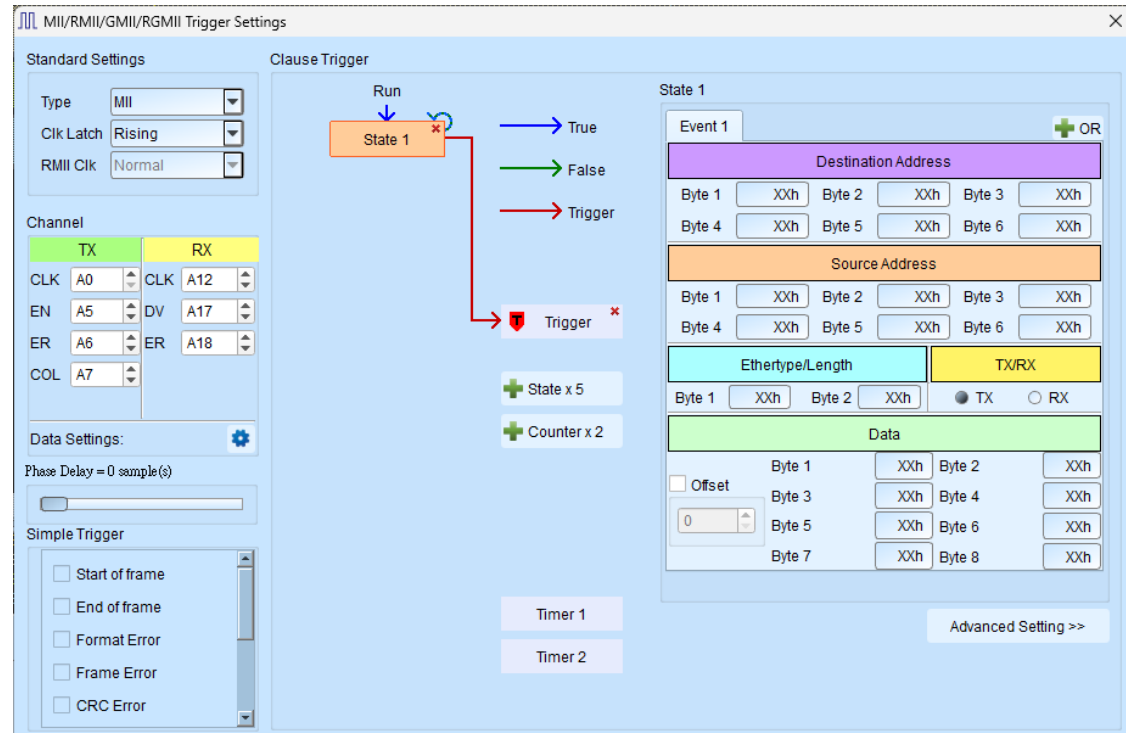
1. **Channel:** Select MDC / MDIO channels.
2. **Preamble:** Select the length of preamble.
3. **Simple Trigger:** Specific trigger function of MDIO.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the ST, OP, PHYADR, REGADR and DATA fields, default value is XX means “don’t care”.

PHYADR(P) / REGADR(R) fields provided the range function:

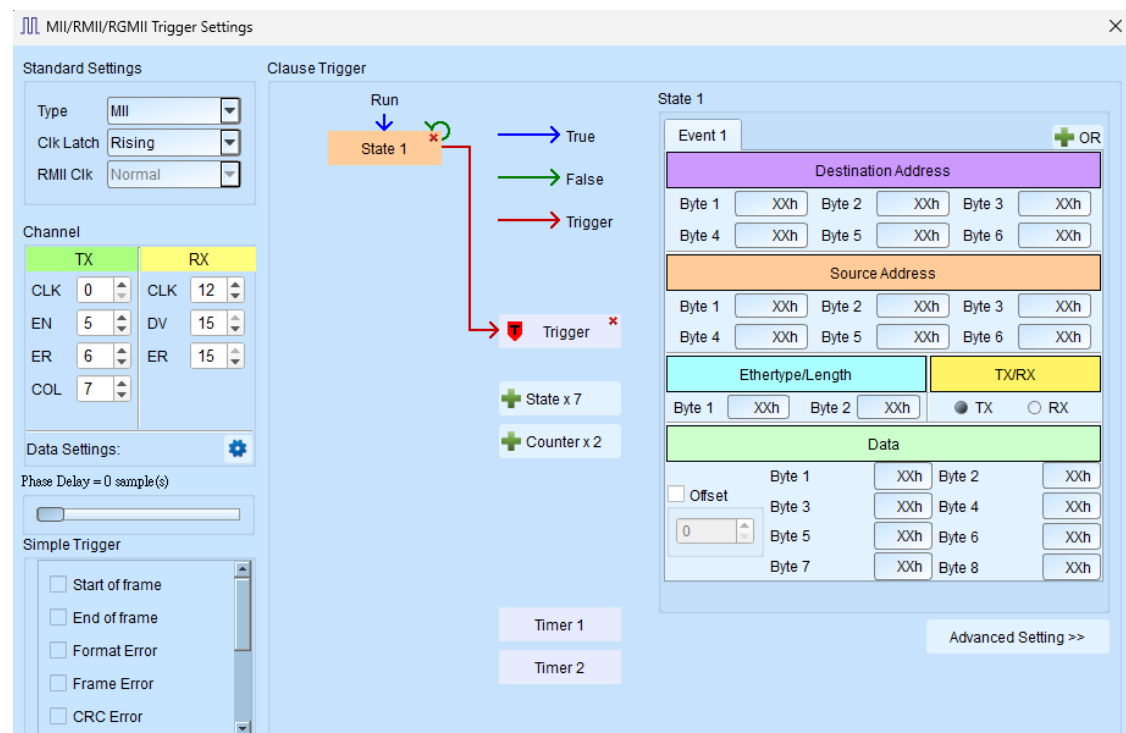


MII / RMI / GMII / RGMII Trigger

BusFinder/LA: Click MII / RMI / GMII / RGMII Trigger in the toolbar and will show the dialog as the following.



Travel Logic/MSO: Click MII / RMI / RGMII Trigger in the toolbar and will show the dialog as the following.



1. Standard Settings:

- I. **Type:** Sets the decoding category. GMII measurement is not supported on TravelLogic and MSO, except for BusFinder/LA models. Additionally, to enable RGMII, the sampling rate must be set to 1 GHz or higher.
- II. **Clk Latch:** Configures whether data is latched on the rising or falling edge of the CLK signal.
- III. **RMII Clk:** Sets the CLK mode for RMII, applicable only when the measurement category is set to RMII.

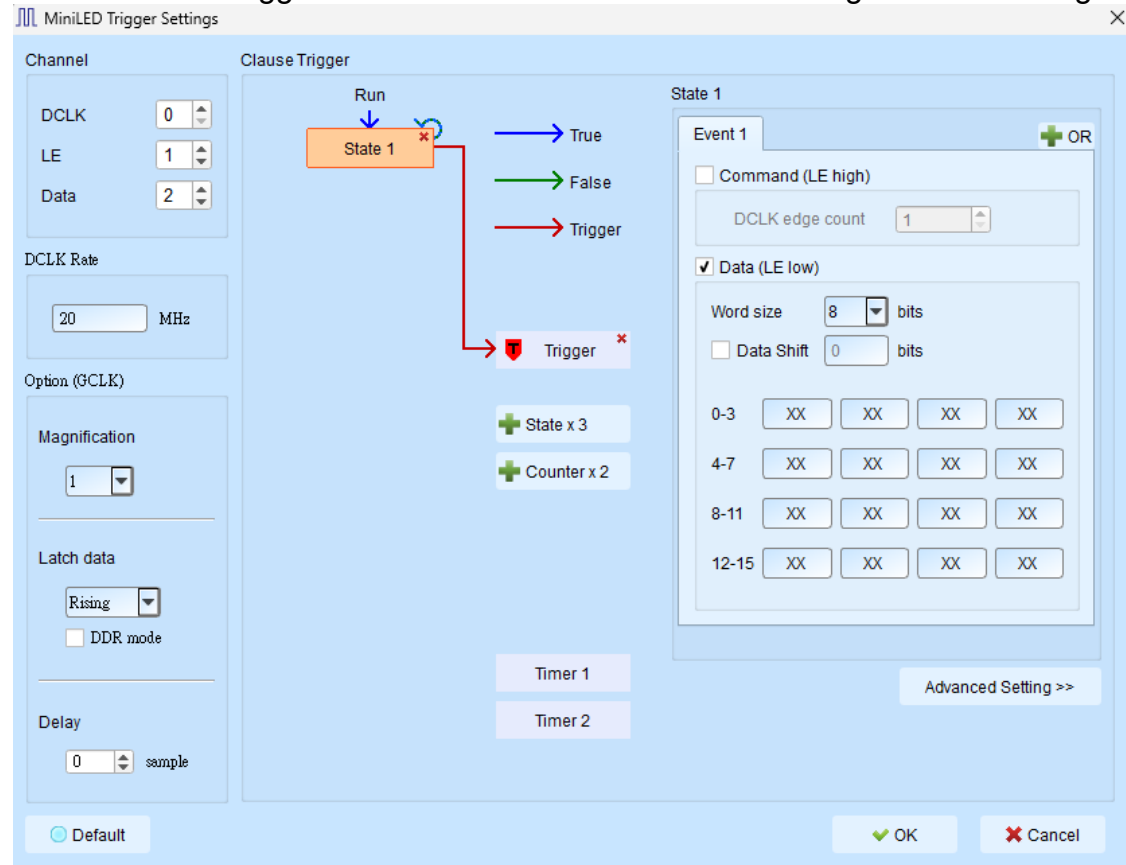
2. Channel:

- I. **TX:** Configures the TX channel, excluding the Data channel.
 - II. **RX:** Configures the RX channel, excluding the Data channel.
 - III. **Data Setting:** Assigns channels for TX Data and RX Data.
- 3. Phases Delay:** Configures the Phase Delay, measured in sample points.
- 4. Simple Trigger:** Provides basic trigger conditions, such as Start of Frame and End of Frame. Enabled when selected.
- 5. Clause Trigger:** Please reference Parallel Clause Trigger chapter.
- 6. State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values for Destination Address, Source Address, or use "X" as a wildcard for any value.

MiniLED Trigger

MiniLED Trigger Settings

Click MiniLED Trigger in the toolbar and will show the dialog as the following.

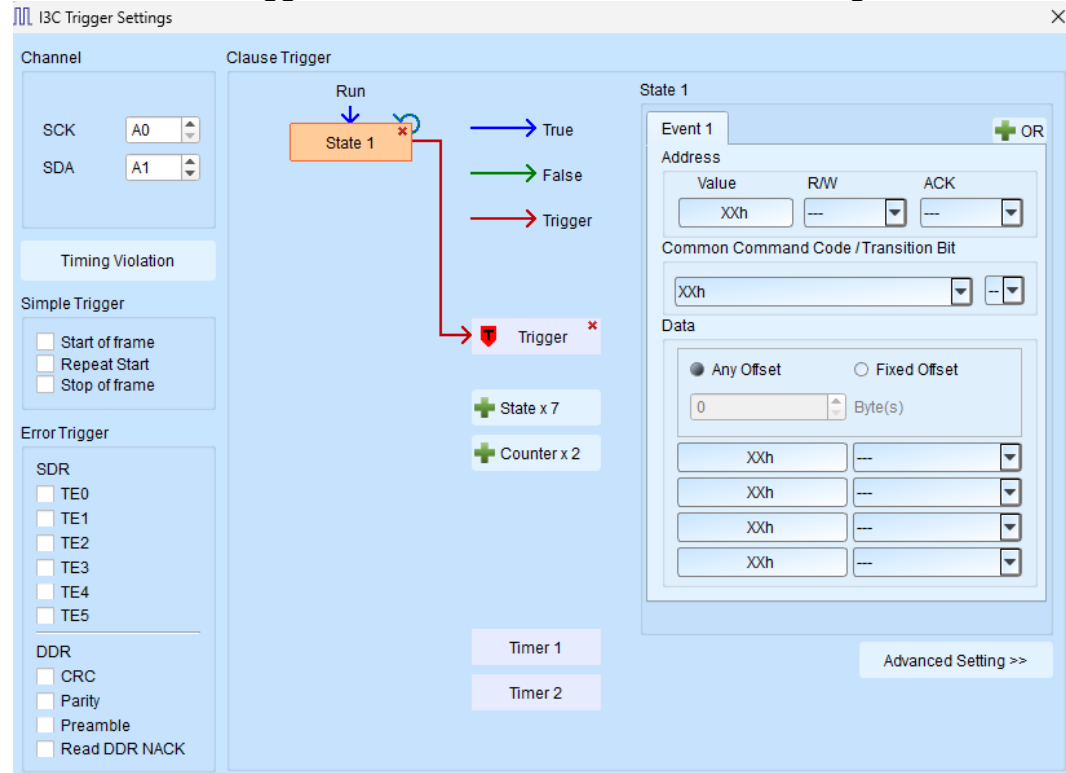


1. **Channel:** Configures the channels for DCLK, LE, and Data.
2. **DCLK Rate:** Sets the speed of DCLK.
3. **Option (GCLK):**
 - I. **Magnification:** Sets the simulation CLK multiplier relative to DCLK.
 - II. **Latch Data:** Determines whether Data is latched on the rising or falling edge.
 - **DDR mode:** Enables DDR mode when selected.
 - III. **Delay:** Configures the delay time, measured in sample points.
4. **Clause Trigger:** Please reference Parallel Clause Trigger chapter.
5. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. In the Command field, enter the DCLK edge count value, while in the Data field, enter a specific trigger value or use 'X' as a wildcard for any value.

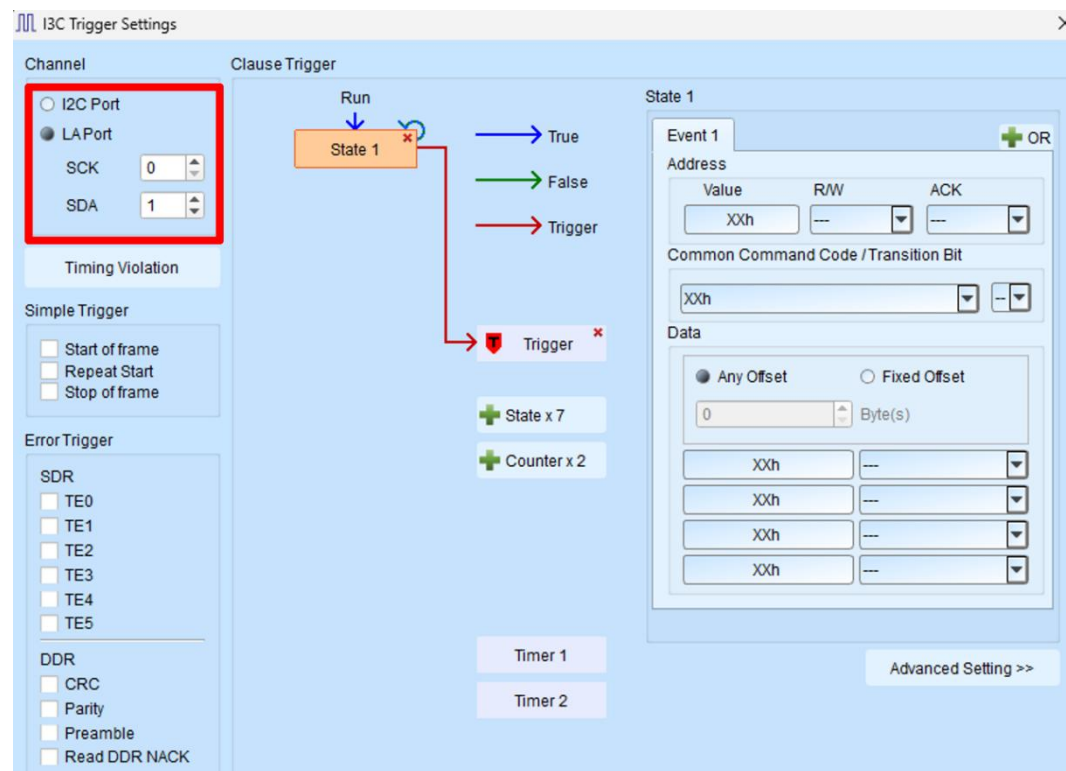
MIPI I3C Trigger

MIPI I3C Trigger Settings

Click MIPI I3C Trigger in the toolbar and will show the dialog as the following.



Travel Bus series



Channel: Configure the I3C channel using either I2C Port or LA Port.

Simple Trigger: Set triggers for I3C Start, Repeat Start, or Stop events.

State: Categorized into Address, Common Command Code (CCC), and Data.

For the Data parameter, two offset options are available:

Any Offset (default): Triggers when the first detected I3C data matches the specified value.

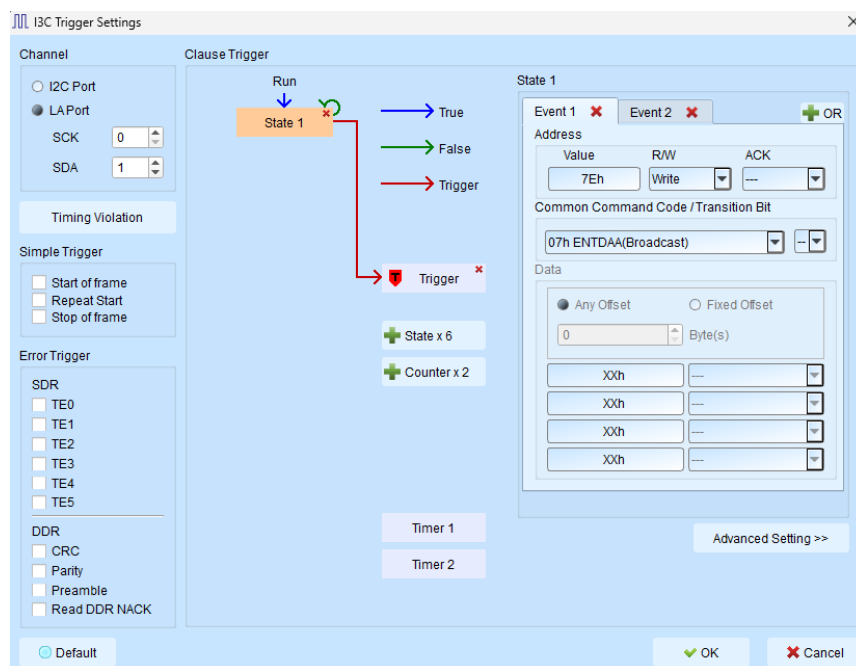
Fixed Offset: Specifies both the I3C data value and its exact position (offset).

An offset of 0 triggers on the first data byte, with the offset unit in bytes.

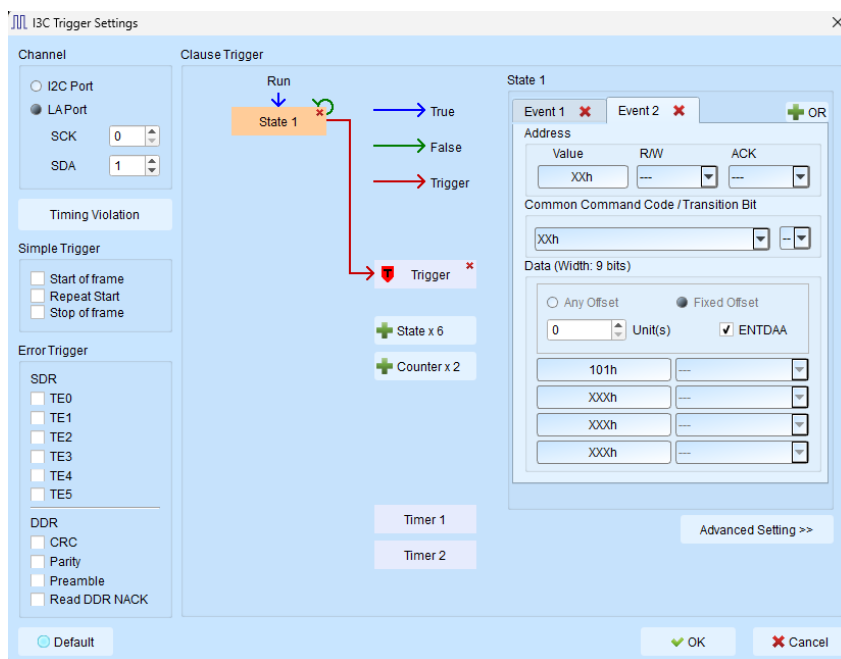
Since some I3C CCCs contain specially formatted data, the following describes their specific trigger settings:

1. Triggering on RSTDAA (06h) / ENTDAAs (07h) data

a. Event 1 CCC is set to RSTDAA (06h) / ENTDAAs (07h).

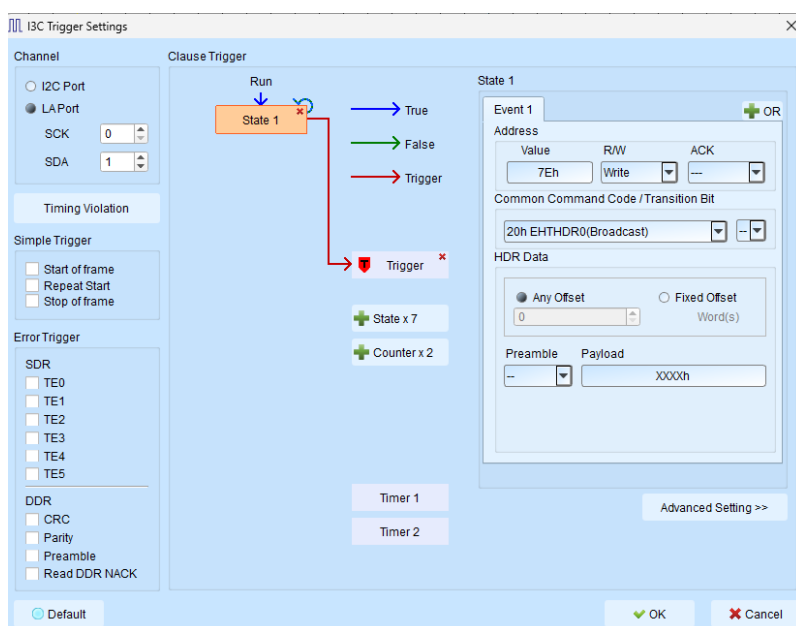


b. Event 2: When selecting ENTDAAs, the entered data width must be 9 bits and is fixed to Fixed Offset.



2. Triggering on EHTHDR0 (20h) / EHTHDR1 (21h) / EHTHDR2 (22h) HDR

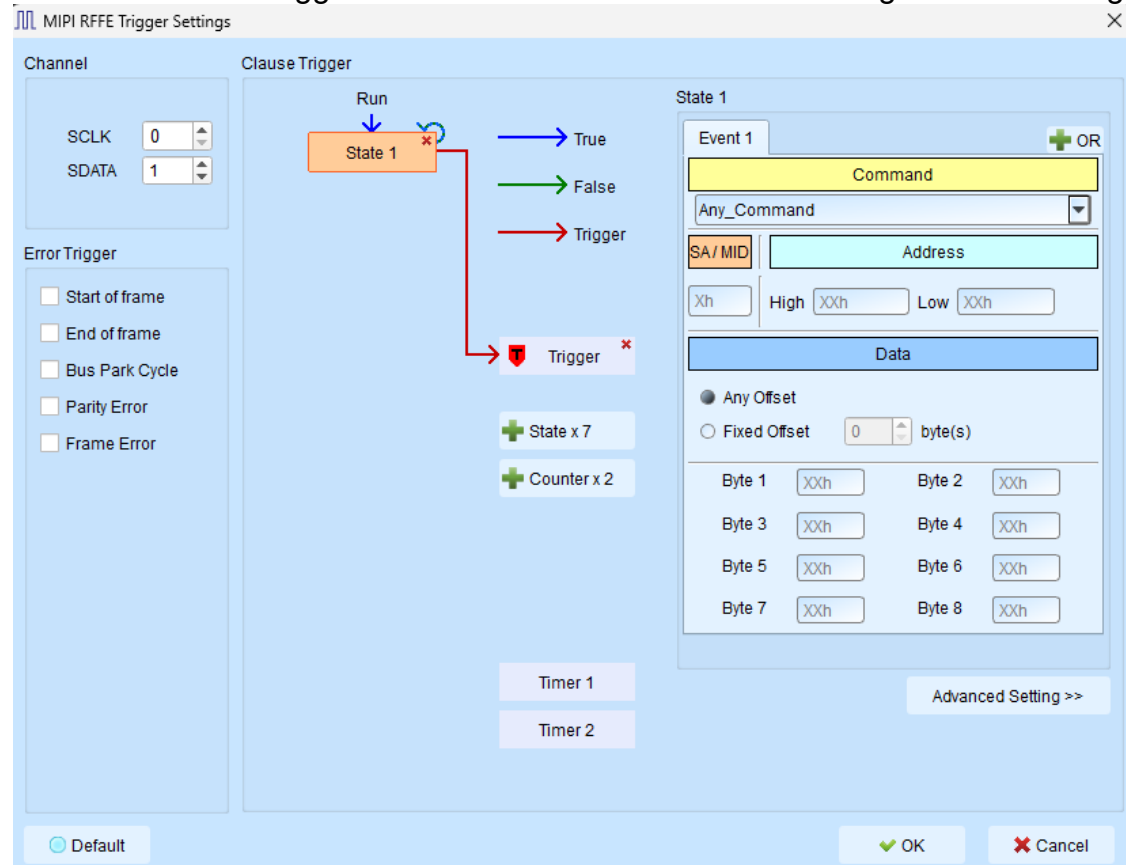
Data: The data format consists of a 16-bit payload.



MIPI RFFE Trigger

MIPI RFFE Trigger Settings

Click MIPI RFFE Trigger in the toolbar and will show the dialog as the following.

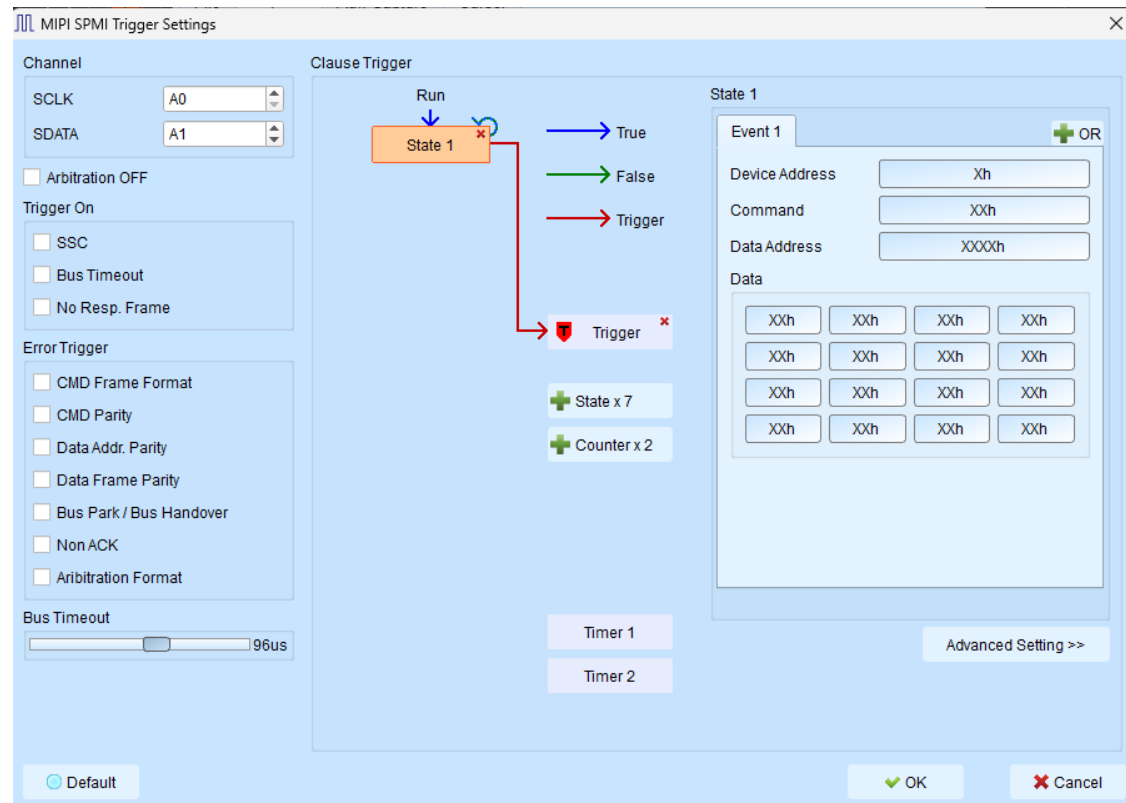


1. **Channel:** Configure the channels for SCLK and SDATA.
2. **Error Trigger:** Provides basic trigger conditions, such as Start of Frame and End of Frame. Enabled when selected.
3. **Clause Trigger:** Please reference Parallel Clause Trigger chapter.
4. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the Command type, enter a specific Address trigger value, or specify a Data trigger value, with the option to use 'X' as a wildcard for any value.

MIPI SPMI Trigger

MIPI SPMI Trigger Settings

Click MIPI SPMI Trigger in the toolbar and will show the dialog as the following.

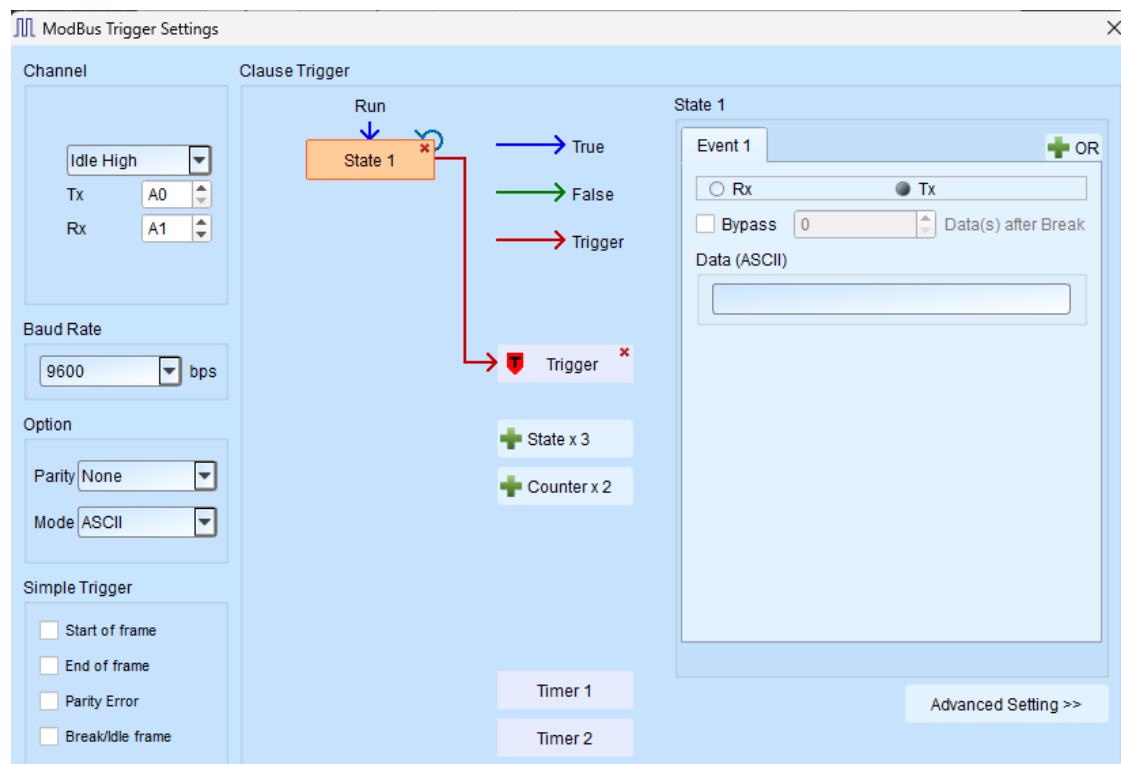


1. **Channel:** Configure the channels for SCLK and SDATA.
2. **Arbitration OFF:** Disables Arbitration. Enabled when selected.
3. **Trigger On:** Configure specific special trigger conditions. Enabled when selected.
4. **Error Trigger:** Provides basic trigger conditions, such as CMD Frame Format and CMD Parity. Enabled when selected.
5. **Bus Timeout:** Set the timeout duration.
6. **Clause Trigger:** Please reference Parallel Clause Trigger chapter.
7. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the Command type, enter a specific Address trigger value, or specify a Data trigger value, with the option to use 'X' as a wildcard for any value.

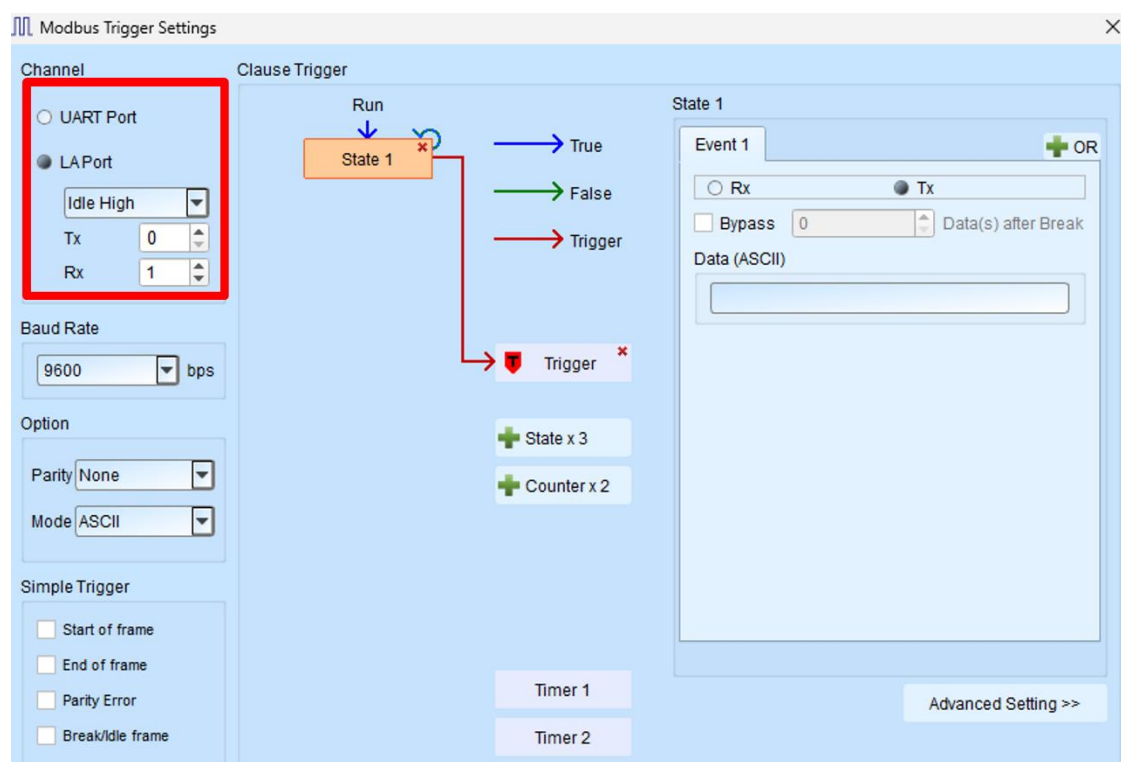
ModBus Trigger

ModBus Trigger Settings

Click ModBus Trigger in the toolbar and will show the dialog as the following.



Travel Bus series



Since TravelBus has specially designed channels for UART, the ModBus settings in the TravelBus software will include additional channel source options.

Channel

UART Port / LA Port : Select ModBus channels.

Baud Rate

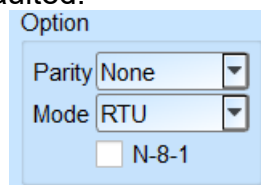
Select the baud rate and providing the manual input if no appropriate selection.

Option

Parity: Provide None/Odd/Even selections, none parity defaulted.

Mode: Provide ASCII/RTU mode, ASCII mode defaulted.

Support the 8-N-1 protocol under RTU mode, 8-N-2 protocol defaulted.



Option

Parity None

Mode RTU

☐ N-8-1

Simple Trigger:

Provide Start of frame, End of frame, Parity Error, Break/Idle frame triggers °

State:

Provide ASCII/HEX input mode by ASCII/RTU mode.

ASCII

State 1

Event 1 + OR

☐ Rx ☒ Tx

☐ Bypass Data(s) after Break

Data (ASCII)

RTU

State 1

Event 1 + OR

☐ Rx ☒ Tx

☐ Bypass Data(s) after Break

Data (Hex)

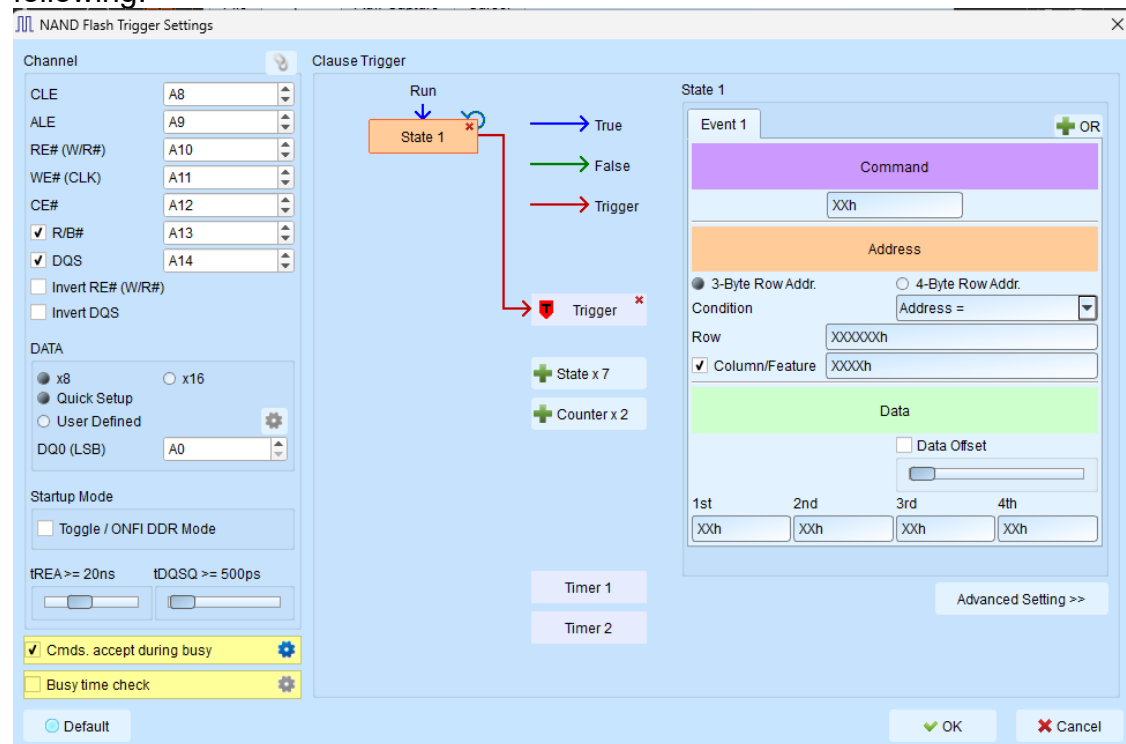
Data Size

0-3

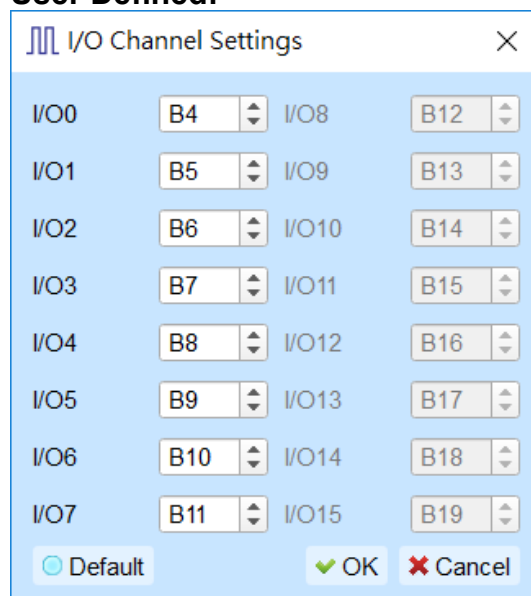
NAND Flash Trigger

NAND Flash Trigger Settings

Click NAND Flash Trigger in the toolbar and will show the dialog as the following.

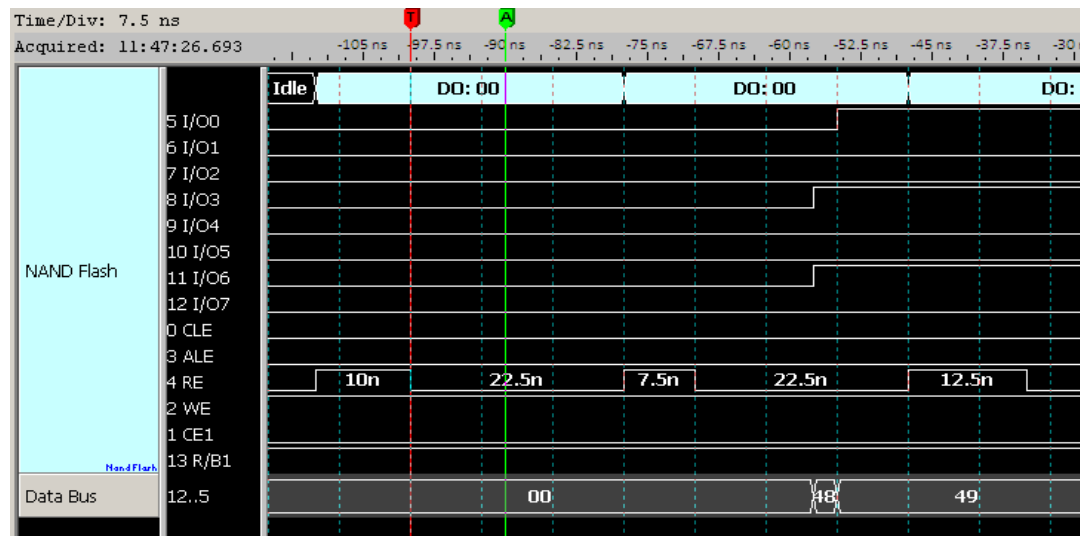


1. **Channel:** Select CLE, ALE, RE, WE, CE, R/B, DQS channels.
2. **DATA:** Select x8 or x16 bits
 - I. **Quick Setup:** Only set DQ0(LSB), others will be set automatically.
(e.g. LSB = B4, MSB = B11; LSB = B7, MSB = B14)
 - II. **User Defined:**

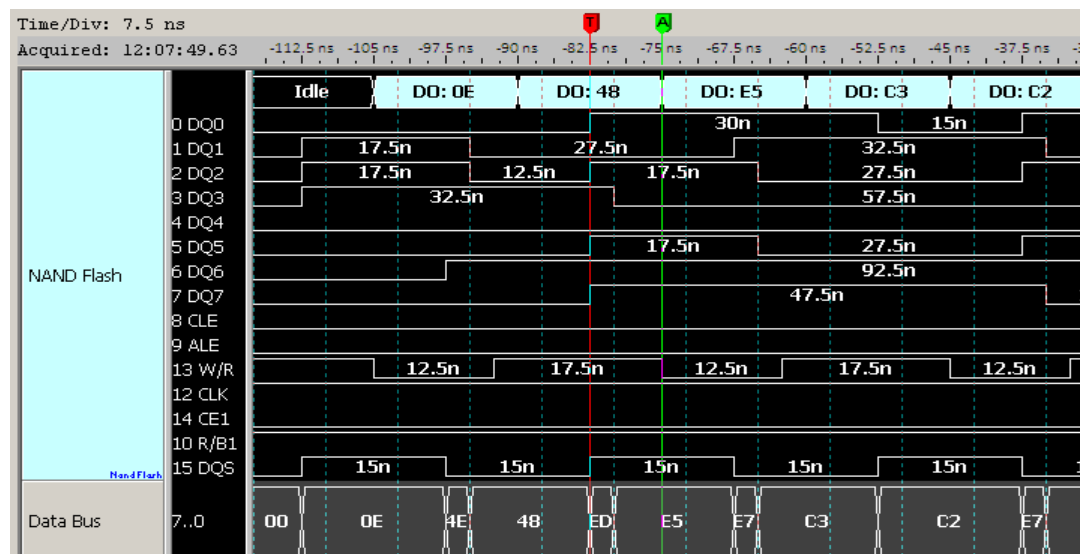


3. **Startup Mode:** Set DDR mode.
4. **tREA / tDQSQ:** Set tREA at SDR mode and tDQSQ at DDR mode.

tREA:



tDQSQ:



5. **Commands accepted during busy:** Set NAND commands still could be triggered during busy state, default is 70h/FFh/78h/7Bh.

Busy Command Settings

Commands

1	70h	5	XXh
2	FFh	6	XXh
3	78h	7	XXh
4	7Bh	8	XXh

☐ Default

Trigger 70h during busy state:



- Busy time check:** Triggers when timing $\geq t_{\text{Busy}}$, providing 6 t_{Busy} to check.

Busy Time Settings

tBusy1 tBusy2 tBusy3 tBusy4 tBusy5 tBusy6

tBusy (Range: 0.1us-250ms)

\geq 250000 us

Command

1 XXh

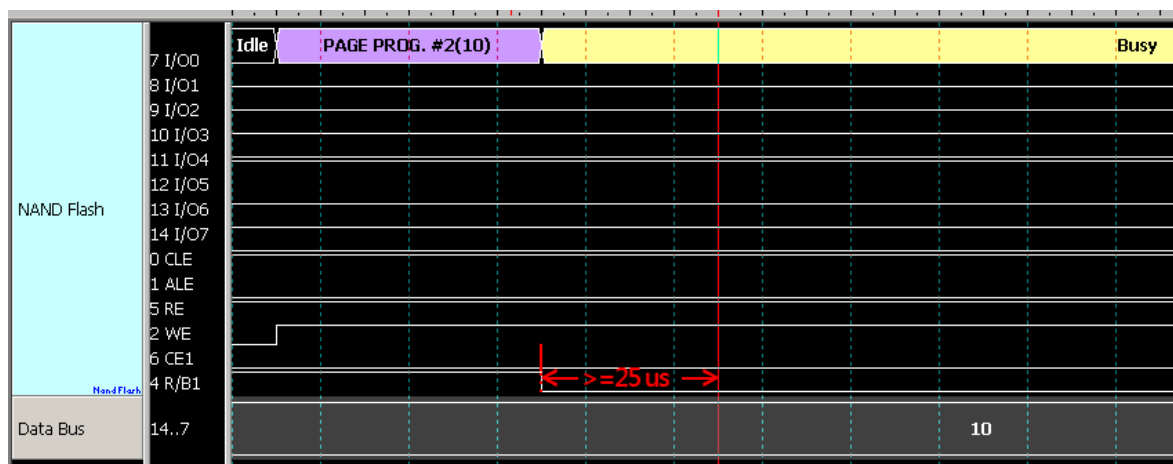
2 XXh

3 XXh

4 XXh

☒ Default

Trigger the tBusy \geq 25 us after NAND command (10h)

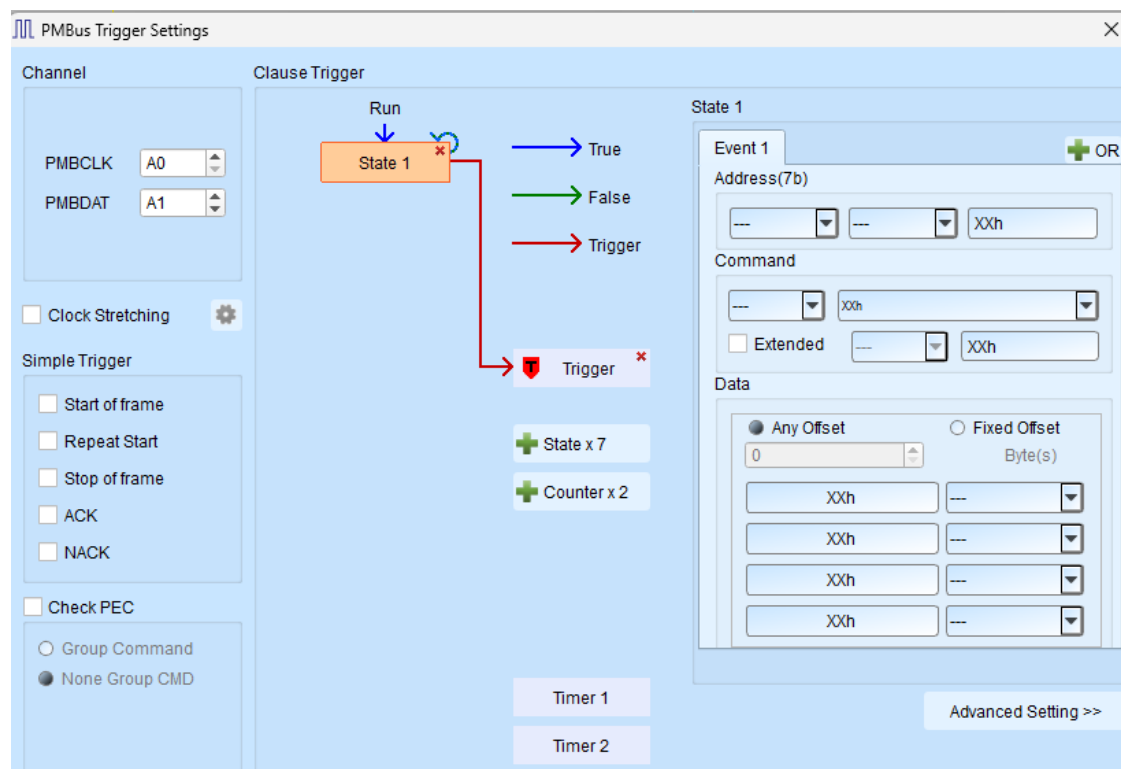


7. **Clause Trigger:** Please reference Clause Trigger chapter.
8. **State:** Show the details of trigger condition in every state as left side; selecting the trigger values in the Command, Address and Data fields, default value is XX means “don’t care”.

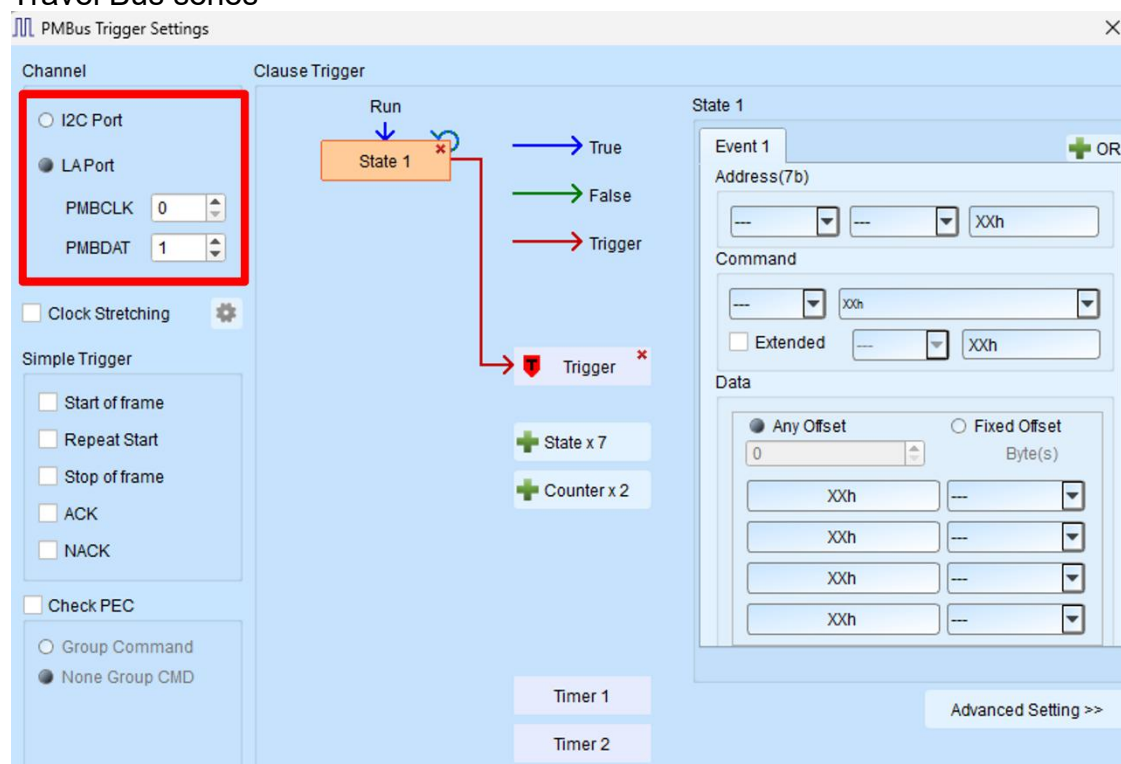
PMBus Trigger

PMBus Trigger Settings

Click PMBus Trigger in the toolbar and will show the dialog as the following.



Travel Bus series



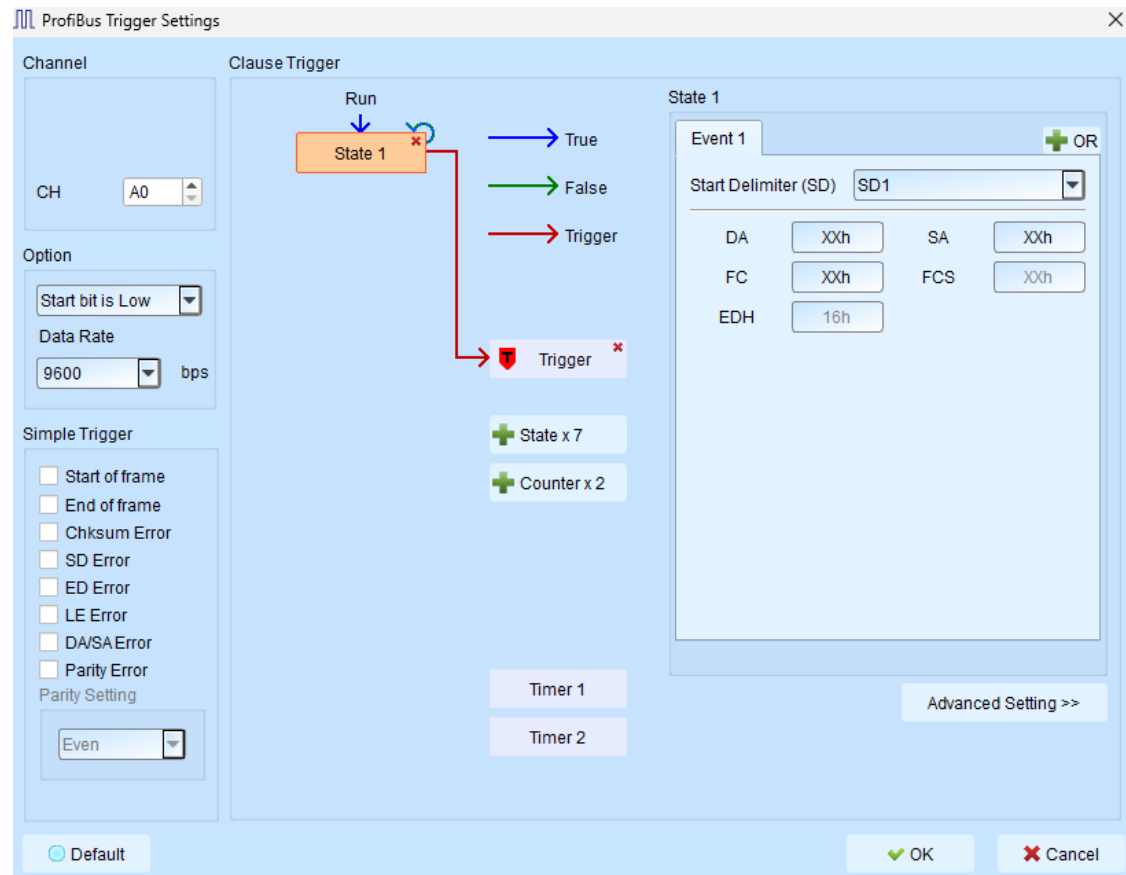
Since TravelBus has specially designed channels for I2C, the PMBus settings in the TravelBus software will include additional channel source options.

1. **Channel:** Configure the I2C interface or LA channel.
2. **Simple Trigger:** Set PMBus-specific frame trigger.
3. **Check PEC:** Configure the trigger for Packet Error Checking (PEC).
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values for Address, Command, and Data, or use 'X' as a wildcard for any value.
 - I. The Data field allows up to 4 Bytes to be set. Unused fields should be filled with XXh to indicate any value.
 - II. The input field can contain the required trigger Data or 'X' as a wildcard.
 - **Hexadecimal** values should end with 'h'.
 - **Binary** values should end with 'b'.
 - **Decimal** values do not require a suffix.
 - III. **Data Offset Triggering:**
 - **Any Offset:** Triggers when valid Data that meets the set conditions appears anywhere in the Data field, regardless of offset.
 - **Fixed Offset:** Triggers only when valid Data that meets the set conditions appears at the specified offset.

ProfiBus Trigger

ProfiBus Trigger Settings

Click ProfiBus Trigger in the toolbar and will show the dialog as the following.

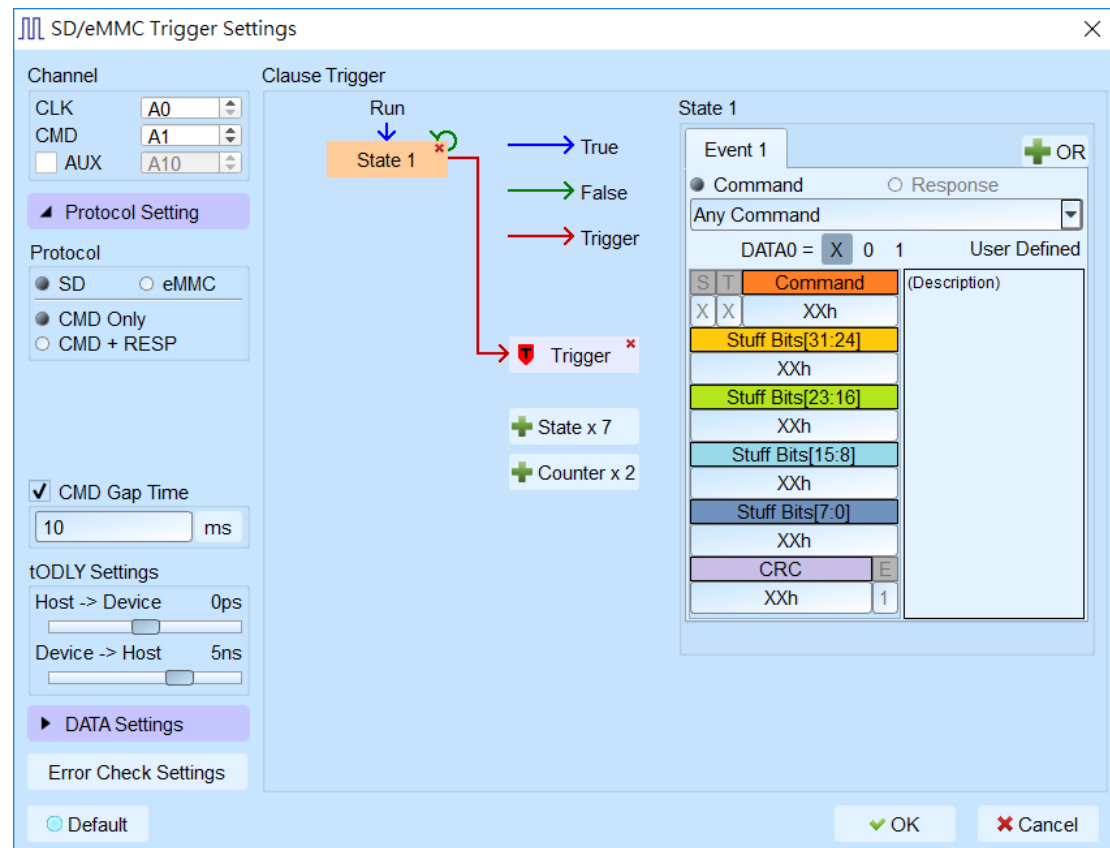


1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of ProfiBus.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SD packet and its fields, default value is XX means “don’t care”.

SD/eMMC Trigger

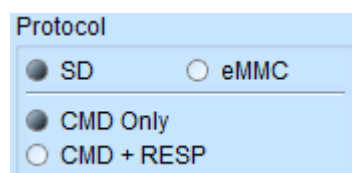
SD/eMMC Trigger Settings

Click **SD/eMMC Trigger** in the toolbar and will show the dialog as the following ◦



1. **Channel:** select CLK, CMD as the trigger channel
AUX can be used for checking power state before running CRC error check, disabled by default.

2. **Protocol:** select SD or eMMC trigger



Command	Response	Argument	CRC7
CMD18:READ_MULTIPLE_BLOCK		000A 8000h	17h
	R1 :CMD18:READ_MULTIPLE_BLOCK	0000 0900h	69h
CMD12:STOP_TRANSMISSION		0000 0000h	30h
	R1b:CMD12:STOP_TRANSMISSION	0000 0B00h	3Fh

3. **CMD Gap time:** delay trigger between the two CMDs.
4. **tODLY Settings:** set the phase delay time such that the device can latch valid command and response.

5. **Error Check Settings:** CRC7 error, CRC16 error, Timeout trigger are parallel structure with the Clause Trigger

I. CRC Error Trigger:

CRC Error Trigger Timeout Trigger

☐ Trigger on CMD (CRC7) error

☐ Trigger on DATA (CRC16) error

Read CMD list for CRC check

Cmd 17 Cmd 18 Cmd 46 Cmd 53

Write CMD list for CRC check

Cmd 24 Cmd 25 Cmd 47 Cmd 54

- ◆ **Trigger on CMD (CRC7) error:** Check the CRC7 error on Command line.
- ◆ **Trigger on DATA (CRC16) error:** Check the CRC16 error on DATA lines.

II. Timeout Trigger: provide 4 statements as following

SD Error Trigger Settings

CRC Error Trigger

Timeout Trigger

☒ Enable Timeout Trigger

☒ Trigger on Data timeout after CMD/DATA

☐ Trigger on Data IDLE timeout before CRC status

☐ Trigger on Busy timeout after CRC Status

☐ Trigger on Busy timeout After CMD

The trigger function will be turned on only after receiving the following command

Cmd 17

Cmd 18

Cmd 24

Cmd 25

- ◆ Trigger on Data timeout after CMD/DATA
- ◆ Trigger on Data IDLE timeout before CRC status
- ◆ Trigger on Busy timeout after CRC status
- ◆ Trigger on Busy timeout after CMD

6. Clause trigger settings: Please reference Clause Trigger chapter

7. Trigger settings

Event 1 + OR

☒ Command ☐ Response

Any Command ▼

DATA0 = ☒ 0 ☐ 1 User Defined

S	T	Command	(Description)
X	X	XXh	
		Stuff Bits[31:24]	
		XXh	
		Stuff Bits[23:16]	
		XXh	
		Stuff Bits[15:8]	
		XXh	
		Stuff Bits[7:0]	
		XXh	
		CRC	E
		XXh	1

SD/eMMC analysis result

Command	Response	Argument (h)	CRC7 (h)	Frequency
CMD23:SET_BLOCK_COUNT		00 00 00 08	BF	166MHz
	R1 :CMD23:SET_BLOCK_COUNT	00 00 09 00	1D	166MHz
CMD18:READ_MULTIPLE_BLOCK		00 00 1D 20	09	166MHz
	R1 :CMD18:READ_MULTIPLE_BLOCK	00 00 09 00	D3	166MHz
CMD23:SET_BLOCK_COUNT		00 00 00 08	BF	166MHz
	R1 :CMD23:SET_BLOCK_COUNT	00 00 09 00	1D	166MHz
CMD18:READ_MULTIPLE_BLOCK		00 00 1C 70	E5	166MHz

Parameter :

DATA0 = ☒ 0 ☐ 1 : use Data0 to judge the R1 and R1b.

Input trigger value, input 'X' means don't care.

Append 'h' for HEX, 'b' for binary, no append for DEC.

When cursor on the input table, the information showed in the right side field.

User Defined add the command reserved:

User Defined Command Setting

Command	Description
Cmd 1	Click To Edit...
Cmd 5	Click To Edit...
Cmd 14	Click To Edit...
Cmd 21	Click To Edit...
Cmd 22	Click To Edit...
Cmd 26	Click To Edit...
Cmd 31	Click To Edit...
Cmd 34	Click To Edit...

SD/eMMC Data Trigger

SD/eMMC Data Trigger Settings

Click **SD/eMMC Data Trigger** in the toolbar and will show the dialog as the following °

1. **Protocol:** select SD or eMMC trigger
2. **Probe Select:** select CLK, CMD and AUX as the trigger channel.
3. **Data Settings:** select current bus width, byte, SDR, DDR of the test object
4. **tODLY Settings:** set the phase delay time such that the device can latch valid command and response.
5. **Data Trigger:** set the patterns of data trigger.
6. **Timeout Trigger:** set the condition of idle time to trigger.

SD/eMMC Data Trigger Settings

Protocol Select

☒ SD
 ☐ eMMC

Probe Select

LA Probe

DATA Settings

☐ 8-bit Data
☒ 4-bit Data
☐ 1-bit Data
☐ DDR Mode
☐ HS 400 (MMC)

Data Length (Byte)

512

TODLY Settings

Host -> Device

0ps

Device -> Host

500ps

Default

Data Trigger

Timeout Trigger

☐ Enable Timeout Trigger

☒ Trigger on Data timeout after CMD/DATA

CMD

DAT

CMD

RESP.

Time

Data

Data

Trigger when

wait Data time >

5

ms

☐ Trigger on Data IDLE timeout before CRC status

CMD

DAT

Time

Data

CRC Status

Trigger when

wait CRC Status time >

5

ms

☐ Trigger on Busy timeout after CRC Status

CMD

DAT

Time

Data

CRC Status

Busy

Trigger when

Busy time >

5

ms

The trigger function will be turned on only after receiving the following command

Cmd 17

Cmd 18

Cmd 24

Cmd 25

OK

Cancel

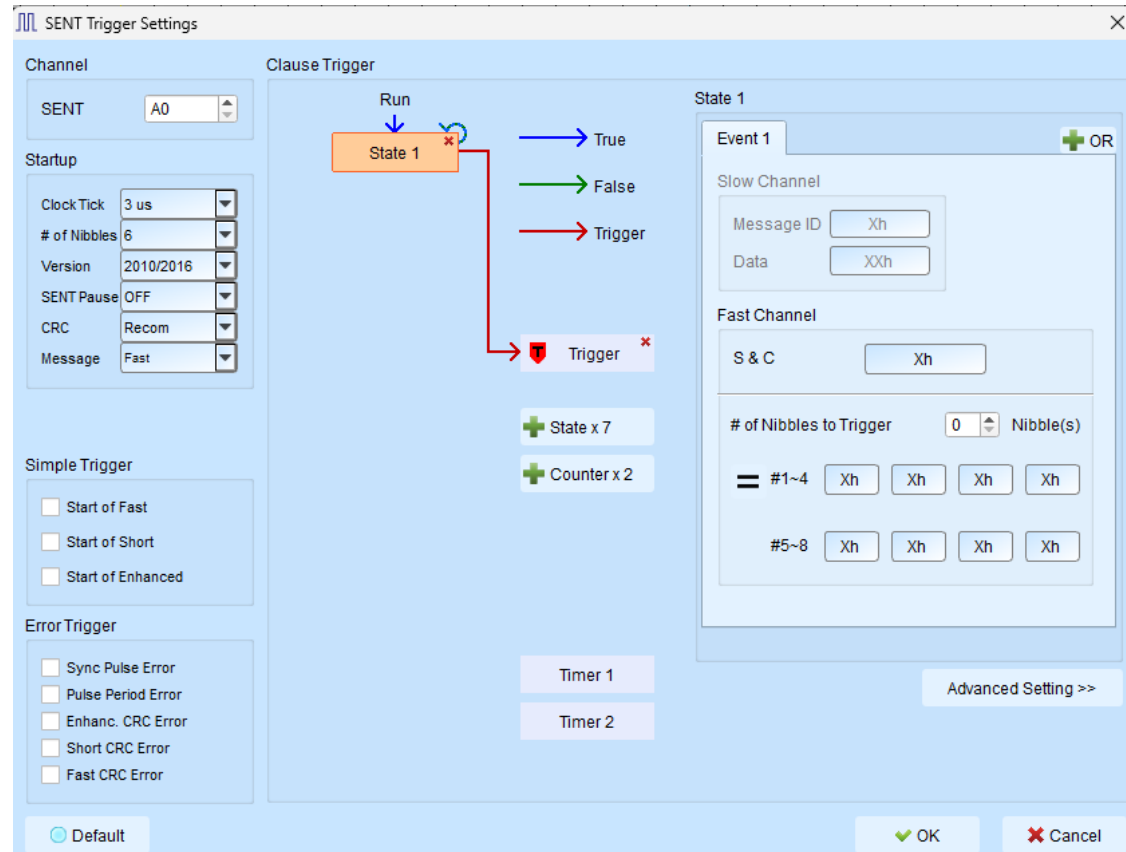
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SENT Trigger

SENT Trigger Settings

Click SENT Trigger in the toolbar and will show the dialog as the following.

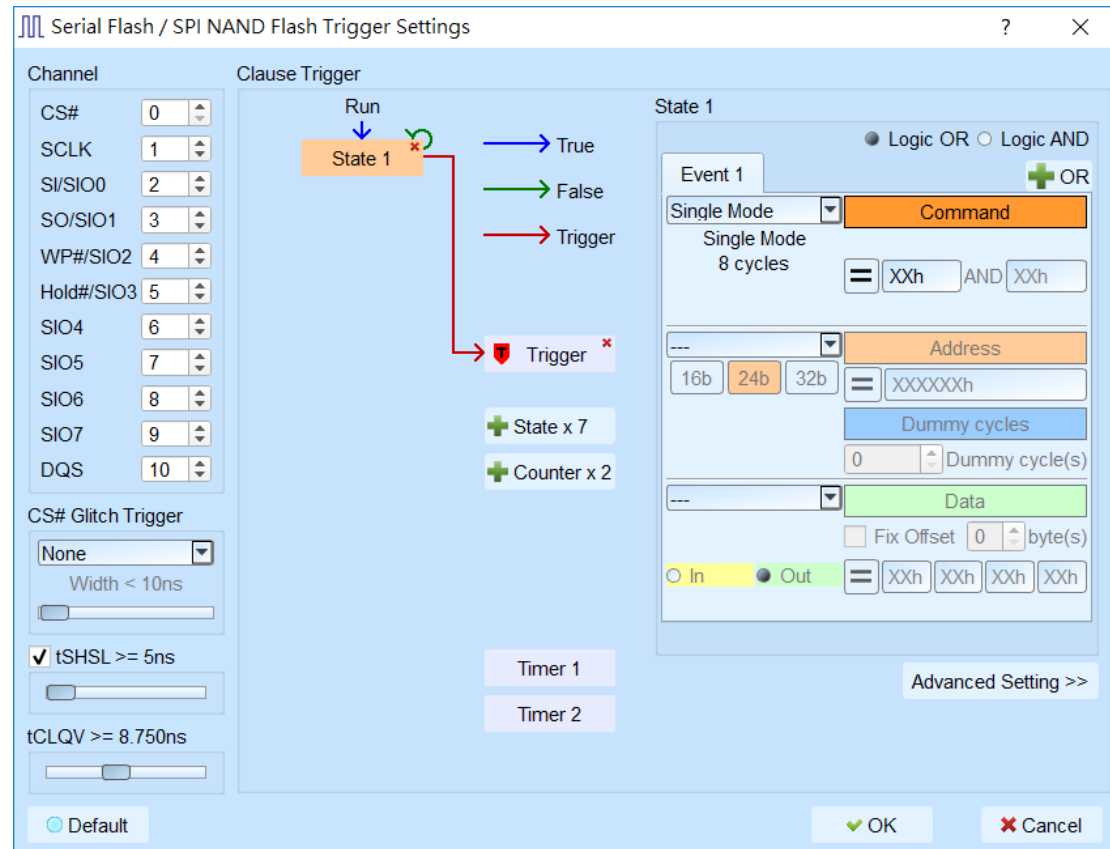


1. **Channel:** Configure the SENT channel.
2. **Startup:** Set the Startup conditions.
3. **Simple Trigger:** Configure SENT-specific frame trigger. Enabled when selected.
4. **Error Trigger:** Configure SENT-specific error trigger. Enabled when selected.
5. **Clause Trigger:** Please reference Clause Trigger chapter.
6. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can configure the Slow Channel Message ID or Data (available only when the Message setting in Startup is set to Short or Enhanced) or specify details in the Fast Channel (available only when the Message setting in Startup is set to Fast).

Serial Flash / SPI NAND Trigger

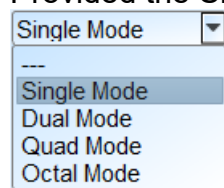
Serial Flash / SPI NAND Flash Trigger Settings

Click Serial Flash Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **CS# Glitch Trigger:** Trigger the glitch on CS# channel.
3. **tSHSL / tCLQV:** Set tSHSL / tCLQV.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the Command, Address and Data fields, default value is XX means “don’t care”.

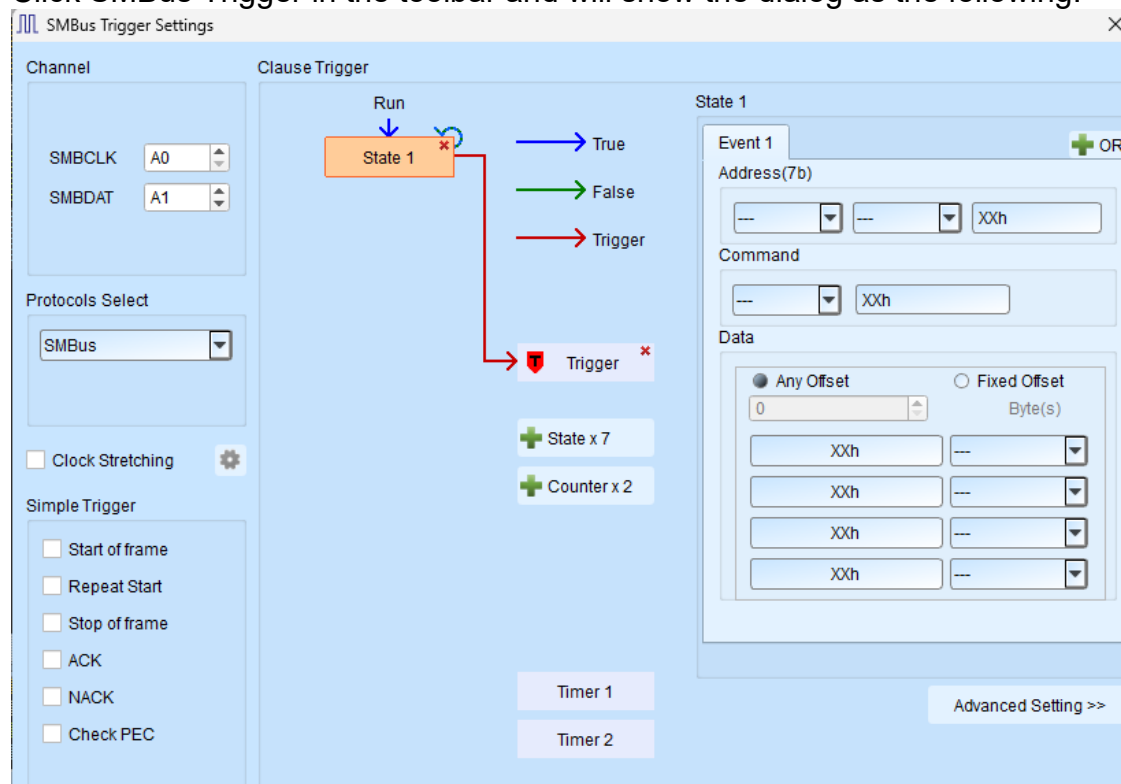
Provided the Single / Dual / Quad / Octal mode.



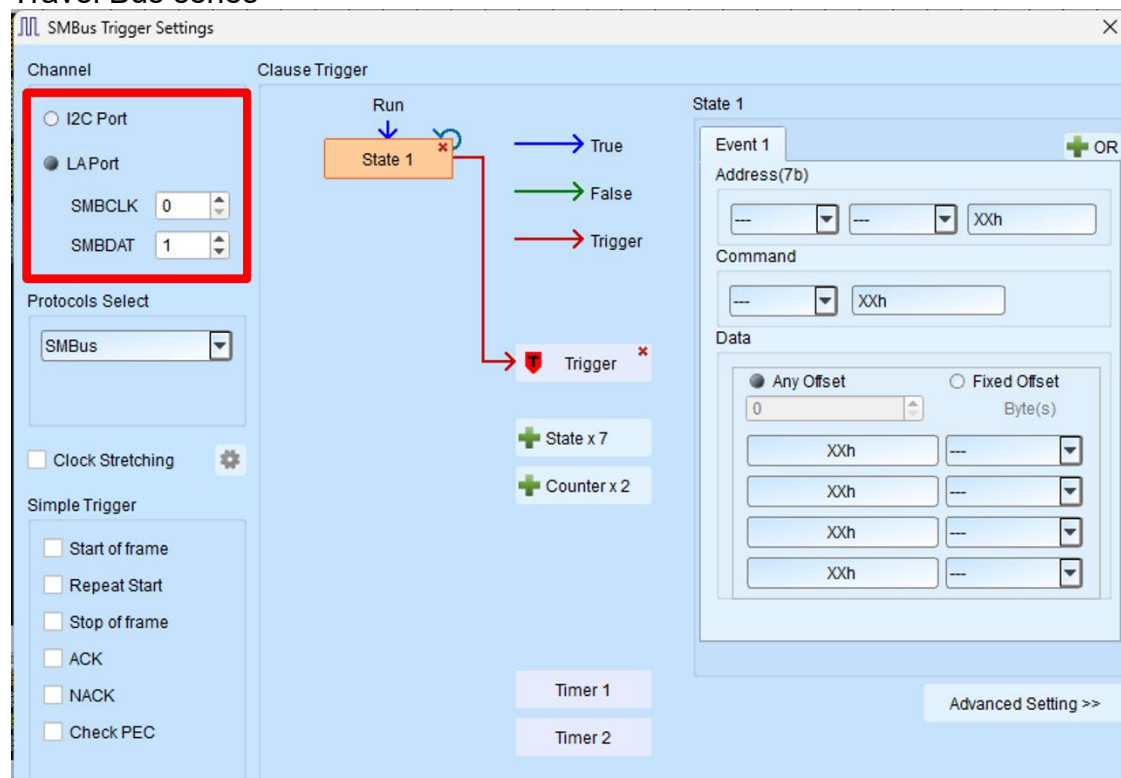
SMBus Trigger

SMBus Trigger Settings

Click SMBus Trigger in the toolbar and will show the dialog as the following.



Travel Bus series



Since TravelBus has specially designed channels for I2C, the SMBus settings in the TravelBus software will include additional channel source options.

1. **Channel:** Configure the I2C interface (supported only on TravelBus B series models) or set to LA channels.
2. **Protocols Select:** Set the trigger for SMBus, SBS, or SPD protocols.
3. **Simple Trigger:** Configure SMBus-specific frame trigger.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Displays the detailed trigger conditions within each level of the trigger process on the left. Users can enter specific trigger values for Address, Command, and Data, or use 'X' as a wildcard for any value. The Command field will display different command formats based on the Protocols Select setting.

I. The Data field allows up to 4 Bytes to be set. Unused fields should be filled with XXh to indicate any value.

II. The input field can contain the required trigger Data or 'X' as a wildcard.

- **Hexadecimal** values should end with 'h'.
- **Binary** values should end with 'b'.
- **Decimal** values do not require a suffix.

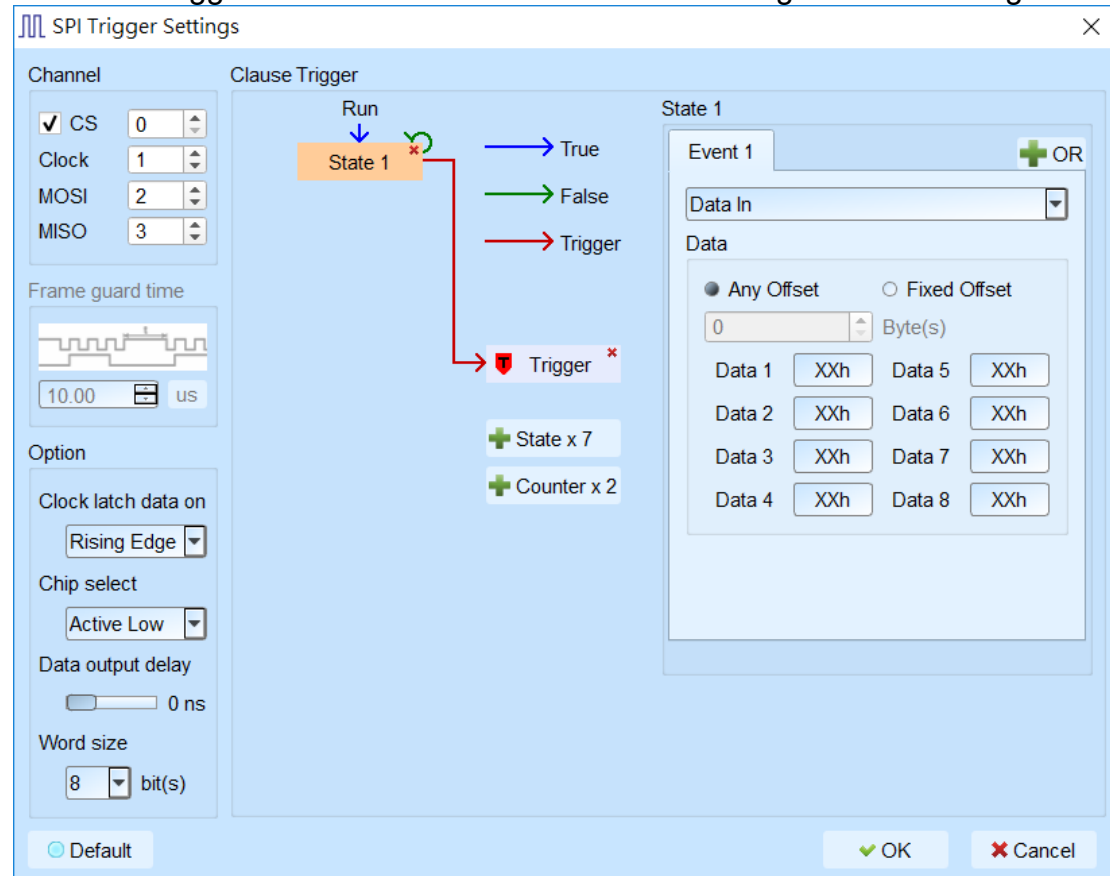
III. Data Offset Triggering:

- **Any Offset:** Triggers when valid Data that meets the set conditions appears anywhere in the Data field, regardless of offset.
- **Fixed Offset:** Triggers only when valid Data that meets the set conditions appears at the specified offset.

SPI Trigger

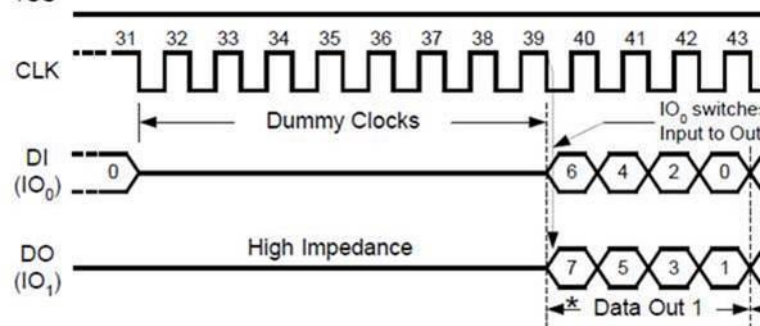
SPI Trigger Settings

Click SPI Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select the channel. Depending on the mode, two to four channels can be used.
2. **Frame guard time:** When CS is not selected, this value can be set to define the time threshold for recognizing the next Frame.
3. **Option:** The Data Output Delay setting specifies how long the Latch Data should be delayed after the transition edge. The default value is 0, with a maximum delay of 75 ns.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Displays the detailed trigger conditions within each level of the trigger process.
 - I. Data In: Triggers based only on the Data In channel.
 - II. Data Out (Ref. Output Delay): Triggers based only on the Data Out channel, applying the Data Output Delay parameter.

- III. Dual Data: Treats Data In/Out as a 2-bit dual-channel mode. For example, if the Word Size is set to 8, only 4 clock cycles are required for transmission. The 1st bit of the Data Out pin represents the MSB.



- IV. Dual Data(Ref. Output Delay): Functions the same as Dual Data, but applies the Data Output Delay parameter.

Data Field Input Rules:

- I. The Data field allows up to 8 Bytes. Unused fields should be filled with XXh to indicate any value.
- II. The input field can contain the required trigger Data or 'X' as a wildcard.
 - Hexadecimal values should end with 'h'.
 - Binary values should end with 'b'.
 - Decimal values do not require a suffix.

III. Data Offset Triggering

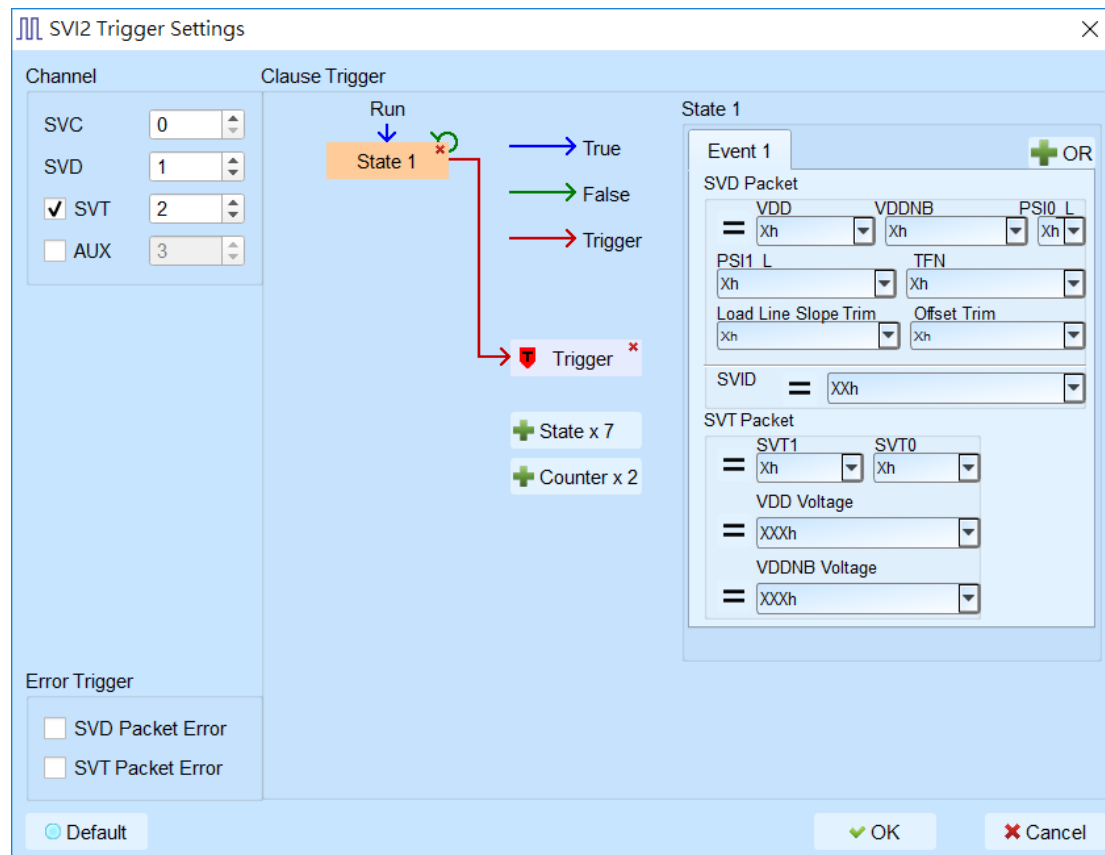
Any Offset: Triggers when valid Data that meets the set conditions appears anywhere in the Data field, regardless of offset.

Fixed Offset: Triggers only when valid Data that meets the set conditions appears at the specified offset.

SVI2 Trigger

SVI2 Trigger Settings

Click SVI2 Trigger in the toolbar and will show the dialog as the following.



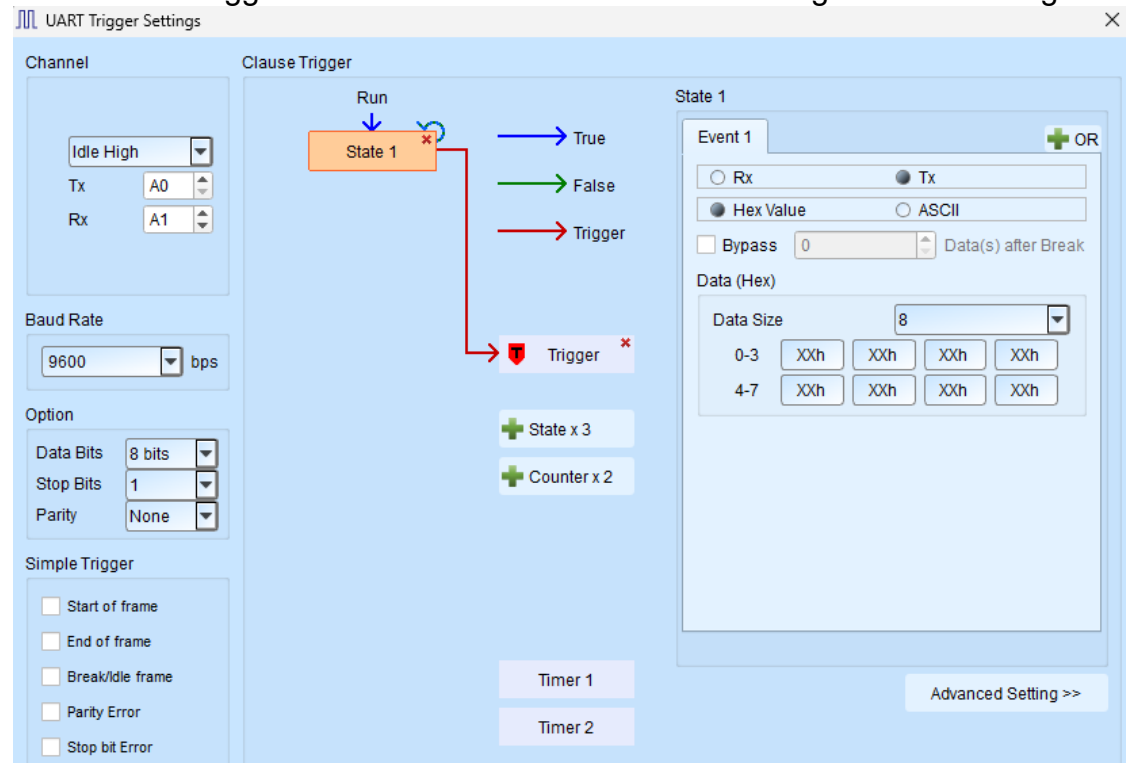
1. **Channel:** Select channels.
2. **Error Trigger:** Trigger specific error of SVI2.
3. **Clause Trigger:** Please reference Clause Trigger chapter.
4. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SVD and SVT packet, default value is XX means “don’t care”.

When check the AUX, the trigger function will refer to the state of AUX (High/Low).

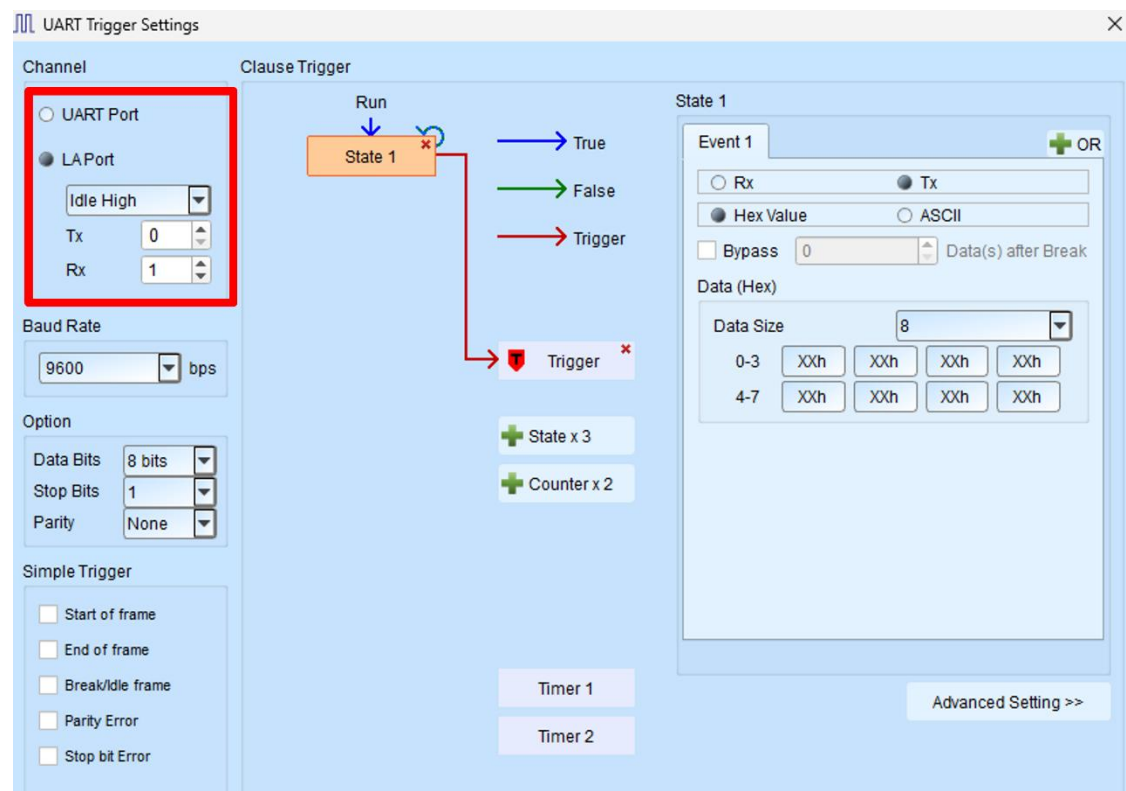
UART Trigger

UART Trigger Settings

Click UART Trigger in the toolbar and will show the dialog as the following.



Travel Bus series



Since TravelBus has specially designed channels for UART, the UART

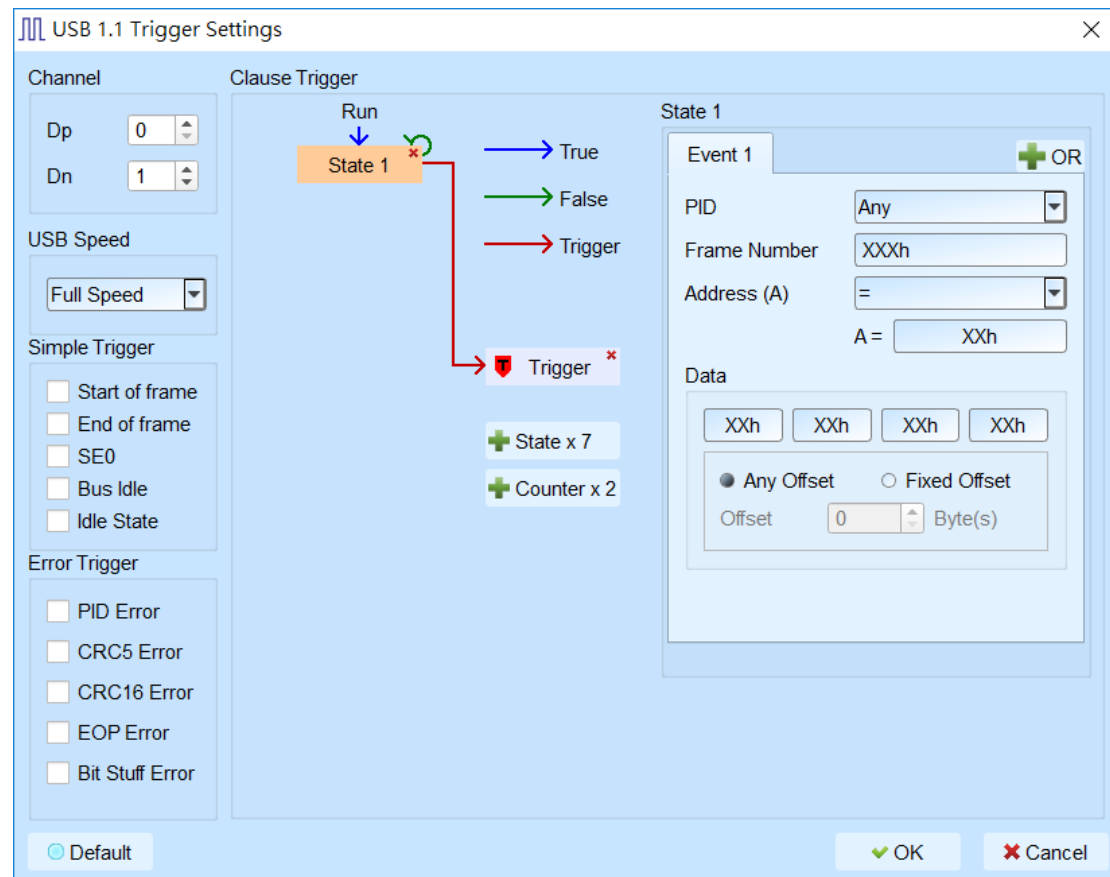
settings in the TravelBus software will include additional channel source options.

1. **Channel:** Configure the UART interface.
2. **Baud Rate:** Set the UART Baud Rate.
3. **Simple Trigger:** Configure UART-specific frame trigger.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Displays the detailed trigger conditions within each level of the trigger process. Users can enter specific trigger values in the Data field or use 'X' as a wildcard for any value. The Data trigger field supports up to 16 Bytes; to specify a trigger data position, Bypass must be selected, and an offset value must be entered.

USB 1.1 Trigger

USB 1.1 Trigger Settings

Click USB 1.1 Trigger in the toolbar and will show the dialog as the following.

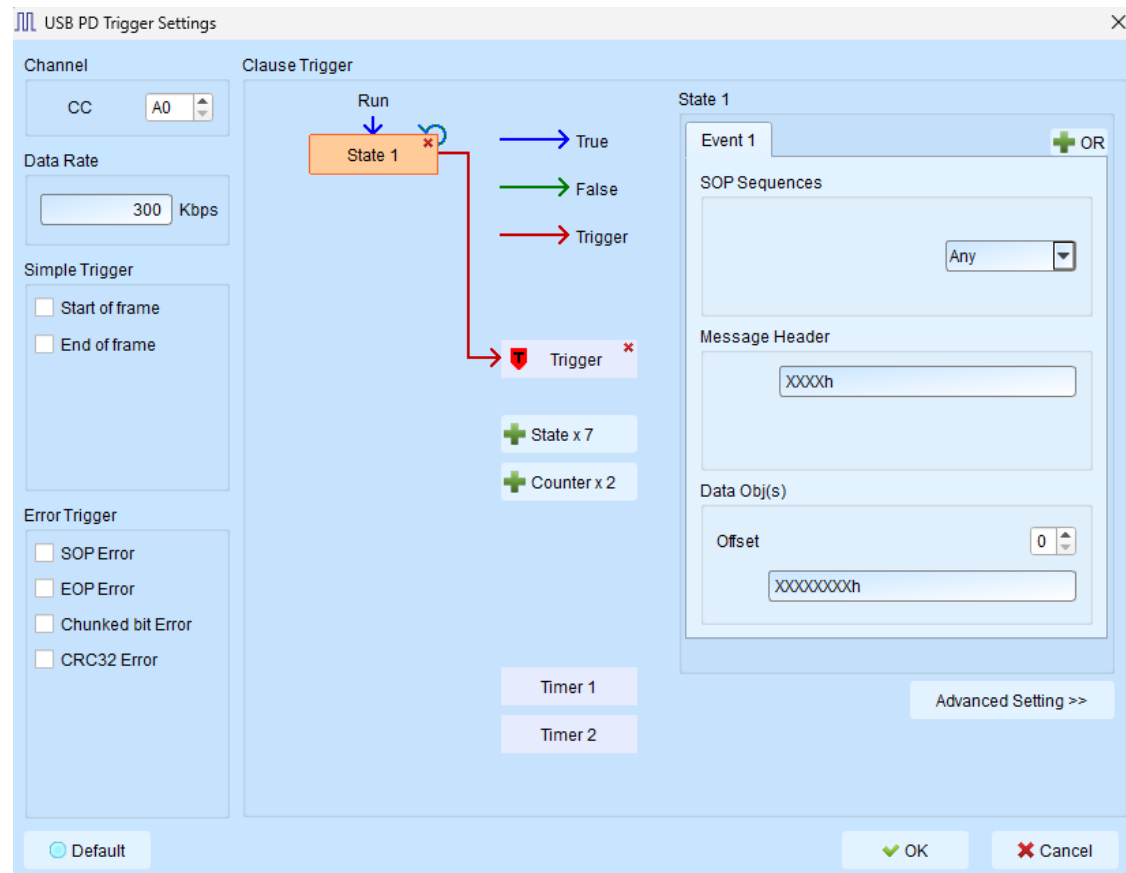


1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of USB 1.1.
3. **Error Trigger:** Trigger specific error of USB 1.1.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the PID, Frame Number, Address and Data Field, default value is XX means “don’t care”.
Data field provided 4 bytes data to trigger, checking the Fixed Offset and selecting the offset value when want to trigger at the specific position.

USB PD Trigger

USB PD 3.0 Trigger Settings

Click USB PD 3.0 Trigger in the toolbar and will show the dialog as the following.



1. **Channel:** Select channels.
2. **Simple Trigger:** Specific trigger function of USB PD 3.0.
3. **Error Trigger:** Trigger specific error of USB PD 3.0.
4. **Clause Trigger:** Please reference Clause Trigger chapter.
5. **State:** Show the details of trigger condition in every state as left side; typing or selecting the trigger values in the SOP Sequences, Message Header and Data Obj(s), default value is XX means “don’t care”.
Provide 0 ~ 7 offset value for Data Obj(s) field.