

Electrical Validation Documents

USER





Table of Contents

Protocols

	I2C Electrical Validation Solution	2
	I2S Electrical Validation Solution	10
	MIPI I3C Electrical Validation Solution	19
	MIPI RFFE Electrical Validation Solution	30
	MIPI SPMI Electrical Validation Solution	36
	PDM Electrical Validation Solution	42
	SMBUS Electrical Validation Solution	53
	SPI Electrical Validation Solution	64
	UART Electrical Validation Solution	69
Additio	onal Settings	
	HTML Report Export	77
	Advanced Settings	79
	MSO/TS3000 series 64-Channel cascading	80



I2C Electrical Validation Solution

Introduction:

File / Settings	s Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

Use an oscilloscope to do I2C Electrical Validation to ensure that the I2C meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

I2C Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the I2C Speed.

Symbol	Parameter	Conditions	C _b = 100	pF (max)	C _b = 4	00 pF ^[2]	Unit
			Min	Max	Min	Max	
f _{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
t _{SU;STA}	set-up time for a repeated START condition		160	-	160	*	ns
t _{HD;STA}	hold time (repeated) START condition		160		160		ns
tLOW	LOW period of the SCL clock		160		320		ns
tHIGH	HIGH period of the SCL clock		60	-	120		ns
t _{SU;DAT}	data set-up time		10	-	10	1	ns
t _{HD;DAT}	data hold time		0 ^[3]	70	0 ^[3]	150	ns
trCL	rise time of SCLH signal		10	40	20	80	ns
t _{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
t _{fCL}	fall time of SCLH signal		10	40	20	80	ns

Part of the electrical characteristics of common I2C specifications:



The report of common	I2C validation:
----------------------	-----------------

o	verview De	tail I2C							
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	fsci.	SCL clock frequencey	0.000 Hz	400.000 KHz	387.596 KHz	387.683 KHz	387.897 KHz	34200	Pass
2	THEUSTA	Hold time(repeated) START condition	600.000 ns	-	1.536 us	1.537 us	1.540 us	200	Pass
3	ISUSTA	Set-up time for a repeated START condition	600.000 ns	-	2.010 us	2.012 us	2.014 us	100	Pass
4	THELENT	Data hold time	-	-	94.000 ns	274.110 ns	1.028 us	17250	Pass
5	T SULDAT	Data Set-up time	100.000 ns	-	472.000 ns	1.066 us	1.444 us	25100	Pass
6	leusro	Set-up time for STOP condition	-	-	-	-	-	0	-
7	tLow	Low Period of the SCL Clock	1.300 us	-	1.538 us	1.542 us	1.544 us	34100	Pass
8	U HICH	High Period of the SCL Clock	600.000 ns	-	974.000 ns	982.475 ns	3.560 us	41800	Pass
9	lect.	Rise time of SCL signal	20.000 ns	300.000 ns	45.999 ns	50.304 ns	51.999 ns	41800	Pass
10	tres.	Fall time of SCL signal	20.000 ns	300.000 ns	10.000 ns	10.528 ns	11.999 ns	41800	Fail
11	\$DA	Rise time of SDA signal	20.000 ns	300.000 ns	37.999 ns	39.210 ns	41.999 ns	9300	Pass
12	10A	Fall time of SDA signal	20.000 ns	300.000 ns	4.000 ns	6.714 ns	10.000 ns	9900	Fail
13	teur	Bus free time between a STOP and START condition	-	-	-	-	-	0	-
14	IVD,DAT	Data valid time	-	900.000 ns	98.000 ns	267.062 ns	1.068 us	15750	Fail
15	TVDLACK	Data valid acknowledge time		900.000 ns	98.000 ns	623.009 ns	1.068 us	1500	Fail

Dedicated page for Electrical Validation:



- Different Speed Mode including Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
- 2. Frequency: Clock speed
- 3. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 4. Voltage: V_IL, V_IH, etc.



I2C Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

Settings		Import	Export
→General XDecode	Channel Settings		
TriggerValidation	SCL: DSO Channel 1 ▼ Probe Settings: x10 ▼ SDA: DSO Channel 2 ▼ Probe Settings: x10 ▼		
	Working Voltage(V₀₀): 3.30 V ♀ Speed Mode		
	 Standard Mode (Max: 100Kbit/s) Fast Mode (Max: 400Kbit/s) 		
	Fast Mode + (Max: 1Mbit/s) High Speed Mode (Max: 3 4Mbit/s) Ch Value= 100of (Max) *		
	Customized Speed 100 Kbit/s		
Default		[Next

2. Decode Settings: I2C decoding settings

Sattingo		Import	Export
✓General	Address Mode		
 Decode Trigger Validation 	 7-bit Addressing 8-bit Addressing (Including R/W in Address) 10-bit Addressing 		
Default		Previous	Next



3. Trigge	r Settings: I2C Address, Data trigger condition		
Settings VGeneral			
 ✓Decode 	Trigger Settings		
 Trigger 	7-bit Address: XXh		
×Validation	Write/Read: 💌		
	ACK/NACK		
	Data		
	Any Offset Fixed Offset		
	0 Bytes		
	Value		
	XXh		
Default		Previous	Next

4. Electrical validation settings: Voltage, timing, frequency limitation

code	Customized E	V Parameter:				
gger idation						
lauton	Name	Description	Min	Max		
	1 ✔ f _{SCL} SCL c	lock frequency	0 kHz	100 kHz		
	Time					
	Name	Description	Min	Max		
	1 ✓ t _{HD,STA}	Hold time(repeated) START condition	4 us	X		
	2 ✓ t _{SU,STA}	Set-up time for a repeated START condition	4.7 us	X		
	3 🗸 t _{HD,DAT}	Data hold time	5 us	Х		
	4 ✓ t _{SU,DAT}	Data Set-up time	250 ns	X		
	5 🗸 t _{SU,STO}	Set-up time for STOP condition	4 us	X		
	6 ✓ t _{LOW}	Low Period of the SCL Clock	4.7 us	X		
	7 🗸 t _{HIGH}	High Period of the SCL Clock	4 us	x		
	8 🗸 t _{rCL}	Rise time of SCL signal	X	1 us		
	9 ✓ t _{fCL}	Fall time of SCL signal	X	300 ns		
	10 ✓ t _{rDA}	Rise time of SDA signal	X	1 us		
	11 🗸 t _{fDA}	Fall time of SDA signal	X	300 ns		



20						
	Settings				Import Expo	
2S 11PI 13C 11PI RFFE 11PI SPMI	 ✓General ✓Decode ✓Trigger 	Customized EV	Parameter:			
MBus	Validation	⊿ Time				
		Name	Description	Min	Max	
ANT(N3232)		1 V tho,sta	Hold time(repeated) START condition	160 ns	X	
		2 ✓ t _{SU,STA}	Set-up time for a repeated START condition	160 ns	X	
		3 V tho,DAT	Data hold time	0 ns	X	
		4 ¥ tsu,DAT	Data set-up time	10 ns	X	
		5 V t _{SU,STO}	Set-up time for STOP condition	160 ns	/0 ns	
				Liow Period of the SCL Clock	100 ns	A
		7 V THIGH		00 ns	40 ns	
		8 V GCH	Rise time of SCLH signal	10 ns	40 ns	
		9 V HCLH	Partime of CDAU signal	10 ms	00 ms	
		10 V GDAH	Rise time of SDAH signal	10 ms	80 ns	
		11 V YDAH	Pur free time between a STOP and STAPT condition	TO IS	~ 	
		12 V t _{BUF}	Data valid time	×		
		1.3 V LVD,DAT	Data valid ume	×	^ 	
		14 V LVD,ACK	Clark extend time	~	25 mg	
			First right adde time of SCI signal after Sr and after ACK bit	^ 10 ns	20 ms	
		- Index sect	interning edge time of occulginal director and alter Horbit	10110	00115	
		Voltage				

The 16th option can only been seen while the I²C speed mode is selected to **High Speed Mode**.



5. Software electrical validation interface:



6. Software electrical validation control panel:



7. Overview Report:

	lalaraa Maraana
Name Description Limit Min Limit Max Min Mean Max andard Deviatic Count Res	lt 🔺
1 fsc. SCL clock frequencey 0.000 Hz 100.000 KHz 99.994 KHz 99.998 KHz 100.004 KHz 11.000 Hz 480 Fail	
2 telosta Hold time(repeated) START condition 4.000 us 2.499 us 3.094 us 4.999 us 1.817 us 21 Fail	
3 tsusta Set-up time for a repeated START condition 0	
4 troux Data hold time 5.000 us 2.497 us 2.498 us 1.118 ns 146 Fail	
5 tsutar Data Set-up time 250.000 ns 2.499 us 2.499 us 2.499 us 722.000 ps 154 Pass	
6 tsusto Set-up time for STOP condition 4.000 us 2.498 us 3.450 us 4.998 us 1.987 us 21 Fail	
7 tow Low Period of the SCL Clock 4.700 us 4.998 us 4.998 us 4.999 us 1.947 ns 480 Pass	
8 teace High Period of the SCL Clock 4.000 us 4.998 us 4.999 us 4.999 us 1.862 ns 480 Pass	
9 to. Rise time of SCL signal 1.000 us 1.223 ns 1.587 ns 2.065 ns 2.050 ns 561 Pass	
	<u> </u>



8. Detail Report:

1	500 mV -3.50		2 500 mV -3.50		3 500 mV -3.50	/	4 500 r -3.50	nV	H 10 -40	0 µs)0 µs Т	I2C Validation	n 500 MS/s	
	ու ու ու ու ու ու ու ու	alanda 🔤											later and
	a an												hikirinin
								******					·····! ·
12C		Addr(7	b):12	10	20	30 , <mark>A</mark> ,	Addr(7b):3F		A, Addr(7	b):46 j	21	3A <mark>A</mark> .	
					· · · · · · · · · · · · · · · · · · ·								
1													
1													
Oven	view Deta	ail I2C											
Oven f _{SCL}	view Deta	ail I2C t _{su,sta} t _i	1D,DAT t _{SU,DA}	r t _{su,sto}	t _{LOW} t _{HIGH}	i t _{rcl} t _{rc}	:L t _{rDA} 1	IDA t _{BUF}	t _{vd,dat} t _{vd}		V _{B1}		
Oven f _{SCL} W	view Deta t _{HD,STA} /aveform No.	ail I2C t _{SU,STA} t _i TimeStamp	ID,DAT tsu,da Status	r t _{SU,STO} Address	t _{LOW} t _{HIGH} D0-D7	t _{rCL} t _{rC} t _{rC}	Limit Max	IDA t _{BUF}	t _{VD,DAT} t _{VD} Mean	ACK VIL Max	V _{IH} Count	Result	
Oven f _{SCL} W 1 1 2 1	view Deta t _{HD,STA} /aveform No.	iil I2C t _{SU,STA} t _i TimeStamp 49.982 ns 239.359 ns	ID.DAT tSU.DA Status START START	r t _{su,sto} Address 12 3F	t _{LOW} t _{HIGH} D0-D7 10 20 30	t _{rCL} t _K Limit Min 0.000 Hz 0.000 Hz	L t _{rDA} 1 Limit Max 100.000 KHz 100.000 KHz	юда t _{виг} Min 99.996 KHz 99.997 KHz	t _{VD,DAT} t _{VD} Mean 99.998 KHz 99.998 KHz	лск V _{IL} Мах 100.000 KHz 100.001 KHz	V _{IH} Count 32 16	Result Pass Fail	
Oven f _{SCL} W 1 1 2 1 3 1	view Deta t _{HD,STA} aveform No.	ail 12C t _{SU,STA} t ₁ TimeStamp 49.982 ns 239.359 ns 337.484 ns	ID.DAT tsu.DA Status START START START	T t _{su,sto} Address 12 3F 46	tLow tHIGH D0-D7 10 20 30 00 21 3A	t _{roL} t _r Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	Limit Max 100.000 KHz 100.000 KHz 100.000 KHz	арда t _{виг} Min 99.996 KHz 99.997 KHz 99.997 KHz	t _{VD,DAT} t _{VD} Mean 99.998 KHz 99.998 KHz 99.998 KHz	ACK V _E Max 100.000 KHz 100.001 KHz 100.000 KHz	V _⊮ Count 32 16 24	Result Pass Fail Pass	
Oven f _{SCL} W 1 2 3 4	view Deta	il I2C t _{SU,STA} t _i TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns	HD.DAT tSU.DA Status START START START START START	r t _{SU,STO} Address 12 3F 46 3F	tLow tHIGH D0-D7 10 20 30 00 21 3A 00	t _{rcL} t _r Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} 1 Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	ырда t _{виг} Min 99.996 KHz 99.997 KHz 99.997 KHz 99.994 KHz	t _{VD,DAT} t _{VD} Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	ACK V _{IL} Max 100.000 KHz 100.001 KHz 100.000 KHz 100.002 KHz	V _{IH} Count 32 16 24 16	Result Pass Fail Fail Fail	
Oven f _{SCL} W 1 2 3 4 5	view Deta t _{HD,STA}	ail 12C t _{SU,STA} t _i TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns	IDDAT TUDAT Status START START START START START	r t _{SU,STO} Address 12 3F 46 3F 46	tLOW tHBH D0-D7 10 20 30 00 21 3A 00 21 3A	t _{rCL} t _R Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	Min 99.996 KHz 99.997 KHz 99.997 KHz 99.994 KHz 99.995 KHz	t _{VD.DAT} t _{VD} Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	ACK VIL Max 100.000 KHz 100.001 KHz 100.000 KHz 100.002 KHz 100.000 KHz	V _{int} Count 32 16 24 16 24 24	Result Pass Fail Pass Fail Pass	*
Over f _{SCL} W 1 2 3 4 5 6	view Deta t _{HD.STA} aveform No.	ail I2C t _{SU,STA} t _i TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns	ID.DAT TUDA Status START START START START START START	tsu.sto Address 12 3F 46 3F 46 12	tLOW tHIGH D0-D7 10 20 30 00 21 3A 00 21 3A 10 20 30	t _{rCL} t _K Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} 1 Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	Min 99.996 KHz 99.997 KHz 99.997 KHz 99.997 KHz 99.995 KHz 99.996 KHz	tvp.p.ar tvp Mean 99.998 KHz 99.998 KHz 99.998 KHz	ACK VL Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.001 KHz	V _{B1} Count 32 16 24 16 24 32	Result Pass Fail Pass Fail Pass Fail	*
Over f _{SCL} W 1 2 3 4 5 6 7	view Detet	II I2C tsusst tr TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 148.108 ns 49.982 ns 239.358 ns	ID.DAT touda Status START START START START START START START	r t _{SU,STO} Address 12 3F 46 3F 46 12 3F	tLOW tHIGH D0-D7 10 20 30 00 21 3A 10 20 30 00 21 3A 10 20 30 00	t,cL tg Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} 1 Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	taur Min 99.996 KHz 99.997 KHz 99.997 KHz 99.995 KHz 99.995 KHz 99.996 KHz 99.996 KHz 99.996 KHz 99.996 KHz	tvo.bar tvo Mean 99.998 KHz 99.998 KHz 99.998 KHz	ACK VL Max 100.000 KHz 100.001 KHz 100.000 KHz 100.002 KHz 100.000 KHz 100.001 KHz 100.001 KHz	V _{int} Count 32 16 24 16 24 32 16 32 16	Result Pass Fail Pass Fail Fail Fail	
Oven fscL W 1 1 2 1 3 1 4 2 5 2 6 3 7 3 8 3	view Deta t _{HD.STA} aveform No.	II I2C tsUJSTA tr TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 239.358 ns 239.358 ns 337.484 ns	ID.DAT TUUDAT START START START START START START START START START	tsu.sto Address 12 3F 46 3F 46 12 3F 46 3F 46 3F 46 46 3F 46 3F 46	tLow tHIGH D0-D7 10 20 30 00 21 3A 00 21 3A 10 20 30 00 21 3A	t _{rCL} t _R Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	taur Min 99.996 KHz 99.997 KHz 99.997 KHz 99.997 KHz 99.997 KHz 99.996 KHz 99.996 KHz 99.996 KHz 99.996 KHz 99.995 KHz 99.995 KHz	t _{VD.DAT} t _{VD} Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	Ack VL Max 100.000 KHz 100.000 KHz 100.000 KHz 100.002 KHz 100.001 KHz 100.001 KHz 100.001 KHz	V _{B1} Count 32 16 24 16 24 32 16 24 32 16 24 32 24 24	Result Pass Pass Pass Fail Pass Fail Fail Fail	A

9. Reference Point Dialog & Waveform:







Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	24554
Test Date	04-17-2023 14:46:14
S/W Version	1.0.25
Protocol	12C
/*************************************	,

Overview Results:

Total: 17 Pass: 9 Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f _{SCL}	SCL clock frequency	0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%	×Fail
2	t _{hd,sta}	Hold time(repeated) START condition	4.000 us		1.538 us	1.538 us	1.539 us	427.000 ps	20	-61.6%		×Fail
3	t _{su,sta}	Set-up time for a repeated START condition	4.700 us		2.013 us	2.014 us	2.015 us	579.000 ps	10	-57.2%		×Fail
4	t _{hd,dat}	Data hold time	5.000 us		94.249 ns	247.342 ns	1.026 us	4.244 us	1575	-98.1%		×Fail
5	t _{SU,DAT}	Data Set-up time	250.000 ns		472.837 ns	1.187 us	1.443 us	5.255 us	1767	18.7%		✓Pass
6	t _{SU,STO}	Set-up time for STOP condition							0			
7	t _{LOW}	Low Period of the SCL Clock	4.700 us		1.539 us	1.541 us	1.543 us	9.208 ns	2670	-67.3%		×Fail
8	t _{HIGH}	High Period of the SCL Clock	4.000 us		977.699 ns	979.666 ns	984.826 ns	20.914 ns	3040	-75.6%		×Fail
9	t _{rCL}	Rise time of SCL signal		1.000 us	45.022 ns	48.118 ns	49.835 ns	14.531 ns	3430		0.5%	✓Pass
10	t _{fCL}	Fall time of SCL signal		300.000 ns	9.888 ns	10.237 ns	10.583 ns	1.448 ns	3430		0.2%	✓Pass
11	t _{rDA}	Rise time of SDA signal		1.000 us	37.719 ns	39.529 ns	41.848 ns	5.148 ns	927		0.4%	✓Pass
12	t _{fDA}	Fall time of SDA signal		300.000 ns	4.616 ns	6.893 ns	9.828 ns	24.035 ns	947		1.8%	✓Pass
13	t _{BUF}	Bus free time between a STOP and START condition							0			
14	t _{VD,DAT}	<u>Data valid time</u>		3.450 us	98.898 ns	270.164 ns	1.067 us	4.200 us	1585		28.9%	✓Pass
15	t _{VD,ACK}	Data valid acknowledge time		3.450 us	141.017 ns	730.257 ns	1.067 us	1.344 us	91		28.0%	✓Pass
16	VIL	Low-level input voltage	-500.000 mV	990.000 mV	-105.670 mV	27.063 mV	104.081 mV	760.863 mV	4367	26.5%	40.5%	✓Pass
17	VIH	High-level input voltage	2.310 V	3.800 V	3.225 V	3.267 V	3.417 V	1.250 V	4367	61.4%	74.3%	✓Pass

f_{SCL} - Test Result: Fail Description: SCL clock frequency

Limit Min Limit Max Min	Mean Max Star	dard Deviatio	n Count Margin M	in Margin Max				
0.000 Hz 100.000 KHz 387.586 KHz 3	87.683 KHz 387.769 KHz 437.	000 Hz	2670 387.6%	387.8%				
	Histografi		Value Danas	0				
Occurance (%), Total 2670			value Range	Occurance Co				
100 -			387.586 kHz ~ 387.604	kHz 9				
90 - 80 -			387.604 kHz ~ 387.623	kHz 23				
70 -			387.623 kHz ~ 387.641	kHz 84				
60 - 50 -			387.641 kHz ~ 387.659	kHz 395				
40 -			387.659 kHz ~ 387.677	kHz 539				
30 - 14.8 20.2	23.7 24.8		387.677 kHz ~ 387.696	kHz 632				
10 0.3 0.9 3.1	8.0	Test Value	387.696 kHz ~ 387.714	kHz 663				
387.586 KHz	387.7	69 KHz	387 714 kHz ~ 387 732	kHz 213				
Test Value			207 722 14 1- 207 754					
	387.586 KHz (387.6%) 387.769 H	<hz (387.8%)<br="">⊣ ∦</hz>	387.732 KHZ ~ 387.751					
Limit 0.000 Hz	100.0	000 KHz	387.751 kHz ~ 387.769	kHz 18				
Min	Detail Report	Row: 12, Tes	t Index: 197 Ma	X			Detail Report	Row: 10, Test Index: 82
500 mV 2 500 mV 3 500 mV -3.50 2 -3.50 3 -3.50	400 ns -3.50 Η -730.2 μs Τ	I2C Validation Stop S/R: 500 M	<u>15/s</u>	500 mV -3.50 2 500 -3.5	mV 3 500 mV 0 3 -3.50	500 mV -3.50 H	400 ns -345.866 µs 🔳	I2C Validation Stop S/R: 500 MS/s
							/	
		de la facta de	···i ···i ···i ···i ···i ···i ···i					
4		197			8	-		
	62		120			7E		
						-		



I2S Electrical Validation Solution

Introduction:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

Use an oscilloscope to do I2S Electrical Validation to ensure that the I2S meets the defined specification. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test.

I²S (Inter-IC Sound) is a standard electrical serial bus interface used for connecting digital audio devices, such as audio codecs, digital-to-analog converters (DACs), and analog-to-digital converters (ADCs). It is commonly used in embedded systems, audio processors, and high-quality audio equipment.

I²S is a straightforward but powerful interface for transmitting digital audio data between devices with high precision and low latency.



I2S Electrical Validation Settings:

1. General Settings:

Settings								Import	Export
General									
XDecode	Channel	Settings							
XTrigger	Mode:	I2S -							
×Validation	SCK:	DSO Channel 1 🔻	Probe Settings:	x10 💌	×10	⇒-			
	WS:	DSO Channel 2 🔻	Probe Settings:	x10 👻	×10	⇒-			
	SD:	DSO Channel 3 🔻	Probe Settings:	x10 👻	×10	⇒-			
	Working	g Voltage(V _{DD}): 3.30 V	*						
	Data R	ate 2.50 MHz	1.0						
	Datarta								

In the General Settings section, it is mandatory to setup the bus configuration, including I2S mode type (I2S, Left Justified, PCM, TDM), the channel settings, working voltage and the data rate of I2S.



2. Decode Settings:

Settings						Import	Export
✓General	Data Format						
TriggerValidation	Bit Order Data Bits	MSB First 16 bits	▼ ◆				

In the Decode Settings, it requires user to setup the I2S data format. Bit order is either MSB First or LSB First. Data Bits can be set in a range of 1-32 bit(s).



3. Trigger Settings:

Settinas					Import	Export
 ✓General ✓Decode 	Data					
 Trigger Validation 	Method Channel Pattern	Data Match				
	Duration	1 frame(s)				
Default					Previous	Next

Set up the data pattern that user expect to trigger on. The data format is set on the previous decode page. The remaining setup is all about the data pattern. Here we provide **Data Match**, **Rising**, **Falling**, **Glitch**, **Mute**, and **Clip**, 6 trigger methods in total.



4. Validation Settings:

✓ Custor	nized EV	Parameter:		
⊿ Fre	equen	су		
Na	me	Description	Min	Max
1 🗸	f _{sck} SCk	Frequency	2.25 MHz	2.75 MHz
📕 Tin	ne			
	Name	Description	Min	Max
1 🗸	t _{HC}	SCK High Period	140 ns	X
2 🗸	t _{LC}	SCK High Period	140 ns	x
3 🗸	t _R	SCK Rise Time	X	60 ns
4 🗸	t _F	SCK Fall Time	Х	60 ns
5 🗸	t _{d,SCKWS}	SCK-WS Delay Time	X	320 ns
6 🗸	t _{d,SCKSD}	SCK-Data Delay Time	X	320 ns
7 🗸	t _{dutySCK}	SCK Duty Cycle	X	x
8 🗸	t _{s,WS}	WS Setup Time	X	80 ns
9 🗸	t _{h,WS}	WS Hold Time	0 ns	х
10 🗸	t _{dutyWS}	WS Duty Cycle	X	x
11 🗸	t.sn	Data Setup Time	x	80 ns

This section displays 3 characteristics table, including

- 1. Frequency
- 2. Timing Parameters
- 3. Voltage requirements

The default values are referenced from the I2S specification rev3.0. All supported validation parameters' symbols and description are listed in the table below.

• I2S Frequency Requirements

Symbol	Electrical Parameter
f _{scк}	SCK Clock Frequency

• I2S Timing Requirements

Symbol	Electrical Parameter
t _{HC}	SCK High Period
t _{LC}	SCK Low Period
t _R	SCK Rise Time
t _F	SCK Fall Time
t _{d,SCKWS}	SCK-WS Delay Time



t _{duty} ,scк	SCK Duty Cycle
t _{s,WS}	WS Setup Time
t _{h,WS}	WS Hold Time
t _{duty,WS}	WS Duty Cycle
t _{s,SD}	Data Setup Time
t _{h,SD}	Data Hold Time

• I2S Voltage Requirements

Symbol	Electrical Parameter
VL	Low-Level Voltage
V _H	High-level Voltage

5. Software electrical validation interface:

1	2 V +1.53			2	2 V -0.97				3 2 V -3.50		Н 20 µs -80 µs	I2S Validation Stop S/R: 250 MS/s
1												
2	dite de te dite de te	inini i portano portan		n hhnh i i i i i i i i i i i i i i i i i i		h hine shi h Li piri piripi Li piri piripi				، ، ، ، ، ، ، ، ، ، ، ، ، ، ، ، ، ، ،	111 PD 11913 A 11 P 4	n 11 bini 11 bini 11 bini 11 bini 12 bin mpada 11 bini 12 bini 1
3											+ ++ ++	
Ove	Timestamp	D0	D1	D2	D3	D4	DS	D6	D7	Information		
1 0	s									Sample Rate: 1.25 MHz - 16 bit		
2 0	s									IDLE		
3 3	.6 µs	L:0000	R:0000	L:E000	R:8000	L:8000	R:E000	L:0000	R:0000			
4 8	.6 µs	L:0000	R:0000	L:0000	R:8000	L:C000	R:8000	L:8000	R:E000			_
5 1	4.2 µs	L:0000	R:0000	L:0000	R:0000	L:1C00	R:C000	L:E000	R:0000			
6 2	1.4 µs	L:0000	R:1000	L:C000	R:C000	L:E000	R:0000	L:0000	R:0000			
7 2	7.8 µs	L:0000	R:0000	L:E000	R:C000	L:C000	R:8000	L:0000	R:0000			
8 3	4.2 µs	L:0000	R:0000	L:0000	R:8000	L:C000	R:C000	L:C000	R:8000			
9 3	9.8 µs	L:0000	R:0000	L:0000	R:0000	L:7000	R:C000	L:8000	R:8000			
10 4	5.4 µs	L:8000	R:0000	L:0000	R:0000	L:0000	R:4000	L:C000	R:C000			
11 5	1 µs	L:8000	R:8000	L:8000	R:0000	L:0000	R:0000	L:0000	R:0000			



6. Software electrical validation control panel:



- Stop Conditions: Stop when acquired X times Stop when Result Fail > X times
- 2. Information: Select waveform
- 3. Save File: Save as Html Save as .MOW(Software format)

7. Overview Report:

+1.53			2	! V 0.97			3 2 V -3.50						H 4	0µs 80µs	T I2S Valid Stop S/	ation R: 250 MS/s
1																
2	a Alain () () () () () () () () () ()	ne per per per		a ha ha ina ha ha Ya ya				┝┝╸┝╽┍┝┝┝ ┝		ן אות קו ליקע האוקא איז לייקע אות אות איז	i ni ni ni ni ni ni ni ni ni ni ni ni ni ni ni ni ni n	, or of the second s	6 m ²			
12S	anditi anditi anditi						inter Dil Di R () n									
Overview	Detail I2S															
_																
Name	Description	Limit Min	Limit Max	Min	Mean	Max 2 990 ns	indard Deviat	i Count	Result							
Name 1 tk 2 tasckws	Description SCK Rise SCK-WS	Limit Min	Limit Max 60.000 ns 320.000 ns	Min 1.639 ns 201.556 ns	Mean 2.062 ns 202.420 ns	Max 2.990 ns 203.654 ns	andard Deviat	i Count 2994 1390	Result Pass Pass	-						
Name 1 ls 2 t_LSCKWS 3 t_LSCKSD	Description SCK Rise SCK-WS SCK-Data	Limit Min	Limit Max 60.000 ns 320.000 ns 320.000 ns	Min 1.639 ns 201.556 ns 201.759 ns	Mean 2.062 ns 202.420 ns 202.758 ns	Max 2.990 ns 203.654 ns 203.957 ns	indard Deviat 442.000 ps 602.000 ps 713.000 ps	i Count 2994 1390 375	Result Pass Pass Pass							
Name 1 tk 2 t_LSCKWS 3 t_LSCKSD 4 t_LWS	Description SCK Rise SCK-WS SCK-Data WS Setup	Limit Min 	Limit Max 60.000 ns 320.000 ns 320.000 ns 80.000 ns	Min 1.639 ns 201.556 ns 201.759 ns 196.354 ns	Mean 2.062 ns 202.420 ns 202.758 ns 197.580 ns	Max 2.990 ns 203.654 ns 203.957 ns 198.443 ns	indard Deviat 442.000 ps 602.000 ps 713.000 ps 599.000 ps	i Count 2994 1390 375 1377	Result Pass Pass Pass Fail							
Name 1 Ik 2 LSCKWS 3 LSCKSD 4 LWS 5 ELWS	Description SCK Rise SCK-WS SCK-Data WS Setup WS Hold T	Limit Min 0.000 ps	Limit Max 60.000 ns 320.000 ns 320.000 ns 80.000 ns 	Min 1.639 ns 201.556 ns 201.759 ns 196.354 ns 197.274 ns	Mean 2.062 ns 202.420 ns 202.758 ns 197.580 ns 198.316 ns	Max 2.990 ns 203.654 ns 203.957 ns 198.443 ns 199.035 ns	indard Deviat 442.000 ps 602.000 ps 713.000 ps 599.000 ps 269.000 ps	i Count 2994 1390 375 1377 1390	Result Pass Pass Pass Fail Pass							
Name 1 lx 2 t_scc.ws 3 t_scc.ws 4 t_sws 5 t_sws 6 t_ssc	Description SCK Rise SCK-WS SCK-Data WS Setup WS Hold T Data Setu	Limit Min 0.000 ps 	Limit Max 60.000 ns 320.000 ns 320.000 ns 80.000 ns 80.000 ns	Min 1.639 ns 201.556 ns 201.759 ns 196.354 ns 197.274 ns 196.039 ns	Mean 2.062 ns 202.420 ns 202.758 ns 197.580 ns 198.316 ns 197.265 ns	Max 2.990 ns 203.654 ns 203.957 ns 198.443 ns 199.035 ns 198.283 ns	Indard Deviat 442.000 ps 602.000 ps 713.000 ps 599.000 ps 269.000 ps 708.000 ps	i Count 2994 1390 375 1377 1390 375	Result Pass Pass Pass Fail Pass Fail							
Name 1 tr. 2 tasckws 3 tasckws 4 tass 5 taws 6 tass 7 tass	Description SCK Rise SCK-WS SCK-Data VS Setup VS Hold T Data Setu Data Hold	Limit Min 0.000 ps 0.000 ps	Limit Max 60.000 ns 320.000 ns 320.000 ns 80.000 ns 80.000 ns 	Min 1.639 ns 201.556 ns 201.759 ns 196.354 ns 197.274 ns 196.039 ns 197.737 ns	Mean 2.062 ns 202.420 ns 202.758 ns 197.580 ns 198.316 ns 197.265 ns 198.588 ns	Max 2.990 ns 203.654 ns 203.957 ns 198.443 ns 199.035 ns 198.283 ns 199.651 ns	Indard Deviat 442.000 ps 602.000 ps 713.000 ps 599.000 ps 269.000 ps 708.000 ps 295.000 ps	i Count 2994 1390 375 1377 1390 375 375	Result Pass Pass Pass Pass Pass Pass Pass Pas							



8. Detail Report:

1	2 V +1.53			2 V -0.97				3 2 V -3.50						H 20 µs -80 µ	3 IS	I2S Vali Stop S	dation I/R: 250 M	<u>5/s</u>	
1																			
2	ани ра <u>А</u> ААМАА ст. у рази у у Эр	64 144 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				╴┝┝┷┝╴┝╵ ┿		┍┙┥┥┍┍┙┥ ╷╷╷╷┯┑┑			"				1999 19 19 19 19 19 19 19 19 19 19 19 19 19 1				
12S		uniti (CEE)					internet (1997) internet (1997) intern		2000 000 0000 				240 000 00 9+1+11		L R L	R. L.O. L			
Over	view Detail	128	1. T																
Over	view Detail t _{d.SCKWS}	I2S t _{d.SCKSD} t _{s.V}	s t _{hws}	t _{s.SD} t _{h.SD}	Limit Max	Min	Mean	Max	Count	Result									
Over t _R	view Detail t _{d.SCKWS} 1 Waveform No 1-1	I2S t _{d,SCKSD} t _{s,V} TimeStamp 300.000 ns	rs t _{huvs} Data R: 8000	t _{s.SD} t _{h.SD} Limit Min	Limit Max 60.000 ns	Min 1.719 ns	Mean 1.719 ns	Max 1.719 ns	Count	Result Pass									
Over t _R 1 2	view Detail t _{4.SCKWS} Waveform No 1-1 1-2	12S t _{dSCKSD} t _{s.V} TimeStamp 300.000 ns 350.000 ns	s t _{ruvs} Data R: 8000 L: 8000	t _{s.SD} t _{h.SD} Limit Min	Limit Max 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns	Mean 1.719 ns 1.707 ns	Max 1.719 ns 1.707 ns	Count 1 1	Result Pass Pass									*
Over t _R 1 2 3	View Detail t _{4.SCKWS} Waveform No 1-1 1-2 1-3	I2S t _{d.SCKSD} t _{e.V} TimeStamp 300.000 ns 350.000 ns 450.000 ns	thws Data Data R: 8000 L: 8000 R: 8000	t _{s.SO} t _{h.SO} Limit Min 	Limit Max 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns	Mean 1.719 ns 1.707 ns 1.707 ns	Max 1.719 ns 1.707 ns 1.707 ns	Count 1 1 1	Result Pass Pass Pass									
Over t _R 1 2 3 4	View Detail t ₄₅₀₀₀₀ 1 Waveform No 1-1 1-2 1-3 1-4	I2S tdsCxSD text TimeStamp 300,000 ns 350,000 ns 450,000 ns 550,000 ns	Image: state	Limit Min	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns	Count 1 1 1 1 1	Result Pass Pass Pass Pass									×
Over t _R 1 2 3 4 5	View Detail t _{4SCKWS} Waveform No 1-1 1-2 1-3 1-4 1-5	12S t _{4.5CK50} t _{s.V} TimeStamp 300.000 ns 350.000 ns 450.000 ns 550.000 ns 650.000 ns	thuss thuss Data R: 8000 L: 8000 L: 8000 R: 8000 R: 8000 R: 8000 R: 8000	t _{s.SD} t _{h.SD} Limit Min 	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.709 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns	Count 1 1 1 1 1 1	Result Pass Pass Pass Pass Pass Pass									*
Over t _R 1 2 3 4 5 6	View Detail t_scows 1 1-1 1 1-2 1 1-3 1 1-4 1 1-5 1	I2S t _{dSOND} t _{eV} TimeStamp 300.000 ns 350.000 ns 450.000 ns 450.000 ns 550.000 ns 650.000 ns 750.000 ns	tws Data R: 8000 I: L: 8000 I: R: 8000 I: L: 8000 I: L: 8000 I: L: 8000 I:	t _{s.SD} t _{h.SD}	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.709 ns 1.719 ns 1.719 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.709 ns 1.719 ns 1.727 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.719 ns 1.743 ns	Count 1 1 1 1 1 1 1 4	Result Pass Pass Pass Pass Pass Pass Pass									×
Over t _R 1 2 3 4 5 6 7	View Detail t ₄₅₀₀₀₀₅ 1 Waveform No 1-1 1-2 1-3 1-4 1-5 1-6 1-7	128 t _{d50050} t _{sV} TimeStamp 300.000 ns 350.000 ns 450.000 ns 550.000 ns 550.000 ns 650.000 ns 750.000 ns 1.150 us	tows tows Data R: 8000 L: 8000 R: 8000 R: 8000 R: 8000 L: 8000 R: 8000 L: 8000 R: 8000 R: 8000 R: 8000 R: 8000 R: 8000	tSO th.SO Limit Min 	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.709 ns 1.719 ns 1.719 ns 1.743 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.709 ns 1.719 ns 1.727 ns 1.743 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.743 ns 1.743 ns	Count 1 1 1 1 1 1 1 4 1	Result Pass Pass Pass Pass Pass Pass Pass Pas									*
Over t _R 1 2 3 4 5 6 7 8	view Detail t_sscwa 1 Waveform No 1-1 1-2 1-3 1-4 1-5 1-6 1-7 1-8 1-8	I2S tasceso t _{ext} TimeStamp 300.000 ns 350.000 ns 550.000 ns 550.000 ns 550.000 ns 150.000 ns 1.150 us 1.250 us 1.250 us	tuwe Data R: 8000 L: 8000 L: 8000 R: 8000 L: 8000 R: 8000 L: 0000	t50 th.50 Limit Min -	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.709 ns 1.719 ns 1.743 ns 1.730 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.719 ns 1.727 ns 1.743 ns 1.730 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.743 ns 1.730 ns	Count 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Result Pass Pass Pass Pass Pass Pass Pass Pas									*
Over t _R 1 2 3 4 5 6 6 7 8 9	New Detail Lacovs 1 Waveform No 1 1-2 1 1-3 1 1-4 1 1-5 1 1-6 1 1-7 1 1-8 1 1-9 1	128 taccoso tav 300.000 ns 350.000 ns 550.000 ns 650.000 ns 1.150 us 1.250 us 1.350 us	s t _t ws Data Data R: 8000 L: 8000 L: 8000 R: 8000 L: 0000 R: 0000 L: 0000 R: 0000	t_s50 t_s50 tumit Min	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.719 ns 1.719 ns 1.719 ns 1.730 ns 1.730 ns 1.719 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.727 ns 1.743 ns 1.730 ns 1.719 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.743 ns 1.730 ns 1.719 ns	Count 1 1 1 1 1 1 4 4 1 1 1 1 1 1 1	Result Pass Pass Pass Pass Pass Pass Pass Pas									
Over t _R 1 2 3 4 5 6 7 8 9 9 10	Hew Detail Lacovs 1 Waveform No 1 1-2 1 1-3 1 1-4 1 1-5 1 1-6 1 1-7 1 1-8 1 1-9 1	128 tacceso tay TimeStamp 300.000 ns 350.000 ns 550.000 ns 750.000 ns 1.150 us 1.250 us 1.350 us 1.450 us	s t.ws Data R: 8000 R: 8000 R: 8000 R: 8000 R: 8000 R: 0000 R: 0000 R: 0000 R: 0000	4,50 4,59 Elimit Min 	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.719 ns 1.719 ns 1.730 ns 1.730 ns	Mean 1,719 ns 1,707 ns 1,707 ns 1,707 ns 1,707 ns 1,719 ns 1,727 ns 1,743 ns 1,730 ns 1,719 ns 1,730 n	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.743 ns 1.730 ns 1.719 ns 1.730 ns	Count 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Result Pass Pass Pass Pass Pass Pass Pass Pas									*
Over t _R 1 2 3 4 5 6 7 8 9 10 11	Vev Detail t ₄₅₀₀₀₅ 1 Vaveform No 1-1 1-2 1-3 1-4 1-5 1-6 1-7 1-8 1-9 1-1 1-9 1-1 1-1 1-1 1-1 1-1	128 tasces task TimeStamp 300.000 ns 350.000 ns 550.000 ns 550.000 ns 150.000 ns 1.50 us 1.250 us 1.350 us 1.450 us 1.550 us	 t.ws Data Data R: 8000 L: 8000 R: 8000 L: 8000 R: 8000 L: 0000 R: 0000 L: 0000 R: 0000 L: 0000 R: 0000 R: 0000 R: 0000 R: 0000 	t_500 t_500 timit Min ac ac	Limit Max 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.719 ns 1.719 ns 1.730 ns 1.730 ns 1.730 ns 1.730 ns 1.730 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.727 ns 1.723 ns 1.730 ns 1.730 ns 1.730 ns 1.730 ns 1.730 ns 1.730 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.743 ns 1.743 ns 1.743 ns 1.730 ns 1.719 ns 1.730 ns 1.719 ns 1.730 ns 1.719 ns	Count 1 1 1 1 1 1 1 4 1 1 1 1 1 1 1	Result Pass Pass Pass Pass Pass Pass Pass Pas									*
Over t _R 1 2 3 4 5 6 7 8 9 10 11 12	Veve Detail t_sscows 1 Vaveform No 1-1 1-2 1-3 1-3 1-4 1-5 1-6 1-7 1-8 1-9 1-10 1-11 1-12	128 tasces task TimeStamp 300.000 ns 350.000 ns 550.000 ns 550.000 ns 150.000 ns 1.50.000 ns 1.250 us 1.350 us 1.450 us 1.450 us 1.550 us 1.650 us	tunes Data R: 8000 L: 8000 R: 8000 L: 8000 L: 8000 L: 0000 R: 0000 L: 0000 R: 0000 L: 0000 L: 0000 L: 0000 L: 8000	L.SO L.SO Limit Min	Limit Max 60.000 ns 60.000 ns	Min 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.719 ns 1.719 ns 1.730 ns 1.730 ns 1.730 ns 1.719 ns 1.730 ns	Mean 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.727 ns 1.727 ns 1.730 ns 1.730 ns 1.730 ns 1.719 ns 1.730 ns	Max 1.719 ns 1.707 ns 1.707 ns 1.707 ns 1.707 ns 1.719 ns 1.743 ns 1.730 ns	Count 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Result Pass Pass Pass Pass Pass Pass Pass Pas									

9. Reference Point Dialog & Waveform:





10. Html Report:



Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 13:34:37
S/W Version	1.8.62
Protocol	12S

Overview Results:

Total:	7
Pass:	5
Fail:	2

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	t _R	SCK Rise Time		60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994		-95.0%	✓Pass
2	t _{d,SCKWS}	SCK-WS Delay Time		320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390		-36.4%	✓Pass
3	t _{d,SCKSD}	SCK-Data Delay Time		320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375		-36.3%	✓Pass
4	t _{s,WS}	WS Setup Time		80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377		148.1%	× Fail
5	t _{h,WS}	WS Hold Time	0.000 ps		197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390			✓Pass
6	t _{s,SD}	Data Setup Time		80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375		147.9%	≍ Fail
7	t _{h,SD}	Data Hold Time	0.000 ps		197.737 ns	198.588 ns	199.651 ns	295.000 ps	375			✓Pass

t_R - Test Result: Pass Description: SCK Rise Time

Limit Min Limit Max Min Mean Max Standard Devia	tion Count Margin Min Margin M	ax		
Histogram	2994			
Occurance (%),Total 3493	Value Range	Occurance Count		
100 -	1.639 ns ~ 1.774 n	1283		
90 -	1.774 ns ~ 1.909 n	578		
70 -	1.909 ns ~ 2.044 n	\$ 439		
60 - 50 -	2.044 ns ~ 2.179 n	\$ 210		
40 - 36.7	2.179 ns ~ 2.314 n	84		
30 - 16.5 20 - 16.5 12.6	2.314 ns ~ 2.450 n	\$ 80		
10 <u>6.0</u> 2.4 2.3 3.2 4.2 4.8	Test Value 2.450 ns ~ 2.585 n	s 112		
1.639 ns	2.990 ns 2.585 ns ~ 2.720 n	147		
Test Value 1.639 ns 2.990 ns (-95.0%)	2.720 ns ~ 2.855 n	s 167		
Limit	60.000 ns 2.855 ns ~ 2.990 n	393		
Min Detail Rep	port Row: 1337, Test Index: 1	Max		Detail Report Row: 765, Test Index:
2 V +1.53 2 V -0.97 3 2 V -3.50 Η 1 ns -134.4 μs	T I2S Validation Stop S/R: 250 MS/s	2 V +1.53 2 V -0.97	3 2 V -3.50	1 ns -59.196 μs I2S Validation Stop <u>S/R: 250 MS/s</u>
	-			
				3
			++	······
	անութափուփոփոփոփոփոփոփո			
26 L:8000		125	R:E000	



MIPI I3C Electrical Validation Solution

Introduction:

File / Setting	s Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

MIPI I3C is backward compatible with many Legacy I²C Devices, but I3C Devices also support higher speed (with SCL clock speed up to 12.5 MHz) and new communication modes. MIPI I3C modes include **Single Data Rate (SDR) Mode**, **High Data Rate (HDR) Mode**. HDR Mode is also divided into **Dual Data Rate (HDR-DDR) Mode**, **Ternary Symbol Legacy Mode (HDR-TTL) Mode**, **Ternary Symbol Pure-bus (HDR-TSP) Mode**, and **Bulk Transport (HDR-BT) Mode**. MIPI I3C Electrical Validation offers various electrical measurements compliance testing as specified in the MIPI I3C Specification (currently supports MIPI I3C version 1.1.1).



MIPI I3C Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

		Import	Export
Settings			
 General Decede 	Channel Settings		
 Trigger Validation 	SCL: DSO Channel 1 Probe Settings: x10 SDA: DSO Channel 2 Probe Settings: x10	×10 =>	
	Working Voltage(V _{DD}): 1.80 V		
	 SDR: Single Data Rate Mode (Max: 12.5 Mbps) HDR-DDR: HDR Double Data Rate Mode (Max: 25 Mbps) 		
	 HDR-TSL: Tenary Symbol Legacy-inclusive-bus Mode (Max: 27.5 Mbps HDR-TSP: HDR Tenary Symbol for Pure-bus Mode (Max: 39.5 Mbps) HDR-BT: HDR Bulk Transport Mode)	
	O Customized Speed 400 Kbps		
	Bus Configuration		
	O Pure Bus: Only I3C devices are presented on the I3C Bus		
	Mixed Bus: At least one I2C Legacy Device is presented on the I3C Bus	s	
	Communicating with I2C Legacy Device		
	• Fast Mode (400 Kbps)		
	O Fast Mode+ (1 Mbps)		
Default		ſ	Next



In the General Settings section, the selection of Speed Mode determines a suitable sample rate for validation, but also affects the timing specification table in the validation settings section. For instance, in HDR-TSL and HDR-TSP Mode, there are additional timing specifications listed in the table.

13 ✔ t _{EDGE}	Edge-to-Edge Period	32 ns	х
14 🗸 t _{skew}	Allow Difference Between Signals for 'Simultaneous' Change	х	12.8 ns
15 ✔ t _{EYE}	Stable Condition Between Signals	12 ns	х
16 ✓ t _{SYMBOL}	Time Between Successive Symbols	32 ns	х
17 ✓ t _{с⊥оск}	Symbol Clock	77.5 ns	Х

Furthermore, the Bus Configuration section specifies the devices you connected on the I3C Bus. If it is a Pure-Bus setup, I²C timing table is thus not required, which is discussed in the Validation Settings section. On the other hand, a Mixed Bus setup will include the timing table for I²C Legacy Devices, and there default timing values are determined by using Fast Mode (Fm) or Fast Mode (Fm+) configuration, which is an identical settings to I²C Electrical Validation setup.



2. Decode Settings

		Import	Export
Settings			
✓General →Decode	Startup		
×Trigger	Startup in I2C mode		
XValidation	PEC Enabled		
	Startup in HDR-DDR mode		
Default		Previous	Next



3. Trigger Settings

o. #:			Import	Export
Settings VGeneral				
✓Decode	Trigger on			
Trigger	Address: XXh			
XValidation	O Common Command Code (CCC):	h, Any	T	
Default			Previous	Next

If you are interested in analyzing specific devices address, set the trigger address to the value you prefer. In the figure above, "XX" stands for don't care term. Thus, it triggers on all address in this case. It also provides triggering on Common Command Code (CCC), which is specified on the Broadcast Address 7'h7E.



4. Validation Settings

✓ Customized	EV Parameter:		
Freque	ency		
Name	Description	Min	Max
1 ✔ f _{SCL}	SCL Clock Frequency when communicating with I2C Legacy Devices	0 MHz	0.4 MHz
2 ✔ f _{SCL_PF}	SCL Clock Frequency	0.01 MHz	12.9 MHz
1 ✔ t _{su s}	TA Setup Time for a Repeated START	600 ns	x
1 ✓ t _{su s}	TA Setup Time for a Repeated START	600 ns	X
-			
2 ✓ t _{HD_5}	TA Hold Time for a (Repeated) START	600 ns	X
2 ✔ t _{HD_5} 3 ✔ t _{LOW}	TTA Hold Time for a (Repeated) START SCL Clock Low Period	600 ns 1300 ns	X X
2 ✔ t _{HD} 3 ✔ t _{LOW} 4 ✔ t _{DIG}	Hold Time for a (Repeated) START SCL Clock Low Period SCL Clock Low Period as seen at the receiver	600 ns 1300 ns 1320 ns	X X X
2 ✓ t _{HD} 3 ✓ t _{LOW} 4 ✓ t _{DIG} 5 ✓ t _{HIGH}	Hold Time for a (Repeated) START SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period	600 ns 1300 ns 1320 ns 600 ns	x x x x x x x x x x x x x x x x x x x
2	Hold Time for a (Repeated) START SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver	600 ns 1300 ns 1320 ns 600 ns 606.55 ns	x x x x x x x x x x x x x x x x x x x
2	Hold Time for a (Repeated) START SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver Tota Setup Time	600 ns 1300 ns 1320 ns 600 ns 606.55 ns 100 ns	x x x x x x x x x x x x x x x x x x x
2	Hold Time for a (Repeated) START SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver SCL Clock High Period as seen at the receiver Tota Setup Time Tota Hold Time	600 ns 1300 ns 1320 ns 600 ns 600 ns 606.55 ns 100 ns X	x x x x x x x x x x x x x x x x x x
2	Hold Time for a (Repeated) START SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver SCL Clock High Period as seen at the receiver To Data Setup Time SCL Signal Rise Time	600 ns 1300 ns 1320 ns 600 ns 600 ns 100 ns X 20 ns	X X X X X X X X X X X X X 300 ns

This section includes 5 parameter tables, including

- Frequency
- I3C timing requirements when communicating with I²C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

All specification table are listed below.

In the Pure Bus setup, the timing requirements table with I^2C Legacy Devices is not required and thus be hidden from the parameter settings dialog. The frequency parameter f_{SCL} will also be hidden in the Pure Bus setup.



MIPI I3C Frequency Requirements

Symbol	Electrical Parameter
f _{SCL}	SCL Clock Frequency when communicating with I ² C Legacy Devices ¹
t _{SCL_PP}	SCL Clock Frequency
t _{bt_freq}	HDR-BT SCL Clock Frequency

MIPI I3C Timing Requirements When Communicating With I²C Legacy Devices¹

Symbol	Electrical Parameter
tsu_sta	Setup Time for a REPEATED START
t _{HD_STA}	Hold Time for a (REPEATED) START
t _{LOW}	SCL Clock Low Period
t _{DIG_L}	SCL Clock Low Period as seen at the
	receiver
tнigн	SCL Clock High Period
t _{DIG_H}	SCL Clock High Period as seen at the
	receiver
t _{su_dat}	Data Setup Time
t _{HD_DAT}	Data Hold Time
t _{rCL}	SCL Signal Rise Time
t _{fCL}	SCL Signal Fall Time
t _{rDA}	SDA Signal Rise Time
t _{rDA_OD}	SDA Signal Rise Time (Open Drain)
t _{fDA}	SDA Signal Fall Time
tsu_sto	Setup Time for STOP
t _{BUF}	Bus Free Time Between a STOP and a
	START
t _{spike}	Pulse Width of Spikes that Spike Filter
	Must Suppress

¹ Only available when the bus configuration is set to Mixed Bus (i.e. at least one I²C legacy device is presented on the I3C bus).



Symbol	Electrical Parameter
tlow_od	SCL Clock Low Period
t _{DIG_OD_L}	SCL Clock Low Period as seen at the receiver
t _{HIGH_INIT}	High Period of SCL Clock (for First Broadcast Address)
t _{HIGH_OD}	SCL Clock High Period
t _{DIG_OD_} н	SCL Clock High Period as seen at the receiver
t _{fDA_OD}	SDA Data Fall Time
t _{su_od}	SDA Data Setup Time During Open Drain Mode
t _{CAS}	Clock After START (S) Condition
t _{CBP}	Clock Before STOP (P) Condition
t _{CRHPOverlap}	Active Controller to Secondary Overlap time during handoff
taval	Bus Available Condition
tidle	Bus Idle Condition
t _{NEWCRLock}	Time Interval Where New Controller Not Driving SDA Low

MIPI I3C Open Drain Timing Requirements



Symbol	Electrical Parameter
tLOW	SCL Clock Low Period
t _{DIG_L}	SCL Clock Low Period as seen at the receiver
t _{нібн}	SCL Clock High Period
t _{DIG_H}	SCL Clock High Period as seen at the receiver
tsco	Clock in to Data Out for Target
t _{CR_PP}	SCL Clock Rise Time
t _{cf_pp}	SCL Clock Fall Time
tHD_PP_Controller	SDA Signal Data Hold (Controller)
t _{HD_PP_Target}	SDA Signal Data Hold (Target)
t _{su_pp}	SDA Signal Data Setup
t _{CASr}	Clock After Repeated START (Sr) Condition
t _{CBSr}	Clock Before Repeated START (Sr) Condition
t _{BT_HO}	HDR-BT Master to Slave Hand Off Delay
t _{BT_STALL}	HDR-BT Clocked Not-Ready Data-Block Headers

MIPI I3C Push-Pull Timing Requirements



MIPI I3C I/O Stage Characteristics Voltage Requirements	
---	--

Symbol	Electrical Parameter
V _{IL}	Low-Level Input Voltage
V _{IH}	High-level Input Voltage
V _{OL}	Low-level Output Voltage
V _{OH}	High-level Output Voltage



5. Sample Result





MIPI RFFE Electrical Validation Solution

Introduction:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

MIPI RFFE (Radio Frequency Front-End) is a standard developed by the MIPI Alliance to define the interface between baseband processors and radio frequency front-end modules in mobile devices, such as smartphones and tablets. It is part of the broader MIPI (Mobile Industry Processor Interface) family, which includes various standards for efficient communication between different components in mobile and embedded devices.

MIPI RFFE is a key enabler in modern wireless devices, providing a standardized and efficient interface for controlling the RF front-end components in mobile and wireless communication systems.



MIPI RFFE Electrical Validation Settings:

1. General Settings: Channel sources, Working Voltage, Frequency Range, Test Point and Read Operation

EV Electrical Validation			×
120	Settings		Import Export
IZS MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	 → General → Trigger ★ Validation 	Channel Settings SCLK: DSO Channel 1 Probe Settings: x10 Probe Set	
	Default		Next

2. Trigger Settings:

EV Electrical Validation	n		×
12C	Settings	Import Export	
I2C I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	Settings General Trigger Validation	Command Sequence Type: Any Command Slave Address: Xh Register Address (Lower): XXh Register Address (Upper): XXh Data • Any Offset • Fixed Offset • Byte(s) Data 1 XXh Data 2 XXh Data 3 Xh Data 4 XXh	
	Default		Previous Next



3. Electrical Validation: Voltage, Timing and Frequency limitation

EV Electrical Validation	1				×	
120	Settings				Import Export	
I2S MIPI I3C MIPI REFE	 ✓General ✓Trigger 	Seneral rigger Customized EV Parameter:				
MIPI SPMI PDM	Validation	Frequency				
SPI		Name	Description	Min	Max	
UART(RS232)		1 ✓ f _{SCLK} SCLK Free	quency	0.032 MHz	26 MHz	
		► Time (Full-S	speed Operations)			
		I Time (Half-S	Speed Data Response Operations)			
		Name	Description	Min 29.1 pc	Max	
		CLEAN CLEAN C		20.1 115		
				20.1 ms	^	
		3 V TSCLKOTR_HSDR (F	ISDR) Clock Output Transition (Rise/Fail) Time	3.5 ns	o.o ns	
		4 V t _{SU_M_Rd_HSDR} (F	HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read	3.75 ns	×	
		5 V t _{H_M_Rd_HSDR} (F	HSDR) SDATA Hold Time, with respect to SCLK Output - BOM - Read	6.75 ns	X	
		✓ Voltage				
		Name	Description	Min	Max	
		1 V _{Low} Low-Leve	el Voltage	0 V	0.36 V	
		2 ✓ V _{High} High-Lev	vel Voltage	1.44 V	1.8 V 💌	
	Default	Advance			Previous Apply	

4. Software electrical validation interface:



Overview Detail MIPI RFFE

ſ	Timestamp	SAMID	Command	Byte Count	Address	Mask	Data	Information
-	1.528 µs	Spare (user-d	Register Writ		1C		PM_TRIG[7:0	
2	1.814 µs						PWR_MODE	
111	3 1.814 µs						TRIG_REG[5:	
4	2.164 µs	PA Module1(F)	Register Writ		1C		PM_TRIG[7:0	
5	5 2.448 µs						PWR_MODE	
6	5 2.448 µs						TRIG_REG[5:	



5. Software electrical validation control panel:



- A. Stop Conditions:
 Stop when acquired X times
 Stop when Result Fail > X times
- B. Information: Select waveform
- C. Save File: Save as Html Save as .MOW(Software format)

6.	Overview	Report:
----	----------	----------------

1	2 V -1.12			2 ² -0	V .05							H 200 ns +4.812 ns HIPI RFFE Validation Stop S/R: 500 MS/s
De								40 V 10 V	Deta: 03		A Address 10 - 11	Date 01 0.0
C	verview Del	tail MIPI RFI	FE									
	Name	Description	Limit Min	Limit Max	Min 49 200 MHz	Mean	Max	andard Deviat	i Count	Result		
2	tsclkon	Clock Out	4 700 ns	52.000 WH2	6 413 ns	7 501 ns	9 281 ns	714 000 ps	230	Pass		
3	tscl.kol	Clock Out	4.700 ns		8.329 ns	41.946 ns	1.563 us	196.252 ns	230	Pass		
4	tsclkotr	Clock Out	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail		
5	tscl.kiH	Clock Inpu							0			
6	tsclkil	Clock Inpu							0			
7	t SCLAITR	Clock Inpu							0			
8	t _{skew_M}	SDATA Sk	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95	Fail		
9	SDATAOTR_M	SDATA Ou	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail		
10	ted_s_a	Time for s							0			
11	SDATAOTR_S_SR	sRead SD							0			<u>-</u>



7. Detail Report:



8. Reference Point Dialog & Waveform:





9. Html Report:



Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 15:32:11
S/W Version	1.8.62
Protocol	MIPI RFFE

Overview Results:

Total: 33 Pass: 2 Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fSCLK	SCLK Frequency	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	89.2%	8.4%	×Fail
2	t _{SCLKOH}	Clock Output High Time	4.700 ns		6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	36.4%		Pass
3	t _{SCLKOL}	Clock Output Low Time	4.700 ns		8.329 ns	41.946 ns	1.563 us	196.252 ns	230	77.2%		✓Pass
4	t _{SCLKOTR}	Clock Output Transition (Rise/Fall) Time	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	×Fail
5	t _{SCLKIH}	Clock Input High Time							0			
6	t _{SCLKIL}	Clock Input Low Time							0			
7	t _{SCLKITR}	Clock Input Transition (Rise/Fall) Time							0			
8	t _{skew_m}	SDATA Skew Relative to SCLK, BOM Master Output	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95		4368.2%	×Fail
9	t _{SDATAOTR_M}	SDATA Output Transition (Rise/Fall) Time, BOM Master	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	×Fail
10	t _{PD_S_sR}	Time for sRead Data Output Valid from SCLK Rising Edge - Slave							0			
11	t _{SDATAOTR_S_sR}	sRead SDATA Output Transition (Rise/Fall) Time - Slave							0			
12	t _{SU_M_Rd}	SDATA Setup Time, with respect to SCLK Output - BOM - Read							0			
13	t _{H_M_Rd}	SDATA Hold Time, with respect to SCLK Output - BOM - Read							0			
14	t _{SU_M_sR}	SDATA Setup Time, with respect to SCLK Output - BOM - sRead							0			
15	t _{H_M_sR}	SDATA Hold Time, with respect to SCLK Output - BOM - sRead							0			
16	t _{su_s}	SDATA Setup Time, with respect to SCLK Input - Slave (or non-BOM)							0			
17	t _{H_S}	SDATA Hold Time, with respect to SCLK Input - Slave (or non-BOM)							0			
18	t _{SCLKOH_HSDR}	(HSDR) Clock Output High Time							0			
19	t _{SCLKOL_HSDR}	(HSDR) Clock Output Low Time							0			
20	t _{SCLKOTR_HSDR}	(HSDR) Clock Output Transition (Rise/Fall) Time							0			
21	t _{SCLKIH_HSDR}	(HSDR) Clock Input High Time							0			
22	t _{SCLKIL_HSDR}	(HSDR) Clock Input Low Time							0			
23	t _{SCLKITR_HSDR}	(HSDR) Clock Input Transition (Rise/Fall) Time							0			
24	tpD_S_Rd_HSDR	(HSDR) Time for Read Data Output Valid from SCLK Rising Edge - Slave							0			
25	tSDATAOTR_S_Rd_HSDR	(HSDR) Read SDATA Output Transition (Rise/Fall) Time - Slave							0			
26	t _{PD_S_sR_HSDR}	(HSDR) Time for sRead Data Output Valid from SCLK Rising Edge - Slave							0			
27	tSDATAOTR_S_SR_HSDR	(HSDR) sRead SDATA Output Transition (Rise/Fall) Time - Slave							0			
28	tSU_M_Rd_HSDR	(HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read							0			
20	tu u ou ucoo	(USDR) SDATA Held Time, with respect to SCLK Output, ROM, Read		1					0			

f_{SCLK} - Test Result: Fail Description: SCLK Frequency




MIPI SPMI Electrical Validation Solution

Introduction:

File / Settings Dis	olay Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	3					

Use an oscilloscope to do MIPI SPMI Electrical Validation to ensure that the MIPI SPMI meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation.

MIPI SPMI (System Power Management Interface) is a specification developed by the **MIPI Alliance** (Mobile Industry Processor Interface) for managing power in mobile and embedded systems. The primary goal of SPMI is to provide a standardized communication interface between power management ICs (PMICs) and various system components, allowing efficient power distribution and power state management in devices like smartphones, tablets, and other embedded systems.



MIPI SPMI Electrical Validation Solution

1. General Setting: Channel sources, working voltage, speed and version

V Electrical Validation	×
Import Settings	Export
I2S MIPIRFEE MIPISSMI PDM SPI UART(RS232) Channel Settings Stringger Working Voltage(Vos): 3.30 V \$ Device Use of (15) Device Low Speed (15) Device Version: v2.0 Use of (15) Device Version: v2.0	Next

2. Trigger Setting:

EV Electrical Validation									×
120	Settings								Import Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	 ✓General →Trigger Xvalidation 	Command Type: 7 Slave Ac Register Data	I Sequence Any Command ddress: Xh r Address: XXX	Xh	•				
		Data 1	XXh	Data 5	XXh	Data 9	XXh	Data 13 XXh	
		Data 2	XXh	Data 6	XXh	Data 10	XXh	Data 14 XXh	
		Data 3	XXh	Data 7	XXh	Data 11	XXh	Data 15 XXh	
		Data 4	XXh	Data 8	XXh	Data 12	XXh	Data 16 XXh	
	Default								Previous Next



3. Electrical validation settings: Frequency, Time and Voltage limitation

EV Electrical Validation	n				
12C	Settings				Import Expo
I2S MIPI I3C MIPI REFE	✓General✓Trigger	Customized EV	Parameter:		
MIPI SPMI	Validation	Frequence	у		
SPI		Name	Description	Min	Max 26 MHz
UART(R5252)		I I ISCLKSCLK	rrequency		
		∠ Time			
		Name	Description	Min	Max
		1 ✓ t _{SCLKOH}	CLK Output High Time	12 ns	×
		2 ✓ t _{SCLKOL}	CLK Output Low Time	12 ns	×
		3 ✔ t _{SCLKOTR} S	CLK Output Transition (Rise/Fall) Time	2.1 ns	5.3 ns
		4 ✓ t _{sdataotr} s	DATA Output Transition (Rise/Fall) Time	2.1 ns	5.3 ns
		5 🗸 t _D	DATA Output Valid Time	0 us	11 ns
		6 √ t _s s	DATA Setup Time	1 ns	×
		7 ✔ t _H 5	DATA Hold Time	5 ns	X
		✓ Voltage			
		Name	Description	Min	Max
		1 ✔ V _L Low-L	evel Voltage	0 V	360 mV
		2 ✔ V. High-I	evel Voltage	1 44 V	18V -
	Default	Advance			Previous Apply

4. Software electrical validation interface:





5. Software electrical validation control panel:



- Stop Conditions: Stop when acquired X times Stop when Result Fail > X times
- B. Information: Select waveform
- C. Save File: Save as Html Save as .MOW(Software format)



High-Level... 1.440 V

1.800 V

10 V_H

2.997 V 3.325 V

3.700 V

134.058 mV





7. Detail Report:



8. Reference Point Dialog & Waveform:





9. Html Report:



Electrical Validation Report

Test instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 14:54:25
S/W Version	1.8.62
Protocol	MIPI SPMI

Overview Results:

Total: 10 Pass: 6 Fail: 4

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Resul
1	^f sclk	SCLK Frequency	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	441.6%	-58.9%	✓Pass
2	t _{SCLKOH}	SCLK Output High Time	12.000 ns		41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	245.0%		✓Pass
3	t _{SCLKOL}	SCLK Output Low Time	12.000 ns		41.351 ns	102.355 ns	5.718 us	501.997 ns	340	244.6%		✓Pass
4	t _{SCLKOTR}	SCLK Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	-53.1%	35.0%	×Fail
5	t _{SDATAOTR}	SDATA Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	-53.6%	-63.5%	×Fail
6	t _D	SDATA Output Valid Time	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114		48997.2%	×Fail
7	ts	SDATA Setup Time	1.000 ns		26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	2569.4%		✓Pass
8	t _H	SDATA Hold Time	5.000 ns		43.207 ns	195.261 ns	5.299 us	790.518 ns	114	764.1%		✓Pass
9	VL	Low-Level Voltage	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340		-21.2%	✓Pass
10	V _H	High-Level Voltage	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	108.1%	105.5%	≍Fail

f_{SCLK} - Test Result: Pass Description: SCLK Frequency





PDM Electrical Validation Solution

Introduction:

File / Settings Di	isplay Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	en File					

Use an oscilloscope to do PCM Electrical Validation to ensure that the PDM meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

PDM Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the PDM baud rate.

PDM_CLK High Frequency Range	fclкн		5.28	8.64	MHz				
PDM_CLK Low Frequency Range	f _{CLKL}		1.84	4.32	MHz				
PDM_CLK High Time	^t PDM_CLKH		40		ns				
PDM_CLK Low Time	tPDM_CLKL		40		ns				

Part of the electrical characteristics of common PDM specifications:

L



The report of common PDM validation:

0	verview	Deta	il PDM									
	Name	e	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result	
1	f _{CLK}		Clock freq	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass	
2	t _{LOW}	1	Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3	t _{HIGH}		High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4	t _{rCL}		Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5	t _{rCL}		Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6	t _{rDD}		Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7	t _{fDV}		Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8	t _{rDD}		Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9	t _{rDV}		Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	
												l

Dedicated page for Electrical Validation:



- 5. Frequency: Clock speed
- 6. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 7. Voltage: VL, VH, etc.



Frequency:

Symbol	Electrical Parameter
f _{SCL}	PDM_CLK Frequency Range

Time:

Symbol	Electrical Parameter
t _{LOW}	Low Period of the Clock
t _{нібн}	High Period of the Clock
t _{rCL}	Rise time of Clock signal
t _{fCL}	Fall time of Clock signal
t _{rDD}	Delay time from Clock edge to Data Rise driven
t _{fDD}	Delay time from Clock edge to Data Fall driven
t _{rDV}	Delay time from Clock edge to Data Rise valid
t _{fDV}	Delay time from Clock edge to Data Fall valid

Voltage:

Symbol	Electrical Parameter
V _{ClkLow}	Low-level Input voltage for clock
V _{ClkHigh}	High-level Input voltage for clock
V _{DataLow}	Low-level Input voltage for data
V _{DataHigh}	High-level Input voltage for data



PDM Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

Settings		
 General Decode 	Channel Settings	
×Validation	CLK: DSO Channel 1 V Probe Settings: x10 V	
	DATA: DSO Channel 2 Probe Settings: x10	
	Working Voltage(V _{DD}): 1.80 V	
	PDM Clock Speed: 3072 - KHz	
Default		Next



2. Decode Settings: PDM decoding settings

Settings			
 ✓General →Decode 	Audio Settings		
×Validation	Decimation Rate: x64		
	Audio Frequency 48 - KHz		
	Mono & Stereo		
	Mode: Stereo 👻		
Default		Previous	Next



de Customized EV F	Parameter:		
Ition Frequence	у		(
Name 1 ☑ f _{CLK} Clock	Description	0 kHz	Ma: 3.072 MHz
⊿ Time			(
Name	Description	Min	Max
1 ✓ t _{LOW} LOW	Period of the Clock	130.208 ns	195.312 ns
2 V t _{HIGH} High		130.208 ns	195.312 ns
	time of CLK signal	X	13 ns
4 v uc∟ Fairi	utime from Clk edge to Data Rise driven	A 40 ns	13 fis
	v time from Clk edge to Data Fall driven	40 ns	80 ns
7 ✓ t _{ov} Dela	v time from Clk edge to Data Rise Valid	X	100 ns
8 V t _{rDV} Dela	y time from Clk edge to Data Fall Valid	X	100 ns
✓ Voltage			(
Name	Description	Min	Ma
1 ✓ V _{ClkLow} L	ow-level input voltage for clock	-0.5 V	0.54 V
2 V _{ClkHigh} H	igh-level input voltage for clock	1.26 V	2.3 V
3 V _{DataLow} L	ow-level input voltage for Data	-0.5 V	0.54 V
4 ✓ V _{DataHigh} H	igh-level input voltage for Data	1.26 V	2.3 V



4. Software electrical validation interface:

500 mV 2 500 mV -3.50 2 -3.50		H 4 µs -65.104 µs T PDM Validation Stop <u>S/R: 500 MS/s</u>
ht nhm mh të mntëre nin k	h ni han h' ha nh a h' a hi kan mi ni k	na an da arro menun hada en a ma din habibata
	n an	
	*********	********
Overview Detail PDM		
Timestamp L	R Information Baseband Sampling Rate:48 KHz Dec	mation
2 0 s	Dascound Camping Nate.40 Ni12, Dec	
3 106 ns 1		
untitled1 × EV_PDM_Stereo ×		 _

5. Software electrical validation control panel:



A. Stop Conditions:

Stop when acquired X times Stop when Result Fail > X times

B. Information: Select waveform

C. Save File: Save as Html Save as .MOW(Software format)



6. Overview Report:

1 500 mV -3.50	2 5	00 mV 3.50				Н	1 µs -328 ns	T PDM Vali Stop <u>S/F</u>	dation R: 500 MS/s	
POM 0, 0, 1, 1						0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	tail PDM									
Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result	_
1 f _{CLK}	Clock freq	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass	
2 t _{Low}	Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3 thigh	High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4 tcL	Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5 t _{ICL}	Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6 t _{fDD}	Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7 t _{fDV}	Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8 t _{ob}	Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9 t _{rDV}	Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	
untitled1 🗙	EV PDM Ste	reo X		<u> </u>	1	1				



7. Detail Report:

-3.50	2 ⁵¹ -3	00 mV 3.50				н	1 µs -328 ns	T PDM Valid Stop <u>S/R</u>	lation : 500 MS/s
						2 3 2	997		
	0 1 0 0 1 0							000000 9 0 0 •••••	
ICLK LOW	t _{HIGH} t _{rCL}	t _{rCL} t _{rDD}	t _{rDV} t _{rD}	D t _{rDV}	V _{CIKLow} V _{Date}	Low V _{ClkHigh}	V _{DataHigh}		
Waveform N	t _{HIGH} t _{rCL}	t _{ICL} t _{IDD}	t _{IDV} t _{rD}	nd t _{rDV}	V _{CIKLow} V _{Dat}	_{ILow} V _{CIRHigh}	V _{DataHigh}	Result	
UCLK ULOW Waveform No 1 1 1-1	t _{HIGH} t _{rCL} TimeStamp 81.316 us	t _{rCL} t _{rDD} Limit Min 0.000 Hz	t _{rDV} t _{rD} Limit Max 3.072 MHz	no t _{rDV} V Min 3.027 MHz	V _{CIKLow} V _{Dat} Mean 3.030 MHz	Low V _{Cliffigh} Max 3.033 MHz	V _{DataHigh} Count 443	Result Pass	
Vaveform No 1 1-1 2 2-1	t _{HIGH} t _{rCL} TimeStamp 81.316 us 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz	t _{rDV} t _{rD} Limit Max 3.072 MHz 3.072 MHz	D t _{rDV} V Min 3.027 MHz 3.028 MHz	V _{CIKLow} V _{Dat} Mean 3.030 MHz 3.030 MHz	Max 3.033 MHz 3.033 MHz	V _{DataHigh} Count 443 443	Result Pass Pass	*
Variation Upper law Waveform Net 1 1 1-1 2 2-1 3 3-1	tнкн t _{rcL} ТітеStamp 81.316 us 81.316 us 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	t _{rDV} t _{rD} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz	trov Y Min 3.027 MHz 3.028 MHz 3.028 MHz	V _{CIKLOW} V _{Dab} Mean 3.030 MHz 3.030 MHz 3.030 MHz	Max Max 3.033 MHz 3.033 MHz 3.034 MHz	V _{DataHigh} Count 443 443 443	Result Pass Pass Pass	
Vicu Low Waveform Nu 1 1 1-1 2 2-1 3 3-1 4 4-1	t _{HIGH} t _{rcL} TIMEStamp 81.316 us 81.316 us 81.316 us 81.316 us	t _{rcL} t _{rDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	t _{IDV} t _{rD} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	t _{rDV} Min 3.027 MHz 3.028 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz	V _{CIKLow} V _{Date} Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Vcliefight Max 3.033 MHz 3.033 MHz 3.034 MHz 3.032 MHz	V _{DataHigh} Count 443 443 443 443	Result Pass Pass Pass Pass	*
Vace Vace 1 1-1 2 2-1 3 3-1 4 4-1 5 5-1	tyncs+ t,cL TimeStamp 81.316 ∪s 81.316 ∪s 81.316 ∪s 81.316 ∪s 81.316 ∪s	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	t _{DV} t _{ro} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	t _{rov} Y Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.028 MHz 3.029 MHz 3.028 MHz	V _{CIKos} V _{Dati} Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Vcietian Max 3.033 MHz 3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz	VDataHigh Count 443 443 443 443 443 443 443	Result Pass Pass Pass Pass Pass	*
Vicu ULOW Waveform Nu 1 1 1-1 2 2-1 3 3-1 4 4-1 5 5-1 6 6-1	tilditi tilditi TimeStamp 81.316 81.316 81.316 81.316 81.316 81.316 81.316	t _{rcL} t _{rDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	t _{DV} t _{rD} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	trov Min 3.027 MHz 3.028 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.029 MHz	Mean 3.030 MHz 3.030 MHz	Vciefiah 3.033 MHz 3.033 MHz 3.034 MHz 3.035 MHz 3.034 MHz 3.035 MHz 3.033 MHz 3.034 MHz 3.033 MHz 3.033 MHz	VDataHigh Count 443 443 443 443 443 443 443 443 443	Result Pass Pass Pass Pass Pass Pass Pass	*
Vaveform No 1 1-1 2 2-1 3 3-1 4 4-1 5 5-1 6 6-1 7 7-1	tinest to tree to tre	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz	t _{DV} t _{ro} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz	t _{rov} Y Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.028 MHz 3.029 MHz 3.027 MHz	V _{CIKLos} V _{Dati} Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Vcientian Max 3.033 MHz 3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz 3.032 MHz 3.033 MHz 3.032 MHz 3.033 MHz	VDataHigh Count 443 443 443 443 443 443 443 443 443 443 443	Result Pass Pass Pass Pass Pass Pass Pass Pass	
Vaveform No 1 1-1 2 2-1 3 3-1 4 4-1 5 5-1 6 6-1 7 7-1 8 8-1	tinicsi tt.	t _{ICL} t _{IDD} Limit Min 0.000 Hz	t _{DV} t _{op} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz	t _{rov} Y Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.027 MHz 3.027 MHz 3.027 MHz 3.027 MHz 3.027 MHz 3.027 MHz	V _{CIKLos} V _{Dati} Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Vcietian Max 3.033 MHz 3.033 MHz 3.034 MHz 3.033 MHz	VDataHigh Count 443 443 443 443 443 443 443 443 443 443 443 443	Result Pass Pass Pass Pass Pass Pass Pass Pass Pass	



8. Reference Point Dialog & Waveform:





9. Html Report:

Acute. PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
est Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

Overview Results:

Total: 13 Pass: 13

Pass:	13
Fail:	0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fCLK	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430		-1.2%	✓Pass
2	LOW	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	tHIGH	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	4 _{CL}	Rise time of CLK signal		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930		-85.7%	✓Pass
5	4CL	Fall time of CLK signal		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930		-85.7%	✓Pass
6	trop	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	trov	Delay time from Clk edge to Data Fall Valid		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500		-20.7%	✓Pass
8	t _{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	✓Pass
9	trDV	Delay time from Clk edge to Data Rise Valid		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440		-24.8%	✓Pass
10	VCIkLow	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	VDataLow	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	VClkHigh	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	✓Pass
13	VDataHigh	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

f_{CLK} - Test Result: Pass Description: Clock frequency

Limit Min Limit Max Min Mean Ma	x Standard Deviation Count	Margin Min Margin	Max			
0.000 Hz 3.072 MHz 3.027 MHz 3.030 MHz 3.034	MHz 17.798 KHz 4430	1.2%				
	Histogram					
Occurance (%), Total 4430		Value Range	Occurance Count			
100 -		3.027 MHz ~ 3.028 MHz	13			
90 -		3.028 MHz ~ 3.028 MHz	70			
80 - 70 -		3.028 MHz ~ 3.029 MHz	298			
60 - 50 -		3.029 MHz ~ 3.03 MHz	813			
40 - 33.0		3.03 MHz ~ 3.03 MHz	1464			
30 242 20 18.4 11.9		3.03 MHz - 3.031 MHz	1073			
10 0.3 1.6 6.7	3.0 0.6 0.2 Test Value	3.031 MHz - 3.032 MHz	529			
3.027 MHz	3.034 MHz	3.032 MHz ~ 3.032 MHz	135			
Test Value		3.032 MHz ~ 3.033 MHz	27			
Limit	3.072 MHz	3.033 MHz = 3.034 MHz				
		COOL IN THE OWNER WITH	•			
Min	Detail Report Row: 1, Tes	st Index: 340 Max	×		Detail Repo	ort Row: 3, Test Index: 431
Min 500 mV 3 50 3 50 3 50	Detail Report Row: 1, Tes 100 ns 112.198 μs PDM Validation Stop S/R 5001	st Index: 340 Max	X 500 mV -3.50 -3.50	mV)	Detail Repo	PDM Validation Stop SIR: 500 MS/s
	Detail Report Row. 1, Tee	st Index. 340 Max	500 mV 3500 mV 3500mV 3500 mV 3500		Detail Repr.	ht Row: 3, Test Index: 431



SMBUS Electrical Validation Solution

Introduction:

File / Settings Displa	y Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation						

Use an oscilloscope to do PCM Electrical Validation to ensure that the PDM meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

PDM Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the PDM baud rate.

DIGITAL AUDIO INTERFACE		 		
PDM_CLK High Frequency Range	fclкн	5.28	8.64	MHz
PDM_CLK Low Frequency Range	f _{CLKL}	1.84	4.32	MHz
PDM_CLK High Time	^t PDM_CLKH	40		ns
PDM_CLK Low Time	tPDM_CLKL	40		ns

Part of the electrical characteristics of common PDM specifications:

L



The report of common PDM validation:

0	verview	Deta	il PDM									
	Name	e	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result	
1	f _{CLK}		Clock freq	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass	
2	t _{LOW}	1	Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3	t _{HIGH}		High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4	t _{rCL}		Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5	t _{rCL}		Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6	t _{rDD}		Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7	t _{fDV}		Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8	t _{rDD}		Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9	t _{rDV}		Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	
												l

Dedicated page for Electrical Validation:



8. Frequency: Clock speed

9. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation

10. Voltage: VL, VH, etc.



Frequency:

Symbol	Electrical Parameter
f _{SCL}	PDM_CLK Frequency Range

Time:

Symbol	Electrical Parameter
t _{LOW}	Low Period of the Clock
t _{нібн}	High Period of the Clock
t _{rCL}	Rise time of Clock signal
t _{fCL}	Fall time of Clock signal
t _{rDD}	Delay time from Clock edge to Data Rise driven
t _{fDD}	Delay time from Clock edge to Data Fall driven
t _{rDV}	Delay time from Clock edge to Data Rise valid
t _{fDV}	Delay time from Clock edge to Data Fall valid

Voltage:

Symbol	Electrical Parameter
V _{ClkLow}	Low-level Input voltage for clock
V _{ClkHigh}	High-level Input voltage for clock
V _{DataLow}	Low-level Input voltage for data
$V_{DataHigh}$	High-level Input voltage for data



SMBUS Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

Settings		
 General Decode 	Channel Settings	
×Validation	CLK: DSO Channel 1 V Probe Settings: x10 V	
	DATA: DSO Channel 2 Probe Settings: x10	
	Working Voltage(V _{DD}): 1.80 V	
	PDM Clock Speed: 3072 KHz	
Default		Next



2. Decode Settings: PDM decoding settings

Sottings			
General	Audio Settinas		
Xvalidation	Decimation Rate: x64 Audio Frequency 48 KHz		
	Mono & Stereo		
	Mode: Stereo 💌		
Default		Previous	Next



Customized EV Parameter.			
Frequency			
Name	Description	Min	Max
1 f _{CLK} Clock frequency		0 kHz	3.072 MHz
∠ Time			
Name	Description	Min	Max
1 ✓ t _{LOW} Low Period of the	Clock	130.208 ns	195.312 ns
2 ✓ t _{HIGH} High Period of the	Clock	130.208 ns	195.312 ns
3 ✔ t _{rCL} Rise time of CLK s	ignal	X	13 ns
4 ✔ t _{ICL} Fall time of CLK si	gnal	X	13 ns
5 ✓ t _{rDD} Delay time from C	k edge to Data Rise driven	40 ns	80 ns
6 ✔ t _{rDD} Delay time from C	k edge to Data Fall driven	40 ns	80 ns
7 ✓ t _{rDV} Delay time from C	k edge to Data Rise Valid	X	100 ns
8 🗸 t _{rDV} Delay time from Cl	k edge to Data Fall Valid	X	100 ns
✓ Voltage			
Name	Description	Min	Max
1 ✓ V _{CIkLow} Low-level input	voltage for clock	-0.5 V	0.54 V
2 ✓ V _{ClkHigh} High-level input	voltage for clock	1.26 V	2.3 V
3 ✓ V _{DataLow} Low-level input	voltage for Data	-0.5 V	0.54 V
4 ✓ V _{DataHigh} High-level input	voltage for Data	1.26 V	2.3 V



4. Software electrical validation interface:

500 mV -3.50 2 500 mV -3.50			H 4 µs -65.104 µs	PDM Validation Stop <u>S/R: 500 MS/</u>	s		
	AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA		Anton Anton Anton		AAAAAAAAAA		
maini kao minina kao kao minina kao kao minina kao kao minina kao kao kao kao kao kao kao kao kao ka	n tan mtann h mmm	n n h n nh Ann m nh An	ivan alm inte Avro in	n von in in nim vin å von	nin minh <mark>h</mark> a		
Overview Detail PDM							
Timestamp L	R	Information			<u> </u>		
1 0 s	Basebar	d Sampling Rate:48 KHz, Decir	mation		_		
2 U S 3 106 ns 1							
					•		

5. Software electrical validation control panel:



D. Stop Conditions: Stop when acquired X times

Stop when Result Fail > X times

- E. Information: Select waveform
- F. Save File: Save as Html Save as .MOW(Software format)



6. Overview Report:

1 500 mV -3.50	2 5	00 mV 3.50				н	1 µs -328 ns	T PDM Vali Stop <u>S/I</u>	idation R: 500 MS/s	
POM. 0.0.111						2 8 9 0 0 1 0 8 0 9		8 9 0 100000 9 0 1		
Overview De	tail PDM									
Name	Clock freq	0 000 Hz	3 072 MHz	Min 3 027 MHz	Mean 3 030 MHz	Max 3 034 MHz	17 798 KHz	4430	Pass	Ē
2 tLow	Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3 thigh	High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4 ta	Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5 t _{fCL}	Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6 t _{rDD}	Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7 t _{fDV}	Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8 t _{rDD}	Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9 t _{rDV}	Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	
untitled1 X	EV PDM Ste	reo 🗶					1			



7. Detail Report:

1 -3.50	2 -3	00 mV .50				Н	1 µs -328 ns	T PDM Valid	lation <u>I: 500 MS/s</u>
						2 3 9	9 6 9	8 9 0	00000
						3 3 5			
	t _{HIGH} t _{rcL}	t _{rcL} t _{rpp}	t _{rDV} t _{rD}	D t _{rDV}	V _{CIKLow} V _{Date}		V _{DataHigh}		
Waveform N	o. TimeStamp	Limit Min	Limit Max	Min	Mean	Max	Count	Result	-
1 1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass	
2 2-1	01 216								
2 2-1	01.310 US	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass	
3 3-1	81.316 us	0.000 Hz 0.000 Hz	3.072 MHz 3.072 MHz	3.028 MHz 3.028 MHz	3.030 MHz 3.030 MHz	3.033 MHz 3.034 MHz	443 443	Pass	
3 3-1 4 4-1	81.316 us 81.316 us	0.000 Hz 0.000 Hz 0.000 Hz	3.072 MHz 3.072 MHz 3.072 MHz	3.028 MHz 3.028 MHz 3.029 MHz	3.030 MHz 3.030 MHz 3.030 MHz	3.033 MHz 3.034 MHz 3.032 MHz	443 443 443	Pass Pass Pass	
3 3-1 4 4-1 5 5-1	81.316 us 81.316 us 81.316 us 81.316 us	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz	3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz	443 443 443 443	Pass Pass Pass Pass	
3 3-1 4 4-1 5 5-1 6 6-1	81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.027 MHz	3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz 3.033 MHz	443 443 443 443 443 443	Pass Pass Pass Pass Pass	
2 2-1 3 3-1 4 4-1 5 5-1 6 6-1 7 7-1	81.316 us	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.027 MHz 3.029 MHz	3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz 3.033 MHz 3.032 MHz	443 443 443 443 443 443 443	Pass Pass Pass Pass Pass Pass Pass Pass	
2 2-1 3 3-1 4 4-1 5 5-1 6 6-1 7 7-1 8 8-1	81.316 us 81.316 us	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.027 MHz 3.029 MHz 3.027 MHz	3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz 3.033 MHz 3.032 MHz 3.033 MHz	443 443 443 443 443 443 443 443 443	Pass Pass Pass Pass Pass Pass Pass	



8. Reference Point Dialog & Waveform:





9. Html Report:

Acute. PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

Overview Results:

Total: 13 Pass: 13

Pass:	13
Fail:	0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fclk	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430		-1.2%	✓Pass
2	LOW	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	tHIGH	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	t _{CL}	Rise time of CLK signal		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930		-85.7%	✓Pass
5	4CL	Fall time of CLK signal		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930		-85.7%	✓Pass
6	4DD	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	t _{fDV}	Delay time from Clk edge to Data Fall Valid		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	***	-20.7%	✓Pass
8	trop	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	Pass
9	t _{rDV}	Delay time from Clk edge to Data Rise Valid		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440		-24.8%	✓Pass
10	VClkLow	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	VDataLow	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	VClkHigh	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	Pass
13	VDataHigh	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

f_{CLK} - Test Result: Pass Description: Clock frequency

Limit	t Min Lim	it Max Min Mean I	Max Standard Deviatio	n Count Marg	gin Min Margin	Max			
0.000	0 Hz 3.07	2 MHz 3.027 MHz 3.030 MHz 3.03	Histogram	4430	-1.2%		1		
			motogrum		Makes Danas	Orange Court			
					value Range	Occurance Count			
100				3.02	7 MHz ~ 3.028 MHz	13			
90	0 +			3.02	8 MHz ~ 3.028 MHz	70			
70	0 -			3.02	8 MHz ~ 3.029 MHz	298			
60	0 • 0 •			3.02	9 MHz ~ 3.03 MHz	813			
40	0+			3.03	MHz ~ 3.03 MHz	1464			
30	0 + 0 +	18.4 24.2		3.03	MHz - 3.031 MHz	1073			
10		1.6	7 3.0 0.6 0.2 Test Val	ue 3.03	1 MHz - 3.032 MHz	529			
3.0	027 MHz		3.034 MHz	3.03	2 MHz ~ 3.032 MHz	135			
Test				3.03	2 MHz ~ 3.033 MHz	27			
Lim	vit -		3.072 MHz	3.03	3 MHz - 3.034 MHz	8			
Min	ı		Detail Report Rov	v: 1, Test Ind	iex: 340 Max		•	Detail Repo	ort Row: 3, Test Index: 431
1	500 mV -3.50	2 500 mV -3.50	100 ns -112.198 μs FDM 1 Stop	Validation S/R: 500 MS/s		i00 mV 2 500 3.50 -3.50	mV 0	100 ns -142.228 µs	PDM Validation Stop S/R: 500 MS/s
							A		
		Contraction of the second	lon	lam	~~~		hum	0	lamm
	,		h	. hon	*~~	····	hung	//+///	
	urm-		harring	. from	****	····	hann hann	Proving.	
1004						~	Manna	N-111-11	
10M	R1					× · · · · · · · · · · · · · · · · · · ·		Derwinn - 	



SPI Electrical Validation Solution

File /	Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
Elec Valid	V trical lation	Open EV File						

Settings Guide

1. General Settings

ettings							Import	Export
General Decede	Channel	Settings						
 Trigger Validation 	Type: SCLK: CS:	4-wire SPI • DSO Channel 1 • DSO Channel 2 •	Probe Settings: Probe Settings:	x10 •	x10			
	SDI: SDO: Working	DSO Channel 3 DSO Channel 4 Voltage(V _{DD}): 3.30 V	Probe Settings: Probe Settings:	x10 • x10 •	x10			
	Working	g Voltage(V _{DD}): 3.30 V	\$					
Default							(Next

In the General Settings section, it is mandatory to select the type of SPI type, depending on your

bus configuration (4-wire SPI or 3-wire SPI).

4-wire Channel Setup

Channel Settings	
Type: 4-wire SPI	•
SCLK: DSO Channe	I1 V Probe Settings: x10 V
CS: DSO Channe	I2 ▼ Probe Settings: x10 ▼ mmttaine
SDI: DSO Channe	I3 ▼ Probe Settings: x10 ▼ mmttaine
SDO: DSO Channe	I4 ▼ Probe Settings: x10 ▼

3-wire Channel Setup



C	hannel	Settings		
	Type:	3-wire SPI		
	SCLK:	DSO Channel 1	Probe Settings: x10 -	
	CS:	DSO Channel 2	Probe Settings: x10 -	
	SDA:	DSO Channel 3	Probe Settings: x10 -	

2. Decode Settings

Sottings					Import	Export
✓General	4-wire SPI					
 Trigger Validation 	Chip Select Edge SDI Edge SDO Edge	Active Low Rising Falling				
	Data Format					
	Bit Order Word Size	MSB First -				
Default					Previous	Next

In the Decode Settings, it requires you to setup the SPI data format and the Latching Edge of each

channel. The SPI data format set here is applied both to the Decode and Trigger Settings.

3. Trigger Settings



			Import Export
Settings			
✓General	Trigger on		
 Trigger 	Data Pin: Data In - SDI	•	
Validation	Data		
	Fixed Offset	Byte(s)	
	Data 1 XXh	Data 5 XXh	
	Data 2 XXh	Data 6 XXh	
	Data 3 XXh	Data 7 XXh	
	Data 4 XXh	Data 8 XXh	
Default			Previous Next

The data format is set on the previous page. The remaining setup is all about the data address and which data pin to trigger.

	Freque	псу		
ion 🗖	Name	Description	Min	Max
	1 ✔ f _{SCLK} SC	CLK Clock Frequency	0 MHz	10 MHz
	Time			
	Name	Description	Min	Max
	1 ✓ t _{su,spi}	SDI Setup Time	5 ns	x
	2 ✔ t _{HD,SDI}	SDI Hold Time	15 ns	x
	3 🗌 t _{DIO}	SDI Output Delay Time	Х	X
	4 ✔ t _{su,spc}	SDO Setup Time	5 ns	x
	5 ✔ t _{HD,SD}	SDO Hold Time	5 ns	Х
	6 ✔ t _D	SDO Output Delay Time	x	6 ns
	7 ✔ t _{HIGH}	SCLK Clock High Time	5 ns	х
	8 ✔ t _{LOW}	SCLK Clock Low Time	5 ns	Х
	9 ✔ t _{su,cs}	CS Chip Select Setup Time	5 ns	x
	10 ✓ t _{HD,CS}	CS Chip Select Hold Time	20 ns	X
	11 V tee	Chin Select Deselect time (Chin Select High Time)	50 ns	X

4. Validation Settings

There are no standard measurement limits defined for SPI bus. Therefore, it is recommended to define your own limits while validate SPI signals.



This section displays 3 characteristics table, including

- Frequency
- Timing parameters
- Voltage requirements

All supported validation parameters' symbols and descriptions are listed in the table below.



SPI Frequency Requirements

Symbol	Electrical Parameter
f _{SCLK}	SCLK Clock Frequency

SPI Timing Requirements

Symbol	Electrical Parameter
t _{su,sdi}	SDI Setup Time
t _{HD,SDI}	SDI Hold Time
t _{DIO}	SDI Output Delay Time
t _{su,sdo}	SDO Setup Time
t _{HU,SDO}	SDO Hold Time
t _D	SDO Output Delay Time
tнigн	SCLK High Time
t _{LOW}	SCLK Low Time
t _{su,cs}	CS Chip Select Setup Time
t _{su,cs}	CS Chip Select Hold Time
t _{cs}	Chip Select Deselect time (Chip Select High Time)
t _{CLKr}	SCLK Clock Rise Time
tclkf	SCLK Clock Fall Time

SPI Voltage Requirements

Symbol	Electrical Parameter
V _{IL}	Low-Level Input Voltage
VIH	High-level Input Voltage
V _{OL}	Low-level Output Voltage
V _{OH}	High-level Output Voltage



UART Electrical Validation Solution

Introduction:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	pen File						

Use an oscilloscope to do UART Electrical Validation to ensure that the UART meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

UART Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the UART Speed.

The report of common UART validation:

Overview Detail UART(RS232)											
	Name		Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f _{UART}	E	Baud rate	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	Pass
2	VLow	L	.ow-level i	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	Fail
3	V _{High}	H	ligh-level i	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	Pass



Dedicated page for Electrical Validation:



- 1. Frequency: Clock speed
- 2. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 3. Voltage: V_L, V_H, etc.



UART Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

Settings		
General		
*Decode	Channel Settings	
×Validation	Data: DSO Channel 1 Probe Settings: x10	
	Voltage High(V _{High}): 5.00 V 🗘 Voltage Low(V _{Low}): -5.00 V	
	Baud Rate	
	9600 v bps	
Default		Next


L. Decoue Jettings. OANT decoung settings	2.	Decode	Settings:	UART	decoding	settings
--	----	--------	-----------	------	----------	----------

General Format Data Bits Polarity /alidation								
Decode /alidation Data Bits Polarity 8 Polarity Idle High Parity Stop Bits None I MSB First Invert Bits Report Size: 16	General	Format						
Alidation Bata Bits Polarity 8 Parity Stop Bits None MSB First Invert Bits Report Size: 16)ecode	Dete Bite	Delorit					
Parity Stop Bits None • 1 • MSB First Invert Bits Report Size: 16 •	lidation/	Data Bits	- Idle H	y iah				
None Image: Copy prior MSB First Invert Bits Report Size: 16		Parity	Stop F	ite	-			
MSB First Invert Bits Report Size: 16 -		None	1	10	•			
MSB First Invert Bits Report Size: 16 -		INONE	·					
Report Size: 16 -		MSB First	nvert Bits					
		Report Size: 16						
		Treport bize. To v						



3. Electrical validation settings: Voltage, timing, frequency limitation

Decode	Customized EV Parameter:								
Validation	⊿ Baud Rate								
	Name Description	Min	Max						
	1 I J f _{UART} Baud rate for UART	-0.5 %	0.5 %						
	I Time								
	Name Description	Min	Max						
	1 t, Edge rise time	х	X						
	2 t _r Edge fall time	Х	X						
	3 ☑ t _{high} High time	98.958 µs	109.375 µs						
	4 √ t _{low} Low time	98.958 µs	109.375 µs						
	Voltage								
	Name Description	Min	Max						
	1 V _{Low} Low-level input voltage	-4.5 V	-5.5 V						
	2 ✔ V _{High} High-level input voltage	4.5 V	5.5 V						



4. Software electrical validation interface:



5. Software electrical validation control panel:



6. Overview Report:





7. Detail Report:



8. Reference Point Dialog & Waveform:





9. Html Report:



Electrical Validation Report

Test Instrument Model	MS03124V
Test Instruments Serial Number	MSV31240017
Test Date	04-27-2023 15:07:32
S/W Version	1.0.25
Protocol	UART(RS232)

Overview Results:

Total:	3
Pass:	2
Fail:	1

index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f UART	Baud rate for UART	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	-100.0%	-80.0%	✓Pass
2	VLow	Low-level input voltage	-7.200 V	-8.800 V	-8.759 V	-7.541 V	Vu 000.0	16.920 V	104	21.7%	-100.0%	×Fail
3	V _{High}	High-level input voltage	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	18.6%	-2.1%	✓Pass

V_{Low} - Test Result: Fail Description: Low-level input voltage

imit Min Limit Max N	lin Mean Max	Standard Deviation	on Count Margin	n Min Margin Ma	x				
7.200 V -8.800 V -8.7	59 V -7.541 V 0.000 uV	16.920 V	104 21.7%	-100.0%					
		Histogram							
Occurance (%) Total 10				Value Range	Occurance Count				
				-8.759 V ~ -7.883 V	88				
90 86.3				-7.883 V ~ -7.007 V	0				
80 - 70 -				-7.007 V ~ -6.131 V	0				
60 · 50 ·				-6.131 V ~ -5.255 V	0				
40 - 30 -				-5.255 V ~ -4.38 V	0				
20 -		13	7	-4.38 V ~ -3.504 V	0				
10			Test Value	-3.504 V ~ -2.628 V	0				
-8.759 V		0	Vu 000.	-2.628 V ~ -1.752 V	0				
				-1.752 V ~ -876 mV	0				
Limit -7.200 V	· · ·		-8.800 V	-876 mV ~ 0 V	14				
Min		Detail Re	port Row: 18,	Test Index: 2	Иах			Detail Rep	ort Row: 16, Test Index
5 V +0.00 2 5 V +0.00	3 5 V +0.00 4 +0.00	H 40 μs -728 μs	UART(RS232) VI Stop <u>S/R: 1 MS</u>	alidation	5 V +0.00 2	5 V 3 5 V +0.00 3 +0.00	4 5V +0.00 H	20 µs -7.24 ms	UART(RS232) Validation Stop S/R: 1 MS/s
		÷							
1				**-*	1				- # - # - 4 - # - # - # - # - # - # - #
Decide		94			booke 73		3	-	



HTML Report Export

Introduction

Every EV Testing includes Html Report exporting. The Html report contains every testing item, limitation, result, max/min value, histogram and waveform screenshots.

🐻 Save as Html			×
C:\Users\User\Documents/Acute/MS3K//EV_Report	(Browse	
Report Title Electrical Validation Report			
Save Settings			
Save Html as: Uncombined 💌			
Set User Logo		Browse	
Additional User Info			
Advance	ОК	Cancel	

Save Settings:

- A. Save Html as: Uncombined/Combined file
 Uncombined: The images of the Html report will not be saved in Html file.
 Combined: The images are embedded in the Html report.
- B. Set User Logo:User can add their Logo to the report
- C. Additional User Info: This allows the user to type in any information that user want to put into the report.

Advance:



	Name	User-Defined Name	Mag. Min	Mag. Max	-	
1	f _{SCL}		1	1		f _{SCL} User Defined Name:
2	thd,sta		1	1		
3	tsu,sta		1	1		Magnification Minimum Imag
4	t _{HD,DAT}		1	1		x1
5	tsu,dat		1	1		Magnification Maximum Imag
6	tsu,sto		1	1		x1
7	t _{LOW}		1	1		
8	t _{HIGH}		1	1	-	Apply

- A. User can adjust the name of the test item that will be displayed in Html report.
- B. User can also adjust the image magnification in Html report.



Advanced Settings

Introduction

EV Testing is able to increase or decrease the default capture timing for each acquisition. Different protocol default clock count or bit rate is not the same. Because the speed of the protocols & the packet length are not the same. But sometimes it needs more packet length. That is why Acute add an advanced settings to adjust the timing.

*Advance Button will only show in EV Parameter Settings State



EV Advanced Settings:

×
💂 (Range = 50~8000)
OK Cancel



MSO/TS3000 series 64-Channel cascading

Introduction

One of the key features of the Acute MSO3K/TS3K oscilloscope is its multi-unit stacking capability, allowing for the stacking of up to 16 devices, achieving a maximum measurement capability of 64 channels at 250MS/s or 16 channels at 1GS/s simultaneously. In terms of its chassis design, the MSO3K/TS3K is specifically designed for stacking applications, featuring carefully designed positioning grooves that allow the oscilloscope to be perfectly aligned when stacked. Additionally, the oscilloscope's thermal performance has been thoroughly considered and includes dual-side heat vents to ensure there are no overheating issues during extended operation.

Regarding signal connections, users have the option to directly connect the test signal to the oscilloscope through standard BNC connectors or use passive probes or differential probes for more extensive measurements. Furthermore, Acute also offers a BNC to Probe Tip Adaptor, which can improve common measurement quality issues associated with traditional probes, ensuring users obtain the most accurate measurement results.



Software User Interface

1. 64Channel @ 250MS/s



2. 16Channel @ 1GS/s





Connection

1. Connect with BNC to BNC Probe



2. Connect with Passive Probe





3. Connect with Passive Probe & BNC to Probe Tip Adaptor



4. Connect with High Voltage Differential Probe





5. Cascading 16 Devices(64 Channels)





Cautions

- The MSO3K/TS3K instrument operates on a USB 3.0 interface and consumes approximately 4.5 to 7.7 watts during operation. It is recommended to connect it to a USB 3.0 port at the rear of your computer or use a USB 3.0 hub with its own power supply to ensure optimal measurement quality.
- 2. The MSO3K/TS3K instrument has undergone internal testing and can operate for extended periods without overheating even in a stacked configuration. However, when using the instrument for an extended period in high-temperature or poorly ventilated environments, it is essential to monitor the operating temperature of the device and consider providing additional cooling measures if needed to prevent overheating (temperature exceeding 80 degrees Celsius) that could impact its operation.



3. When multiple units are stacked, there will be some level of phase difference between them due to differences in sampling rates. For example, at a 1GS/s sampling rate, the phase difference between the master unit and the first slave unit is < ±2ns, and between the master unit and the last slave unit is < ±3ns.</p>







Master & Slave (16th Device) Phase Delay

