2023

Acute®
PC-based T&M Instruments

Electrical Validation Documents

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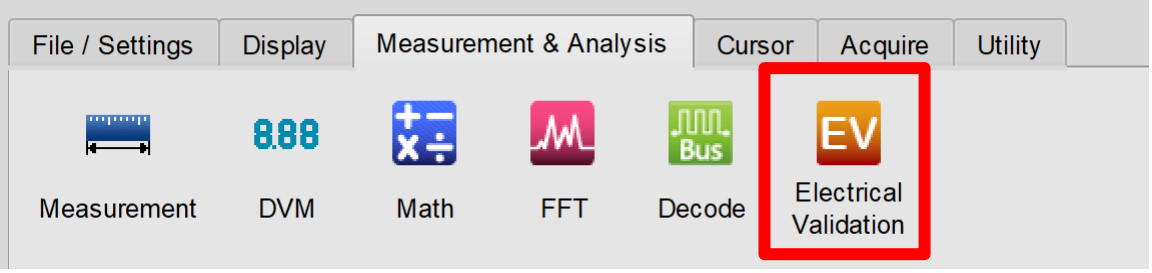
I2C Electrical Validation Solution

Introduction:



Use an oscilloscope to do I2C Electrical Validation to ensure that the I2C meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

I2C Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the I2C Speed.

Part of the electrical characteristics of common I2C specifications:

Table 13. Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I^2C-bus devices[1]

Symbol	Parameter	Conditions	C_b = 100 pF (max)		C_b = 400 pF[2]		Unit
			Min	Max	Min	Max	
f_{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
$t_{SU;STA}$	set-up time for a repeated START condition		160	-	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		160	-	320	-	ns
t_{HIGH}	HIGH period of the SCL clock		60	-	120	-	ns
$t_{SU;DAT}$	data set-up time		10	-	10	-	ns
$t_{HD;DAT}$	data hold time		0[3]	70	0[3]	150	ns
t_{rCL}	rise time of SCLH signal		10	40	20	80	ns
t_{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
t_{fCL}	fall time of SCLH signal		10	40	20	80	ns

The report of common I2C validation:

Overview | Detail | I2C

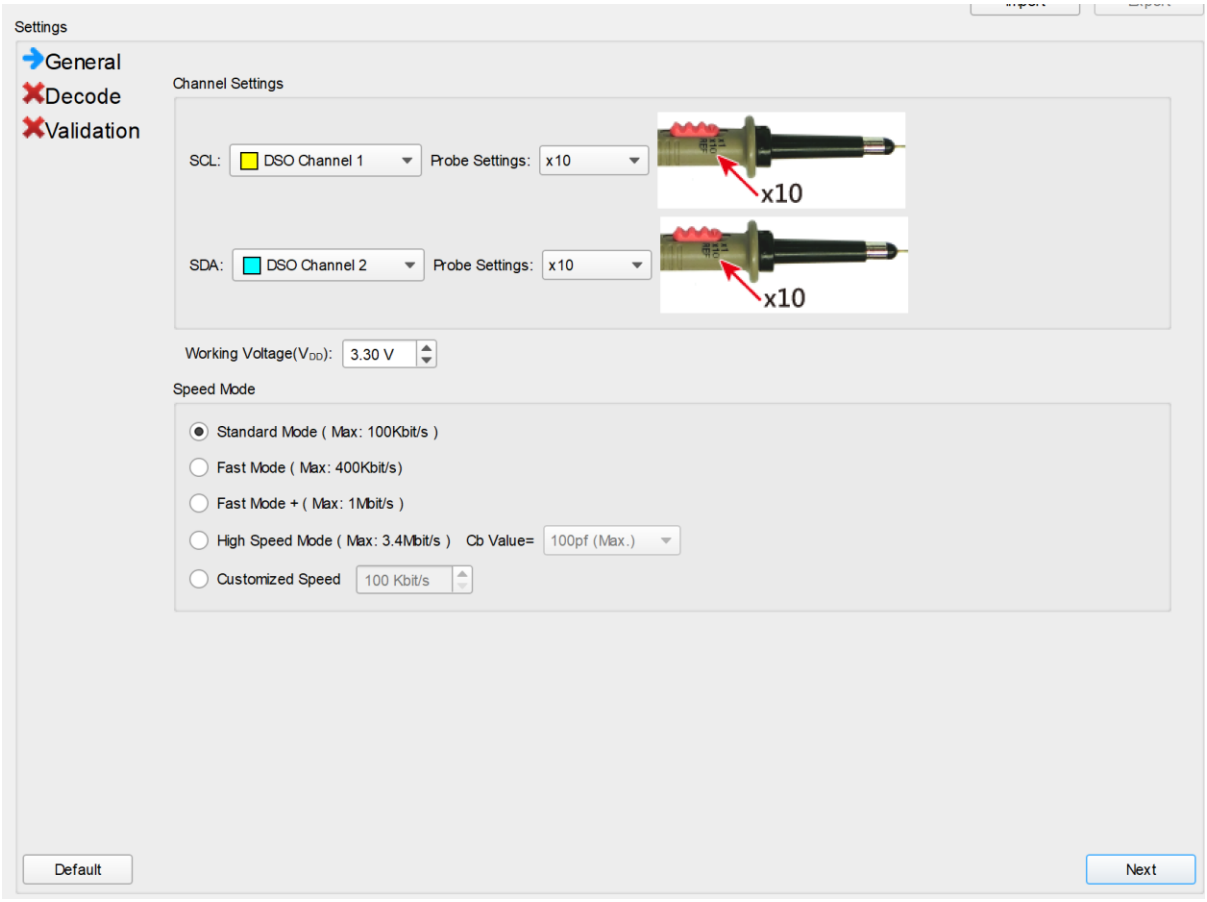
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	f_{SCL}	SCL clock frequencey	0.000 Hz	400.000 KHz	387.596 KHz	387.683 KHz	387.897 KHz	34200	Pass
2	$t_{HD;STA}$	Hold time(repeated) START condition	600.000 ns	—	1.536 us	1.537 us	1.540 us	200	Pass
3	$t_{SU;STA}$	Set-up time for a repeated START condition	600.000 ns	—	2.010 us	2.012 us	2.014 us	100	Pass
4	$t_{HD;DAT}$	Data hold time	—	—	94.000 ns	274.110 ns	1.028 us	17250	Pass
5	$t_{SU;DAT}$	Data Set-up time	100.000 ns	—	472.000 ns	1.066 us	1.444 us	25100	Pass
6	$t_{SU;STO}$	Set-up time for STOP condition	—	—	—	—	—	0	—
7	t_{LOW}	Low Period of the SCL Clock	1.300 us	—	1.538 us	1.542 us	1.544 us	34100	Pass
8	t_{HIGH}	High Period of the SCL Clock	600.000 ns	—	974.000 ns	982.475 ns	3.560 us	41800	Pass
9	t_{rCL}	Rise time of SCL signal	20.000 ns	300.000 ns	45.999 ns	50.304 ns	51.999 ns	41800	Pass
10	t_{fCL}	Fall time of SCL signal	20.000 ns	300.000 ns	10.000 ns	10.528 ns	11.999 ns	41800	Fail
11	t_{rDA}	Rise time of SDA signal	20.000 ns	300.000 ns	37.999 ns	39.210 ns	41.999 ns	9300	Pass
12	t_{fDA}	Fall time of SDA signal	20.000 ns	300.000 ns	4.000 ns	6.714 ns	10.000 ns	9900	Fail
13	t_{BUF}	Bus free time between a STOP and START condition	—	—	—	—	—	0	—
14	$t_{VD;DAT}$	Data valid time	—	900.000 ns	98.000 ns	267.062 ns	1.068 us	15750	Fail
15	$t_{VD;ACK}$	Data valid acknowledge time	—	900.000 ns	98.000 ns	623.009 ns	1.068 us	1500	Fail

Dedicated page for Electrical Validation:

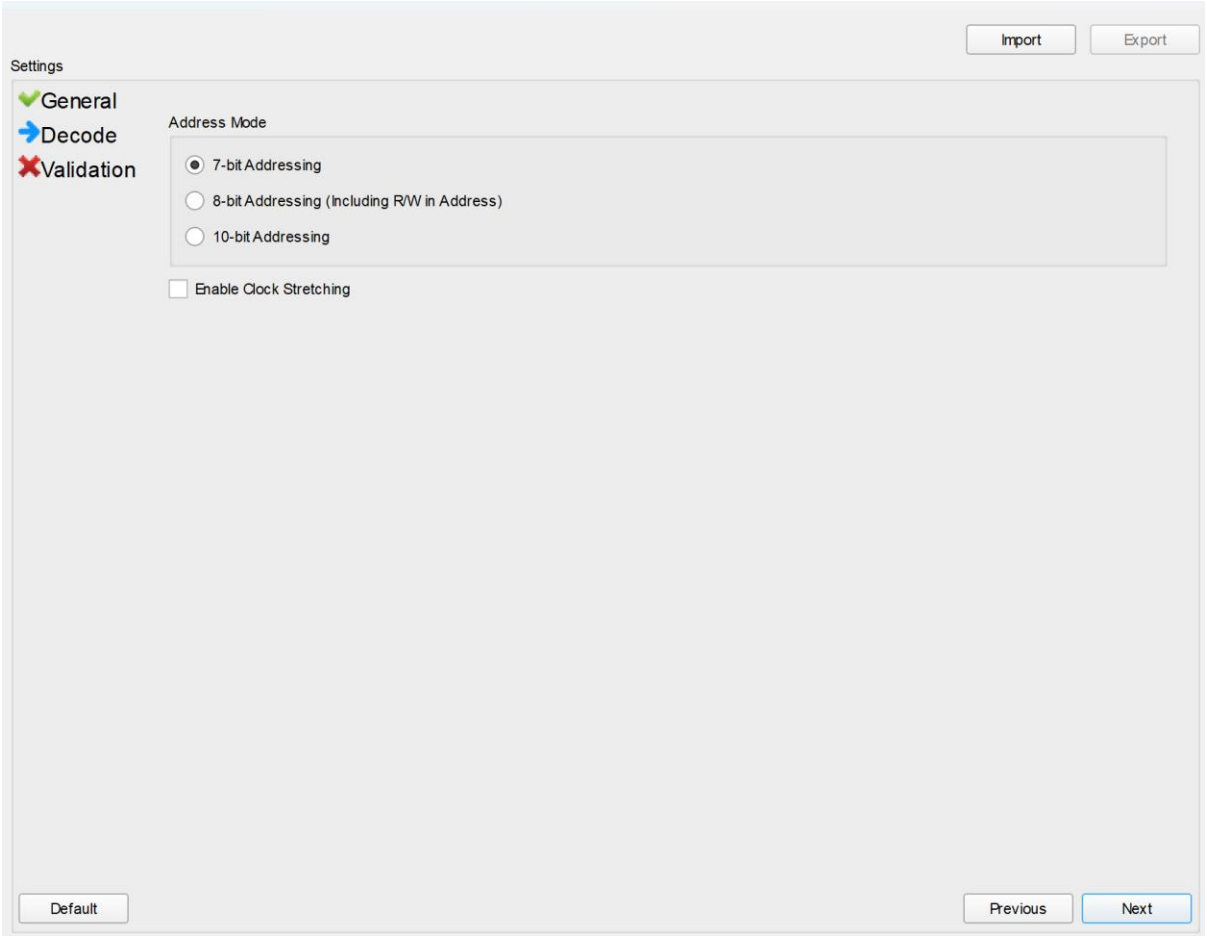
1. Different Speed Mode including Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
2. Frequency: Clock speed
3. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
4. Voltage: V_IL, V_IH, etc.

I2C Electrical Validation Settings:

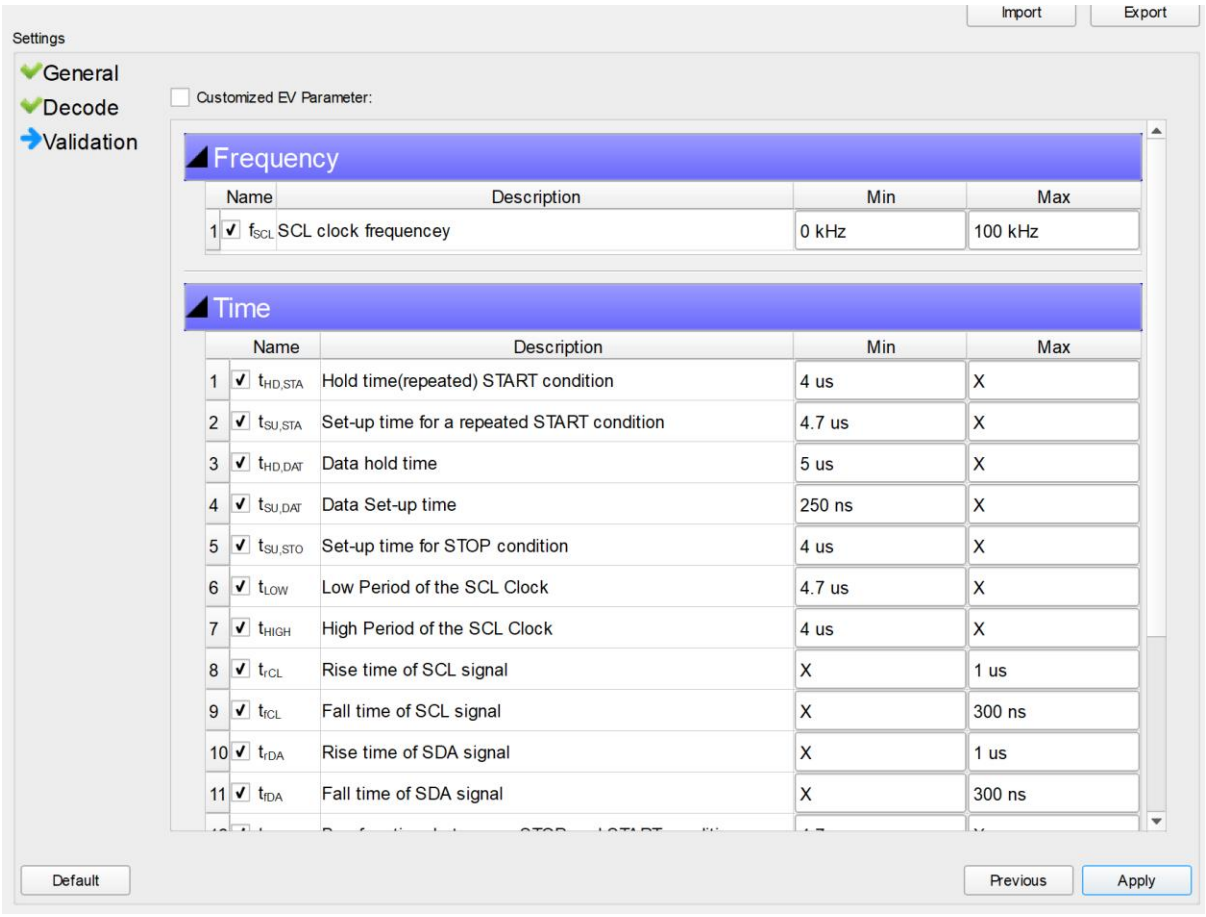
1. General Settings: Channel sources, working voltage and speed



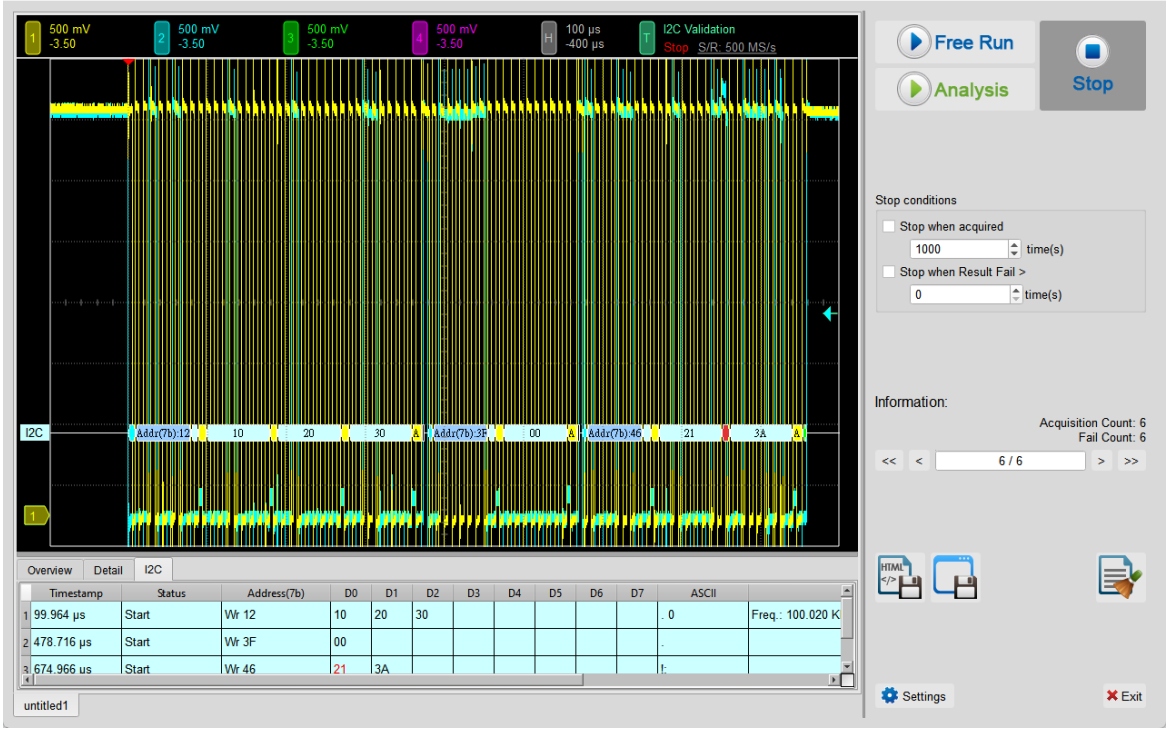
2. Decode Settings: I2C decoding settings



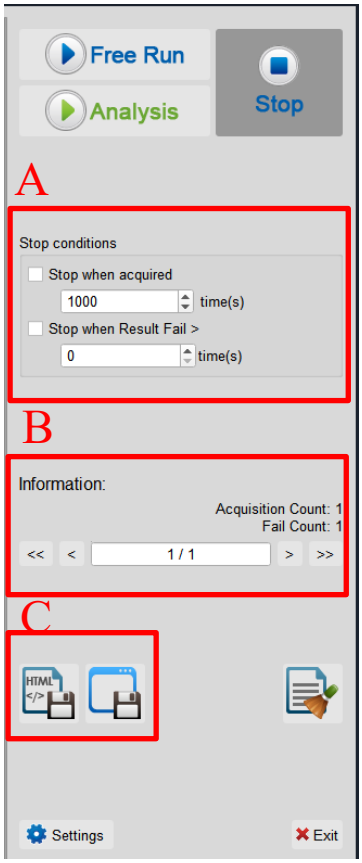
3. Electrical validation settings: Voltage, timing, frequency limitation



4. Software electrical validation interface:



5. Software electrical validation control panel:



A. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

B. Information:

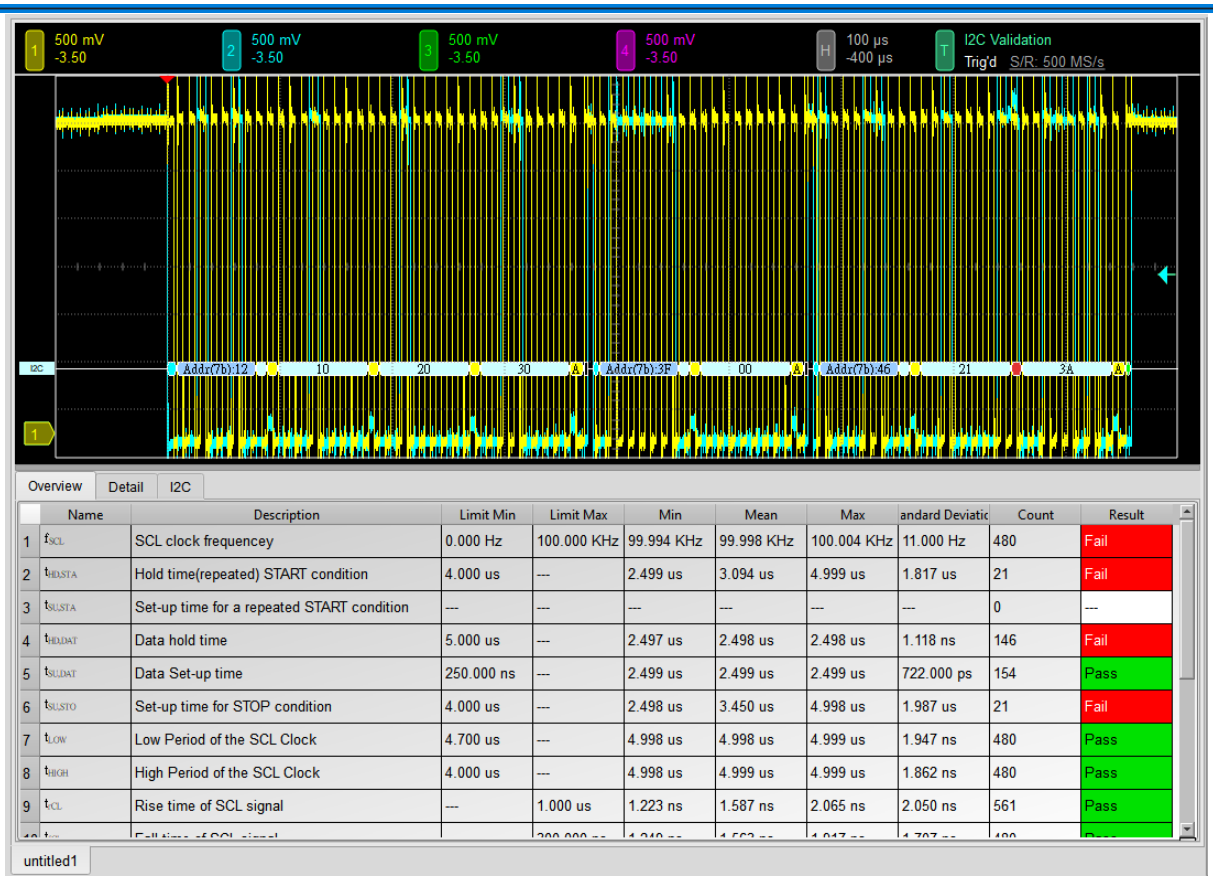
Select waveform

C. Save File:

Save as Html

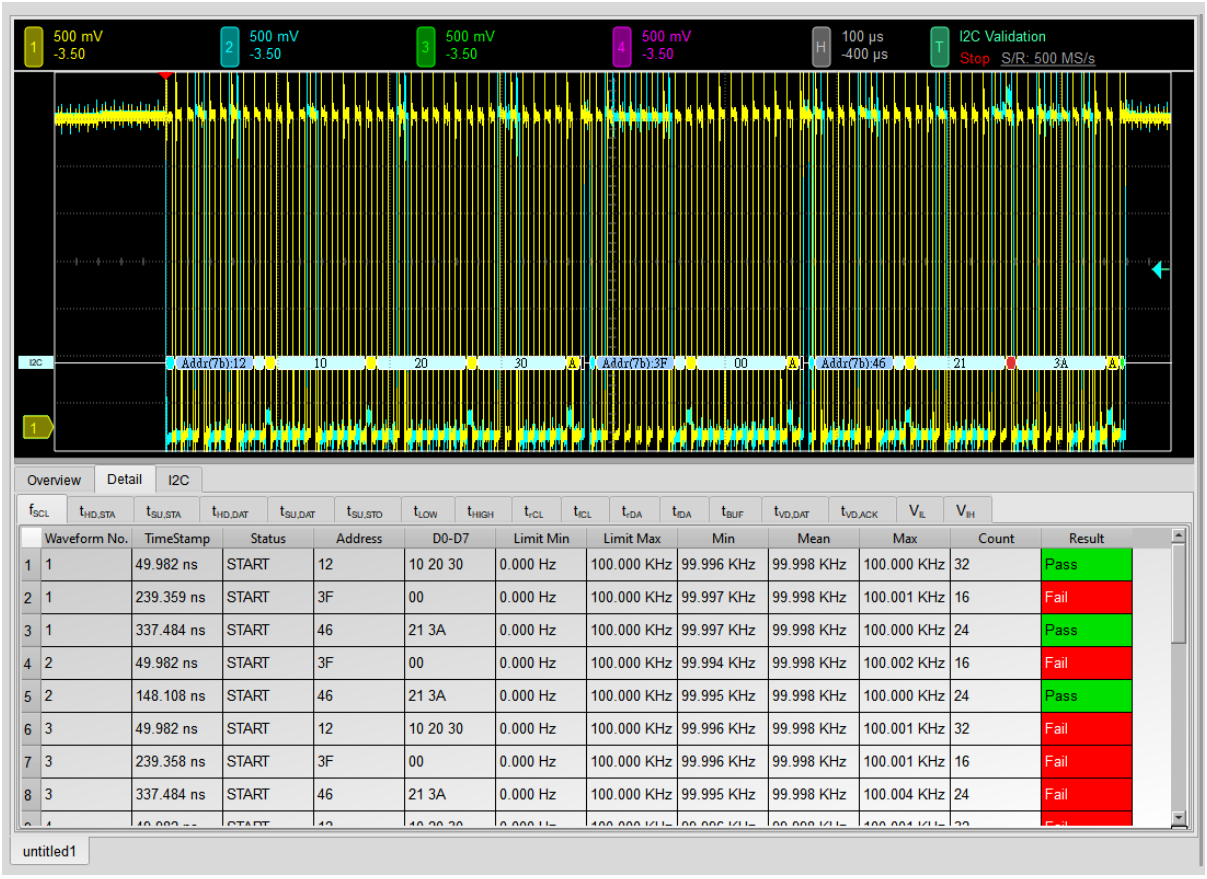
Save as .MOW(Software format)

6. Overview Report:



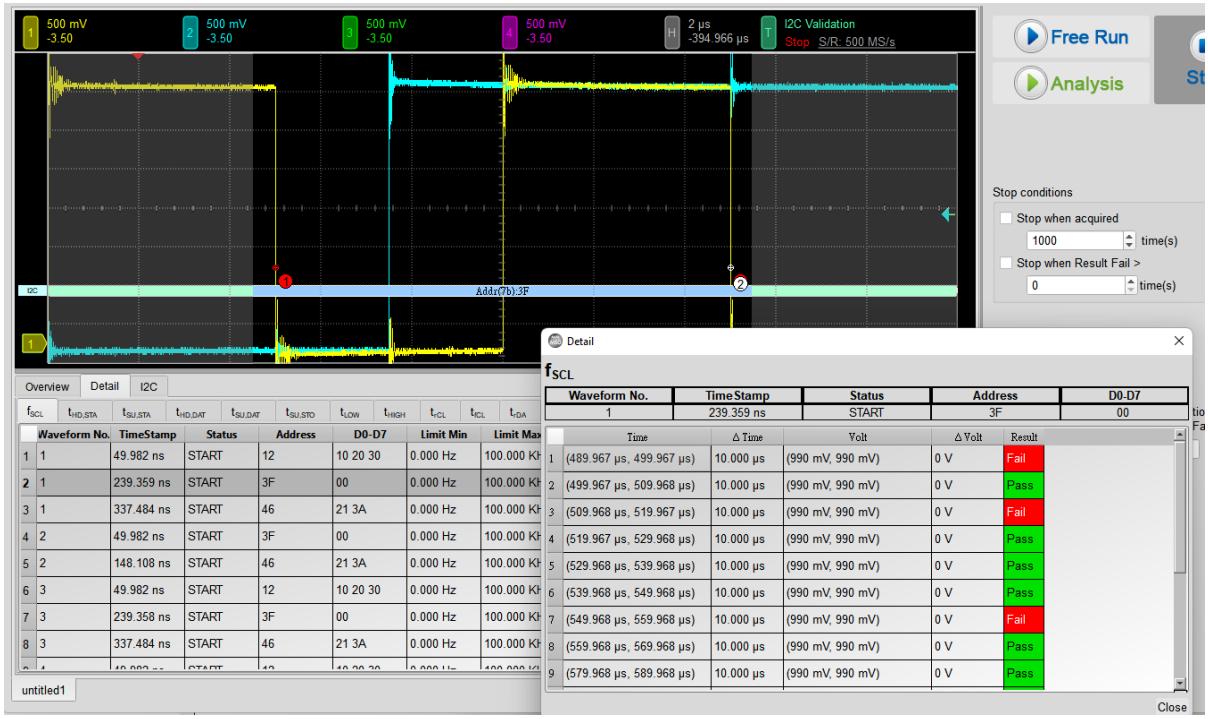
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviatic	Count	Result
1	f_{SCL}	SCL clock frequencey	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.004 KHz	11.000 Hz	480	Fail
2	$t_{HD,STA}$	Hold time(repeated) START condition	4.000 us	---	2.499 us	3.094 us	4.999 us	1.817 us	21	Fail
3	$t_{SU,STA}$	Set-up time for a repeated START condition	---	---	---	---	---	---	0	---
4	$t_{HD,DAT}$	Data hold time	5.000 us	---	2.497 us	2.498 us	2.498 us	1.118 ns	146	Fail
5	$t_{SU,DAT}$	Data Set-up time	250.000 ns	---	2.499 us	2.499 us	2.499 us	722.000 ps	154	Pass
6	$t_{SU,STO}$	Set-up time for STOP condition	4.000 us	---	2.498 us	3.450 us	4.998 us	1.987 us	21	Fail
7	t_{LOW}	Low Period of the SCL Clock	4.700 us	---	4.998 us	4.998 us	4.999 us	1.947 ns	480	Pass
8	t_{HIGH}	High Period of the SCL Clock	4.000 us	---	4.998 us	4.999 us	4.999 us	1.862 ns	480	Pass
9	t_{rCL}	Rise time of SCL signal	---	1.000 us	1.223 ns	1.587 ns	2.065 ns	2.050 ns	561	Pass

7. Detail Report:



	Waveform No.	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.000 KHz	32	Pass
2	1	239.359 ns	START	3F	00	0.000 Hz	100.000 KHz	99.997 KHz	99.998 KHz	100.001 KHz	16	Fail
3	1	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.997 KHz	99.998 KHz	100.000 KHz	24	Pass
4	2	49.982 ns	START	3F	00	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.002 KHz	16	Fail
5	2	148.108 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.995 KHz	99.998 KHz	100.000 KHz	24	Pass
6	3	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.001 KHz	32	Fail
7	3	239.358 ns	START	3F	00	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.001 KHz	16	Fail
8	3	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.995 KHz	99.998 KHz	100.004 KHz	24	Fail

8. Reference Point Dialog & Waveform:



9. Html Report:

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Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	24554
Test Date	04-17-2023 14:46:14
S/W Version	1.0.25
Protocol	I2C

```
/*****************************/
DUT INFO

Speed: 400KHz

EEPROM Communication
/*****************************/
```

Overview Results:

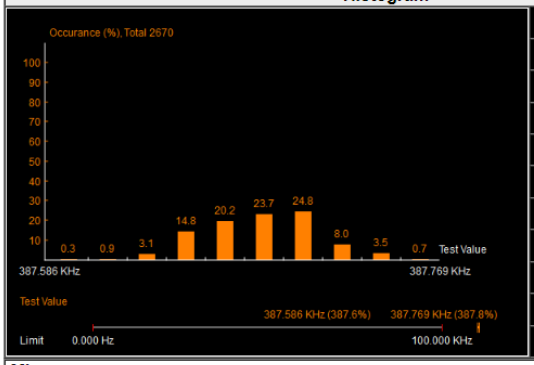
Total: 17
Pass: 9
Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCL}	SCL clock frequency	0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%	✘Fail
2	$t_{HD,STA}$	Hold time(repeated) START condition	4.000 us	---	1.538 us	1.538 us	1.539 us	427.000 ps	20	-61.6%	---	✘Fail
3	$t_{SU,STA}$	Set-up time for a repeated START condition	4.700 us	---	2.013 us	2.014 us	2.015 us	579.000 ps	10	-57.2%	---	✘Fail
4	$t_{HD,DAT}$	Data hold time	5.000 us	---	94.249 ns	247.342 ns	1.026 us	4.244 us	1575	-98.1%	---	✘Fail
5	$t_{SU,DAT}$	Data Set-up time	250.000 ns	---	472.837 ns	1.187 us	1.443 us	5.255 us	1767	18.7%	---	✔Pass
6	$t_{SU,STO}$	Set-up time for STOP condition	---	---	---	---	---	---	0	---	---	---
7	t_{LOW}	Low Period of the SCL Clock	4.700 us	---	1.539 us	1.541 us	1.543 us	9.208 ns	2670	-67.3%	---	✘Fail
8	t_{HIGH}	High Period of the SCL Clock	4.000 us	---	977.699 ns	979.666 ns	984.826 ns	20.914 ns	3040	-75.6%	---	✘Fail
9	t_{rCL}	Rise time of SCL signal	---	1.000 us	45.022 ns	48.118 ns	49.835 ns	14.531 ns	3430	---	0.5%	✔Pass
10	t_{fCL}	Fall time of SCL signal	---	300.000 ns	9.888 ns	10.237 ns	10.583 ns	1.448 ns	3430	---	0.2%	✔Pass
11	t_{rDA}	Rise time of SDA signal	---	1.000 us	37.719 ns	39.529 ns	41.848 ns	5.148 ns	927	---	0.4%	✔Pass
12	t_{fDA}	Fall time of SDA signal	---	300.000 ns	4.616 ns	6.893 ns	9.828 ns	24.035 ns	947	---	1.8%	✔Pass
13	t_{BUF}	Bus free time between a STOP and START condition	---	---	---	---	---	---	0	---	---	---
14	$t_{VD,DAT}$	Data valid time	---	3.450 us	98.898 ns	270.164 ns	1.067 us	4.200 us	1585	---	28.9%	✔Pass
15	$t_{VD,ACK}$	Data valid acknowledge time	---	3.450 us	141.017 ns	730.257 ns	1.067 us	1.344 us	91	---	28.0%	✔Pass
16	V_{IL}	Low-level input voltage	-500.000 mV	990.000 mV	-105.670 mV	27.063 mV	104.081 mV	760.863 mV	4367	26.5%	40.5%	✔Pass
17	V_{IH}	High-level input voltage	2.310 V	3.800 V	3.225 V	3.267 V	3.417 V	1.250 V	4367	61.4%	74.3%	✔Pass

f_{SCL} - Test Result: Fail
Description: SCL clock frequency

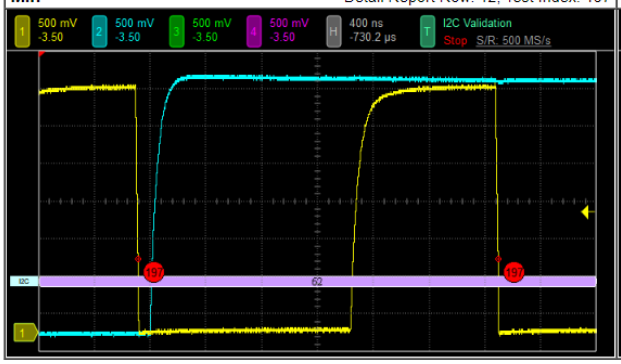
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%

Histogram

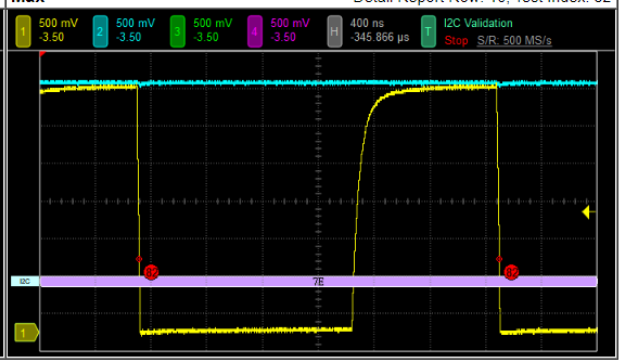


Value Range	Occurance Count
387.586 kHz ~ 387.604 kHz	9
387.604 kHz ~ 387.623 kHz	23
387.623 kHz ~ 387.641 kHz	84
387.641 kHz ~ 387.659 kHz	395
387.659 kHz ~ 387.677 kHz	539
387.677 kHz ~ 387.696 kHz	632
387.696 kHz ~ 387.714 kHz	663
387.714 kHz ~ 387.732 kHz	213
387.732 kHz ~ 387.751 kHz	94
387.751 kHz ~ 387.769 kHz	18

Min Detail Report Row: 12, Test Index: 197



Max Detail Report Row: 10, Test Index: 82



MIPI I3C Electrical Validation Solution

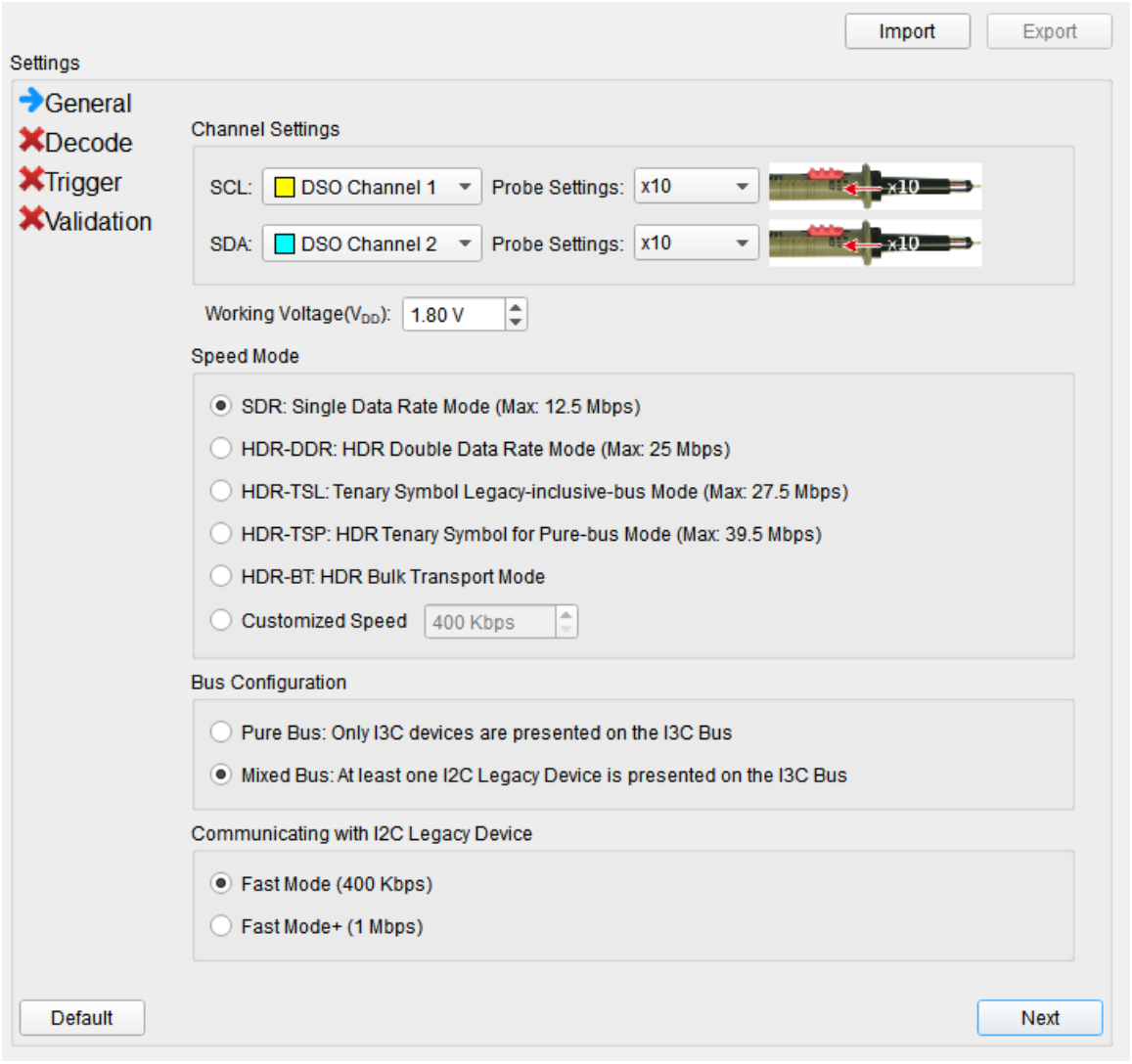
Introduction:

MIPI I3C is backward compatible with many Legacy I^2C Devices, but I3C Devices also support higher speed (with SCL clock speed up to 12.5 MHz) and new communication modes. MIPI I3C modes include **Single Data Rate (SDR) Mode**, **High Data Rate (HDR) Mode**. HDR Mode is also divided into **Dual Data Rate (HDR-DDR) Mode**, **Ternary Symbol Legacy Mode (HDR-TTL) Mode**, **Ternary Symbol Pure-bus (HDR-TSP) Mode**, and **Bulk Transport (HDR-BT) Mode**.

MIPI I3C Electrical Validation offers various electrical measurements compliance testing as specified in the MIPI I3C Specification (currently supports MIPI I3C version 1.1.1).

I3C Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

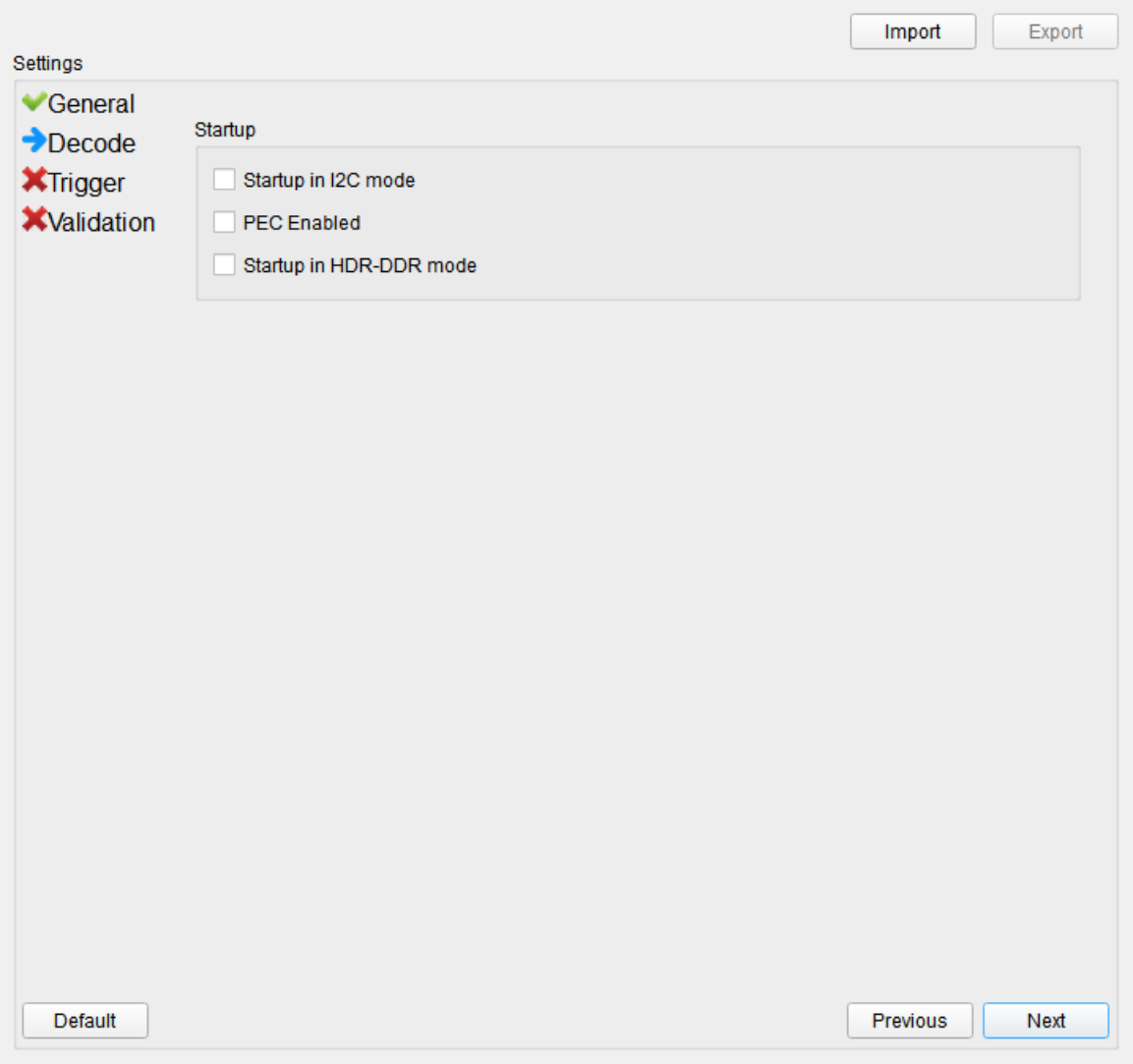


In the General Settings section, the selection of Speed Mode determines a suitable sample rate for validation, but also affects the timing specification table in the validation settings section. For instance, in HDR-TSL and HDR-TSP Mode, there are additional timing specifications listed in the table.

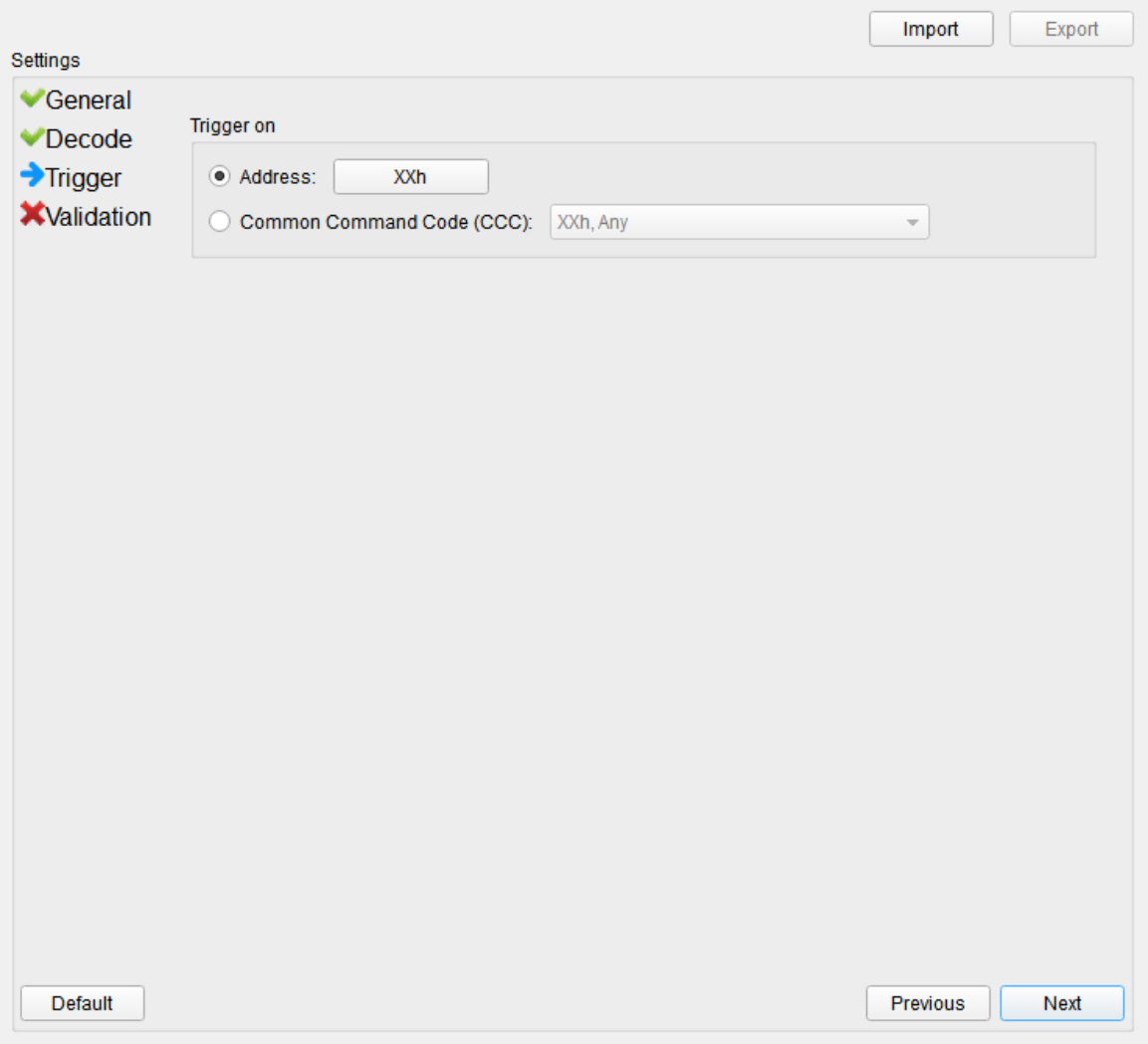
13	☑ t_{EDGE}	Edge-to-Edge Period	32 ns	X
14	☑ t_{SKEW}	Allow Difference Between Signals for 'Simultaneous' Change	X	12.8 ns
15	☑ t_{EYE}	Stable Condition Between Signals	12 ns	X
16	☑ t_{SYMBOL}	Time Between Successive Symbols	32 ns	X
17	☑ t_{CLOCK}	Symbol Clock	77.5 ns	X

Furthermore, the Bus Configuration section specifies the devices you connected on the I3C Bus. If it is a Pure-Bus setup, I^2C timing table is thus not required, which is discussed in the Validation Settings section. On the other hand, a Mixed Bus setup will include the timing table for I^2C Legacy Devices, and there default timing values are determined by using Fast Mode (Fm) or Fast Mode (Fm+) configuration, which is an identical settings to I^2C Electrical Validation setup.

2. Decode Settings

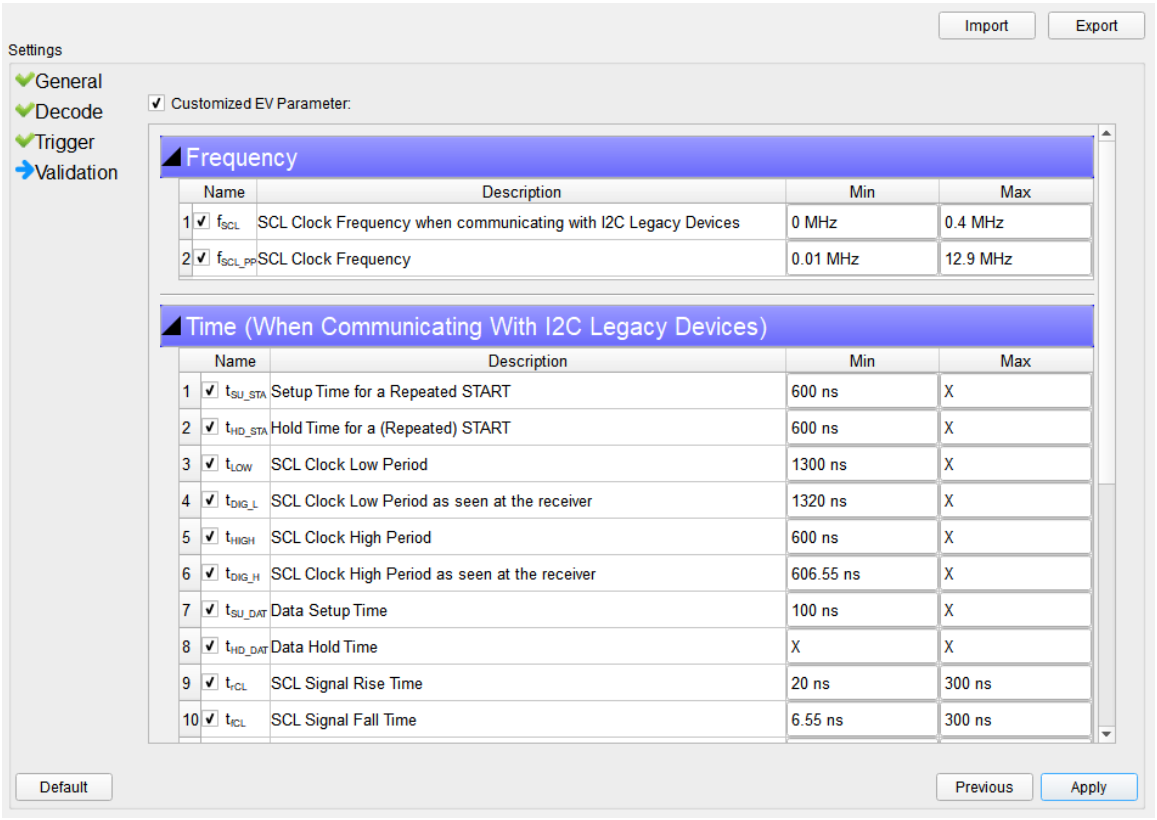


3. Trigger Settings



If you are interested in analyzing specific devices address, set the trigger address to the value you prefer. In the figure above, “XX” stands for don’t care term. Thus, it triggers on all address in this case. It also provides triggering on Common Command Code (CCC), which is specified on the Broadcast Address 7’h7E.

4. Validation Settings



This section includes 5 parameter tables, including

- Frequency
- I3C timing requirements when communicating with I^2C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

All specification table are listed below.

In the Pure Bus setup, the timing requirements table with I^2C Legacy Devices is not required and thus be hidden from the parameter settings dialog. The frequency parameter f_{SCL} will also be hidden in the Pure Bus setup.

I3C Frequency Requirements

Symbol	Electrical Parameter
f_{SCL}	SCL Clock Frequency when communicating with I^2C Legacy Devices[1]
t_{SCL_PP}	SCL Clock Frequency
t_{BT_FREQ}	HDR-BT SCL Clock Frequency

I3C Timing Requirements When Communicating With I^2C Legacy Devices[1]

Symbol	Electrical Parameter
t_{SU_STA}	Setup Time for a REPEATED START
t_{HD_STA}	Hold Time for a (REPEATED) START
t_{LOW}	SCL Clock Low Period
t_{DIG_L}	SCL Clock Low Period as seen at the receiver
t_{HIGH}	SCL Clock High Period
t_{DIG_H}	SCL Clock High Period as seen at the receiver
t_{SU_DAT}	Data Setup Time
t_{HD_DAT}	Data Hold Time
t_{rCL}	SCL Signal Rise Time
t_{fCL}	SCL Signal Fall Time
t_{rDA}	SDA Signal Rise Time
t_{rDA_OD}	SDA Signal Rise Time (Open Drain)
t_{fDA}	SDA Signal Fall Time
t_{SU_STO}	Setup Time for STOP
t_{BUF}	Bus Free Time Between a STOP and a START
t_{SPIKE}	Pulse Width of Spikes that Spike Filter Must Suppress

[1] Only available when the bus configuration is set to Mixed Bus (i.e. at least one I^2C legacy device is presented on the I3C bus).

I3C Open Drain Timing Requirements

Symbol	Electrical Parameter
t_{LOW_OD}	SCL Clock Low Period
$t_{DIG\_OD\_L}$	SCL Clock Low Period as seen at the receiver
t_{HIGH_INIT}	High Period of SCL Clock (for First Broadcast Address)
t_{HIGH_OD}	SCL Clock High Period
$t_{DIG\_OD\_H}$	SCL Clock High Period as seen at the receiver
t_{fDA_OD}	SDA Data Fall Time
t_{SU_OD}	SDA Data Setup Time During Open Drain Mode
t_{CAS}	Clock After START (S) Condition
t_{CBP}	Clock Before STOP (P) Condition
$t_{CRHPOverlap}$	Active Controller to Secondary Overlap time during handoff
t_{AVAL}	Bus Available Condition
t_{IDLE}	Bus Idle Condition
$t_{NEWCRLock}$	Time Interval Where New Controller Not Driving SDA Low

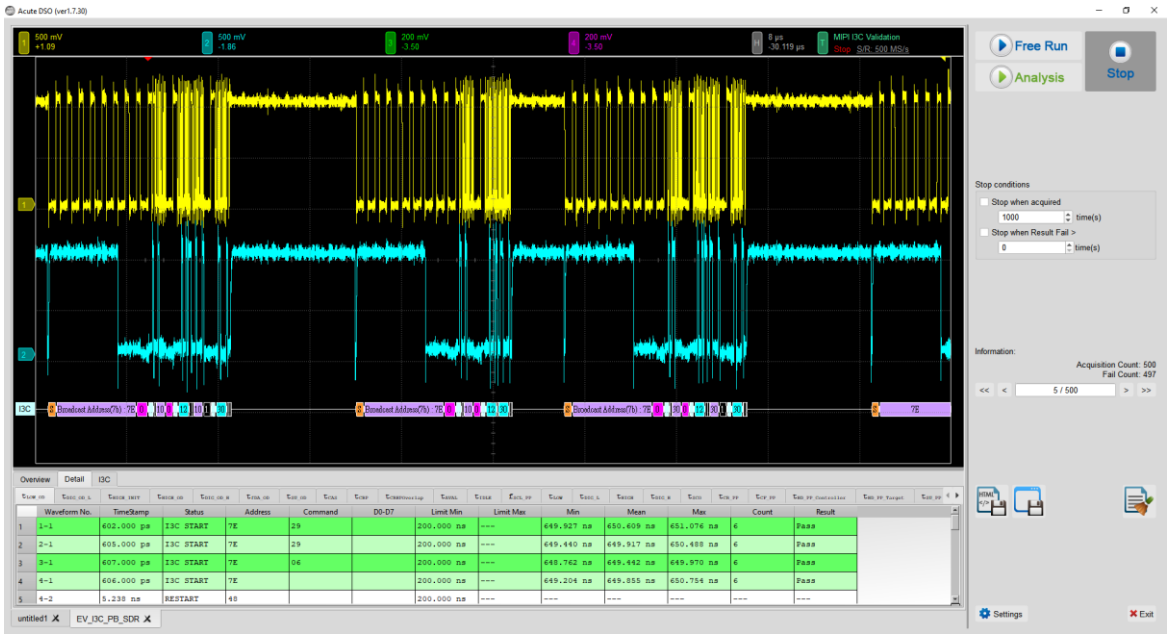
I3C Push-Pull Timing Requirements

Symbol	Electrical Parameter
t_{LOW}	SCL Clock Low Period
t_{DIG_L}	SCL Clock Low Period as seen at the receiver
t_{HIGH}	SCL Clock High Period
t_{DIG_H}	SCL Clock High Period as seen at the receiver
t_{SCO}	Clock in to Data Out for Target
t_{CR_PP}	SCL Clock Rise Time
t_{CF_PP}	SCL Clock Fall Time
$t_{HD\_PP\_Controller}$	SDA Signal Data Hold (Controller)
$t_{HD\_PP\_Target}$	SDA Signal Data Hold (Target)
t_{SU_PP}	SDA Signal Data Setup
t_{CASr}	Clock After Repeated START (Sr) Condition
t_{CBSr}	Clock Before Repeated START (Sr) Condition
t_{BT_HO}	HDR-BT Master to Slave Hand Off Delay
t_{BT_STALL}	HDR-BT Clocked Not-Ready Data-Block Headers

I3C I/O Stage Characteristics Voltage Requirements

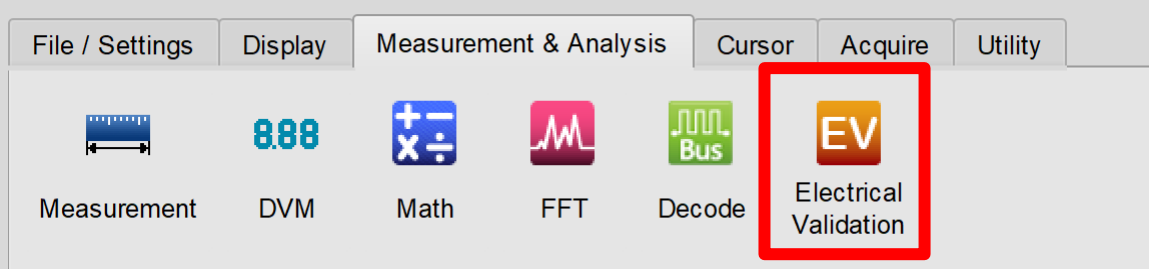
Symbol	Electrical Parameter
V_{IL}	Low-Level Input Voltage
V_{IH}	High-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage

5. Sample Result



PDM Electrical Validation Solution

Introduction:



Use an oscilloscope to do PCM Electrical Validation to ensure that the PDM meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

PDM Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the PDM baud rate.

Part of the electrical characteristics of common PDM specifications:

DIGITAL AUDIO INTERFACE					
PDM_CLK High Frequency Range	f_{CLKH}		5.28	8.64	MHz
PDM_CLK Low Frequency Range	f_{CLKL}		1.84	4.32	MHz
PDM_CLK High Time	t_{PDM_CLKH}		40		ns
PDM_CLK Low Time	t_{PDM_CLKL}		40		ns

The report of common PDM validation:

Overview | Detail | PDM

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f_{CLK}	Clock freq...	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass
2	t_{LOW}	Low Perio...	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass
3	t_{HIGH}	High Perio...	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass
4	t_{rCL}	Rise time ...	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass
5	t_{fCL}	Fall time o...	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass
6	t_{rDD}	Delay time...	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass
7	t_{rDV}	Delay time...	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass
8	t_{fDD}	Delay time...	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass
9	t_{fDV}	Delay time...	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass

Dedicated page for Electrical Validation:

5. Frequency: Clock speed
6. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
7. Voltage: VL, VH, etc.

Frequency:

Symbol	Electrical Parameter
f_{SCL}	PDM_CLK Frequency Range

Time:

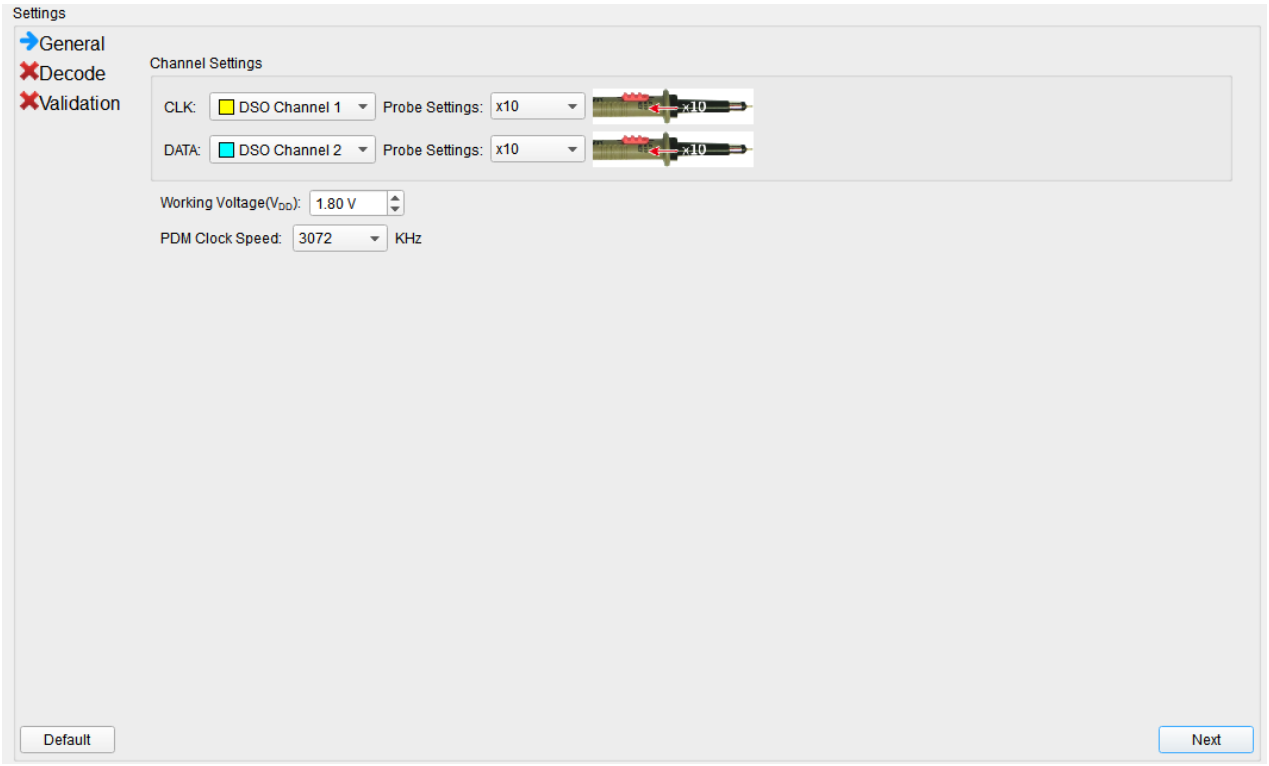
Symbol	Electrical Parameter
t_{LOW}	Low Period of the Clock
t_{HIGH}	High Period of the Clock
t_{rCL}	Rise time of Clock signal
t_{fCL}	Fall time of Clock signal
t_{rDD}	Delay time from Clock edge to Data Rise driven
t_{fDD}	Delay time from Clock edge to Data Fall driven
t_{rDV}	Delay time from Clock edge to Data Rise valid
t_{fDV}	Delay time from Clock edge to Data Fall valid

Voltage:

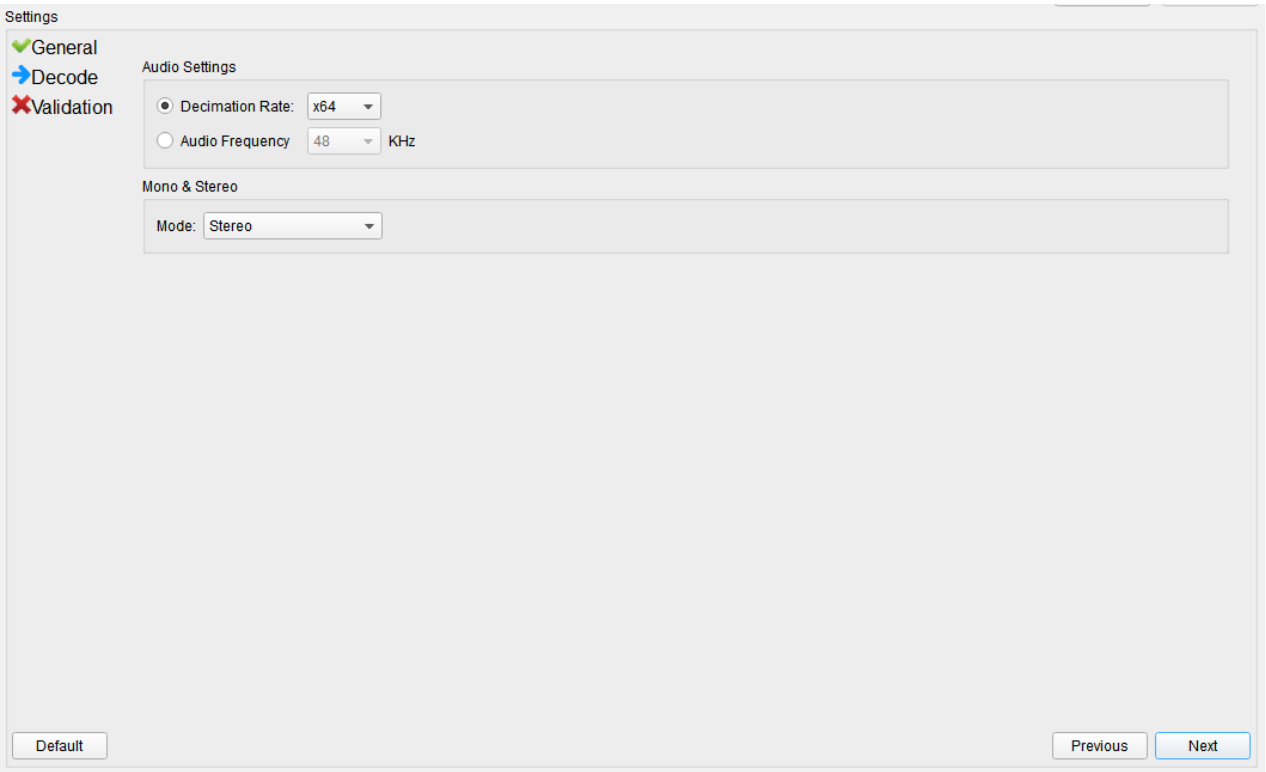
Symbol	Electrical Parameter
V_{ClkLow}	Low-level Input voltage for clock
$V_{ClkHigh}$	High-level Input voltage for clock
$V_{DataLow}$	Low-level Input voltage for data
$V_{DataHigh}$	High-level Input voltage for data

PDM Electrical Validation Settings:

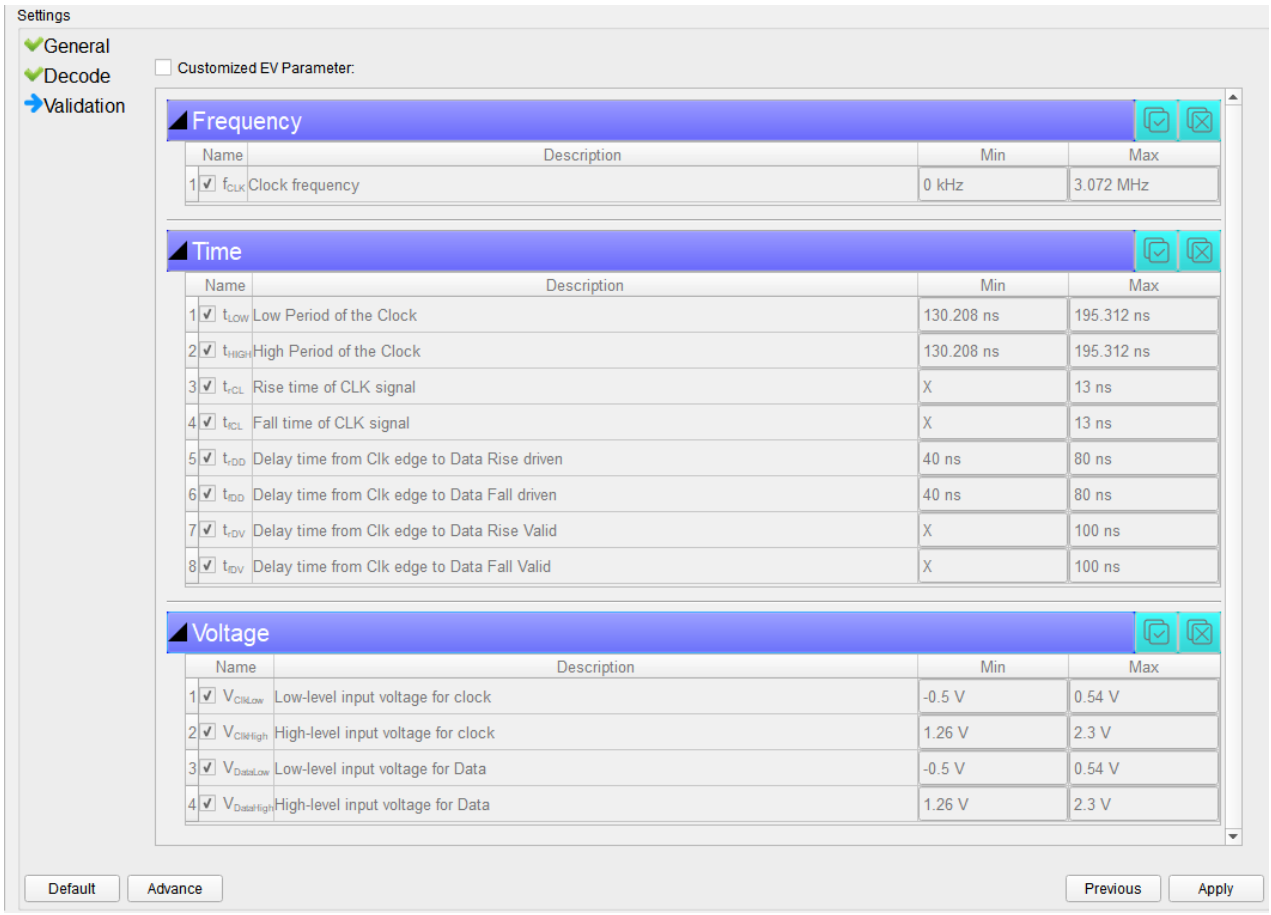
1. General Settings: Channel sources, working voltage and speed



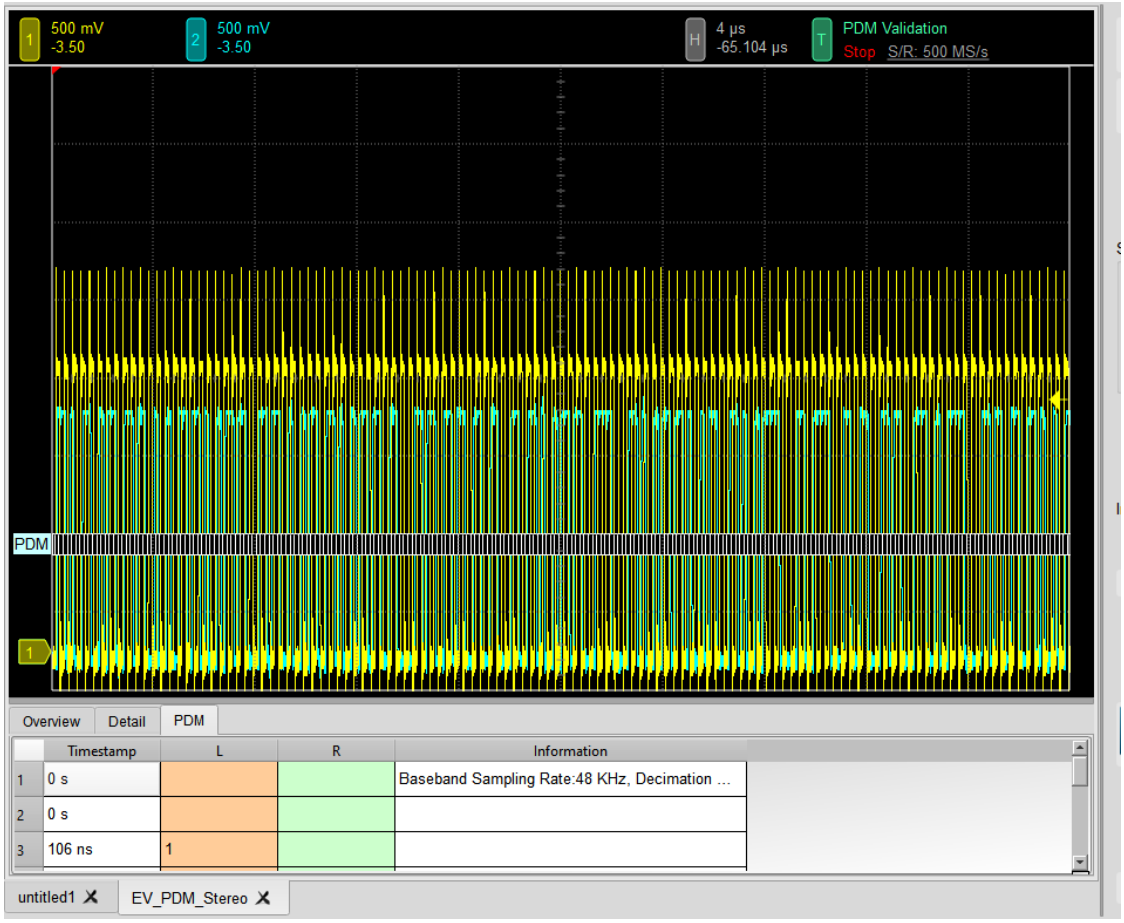
2. Decode Settings: PDM decoding settings



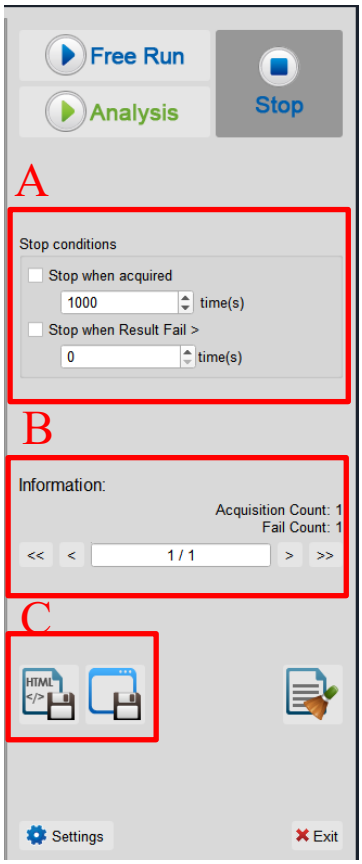
3. Electrical validation settings: Voltage, timing, frequency limitation



4. Software electrical validation interface:



5. Software electrical validation control panel:



A. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

B. Information:

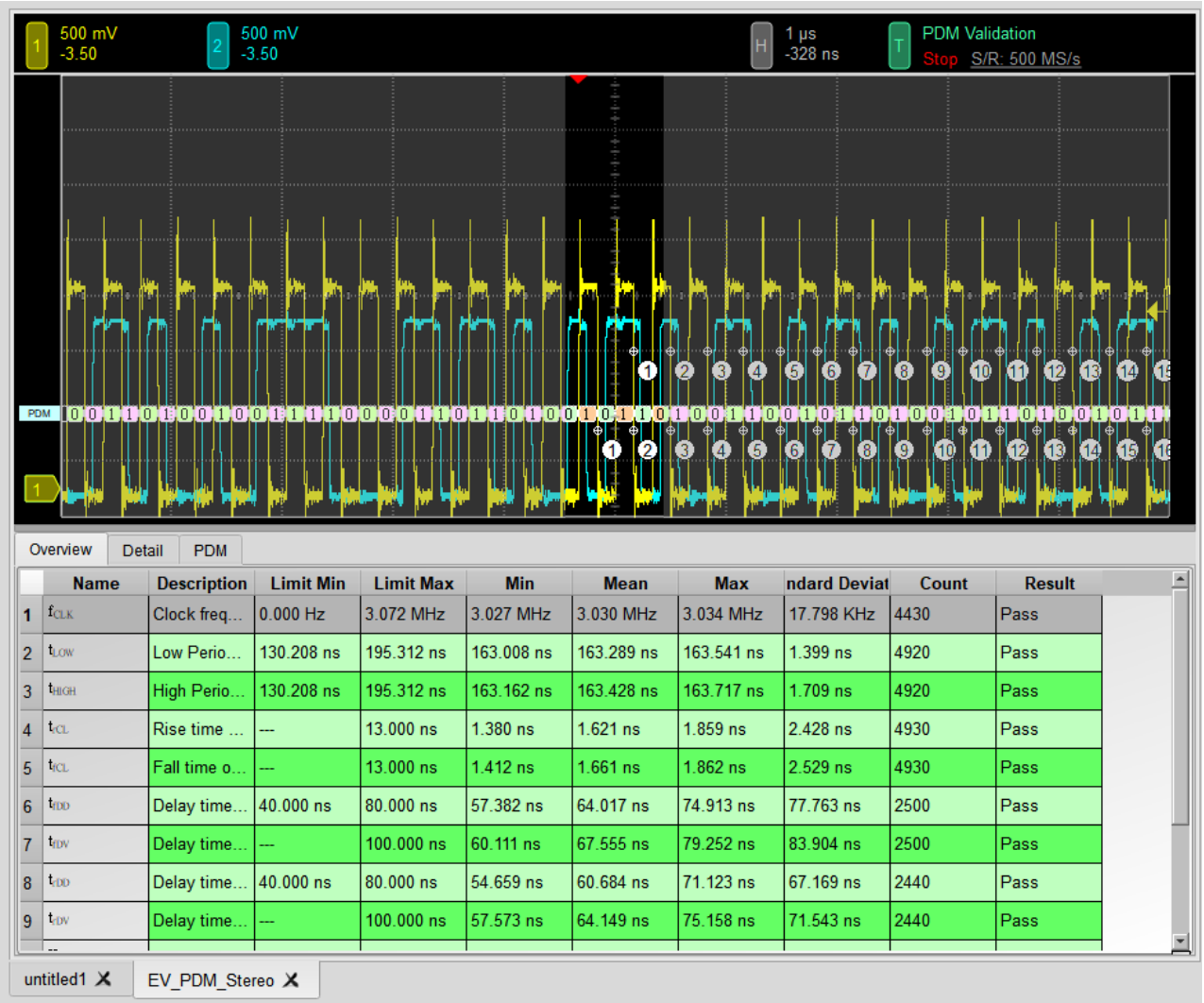
Select waveform

C. Save File:

Save as Html

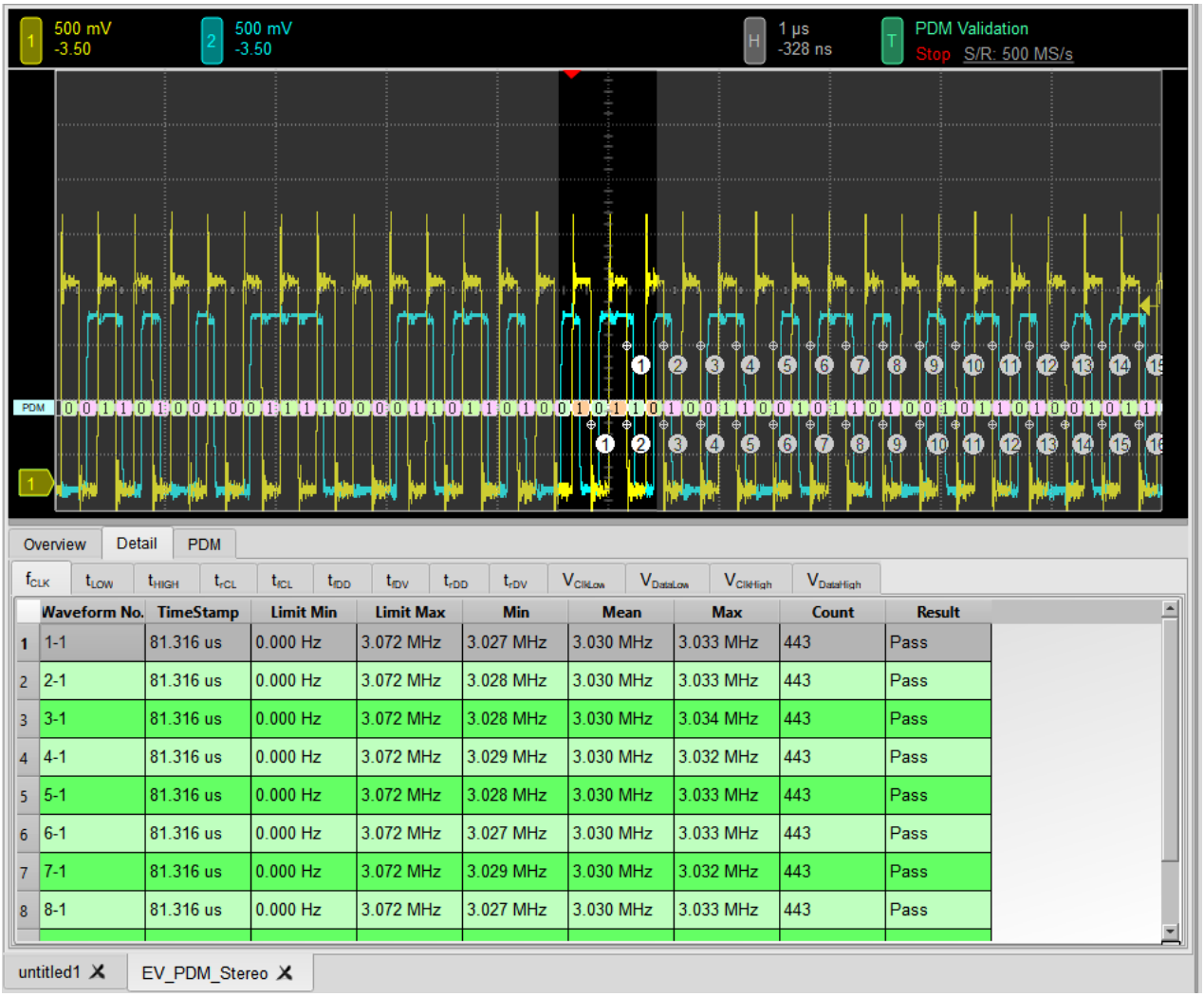
Save as .MOW(Software format)

6. Overview Report:



	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f_{CLK}	Clock freq...	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass
2	t_{LOW}	Low Perio...	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass
3	t_{HIGH}	High Perio...	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass
4	t_{rCL}	Rise time ...	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass
5	t_{fCL}	Fall time o...	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass
6	t_{fDD}	Delay time...	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass
7	t_{fDV}	Delay time...	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass
8	t_{rDD}	Delay time...	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass
9	t_{rDV}	Delay time...	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass

7. Detail Report:



	Waveform No.	TimeStamp	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass
2	2-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass
3	3-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.034 MHz	443	Pass
4	4-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass
5	5-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass
6	6-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass
7	7-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass
8	8-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass

8. Reference Point Dialog & Waveform:

9. Html Report:

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

Total: 13
Pass: 13
Fail: 0

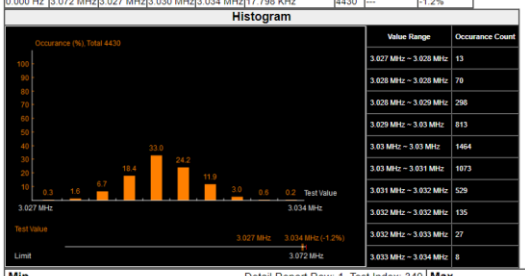
Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{CLK}	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%	✓Pass
2	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	t_{rCL}	Rise time of CLK signal	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	---	-85.7%	✓Pass
5	t_{fCL}	Fall time of CLK signal	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	---	-85.7%	✓Pass
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	t_{fDV}	Delay time from Clk edge to Data Fall Valid	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	---	-20.7%	✓Pass
8	t_{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	✓Pass
9	t_{rDV}	Delay time from Clk edge to Data Rise Valid	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	---	-24.8%	✓Pass
10	V_{ClkLow}	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	$V_{DataLow}$	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	$V_{ClkHigh}$	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	✓Pass
13	$V_{DataHigh}$	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

---

f_{CLK} - Test Result: Pass
Description: Clock frequency

Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%

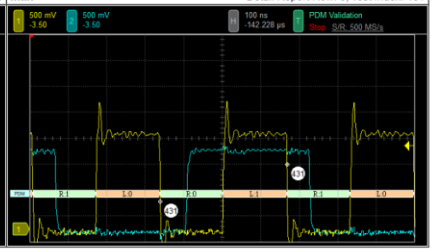
Histogram



Value Range	Occurance Count
3.027 MHz ~ 3.028 MHz	13
3.028 MHz ~ 3.028 MHz	78
3.028 MHz ~ 3.029 MHz	298
3.029 MHz ~ 3.03 MHz	813
3.03 MHz ~ 3.03 MHz	1464
3.03 MHz ~ 3.031 MHz	1073
3.031 MHz ~ 3.032 MHz	529
3.032 MHz ~ 3.032 MHz	135
3.032 MHz ~ 3.033 MHz	27
3.033 MHz ~ 3.034 MHz	8

Min Detail Report Row: 1, Test Index: 340

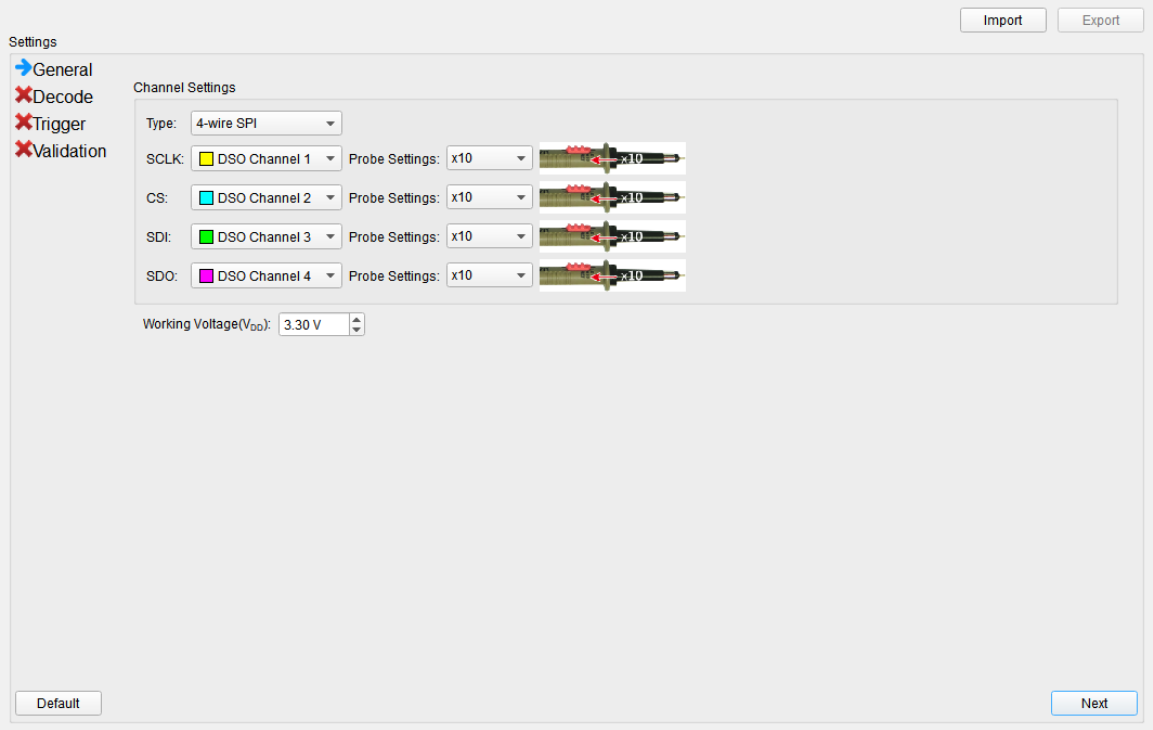
Max Detail Report Row: 3, Test Index: 431



SPI Electrical Validation User Guide

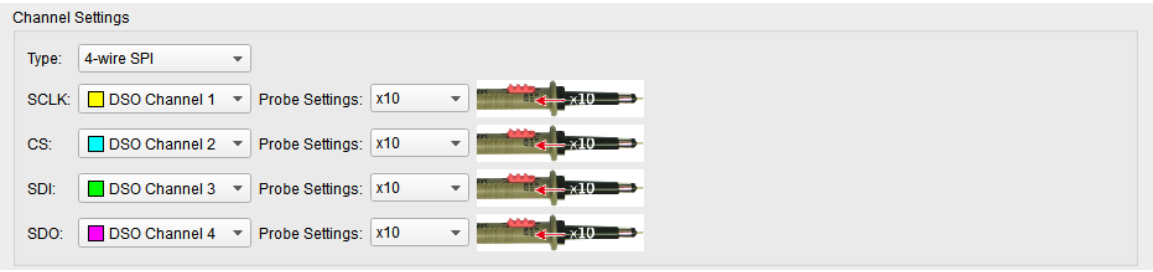
Settings Guide

1. General Settings

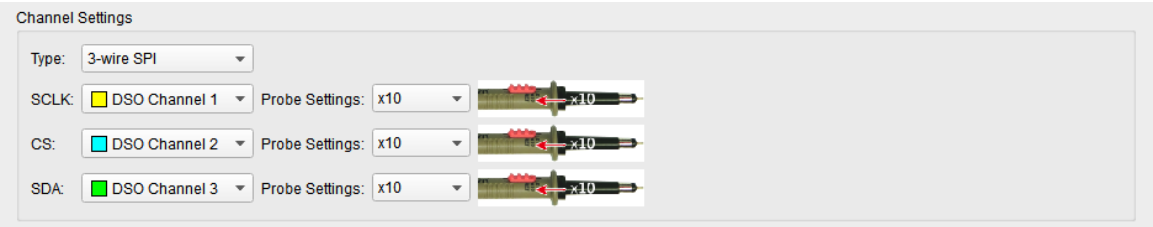


In the General Settings section, it is mandatory to select the type of SPI type, depending on your bus configuration (4-wire SPI or 3-wire SPI).

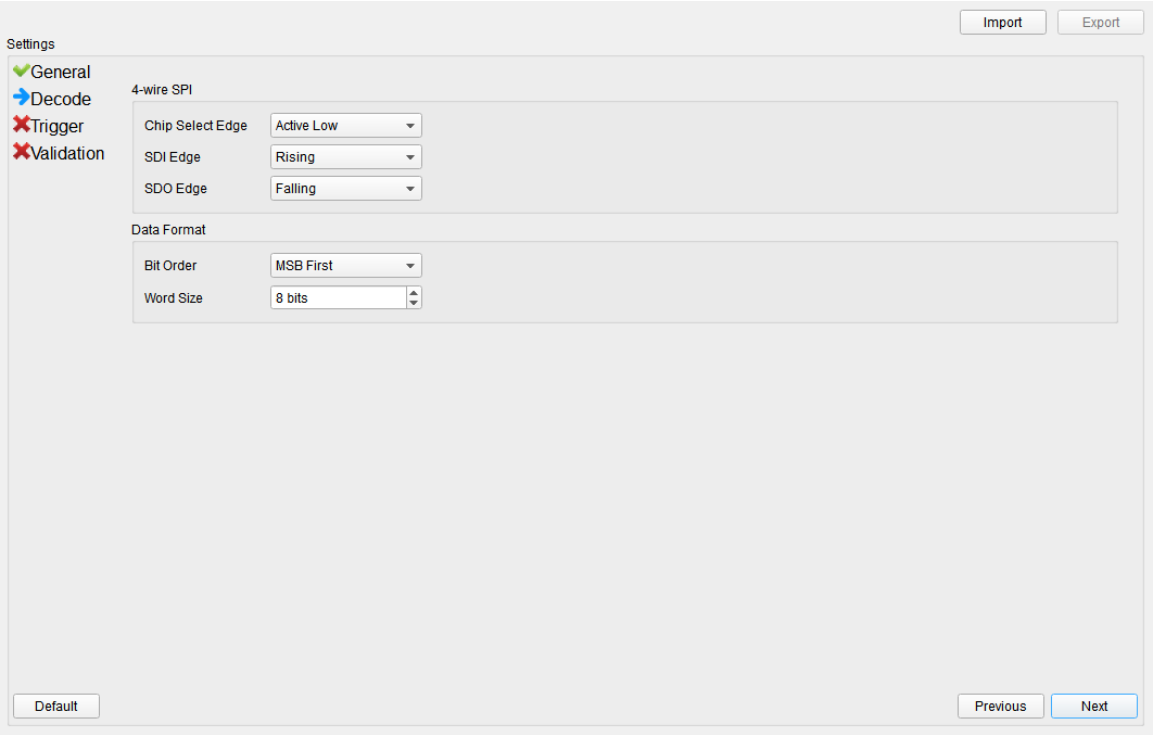
4-wire Channel Setup



3-wire Channel Setup

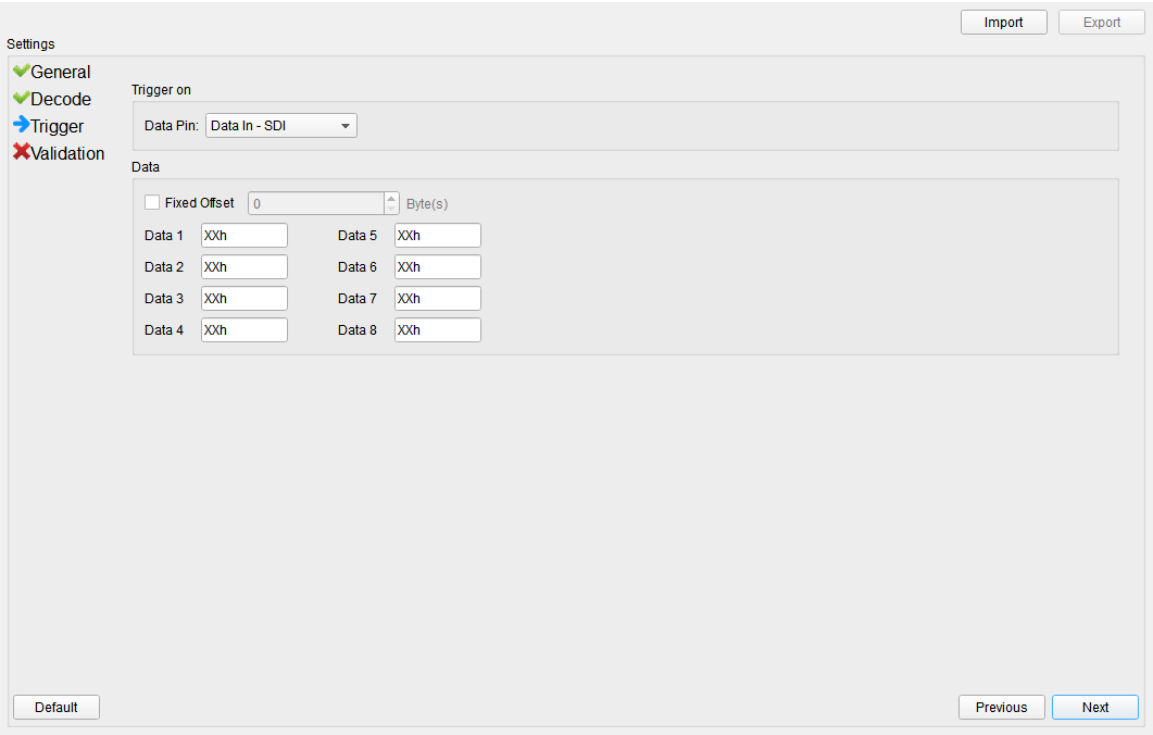


2. Decode Settings



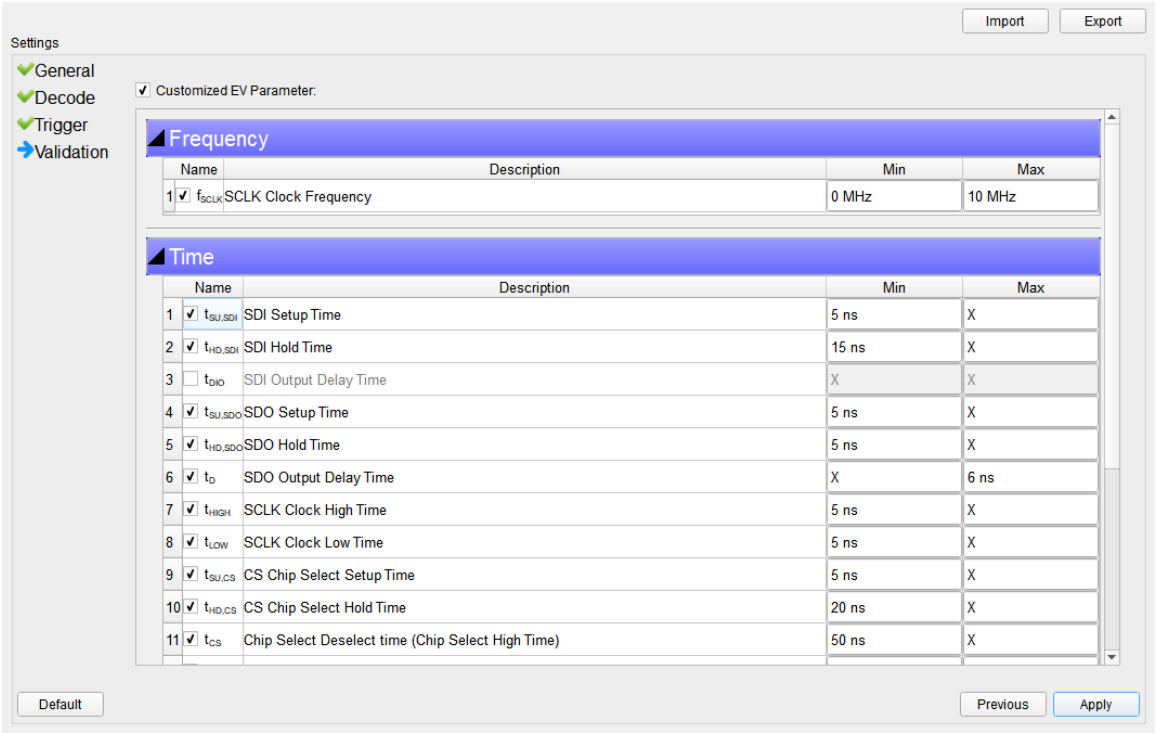
In the Decode Settings, it requires you to setup the SPI data format and the Latching Edge of each channel. The SPI data format set here is applied both to the Decode and Trigger Settings.

3. Trigger Settings



The data format is set on the previous page. The remaining setup is all about the data address and which data pin to trigger.

4. Validation Settings



There are no standard measurement limits defined for SPI bus. Therefore, it is recommended to define your own limits while validate SPI signals.

This section displays 3 characteristics table, including

- Frequency
- Timing parameters
- Voltage requirements

All supported validation parameters' symbols and descriptions are listed in the table below.

SPI Frequency Requirements

Symbol	Electrical Parameter
f_{SCLK}	SCLK Clock Frequency

SPI Timing Requirements

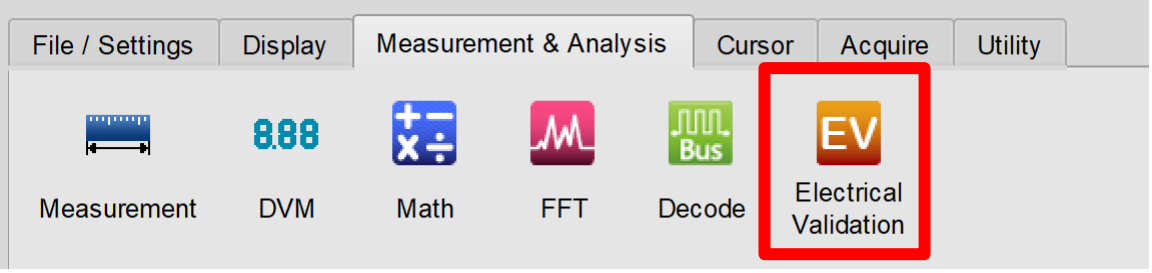
Symbol	Electrical Parameter
$t_{SU,SDI}$	SDI Setup Time
$t_{HD,SDI}$	SDI Hold Time
t_{DIO}	SDI Output Delay Time
$t_{SU,SDO}$	SDO Setup Time
$t_{HU,SDO}$	SDO Hold Time
t_D	SDO Output Delay Time
t_{HIGH}	SCLK High Time
t_{LOW}	SCLK Low Time
$t_{SU,CS}$	CS Chip Select Setup Time
$t_{SU,CS}$	CS Chip Select Hold Time
t_{CS}	Chip Select Deselect time (Chip Select High Time)
t_{CLKr}	SCLK Clock Rise Time
t_{CLKf}	SCLK Clock Fall Time

SPI Voltage Requirements

Symbol	Electrical Parameter
V_{IL}	Low-Level Input Voltage
V_{IH}	High-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage

UART Electrical Validation Solution

Introduction:



Use an oscilloscope to do UART Electrical Validation to ensure that the UART meets the defined specifications. It can be confirmed that the electrical characteristics of the signal to be tested meet the specifications after a long burn-in test. For protocol electrical validation

UART Protocol electrical characteristic detection is usually divided into two types: vertical (voltage) and horizontal (time/phase).

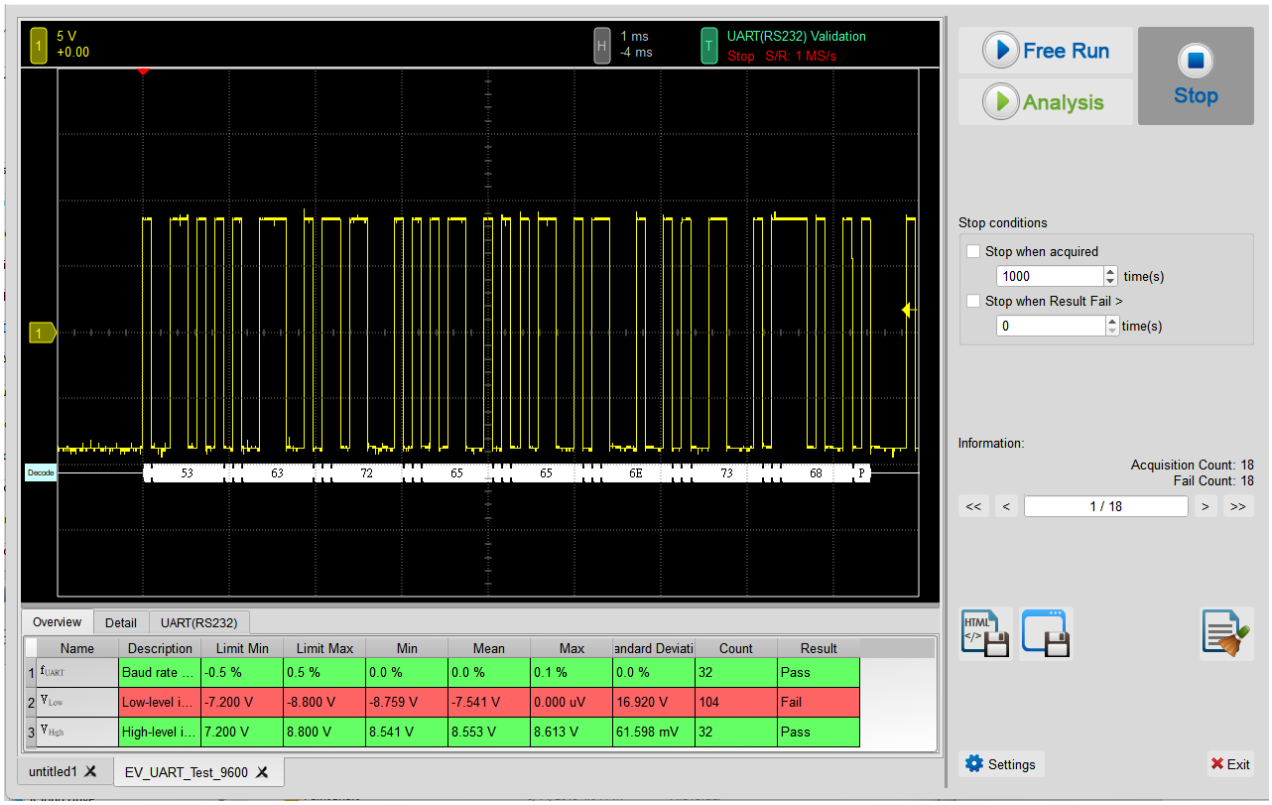
Therefore, when using this function, you must first set the selected protocol and specifications, and then repeat the test to get the electrical characteristics test report. The test items will have different specifications and standards depending on the UART Speed.

The report of common UART validation:

Overview | Detail | UART(RS232)

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f_{UART}	Baud rate ...	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	Pass
2	V_{Low}	Low-level i...	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	Fail
3	V_{High}	High-level i...	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	Pass

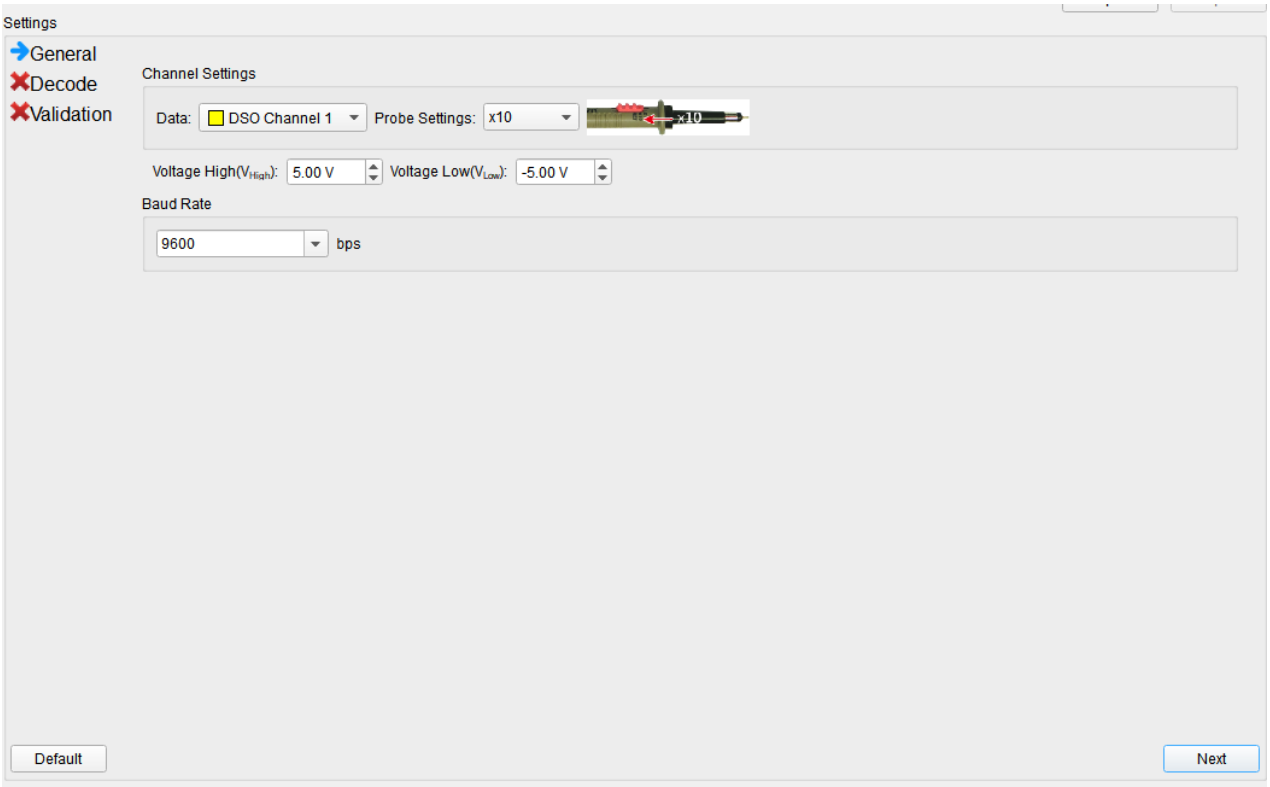
Dedicated page for Electrical Validation:



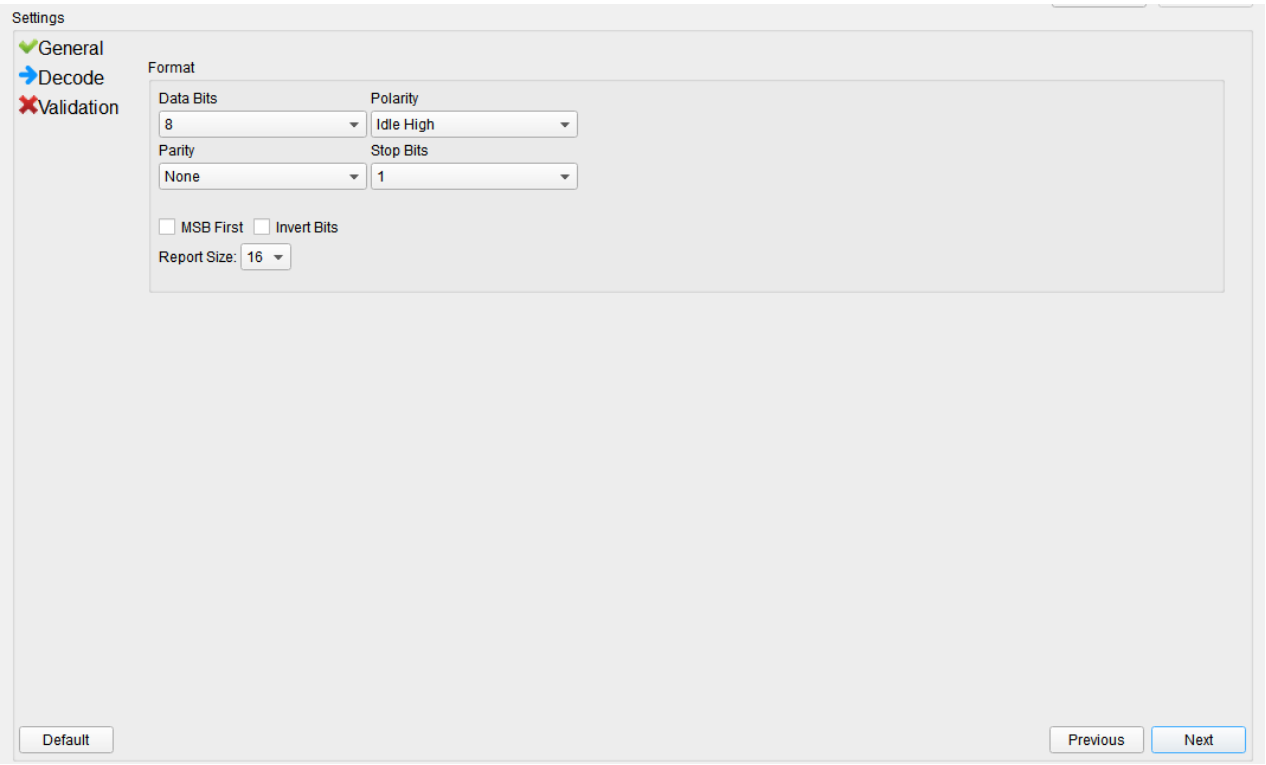
1. Frequency: Clock speed
2. Timing: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
3. Voltage: V_L, V_H, etc.

UART Electrical Validation Settings:

1. General Settings: Channel sources, working voltage and speed

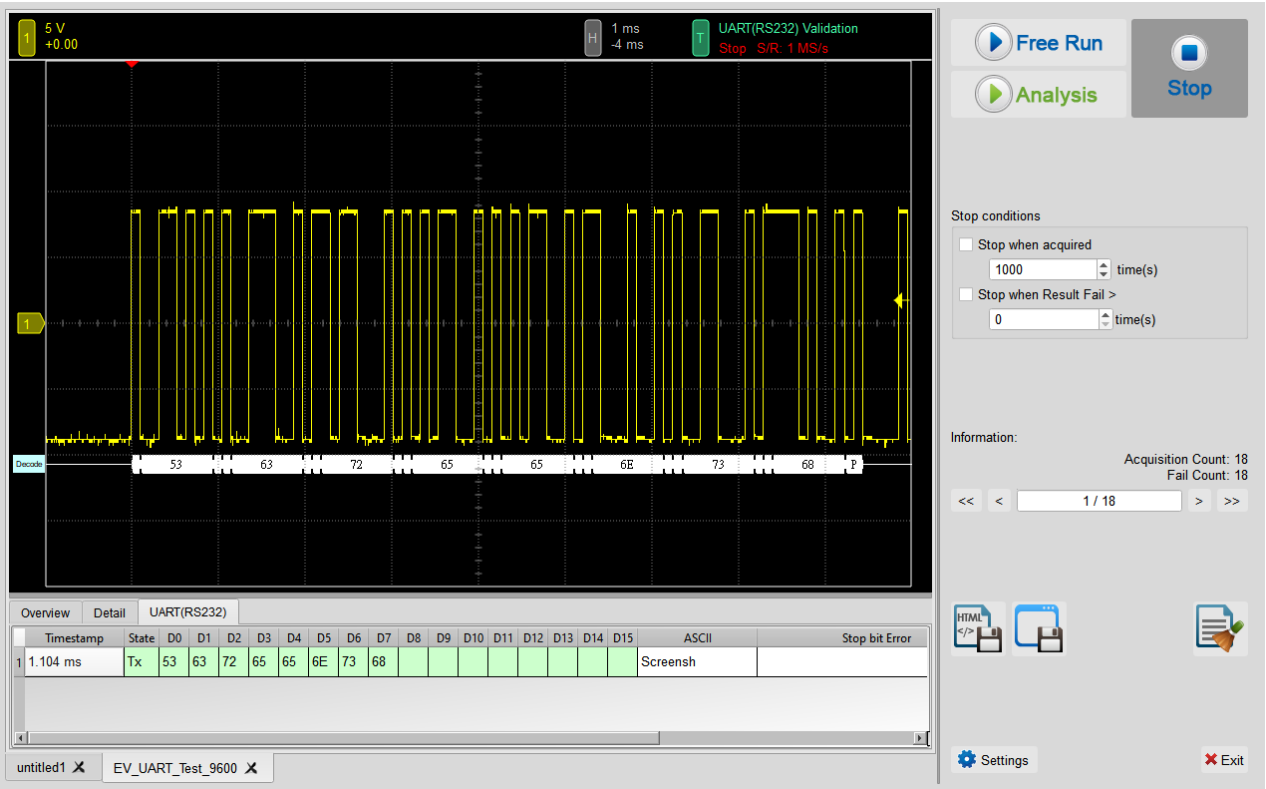


2. Decode Settings: UART decoding settings

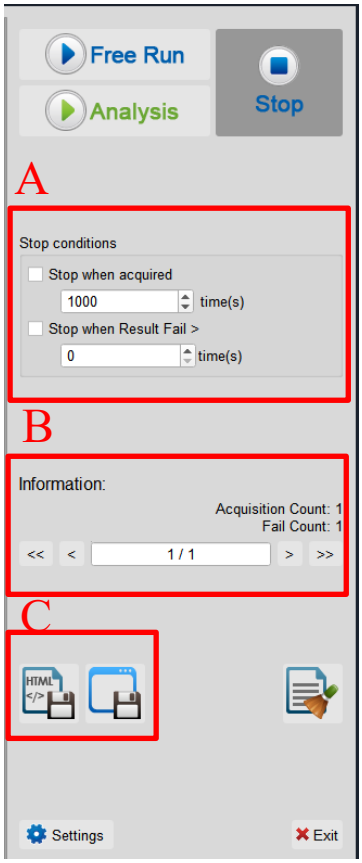


3. Electrical validation settings: Voltage, timing, frequency limitation

4. Software electrical validation interface:



5. Software electrical validation control panel:



D. Stop Conditions:

Stop when acquired X times

Stop when Result Fail > X times

E. Information:

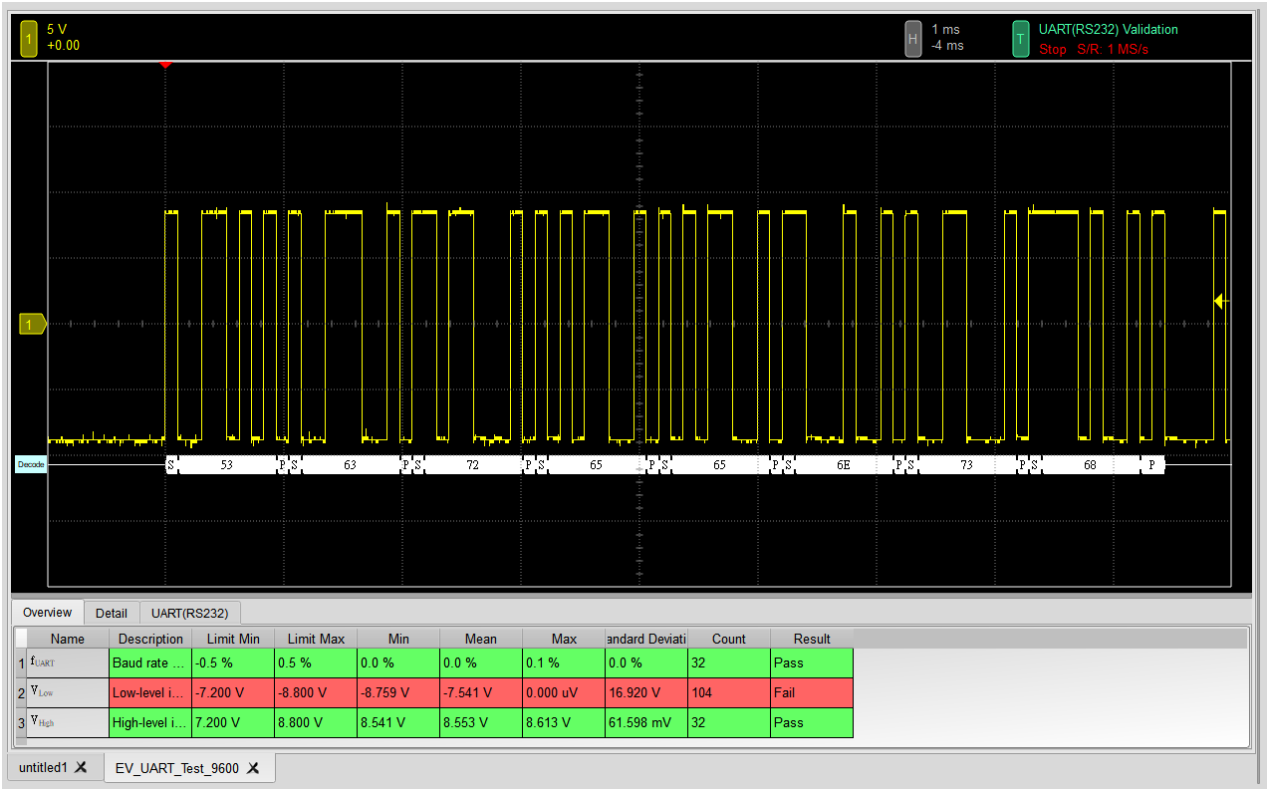
Select waveform

F. Save File:

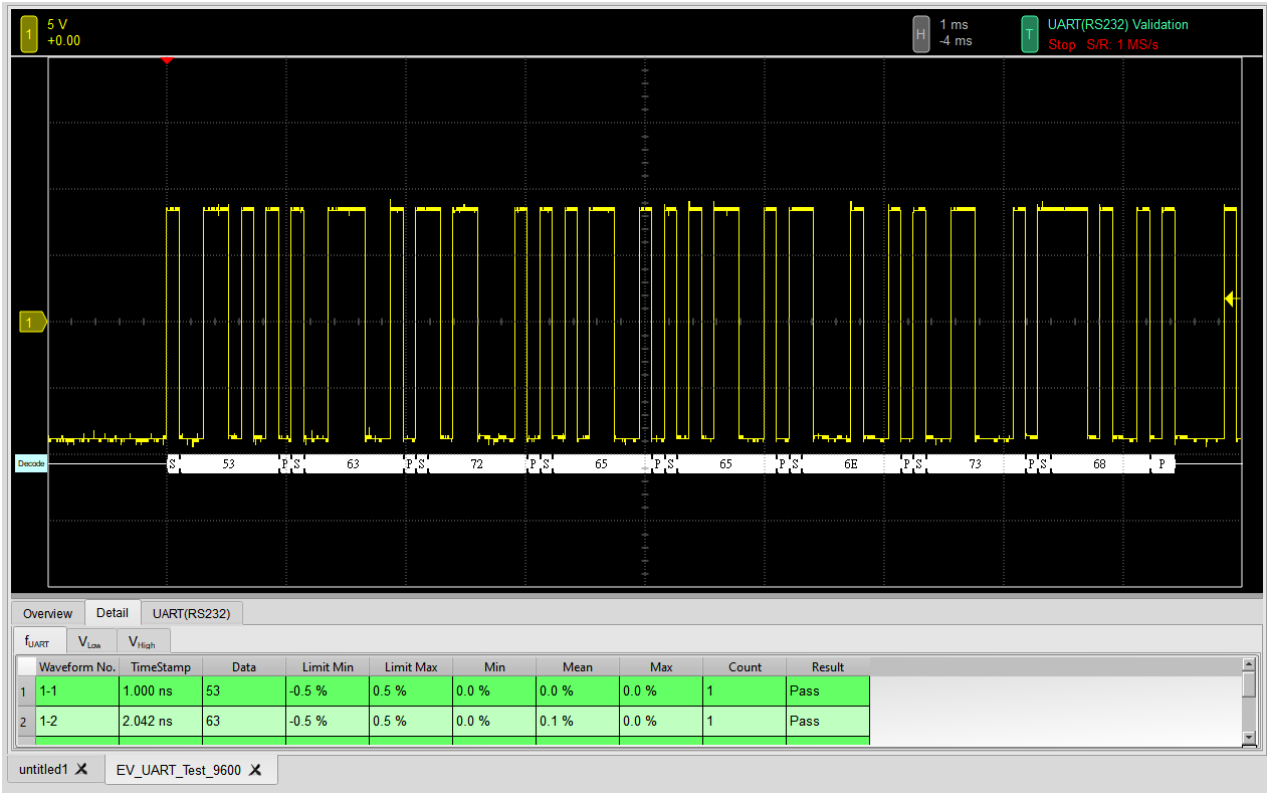
Save as Html

Save as .MOW(Software format)

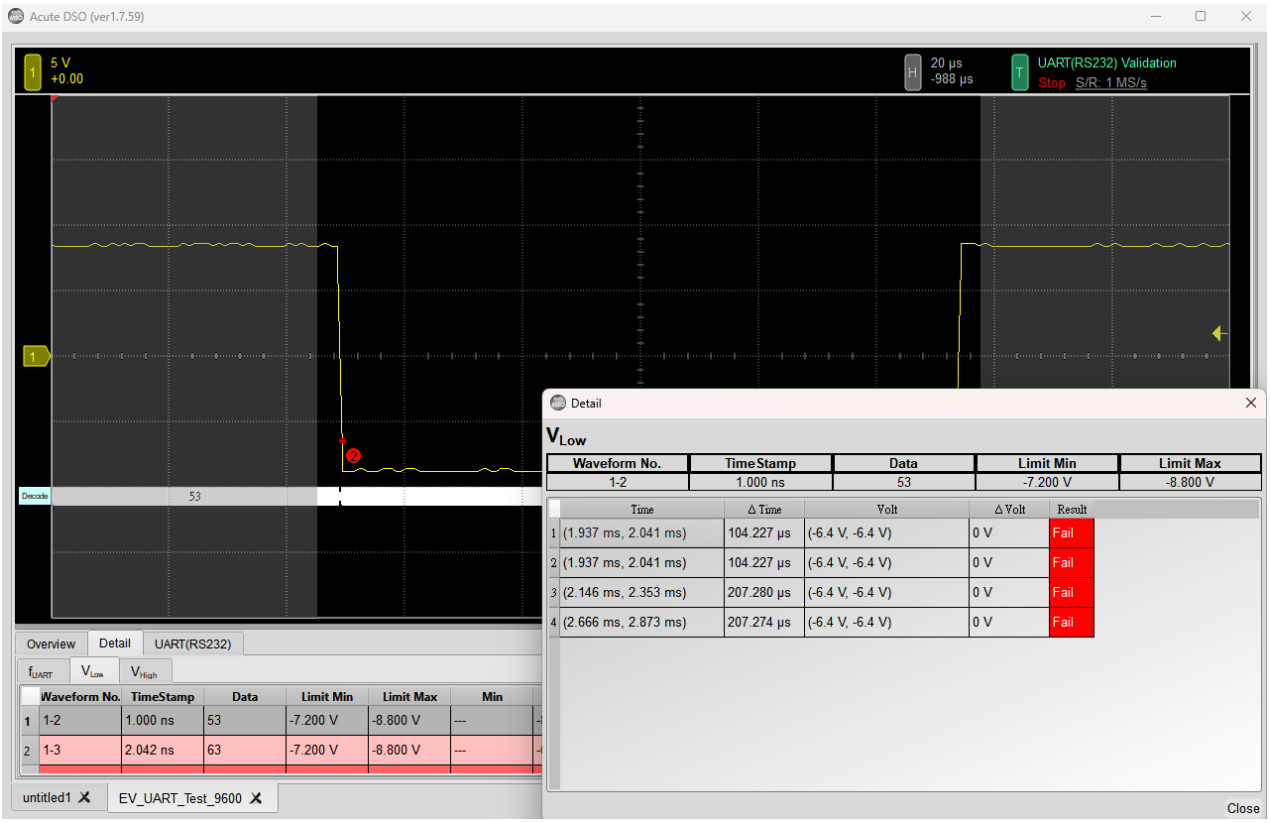
6. Overview Report:



7. Detail Report:



8. Reference Point Dialog & Waveform:



9. Html Report:

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	04-27-2023 15:07:32
S/W Version	1.0.25
Protocol	UART(RS232)

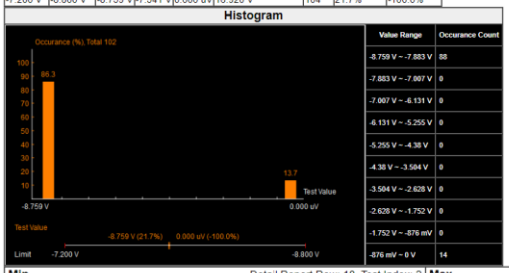
Overview Results:

Total: 3
Pass: 2
Fail: 1

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{UART}	Baud rate for UART	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	-100.0%	-80.0%	Pass
2	V_{Low}	Low-level input voltage	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	21.7%	-100.0%	Fail
3	V_{High}	High-level input voltage	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	18.6%	-2.1%	Pass

V_{Low} - Test Result: Fail
Description: Low-level input voltage

Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	21.7%	-100.0%



MSO/TS3000 series 64-Channel cascading

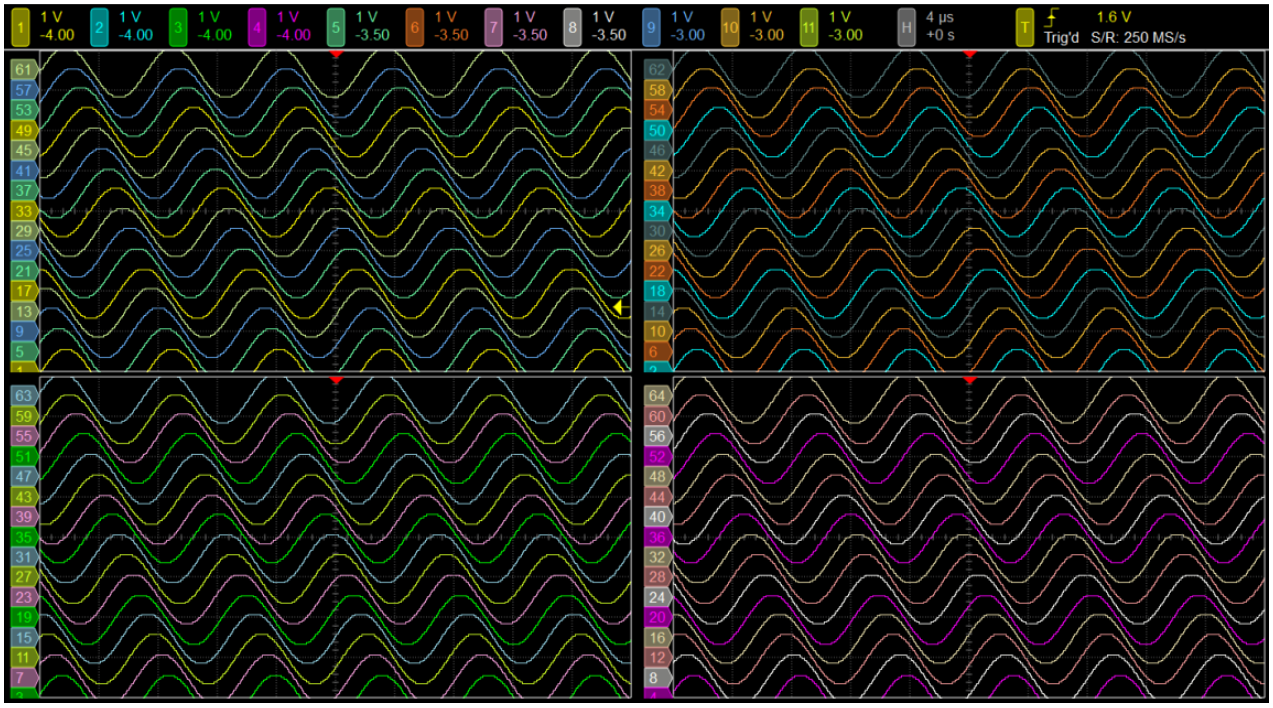
Introduction

One of the key features of the Acute MSO3K/TS3K oscilloscope is its multi-unit stacking capability, allowing for the stacking of up to 16 devices, achieving a maximum measurement capability of 64 channels at 250MS/s or 16 channels at 1GS/s simultaneously. In terms of its chassis design, the MSO3K/TS3K is specifically designed for stacking applications, featuring carefully designed positioning grooves that allow the oscilloscope to be perfectly aligned when stacked. Additionally, the oscilloscope's thermal performance has been thoroughly considered and includes dual-side heat vents to ensure there are no overheating issues during extended operation.

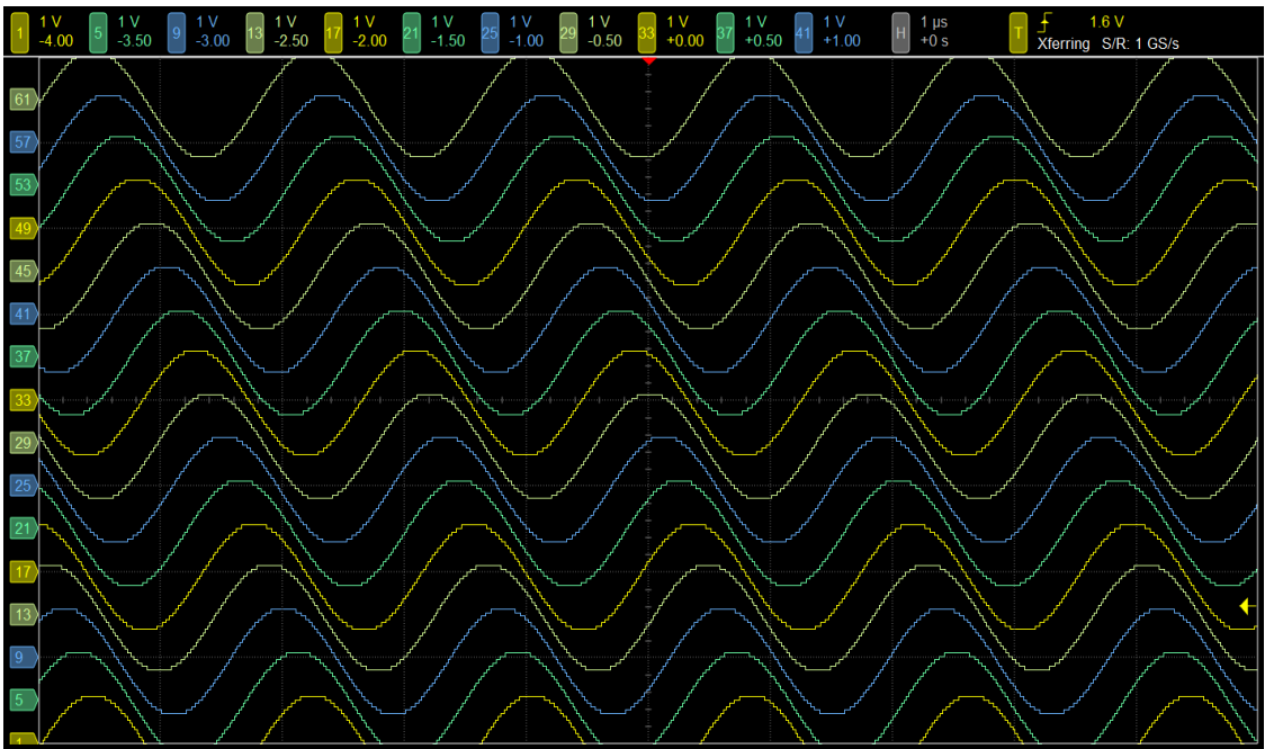
Regarding signal connections, users have the option to directly connect the test signal to the oscilloscope through standard BNC connectors or use passive probes or differential probes for more extensive measurements. Furthermore, Acute also offers a BNC to Probe Tip Adaptor, which can improve common measurement quality issues associated with traditional probes, ensuring users obtain the most accurate measurement results.

Software User Interface

1. 64Channel @ 250MS/s



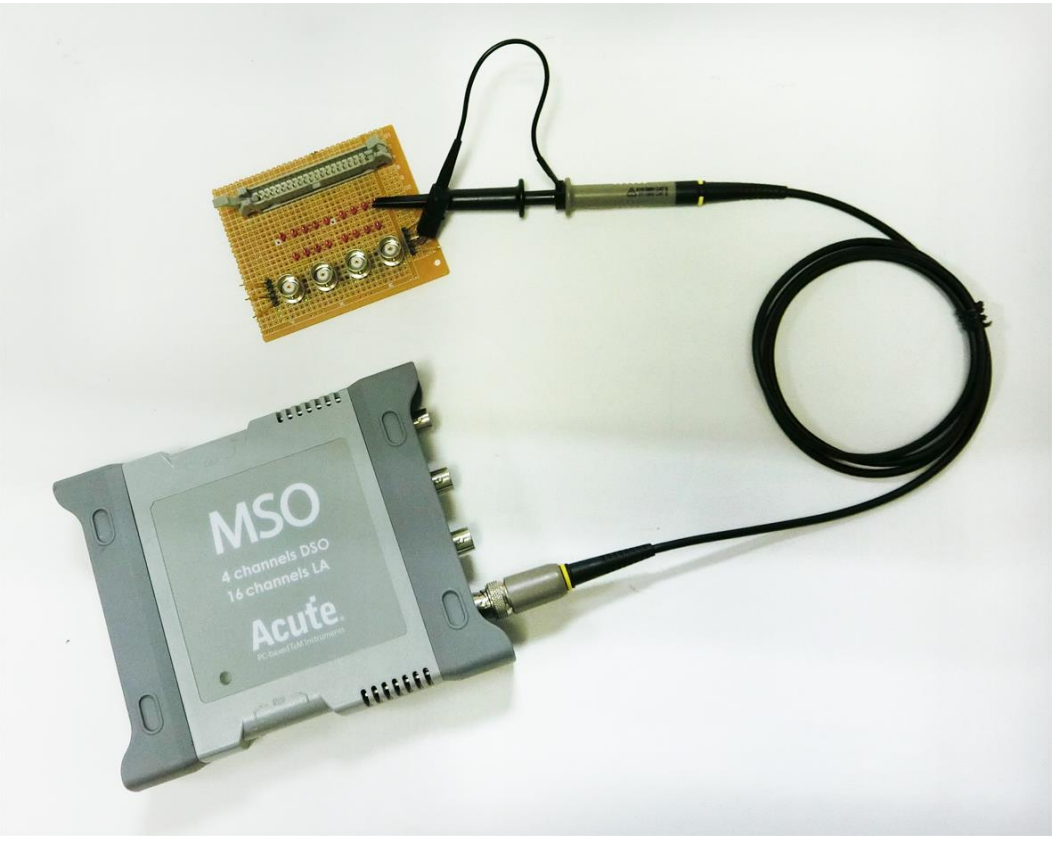
2. 16Channel @ 1GS/s



Connection

1. Connect with BNC to BNC Probe

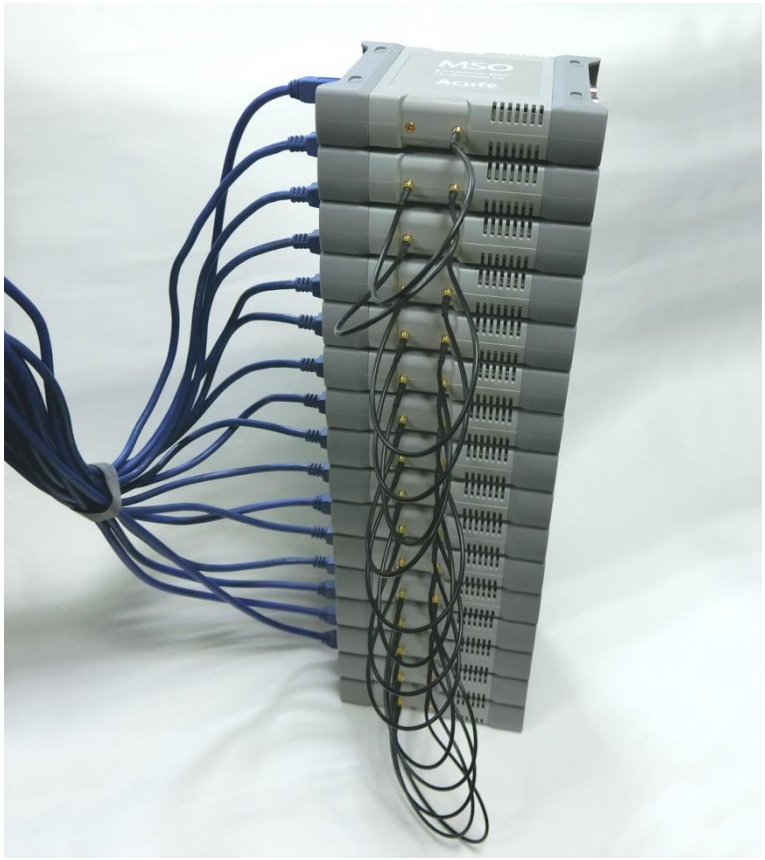
2. Connect with Passive Probe



3. Connect with Passive Probe & BNC to Probe Tip Adaptor

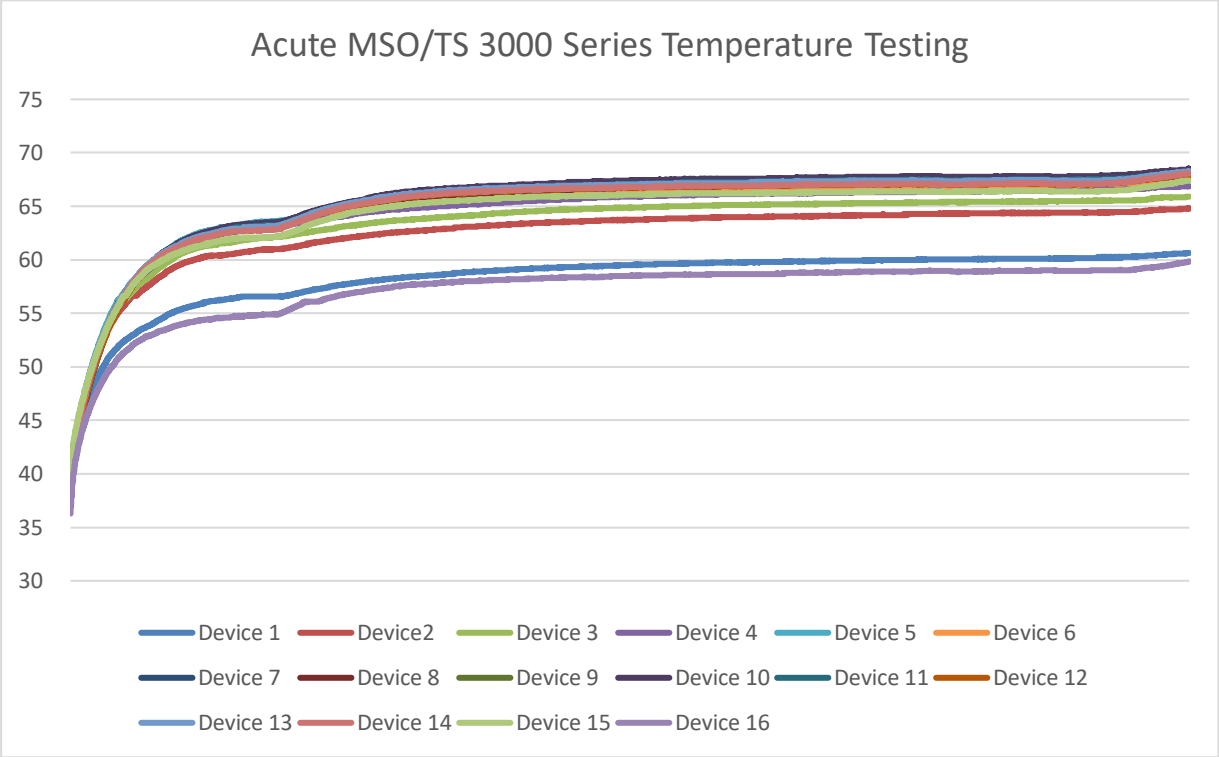
4. Connect with High Voltage Differential Probe

5. Cascading 16 Devices(64 Channels)



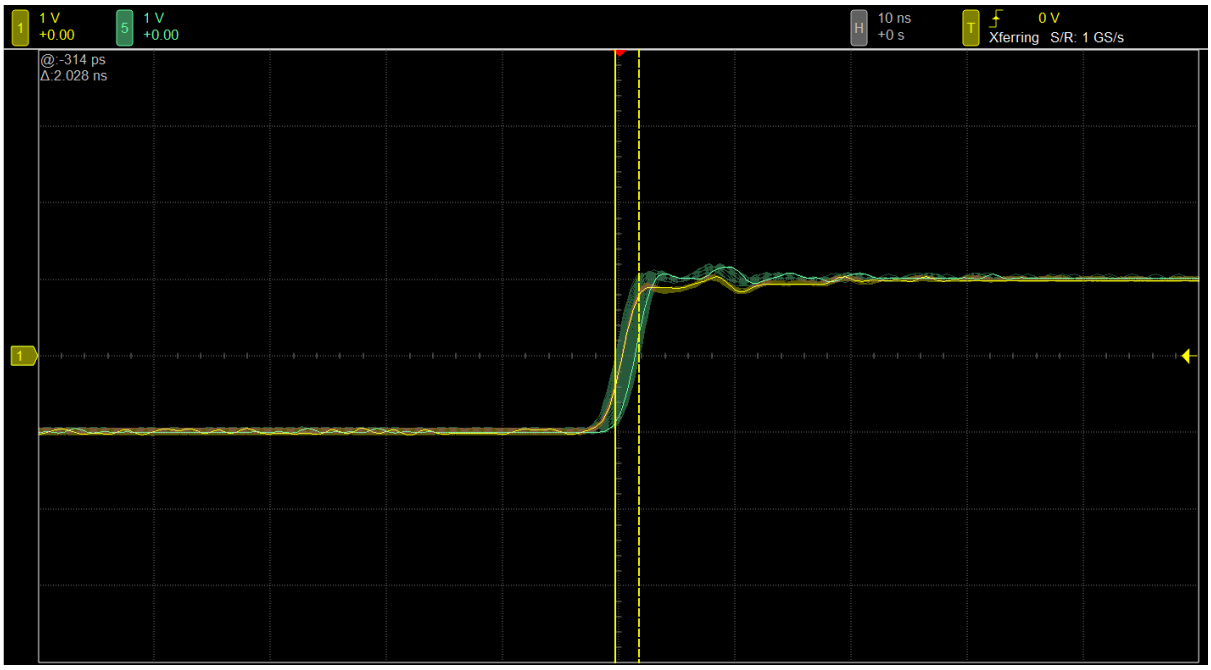
Cautions

1. The MSO3K/TS3K instrument operates on a USB 3.0 interface and consumes approximately 4.5 to 7.7 watts during operation. It is recommended to connect it to a USB 3.0 port at the rear of your computer or use a USB 3.0 hub with its own power supply to ensure optimal measurement quality.
2. The MSO3K/TS3K instrument has undergone internal testing and can operate for extended periods without overheating even in a stacked configuration. However, when using the instrument for an extended period in high-temperature or poorly ventilated environments, it is essential to monitor the operating temperature of the device and consider providing additional cooling measures if needed to prevent overheating (temperature exceeding 80 degrees Celsius) that could impact its operation.



3. When multiple units are stacked, there will be some level of phase difference between them due to differences in sampling rates. For example, at a 1GS/s sampling rate, the phase difference between the master unit and the first slave unit is < ±2ns, and between the master unit and the last slave unit is < ±3ns.

Master & Slave (2nd Device) Phase Delay



Master & Slave (16th Device) Phase Delay