2025

Acute®
PC-based T&M Instruments

电气特性验证说明

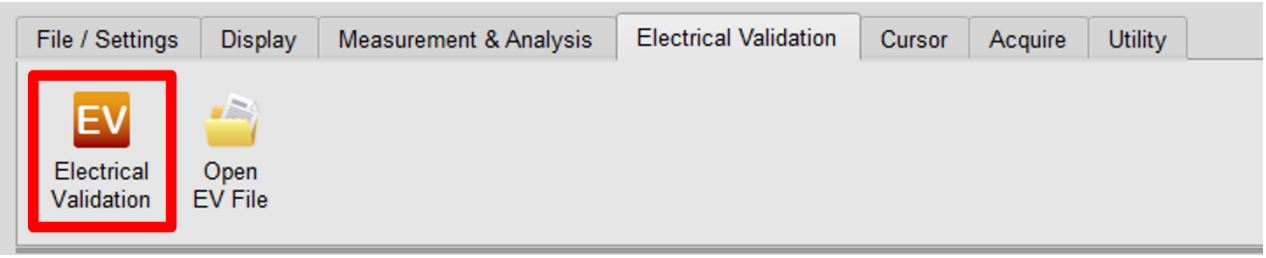
目录

Protocols

其他设置

I2C 电气特性验证解决方案

■ 简介:



使用示波器进行 I2C 电气特性验证，以确保 I2C 符合定义的规范。在经过长时间的持续运行测试后，可以确认所测试的信号电气特性符合规范。

I2C 协议的电气特性检测通常分为两种类型：垂直（电压）与水平（时间/相位）。

因此，在使用此功能时，必须先设置所选的协议与规格，然后重复测试以取得电气特性测试报告。测试项目会依据 I2C 的速度而有所不同。

常见 I2C 规格中的部分电气特性规格：

Table 13. Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I^2C-bus devices[1]

Symbol	Parameter	Conditions	C_b = 100 pF (max)		C_b = 400 pF[2]		Unit
			Min	Max	Min	Max	
f_{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
$t_{SU;STA}$	set-up time for a repeated START condition		160	-	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		160	-	320	-	ns
t_{HIGH}	HIGH period of the SCL clock		60	-	120	-	ns
$t_{SU;DAT}$	data set-up time		10	-	10	-	ns
$t_{HD;DAT}$	data hold time		0[3]	70	0[3]	150	ns
t_{rCL}	rise time of SCLH signal		10	40	20	80	ns
t_{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
t_{fCL}	fall time of SCLH signal		10	40	20	80	ns

I2C 电气特性验证 报告内容：

Overview | Detail | I2C

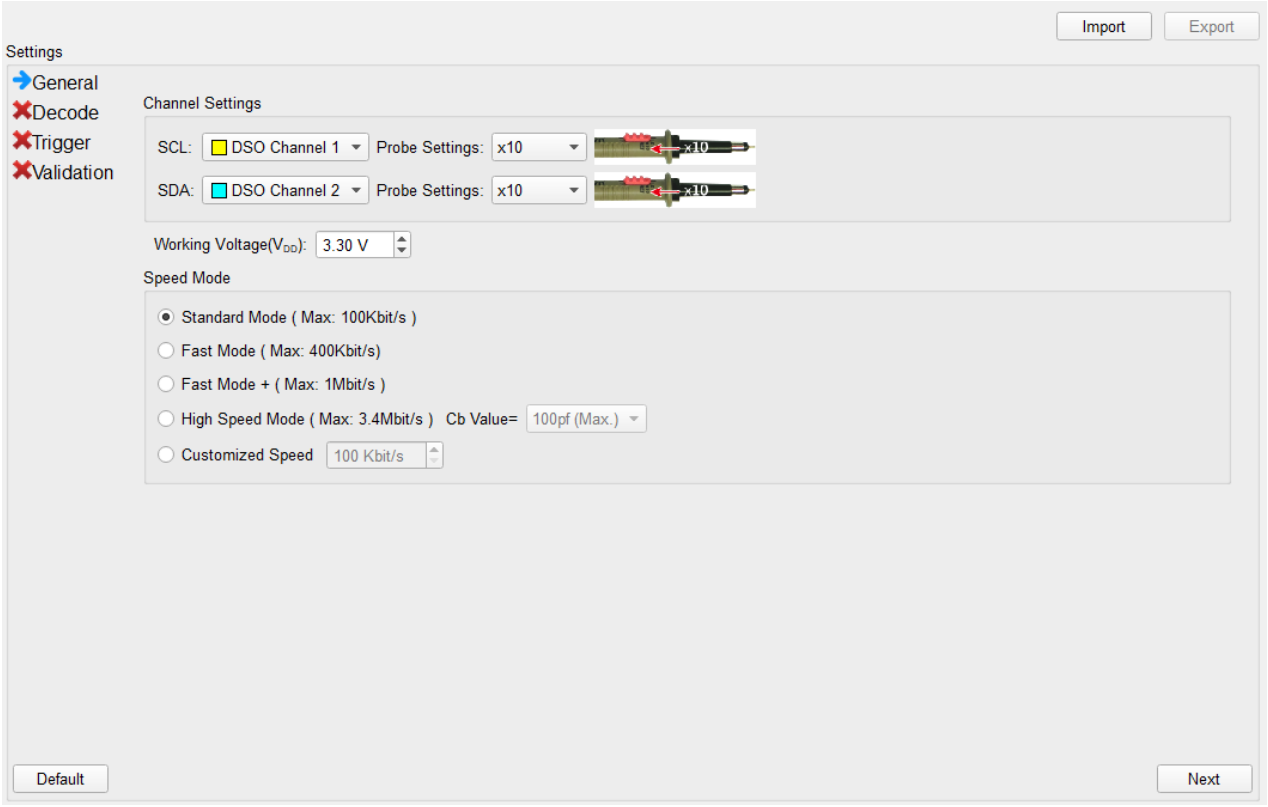
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	f_{SCL}	SCL clock frequencey	0.000 Hz	400.000 KHz	387.596 KHz	387.683 KHz	387.897 KHz	34200	Pass
2	$t_{HD;STA}$	Hold time(repeated) START condition	600.000 ns	—	1.536 us	1.537 us	1.540 us	200	Pass
3	$t_{SU;STA}$	Set-up time for a repeated START condition	600.000 ns	—	2.010 us	2.012 us	2.014 us	100	Pass
4	$t_{HD;DAT}$	Data hold time	—	—	94.000 ns	274.110 ns	1.028 us	17250	Pass
5	$t_{SU;DAT}$	Data Set-up time	100.000 ns	—	472.000 ns	1.066 us	1.444 us	25100	Pass
6	$t_{SU;STO}$	Set-up time for STOP condition	—	—	—	—	—	0	—
7	t_{LOW}	Low Period of the SCL Clock	1.300 us	—	1.538 us	1.542 us	1.544 us	34100	Pass
8	t_{HIGH}	High Period of the SCL Clock	600.000 ns	—	974.000 ns	982.475 ns	3.560 us	41800	Pass
9	t_{rCL}	Rise time of SCL signal	20.000 ns	300.000 ns	45.999 ns	50.304 ns	51.999 ns	41800	Pass
10	t_{fCL}	Fall time of SCL signal	20.000 ns	300.000 ns	10.000 ns	10.528 ns	11.999 ns	41800	Fail
11	t_{rDA}	Rise time of SDA signal	20.000 ns	300.000 ns	37.999 ns	39.210 ns	41.999 ns	9300	Pass
12	t_{fDA}	Fall time of SDA signal	20.000 ns	300.000 ns	4.000 ns	6.714 ns	10.000 ns	9900	Fail
13	t_{BUF}	Bus free time between a STOP and START condition	—	—	—	—	—	0	—
14	$t_{VD;DAT}$	Data valid time	—	900.000 ns	98.000 ns	267.062 ns	1.068 us	15750	Fail
15	$t_{VD;ACK}$	Data valid acknowledge time	—	900.000 ns	98.000 ns	623.009 ns	1.068 us	1500	Fail

电气特性验证_软件画面：

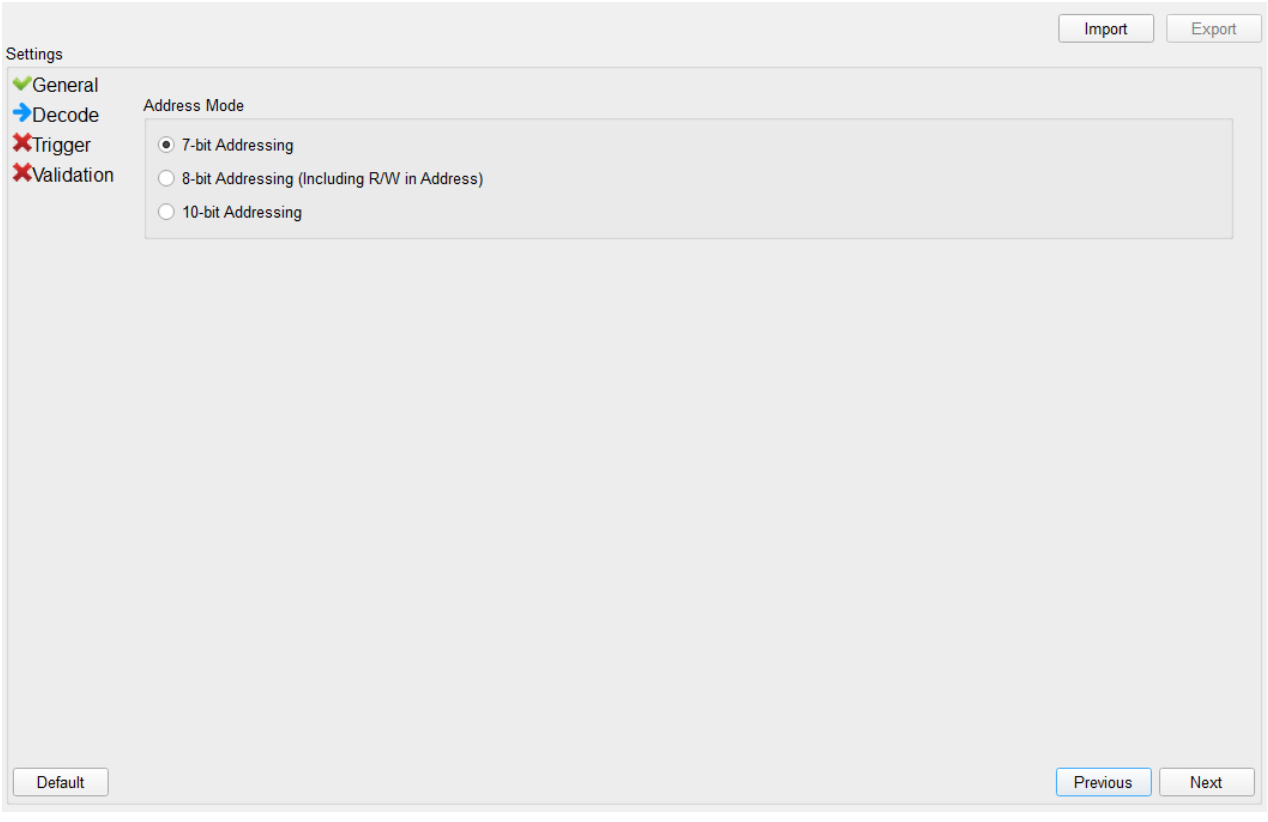
1. 不同的速度模式，包含标准模式（Standard Speed Mode，约 100kHz）/ 快速模式（Fast Mode，约 400kHz）/ 快速模式+（Fast Mode+，约 1MHz）/ 高速模式（HS Mode，约 3.4MHz）
2. 频率：时钟频率（Clock Speed）
3. 时序参数：建立时间（Set-up Time）、保持时间（Hold Time）、上升时间（Rise Time）、下降时间（Fall Time）与时钟拉伸（Clock Stretching）时间限制
4. 电压参数：V_IL（输入低电位）、V_IH（输入高电位）等

I2C 电气特性验证设置

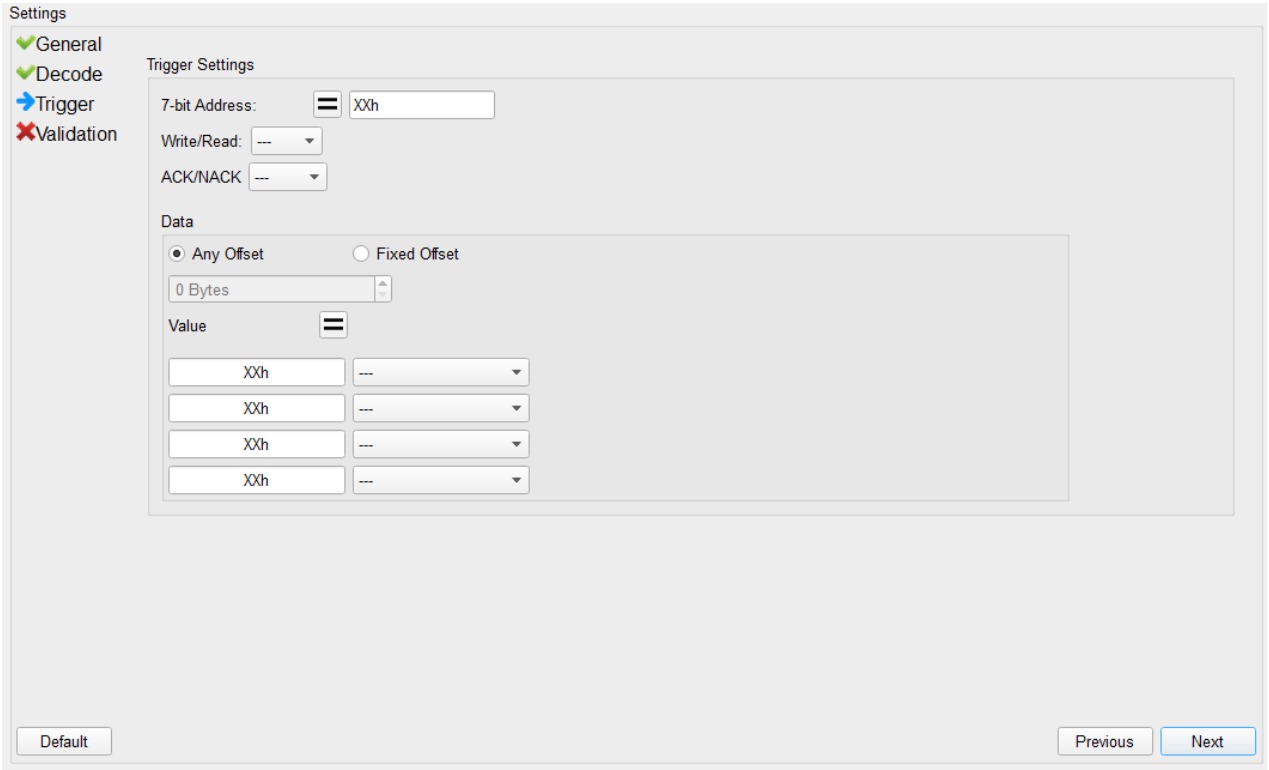
1. 一般设置：通道来源、工作电压与速度



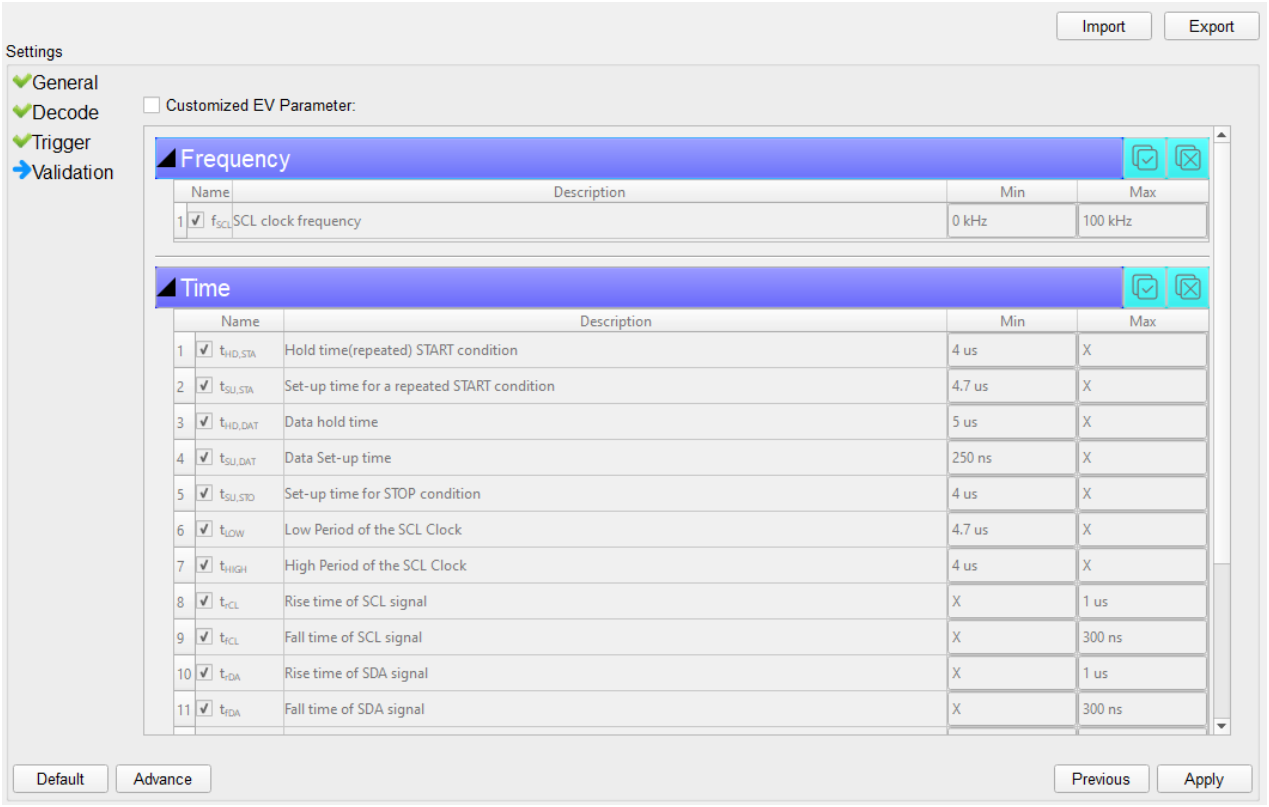
2. 解码设置：I2C 解码设置

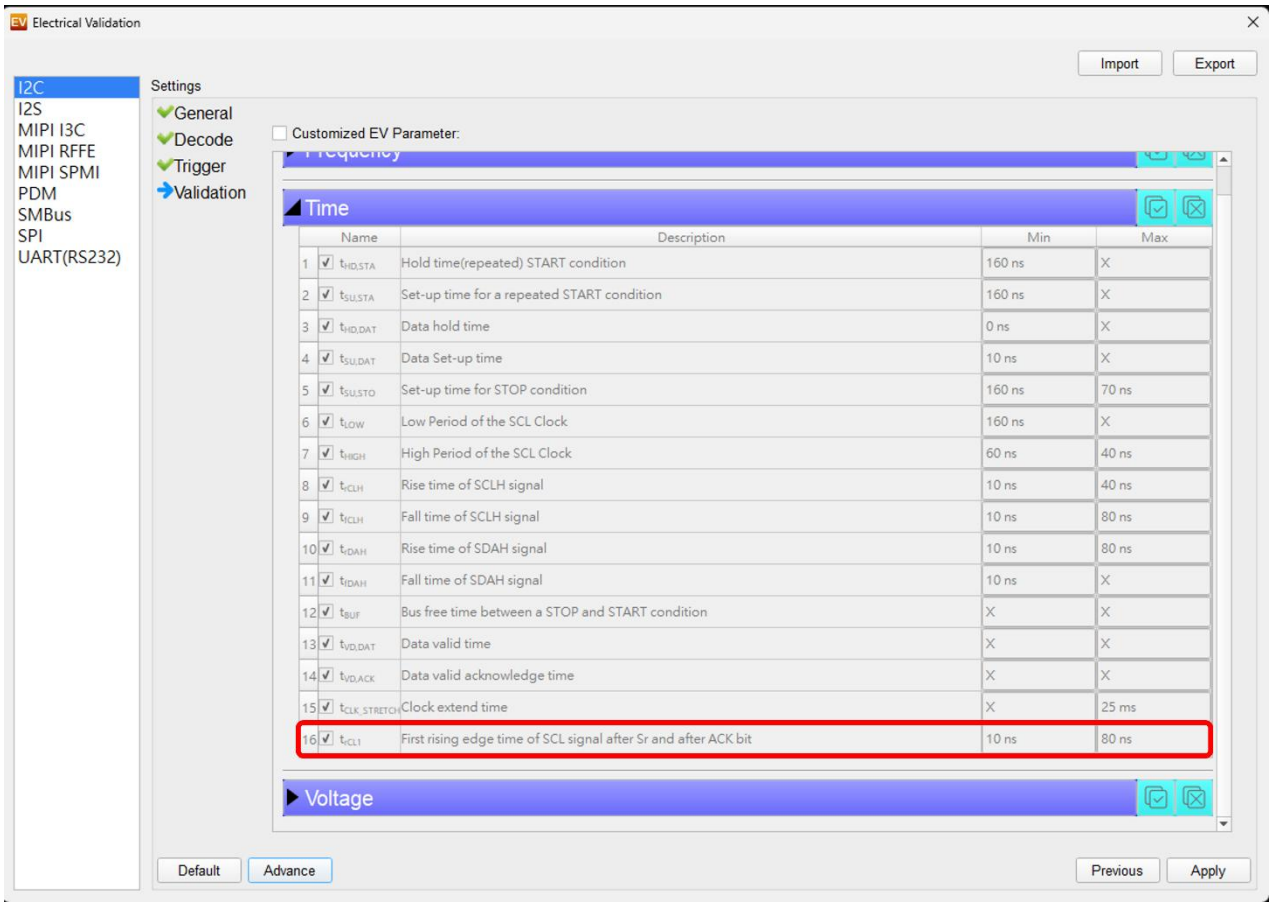


3. 触发设置：I2C Address、Data 触发条件



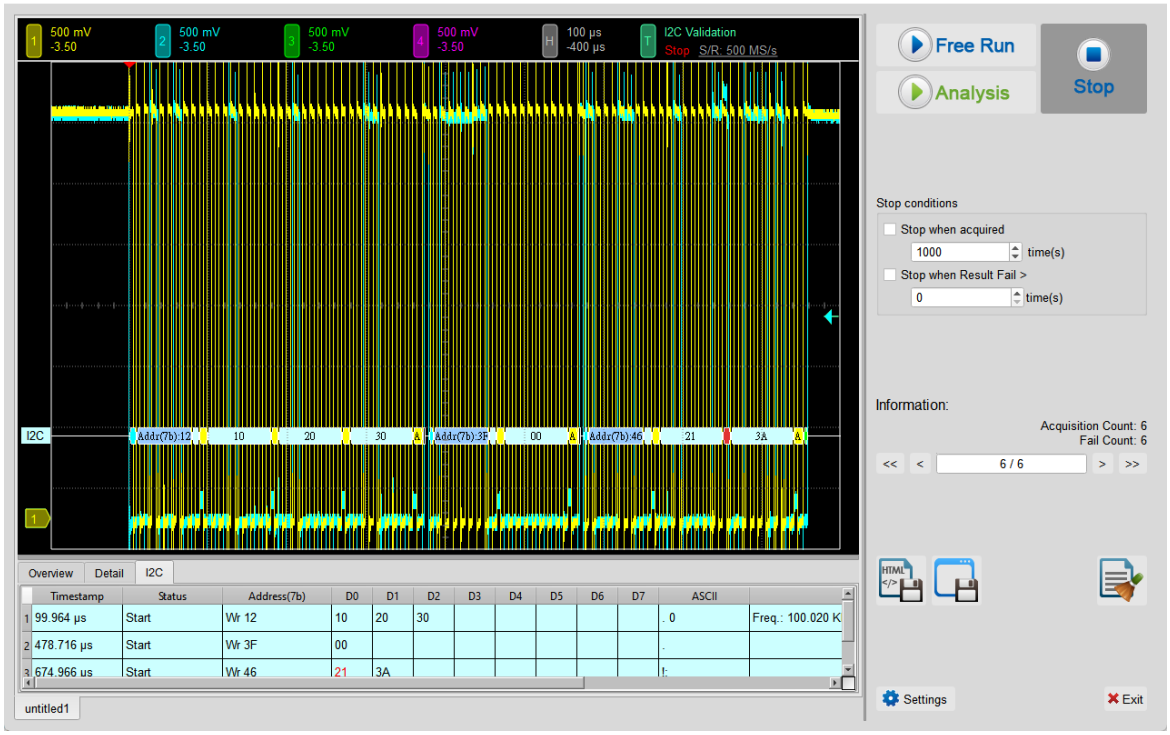
4. 验证参数设置：频率、时序与电压限制条件



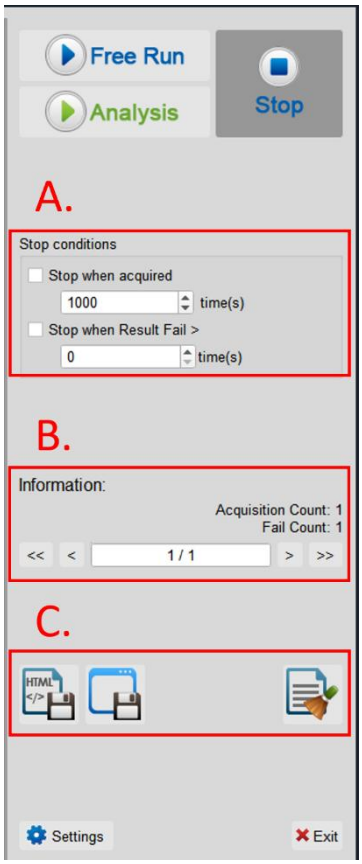


*第 16 项选项仅在 I2C 速度模式设置为**高速模式（High Speed Mode）**时可见*

5. 电气特性验证_软件画面



6. 控制面板



A. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

B. 信息：

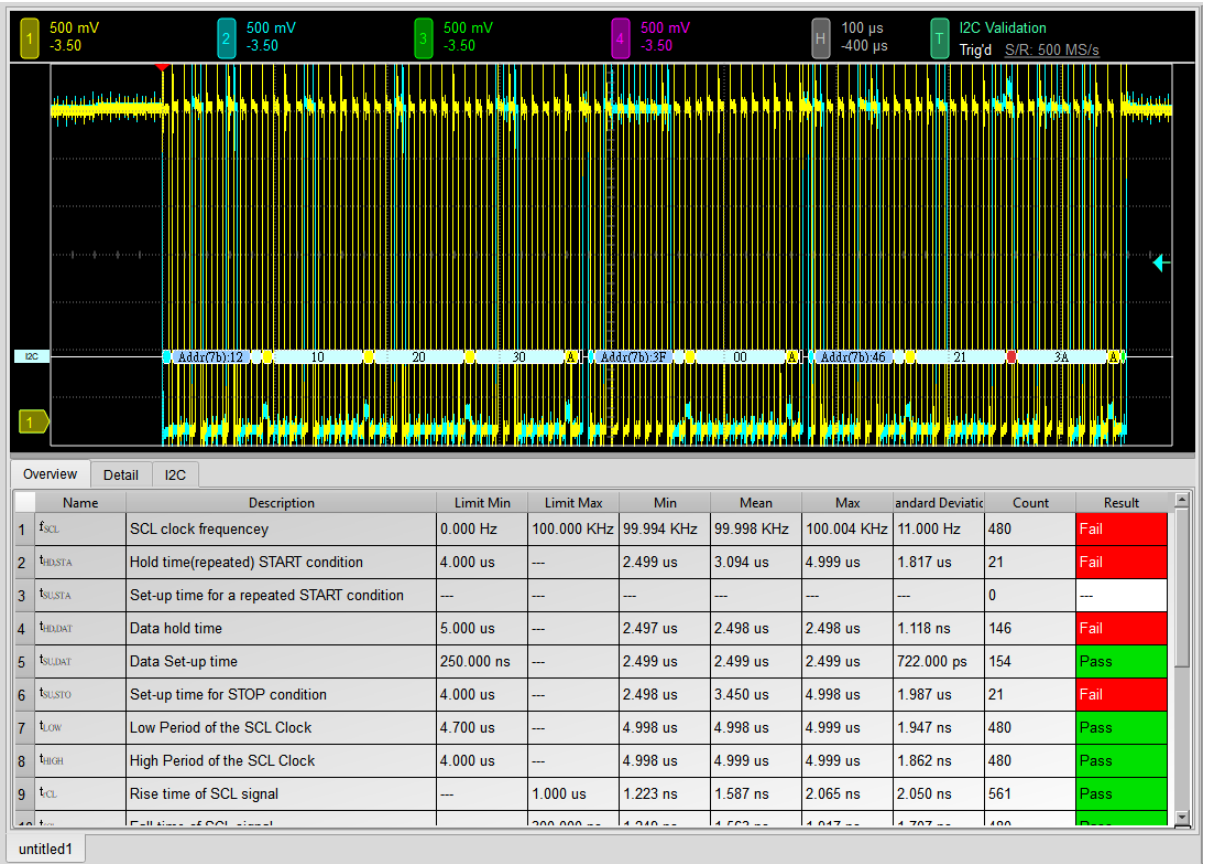
选择查看波形

C. 储存档案：

储存为 HTML 格式

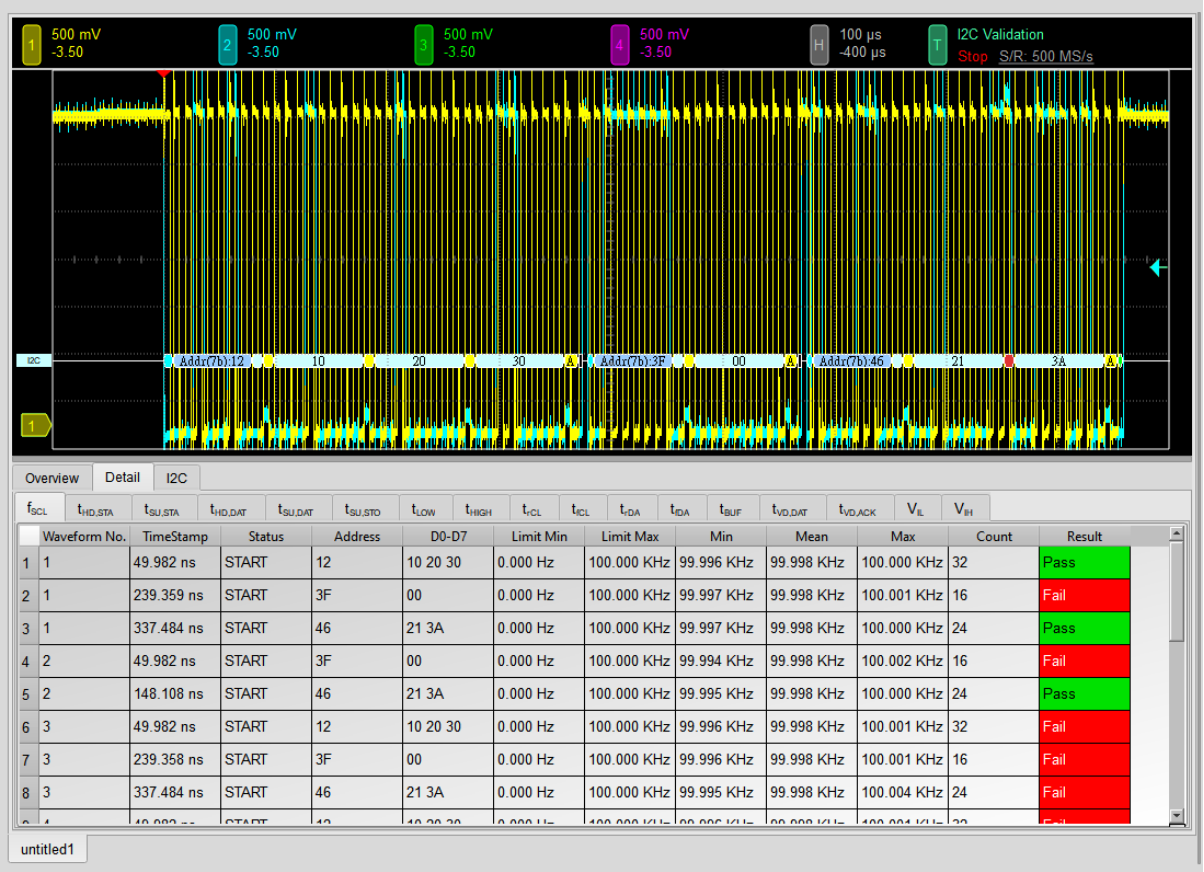
储存为 .MOW（Acute软件专用格式）

7. 概览报告



	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviatic	Count	Result
1	f_{SCL}	SCL clock frequencey	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.004 KHz	11.000 Hz	480	Fail
2	$t_{HD,STA}$	Hold time(repeated) START condition	4.000 us	---	2.499 us	3.094 us	4.999 us	1.817 us	21	Fail
3	$t_{SU,STA}$	Set-up time for a repeated START condition	---	---	---	---	---	---	0	---
4	$t_{HD,DAT}$	Data hold time	5.000 us	---	2.497 us	2.498 us	2.498 us	1.118 ns	146	Fail
5	$t_{SU,DAT}$	Data Set-up time	250.000 ns	---	2.499 us	2.499 us	2.499 us	722.000 ps	154	Pass
6	$t_{SU,STO}$	Set-up time for STOP condition	4.000 us	---	2.498 us	3.450 us	4.998 us	1.987 us	21	Fail
7	t_{LOW}	Low Period of the SCL Clock	4.700 us	---	4.998 us	4.998 us	4.999 us	1.947 ns	480	Pass
8	t_{HIGH}	High Period of the SCL Clock	4.000 us	---	4.998 us	4.999 us	4.999 us	1.862 ns	480	Pass
9	t_{rCL}	Rise time of SCL signal	---	1.000 us	1.223 ns	1.587 ns	2.065 ns	2.050 ns	561	Pass

8. 详细报告



	Waveform No.	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.000 KHz	32	Pass
2	1	239.359 ns	START	3F	00	0.000 Hz	100.000 KHz	99.997 KHz	99.998 KHz	100.001 KHz	16	Fail
3	1	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.997 KHz	99.998 KHz	100.000 KHz	24	Pass
4	2	49.982 ns	START	3F	00	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.002 KHz	16	Fail
5	2	148.108 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.995 KHz	99.998 KHz	100.000 KHz	24	Pass
6	3	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.001 KHz	32	Fail
7	3	239.358 ns	START	3F	00	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.001 KHz	16	Fail
8	3	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.995 KHz	99.998 KHz	100.004 KHz	24	Fail

9. 波形和参考点

	Waveform No.	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max
1	1	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KH
2	1	239.359 ns	START	3F	00	0.000 Hz	100.000 KH
3	1	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KH
4	2	49.982 ns	START	3F	00	0.000 Hz	100.000 KH
5	2	148.108 ns	START	46	21 3A	0.000 Hz	100.000 KH
6	3	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KH
7	3	239.358 ns	START	3F	00	0.000 Hz	100.000 KH
8	3	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KH

Waveform No.	TimeStamp	Status	Address	D0-D7
1	239.359 ns	START	3F	00

	Time	Δ Time	Volt	Δ Volt	Result
1	(489.967 µs, 499.967 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail
2	(499.967 µs, 509.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
3	(509.968 µs, 519.967 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail
4	(519.967 µs, 529.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
5	(529.968 µs, 539.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
6	(539.968 µs, 549.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
7	(549.968 µs, 559.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail
8	(559.968 µs, 569.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
9	(579.968 µs, 589.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass

10. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	24554
Test Date	04-17-2023 14:46:14
S/W Version	1.0.25
Protocol	I2C

```
/*****************************/
DUT INFO

Speed: 400KHz

EEPROM Communication
/*****************************/
```

Overview Results:

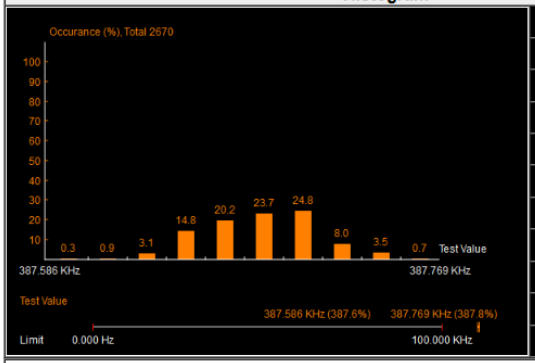
Total: 17
Pass: 9
Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCL}	SCL clock frequency	0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%	✘Fail
2	$t_{HD,STA}$	Hold time(repeated) START condition	4.000 us	---	1.538 us	1.538 us	1.539 us	427.000 ps	20	-61.6%	---	✘Fail
3	$t_{SU,STA}$	Set-up time for a repeated START condition	4.700 us	---	2.013 us	2.014 us	2.015 us	579.000 ps	10	-57.2%	---	✘Fail
4	$t_{HD,DAT}$	Data hold time	5.000 us	---	94.249 ns	247.342 ns	1.026 us	4.244 us	1575	-98.1%	---	✘Fail
5	$t_{SU,DAT}$	Data Set-up time	250.000 ns	---	472.837 ns	1.187 us	1.443 us	5.255 us	1767	18.7%	---	✔Pass
6	$t_{SU,STO}$	Set-up time for STOP condition	---	---	---	---	---	---	0	---	---	---
7	t_{LOW}	Low Period of the SCL Clock	4.700 us	---	1.539 us	1.541 us	1.543 us	9.208 ns	2670	-67.3%	---	✘Fail
8	t_{HIGH}	High Period of the SCL Clock	4.000 us	---	977.699 ns	979.666 ns	984.826 ns	20.914 ns	3040	-75.6%	---	✘Fail
9	t_{rCL}	Rise time of SCL signal	---	1.000 us	45.022 ns	48.118 ns	49.835 ns	14.531 ns	3430	---	0.5%	✔Pass
10	t_{fCL}	Fall time of SCL signal	---	300.000 ns	9.888 ns	10.237 ns	10.583 ns	1.448 ns	3430	---	0.2%	✔Pass
11	t_{rDA}	Rise time of SDA signal	---	1.000 us	37.719 ns	39.529 ns	41.848 ns	5.148 ns	927	---	0.4%	✔Pass
12	t_{fDA}	Fall time of SDA signal	---	300.000 ns	4.616 ns	6.893 ns	9.828 ns	24.035 ns	947	---	1.8%	✔Pass
13	t_{BUF}	Bus free time between a STOP and START condition	---	---	---	---	---	---	0	---	---	---
14	$t_{VD,DAT}$	Data valid time	---	3.450 us	98.898 ns	270.164 ns	1.067 us	4.200 us	1585	---	28.9%	✔Pass
15	$t_{VD,ACK}$	Data valid acknowledge time	---	3.450 us	141.017 ns	730.257 ns	1.067 us	1.344 us	91	---	28.0%	✔Pass
16	V_{IL}	Low-level input voltage	-500.000 mV	990.000 mV	-105.670 mV	27.063 mV	104.081 mV	760.863 mV	4367	26.5%	40.5%	✔Pass
17	V_{IH}	High-level input voltage	2.310 V	3.800 V	3.225 V	3.267 V	3.417 V	1.250 V	4367	61.4%	74.3%	✔Pass

f_{SCL} - Test Result: Fail
Description: SCL clock frequency

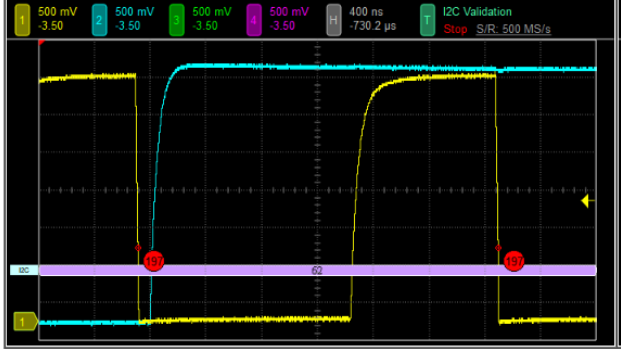
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%

Histogram

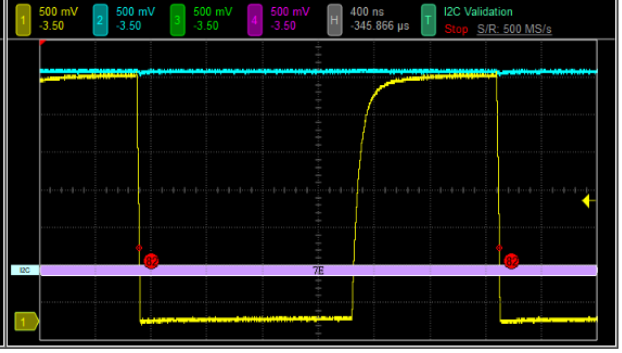


Value Range	Occurance Count
387.586 kHz ~ 387.604 kHz	9
387.604 kHz ~ 387.623 kHz	23
387.623 kHz ~ 387.641 kHz	84
387.641 kHz ~ 387.659 kHz	395
387.659 kHz ~ 387.677 kHz	539
387.677 kHz ~ 387.696 kHz	632
387.696 kHz ~ 387.714 kHz	663
387.714 kHz ~ 387.732 kHz	213
387.732 kHz ~ 387.751 kHz	94
387.751 kHz ~ 387.769 kHz	18

Min Detail Report Row: 12, Test Index: 197

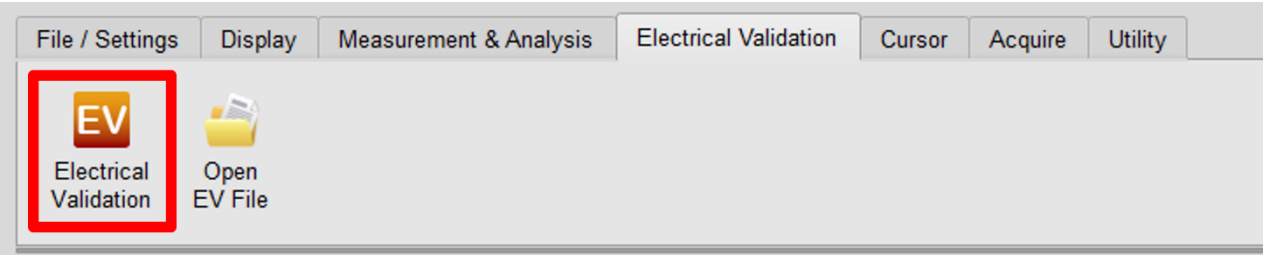


Max Detail Report Row: 10, Test Index: 82



I2S 电气特性验证解决方案

■ 简介：



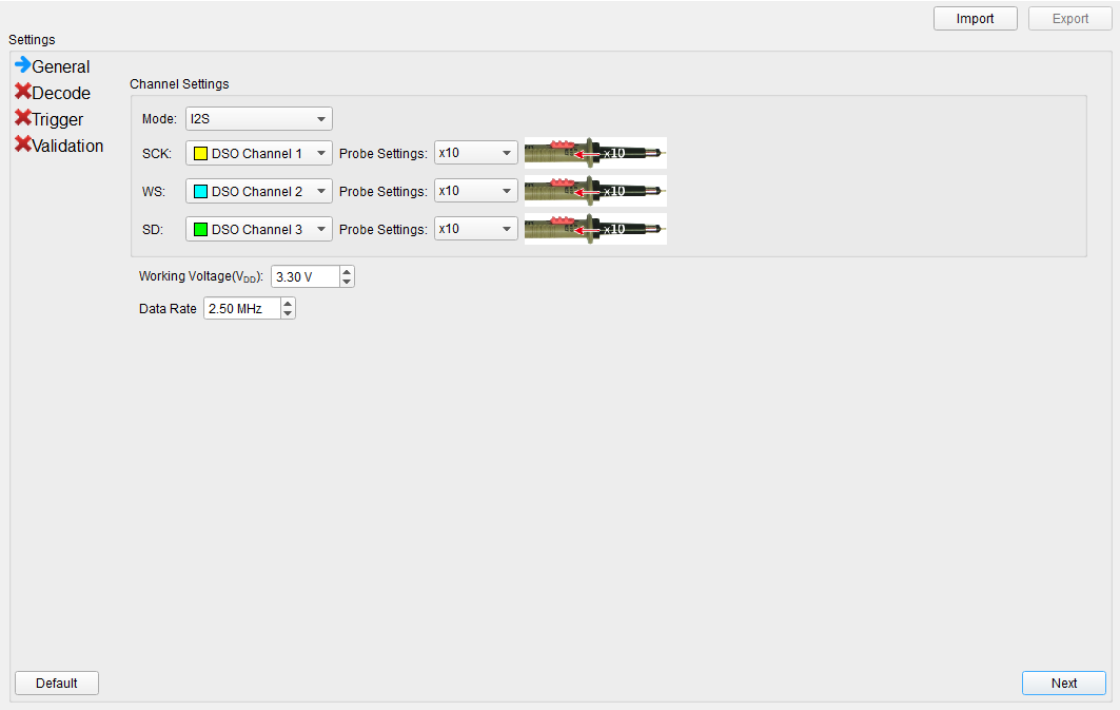
使用示波器执行 I2S 电气特性验证，以确保 I2S 符合既定规格。在经过长时间的持续运行测试后，可以确认所测试的信号电气特性符合规范。

I²S（Inter-IC Sound）是一种标准的串行总线接口，用于连接数字音频装置，例如音频编码器、数字模拟转换器（DAC）与模拟数字转换器（ADC）。它常见于嵌入式系统、音频处理器与高质量音频设备中。

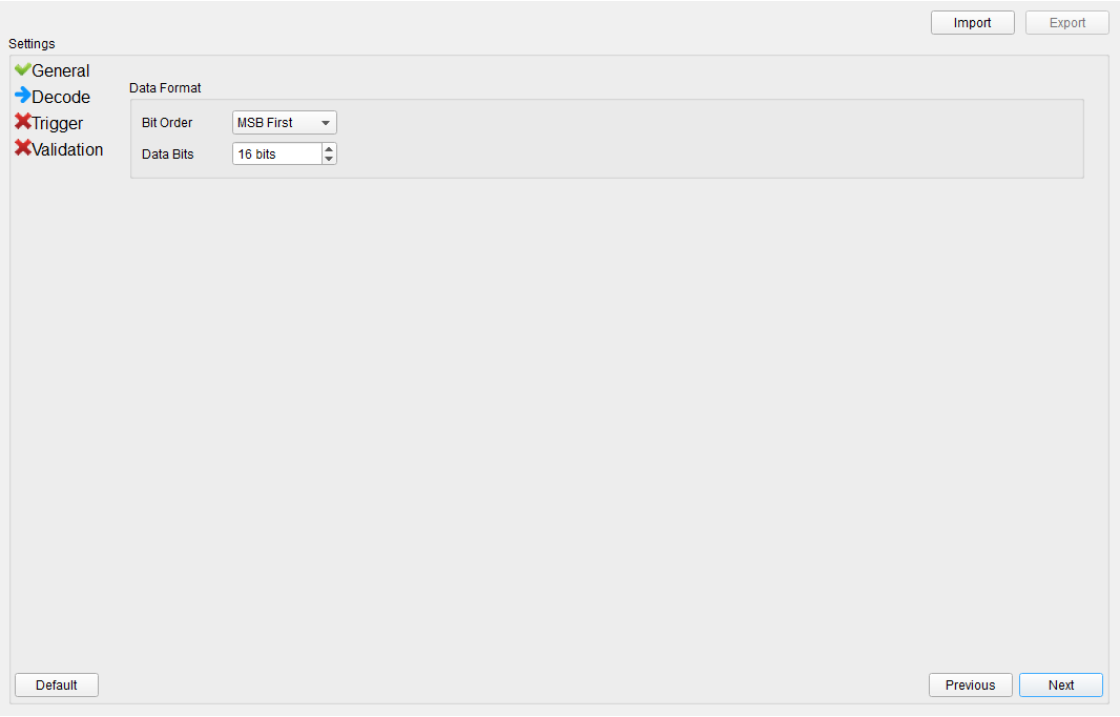
I²S 是一种结构简单但功能强大的接口，可在装置之间以高精度、低延迟地传送数字音频数据。

I2S 电气特性验证设置

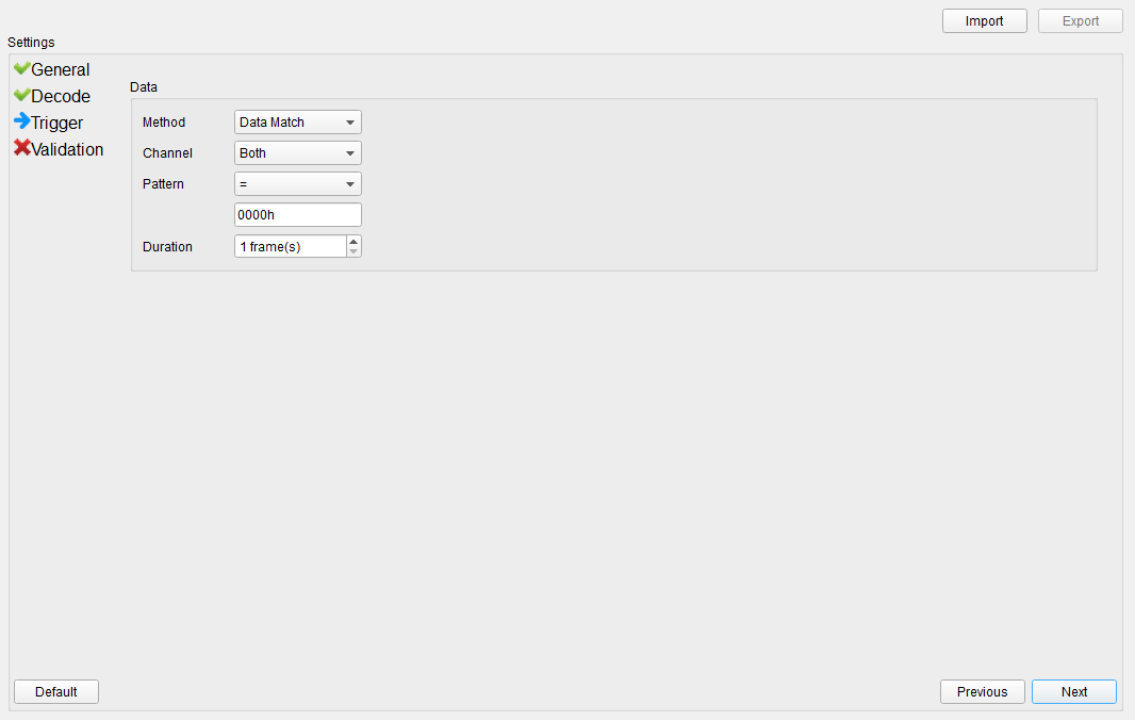
1. **一般设置：**设置总线配置，包括 I2S 模式类型（I2S、Left Justified、PCM、TDM）、通道设置、工作电压与数据速率。



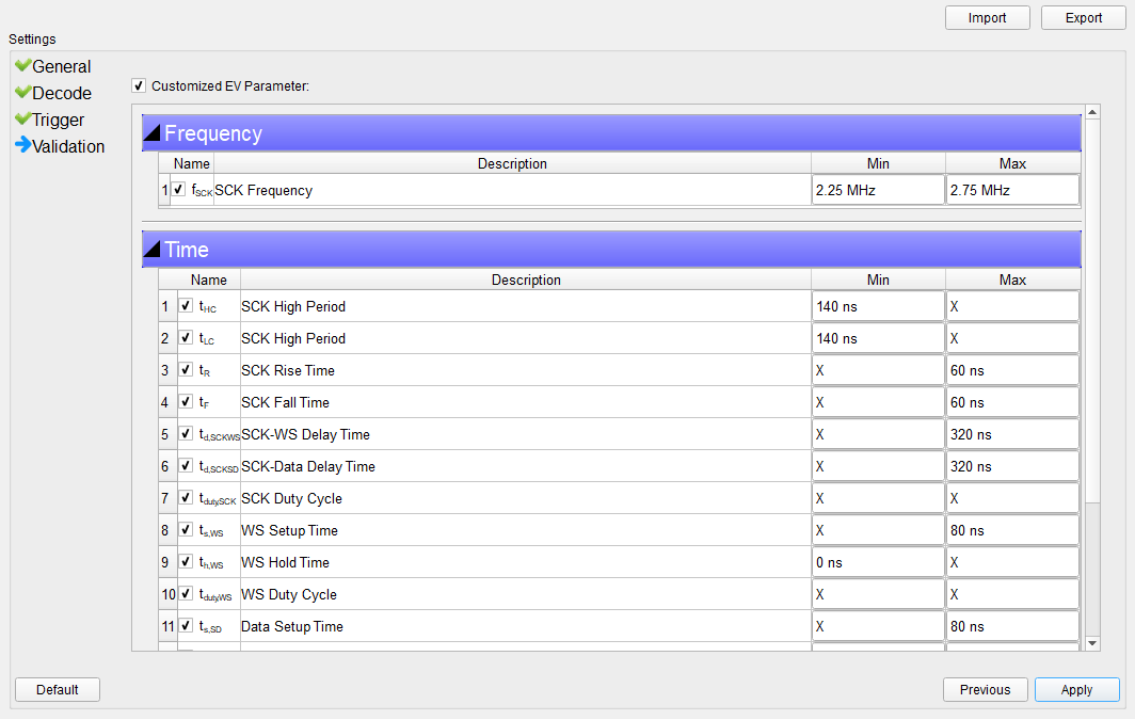
2. **解码设置：**设置 I2S 数据格式。位顺序可选择 MSB First 或 LSB First。数据位数可设置为 1 到 32 位之间。



3. **触发设置：**设置用户需要触发的数据模式。数据格式已在前一页的解码设置中设置完成，其余设置仅与数据模式相关。此处共提供 6 种触发方式：Data Match, Rising, Falling, Glitch, Mute, and Clip。



4. **验证参数设置**



此部分提供三张特性参数表，包含：

- 频率
- 时序参数
- 电压要求

默认值参考自 I2S 规范 Rev3.0。下方列出所有支持的验证参数符号与说明：

- **I2S Frequency Requirements**

Symbol	**Electrical Parameter**
f_{SCK}	SCK Clock Frequency

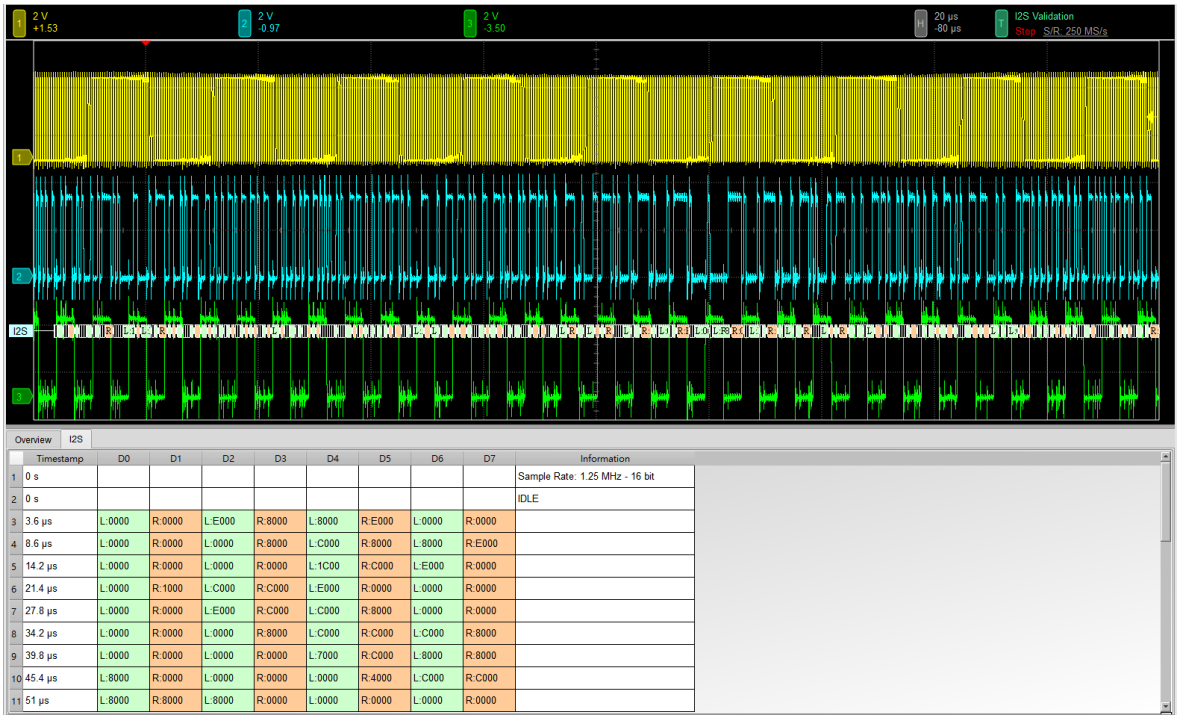
- **I2S Timing Requirements**

Symbol	**Electrical Parameter**
t_{HC}	SCK High Period
t_{LC}	SCK Low Period
t_R	SCK Rise Time
$t\text{-}_F$	SCK Fall Time
$t_{d,SCKWS}$	SCK-WS Delay Time
$t_{duty,SCK}$	SCK Duty Cycle
$t_{s,WS}$	WS Setup Time
$t_{h,WS}$	WS Hold Time
$t_{duty,WS}$	WS Duty Cycle
$t_{s,SD}$	Data Setup Time
$t_{h,SD}$	Data Hold Time

- **I2S Voltage Requirements**

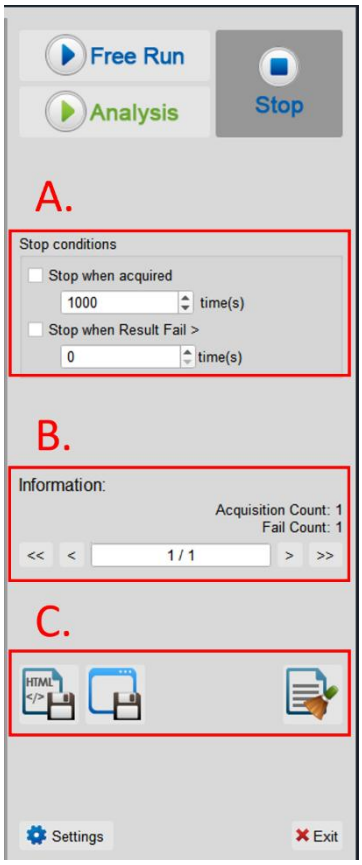
Symbol	**Electrical Parameter**
V_L	Low-Level Voltage
V_H	High-level Voltage

5. 电气特性验证_软件画面



	Timestamp	D0	D1	D2	D3	D4	D5	D6	D7	Information
1	0 s									Sample Rate: 1.25 MHz - 16 bit
2	0 s									IDLE
3	3.6 µs	L:0000	R:0000	L:E000	R:8000	L:8000	R:E000	L:0000	R:0000	
4	8.6 µs	L:0000	R:0000	L:0000	R:8000	L:C000	R:8000	L:8000	R:E000	
5	14.2 µs	L:0000	R:0000	L:0000	R:0000	L:1C00	R:C000	L:E000	R:0000	
6	21.4 µs	L:0000	R:1000	L:C000	R:C000	L:E000	R:0000	L:0000	R:0000	
7	27.8 µs	L:0000	R:0000	L:E000	R:C000	L:C000	R:8000	L:0000	R:0000	
8	34.2 µs	L:0000	R:0000	L:0000	R:8000	L:C000	R:C000	L:C000	R:8000	
9	39.8 µs	L:0000	R:0000	L:0000	R:0000	L:7000	R:C000	L:8000	R:8000	
10	45.4 µs	L:8000	R:0000	L:0000	R:0000	L:0000	R:4000	L:C000	R:C000	
11	51 µs	L:8000	R:8000	L:8000	R:0000	L:0000	R:0000	L:0000	R:0000	

6. 控制面板



A. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

B. 信息：

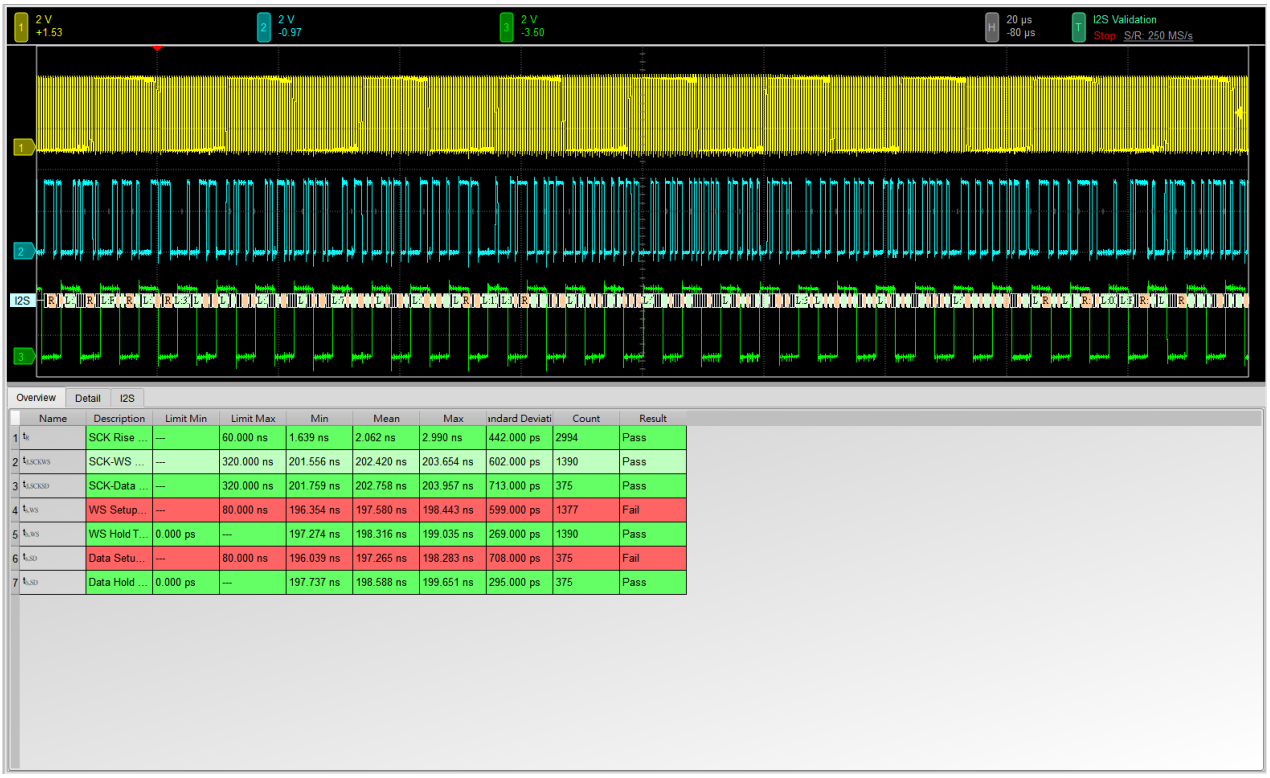
选择查看波形

C. 储存档案：

储存为 HTML 格式

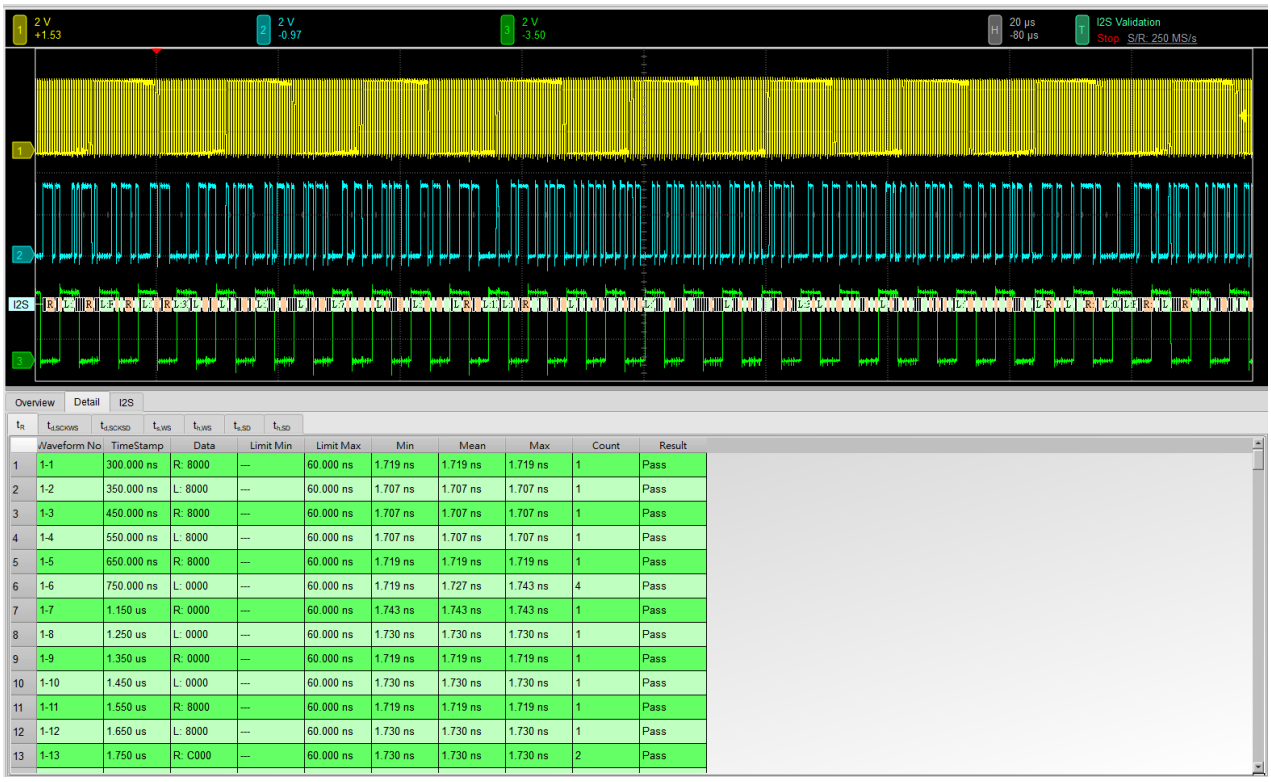
储存为 .MOW（Acute软件专用格式）

7. 概览报告



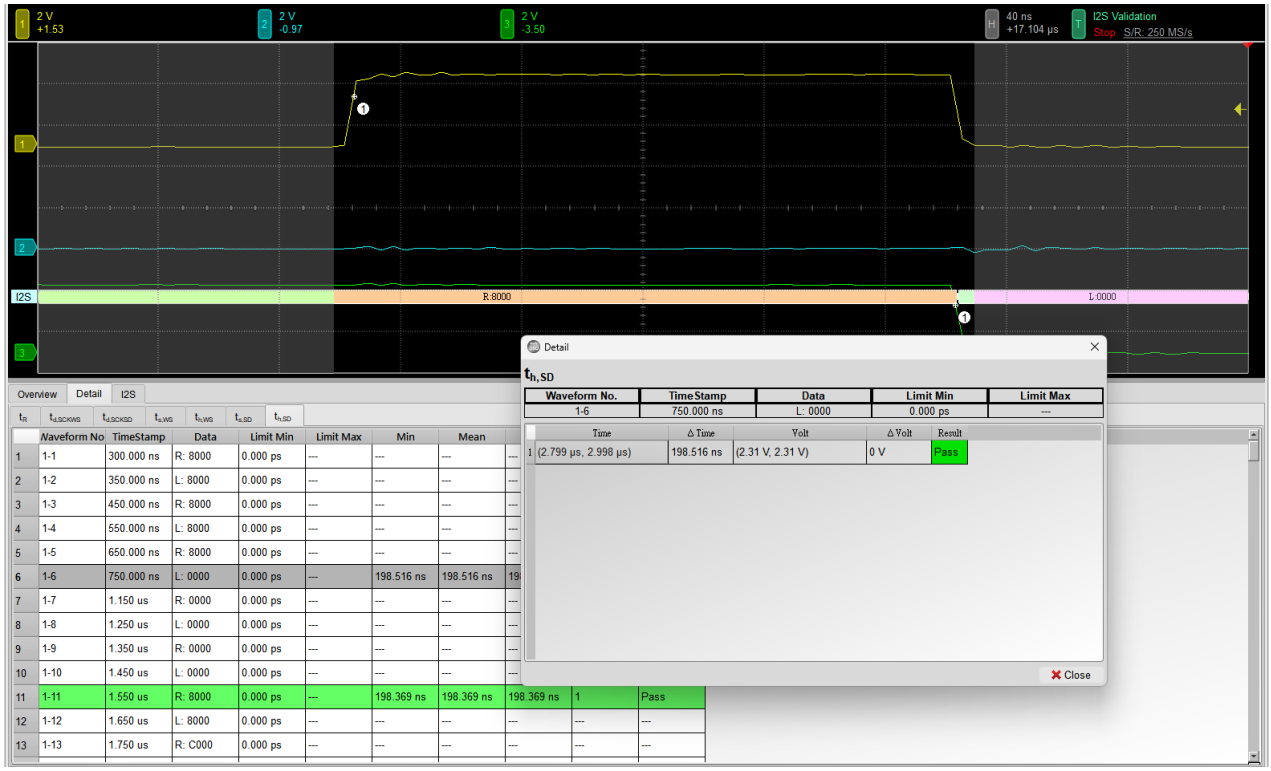
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ındard Deviati	Count	Result
1	t_R	SCK Rise ...	---	60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994	Pass
2	t_{LSCKWS}	SCK-WS ...	---	320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390	Pass
3	t_{LSCKSD}	SCK-Data ...	---	320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375	Pass
4	t_{LWS}	WS Setup...	---	80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377	Fail
5	t_{LWS}	WS Hold T...	0.000 ps	---	197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390	Pass
6	t_{LSD}	Data Setu...	---	80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375	Fail
7	t_{LSD}	Data Hold ...	0.000 ps	---	197.737 ns	198.588 ns	199.651 ns	295.000 ps	375	Pass

8. 详细报告



	Waveform No	TimeStamp	Data	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	300.000 ns	R: 8000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
2	1-2	350.000 ns	L: 8000	---	60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass
3	1-3	450.000 ns	R: 8000	---	60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass
4	1-4	550.000 ns	L: 8000	---	60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass
5	1-5	650.000 ns	R: 8000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
6	1-6	750.000 ns	L: 0000	---	60.000 ns	1.719 ns	1.727 ns	1.743 ns	4	Pass
7	1-7	1.150 us	R: 0000	---	60.000 ns	1.743 ns	1.743 ns	1.743 ns	1	Pass
8	1-8	1.250 us	L: 0000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass
9	1-9	1.350 us	R: 0000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
10	1-10	1.450 us	L: 0000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass
11	1-11	1.550 us	R: 8000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
12	1-12	1.650 us	L: 8000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass
13	1-13	1.750 us	R: C000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	2	Pass

9. 波形和参考点



10. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 13:34:37
S/W Version	1.8.62
Protocol	I2S

Overview Results:

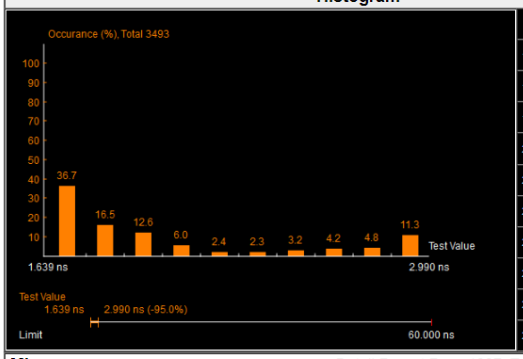
Total: 7
Pass: 5
Fail: 2

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	t_R	SCK Rise Time	---	60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994	---	-95.0%	Pass
2	$t_{d,SCKWS}$	SCK-WS Delay Time	---	320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390	---	-36.4%	Pass
3	$t_{d,SCKSD}$	SCK-Data Delay Time	---	320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375	---	-36.3%	Pass
4	$t_{s,WS}$	WS Setup Time	---	80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377	---	148.1%	Fail
5	$t_{h,WS}$	WS Hold Time	0.000 ps	---	197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390	---	---	Pass
6	$t_{s,SD}$	Data Setup Time	---	80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375	---	147.9%	Fail
7	$t_{h,SD}$	Data Hold Time	0.000 ps	---	197.737 ns	198.588 ns	199.651 ns	295.000 ps	375	---	---	Pass

t_R - Test Result: Pass
Description: SCK Rise Time

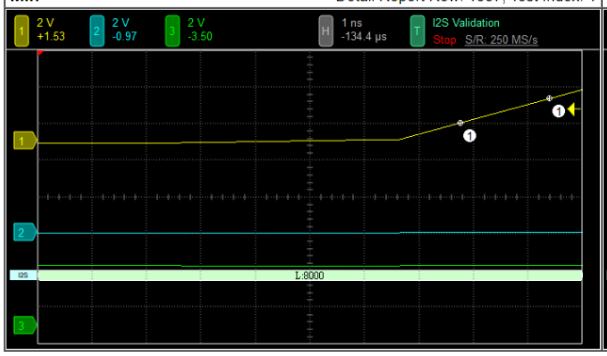
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
---	60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994	---	-95.0%

Histogram

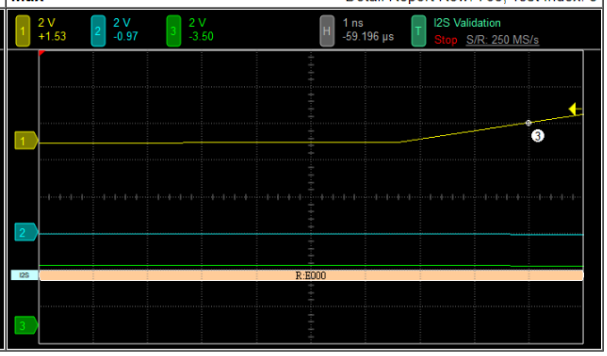


Value Range	Occurance Count
1.639 ns ~ 1.774 ns	1283
1.774 ns ~ 1.909 ns	578
1.909 ns ~ 2.044 ns	439
2.044 ns ~ 2.179 ns	210
2.179 ns ~ 2.314 ns	84
2.314 ns ~ 2.450 ns	80
2.450 ns ~ 2.585 ns	112
2.585 ns ~ 2.720 ns	147
2.720 ns ~ 2.855 ns	167
2.855 ns ~ 2.990 ns	393

Min Detail Report Row: 1337, Test Index: 1

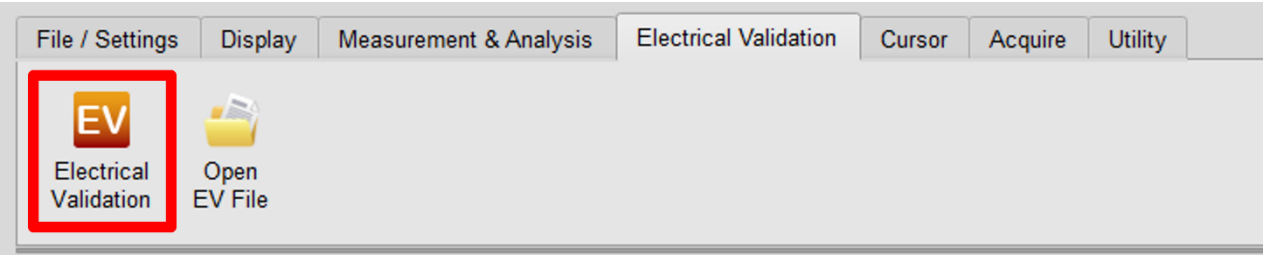


Max Detail Report Row: 765, Test Index: 3



MIPI I3C 电气特性验证解决方案

■ 简介：

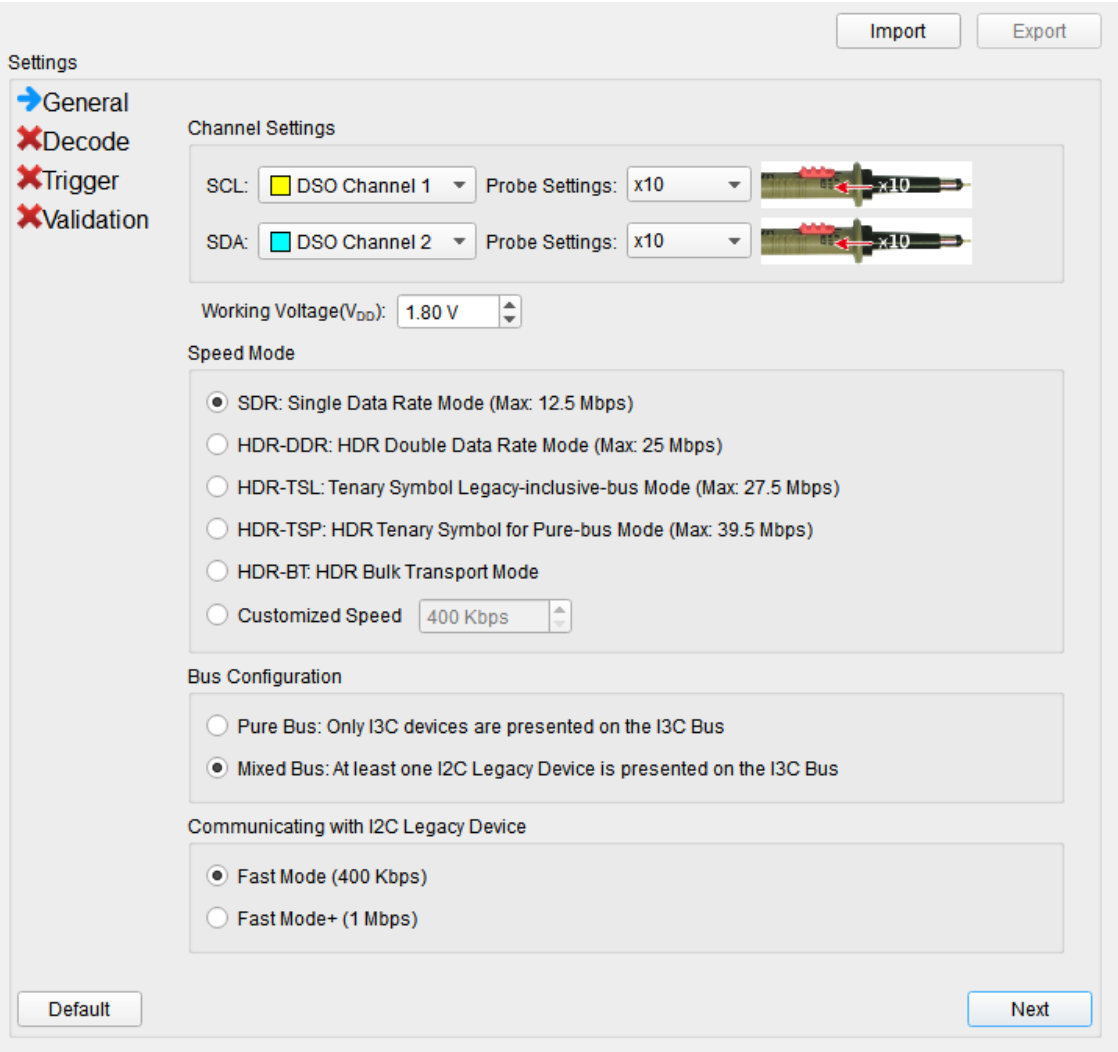


MIPI I3C 向下兼容许多传统 I2C 装置，但同时 I3C 装置还支持更高速传输速率（SCL 时钟频率可达 12.5 MHz）及全新的通信模式。MIPI I3C 工作模式包含 **Single Data Rate (SDR) Mode, High Data Rate (HDR) Mode**. HDR Mode 进一步细分为 **Dual Data Rate (HDR-DDR) Mode, Ternary Symbol Legacy Mode (HDR-TTL) Mode, Ternary Symbol Pure-bus (HDR-TSP) Mode, Bulk Transport (HDR-BT) Mode**.

MIPI I3C 电气特性验证提供多项符合 MIPI I3C 规格的电气测量项目（目前支持 MIPI I3C 版本 1.1.1）。

MIPI I3C Electrical Validation Settings:

1. 一般设置：设置通道来源、工作电压与传输速率。



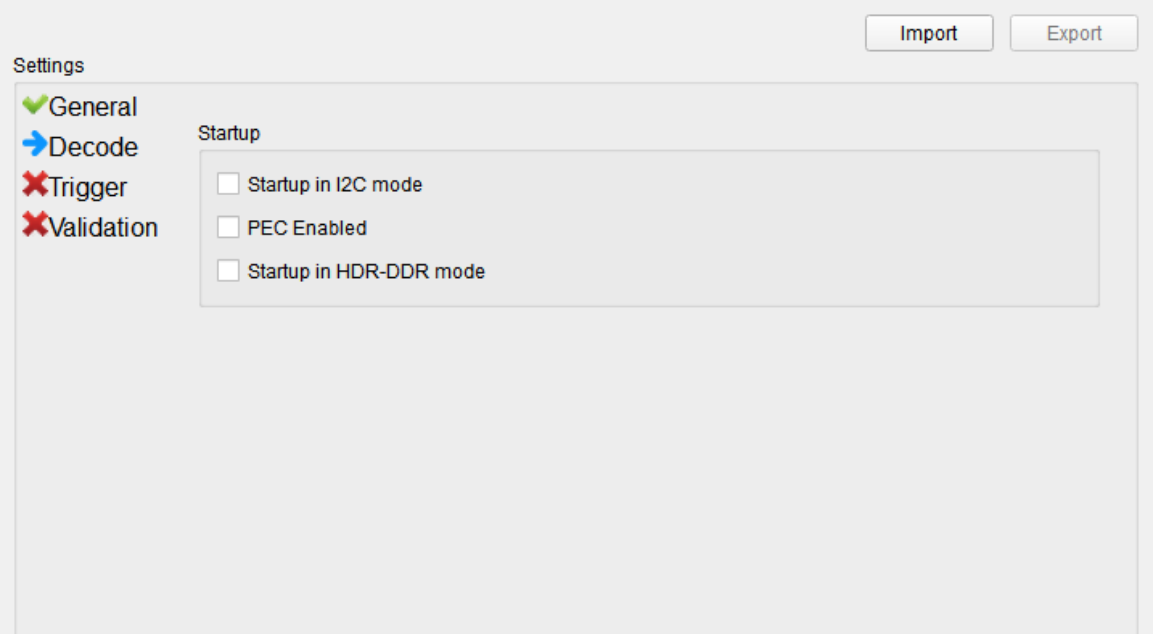
在此部分中，所选的速度模式会影响验证所需的采样率，同时也会影响后续「验证设置」部分中的时序规格表。例如，在 HDR-TSL 与 HDR-TSP 模式下，将额外显示专属的时序规格。

13	✓	t_{EDGE}	Edge-to-Edge Period	32 ns	X
14	✓	t_{SKEW}	Allow Difference Between Signals for 'Simultaneous' Change	X	12.8 ns
15	✓	t_{EYE}	Stable Condition Between Signals	12 ns	X
16	✓	t_{SYMBOL}	Time Between Successive Symbols	32 ns	X
17	✓	t_{CLOCK}	Symbol Clock	77.5 ns	X

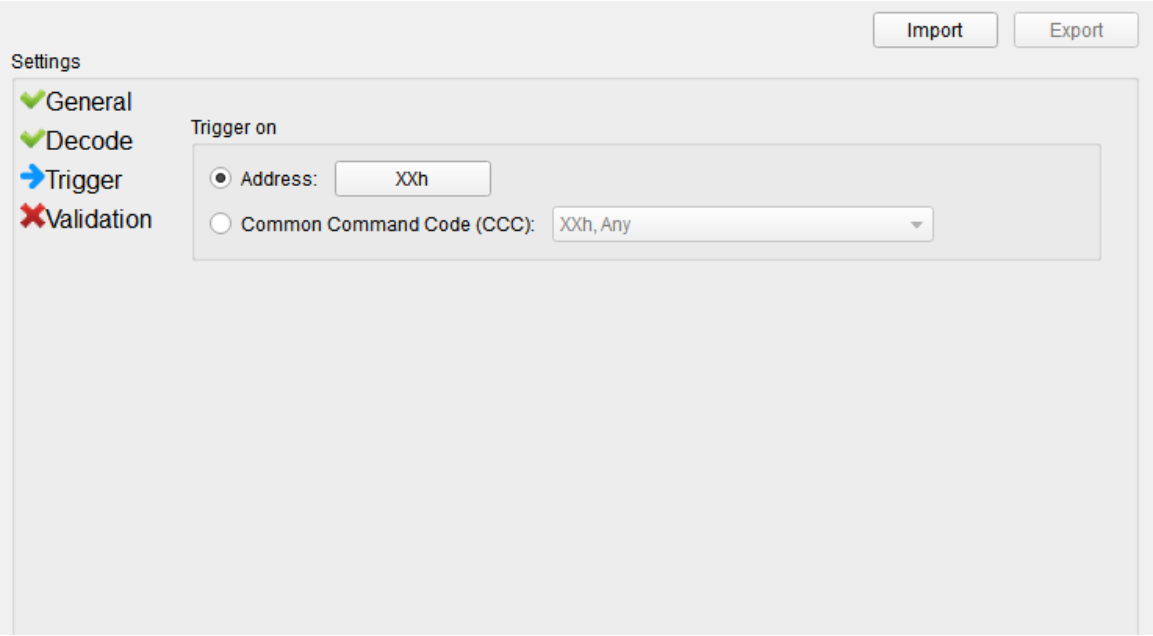
此外，在「Bus Configuration」中需指定总线上连接的装置类型：

- **纯 I3C 总线（Pure-Bus）**：不需要 I2C 时序规格。
- **混合总线（Mixed Bus）**：需加入 I2C 兼容装置的时序规格，默认值采用 Fast Mode（Fm）或 Fast Mode+（Fm+）设置，与 I2C 验证设置相同。

2. 解码设置

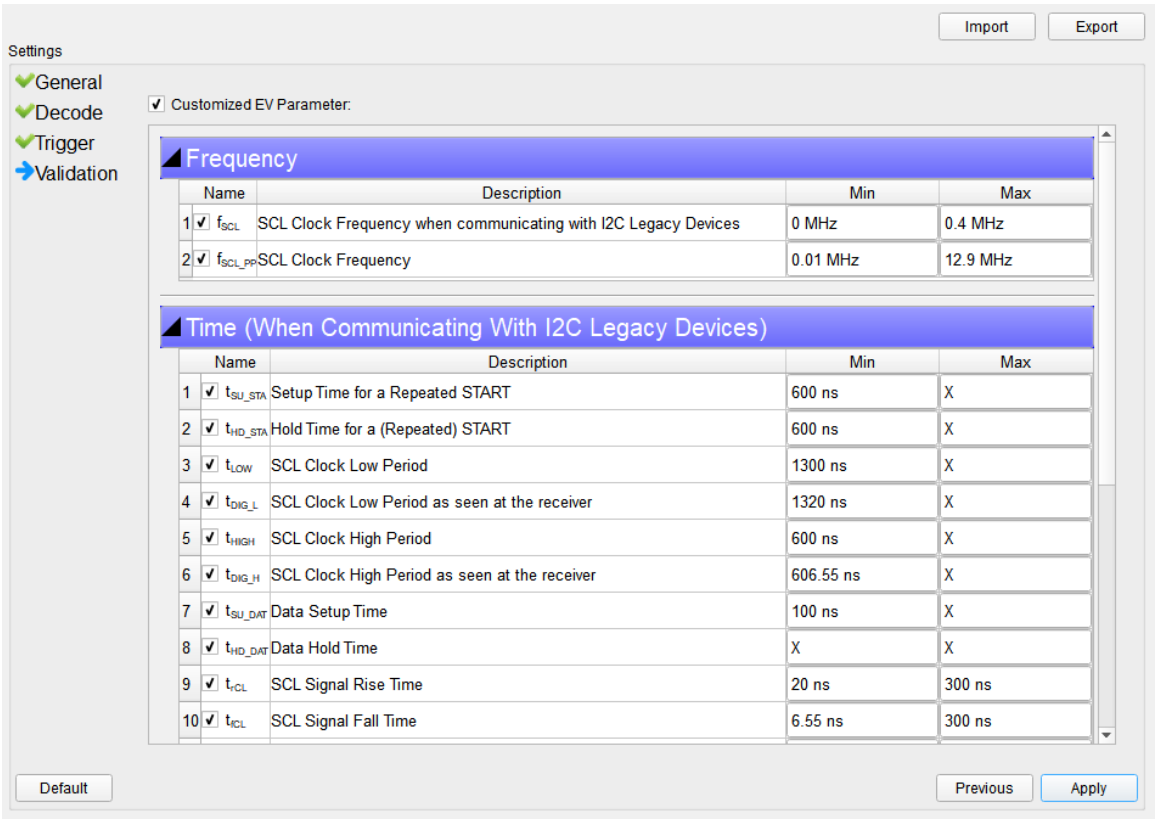


3. 触发设置



若需要分析特定装置地址，可设置特定地址为触发条件。如图中 "XX" 表示「任意」的位，将会触发所有地址。此外亦支持针对常用命令码（CCC）的触发，可透过广播地址 7'h7E 指定。

4. 验证参数设置



本部分共包含五种参数表：

- Frequency
- I3C timing requirements when communicating with I^2C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

若为纯 I3C 总线，则不会显示与 I2C 装置相关的时序表，也不会显示 f_{SCL} 频率参数。

MIPI I3C Frequency Requirements

Symbol	Electrical Parameter
f_{SCL}	SCL Clock Frequency when communicating with I^2C Legacy Devices[1]
t_{SCL_PP}	SCL Clock Frequency
t_{BT_FREQ}	HDR-BT SCL Clock Frequency

MIPI I3C Timing Requirements When Communicating With I^2C Legacy Devices[1]

Symbol		Electrical Parameter
t_{SU_STA}		Setup Time for a REPEATED START
t_{HD_STA}		Hold Time for a (REPEATED) START
t_{LOW}		SCL Clock Low Period
$t\text{-}_{DIG\_L}$		SCL Clock Low Period as seen at the receiver
t_{HIGH}		SCL Clock High Period
t_{DIG_H}		SCL Clock High Period as seen at the receiver
t_{SU_DAT}		Data Setup Time
t_{HD_DAT}		Data Hold Time
t_{rCL}		SCL Signal Rise Time
$t\text{-}_{fCL}$		SCL Signal Fall Time
t_{rDA}		SDA Signal Rise Time
$t\text{-}_{rDA\_OD}$		SDA Signal Rise Time (Open Drain)
$t\text{-}_{fDA}$		SDA Signal Fall Time
t_{SU_STO}		Setup Time for STOP
$t\text{-}_{BUF}$		Bus Free Time Between a STOP and a START
t_{SPIKE}		Pulse Width of Spikes that Spike Filter Must Suppress

[1] Only available when the bus configuration is set to Mixed Bus (i.e. at least one I^2C legacy device is presented on the I3C bus).

MIPI I3C Open Drain Timing Requirements

Symbol	Electrical Parameter
t_{LOW_OD}	SCL Clock Low Period
$t_{DIG\_OD\_L}$	SCL Clock Low Period as seen at the receiver
t_{HIGH_INIT}	High Period of SCL Clock (for First Broadcast Address)
$t\text{-}_{HIGH\_OD}$	SCL Clock High Period
$t_{DIG\_OD\_H}$	SCL Clock High Period as seen at the receiver
t_{fDA_OD}	SDA Data Fall Time
t_{SU_OD}	SDA Data Setup Time During Open Drain Mode
t_{CAS}	Clock After START (S) Condition
t_{CBP}	Clock Before STOP (P) Condition
$t\text{-}_{CRHPOverlap}$	Active Controller to Secondary Overlap time during handoff
t_{AVAL}	Bus Available Condition
$t\text{-}_{IDLE}$	Bus Idle Condition
$t_{NEWCRLock}$	Time Interval Where New Controller Not Driving SDA Low

MIPI I3C Push-Pull Timing Requirements

Symbol	Electrical Parameter
t_{LOW}	SCL Clock Low Period
t_{DIG_L}	SCL Clock Low Period as seen at the receiver
t_{HIGH}	SCL Clock High Period
t_{DIG_H}	SCL Clock High Period as seen at the receiver
t_{SCO}	Clock in to Data Out for Target
t_{CR_PP}	SCL Clock Rise Time
t_{CF_PP}	SCL Clock Fall Time
$t_{HD-\_PP\_Controller}$	SDA Signal Data Hold (Controller)
$t\text{-}_{HD\_PP\_Target}$	SDA Signal Data Hold (Target)
t_{SU_PP}	SDA Signal Data Setup
$t\text{-}_{CASr}$	Clock After Repeated START (Sr) Condition
t_{CBSr}	Clock Before Repeated START (Sr) Condition
t_{BT_HO}	HDR-BT Master to Slave Hand Off Delay
t_{BT_STALL}	HDR-BT Clocked Not-Ready Data-Block Headers

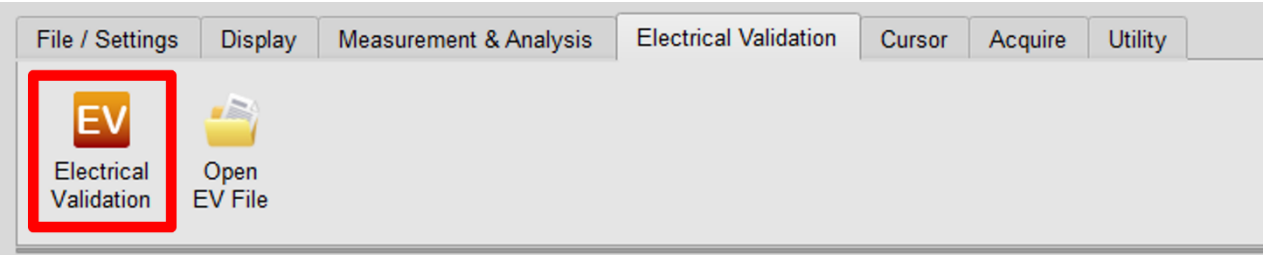
MIPI I3C I/O Stage Characteristics Voltage Requirements

Symbol	Electrical Parameter
V_{IL}	Low-Level Input Voltage
V_{IH}	High-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage

5. 电气特性验证_软件画面

MIPI RFFE 电气特性验证解决方案

■ 简介：

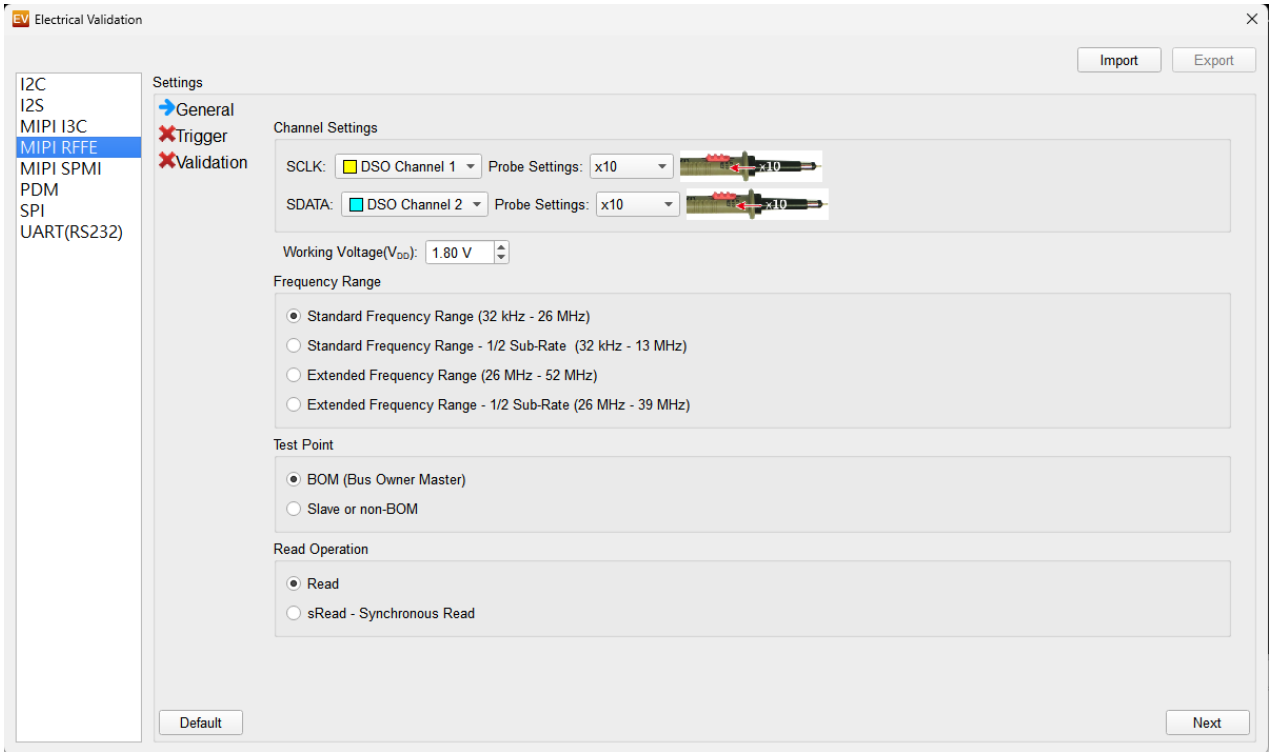


MIPI RFFE（Radio Frequency Front-End）是由 MIPI 联盟所制定的标准规范，用以定义移动装置（如智能型手机和平板电脑）中基带处理器与射频前端模块之间的通信标准。这是 MIPI (Mobile Industry Processor Interface) 标准家族的重要组成部分，涵盖多种针对移动与嵌入式设备中组件之间通信效率所设计的标准。

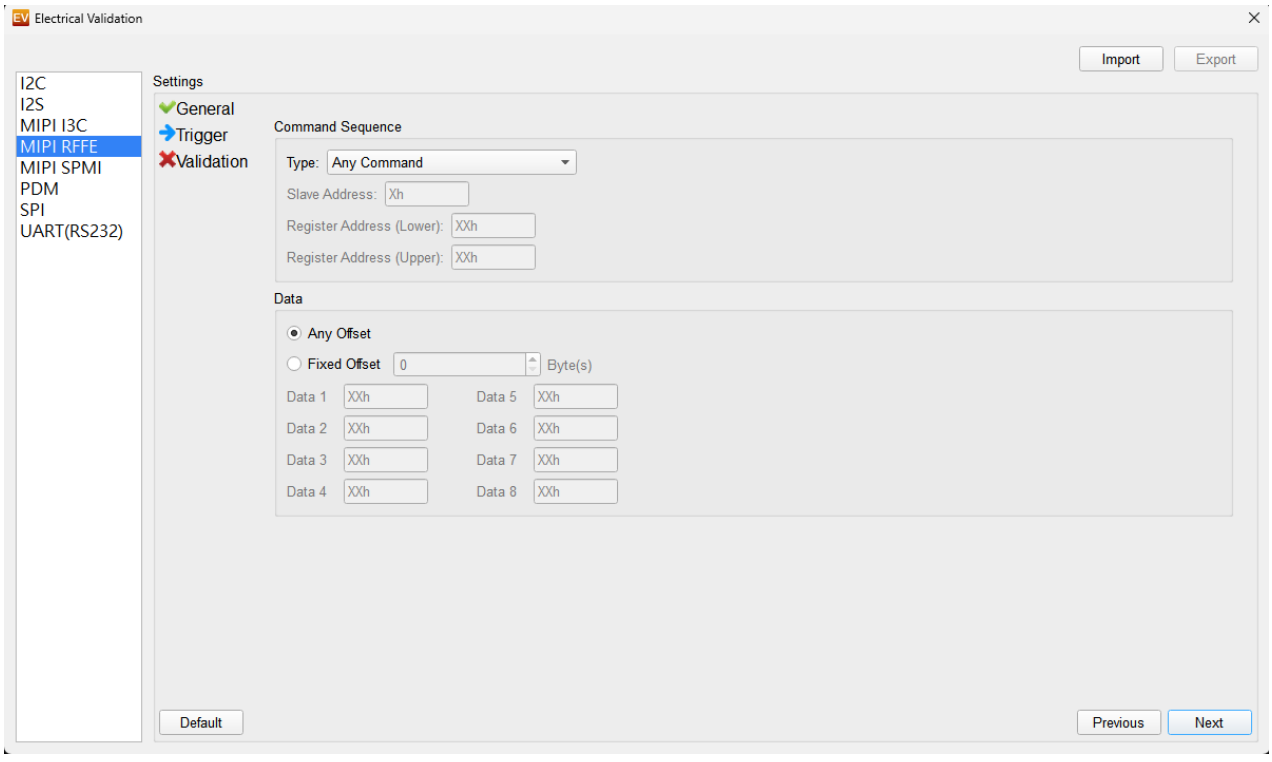
MIPI RFFE 是现代无线设备的关键技术，提供一个标准化且高效的接口，用于控制无线通信系统中的射频前端组件。

MIPI RFFE 电气特性验证设置：

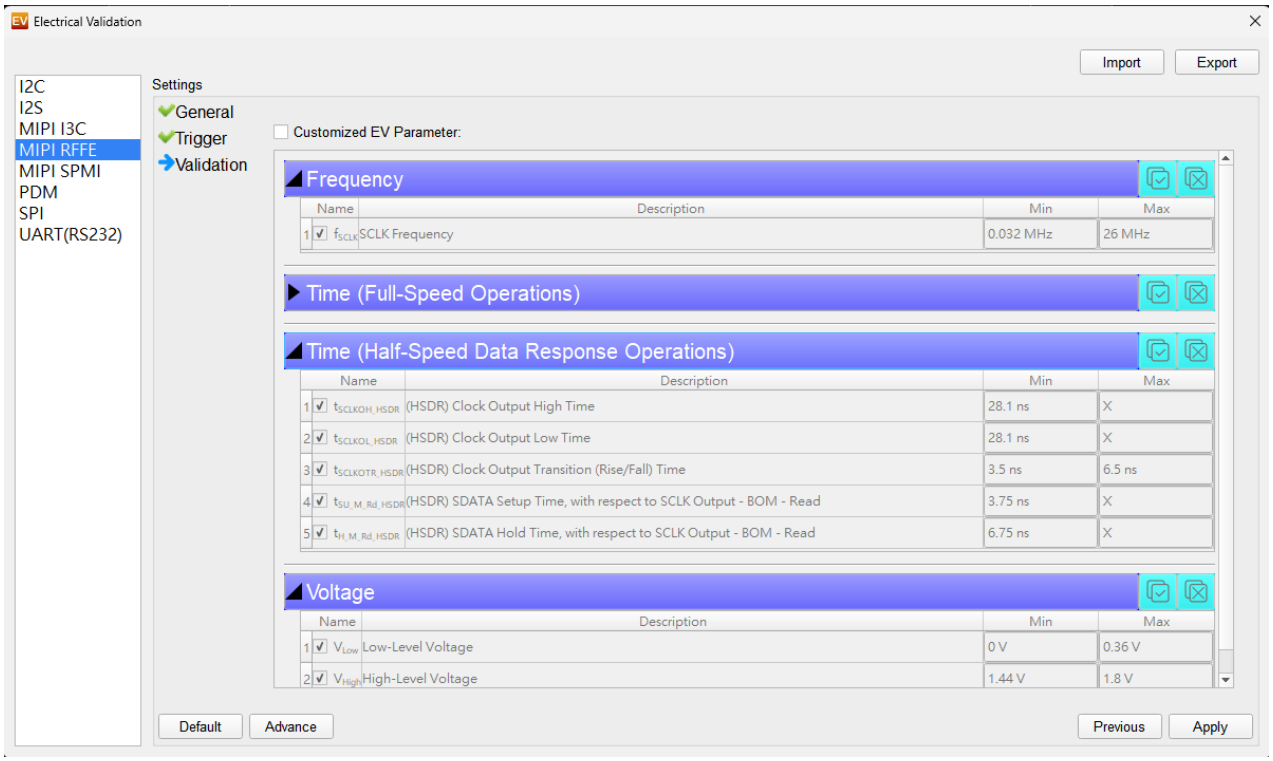
1. **一般设置：**设置通道来源、工作电压、频率范围、Test Point 和 Read Operation。



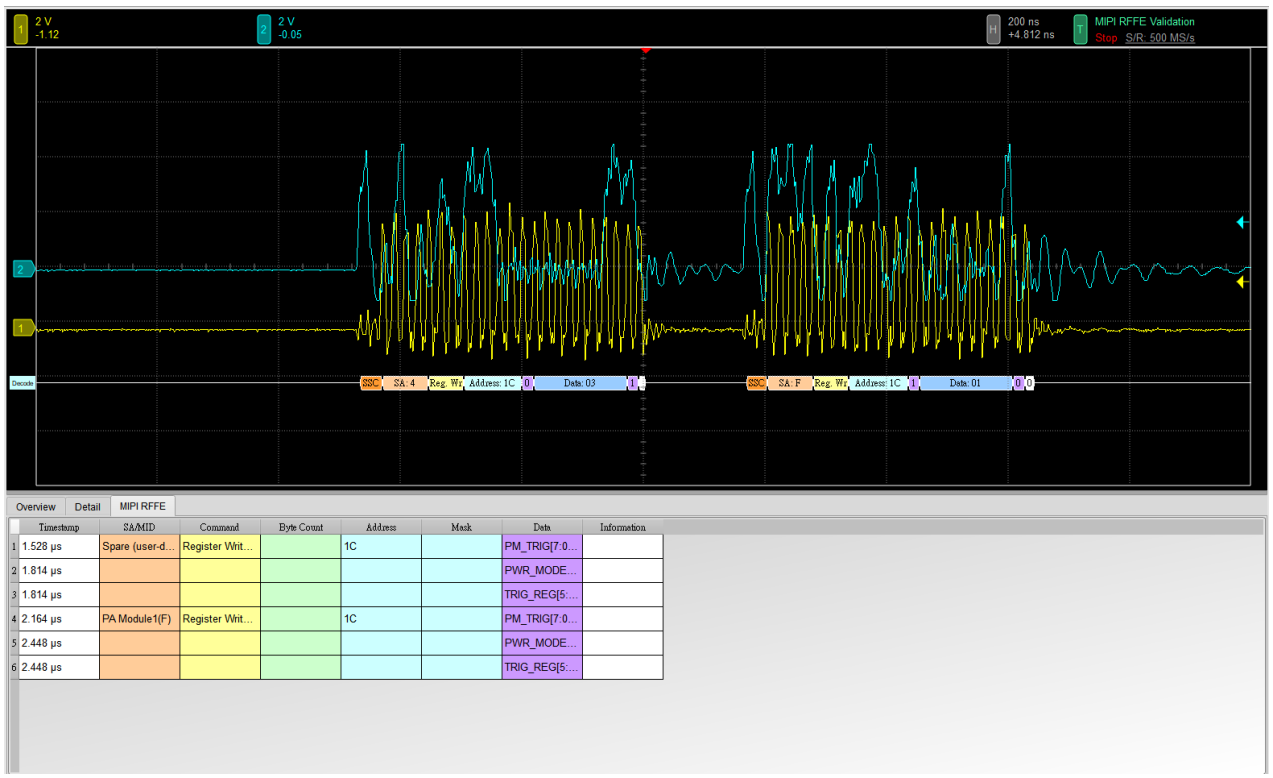
2. **触发设置**



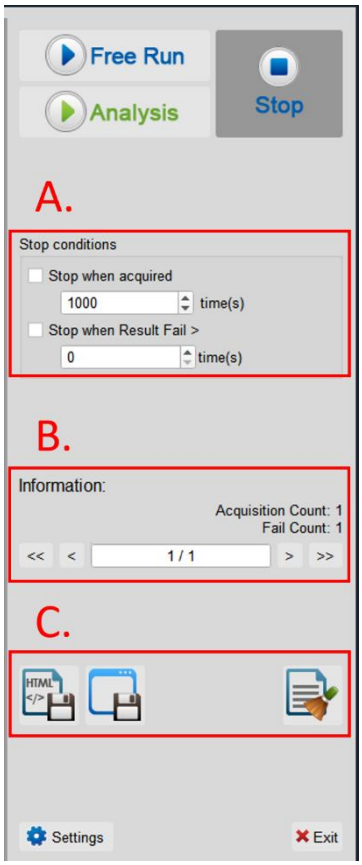
3. 验证设置：包含电压、时序与频率的限制条件



4. 电气特性验证_软件画面



5. 控制面板



A. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

B. 信息：

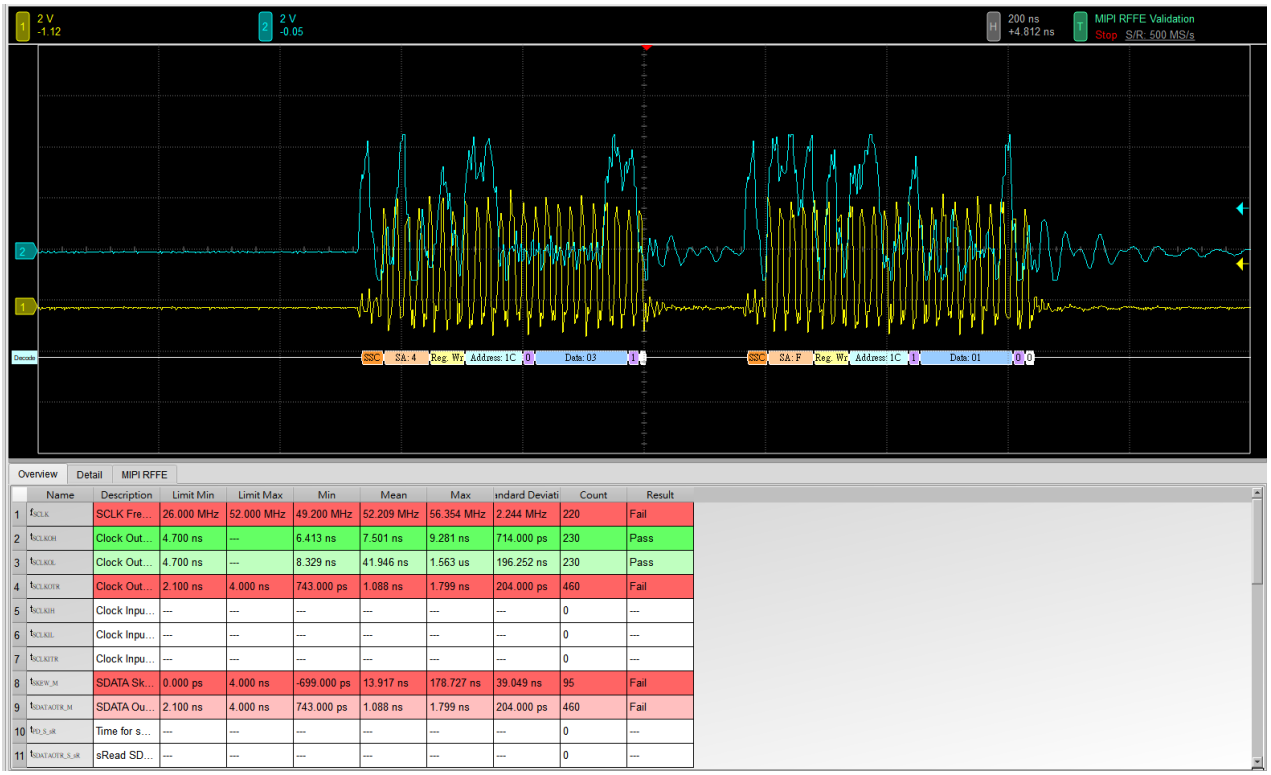
选择查看波形

C. 储存档案：

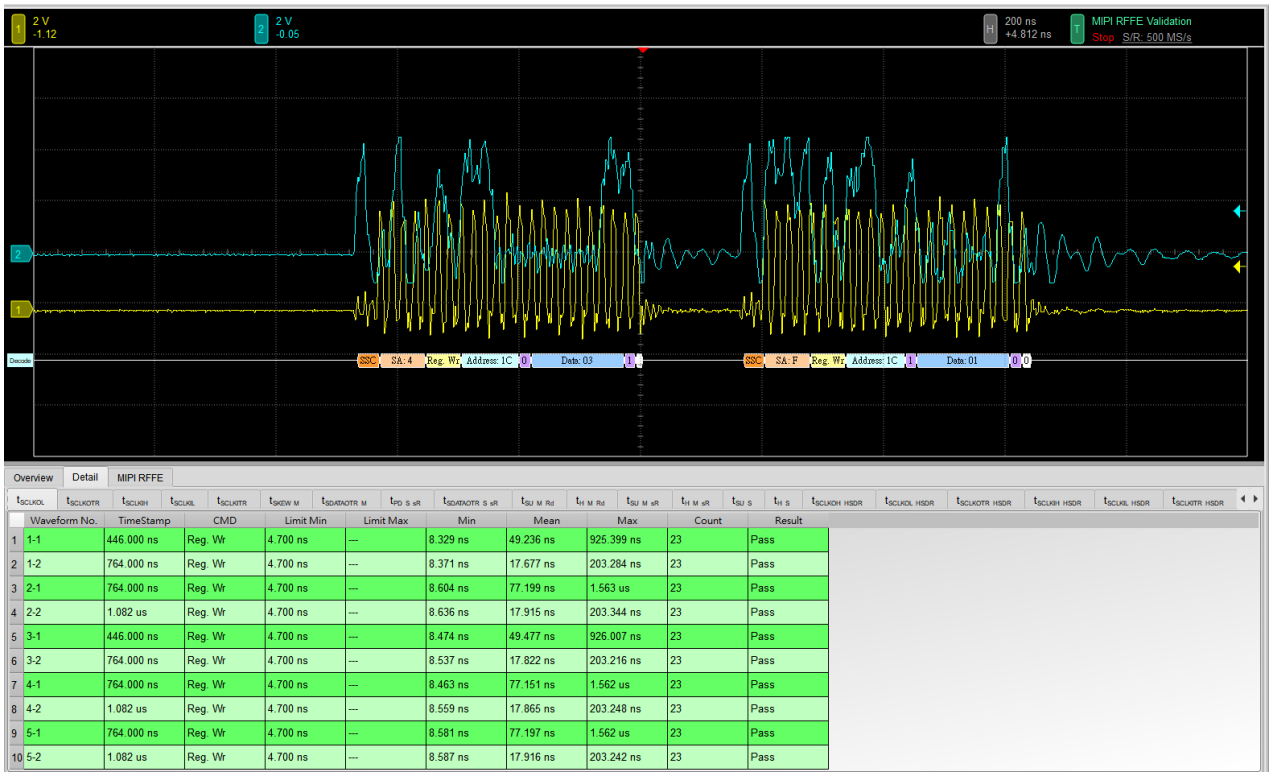
储存为 HTML 格式

储存为 .MOW（Acute软件专用格式）

6. 概览报告

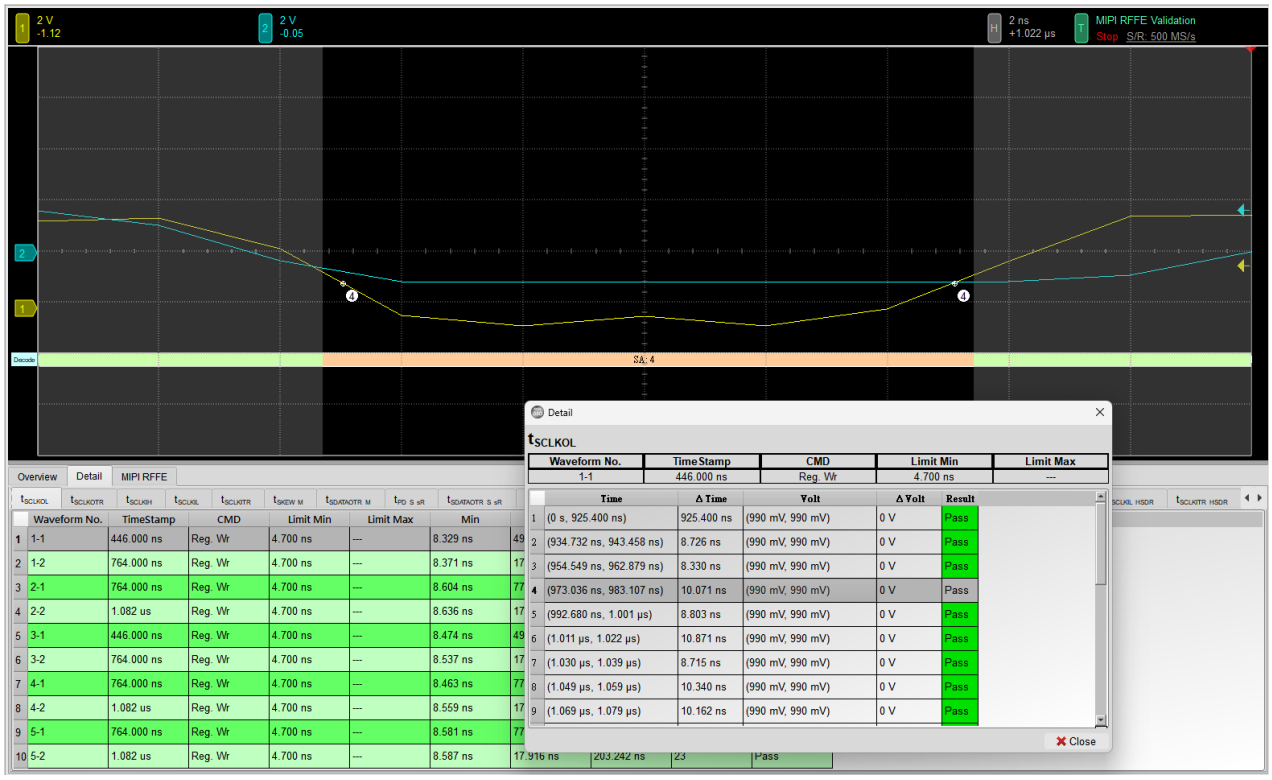


7. 详细报告



	Waveform No.	TimeStamp	CMD	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	446.000 ns	Reg. Wr	4.700 ns	---	8.329 ns	49.236 ns	925.399 ns	23	Pass
2	1-2	764.000 ns	Reg. Wr	4.700 ns	---	8.371 ns	17.677 ns	203.284 ns	23	Pass
3	2-1	764.000 ns	Reg. Wr	4.700 ns	---	8.604 ns	77.199 ns	1.563 us	23	Pass
4	2-2	1.082 us	Reg. Wr	4.700 ns	---	8.636 ns	17.915 ns	203.344 ns	23	Pass
5	3-1	446.000 ns	Reg. Wr	4.700 ns	---	8.474 ns	49.477 ns	926.007 ns	23	Pass
6	3-2	764.000 ns	Reg. Wr	4.700 ns	---	8.537 ns	17.822 ns	203.216 ns	23	Pass
7	4-1	764.000 ns	Reg. Wr	4.700 ns	---	8.463 ns	77.151 ns	1.562 us	23	Pass
8	4-2	1.082 us	Reg. Wr	4.700 ns	---	8.559 ns	17.865 ns	203.248 ns	23	Pass
9	5-1	764.000 ns	Reg. Wr	4.700 ns	---	8.581 ns	77.197 ns	1.562 us	23	Pass
10	5-2	1.082 us	Reg. Wr	4.700 ns	---	8.587 ns	17.916 ns	203.242 ns	23	Pass

8. 波形和参考点



	Waveform No.	TimeStamp	CMD	Limit Min	Limit Max	Min
1	1-1	446.000 ns	Reg. Wr	4.700 ns	---	8.329 ns
2	1-2	764.000 ns	Reg. Wr	4.700 ns	---	8.371 ns
3	2-1	764.000 ns	Reg. Wr	4.700 ns	---	8.604 ns
4	2-2	1.082 us	Reg. Wr	4.700 ns	---	8.636 ns
5	3-1	446.000 ns	Reg. Wr	4.700 ns	---	8.474 ns
6	3-2	764.000 ns	Reg. Wr	4.700 ns	---	8.537 ns
7	4-1	764.000 ns	Reg. Wr	4.700 ns	---	8.463 ns
8	4-2	1.082 us	Reg. Wr	4.700 ns	---	8.559 ns
9	5-1	764.000 ns	Reg. Wr	4.700 ns	---	8.581 ns
10	5-2	1.082 us	Reg. Wr	4.700 ns	---	8.587 ns

9. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 15:32:11
S/W Version	1.8.62
Protocol	MIPI RFFE

Overview Results:

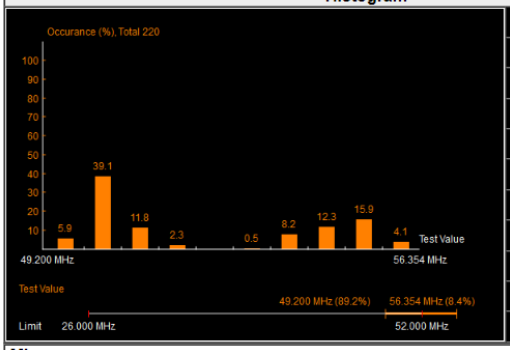
Total: 33
Pass: 2
Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCLK}	SCLK Frequency	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	89.2%	8.4%	✖Fail
2	t_{SCLKOH}	Clock Output High Time	4.700 ns	---	6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	36.4%	---	✔Pass
3	t_{SCLKOL}	Clock Output Low Time	4.700 ns	---	8.329 ns	41.946 ns	1.563 us	196.252 ns	230	77.2%	---	✔Pass
4	$t_{SCLKOTR}$	Clock Output Transition (Rise/Fall) Time	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	✖Fail
5	t_{SCLKIH}	Clock Input High Time	---	---	---	---	---	---	0	---	---	---
6	t_{SCLKIL}	Clock Input Low Time	---	---	---	---	---	---	0	---	---	---
7	$t_{SCLKITR}$	Clock Input Transition (Rise/Fall) Time	---	---	---	---	---	---	0	---	---	---
8	t_{SKEW_M}	SDATA Skew Relative to SCLK, BOM Master Output	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95	---	4368.2%	✖Fail
9	$t_{SDATAOTR\_M}$	SDATA Output Transition (Rise/Fall) Time, BOM Master	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	✖Fail
10	$t_{PD\_S\_sR}$	Time for sRead Data Output Valid from SCLK Rising Edge - Slave	---	---	---	---	---	---	0	---	---	---
11	$t_{SDATAOTR\_S\_sR}$	sRead SDATA Output Transition (Rise/Fall) Time - Slave	---	---	---	---	---	---	0	---	---	---
12	$t_{SU\_M\_Rd}$	SDATA Setup Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---
13	$t_{H\_M\_Rd}$	SDATA Hold Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---
14	$t_{SU\_M\_sR}$	SDATA Setup Time, with respect to SCLK Output - BOM - sRead	---	---	---	---	---	---	0	---	---	---
15	$t_{H\_M\_sR}$	SDATA Hold Time, with respect to SCLK Output - BOM - sRead	---	---	---	---	---	---	0	---	---	---
16	t_{SU_S}	SDATA Setup Time, with respect to SCLK Input - Slave (or non-BOM)	---	---	---	---	---	---	0	---	---	---
17	t_{H_S}	SDATA Hold Time, with respect to SCLK Input - Slave (or non-BOM)	---	---	---	---	---	---	0	---	---	---
18	t_{SCLKOH_HSDR}	(HSDR) Clock Output High Time	---	---	---	---	---	---	0	---	---	---
19	t_{SCLKOL_HSDR}	(HSDR) Clock Output Low Time	---	---	---	---	---	---	0	---	---	---
20	$t_{SCLKOTR\_HSDR}$	(HSDR) Clock Output Transition (Rise/Fall) Time	---	---	---	---	---	---	0	---	---	---
21	t_{SCLKIH_HSDR}	(HSDR) Clock Input High Time	---	---	---	---	---	---	0	---	---	---
22	t_{SCLKIL_HSDR}	(HSDR) Clock Input Low Time	---	---	---	---	---	---	0	---	---	---
23	$t_{SCLKITR\_HSDR}$	(HSDR) Clock Input Transition (Rise/Fall) Time	---	---	---	---	---	---	0	---	---	---
24	$t_{PD\_S\_Rd\_HSDR}$	(HSDR) Time for Read Data Output Valid from SCLK Rising Edge - Slave	---	---	---	---	---	---	0	---	---	---
25	$t_{SDATAOTR\_S\_Rd\_HSDR}$	(HSDR) Read SDATA Output Transition (Rise/Fall) Time - Slave	---	---	---	---	---	---	0	---	---	---
26	$t_{PD\_S\_sR\_HSDR}$	(HSDR) Time for sRead Data Output Valid from SCLK Rising Edge - Slave	---	---	---	---	---	---	0	---	---	---
27	$t_{SDATAOTR\_S\_sR\_HSDR}$	(HSDR) sRead SDATA Output Transition (Rise/Fall) Time - Slave	---	---	---	---	---	---	0	---	---	---
28	$t_{SU\_M\_Rd\_HSDR}$	(HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---
29	$t_{H\_M\_Rd\_HSDR}$	(HSDR) SDATA Hold Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---

f_{SCLK} - Test Result: Fail
Description: SCLK Frequency

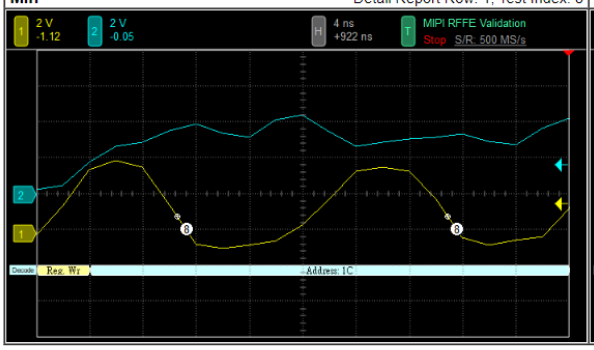
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	89.2%	8.4%

Histogram

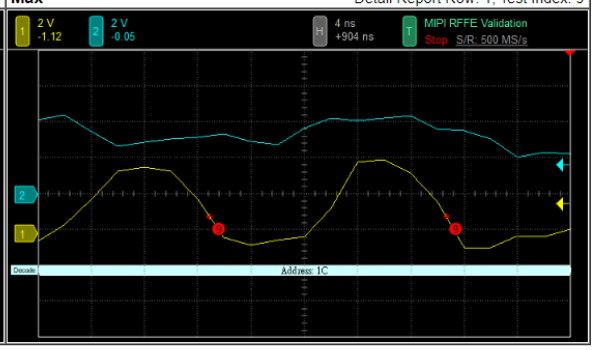


Value Range	Occurance Count
49.2 MHz ~ 49.916 MHz	13
49.916 MHz ~ 50.631 MHz	86
50.631 MHz ~ 51.347 MHz	26
51.347 MHz ~ 52.062 MHz	5
52.062 MHz ~ 52.777 MHz	0
52.777 MHz ~ 53.493 MHz	1
53.493 MHz ~ 54.208 MHz	18
54.208 MHz ~ 54.923 MHz	27
54.923 MHz ~ 55.639 MHz	35
55.639 MHz ~ 56.354 MHz	9

Min Detail Report Row: 1, Test Index: 8

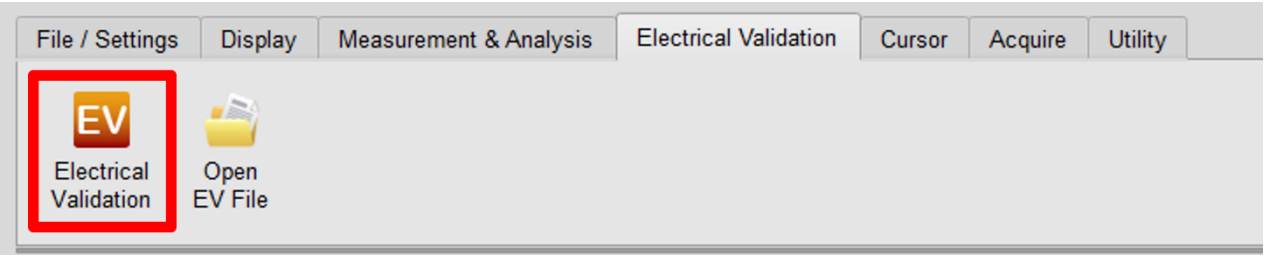


Max Detail Report Row: 1, Test Index: 9



MIPI SPMI 电气特性验证解决方案

■ 简介：

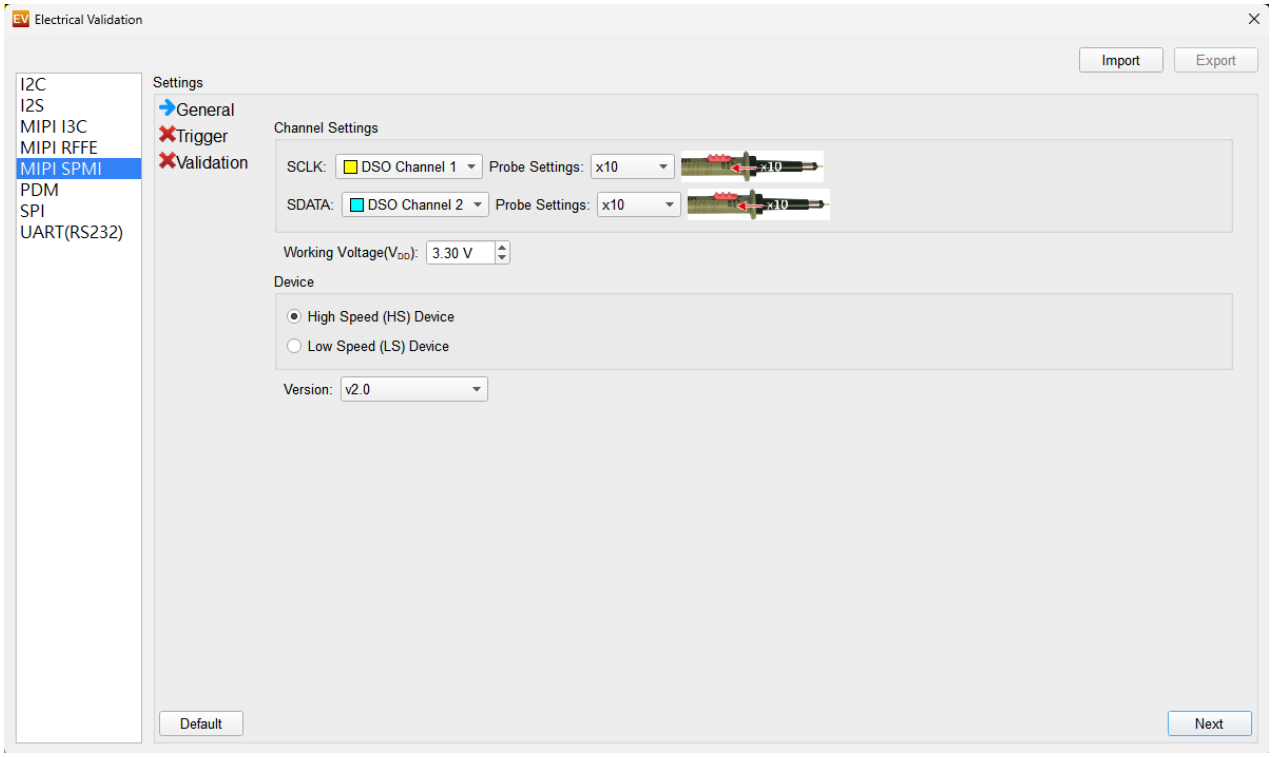


使用示波器执行 MIPI SPMI 电气特性验证，以确保 MIPI SPMI 协议符合既定规格。在经过长时间持续运行测试后，可确认所测试的信号电气特性是否符合标准。

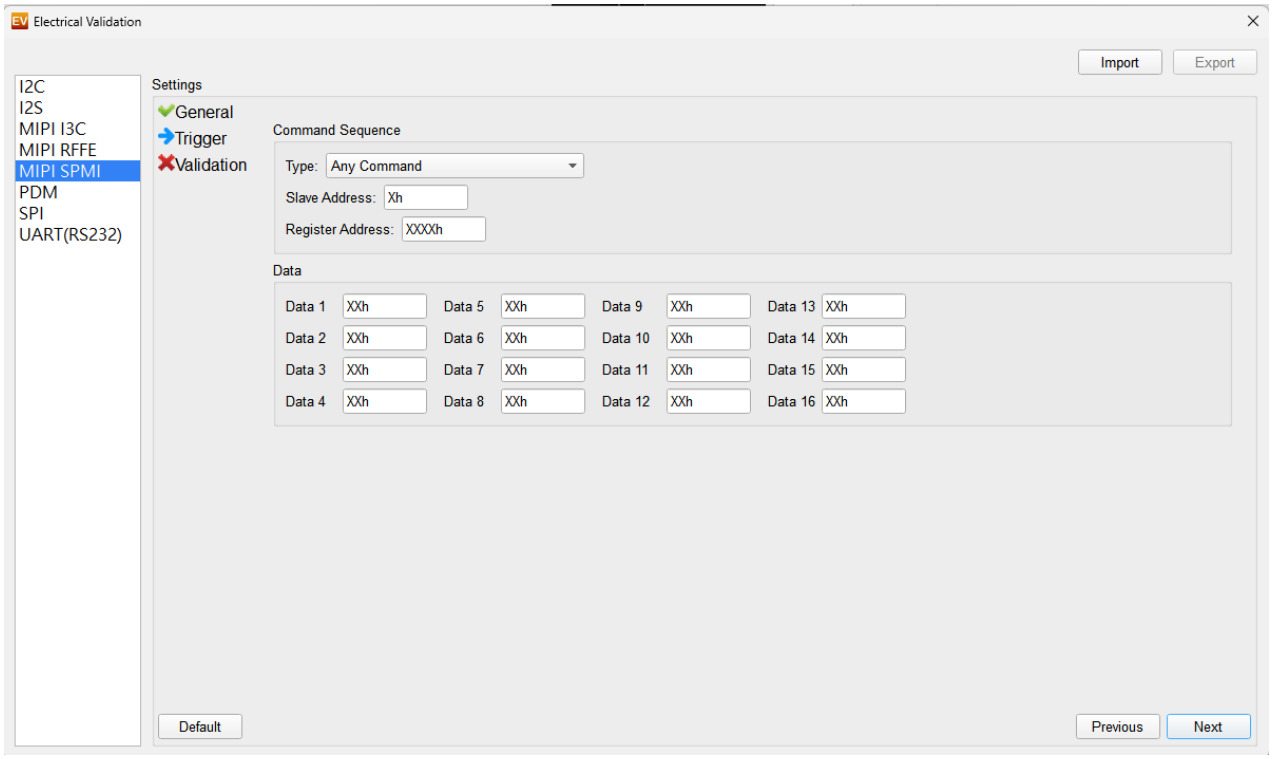
MIPI SPMI（System Power Management Interface）是由 MIPI 联盟（Mobile Industry Processor Interface）制定的标准规范，主要目的是为了在移动与嵌入式系统中实现电源管理。SPMI 提供标准化的通信接口，用于在电源管理 IC（PMIC）与各个系统组件之间有效地分配电力移管理电源状态，常见于智能型手机、平板电脑等装置中。

MIPI SPMI 电气特性验证设置

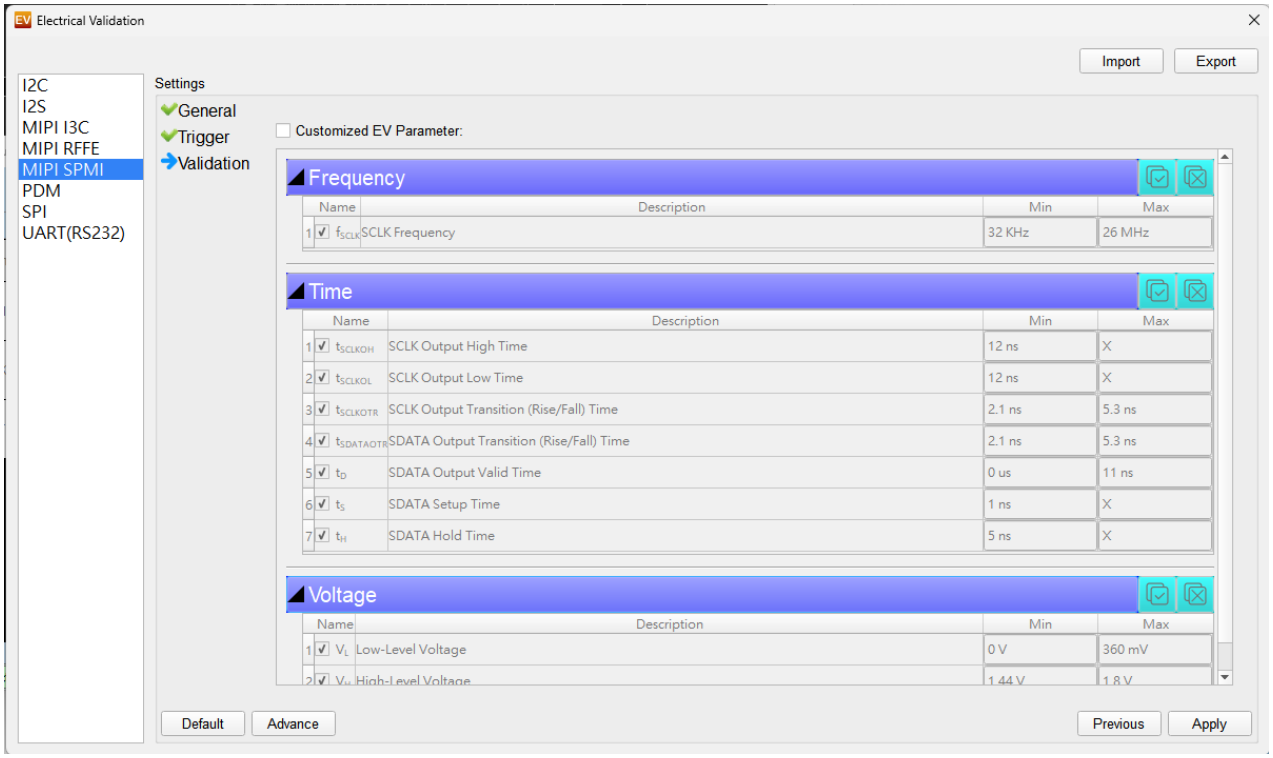
1. 一般设置：设置通道来源、工作电压、传输速率与协议版本。



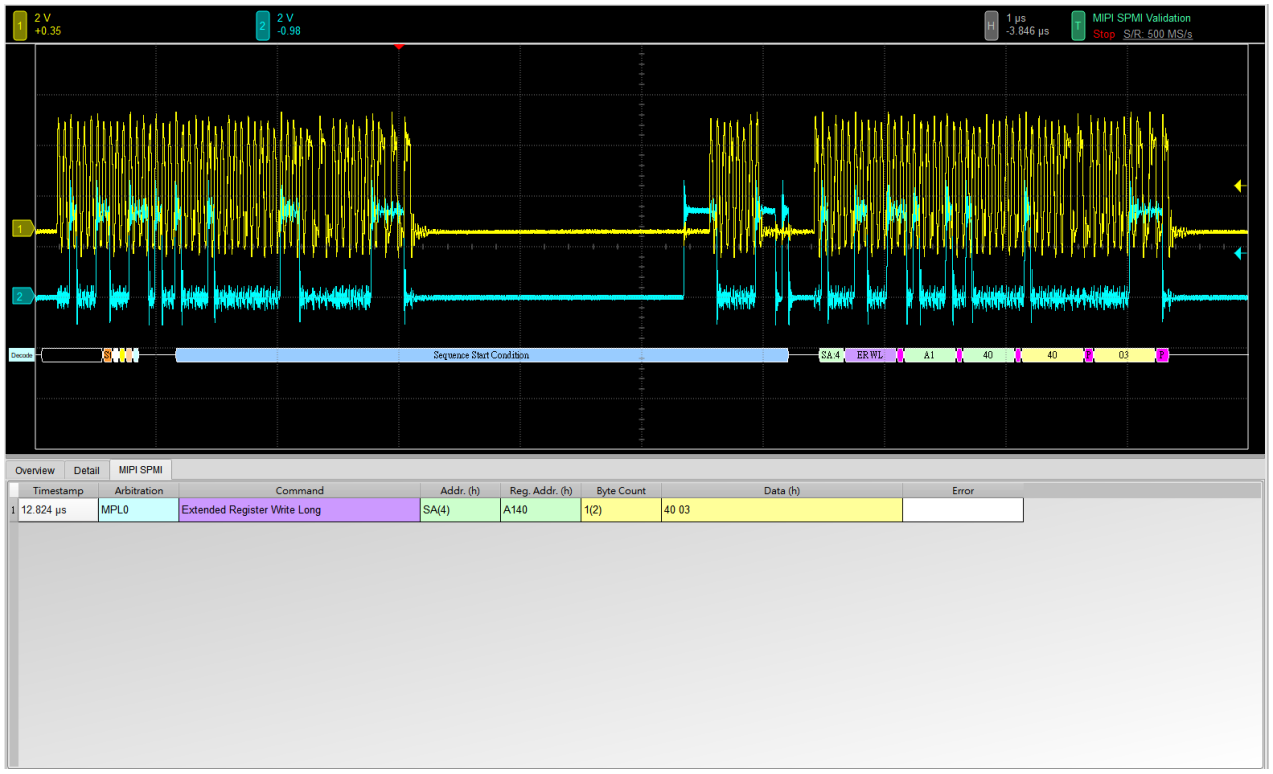
2. 触发设置



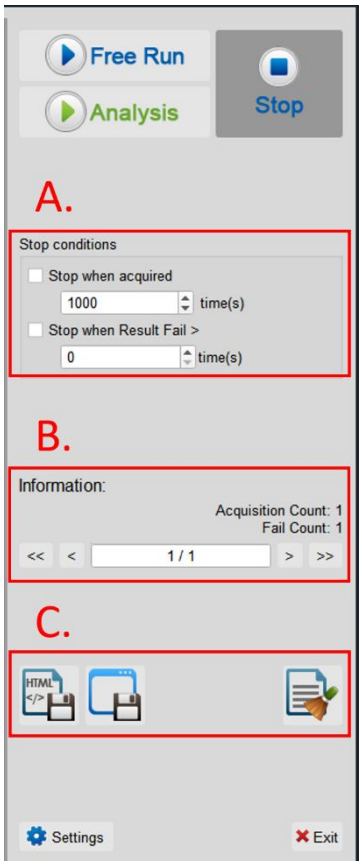
3. 验证参数设置：包含频率、时间与电压限制条件



4. 电气特性验证_软件画面



5. 控制面板



A. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

B. 信息：

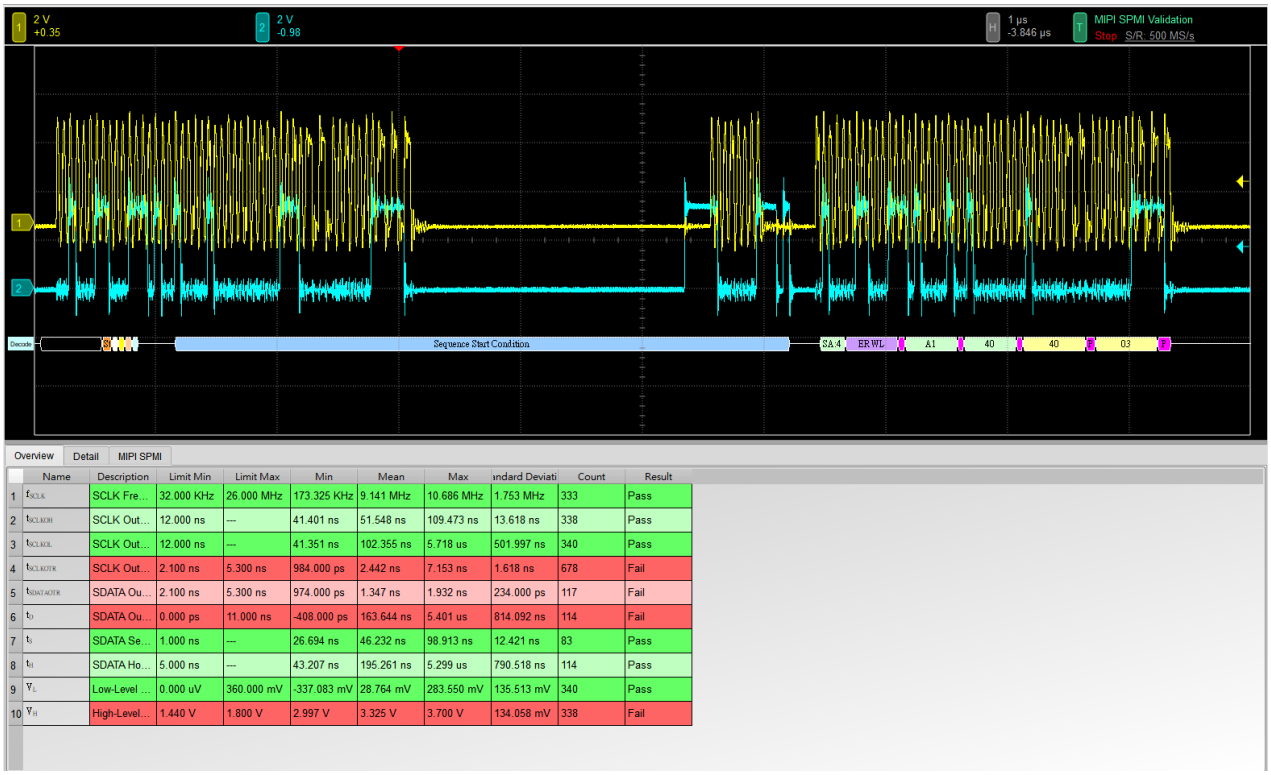
选择查看波形

C. 储存档案：

储存为 HTML 格式

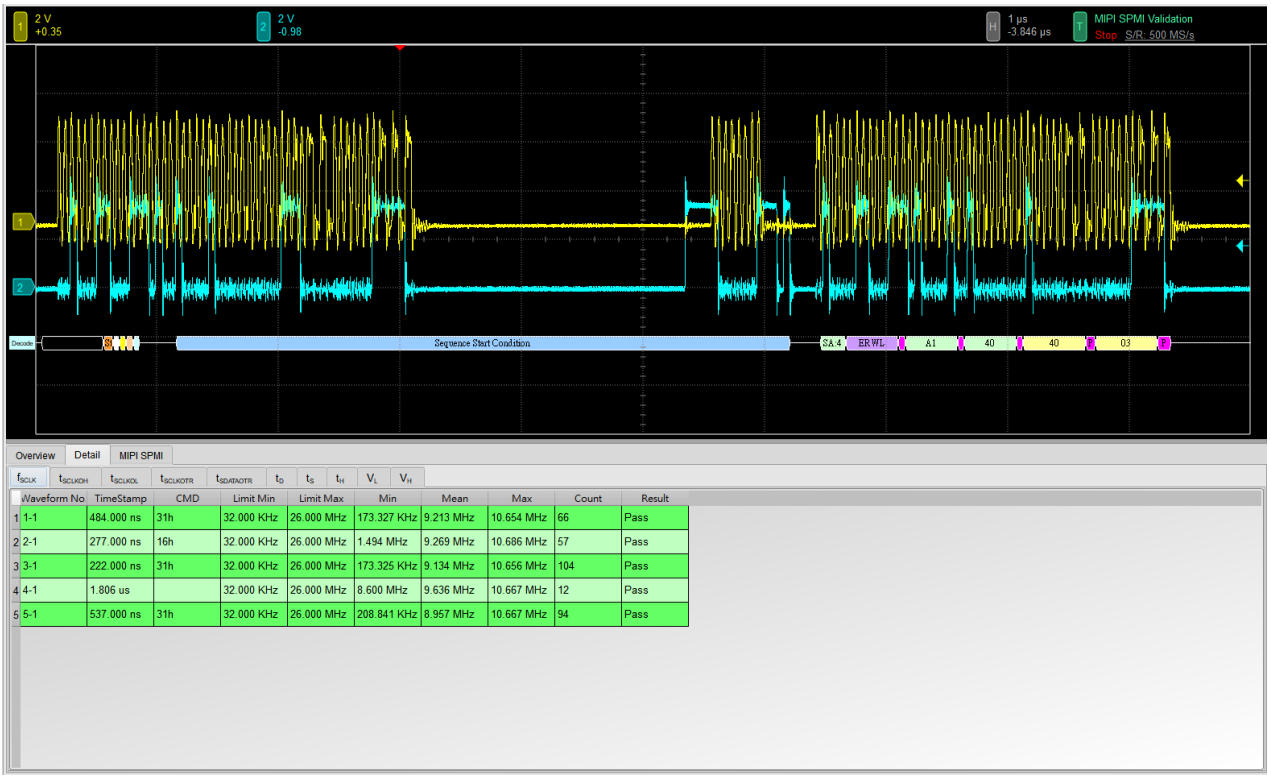
储存为 .MOW（Acute软件专用格式）

6. 概览报告



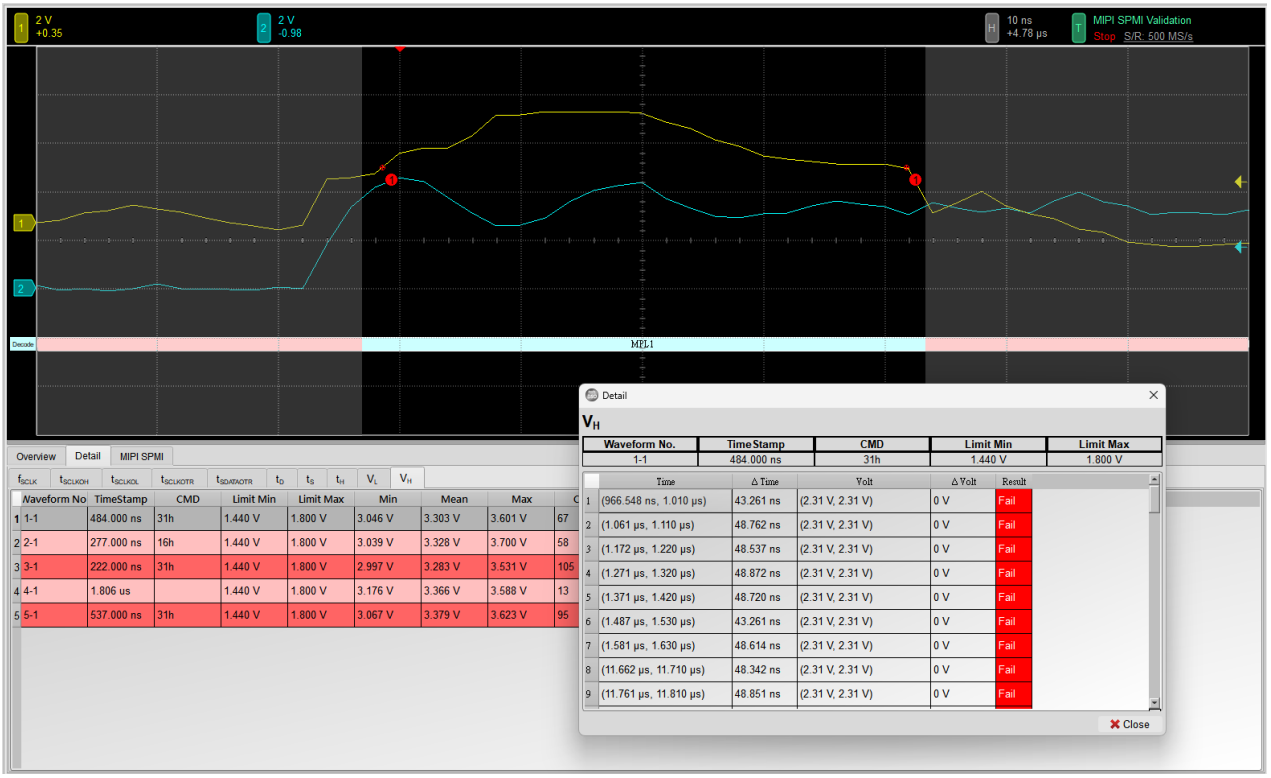
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviati	Count	Result
1	t_{SCLK}	SCLK Fre...	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	Pass
2	t_{SCLKOH}	SCLK Out...	12.000 ns	---	41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	Pass
3	t_{SCLKOL}	SCLK Out...	12.000 ns	---	41.351 ns	102.355 ns	5.718 us	501.997 ns	340	Pass
4	$t_{SCLKOTK}$	SCLK Out...	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	Fail
5	$t_{SDATAOTK}$	SDATA Ou...	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	Fail
6	t_O	SDATA Ou...	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	Fail
7	t_S	SDATA Se...	1.000 ns	---	26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	Pass
8	t_H	SDATA Ho...	5.000 ns	---	43.207 ns	195.261 ns	5.299 us	790.518 ns	114	Pass
9	V_L	Low-Level ...	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340	Pass
10	V_H	High-Level...	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	Fail

7. 详细报告



Waveform No	TimeStamp	CMD	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1 1-1	484.000 ns	31h	32.000 KHz	26.000 MHz	173.327 KHz	9.213 MHz	10.654 MHz	66	Pass
2 2-1	277.000 ns	16h	32.000 KHz	26.000 MHz	1.494 MHz	9.269 MHz	10.686 MHz	57	Pass
3 3-1	222.000 ns	31h	32.000 KHz	26.000 MHz	173.325 KHz	9.134 MHz	10.656 MHz	104	Pass
4 4-1	1.806 us		32.000 KHz	26.000 MHz	8.600 MHz	9.636 MHz	10.667 MHz	12	Pass
5 5-1	537.000 ns	31h	32.000 KHz	26.000 MHz	208.841 KHz	8.957 MHz	10.667 MHz	94	Pass

8. 波形和参考点



Waveform No	TimeStamp	CMD	Limit Min	Limit Max	Min	Mean	Max	C
1 1-1	484.000 ns	31h	1.440 V	1.800 V	3.046 V	3.303 V	3.601 V	67
2 2-1	277.000 ns	16h	1.440 V	1.800 V	3.039 V	3.328 V	3.700 V	58
3 3-1	222.000 ns	31h	1.440 V	1.800 V	2.997 V	3.283 V	3.531 V	105
4 4-1	1.806 us		1.440 V	1.800 V	3.176 V	3.366 V	3.588 V	13
5 5-1	537.000 ns	31h	1.440 V	1.800 V	3.067 V	3.379 V	3.623 V	95

Waveform No.	TimeStamp	CMD	Limit Min	Limit Max
1-1	484.000 ns	31h	1.440 V	1.800 V

	Time	Δ Time	Volt	Δ Volt	Result
1	(966.548 ns, 1.010 µs)	43.261 ns	(2.31 V, 2.31 V)	0 V	Fail
2	(1.061 µs, 1.110 µs)	48.762 ns	(2.31 V, 2.31 V)	0 V	Fail
3	(1.172 µs, 1.220 µs)	48.537 ns	(2.31 V, 2.31 V)	0 V	Fail
4	(1.271 µs, 1.320 µs)	48.872 ns	(2.31 V, 2.31 V)	0 V	Fail
5	(1.371 µs, 1.420 µs)	48.720 ns	(2.31 V, 2.31 V)	0 V	Fail
6	(1.487 µs, 1.530 µs)	43.261 ns	(2.31 V, 2.31 V)	0 V	Fail
7	(1.581 µs, 1.630 µs)	48.614 ns	(2.31 V, 2.31 V)	0 V	Fail
8	(11.662 µs, 11.710 µs)	48.342 ns	(2.31 V, 2.31 V)	0 V	Fail
9	(11.761 µs, 11.810 µs)	48.851 ns	(2.31 V, 2.31 V)	0 V	Fail

Close

9. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 14:54:25
S/W Version	1.8.62
Protocol	MIPI SPMI

Overview Results:

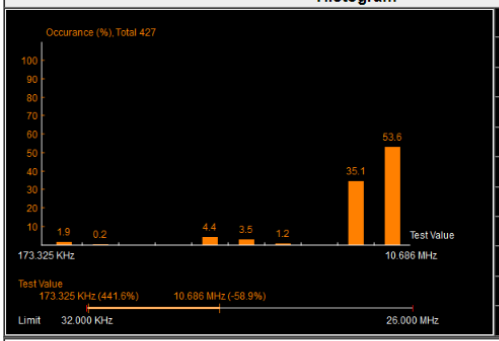
Total: 10
Pass: 6
Fail: 4

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCLK}	SCLK Frequency	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	441.6%	-58.9%	Pass
2	t_{SCLKOH}	SCLK Output High Time	12.000 ns	---	41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	245.0%	---	Pass
3	t_{SCLKOL}	SCLK Output Low Time	12.000 ns	---	41.351 ns	102.355 ns	5.718 us	501.997 ns	340	244.6%	---	Pass
4	$t_{SCLKOTR}$	SCLK Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	-53.1%	35.0%	Fail
5	$t_{SDATAOTR}$	SDATA Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	-53.6%	-63.5%	Fail
6	t_D	SDATA Output Valid Time	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	---	48997.2%	Fail
7	t_S	SDATA Setup Time	1.000 ns	---	26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	2569.4%	---	Pass
8	t_H	SDATA Hold Time	5.000 ns	---	43.207 ns	195.261 ns	5.299 us	790.518 ns	114	764.1%	---	Pass
9	V_L	Low-Level Voltage	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340	---	-21.2%	Pass
10	V_H	High-Level Voltage	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	108.1%	105.5%	Fail

f_{SCLK} - Test Result: Pass
Description: SCLK Frequency

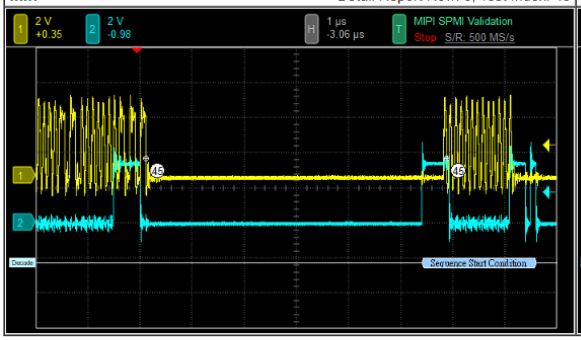
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	441.6%	-58.9%

Histogram

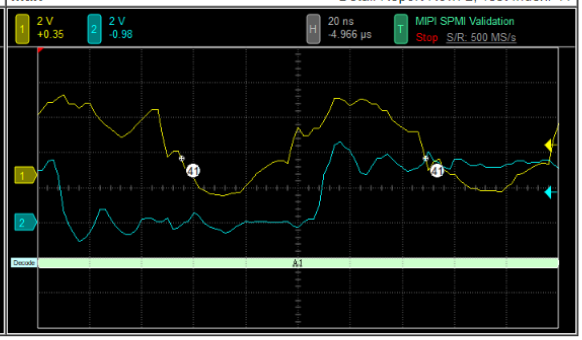


Value Range	Occurance Count
173.325 kHz ~ 1.225 MHz	8
1.225 MHz ~ 2.276 MHz	1
2.276 MHz ~ 3.327 MHz	0
3.327 MHz ~ 4.378 MHz	0
4.378 MHz ~ 5.429 MHz	19
5.429 MHz ~ 6.481 MHz	15
6.481 MHz ~ 7.532 MHz	5
7.532 MHz ~ 8.583 MHz	0
8.583 MHz ~ 9.634 MHz	150
9.634 MHz ~ 10.686 MHz	229

Min Detail Report Row: 3, Test Index: 45

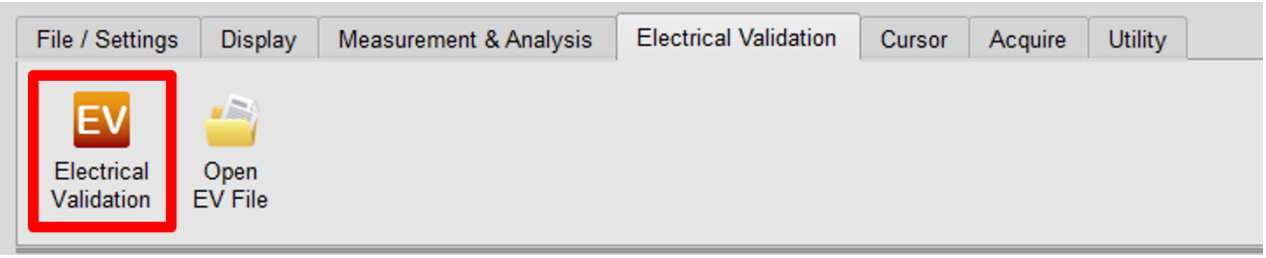


Max Detail Report Row: 2, Test Index: 41



PDM 电气特性验证解决方案

■ 简介：



使用示波器执行 PDM（Pulse Density Modulation）电气特性验证，以确保其信号符合既定电气标准规格。在经过长时间持续运行测试后，可以确认待测信号的电气特性是否满足标准要求。

PDM 协议的电气特性检测通常分为两大类：

- 垂直属性（电压）
- 水平属性（时间 / 相位）

因此，使用此功能时，必须先设置所选的协议与测试规范，并透过重复测试来取得电气特性报告。测试项目会根据 PDM 传输速率而有所不同。

常用 PDM 规格中的部分电气特性项目参数：

DIGITAL AUDIO INTERFACE					
PDM_CLK High Frequency Range	f_{CLKH}		5.28	8.64	MHz
PDM_CLK Low Frequency Range	f_{CLKL}		1.84	4.32	MHz
PDM_CLK High Time	t_{PDM_CLKH}		40		ns
PDM_CLK Low Time	t_{PDM_CLKL}		40		ns

常用 PDM 验证报告内容：

Overview | Detail | PDM

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f_{CLK}	Clock freq...	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass
2	t_{LOW}	Low Perio...	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass
3	t_{HIGH}	High Perio...	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass
4	t_{CL}	Rise time ...	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass
5	t_{FCL}	Fall time o...	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass
6	t_{DD}	Delay time...	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass
7	t_{RDV}	Delay time...	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass
8	t_{DD}	Delay time...	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass
9	t_{RDV}	Delay time...	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass

电气特性验证_软件画面：

1. 频率：时钟频率（Clock Speed）
2. 时序参数：建立时间（Set-up Time）、保持时间（Hold Time）、上升时间（Rise Time）、下降时间（Fall Time）与时钟拉伸（Clock Stretching）时间限制
3. 电压参数：V_IL（输入低电位）、V_IH（输入高电位）等

拉伸:

Symbol	**Electrical Parameter**
f_{SCL}	PDM_CLK Frequency Range

时间:

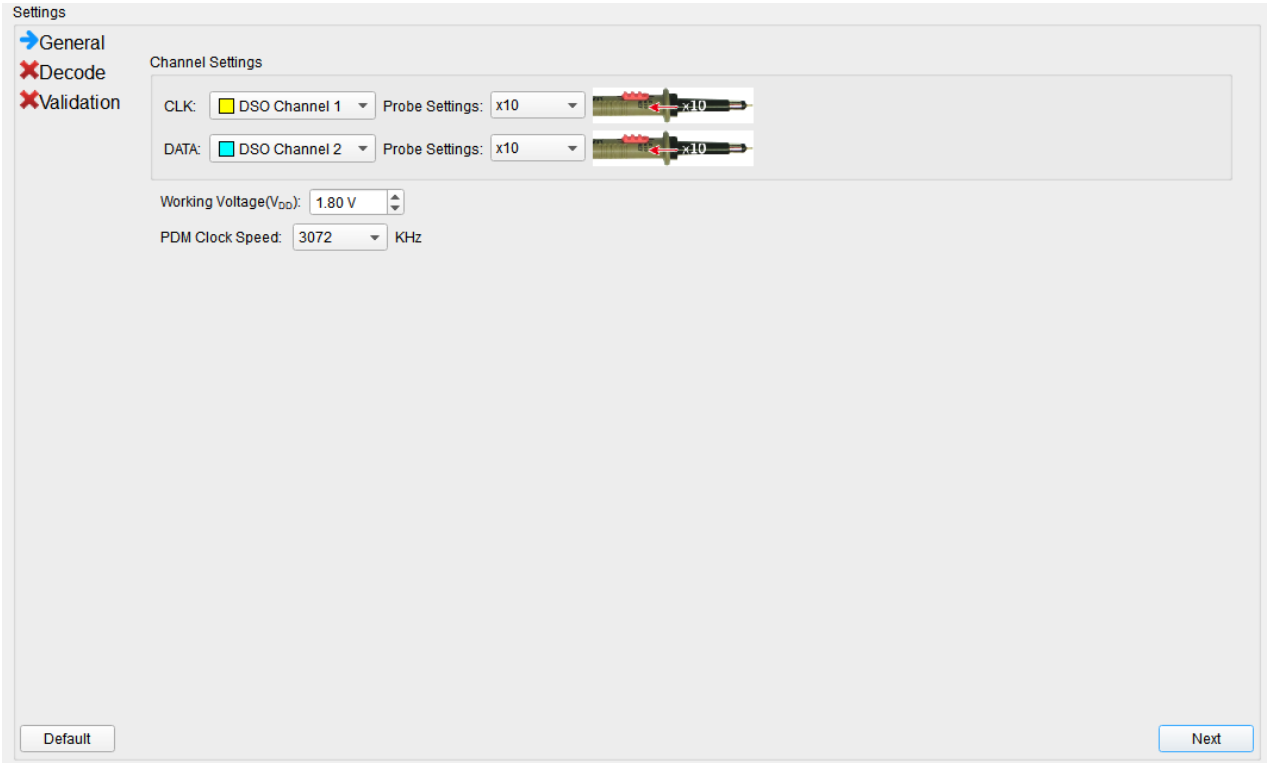
Symbol	**Electrical Parameter**
t_{LOW}	Low Period of the Clock
t_{HIGH}	High Period of the Clock
t_{rCL}	Rise time of Clock signal
$t\text{-}_{fCL}$	Fall time of Clock signal
t_{rDD}	Delay time from Clock edge to Data Rise driven
t_{fDD}	Delay time from Clock edge to Data Fall driven
t_{rDV}	Delay time from Clock edge to Data Rise valid
t_{fDV}	Delay time from Clock edge to Data Fall valid

电压:

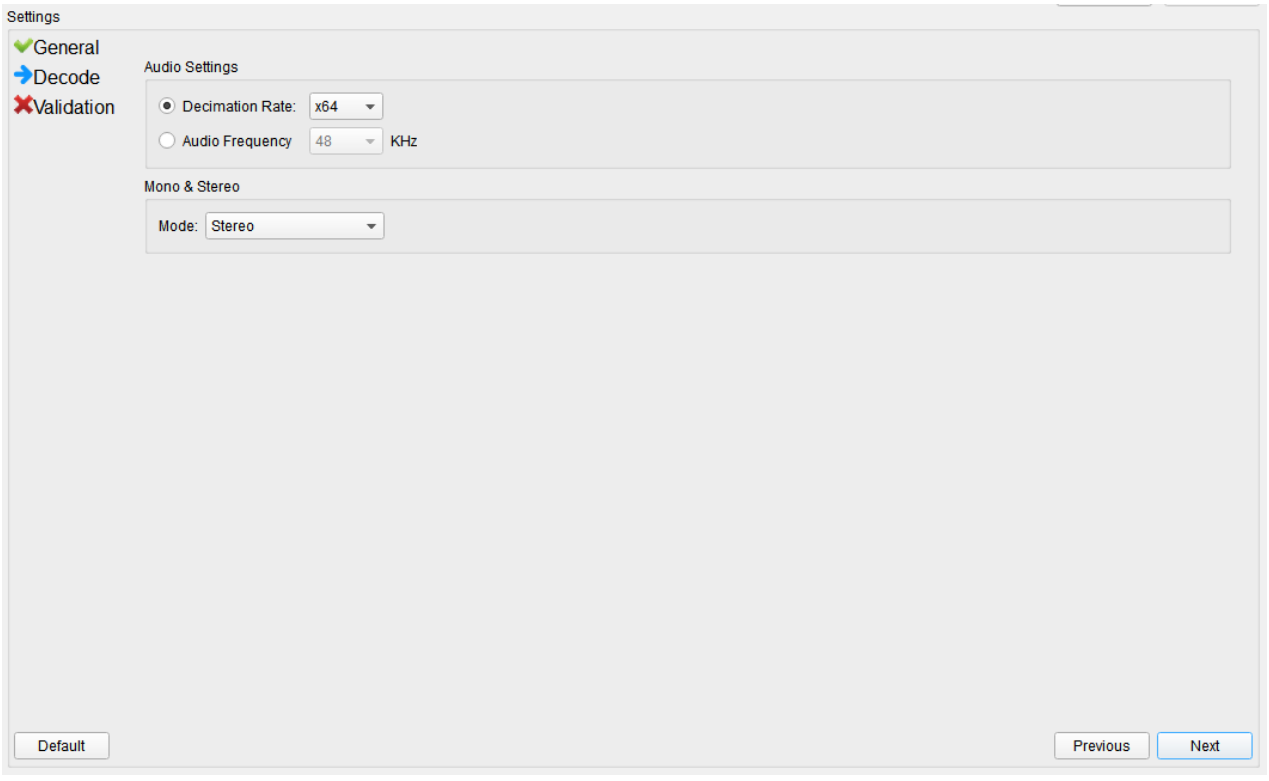
Symbol	**Electrical Parameter**
V_{ClkLow}	Low-level Input voltage for clock
$V_{ClkHigh}$	High-level Input voltage for clock
$V_{DataLow}$	Low-level Input voltage for data
$V_{DataHigh}$	High-level Input voltage for data

PDM 电气特性验证设置

1. 一般设置： 设置通道来源、工作电压与传输速率。



2. 解码设置： 设置 PDM 解码参数



3. 验证参数设置：频率、时序与电压限制条件

Settings

General
Decode
Validation

Customized EV Parameter:

Frequency

	Name	Description	Min	Max
1	f_{CLK}	Clock frequency	0 kHz	3.072 MHz

Time

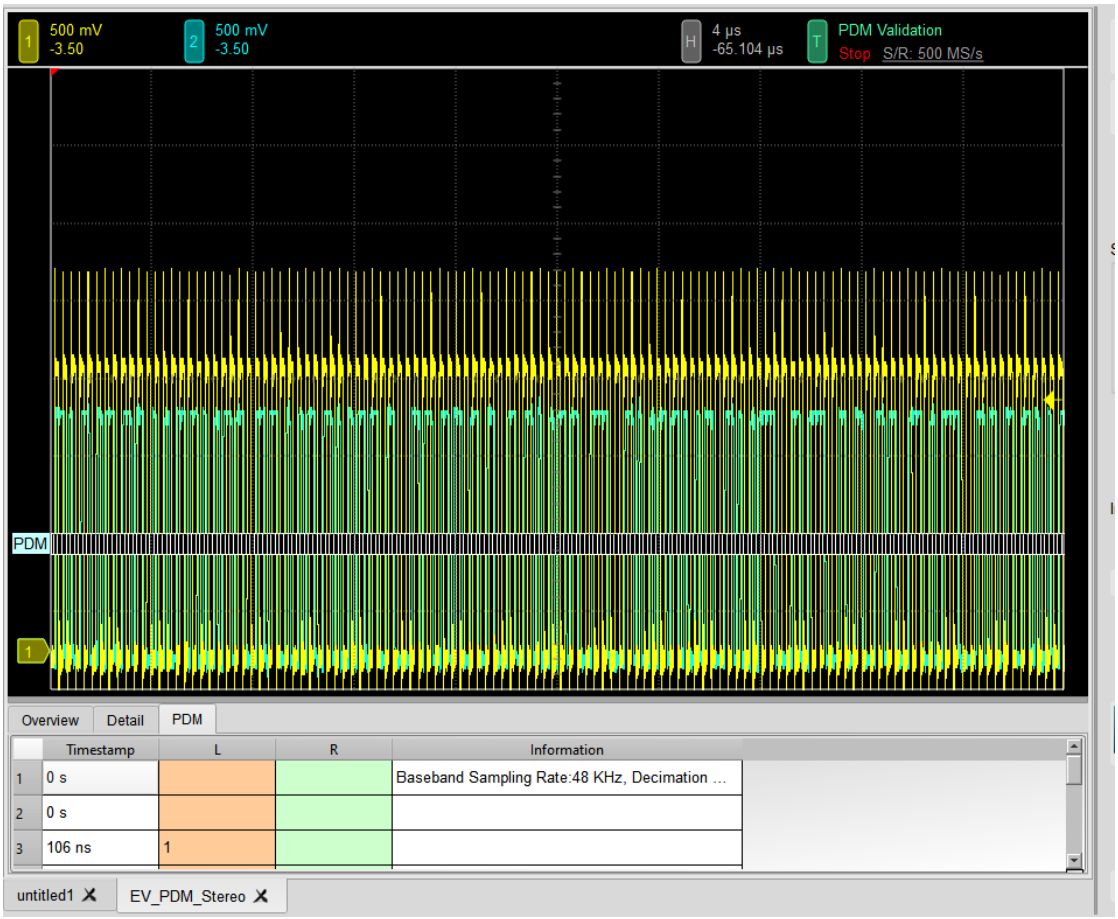
	Name	Description	Min	Max
1	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns
2	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns
3	t_{rCL}	Rise time of CLK signal	X	13 ns
4	t_{fCL}	Fall time of CLK signal	X	13 ns
5	t_{rDD}	Delay time from Clk edge to Data Rise driven	40 ns	80 ns
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40 ns	80 ns
7	t_{rDV}	Delay time from Clk edge to Data Rise Valid	X	100 ns
8	t_{fDV}	Delay time from Clk edge to Data Fall Valid	X	100 ns

Voltage

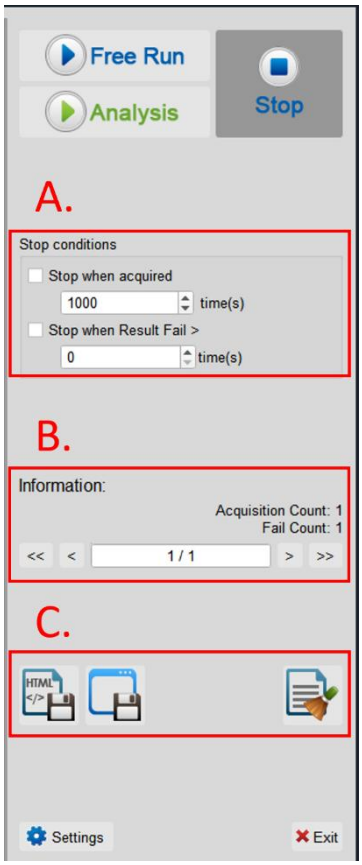
	Name	Description	Min	Max
1	V_{ClkLow}	Low-level input voltage for clock	-0.5 V	0.54 V
2	$V_{ClkHigh}$	High-level input voltage for clock	1.26 V	2.3 V
3	$V_{DataLow}$	Low-level input voltage for Data	-0.5 V	0.54 V
4	$V_{DataHigh}$	High-level input voltage for Data	1.26 V	2.3 V

Default | Advance | Previous | Apply

4. 电气特性验证_软件画面



5. 控制面板



A. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

B. 信息：

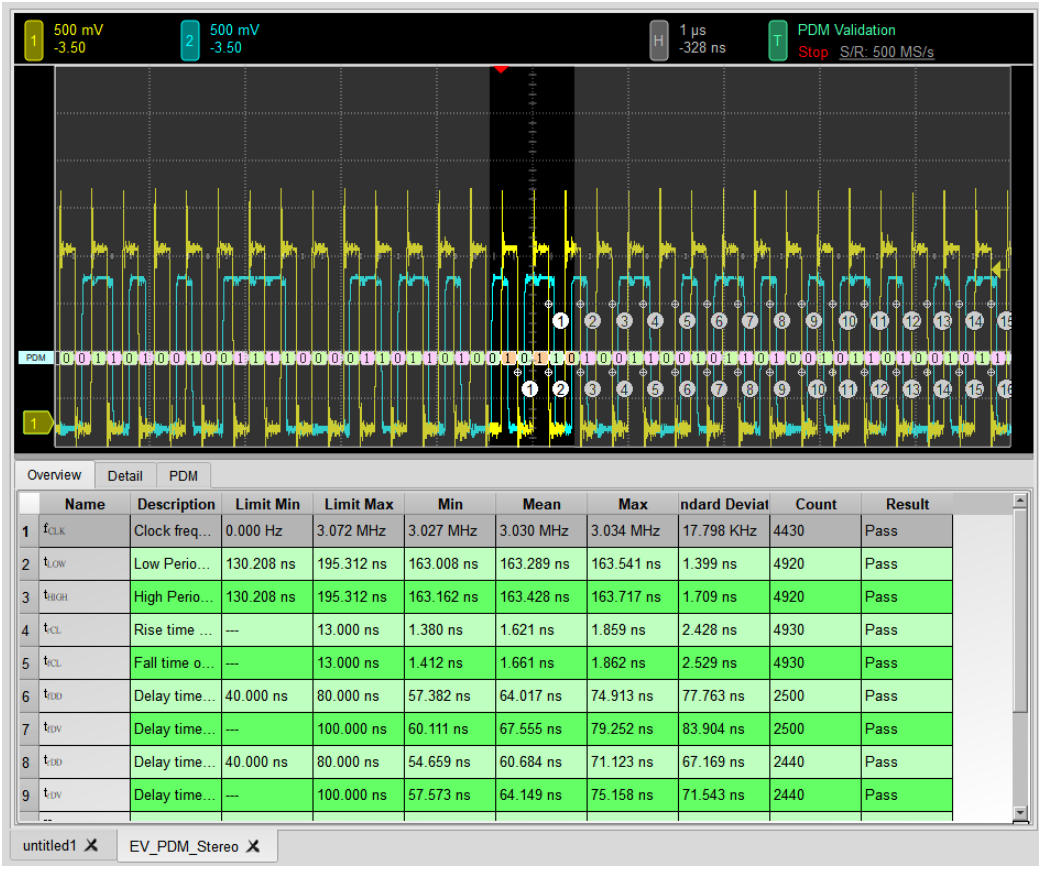
选择查看波形

C. 储存档案：

储存为 HTML 格式

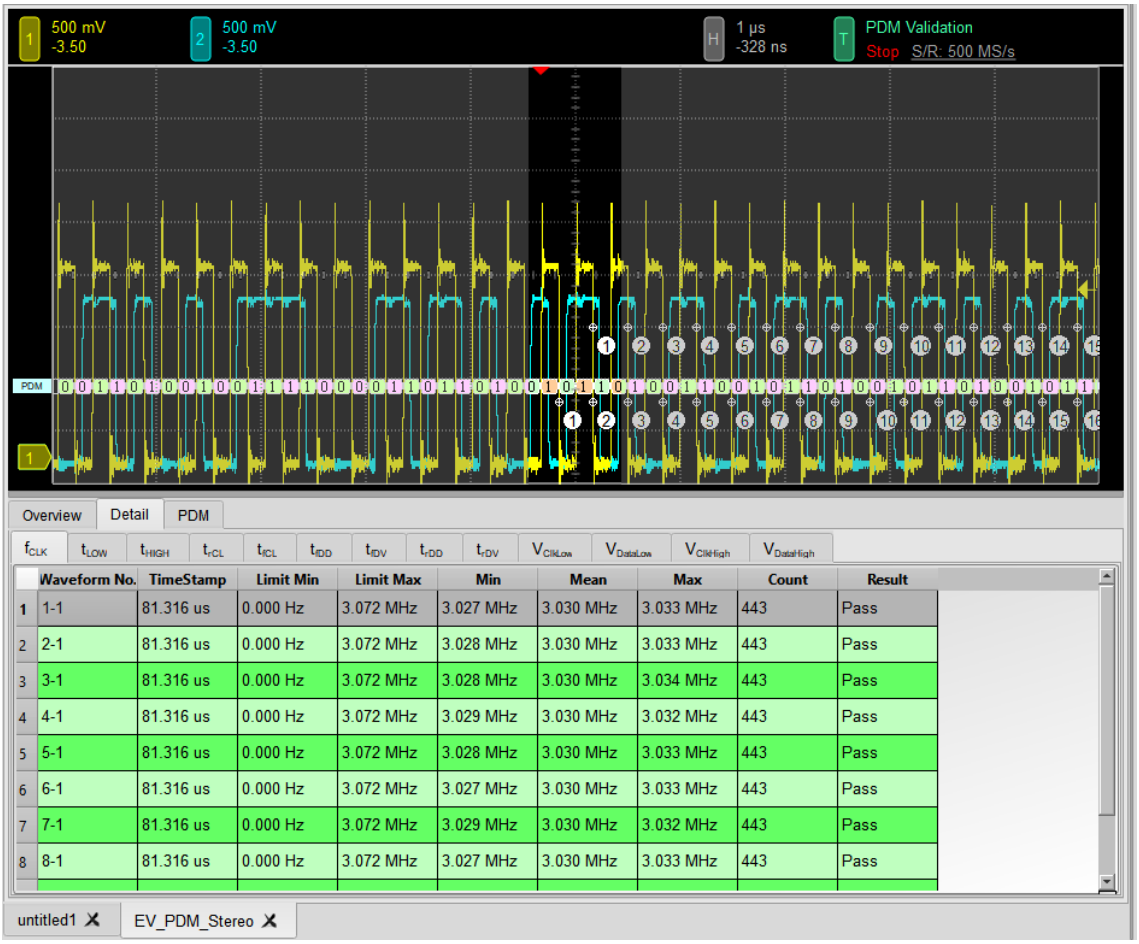
储存为 .MOW（Acute软件专用格式）

6. 概览报告



	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	t_{CLK}	Clock freq...	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass
2	t_{LOW}	Low Perio...	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass
3	t_{HIGH}	High Perio...	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass
4	t_{CL}	Rise time ...	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass
5	t_{CL}	Fall time o...	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass
6	t_{DD}	Delay time...	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass
7	t_{DV}	Delay time...	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass
8	t_{DD}	Delay time...	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass
9	t_{DV}	Delay time...	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass

7. 详细报告



	Waveform No.	TimeStamp	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass
2	2-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass
3	3-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.034 MHz	443	Pass
4	4-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass
5	5-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass
6	6-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass
7	7-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass
8	8-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass

8. 波形和参考点

Waveform No.	TimeStamp	Limit Min	Limit Max	Min
1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz

	Time	Δ Time	Volt	Δ Volt	Result
1	(16.439 µs, 16.769 µs)	330.000 ns	(540 mV, 1.26 V)	720 mV	Pass
2	(16.769 µs, 17.099 µs)	330.022 ns	(540 mV, 1.26 V)	720 mV	Pass
3	(17.099 µs, 17.429 µs)	329.944 ns	(540 mV, 1.26 V)	720 mV	Pass
4	(17.429 µs, 17.759 µs)	330.069 ns	(540 mV, 1.26 V)	720 mV	Pass
5	(17.759 µs, 18.089 µs)	330.059 ns	(540 mV, 1.26 V)	720 mV	Pass
6	(18.089 µs, 18.419 µs)	329.840 ns	(540 mV, 1.26 V)	720 mV	Pass
7	(18.419 µs, 18.749 µs)	330.122 ns	(540 mV, 1.26 V)	720 mV	Pass
8	(18.749 µs, 19.079 µs)	330.000 ns	(540 mV, 1.26 V)	720 mV	Pass
9	(19.079 µs, 19.409 µs)	329.943 ns	(540 mV, 1.26 V)	720 mV	Pass

9. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

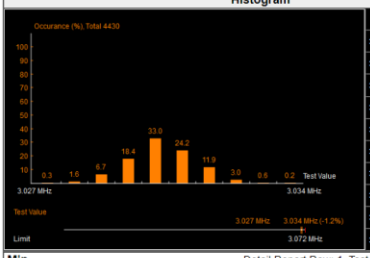
Total: 13
Pass: 13
Fail: 0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{CLK}	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%	✓Pass
2	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	t_{rCL}	Rise time of CLK signal	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	---	-85.7%	✓Pass
5	t_{fCL}	Fall time of CLK signal	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	---	-85.7%	✓Pass
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	t_{fDV}	Delay time from Clk edge to Data Fall Valid	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	---	-20.7%	✓Pass
8	t_{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	✓Pass
9	t_{rDV}	Delay time from Clk edge to Data Rise Valid	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	---	-24.8%	✓Pass
10	V_{ClkLow}	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	$V_{DataLow}$	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	$V_{ClkHigh}$	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	✓Pass
13	$V_{DataHigh}$	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

f_{CLK} - Test Result: Pass
Description: Clock frequency

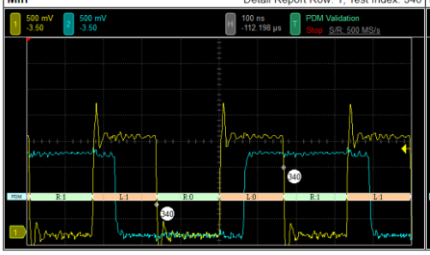
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%

Histogram

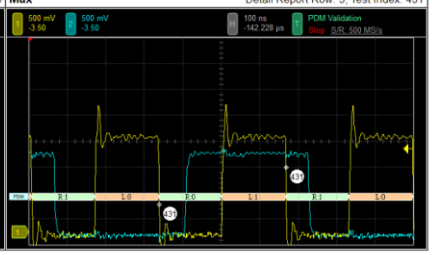


Value Range	Occurance Count
3.027 MHz ~ 3.028 MHz	13
3.028 MHz ~ 3.028 MHz	70
3.028 MHz ~ 3.029 MHz	298
3.029 MHz ~ 3.03 MHz	813
3.03 MHz ~ 3.03 MHz	1464
3.03 MHz ~ 3.031 MHz	1073
3.031 MHz ~ 3.032 MHz	529
3.032 MHz ~ 3.032 MHz	135
3.032 MHz ~ 3.033 MHz	27
3.033 MHz ~ 3.034 MHz	8

Min — Detail Report Row: 1, Test Index: 340

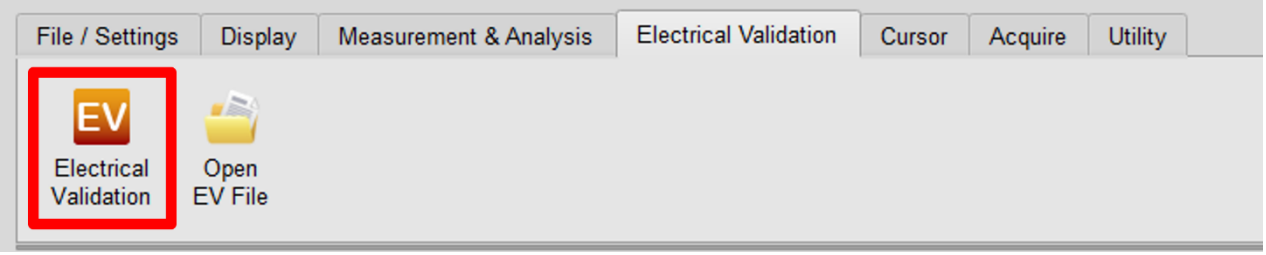


Max — Detail Report Row: 3, Test Index: 431



SMBus 电气特性验证解决方案

简介:



使用示波器执行 SMBus（System Management Bus）电气特性验证，以确保其信号符合所定义的电气特性规格。在经过长时间持续运行测试后，可确认待测信号的电气特性是否达标。

SMBus 协议的电气特性检测方式与 I2C 类似，通常分为两大类：

- 垂直属性（电压）
- 水平属性（时间 / 相位）

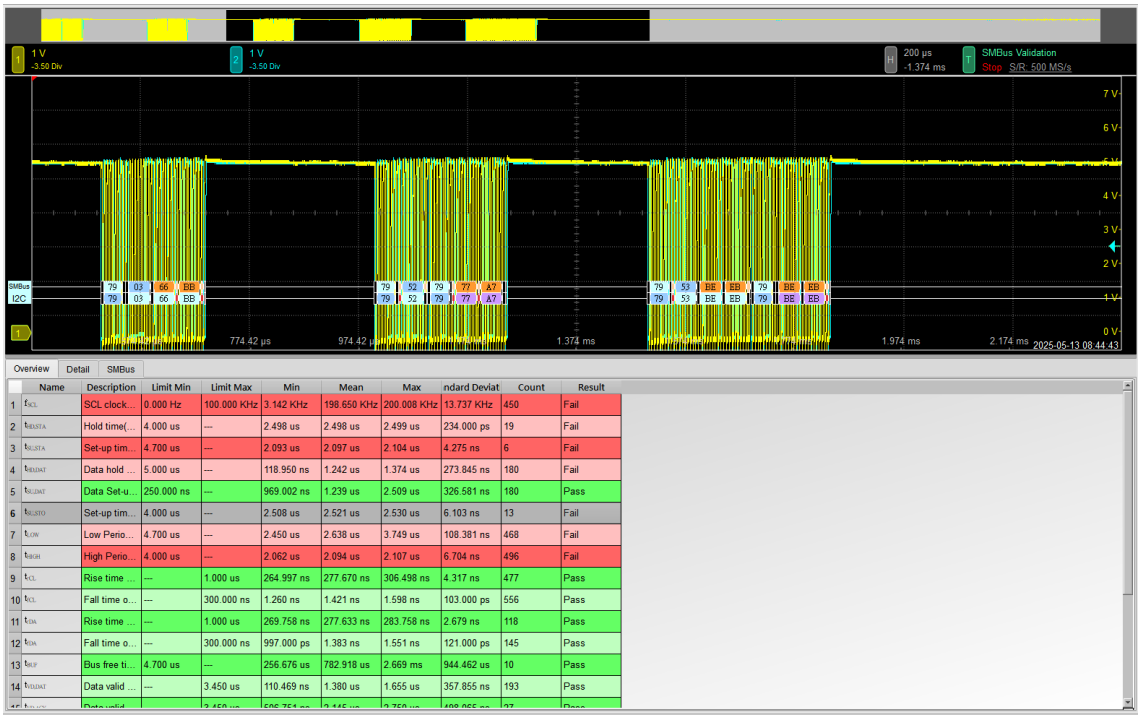
因此，使用此功能前，须先设置所选协议与规格，并透过反复测试以取得电气特性测试报告。测试项目会根据 SMBus 的传输速率而有所不同。

SMBus 验证报告内容：

Overview | Detail | SMBus

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f_{SCL}	SCL clock...	0.000 Hz	100.000 KHz	3.142 KHz	198.650 KHz	200.008 KHz	13.737 KHz	450	Fail
2	$t_{HD;STA}$	Hold time(...	4.000 us	---	2.498 us	2.498 us	2.499 us	234.000 ps	19	Fail
3	$t_{SU;STA}$	Set-up tim...	4.700 us	---	2.093 us	2.097 us	2.104 us	4.275 ns	6	Fail
4	$t_{HD;DAT}$	Data hold ...	5.000 us	---	118.950 ns	1.242 us	1.374 us	273.845 ns	180	Fail
5	$t_{SU;DAT}$	Data Set-u...	250.000 ns	---	969.002 ns	1.239 us	2.509 us	326.581 ns	180	Pass
6	$t_{SU;STO}$	Set-up tim...	4.000 us	---	2.508 us	2.521 us	2.530 us	6.103 ns	13	Fail
7	t_{LOW}	Low Perio...	4.700 us	---	2.450 us	2.638 us	3.749 us	108.381 ns	468	Fail
8	t_{HIGH}	High Perio...	4.000 us	---	2.062 us	2.094 us	2.107 us	6.704 ns	496	Fail
9	t_{rCL}	Rise time ...	---	1.000 us	264.997 ns	277.670 ns	306.498 ns	4.317 ns	477	Pass
10	t_{fCL}	Fall time o...	---	300.000 ns	1.260 ns	1.421 ns	1.598 ns	103.000 ps	556	Pass
11	t_{rDA}	Rise time ...	---	1.000 us	269.758 ns	277.633 ns	283.758 ns	2.679 ns	118	Pass
12	t_{fDA}	Fall time o...	---	300.000 ns	997.000 ps	1.383 ns	1.551 ns	121.000 ps	145	Pass
13	t_{BUF}	Bus free ti...	4.700 us	---	256.676 us	782.918 us	2.669 ms	944.462 us	10	Pass
14	$t_{VD;DAT}$	Data valid ...	---	3.450 us	110.469 ns	1.380 us	1.655 us	357.855 ns	193	Pass

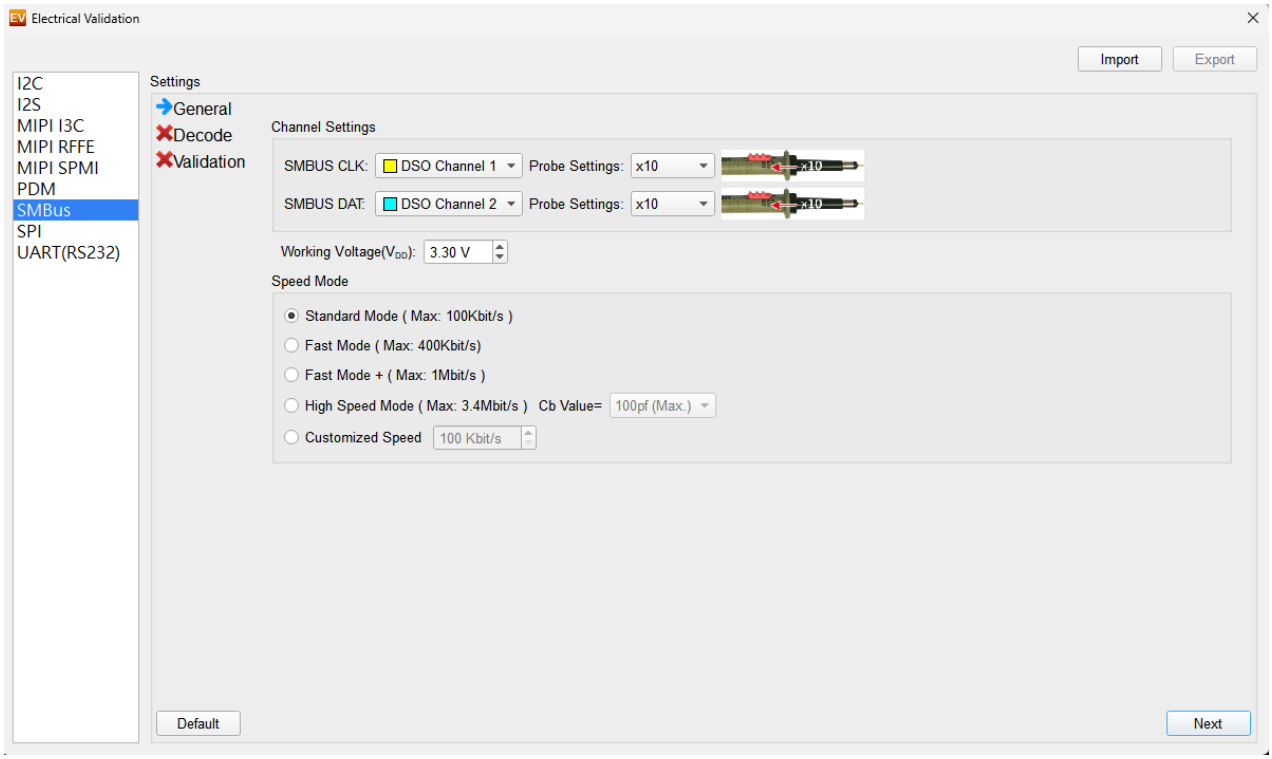
电气特性验证_软件画面：



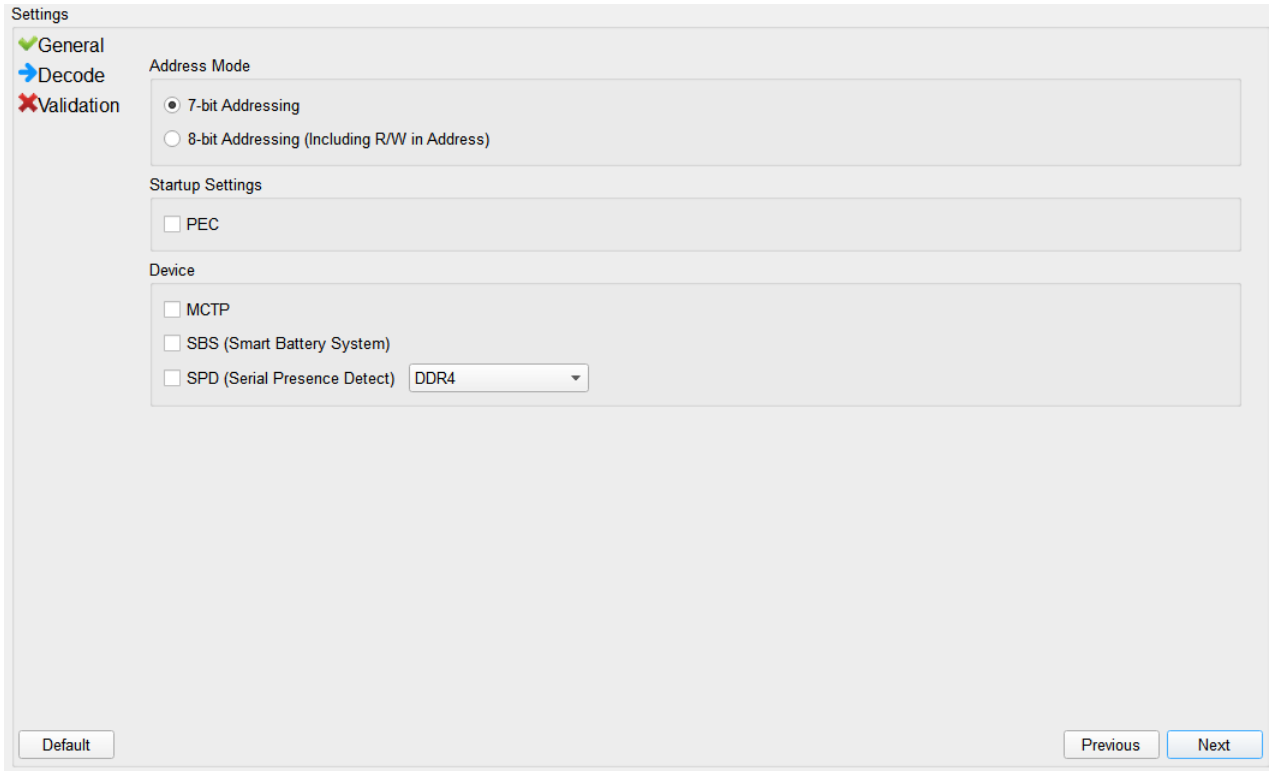
1. 不同的传输速率模式，包括 Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
2. 频率：频率速度
3. 时序参数：建立时间（Set-up Time）、保持时间（Hold Time）、上升时间（Rise Time）、下降时间（Fall Time）与时钟拉伸（Clock Stretching）时间限制
4. 电压参数：V_IL（输入低电位）、V_IH（输入高电位）等

SMBus 电气特性验证设置

1. 一般设置：设置通道来源、工作电压与传输速率



2. 解码设置：设置 SMBus 解码参数



3. 验证项目设置：包含频率、时序与电压限制条件

Settings

- General
- Decode
- Validation

Customized EV Parameter:

Frequency

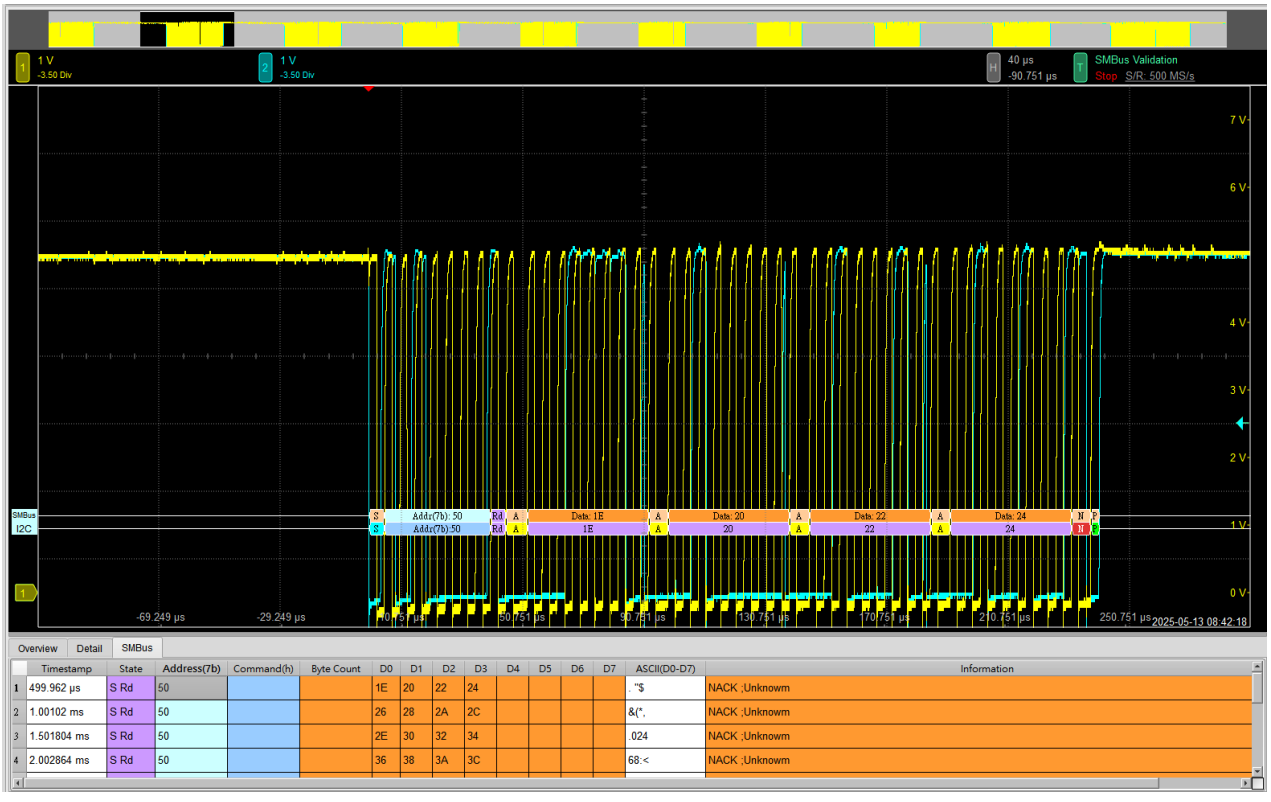
	Name	Description	Min	Max
1	☑ f_{SCL}	SCL clock frequency	0 kHz	100 kHz

Time

	Name	Description	Min	Max
1	☑ $t_{HD,STA}$	Hold time(repeated) START condition	4 us	X
2	☑ $t_{SU,STA}$	Set-up time for a repeated START condition	4.7 us	X
3	☑ $t_{HD,DAT}$	Data hold time	5 us	X
4	☑ $t_{SU,DAT}$	Data Set-up time	250 ns	X
5	☑ $t_{SU,STO}$	Set-up time for STOP condition	4 us	X
6	☑ t_{LOW}	Low Period of the SCL Clock	4.7 us	X
7	☑ t_{HIGH}	High Period of the SCL Clock	4 us	X
8	☑ t_{rCL}	Rise time of SCL signal	X	1 us
9	☑ t_{fCL}	Fall time of SCL signal	X	300 ns
10	☑ t_{rDA}	Rise time of SDA signal	X	1 us
11	☑ t_{fDA}	Fall time of SDA signal	X	300 ns

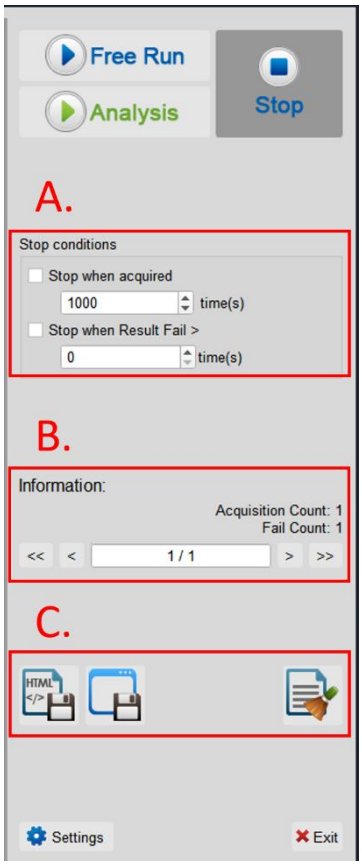
Default | Advance | Previous | Apply

4. 电气特性验证_软件画面



	Timestamp	State	Address(7b)	Command(h)	Byte Count	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
1	499.962 µs	S Rd	50			1E	20	22	24					.'$	NACK ;Unknown
2	1.00102 ms	S Rd	50			26	28	2A	2C					&(*,	NACK ;Unknown
3	1.501804 ms	S Rd	50			2E	30	32	34					.024	NACK ;Unknown
4	2.002864 ms	S Rd	50			36	38	3A	3C					68:<	NACK ;Unknown

5. 控制面板



A. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

B. 信息：

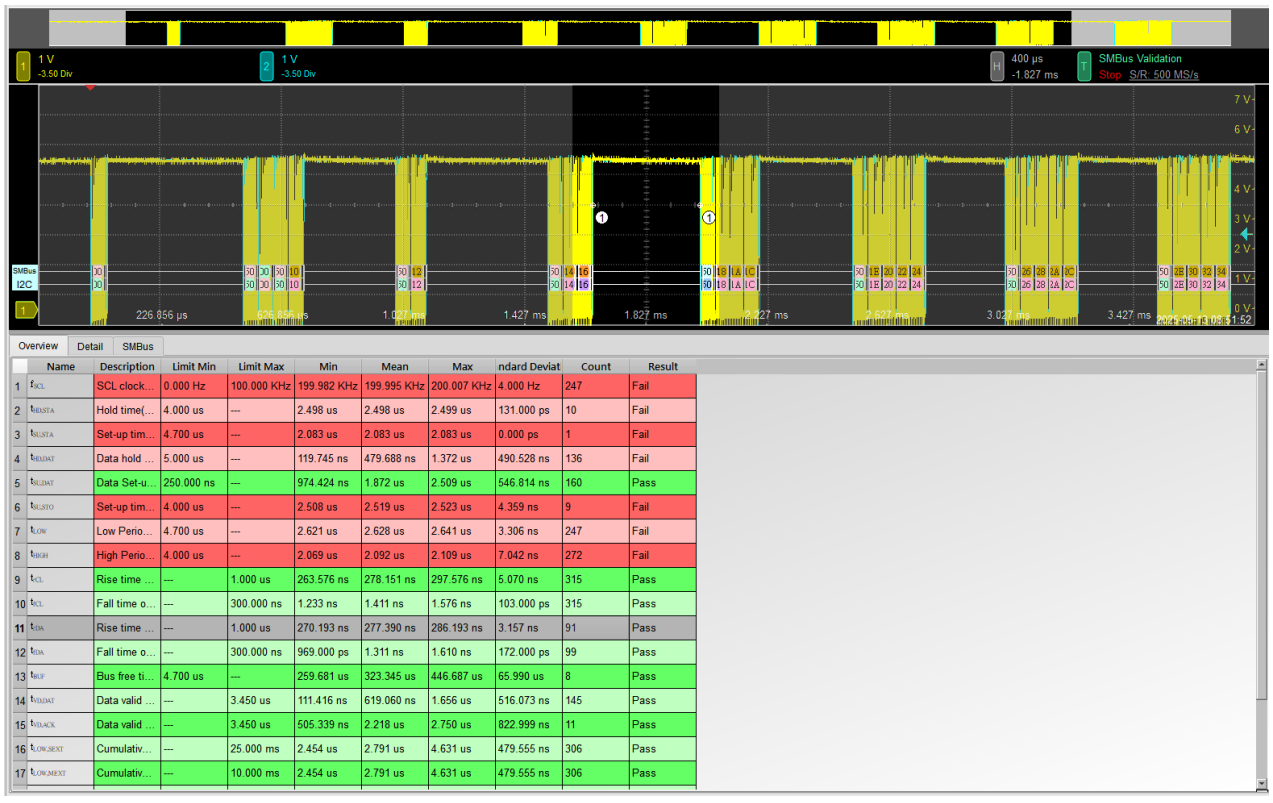
选择查看波形

C. 储存档案：

储存为 HTML 格式

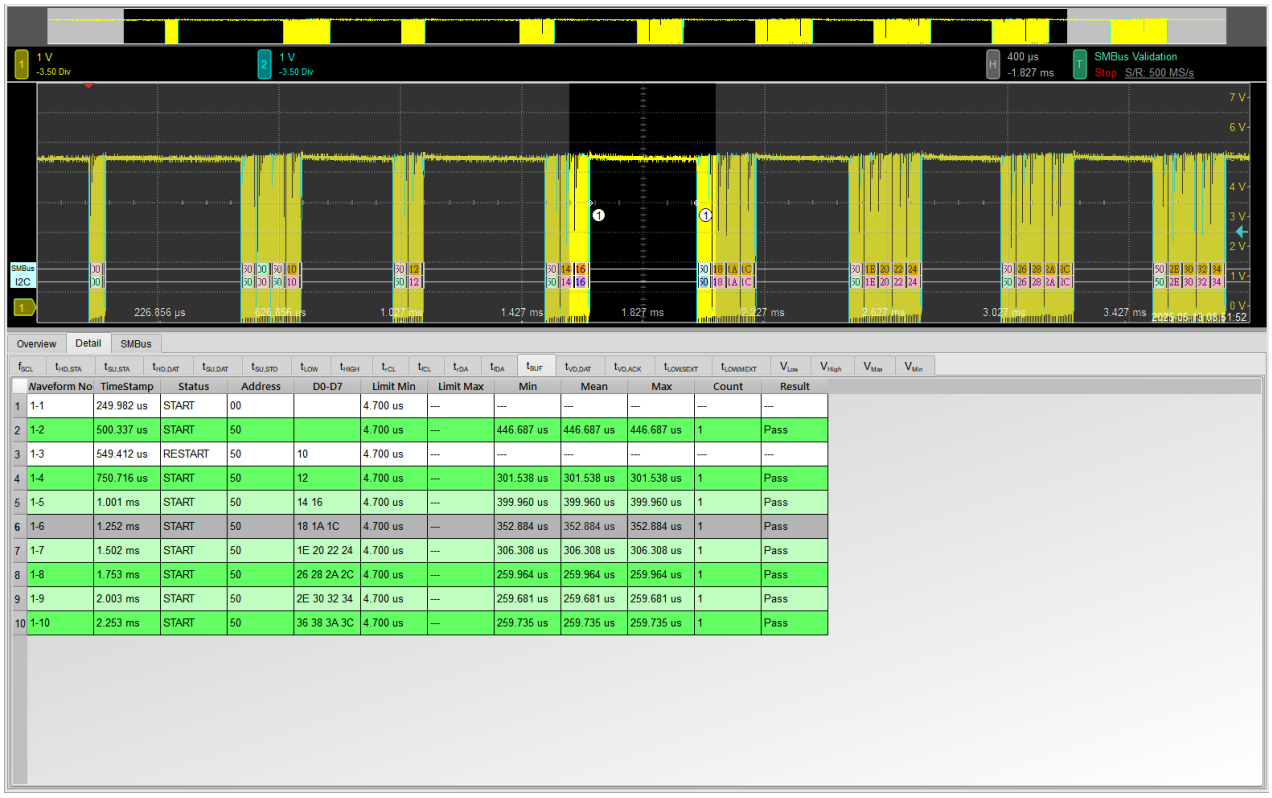
储存为 .MOW（Acute软件专用格式）

6. 概览报告



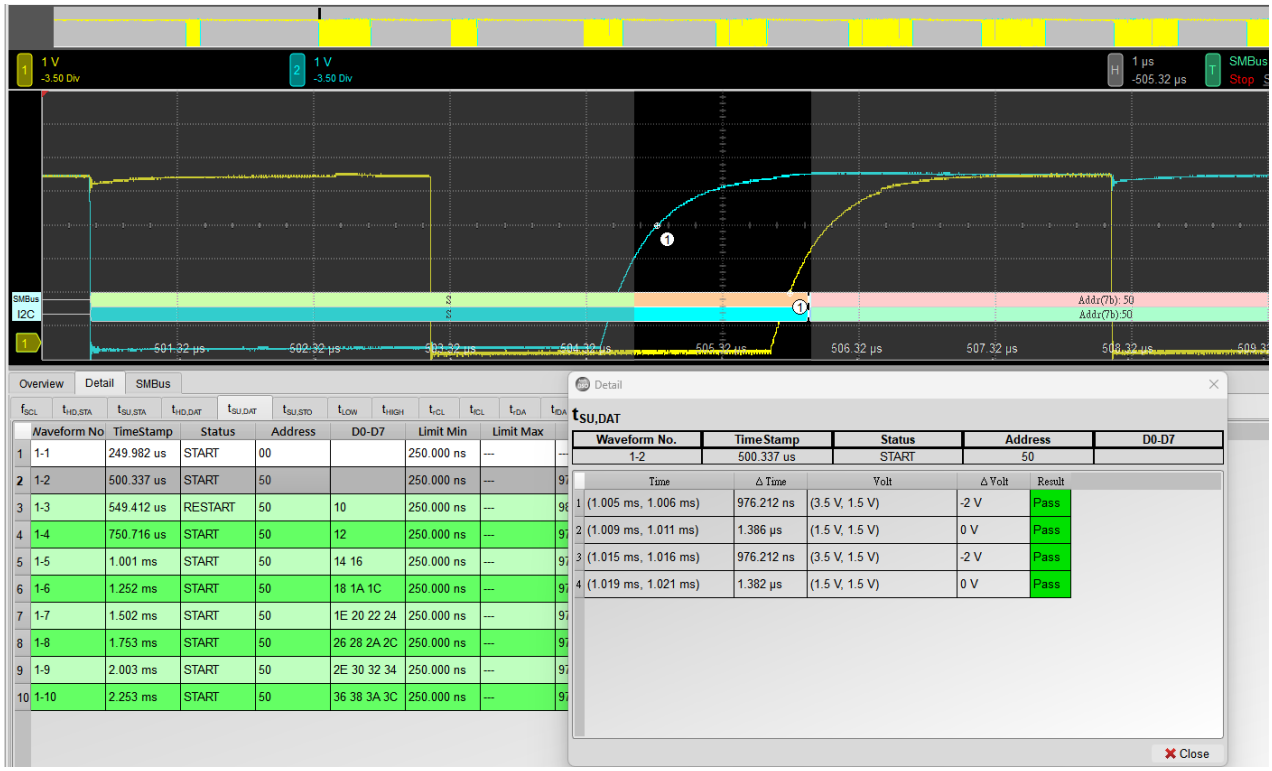
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f_{SCL}	SCL clock...	0.000 Hz	100.000 KHz	199.982 KHz	199.995 KHz	200.007 KHz	4.000 Hz	247	Fail
2	$t_{HD;STA}$	Hold time(...	4.000 us	---	2.498 us	2.498 us	2.499 us	131.000 ps	10	Fail
3	$t_{SU;STA}$	Set-up tim...	4.700 us	---	2.083 us	2.083 us	2.083 us	0.000 ps	1	Fail
4	$t_{HD;DAT}$	Data hold ...	5.000 us	---	119.745 ns	479.688 ns	1.372 us	490.528 ns	136	Fail
5	$t_{SU;DAT}$	Data Set-u...	250.000 ns	---	974.424 ns	1.872 us	2.509 us	546.814 ns	160	Pass
6	$t_{SU;STO}$	Set-up tim...	4.000 us	---	2.508 us	2.519 us	2.523 us	4.359 ns	9	Fail
7	t_{LOW}	Low Perio...	4.700 us	---	2.621 us	2.628 us	2.641 us	3.306 ns	247	Fail
8	t_{HIGH}	High Perio...	4.000 us	---	2.069 us	2.092 us	2.109 us	7.042 ns	272	Fail
9	t_{rCL}	Rise time ...	---	1.000 us	263.576 ns	278.151 ns	297.576 ns	5.070 ns	315	Pass
10	t_{fCL}	Fall time o...	---	300.000 ns	1.233 ns	1.411 ns	1.576 ns	103.000 ps	315	Pass
11	t_{rDA}	Rise time ...	---	1.000 us	270.193 ns	277.390 ns	286.193 ns	3.157 ns	91	Pass
12	t_{fDA}	Fall time o...	---	300.000 ns	969.000 ps	1.311 ns	1.610 ns	172.000 ps	99	Pass
13	t_{BUF}	Bus free ti...	4.700 us	---	259.681 us	323.345 us	446.687 us	65.990 us	8	Pass
14	$t_{VD;DAT}$	Data valid ...	---	3.450 us	111.416 ns	619.060 ns	1.656 us	516.073 ns	145	Pass
15	$t_{VD;ACK}$	Data valid ...	---	3.450 us	505.339 ns	2.218 us	2.750 us	822.999 ns	11	Pass
16	$t_{LOW;SEXT}$	Cumulativ...	---	25.000 ms	2.454 us	2.791 us	4.631 us	479.555 ns	306	Pass
17	$t_{LOW;MEXT}$	Cumulativ...	---	10.000 ms	2.454 us	2.791 us	4.631 us	479.555 ns	306	Pass

7. 详细报告



	Waveform No	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	249.982 us	START	00		4.700 us	---	---	---	---	---	---
2	1-2	500.337 us	START	50		4.700 us	---	446.687 us	446.687 us	446.687 us	1	Pass
3	1-3	549.412 us	RESTART	50	10	4.700 us	---	---	---	---	---	---
4	1-4	750.716 us	START	50	12	4.700 us	---	301.538 us	301.538 us	301.538 us	1	Pass
5	1-5	1.001 ms	START	50	14 16	4.700 us	---	399.960 us	399.960 us	399.960 us	1	Pass
6	1-6	1.252 ms	START	50	18 1A 1C	4.700 us	---	352.884 us	352.884 us	352.884 us	1	Pass
7	1-7	1.502 ms	START	50	1E 20 22 24	4.700 us	---	306.308 us	306.308 us	306.308 us	1	Pass
8	1-8	1.753 ms	START	50	26 28 2A 2C	4.700 us	---	259.964 us	259.964 us	259.964 us	1	Pass
9	1-9	2.003 ms	START	50	2E 30 32 34	4.700 us	---	259.681 us	259.681 us	259.681 us	1	Pass
10	1-10	2.253 ms	START	50	36 38 3A 3C	4.700 us	---	259.735 us	259.735 us	259.735 us	1	Pass

8. 波形和参考点



	Waveform No	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max
1	1-1	249.982 us	START	00		250.000 ns	---
2	1-2	500.337 us	START	50		250.000 ns	---
3	1-3	549.412 us	RESTART	50	10	250.000 ns	---
4	1-4	750.716 us	START	50	12	250.000 ns	---
5	1-5	1.001 ms	START	50	14 16	250.000 ns	---
6	1-6	1.252 ms	START	50	18 1A 1C	250.000 ns	---
7	1-7	1.502 ms	START	50	1E 20 22 24	250.000 ns	---
8	1-8	1.753 ms	START	50	26 28 2A 2C	250.000 ns	---
9	1-9	2.003 ms	START	50	2E 30 32 34	250.000 ns	---
10	1-10	2.253 ms	START	50	36 38 3A 3C	250.000 ns	---

Waveform No.	TimeStamp	Status	Address	D0-D7
1-2	500.337 us	START	50	

	Time	Δ Time	Volt	Δ Volt	Result
1	(1.005 ms, 1.006 ms)	976.212 ns	(3.5 V, 1.5 V)	-2 V	Pass
2	(1.009 ms, 1.011 ms)	1.386 µs	(1.5 V, 1.5 V)	0 V	Pass
3	(1.015 ms, 1.016 ms)	976.212 ns	(3.5 V, 1.5 V)	-2 V	Pass
4	(1.019 ms, 1.021 ms)	1.382 µs	(1.5 V, 1.5 V)	0 V	Pass

9. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

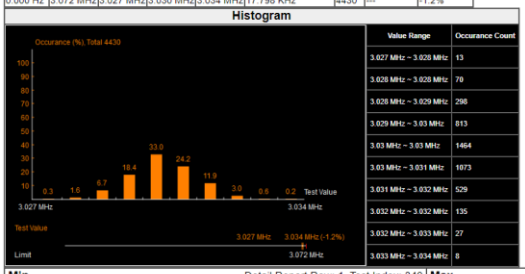
Total: 13
Pass: 13
Fail: 0

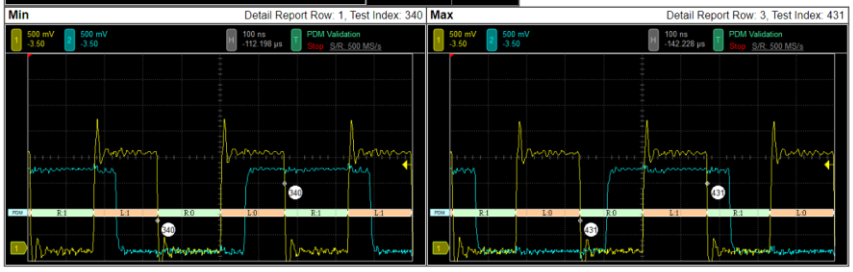
Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{CLK}	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%	✓Pass
2	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	t_{rCL}	Rise time of CLK signal	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	---	-85.7%	✓Pass
5	t_{fCL}	Fall time of CLK signal	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	---	-85.7%	✓Pass
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	t_{fDV}	Delay time from Clk edge to Data Fall Valid	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	---	-20.7%	✓Pass
8	t_{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	✓Pass
9	t_{rDV}	Delay time from Clk edge to Data Rise Valid	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	---	-24.8%	✓Pass
10	V_{ClkLow}	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	$V_{DataLow}$	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	$V_{ClkHigh}$	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	✓Pass
13	$V_{DataHigh}$	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

---

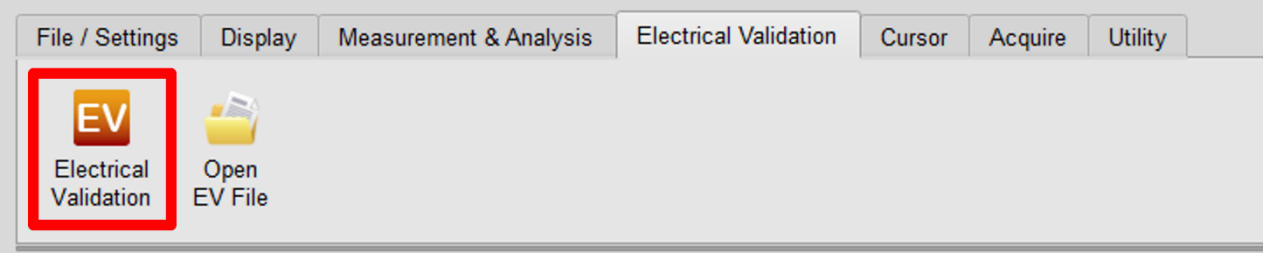
f_{CLK} - Test Result: Pass
Description: Clock frequency

Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%





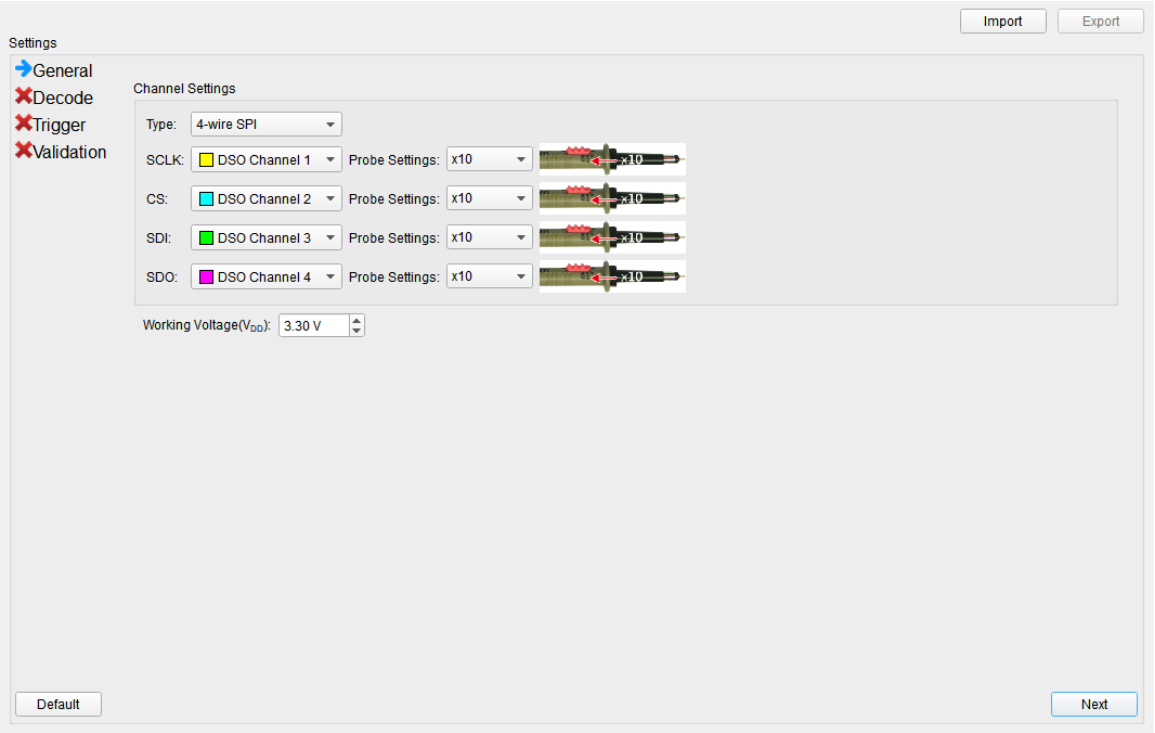
SPI 电气特性验证解决方案



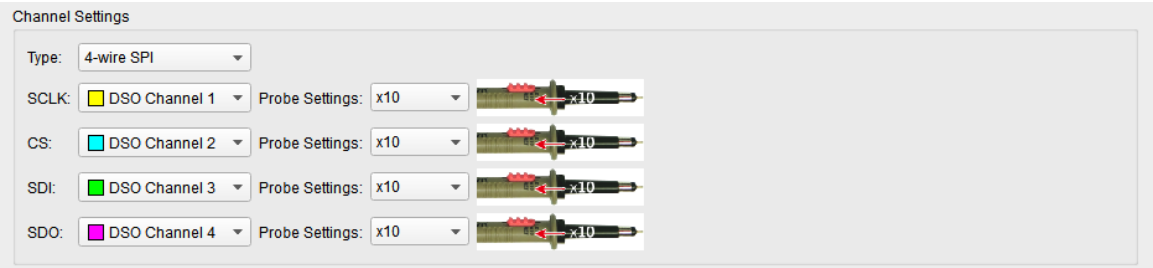
使用示波器执行 SPI（Serial Peripheral Interface）电气特性验证，以确保其信号符合所定义的电气规格。在经过长时间持续运行测试后，可确认待测信号的电气特性是否达标。

SPI 电气特性验证设置

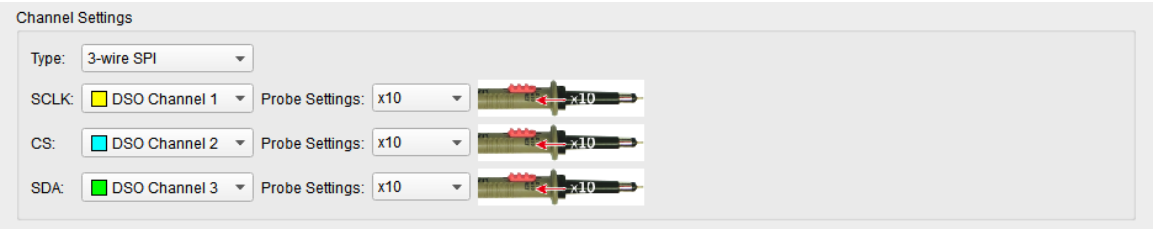
1. 一般设置：根据总线配置选择 SPI 类型（4-wire SPI 或 3-wire SPI）。



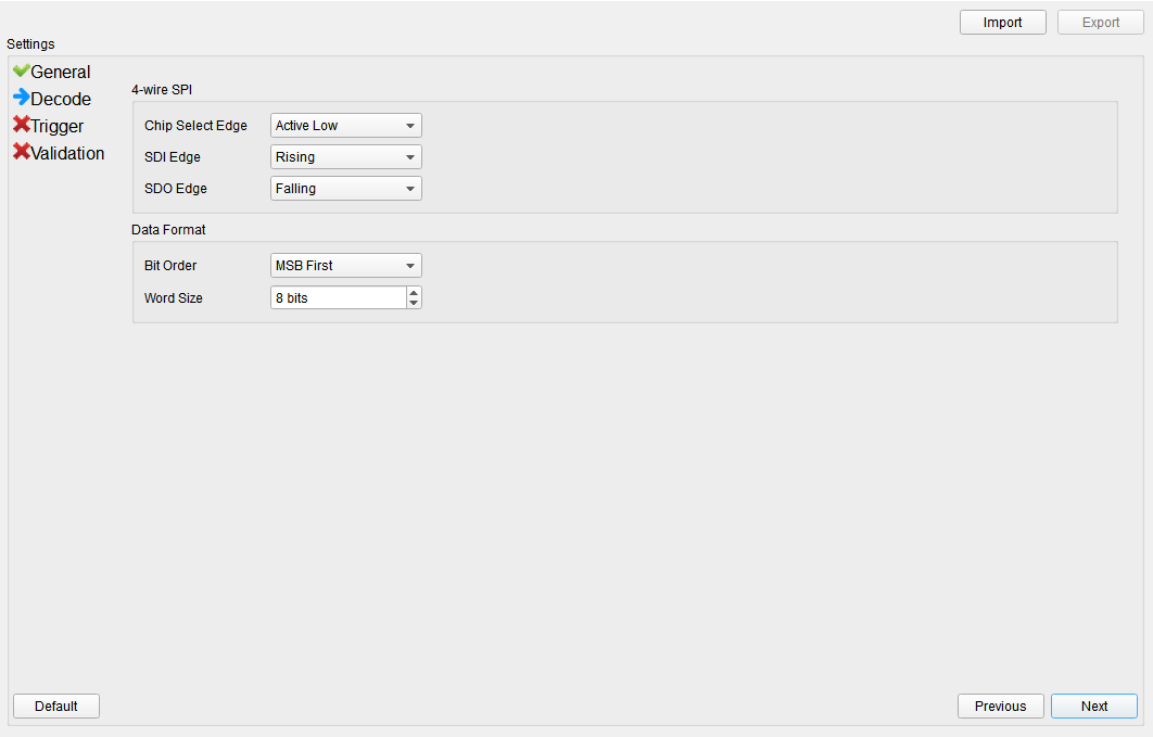
4-wire 设置：



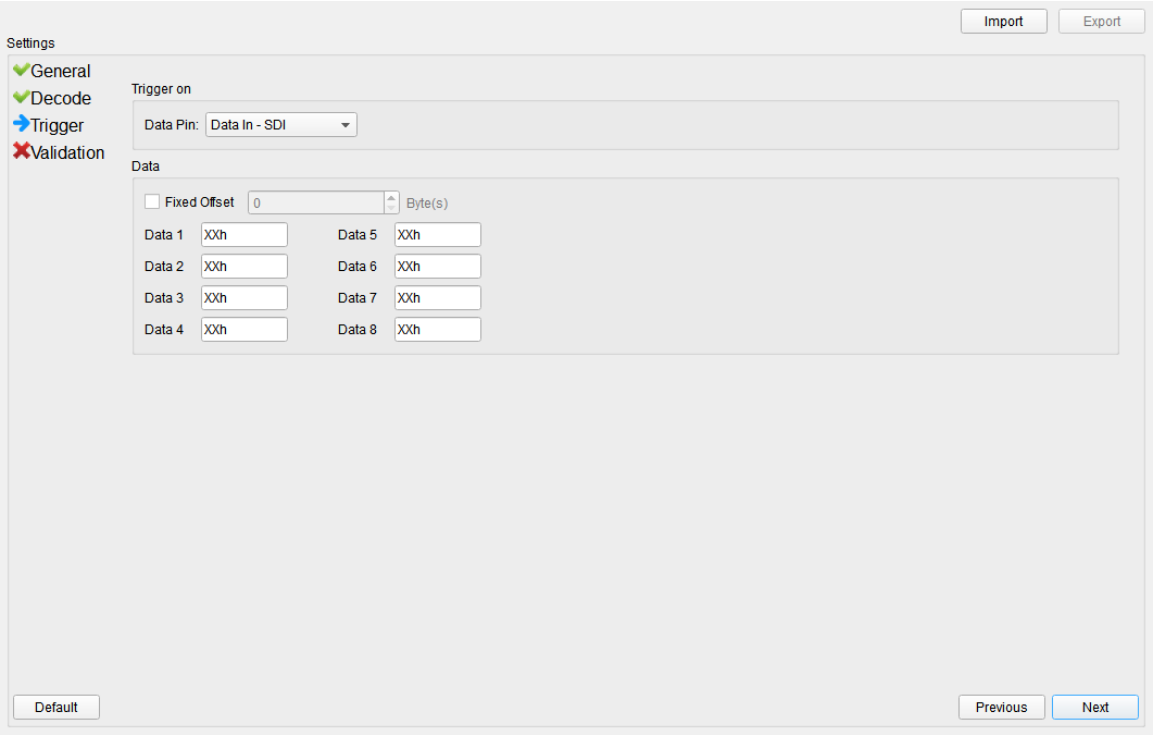
3-wire 设置：



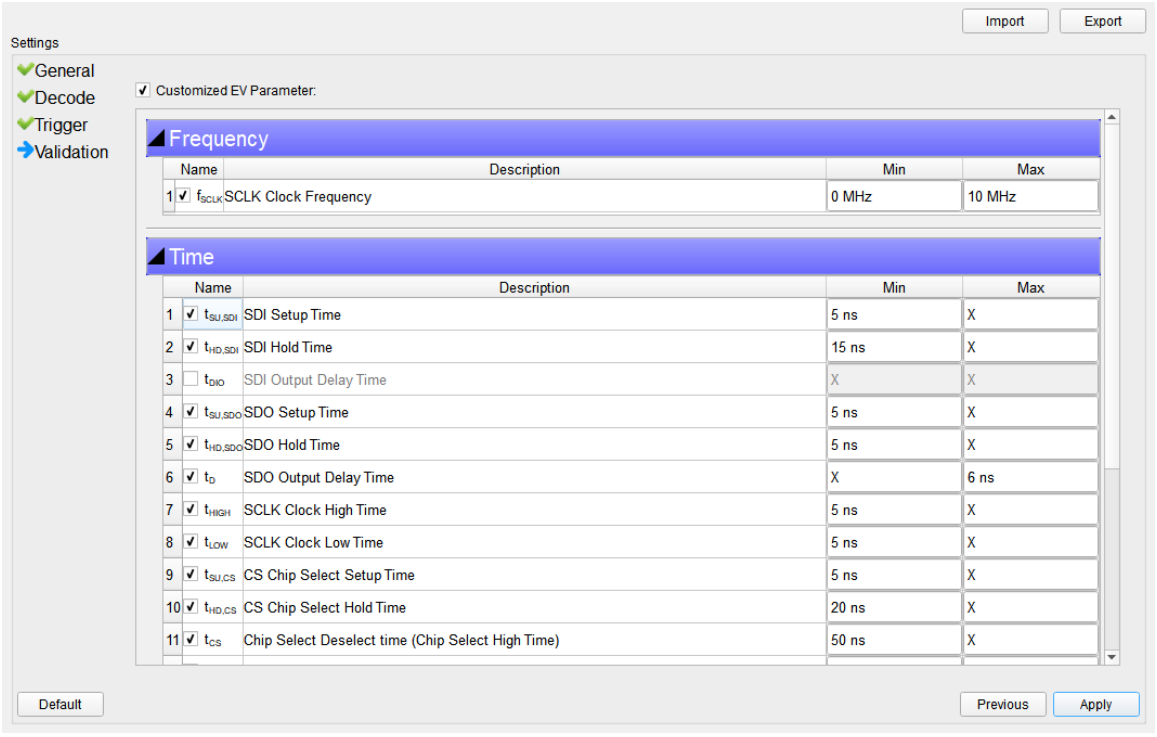
2. 解码设置： 设置 SPI 的数据格式以及各个通道的 Latching Edge。这里所设置的 SPI 数据格式会同时套用至解码与触发设置中。



3. 触发设置： 数据格式已在上一页设置完毕。本部分剩下的设置重点是数据地址与要触发的数据脚位。



4. 验证参数设置



由于 SPI 总线并未有行业标准的测量门限值，因此用户在进行验证时请自行定义合适的门限值。

本部分显示三项特性参数表，包括：

- 频率
- 时序参数
- 电压需求

所有支持的验证参数项目与说明如下：

SPI Frequency Requirements

Symbol	Electrical Parameter
f_{SCLK}	SCLK Clock Frequency

SPI Timing Requirements

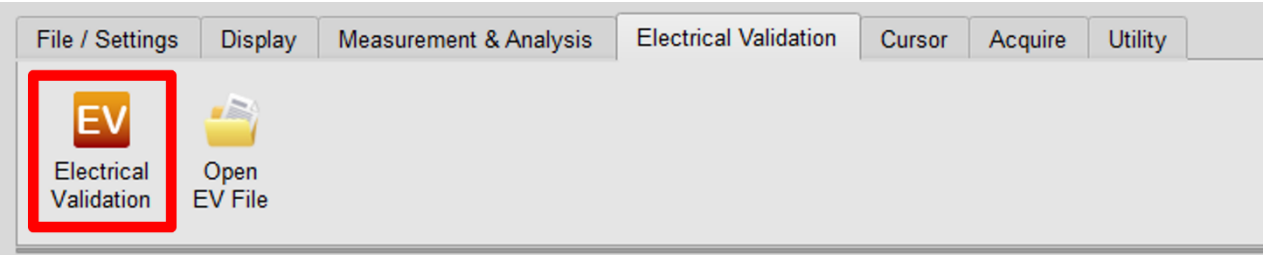
Symbol	Electrical Parameter
$t_{SU,SDI}$	SDI Setup Time
$t_{HD,SDI}$	SDI Hold Time
t_{DIO}	SDI Output Delay Time
$t\text{-}_{SU,SDO}$	SDO Setup Time
$t_{HU,SDO}$	SDO Hold Time
t_D	SDO Output Delay Time
t_{HIGH}	SCLK High Time
t_{LOW}	SCLK Low Time
$t_{SU,CS}$	CS Chip Select Setup Time
$t_{SU,CS}$	CS Chip Select Hold Time
t_{CS}	Chip Select Deselect time (Chip Select High Time)
t_{CLKr}	SCLK Clock Rise Time
$t\text{-}_{CLKf}$	SCLK Clock Fall Time

SPI Voltage Requirements

Symbol	Electrical Parameter
V_{IL}	Low-Level Input Voltage
V_{IH}	High-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage

UART 电气特性验证解决方案

■ 简介：



使用示波器进行 UART 电气特性验证，以确认 UART 是否符合所定义的规格。在长时间持续运行测试之后，可验证被测信号的电气特性是否达标。

对于协议的电气验证，UART 协议的电气特性检测通常分为两种：**垂直（电压）与水平（时间/相位）**。

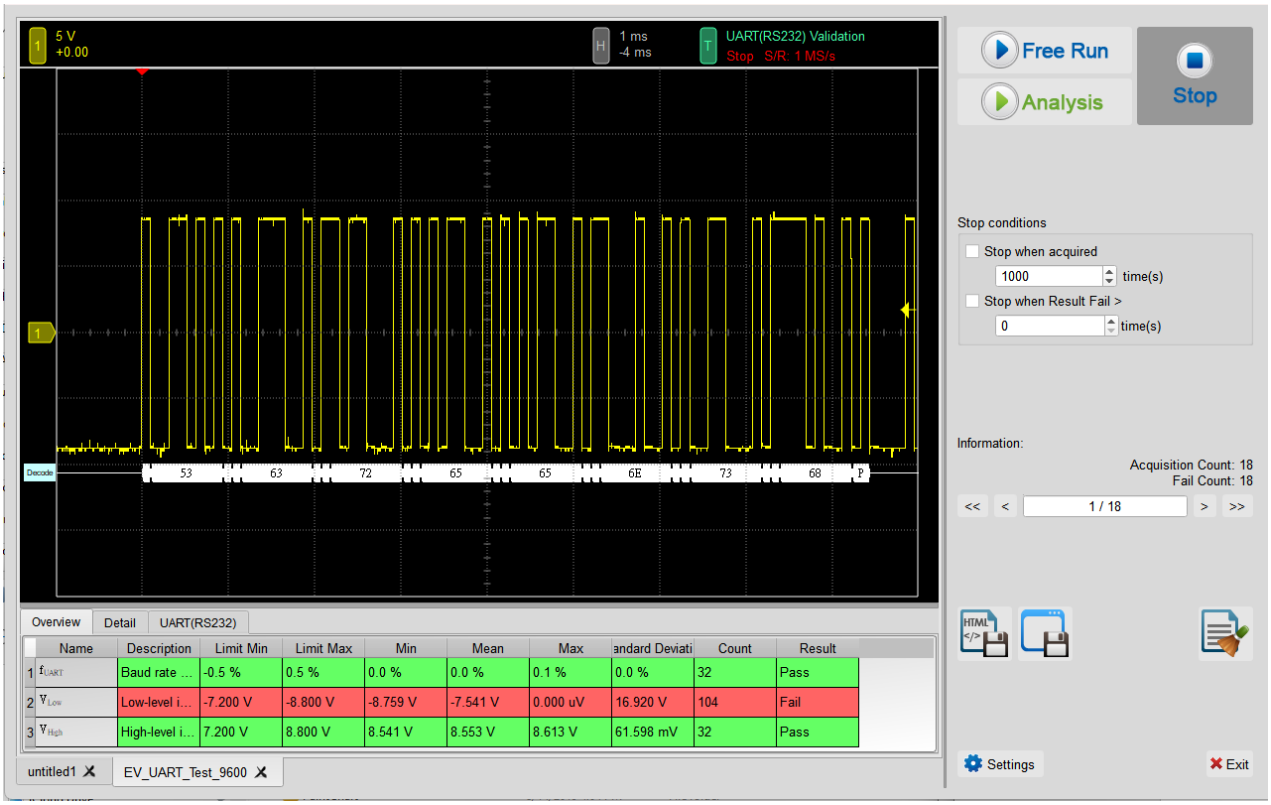
因此，使用本功能前，需先设置协议类型与规格，然后重复测试以获得电气特性测试报告。测试项目会依 UART 传输速率不同而有不同的规格与标准。

UART 验证报告：

Overview | Detail | UART(RS232)

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f_{UART}	Baud rate ...	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	Pass
2	V_{Low}	Low-level i...	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	Fail
3	V_{High}	High-level i...	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	Pass

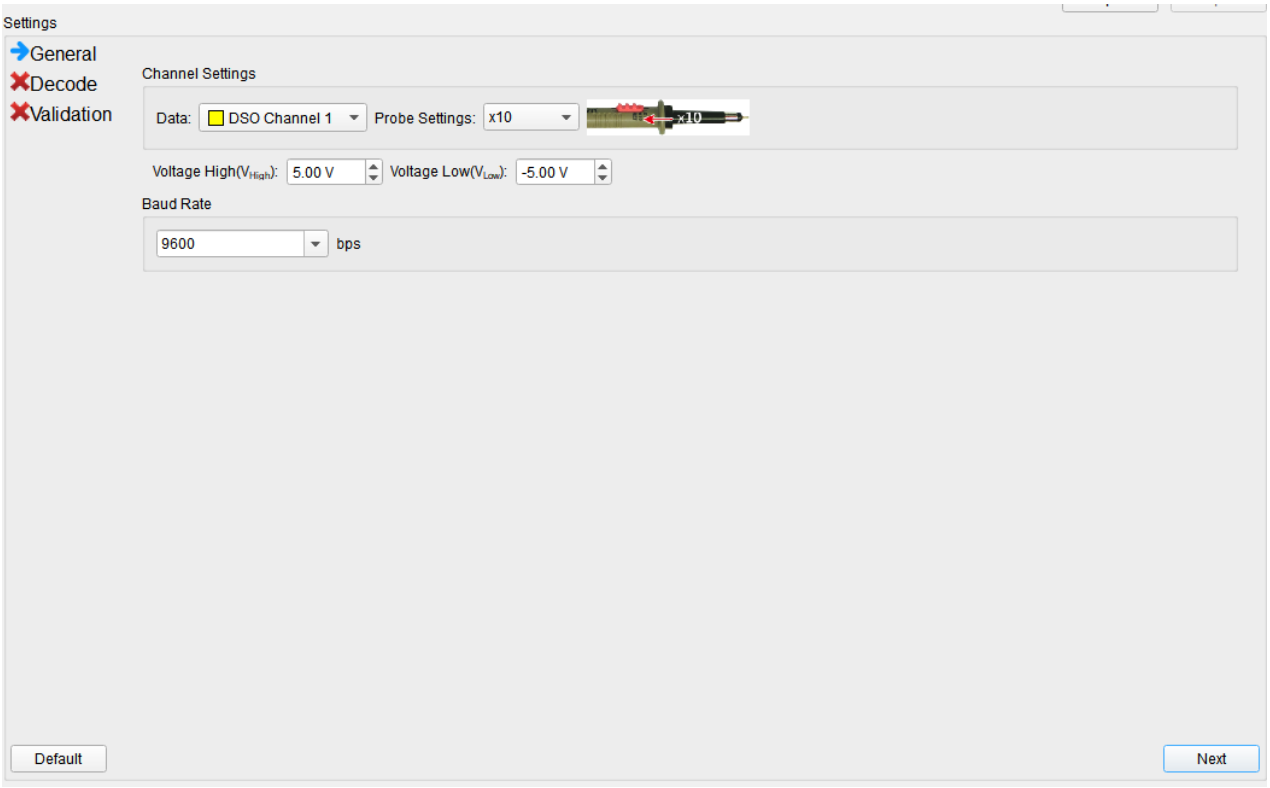
电气特性验证_软件画面：



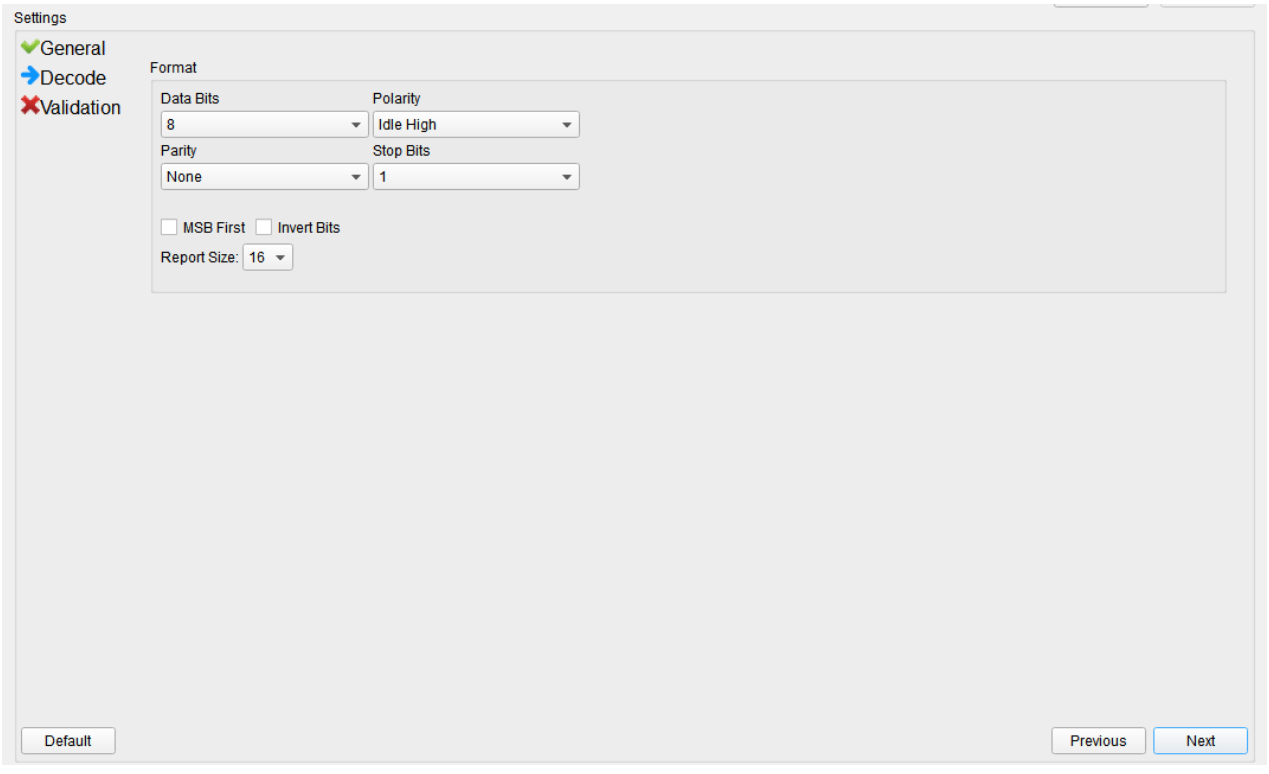
1. 频率：时钟速率
2. 时序参数：建立时间（Set-up Time）、保持时间（Hold Time）、上升时间（Rise Time）、下降时间（Fall Time）与时钟拉伸（Clock Stretching）时间限制
3. 电压参数：V_IL（输入低电位）、V_IH（输入高电位）等

UART 电气特性验证设置

1. 一般设置：通道来源、工作电压与传输速率

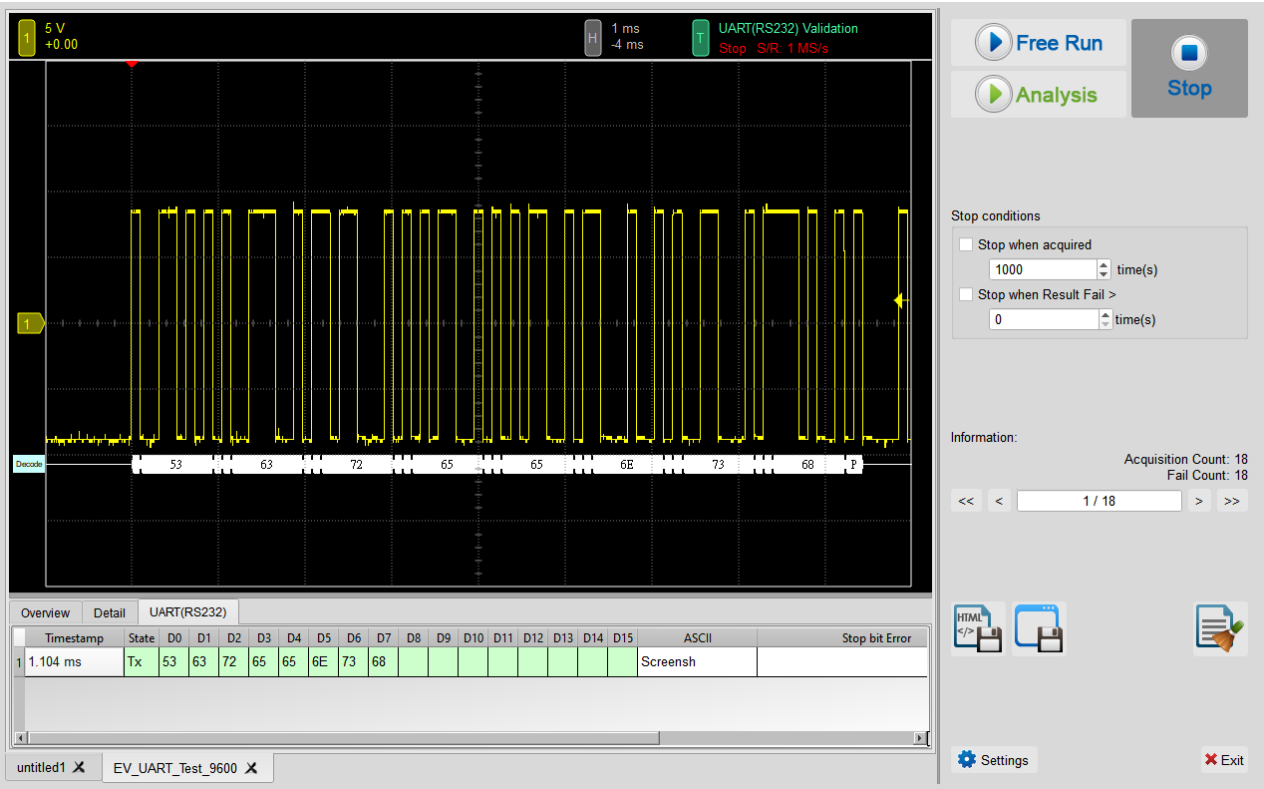


2. 解码设置：UART 解码设置

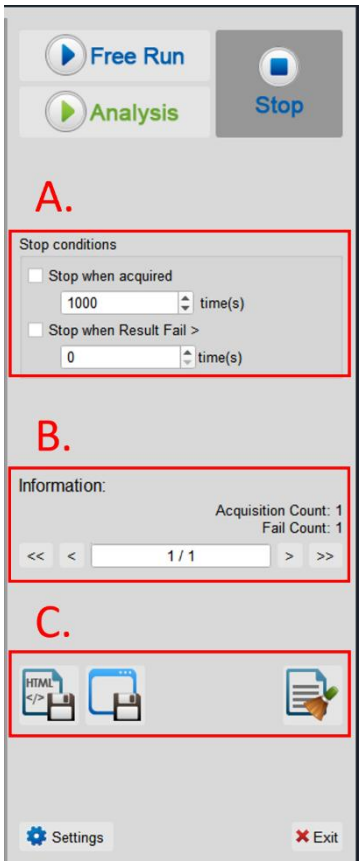


3. 验证参数设置：频率、时序与电压限制条件

4. 电气特性验证_软件画面



5. 控制面板



D. 停止条件：

当采集达到 X 次时停止

当测试结果失败超过 X 次时停止

E. 信息：

选择查看波形

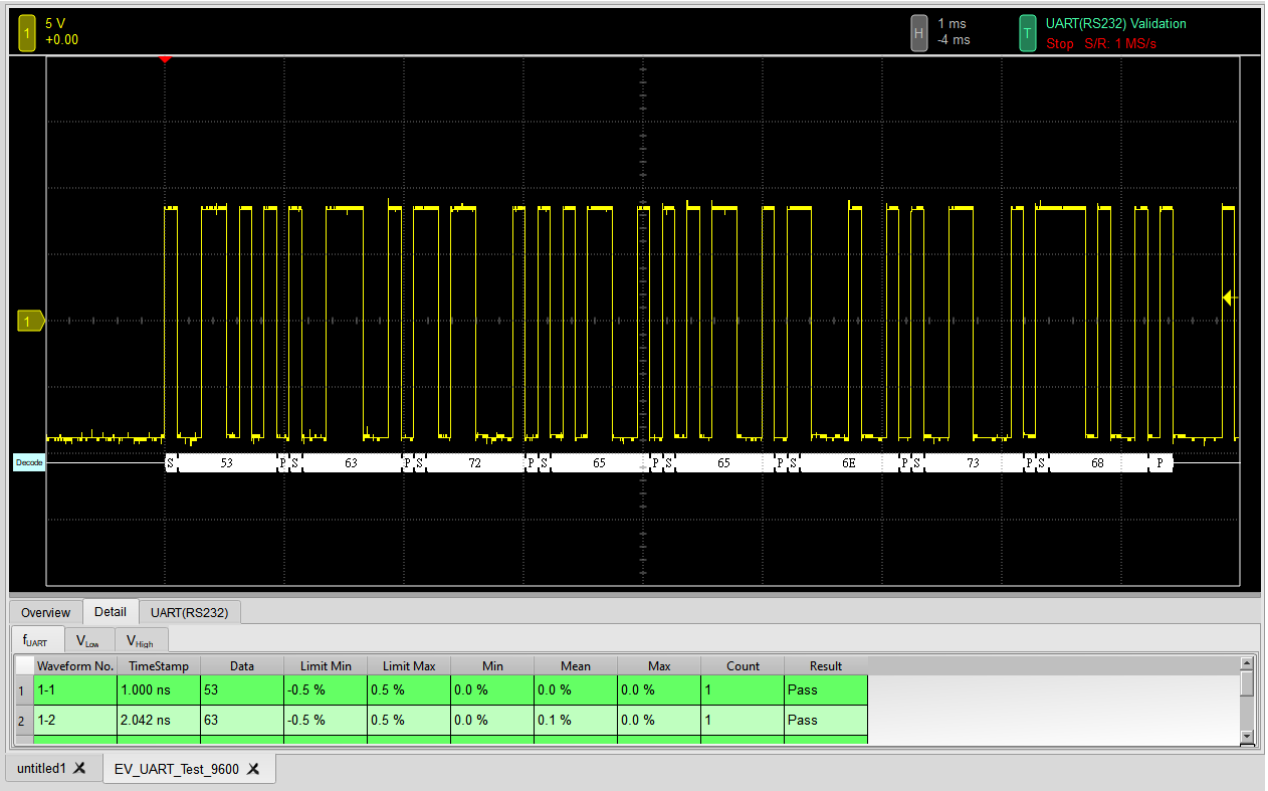
F. 储存档案：

储存为 HTML 格式

储存为 .MOW（Acute软件专用格式）

6. 概览报告

7. 详细报告



8. 波形和参考点

9. Html 报告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	04-27-2023 15:07:32
S/W Version	1.0.25
Protocol	UART(RS232)

Overview Results:

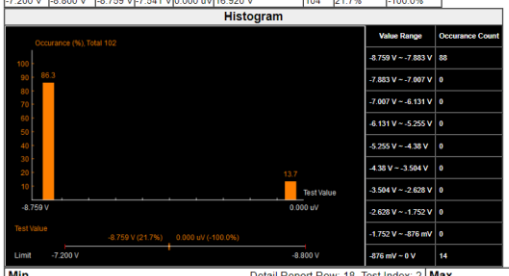
Total: 3
Pass: 2
Fail: 1

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{UART}	Baud rate for UART	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	-100.0%	-80.0%	✓Pass
2	V_{Low}	Low-level input voltage	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	21.7%	-100.0%	✗Fail
3	V_{High}	High-level input voltage	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	18.6%	-2.1%	✓Pass

V_{Low} - Test Result: Fail
Description: Low-level input voltage

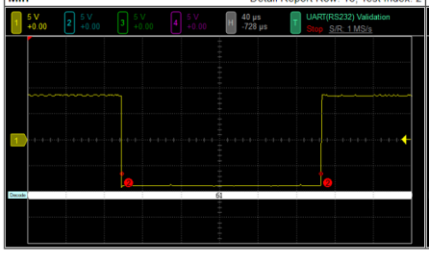
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	21.7%	-100.0%

Histogram

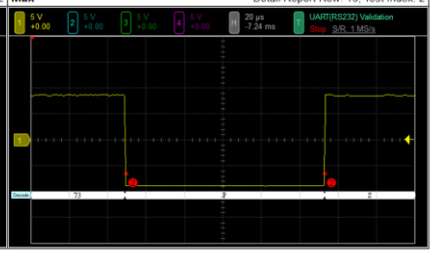


Value Range	Occurance Count
-8.759 V ~ -7.883 V	88
-7.883 V ~ -7.007 V	0
-7.007 V ~ -6.131 V	0
-6.131 V ~ -5.255 V	0
-5.255 V ~ -4.38 V	0
-4.38 V ~ -3.504 V	0
-3.504 V ~ -2.628 V	0
-2.628 V ~ -1.752 V	0
-1.752 V ~ -876 mV	0
-876 mV ~ 0 V	14

Min Detail Report Row: 18, Test Index: 2



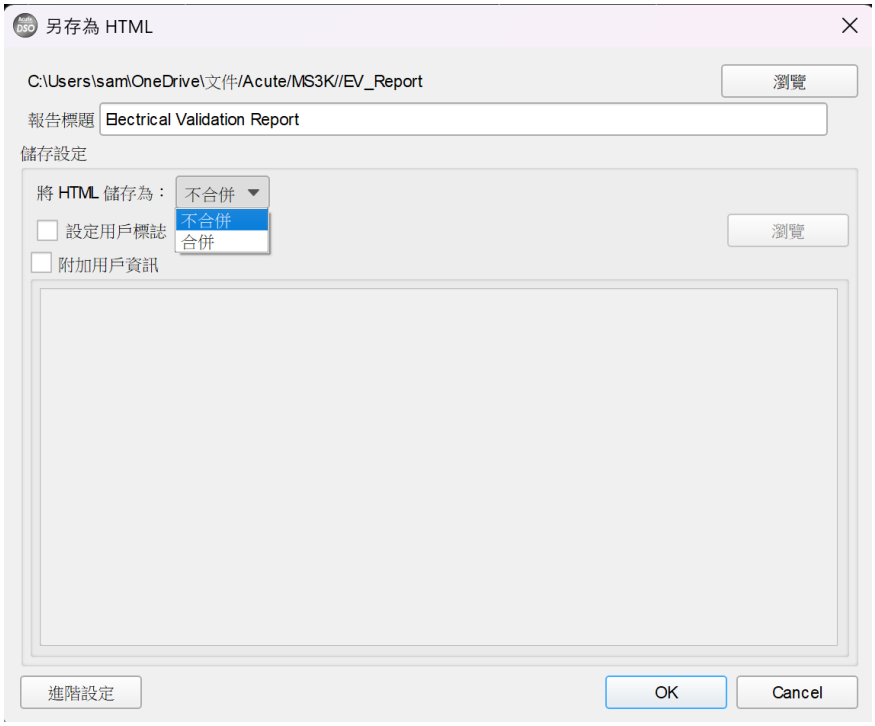
Max Detail Report Row: 16, Test Index: 2



HTML 报告导出

■ 简介

每次 EV 测试皆支持导出 HTML 报告。HTML 报告包含每个测试项目、测试结果、最大/最小值、直方图与波形截图。



储存设置：

A. 将 HTML 储存为：不合并/合并

不合并：图片会与 HTML 分开储存。

合并：图片会嵌入在 HTML 档案中（单一档案）。

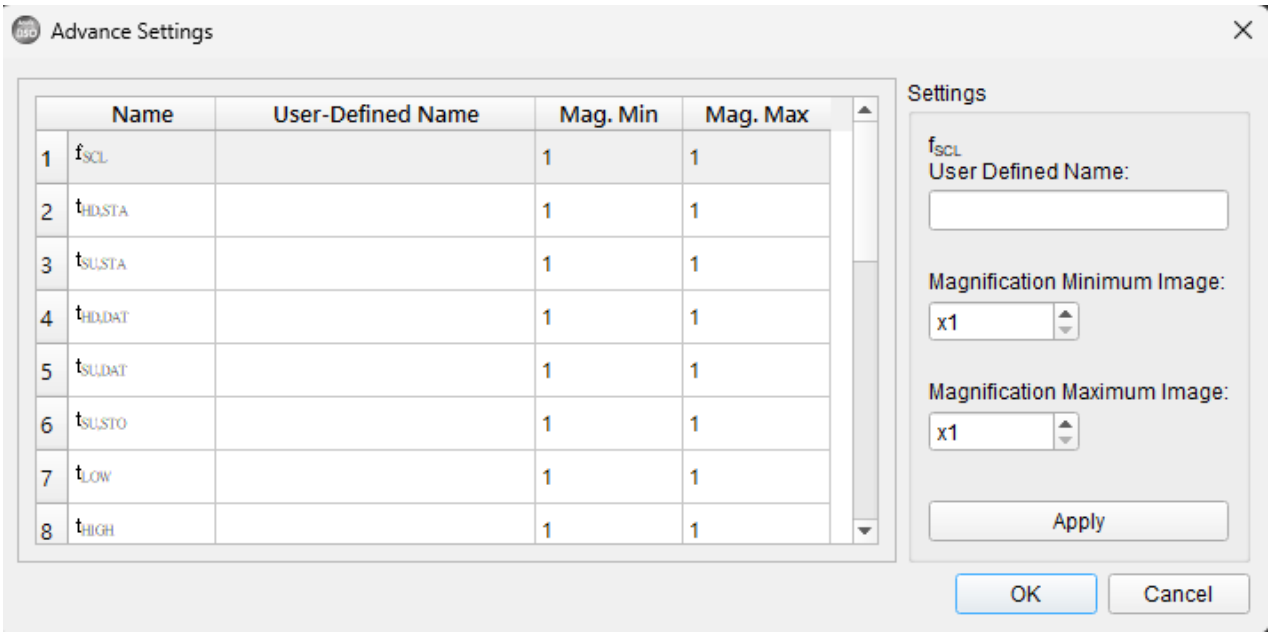
B. 设置用户标志 Logo：

勾选后可选择图片文件作为报告中的公司/用户标志。

C. 附加用户信息：

可在此输入任何想要加入到报告中的补充说明或用户信息。

进阶设置：



A. 用户可自定义测试项目于 HTML 报告中的显示名称

B. 用户亦可调整 HTML 报告中图片的显示倍率

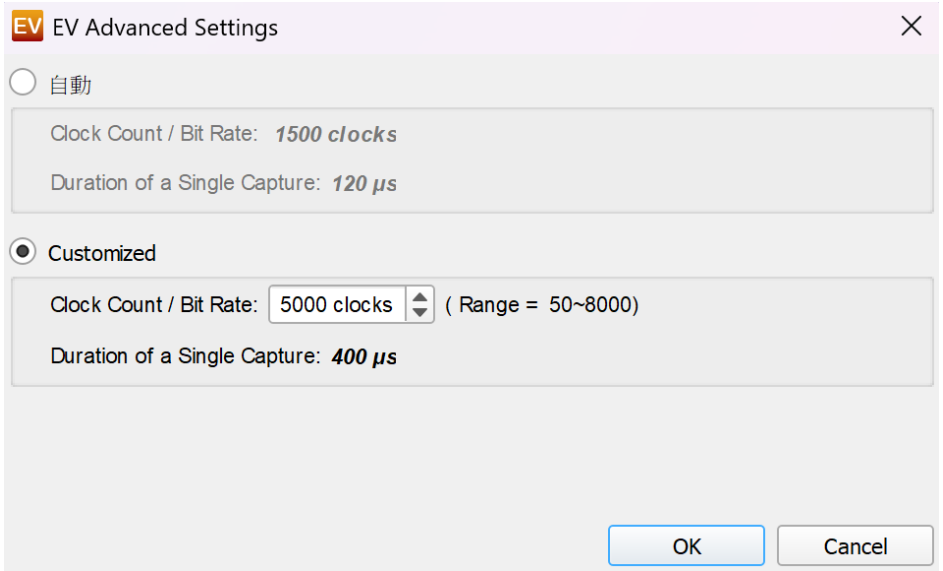
进阶设置

简介

EV 测试允许使用者根据每次采集的需求，调整预设的采集时间。由于不同的协议有不同的预设频率或传输速率，这些差异主要来自于协议的传输速度与数据包长度的不同。有时候，为了更准确地分析数据，可能需要采集更长的数据包。因此，**Acute** 提供了 **进阶设置** 功能，让用户可以个别调整各项参数的采集时间。

*仅在进入 EV 参数设置 时，才会显示 进阶设置 按钮

EV 进阶设置：



MSO/TS3000 系列多机叠加

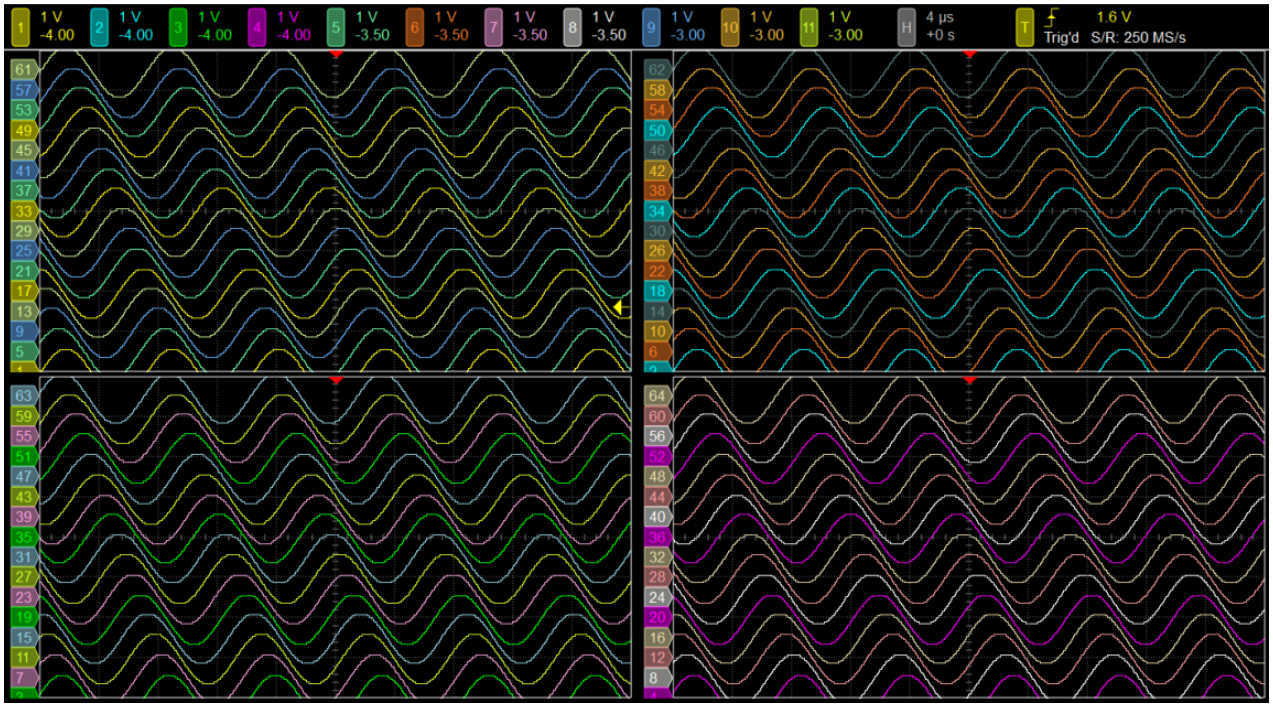
简介

Acute MSO3K / TS3K示波器的特点之一是其多机组合叠加功能，这使得最多可叠加16台示波器，同时实现64通道最高250MS/s，或是16通道最高1GS/s的测量能力。在机壳设计方面，MSO3K / TS3K专为叠加应用而设计，具备精心设计的定位导槽，使示波器在叠加配置中能够完美摆放。此外，示波器的散热性能也得到了充分考虑，配置了双侧散热孔，确保长时间运行时不会出现过热问题。

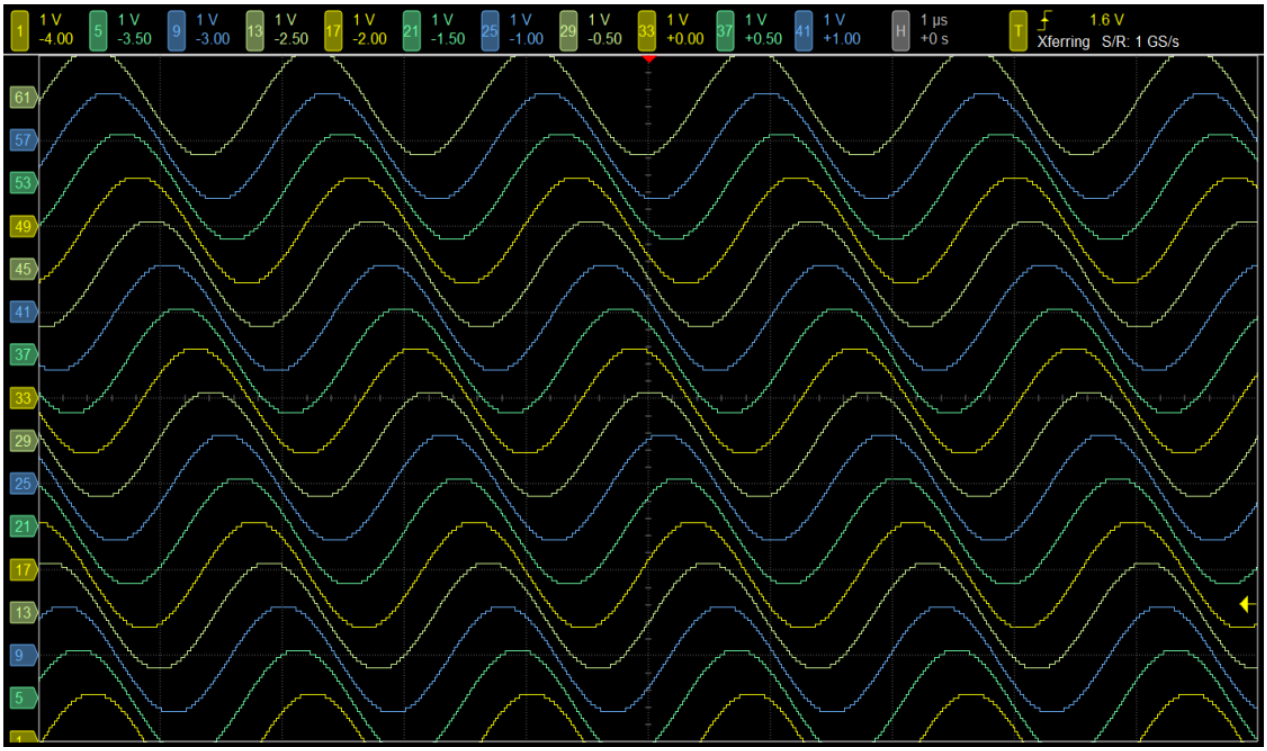
在信号连接方面，用户可以选择直接将待测信号通过标准BNC接头连接到示波器，或者使用被动探棒或差分探棒进行更广泛性的测量。此外，Acute还提供了BNC to Probe Tip Adaptor，可以改善传统探棒在连接上常见的测量连接质量问题，确保用户获得最准确的测量结果。

软件画面

1. 64Channel @ 250MS/s



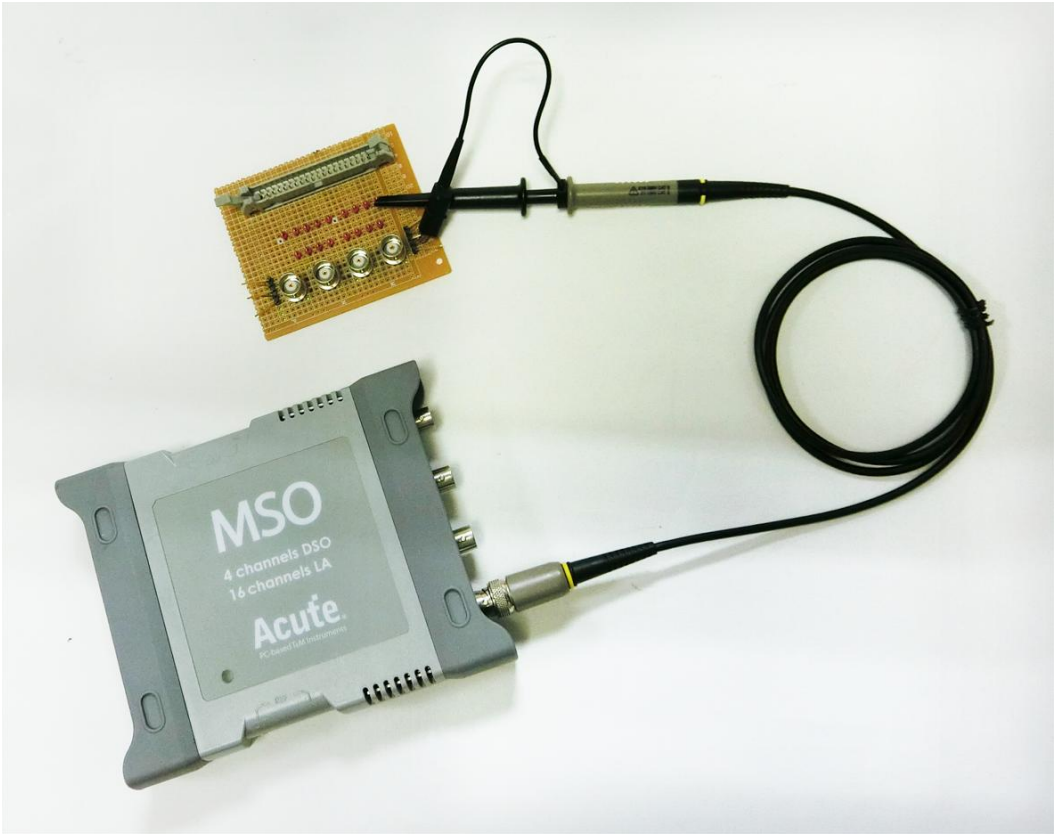
2. 16Channel @ 1GS/s



各种信讯号连接方式

1. 信号线直接透过BNC to BNC接头连接

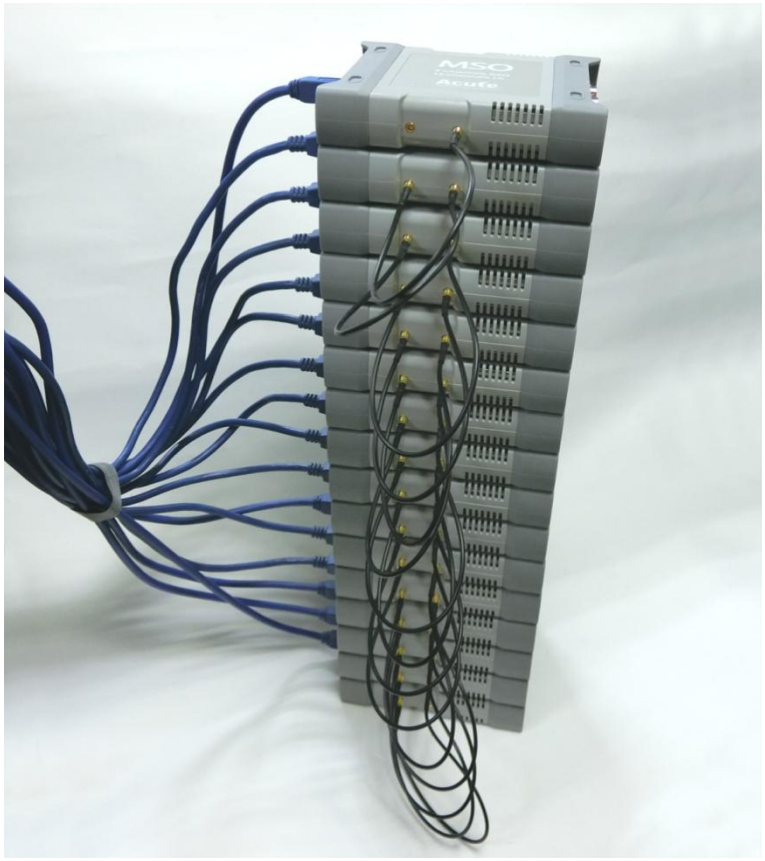
2. 搭配被动探棒测量



3. 搭配被动探棒以及BNC to Probe Tip Adaptor测量

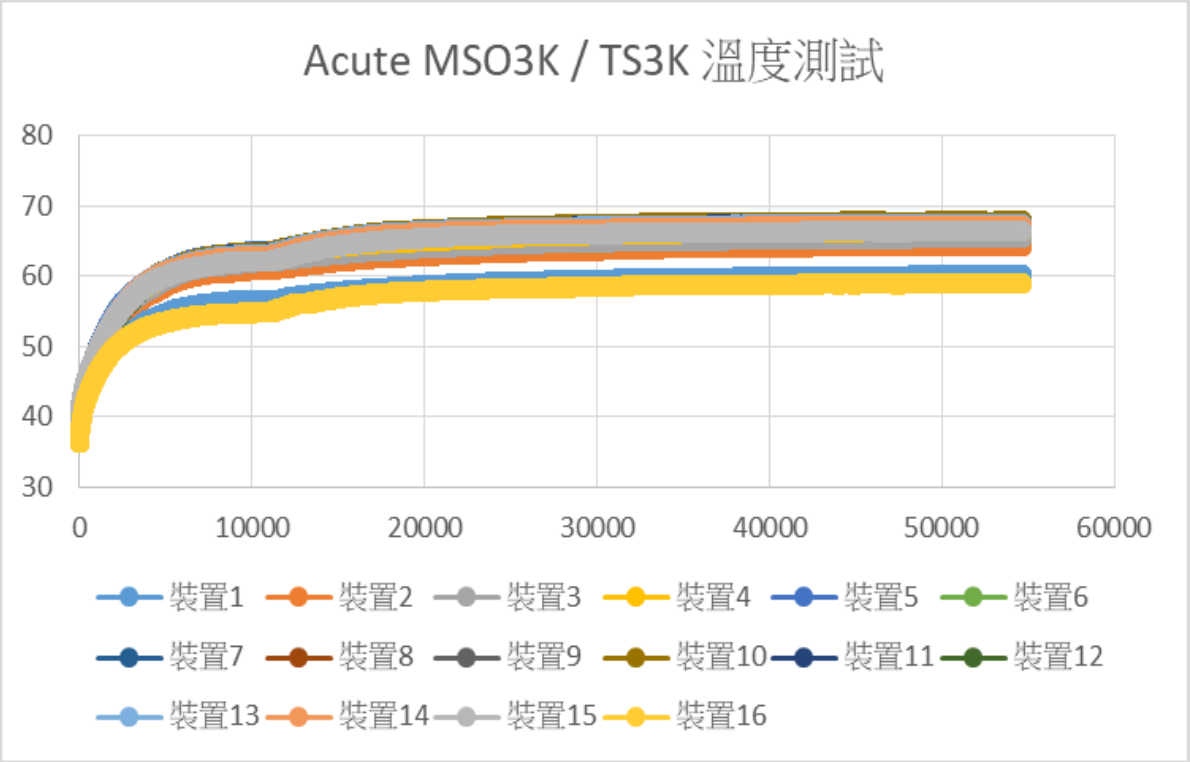
4. 搭配高压差分探棒测量

5. 实际叠加画面 16台(64 Channels)



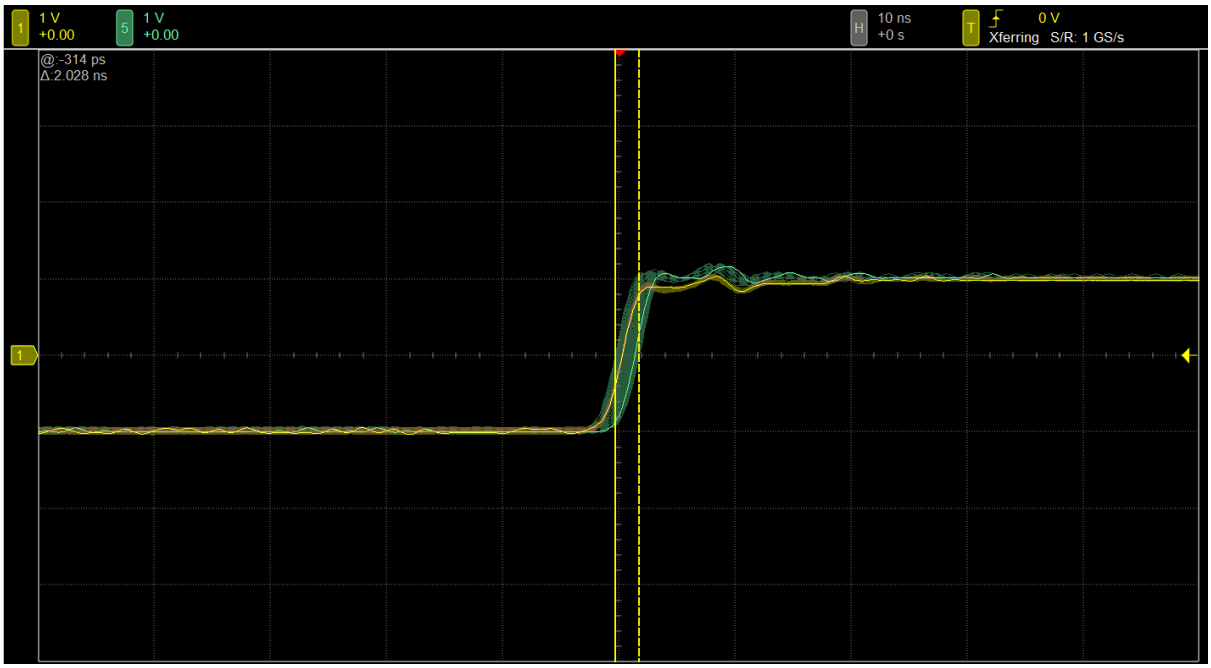
注意事項

1. MSO3K / TS3K 示波器为 USB3.0 接口界面的仪器，运作时需消耗 4.5~7.7W，使用时建议连接至台式电脑后方的 USB3.0 插槽或是使用具有独立供电的 USB3.0 hub，以提供最佳的电力供应及最佳的测量性能。
2. MSO3K / TS3K 示波器经过内部测试，在叠加状态下仍可保持长时间运作不致过热，但若长时间于高温或不利于散热环境使用时，仍须注意示波器工作温度并适度提供额外散热方式，以避免示波器过热（> 80 度 C）而影响操作。



3. 多机叠加时，各机器间根据采样率不同，会产生一定程度的相位差，以 1GS/s 采样率为例，主机和第一台从机间的相位差为 < ±2ns，和最后一台从机间的相位差为 < ±3ns。

主机和第一台从机(2nd)的相位差



主机和最后一台从机(16th)的相位差