

电气特性验证说明





Protocols

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I2C 电气特性验证解决方案

■ 简介:

File / Settings Disp	lay Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation						

使用示波器进行 I2C 电气特性验证,以确保 I2C 符合定义的规范。在经过长时间的持续 运行测试后,可以确认所测试的信号电气特性符合规范。

I2C 协议的电气特性检测通常分为两种类型:垂直(电压)与水平(时间/相位)。

因此,在使用此功能时,必须先设置所选的协议与规格,然后重复测试以取得电气特性测试报告。测试项目会依据 I2C 的速度而有所不同。

常见 I2C 规格中的部分电气特性规格:

Symbol	Parameter	Conditions	C _b = 100	pF (max)	C _b = 4	00 pF ^[2]	Unit
			Min	Max	Min	Max	
f _{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
t _{SU;STA}	set-up time for a repeated START condition		160	-	160	*	ns
t _{HD;STA}	hold time (repeated) START condition		160		160		ns
tLOW	LOW period of the SCL clock		160		320	i i	ns
t _{HIGH}	HIGH period of the SCL clock		60	-	120	-	ns
t _{SU;DAT}	data set-up time		10	-	10	8	ns
t _{HD;DAT}	data hold time		0 ^[3]	70	0 ^[3]	150	ns
t _{rCL}	rise time of SCLH signal		10	40	20	80	ns
t _{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
t _{fCL}	fall time of SCLH signal		10	40	20	80	ns

Table 13. Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I²C-bus devices^[1]



I2C 电气特性验证 报告内容:

C	verview [etail I2C							
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	fact.	SCL clock frequencey	0.000 Hz	400.000 KHz	387.596 KHz	387.683 KHz	387.897 KHz	34200	Pass
2	THEUST A	Hold time(repeated) START condition	600.000 ns	-	1.536 us	1.537 us	1.540 us	200	Pass
3	ISU,STA	Set-up time for a repeated START condition	600.000 ns	-	2.010 us	2.012 us	2.014 us	100	Pass
4	UHDLDAT	Data hold time	-	-	94.000 ns	274.110 ns	1.028 us	17250	Pass
5	I SULDAT	Data Set-up time	100.000 ns	-	472.000 ns	1.066 us	1.444 us	25100	Pass
6	leusto	Set-up time for STOP condition	-	-	-	-	-	0	
7	tLow	Low Period of the SCL Clock	1.300 us	-	1.538 us	1.542 us	1.544 us	34100	Pass
8	чнон	High Period of the SCL Clock	600.000 ns	-	974.000 ns	982.475 ns	3.560 us	41800	Pass
9	Vci.	Rise time of SCL signal	20.000 ns	300.000 ns	45.999 ns	50.304 ns	51.999 ns	41800	Pass
10	\$rcL	Fall time of SCL signal	20.000 ns	300.000 ns	10.000 ns	10.528 ns	11.999 ns	41800	Fail
11	\$DA	Rise time of SDA signal	20.000 ns	300.000 ns	37.999 ns	39.210 ns	41.999 ns	9300	Pass
12	10A	Fall time of SDA signal	20.000 ns	300.000 ns	4.000 ns	6.714 ns	10.000 ns	9900	Fail
13	teur	Bus free time between a STOP and START condition	-	-	-	-	-	0	-
14	IVD,DAT	Data valid time	-	900.000 ns	98.000 ns	267.062 ns	1.068 us	15750	Fail
15	TVELACK	Data valid acknowledge time	-	900.000 ns	98.000 ns	623.009 ns	1.068 us	1500	Fail

电气特性验证_软件画面:



- 不同的速度模式,包含标准模式(Standard Speed Mode,约 100kHz)/快速模式 (Fast Mode,约 400kHz)/快速模式+(Fast Mode+,约 1MHz)/高速模式(HS Mode,约 3.4MHz)
- 2. 频率:时钟频率(Clock Speed)
- 时序参数:建立时间(Set-up Time)、保持时间(Hold Time)、上升时间(Rise Time)、 下降时间(Fall Time)与时钟拉伸(Clock Stretching)时间限制
- 4. 电压参数: V_IL (输入低电位)、V_IH (输入高电位) 等



■ I2C 电气特性验证设置

1. 一般设置: 通道来源、工作电压与速度

Orthings		Import	Export
General	Channel Settings		
TriggerValidation	SCL: DSO Channel 1 • Probe Settings: x10 • Image: state sta		
	Working Voltage(V₀₀): 3.30 V ♀ Speed Mode		
	 Standard Mode (Max: 100Kbit/s) Fast Mode (Max: 400Kbit/s) 		
	 ○ Fast Mode + (Max: 1Mbit/s) ○ High Speed Mode (Max: 3.4Mbit/s) Cb Value= 100pf (Max.) ▼ 		
	O Customized Speed 100 Kbit/s €		
Default		(Next

2. 解码设置: I2C 解码设置

Sottings		Import	Export
 ✓General →Decode 	Address Mode		
XTrigger XValidation	 7-bit Addressing 8-bit Addressing (Including R/W in Address) 10-bit Addressing 		
Default		Previous	Next



3. 触发设置: I2C Address、Data 触发条件

Settings		
 ✓General ✓Decode 	Trigger Settings	
 Trigger Validation 	7-bit Address: XXh Write/Read: ACK/NACK Data	
	Any Offset Fixed Offset Bytes	
	Value	
	XXh •	
	XXh	
	XX(h • • • •	
	XXh ·	
Defeut		Projeus
Derault		Previous Next

4. 验证参数设置: 频率、时序与电压限制条件

de	Customized E	V Parameter:		
er ation	Frequen	су		
ation	Name	Description	Min	Max
	1 ✔ f _{SCL} SCL c	lock frequency	0 kHz	100 kHz
	⊿ Time			
	Name	Description	Min	Max
	1 ⊻ t _{HD,STA}	Hold time(repeated) START condition	4 us	Х
	2 ✓ t _{SU,STA}	Set-up time for a repeated START condition	4.7 us	X
	3 ✓ t _{HD,DAT}	Data hold time	5 us	х
	4 ✓ t _{SU,DAT}	Data Set-up time	250 ns	х
	5 ✓ t _{SU,STD}	Set-up time for STOP condition	4 us	Х
	6 ✓ t _{LOW}	Low Period of the SCL Clock	4.7 us	х
	7 ✓ t _{HIGH}	High Period of the SCL Clock	4 us	x
	8 ✔ t _{rCL}	Rise time of SCL signal	х	1 us
	9 ✔ t _{fCL}	Fall time of SCL signal	X	300 ns
	10 ✔ t _{rDA}	Rise time of SDA signal	Х	1 us
	11 ✓ t _{fDA}	Fall time of SDA signal	х	300 ns



EV Electrical Validation	ı				
120	Settings				Import Export
I2C I2S MIPI I3C MIPI RFFE MIPI SPMI PDM	 ✓General ✓Decode ✓Trigger ✓Validation 	Customized EV	Parameter: y		
SMBus		Name	Description	Min	Max Max
UART(RS232)		1 Vunc 1 V t _{HD,STA}	Hold time(repeated) START condition	160 ns	X
		2 ✔ t _{SU,STA}	Set-up time for a repeated START condition	160 ns	X
		3 🗸 t _{HD,DAT}	Data hold time	0 ns	X
		4 ✔ t _{su,DAT}	Data Set-up time	10 ns	X
		5 ✔ t _{su,sto}	Set-up time for STOP condition	160 ns	70 ns
		6 ✓ t _{LOW}	Low Period of the SCL Clock	160 ns	X
		7 🗹 t _{HIGH}	High Period of the SCL Clock	60 ns	40 ns
		8 🗹 t _{rCLH}	Rise time of SCLH signal	10 ns	40 ns
		9 🗹 t _{ICLH}	Fall time of SCLH signal	10 ns	80 ns
		10 🗸 t _{rDAH}	Rise time of SDAH signal	10 ns	80 ns
		11 ✔ t _{fDAH}	Fall time of SDAH signal	10 ns	×
		12 🗸 t _{BUF}	Bus free time between a STOP and START condition	×	×
		13 ✔ t _{VD,DAT}	Data valid time	×	×
		14 VD,ACK	Data valid acknowledge time	×	×
		15 V t _{CLK_STRET}	Or Clock extend time	×	25 ms
		16 ✔ t _{rCL1}	First rising edge time of SCL signal after Sr and after ACK bit	10 ns	80 ns
		Voltage			
	Default	Advance			Previous Apply

第 16 项选项仅在 I2C 速度模式设置为高速模式(High Speed Mode)时可见



5. 电气特性验证_软件画面



6. 控制面板



A. 停止条件:

当采集达到 X 次时停止 当测试结果失败超过 X 次时停止

B. 信息: 选择查看波形

C. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)

7. 概览报告

1	500 mV -3.50	2 500 mV -3.50 3	500 mV -3.50		4 500 mV -3.50		Н 100 µs -400 µs	T 12C Trig	Validation d <u>S/R: 500 N</u>	<u>15/s</u>
1										
Ov	erview Deta	ail I2C	Limit Min	Limit May	Min	Maan	Max	andard Doviativ	Count	Pocult *
1	f _{SCL}	SCL clock frequencey	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.004 KHz	11.000 Hz	480	Fail
2	t _{HD,STA}	Hold time(repeated) START condition	4.000 us		2.499 us	3.094 us	4.999 us	1.817 us	21	Fail
3	tsu,sta	Set-up time for a repeated START condition							0	
4	t _{HD,DAT}	Data hold time	5.000 us		2.497 us	2.498 us	2.498 us	1.118 ns	146	Fail
5	tsu,dat	Data Set-up time	250.000 ns		2.499 us	2.499 us	2.499 us	722.000 ps	154	Pass
6	tsu,sro	Set-up time for STOP condition	4.000 us		2.498 us	3.450 us	4.998 us	1.987 us	21	Fail
7	tLow	Low Period of the SCL Clock	4.700 us		4.998 us	4.998 us	4.999 us	1.947 ns	480	Pass
8	thigh	High Period of the SCL Clock	4.000 us		4.998 us	4.999 us	4.999 us	1.862 ns	480	Pass
9	ta	Rise time of SCL signal		1.000 us	1.223 ns	1.587 ns	2.065 ns	2.050 ns	561	Pass
40	t	F-11-2		200 000	1 040	4 500	1 047	4 707	400	



8. 详细报告

1 500 mV -3.50	2 500 mV -3.50		3 500 mV -3.50		4 500 n -3.50		H 100) µs 0 µs Т	I2C Validatio	n 500 <u>MS/s</u>
				30					21	
			den den den den	af a statetaka ar	N Y Y Y Y Y	a alavarabalere	de a la dela.	a <mark>Mala Jun</mark> a A	<mark>datan kara</mark> ta	
1 Overview Detail									Cataban a matter.	
Overview Detail	I2C tsu,sta tho,par tsu,c	AT tsu,sto	tLow thigh	tron trong	L t _{rDA} t		t _{VD,DAT} t _{VD}			
Overview Detail	tour of the approximation of the second seco	AT t _{SU,STO} Address	t _{LOW} t _{HIGH}	t _{rCL} t _{rC} Limit Min	L t _{rDA} t Limit Max	IDA t _{BUF} Min 99.996 KHz	t _{VD,DAT} t _{VD} Mean		V _{IH} Count	Result A
Overview Detail fscL tHD.STA Waveform No. 1 1 45 0 1	Inclusion Inclusion <t< td=""><td>AT t_{SU,STD} Address 12</td><td>t_{LOW} t_{HIGH} D0-D7 10 20 30</td><td>t_{rcL} t_{rc} Limit Min 0.000 Hz</td><td>L t_{rDA} t Limit Max 100.000 KHz</td><td>DA t_{BUF} Min 99.996 KHz</td><td>t_{vD,DAT} t_{vD} Mean 99.998 KHz</td><td>Max 100.000 KHz</td><td>V_{EH} Count 32</td><td>Result A</td></t<>	AT t _{SU,STD} Address 12	t _{LOW} t _{HIGH} D0-D7 10 20 30	t _{rcL} t _{rc} Limit Min 0.000 Hz	L t _{rDA} t Limit Max 100.000 KHz	DA t _{BUF} Min 99.996 KHz	t _{vD,DAT} t _{vD} Mean 99.998 KHz	Max 100.000 KHz	V _{EH} Count 32	Result A
Overview Detail fsc. t _{HD,STA} Waveform No. 1 1 45 2 1 22 4 22 23	12C tau.stn. tuburt tau. TimeStamp Status 9.982 ns START 39.359 ns START	AT t _{SU,STO} Address 12 3F	tLow tHIGH D0-D7 10 20 30 00	t _{rcL} t _{rc} Limit Min 0.000 Hz 0.000 Hz	L t _{-DA} t Limit Max 100.000 KHz	Min 99.996 KHz 99.997 KHz	t _{VD,DAT} t _{VD} Mean 99.998 KHz 99.998 KHz	Max 100.000 KHz 100.001 KHz	V _{EH} Count 32	Result A
Overview Detail fscl t _{HD,STA} Waveform No. 1 1 45 2 1 3 1	I2C tsu.stn typ.par TimeStamp Status 9.982 ns START 39.359 ns START 37.484 ns START	AT t _{SU,STO} Address 12 3F 46	t _{LOW} t _{HIGH} D0-D7 10 20 30 00 21 3A	t _{rcL} t _{rc} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} t Limit Max 100.000 KHz 100.000 KHz	na t _{eur} Min 99.996 KHz 99.997 KHz 99.997 KHz	t _{vp.par} t _{vp.} Mean 99.998 KHz 99.998 KHz	ACK VIL Max 100.000 KHz 100.000 KHz 100.000 KHz	V _{III} Count 32 16 24	Result A Pass Fail Pass
Overview Detail fscl. t _{HD.STA} Waveform No. 1 1 45 2 1 3 1 3 2 4 2	I2C tsu.stn tyto.oxt tsu.stn 9.982 ns START 39.359 ns START 37.484 ns START 9.982 ns START	AT t _{SU,STO} Address 12 3F 46 3F	t _{LOW} t _{HIGH} D0-D7 10 20 30 00 21 3A 00	t _{rCL} t _c Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} t Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	 τ_{виг} τ_{виг} Min 99.996 KHz 99.997 KHz 99.997 KHz 99.994 KHz 	t _{vp.p.vr} t _{vp.} <u>Mean</u> 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	ACK VI. Max Max 100.000 KHz 100.001 KHz 100.000 KHz 100.000 KHz 100.002 KHz	V _{E1} Count 32 16 24 16	Result A Pass Fail Pass Fail
Overview Detail fscL t _{HD.STA} Waveform No. 1 1 2 3 1 3 2 4 2 5 2	I2C tsu.stn. typ.par tsu.stn. typ.par 9.982 ns START 39.359 ns START 37.484 ns START 9.982 ns START 37.484 ns START 48.108 ns START	AT t _{SU,STO} Address 12 3F 46 3F 46	t _{LCOW} t _{HIGH} D0-D7 10 20 30 00 21 3A 21 3A 21 3A	t _{rcL} t _{rC} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} t Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	DA teur Min 99.996 KHz 99.997 KHz 99.997 KHz 99.994 KHz 99.995 KHz	tvo.ovr tvo. Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	Ack V _E Max 100.000 KHz 100.000 KHz 100.000 KHz 100.002 KHz 100.000 KHz	V _{B1} Count 32 16 24 16 24	Result Pass Fail Pass Fail Pass
Overview Detail fscL tri0.stA Waveform No. 1 1 2 3 1 3 1 4 2 5 2 14 45	I2C tau.srx tau.srx 9.982 ns START 39.359 ns START 37.484 ns START 9.982 ns START	AT t _{SU,STO} Address 12 3F 46 3F 46 46 12	t _{LOW} t _{HEGH} D0-D7 10 20 30 00 21 3A 10 20 30 21 3A 10 20 30	t _{rcL} t _c Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	trop trop trop trop trop trop trop trop	Iteur Iteur Min 99.996 KHz 99.997 KHz 99.997 KHz 99.995 KHz 99.995 KHz 99.996 KHz 99.996 KHz	tvp.par tvp. Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	Ack V _E Max 100.000 KHz 100.001 KHz 100.002 KHz 100.002 KHz 100.002 KHz 100.002 KHz 100.001 KHz	V _{III} Count 32 16 24 16 24 32	Result Pass Fail Pass Fail Pass Fail
Overview Detail facL t _{ID.STA} Waveform No. 1 1 1 2 1 3 1 3 1 5 2 14 2 6 3 4 45 7 3	I2C I2C taus g.g82 ns START 39.362 ns START 39.362 ns START 39.362 ns START 9.982 ns START	Art tsu.sro Address 12 3F 46 3F 46 3F 3F 46 3F 3F 3F	tLOW tHEAT	t _{rcL} t _c Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} t Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	ал t _{виг} Min 99.996 KHz 99.997 KHz 99.997 KHz 99.995 KHz 99.996 KHz 99.996 KHz	tvp.p.vr tvp. Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	Ack Vil. Max 100.000 KHz 100.001 KHz 100.002 KHz 100.002 KHz 100.001 KHz 100.001 KHz 100.001 KHz	V⊮1 Count 32 16 24 16 24 32 24 32 16	Result Pass Fail Pass Fail Pass Fail Fail Fail
Overview Detail fac. t _{10.57A} Waveform No. 1 1 1 4 2 3 1 5 2 14 2 6 3 7 3 2 2 8 3	I2C I2C I2C I2C I2DDAT Isuar I2DAT Isuar I2DAT	Art tsu.sto Address 12 3F 46 3F 46 3F 46 46 37 46 46 3F 46	t	t _{rcL} t _c Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	L t _{tDA} t Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	teur Min 99.996 KHz 99.997 KHz 99.997 KHz 99.997 KHz 99.996 KHz 99.995 KHz 99.996 KHz 99.996 KHz 99.995 KHz 99.995 KHz 99.995 KHz 99.995 KHz 99.995 KHz 99.995 KHz	tvp.p.vr tvp. Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	ACK VE. 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.001 KHz 100.001 KHz 100.001 KHz 100.001 KHz	V _{B1} Count 32 16 24 32 24 32 32 16 24 32 16 24	Result Pass Fail Pass Fail Pass Fail Fail Fail Fail
Overview Detail fac. tito.stx. Waveform No. 1 1 1 4 2 3 1 5 2 14 45 5 2 14 45 5 2 14 3 6 3 4 2 8 3 6 3	I2C tau.stx. turo.put tau.stx. 9.982 ns START 39.369 ns START 39.369 ns START 9.982 ns START 39.358 ns START 37.484 ns START 0.002 CTATT	AT tsu.sto Address 12 3F 46 3F 46 3F 46 12 3F 46 3F 46 3F 46 3F 46 3F 42 3F	tt.Harden t tt.t.Harden tt. tt.t.t.t.t.t.t.t.t.t.t.t	t _{rcL} t _c Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	L t _{rDA} t Limit Max 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz	taur taur Min 99.996 KHz 99.997 KHz 99.997 KHz 99.997 KHz 99.997 KHz 99.996 KHz 99.996 KHz 99.996 KHz 99.996 KHz 99.995 KHz 99.995 KHz 99.995 KHz 99.995 KHz	tvp.par tvp. Mean 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz 99.998 KHz	ACK VE. 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.000 KHz 100.001 KHz 100.001 KHz 100.001 KHz 100.004 KHz	V _{B1} Count 32 16 24 16 24 32 16 24 32 16 24 22	Result Pass Fail Pass Fail Fail Fail Fail Fail

9. 波形和参考点

1 500 mV -3.50		2 500 mV -3.50		3 500 m ³ -3.50		4 500 -3,8	0 m 50	V н	2 µs -394	966 µs Т	I2C Validation Stop S/R: 500 MS/s		Fr	ee Run
	*					- Pro-								nalysis St
						Addr(7b):3F				•		•	Stop condition Stop whe 1000 Stop whe 0	s n acquired
							E.) Detail						×
Overview De	tail I2C						Г Г	CL Waveform No.	1	Fime Stamp	Status	A	ddress	D0-D7
f _{SCL} t _{HD,STA}	t _{su,sta} t	HD,DAT t _{SU,DA}	r t _{su,sto}	t _{LOW} t _{HIG}	H t _{rCL} t _R	al t _{rDA}		1		239.359 ns	START		3F	00 tio
Waveform N	o. TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max		Time		∆ Time	Volt	∆ Volt	Result	<u> </u>
1 1	49.982 ns	START	40	40.00.20						1		1		
2 1		0.000	12	10 20 30	0.000 Hz	100.000 KH	1	(489.967 µs, 499.967	µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail	
	239.359 ns	START	3F	00	0.000 Hz 0.000 Hz	100.000 KH 100.000 KH	1 2	(489.967 µs, 499.967 (499.967 µs, 509.968	µs) µs)	10.000 µs 10.000 µs	(990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V	Fail Pass	
3 1	239.359 ns 337.484 ns	START START	3F 46	00 21 3A	0.000 Hz 0.000 Hz 0.000 Hz	100.000 KH 100.000 KH 100.000 KH	1 2 3	(489.967 µs, 499.967 (499.967 µs, 509.968 (509.968 µs, 519.967	hs) hs)	10.000 µs 10.000 µs 10.000 µs	(990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V	Fail Pass Fail	
3 1 4 2	239.359 ns 337.484 ns 49.982 ns	START START START	3F 46 3F	00 21 3A 00	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	100.000 KH 100.000 KH 100.000 KH 100.000 KH	1 2 3 4	(489.967 µs, 499.967 (499.967 µs, 509.968 (509.968 µs, 519.967 (519.967 µs, 529.968	hs) hs) hs)	10.000 µs 10.000 µs 10.000 µs 10.000 µs	(990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V 0 V	Fail Pass Fail Pass	
3 1 4 2 5 2	239.359 ns 337.484 ns 49.982 ns 148.108 ns	START START START START	3F 46 3F 46	00 21 3A 00 21 3A	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF	1 2 3 4 5	(489.967 µs, 499.967 (499.967 µs, 509.968 (509.968 µs, 519.967 (519.967 µs, 529.968 (529.968 µs, 539.968	hs) hs) hs)	10.000 µs 10.000 µs 10.000 µs 10.000 µs 10.000 µs	(990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V 0 V 0 V	Fail Pass Fail Pass Pass	
3 1 4 2 5 2 6 3	239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns	START START START START START	3F 46 3F 46 12	00 21 3A 00 21 3A 10 20 30	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH	1 2 3 4 5 6	(489.967 µs, 499.967 (499.967 µs, 509.968 (509.968 µs, 519.967 (519.967 µs, 529.968 (529.968 µs, 539.968 (539.968 µs, 549.968	μs) μs) μs) μs) μs)	10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs	(990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V 0 V 0 V	Fail Pass Fail Pass Pass	
3 1 4 2 5 2 6 3 7 3	239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 239.358 ns	START START START START START START	3F 46 3F 46 12 3F	00 20 30 21 3A 00 21 3A 10 20 30 00 20 30 00 20 30 00 00 00 00 00 00 00 00 00 00 00 00	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF	1 2 3 4 5 6 7	 (489.967 μs, 499.967 (499.967 μs, 509.968 (509.968 μs, 519.967 (519.967 μs, 529.968 (529.968 μs, 539.968 (539.968 μs, 549.968 (549.968 μs, 559.968 (549.968 μs, 559.968 	μs) μs) μs) μs) μs) μs) μs)	10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs	(990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V 0 V 0 V 0 V 0 V	Fail Pass Fail Pass Pass Pass Fail	_
3 1 4 2 5 2 6 3 7 3 8 3	239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 239.358 ns 337.484 ns	START START START START START START START	12 3F 46 3F 46 12 3F 46 46	10 20 30 00 21 3A 00 21 3A 10 20 30 00 21 3A	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF	1 2 3 4 5 6 7 8	(489.967 μs, 499.967 (499.967 μs, 509.968 (509.968 μs, 519.967 (519.967 μs, 529.968 (529.968 μs, 539.968 (539.968 μs, 549.968 (549.968 μs, 559.968	μs) μs) μs) μs) μs) μs) μs) μs)	10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs	(990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V 0 V 0 V 0 V 0 V	Fail Pass Fail Pass Pass Pass Fail Pass	_
3 1 4 2 5 2 6 3 7 3 8 3 4 4	239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 239.358 ns 337.484 ns	START START START START START START START	12 3F 46 3F 46 12 3F 46 46	10 20 30 00 21 3A 00 21 3A 10 20 30 00 21 3A	0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF 100.000 KF	1 2 3 4 5 6 7 8 9	(489.967 μs, 499.967 (499.967 μs, 509.968 (509.968 μs, 519.967 (519.967 μs, 529.968 (529.968 μs, 539.968 (539.968 μs, 549.968 (559.968 μs, 559.968 (559.968 μs, 569.968	μs) μs) μs) μs) μs) μs) μs) μs)	10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs	(990 mV, 990 mV) (990 mV, 990 mV)	0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V	Fail Pass Fail Pass Pass Pass Fail Pass	





Electrical Validation Report

Test Instrument Model	MSO3124V		
Test Instruments Serial Number	24554		
Test Date	04-17-2023 14:46:14		
S/W Version	1.0.25		
Protocol	I2C		
/*************************************			

Overview Results:

Total: 17 Pass: 9 Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f _{SCL}	SCL clock frequency	0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%	×Fail
2	t _{HD,STA}	Hold time(repeated) START condition	4.000 us		1.538 us	1.538 us	1.539 us	427.000 ps	20	-61.6%		×Fail
3	t _{su,sta}	Set-up time for a repeated START condition	4.700 us		2.013 us	2.014 us	2.015 us	579.000 ps	10	-57.2%		×Fail
4	t _{hd,dat}	Data hold time	5.000 us		94.249 ns	247.342 ns	1.026 us	4.244 us	1575	-98.1%		×Fail
5	t _{SU,DAT}	Data Set-up time	250.000 ns		472.837 ns	1.187 us	1.443 us	5.255 us	1767	18.7%		✓Pass
6	t _{SU,STO}	Set-up time for STOP condition							0			
7	t _{LOW}	Low Period of the SCL Clock	4.700 us		1.539 us	1.541 us	1.543 us	9.208 ns	2670	-67.3%		×Fail
8	t _{HIGH}	High Period of the SCL Clock	4.000 us		977.699 ns	979.666 ns	984.826 ns	20.914 ns	3040	-75.6%		×Fail
9	t _{rCL}	Rise time of SCL signal		1.000 us	45.022 ns	48.118 ns	49.835 ns	14.531 ns	3430		0.5%	✓Pass
10	t _{fCL}	Fall time of SCL signal		300.000 ns	9.888 ns	10.237 ns	10.583 ns	1.448 ns	3430		0.2%	✓Pass
11	t _{rDA}	Rise time of SDA signal		1.000 us	37.719 ns	39.529 ns	41.848 ns	5.148 ns	927		0.4%	✓Pass
12	t _{fDA}	Fall time of SDA signal		300.000 ns	4.616 ns	6.893 ns	9.828 ns	24.035 ns	947		1.8%	✓Pass
13	t _{BUF}	Bus free time between a STOP and START condition							0			
14	t _{VD,DAT}	<u>Data valid time</u>		3.450 us	98.898 ns	270.164 ns	1.067 us	4.200 us	1585		28.9%	✓Pass
15	t _{VD,ACK}	Data valid acknowledge time		3.450 us	141.017 ns	730.257 ns	1.067 us	1.344 us	91		28.0%	✓Pass
16	VIL	Low-level input voltage	-500.000 mV	990.000 mV	-105.670 mV	27.063 mV	104.081 mV	760.863 mV	4367	26.5%	40.5%	✓Pass
17	V _{IH}	<u>High-level input voltage</u>	2.310 V	3.800 V	3.225 V	3.267 V	3.417 V	1.250 V	4367	61.4%	74.3%	✓Pass

f_{SCL} - Test Result: Fail Description: SCL clock frequency

Limit Min Limit Max Min	Mean Max Sta	andard Deviation	n Count Margin Min	Aargin Max			
0.000 Hz 100.000 KHz 387.586 KHz	387.683 KHz 387.769 KHz 437	7.000 Hz	2670 387.6%	87.8%	-		
	Histogram	1					
Occurance (%), Total 2670			Value Range	Occurance Coun	t		
100 -			387.586 kHz ~ 387.604 kHz	9			
90 -			387.604 kHz ~ 387.623 kHz	23			
70			387.623 kHz ~ 387.641 kHz	84			
60 - 50 -			387.641 kHz ~ 387.659 kHz	395			
40 -			387.659 kHz ~ 387.677 kHz	539			
20.2	23.7 24.8		387.677 kHz ~ 387.696 kHz	632			
10 0.3 0.9 3.1	8.0 3.5 0.7	Test Value	387.696 kHz ~ 387.714 kHz	663			
387.586 KHz	387	.769 KHz	387.714 kHz ~ 387.732 kHz	213			
Test Value		KHz (387.8%)	387.732 kHz ~ 387.751 kHz	94			
Limit 0.000 Hz	100	.000 KHz	387.751 kHz ~ 387.769 kHz	18			
Min	Detail Repor	rt Row: 12, Test	t Index: 197 Max			Detail Rep	ort Row: 10, Test Index: 82
500 mV 2 500 mV 3 500 mV -3.50 2 -3.50 3 -3.50	400 ns -3.50 Η 400 ns -730.2 μs	I2C Validation Stop S/R: 500 M	AS/s 50	0 mV 2 500 m 50 -3.50	V 3 500 mV 4 500 n -3.50 4 -3.50	nV H 400 ns -345.866 µs	I2C Validation Stop S/R: 500 MS/s
						-	
						1	
						<u> </u>	
						÷ /	
ու իս փոփոփով ու անդու փոփոփոփոփոփոփոփոփոփոփո							
197	62	197	120		82	7E	less line
	+					+	
			I				
						-	



I2S 电气特性验证解决方案

■ 简介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器执行 I2S 电气特性验证,以确保 I2S 符合既定规格。在经过长时间的持续运行测试后,可以确认所测试的信号电气特性符合规范。

I²S(Inter-IC Sound)是一种标准的串行总线接口,用于连接数字音频装置,例如音频编码器、数字模拟转换器(DAC)与模拟数字转换器(ADC)。它常见于嵌入式系统、音频处理器与高质量音频设备中。

I²S 是一种结构简单但功能强大的接口,可在装置之间以高精度、低延迟地传送数字音频数据。



■ I2S 电气特性验证设置

1. 一般设置:设置总线配置,包括 I2S 模式类型(I2S、Left Justified、

PCM、TDM)、通道设置、工作电压与数据速率。

Settings		Import	Export
→General	Channel Settings		
XTrigger XValidation	Mode: 12S • SCK: DS0 Channel 1 • • WS: DS0 Channel 2 • • SD: DS0 Channel 3 • • Probe Settings: x10 • • SD: DS0 Channel 3 • •		
	Working Voltage(V _{b0}): 3.30 V		
Default			Next

2. 解码设置:设置 I2S 数据格式。位顺序可选择 MSB First 或 LSB First。数

据位数可设置为 1 到 32 位之间。

tings						Import	Export
General	Data Format						
Trigger Validation	Bit Order Data Bits	MSB First 16 bits	• •				



1. 触发设置: 设置用户需要触发的数据模式。数据格式已在前一页的解码设置中设置完成,其余设置仅与数据模式相关。此处共提供 6 种触发方

式: Data Match, Rising, Falling, Glitch, Mute, and Clip。

Settings			Import Export
✓General	Data		
 Trigger Walidation 	Method	Data Match 👻	
▲Validation	Channel Pattern	Both	
		0000h	
	Duration	1 frame(s)	
Default			Previous Next

4. 验证参数设置

ll –	/ Customized	2) Paramatar		
e "	Customized	ev Farameter.		
	Freque	ncy		
on	Name	Description	Min	Max
	1 ✔ f _{SCK} SC	CK Frequency	2.25 MHz	2.75 MHz
			2	
	Time			
	Name	Description	Min	Max
	1 ✔ t _{HC}	SCK High Period	140 ns	x
	2 ✔ t _{LC}	SCK High Period	140 ns	x
	3 ✔ t _R	SCK Rise Time	X	60 ns
	4 √ t _F	SCK Fall Time	Х	60 ns
	5 ✔ t _{d,SCK}	wsSCK-WS Delay Time	х	320 ns
	6 ✔ t _{d,SCK}	so SCK-Data Delay Time	x	320 ns
	7 ✔ t _{dutyS}	K SCK Duty Cycle	x	x
	8 ✔ t _{s,WS}	WS Setup Time	X	80 ns
	9 ✔ t _{h,WS}	WS Hold Time	0 ns	x
	10 ✔ t _{dutyW}	WS Duty Cycle	X	x
	11 ✔ t _{s,SD}	Data Setup Time	x	80 ns
				-



此部分提供三张特性参数表,包含:

- 频率
- 时序参数
- 电压要求

默认值参考自 I2S 规范 Rev3.0。下方列出所有支持的验证参数符号与说明:

• I2S Frequency Requirements

Symbol	Electrical Parameter
f _{SCK}	SCK Clock Frequency

• I2S Timing Requirements

Symbol	Electrical Parameter
t _{HC}	SCK High Period
t _{LC}	SCK Low Period
t _R	SCK Rise Time
t- _F	SCK Fall Time
t _{d,SCKWS}	SCK-WS Delay Time
t _{duty,SCK}	SCK Duty Cycle
t _{s,WS}	WS Setup Time
t _{h,WS}	WS Hold Time
t _{duty,WS}	WS Duty Cycle
t _{s,SD}	Data Setup Time
t _{h,SD}	Data Hold Time

• I2S Voltage Requirements

Symbol	Electrical Parameter
VL	Low-Level Voltage
V _H	High-level Voltage



5. 电气特性验证_软件画面



6. 控制面板



A. 停止条件:

当采集达到 X 次时停止 当测试结果失败超过 X 次时停止

B. 信息: 选择查看波形

C. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)



7. 概览报告



8. 详细报告

1	2 V +1.53			2 V -0.97				3 2 V -3.50					Н 20 µs -80 µ	s T	I2S Valid Stop S/	ation 'R: 250 MS/	<u>s</u>
1					n N												
2				n y y y y y y y y y y y y y y y y y y y				┍┥┥┥┍╼┥┥ ┥╷╵┝┯╌╸	┙┙┿┍╺┍┍ ┍ ┍					100 P			
12S					9) 11 22/00 	in an	L R L L I					 ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		21 <mark>8</mark> (121)			
Over	view Detail	128															
^L R	Vaveform No	TimeStamp	s t _{hows} Data	Limit Min	Limit Max	Min	Mean	Max	Count	Result							-
1	1-1	300.000 ns	R: 8000		60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass							_
2	1-2	350.000 ns	L: 8000		60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass							
3	1-3	450.000 ns	R: 8000		60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass							
4	1-4	550.000 ns	L: 8000		60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass							
5	1-5	650.000 ns	R: 8000		60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass							
6	1-6	750.000 ns	L: 0000		60.000 ns	1.719 ns	1.727 ns	1.743 ns	4	Pass							
7	1-7	1.150 us	R: 0000		60.000 ns	1.743 ns	1.743 ns	1.743 ns	1	Pass							
8	1-8	1.250 us	L: 0000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass							
9	1-9	1.350 us	R: 0000		60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass -							
10	1-10	1.450 us	L: 0000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass							
11	1-11	1.550 US	R: 8000		60.000 ns	1.719 hs	1.719 hs	1.719 ns	1	Pass							
12	1-12	1.050 US	D: C000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	2	Pass							
13	1-13	1.750 US	K. C000		00.000 ns	1.750 hs	1.750 hs	1.750 hs	2	Fass							



9. 波形和参考点

1	2 V +1.53			2 2 V -0.97				3	2 V -3.50							H 40 ns +17.104 µs	T I2S Validation Stop S/R: 250	MS/s
1					ſ													
2							·····								······			
125							R:80	00							1		L:0000	
3									💿 Detail t_{h.SD}		Ţ						×	
Over	view Detail	128							Wave	form No.	TimeSt	amp	Data	Limi	t Min	Limit Ma	x	
t _R	t _{d,SCKWS} t	l _{a,sokso} t _{a,wi}	s t _{h.ws}	t _{s,SD} t _{h,SD}				_		7	750.000	ins i	L: 0000	0.00	0 ps			
1	Naveform No	TimeStamp	Data P: 8000	Limit Min	Limit Max	Min	Mean		1 (2.799	ume µs, 2.998 µs)	198.516	ns (2.31	V, 2.31 V)	0 V	Pass		_	^
2	1.2	350.000 ns	1 . 8000	0.000 ps														
3	1-3	450.000 ns	R: 8000	0.000 ps														
4	1-4	550.000 ns	L: 8000	0.000 ps														
5	1-5	650.000 ns	R: 8000	0.000 ps														
6	1-6	750.000 ns	L: 0000	0.000 ps		198.516 ns	198.516 ns	19										
7	1-7	1.150 us	R: 0000	0.000 ps														
8	1-8	1.250 us	L: 0000	0.000 ps														
9	1-9	1.350 us	R: 0000	0.000 ps														
10	1-10	1.450 us	L: 0000	0.000 ps												×	Close	
11	1-11	1.550 us	R: 8000	0.000 ps		198.369 ns	198.369 ns	198	.369 ns	1	Pass							
12	1-12	1.650 us	L: 8000	0.000 ps			-											
13	1-13	1.750 us	R: C000	0.000 ps														-



10. Html 报告



Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 13:34:37
S/W Version	1.8.62
Protocol	128

Overview Results:

t_R - Test Result: Pass Description: SCK Rise Time

Total:	7
Pass:	5
Fail:	2

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	t _R	SCK Rise Time		60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994		-95.0%	✓Pass
2	t _{d,SCKWS}	SCK-WS Delay Time		320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390		-36.4%	✓Pass
3	t _{d,SCKSD}	SCK-Data Delay Time		320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375		-36.3%	✓Pass
4	t _{s,WS}	WS Setup Time		80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377		148.1%	≍Fail
5	t _{h,WS}	WS Hold Time	0.000 ps		197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390			✓Pass
6	t _{s,SD}	Data Setup Time		80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375		147.9%	≍Fail
7	t _{h,SD}	Data Hold Time	0.000 ps		197.737 ns	198.588 ns	199.651 ns	295.000 ps	375			✓Pass

Limit Min Limit Max Min Mean Max Standard Deviation Count Margin Min Margin Max 60.000 ns 1.639 ns 2.062 ns 2.990 ns 442.000 ps 95.0 Histogram Value Range Oc 1.639 ns ~ 1.774 ns | 1283 100 90 80 70 60 50 40 30 1.774 ns ~ 1.909 ns 578 1.909 ns ~ 2.044 ns 439 2.044 ns ~ 2.179 ns 210 2.179 ns ~ 2.314 ns 84 2.314 ns ~ 2.450 ns 80 2.450 ns ~ 2.585 ns 112 2.585 ns ~ 2.720 ns 147 2.720 ns ~ 2.855 ns 167 60.000 ns 2.855 ns ~ 2.990 ns 393 Detail Report Row: 1337, Test Index: 1 Max Detail Report Row: 765, Test Index: 3 Min 2 V +1.53 H 1 ns -59.196 µs 1 ns -134.4 µs 2 V 0 01 1 1 3



MIPI I3C 电气特性验证解决方案

■ 简介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

MIPI I3C 向下兼容许多传统 I2C 装置,但同时 I3C 装置还支持更高速传输速率(SCL 时钟 频率可达 12.5 MHz)及全新的通信模式。MIPI I3C 工作模式包含 Single Data Rate (SDR) Mode, High Data Rate (HDR) Mode. HDR Mode 进一步细分为 Dual Data Rate (HDR-DDR) Mode, Ternary Symbol Legacy Mode (HDR-TTL) Mode, Ternary Symbol Pure-bus (HDR-TSP) Mode, Bulk Transport (HDR-BT) Mode.

MIPI I3C 电气特性验证提供多项符合 MIPI I3C 规格的电气测量项目(目前支持 MIPI I3C 版本 1.1.1)。



MIPI I3C Electrical Validation Settings:

1. 一般设置: 设置通道来源、工作电压与传输速率。

Settings	Import	rt
→General	Channel Settings	
 Decode Trigger Validation 	SCL: DSO Channel 1 Probe Settings: x10 SDA: DSO Channel 2 Probe Settings: x10	
	Working Voltage(V _{DD}): 1.80 V	
	 SDR: Single Data Rate Mode (Max: 12.5 Mbps) HDR-DDR: HDR Double Data Rate Mode (Max: 25 Mbps) HDR-TSL: Tenary Symbol Legacy-inclusive-bus Mode (Max: 27.5 Mbps) HDR-TSP: HDR Tenary Symbol for Pure-bus Mode (Max: 39.5 Mbps) HDR-BT: HDR Bulk Transport Mode Customized Speed 400 Kbps 2 	
	Bus Configuration	
	 Pure Bus: Only I3C devices are presented on the I3C Bus Mixed Bus: At least one I2C Legacy Device is presented on the I3C Bus 	
	Communicating with I2C Legacy Device	
	 Fast Mode (400 Kbps) Fast Mode+ (1 Mbps) 	
Default	Next	

在此部分中,所选的速度模式会影响验证所需的采样率,同时也会影响后续「验证设置」 部分中的时序规格表。例如,在 HDR-TSL 与 HDR-TSP 模式下,将额外显示专属的时序规 格。

13 ✔ t _{EDGE}	Edge-to-Edge Period	32 ns	х
14 ✔ t _{skew}	Allow Difference Between Signals for 'Simultaneous' Change	х	12.8 ns
15 ✔ t _{EYE}	Stable Condition Between Signals	12 ns	х
16 ✓ t _{SYMBOL}	Time Between Successive Symbols	32 ns	х
17 ✓ t _{сьоск}	Symbol Clock	77.5 ns	x

此外,在「Bus Configuration」中需指定总线上连接的装置类型:

- 纯 I3C 总线 (Pure-Bus): 不需要 I2C 时序规格。
- **混合总线(Mixed Bus):** 需加入 I2C 兼容装置的时序规格,默认值采用 Fast Mode
 (Fm)或 Fast Mode+(Fm+)设置,与 I2C 验证设置相同。



2. 解码设置

ettings		Import Export
General	Startup	
Trigger Validation	 Startup in I2C mode PEC Enabled Startup in HDR-DDR mode 	

3. 触发设置

ess: XXh mon Command Code (CCC	C): XXh, Any		

若需要分析特定装置地址,可设置特定地址为触发条件。如图中 "XX" 表示「任意」的 位,将会触发所有地址。此外亦支持针对常用命令码(CCC)的触发,可透过广播地址 7'h7E 指定。



4. 验证参数设置

0.00				
ode	Customized EV F	Parameter:		
ger dation		¢y		
	Name	Description	Min	Max
	1 ✔ f _{SCL} SC	L Clock Frequency when communicating with I2C Legacy Devices	0 MHz	0.4 MHz
	2 ✔ f _{SCL_PP} SC	L Clock Frequency	0.01 MHz	12.9 MHz
	Time (Wh	hen Communicating With I2C Legacy Devices)		
	Name	Description	Min	Max
	1 ✓ t _{SU_STA} S	etup Time for a Repeated START	600 ns	X
	2 ✔ t _{HD_STA} H	old Time for a (Repeated) START	600 ns	х
	3 ✔ t _{LOW} S	CL Clock Low Period	1300 ns	x
	4 ✔ t _{DIG_L} S	CL Clock Low Period as seen at the receiver	1320 ns	x
	5 🗸 t _{HIGH} S	CL Clock High Period	600 ns	x
	6 ✔ t _{DIG_H} S	CL Clock High Period as seen at the receiver	606.55 ns	х
	7 7 1 0	ata Setup Time	100 ns	x
			X	x
	8 V t _{HD_DAT} D	lata Hold Time		300 ns
	8 ✓ t _{HD_DAT} D 9 ✓ t _{rCL} S	CL Signal Rise Time	20 ns	000110

本部分共包含五种参数表:

- Frequency
- I3C timing requirements when communicating with I²C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

若为纯 I3C 总线,则不会显示与 I2C 装置相关的时序表,也不会显示 fscl 频率参数。



MIPI I3C Frequency Requirements

Symbol	Electrical Parameter
f _{SCL}	SCL Clock Frequency when communicating with I ² C Legacy Devices ¹
t _{SCL_PP}	SCL Clock Frequency
t _{bt_freq}	HDR-BT SCL Clock Frequency

MIPI I3C Timing Requirements When Communicating With I²C Legacy Devices¹

Symbol	Electrical Parameter
t _{su_sta}	Setup Time for a REPEATED START
t _{HD_STA}	Hold Time for a (REPEATED) START
t _{LOW}	SCL Clock Low Period
t-dig_l	SCL Clock Low Period as seen at the
	receiver
t _{нібн}	SCL Clock High Period
t _{DIG_H}	SCL Clock High Period as seen at the
	receiver
t _{su_dat}	Data Setup Time
t _{HD_DAT}	Data Hold Time
t _{rCL}	SCL Signal Rise Time
t- _{fCL}	SCL Signal Fall Time
t _{rDA}	SDA Signal Rise Time
t- _{rDA_OD}	SDA Signal Rise Time (Open Drain)
t- _{fDA}	SDA Signal Fall Time
tsu_sto	Setup Time for STOP
t- _{BUF}	Bus Free Time Between a STOP and a
	START
tspike	Pulse Width of Spikes that Spike Filter
	Must Suppress

¹ Only available when the bus configuration is set to Mixed Bus (i.e. at least one I²C legacy device is presented on the I3C bus).



Symbol	Electrical Parameter
tlow_od	SCL Clock Low Period
t _{DIG_OD_L}	SCL Clock Low Period as seen at the receiver
t _{HIGH_INIT}	High Period of SCL Clock (for First Broadcast Address)
t- _{HIGH_OD}	SCL Clock High Period
t _{DIG_OD_H}	SCL Clock High Period as seen at the receiver
t _{fDA_OD}	SDA Data Fall Time
t _{su_od}	SDA Data Setup Time During Open Drain Mode
t _{CAS}	Clock After START (S) Condition
t _{CBP}	Clock Before STOP (P) Condition
t-CRHPOverlap	Active Controller to Secondary Overlap time during handoff
t _{AVAL}	Bus Available Condition
t-idle	Bus Idle Condition
t _{NEWCRLock}	Time Interval Where New Controller Not Driving SDA Low

MIPI I3C Open Drain Timing Requirements



Symbol	Electrical Parameter					
t _{LOW}	SCL Clock Low Period					
t _{DIG_L}	SCL Clock Low Period as seen at the receiver					
t _{HIGH} SCL Clock High Period						
t _{DIG_H}	SCL Clock High Period as seen at the receiver					
t _{sco}	Clock in to Data Out for Target					
t _{cr_pp}	SCL Clock Rise Time					
t _{CF_PP}	SCL Clock Fall Time					
$t_{HDPP_Controller}$	SDA Signal Data Hold (Controller)					
t-HD_PP_Target	SDA Signal Data Hold (Target)					
t _{su_pp}	SDA Signal Data Setup					
t- _{CASr}	Clock After Repeated START (Sr) Condition					
t _{CBSr}	Clock Before Repeated START (Sr) Condition					
t _{BT_HO}	HDR-BT Master to Slave Hand Off Delay					
t _{BT_STALL}	HDR-BT Clocked Not-Ready Data-Block Headers					

MIPI I3C Push-Pull Timing Requirements



MIPI I3C I/O Stage Characteristics Voltage Req	uirements
--	-----------

Symbol	Electrical Parameter
V _{IL}	Low-Level Input Voltage
VIH	High-level Input Voltage
V _{OL}	Low-level Output Voltage
V _{OH}	High-level Output Voltage



5. 电气特性验证_软件画面





MIPI RFFE 电气特性验证解决方案

■ 简介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
Electrical	Open						
Validation	EV File						

MIPI RFFE(Radio Frequency Front-End)是由 MIPI 联盟所制定的标准规范,用以定义移动装置(如智能型手机和平板电脑)中基带处理器与射频前端模块之间的通信标准。这是 MIPI (Mobile Industry Processor Interface)标准家族的重要组成部分,涵盖多种针对移动与嵌入式设备中组件之间通信效率所设计的标准。

MIPI RFFE 是现代无线设备的关键技术,提供一个标准化且高效的接口,用于控制无线通 信系统中的射频前端组件。



■ MIPI RFFE 电气特性验证设置:

1. 一般设置:设置通道来源、工作电压、频率范围、Test Point 和 Read

Operation .

EV Electrical Validatio	n		×
12C	Settings		Import Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	→ General ★ Trigger ★ Validation	Channel Settings SCLK: DSO Channel 1 Probe Settings: x10 Probe Se	

2. 触发设置

EV Electrical Validation		×
I2C Settings		Import Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232) ↓Validation Default	Command Sequence Type: Any Command Register Address (Lower): XXh Register Address (Upper): XXh Otata • Any Offset • Fixed Offset 0 Byte(s) Data 1 Xh Data 5 Xh Data 2 Xh Data 3 Xh Data 4 Xh Data 8	Previous Next



3. 验证设置: 包含电压、时序与频率的限制条件

EV Electrical Validation	n				
I2C	Settings				Import Export
I2S MIPI I3C MIPI REFE	✓General✓Trigger	Customized EV Parameter:			
MIPI SPMI PDM	Validation	Frequency			
SPI		Name	Description	Min	Max
UART(RS232)		1 ✔ f _{SCLK} SCLK Frequency		0.032 MHz	26 MHz
		► Time (Full-Speed O	perations)		
		Time (Half-Speed D	ata Response Operations)		
		Name	Description	Min	Max
		1 V t _{SCLKOH_HSDR} (HSDR) Clock (Output High Time	28.1 ns	X
		2 V t _{SCLKOL_HSDR} (HSDR) Clock (Output Low Time	28.1 ns	X
		3 ✓ t _{SCLKOTR_HSDR} (HSDR) Clock (Output Transition (Rise/Fall) Time	3.5 ns	6.5 ns
		4 ✓ t _{SU_M_Rd_HSDR} (HSDR) SDATA	Setup Time, with respect to SCLK Output - BOM - Read	3.75 ns	×
		5 ✓ t _{H_M_Rd_HSDR} (HSDR) SDATA	Hold Time, with respect to SCLK Output - BOM - Read	6.75 ns	×
		∠ Voltage			
		Name	Description	Min	Max
		1 ✔ V _{Low} Low-Level Voltage		0 V	0.36 V
		2 ✔ V _{High} High-Level Voltage		1.44 V	1.8 V 💌
	Default	Advance			Previous Apply

4. 电气特性验证_软件画面





5. 控制面板



A. 停止条件: 当采集达到 X 次时停止 当测试结果失败超过 X 次时停止

B. 信息: 选择查看波形

C. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)

6. 概览报告

1 2V -1.12			2 2 ² -0	V 05						H 200 ns MIPI RFFE Validation +4.812 ns Sing <u>SiR: 500 MS/s</u>
	,			بر المراجع الم المراجع المراجع				Dea: 03		1 1
Overview [Detail MIPI RFI	FE	Linck Mary	A.C.	Mara	Mari	and and Day int	Count	Devila	
1 fscl.k	SCLK Fre	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	Fail	
2 tscl.koh	Clock Out	4.700 ns		6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	Pass	
3 tscl.kol	Clock Out	4.700 ns		8.329 ns	41.946 ns	1.563 us	196.252 ns	230	Pass	
4 tsclkotr	Clock Out	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail	-
5 tscl.kiH	Clock Inpu							0		
6 tscl.kil	Clock Inpu							0		
7 tsclaitr	Clock Inpu							0		
8 t _{SKEW_M}	SDATA Sk	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95	Fail	
9 SDATAOTR_M	SDATA Ou	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail	
10 t _{PD_S_R}	Time for s							0		
11 ISDATAOTR_S_SR	sRead SD							0		



7. 详细报告



8. 波形和参考点





8.4%

-55.0%

✓Pass
 ✓Pass
 ×Fail

9. Html 报告

Acute. **Electrical Validation Report** Test Instrument Model MS03124V st Instruments Serial Number Test Date S/W Version Protocol MSV31240021 12-09-2024 15:32:11 1.8.62 MIPI RFFE **Overview Results:** Total: 33 Pass: 2 Fail: 6 26.000 MHz 52.000 MHz 49.200 MHz 52.209 MHz 56.354 MHz 2.244 MHz CLK Frequency 220 89.2% 6.413 ns 7.501 ns 9.281 ns 714.000 ps 8.329 ns 41.946 ns 1.563 us 196.252 ns 743.000 ps 1.088 ns 1.799 ns 204.000 ps lock Output High Time lock Output Low Time 4.700 ns 4.700 ns 230 36.4% 230 77.2% 4.000 ns 2.100 ns 460 -64.6% Clock Output Transition (Rise/Fall) t_{SCLKIH} ock Input High Time 0 ----

× 1	SCEKIE	olock linder cow time							r 1			
7	t _{SCLKITR}	Clock Input Transition (Rise/Fall) Time							0			
8	t _{skew_m}	SDATA Skew Relative to SCLK, BOM Master Output	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95		4368.2%	×Fail
9	t _{SDATAOTR_M}	SDATA Output Transition (Rise/Fall) Time, BOM Master	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	×Fail
10	t _{PD_S_sR}	Time for sRead Data Output Valid from SCLK Rising Edge - Slave							0			
11	tSDATAOTR_S_SR	sRead SDATA Output Transition (Rise/Fall) Time - Slave							0			
12	tsu_M_Rd	SDATA Setup Time, with respect to SCLK Output - BOM - Read							0			
13	t _{H_M_Ra}	SDATA Hold Time, with respect to SCLK Output - BOM - Read							0			
14	t _{su_M_≉R}	SDATA Setup Time, with respect to SCLK Output - BOM - sRead							0			
15	t _{H_M_sR}	SDATA Hold Time, with respect to SCLK Output - BOM - sRead							0			
16	t _{su_s}	SDATA Setup Time, with respect to SCLK Input - Slave (or non-BOM)							0			
17	t _{H_S}	SDATA Hold Time, with respect to SCLK Input - Slave (or non-BOM)							0			
18	t _{SCLKOH_HSDR}	(HSDR) Clock Output High Time							0			
19	t _{SCLKOL_HSDR}	(HSDR) Clock Output Low Time							0			
20	t _{SCLKOTR_HSDR}	(HSDR) Clock Output Transition (Rise/Fall) Time							0			
21	t _{SCLKIH_HSDR}	(HSDR) Clock Input High Time							0			
22	t _{SCLKIL_HSDR}	(HSDR) Clock Input Low Time							0			
23	t _{SCLKITR_HSDR}	(HSDR) Clock Input Transition (Rise/Fall) Time							0			
24	tPD_S_Rd_HSDR	(HSDR) Time for Read Data Output Valid from SCLK Rising Edge - Slave							0			
25	tSDATAOTR_S_Rd_HSDR	(HSDR) Read SDATA Output Transition (Rise/Fall) Time - Slave							0			
26	t _{PD_S_SR_HSDR}	(HSDR) Time for sRead Data Output Valid from SCLK Rising Edge - Slave							0			
27	tsdataotr_s_sr_hsdr	(HSDR) sRead SDATA Output Transition (Rise/Fall) Time - Slave							0			
28	t _{SU_M_Rd_HSDR}	(HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read							0			
20		(USDD) SDATA Held Time, with respect to SOLK Output, BOAL Board							0			

f_{SCLK} - Test Result: Fail

Description: SCLK Frequency





MIPI SPMI 电气特性验证解决方案

■ 简介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器执行 MIPI SPMI 电气特性验证,以确保 MIPI SPMI 协议符合既定规格。在经过 长时间持续运行测试后,可确认所测试的信号电气特性是否符合标准。

MIPI SPMI(System Power Management Interface)是由 MIPI 联盟(Mobile Industry Processor Interface)制定的标准规范,主要目的是为了在移动与嵌入式系统中实现电源管理。SPMI 提供标准化的通信接口,用于在电源管理 IC(PMIC)与各个系统组件之间有效 地分配电力移管理电源状态,常见于智能型手机、平板电脑等装置中。



■ MIPI SPMI 电气特性验证设置

1. 一般设置: 设置通道来源、工作电压、传输速率与协议版本。

EV Electrical Validation			>	<
12C	Settings		Import Export	
I2S MIPI I3C MIPI RFFE PDM SPI UART(RS232)	 →General ★Trigger ★Validation 	Channel Settings SCLK: DSO Channel 1 Probe Settings: x10 SDATA: DSO Channel 2 Probe Settings: x10 Working Voltage(V _{DO}): 3.30 Constraints of the set of the s		
	Default		Next	

2. 触发设置

EV Electrical Validation										×
12C	Settings									Import Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	 ✓General →Trigger Xvalidation 	Command Sequence Type: Any Command Slave Address: Xh Register Address: XXXh Data								
		Data 1	XXh	Data 5	XXh	Data 9	XXh	Data 13 XXh		
		Data 2	XXh	Data 6	XXh	Data 10	XXh	Data 14 XXh		
		Data 3	XXh	Data 7	XXh	Data 11	XXh	Data 15 XXh		
		Data 4	XXh	Data 8	XXh	Data 12	XXh	Data 16 XXh		
	Default									Previous Next



3. 验证参数设置: 包含频率、时间与电压限制条件

EV Electrical Validation	n									
12C	Settings				Import Export					
Electrical Validation	 ✓General ✓Trigger 	Customized EV	Parameter:							
	Validation	Frequency								
SPI		Name	Description	Min	Max					
UART(RS232)		1 ✓ f _{SCLK} SCLK	Frequency	32 KHz	26 MHz					
		⊿ Time								
		Name	Description	Min	Max					
		1 ✔ t _{SCLKOH} S	CLK Output High Time	12 ns	X					
		2 ✓ t _{SCLKOL} S	CLK Output Low Time	12 ns	Х					
		3 ✔ t _{SCLKOTR} S	CLK Output Transition (Rise/Fall) Time	2.1 ns	5.3 ns					
		4 ✓ t _{sdataotr} S	DATA Output Transition (Rise/Fall) Time	2.1 ns	5.3 ns					
		5 ✔ t _D S	DATA Output Valid Time	0 us	11 ns					
		6 ✔ t _s S	DATA Setup Time	1 ns	X					
		7 ✔ t _H S	SDATA Hold Time	5 ns	X					
		∠ Voltage	✓ Voltage							
		Name	Description	Min	Max					
		1 ✓ V _L Low-Le	evel Voltage	0 V	360 mV					
		2 ✔ Vy High-I	evel Voltage	1 44 V	18V 🔻					
	Default	Advance			Previous Apply					

4. 电气特性验证_软件画面




5. 控制面板



A. 停止条件: 当采集达到 X 次时停止 当测试结果失败超过 X 次时停止

B. 信息: 选择查看波形

C. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)

6. 概览报告

1	2 V +0.35		a de la companya de la Companya de la companya				Sequence Start	t Condition			El 1 µs 3 846 µs T MIPI SPMI Validation Shop SrR. 500 MS/s 4 40 40 8 03 8 5 44 ER WL A1 40 40 8 03 8	
Ove	erview Det	tail MIPI SPI						1.15.11		D 1		
1 1	SCLK	SCLK Fre	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	Pass		
2 1	SCLKOH	SCLK Out	12.000 ns		41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	Pass		
3 1	SCLKOL	SCLK Out	12.000 ns		41.351 ns	102.355 ns	5.718 us	501.997 ns	340	Pass		
4	SCLKOTR	SCLK Out	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	Fail		
5 1	SDATAOTR	SDATA Ou	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	Fail		
6 1	6	SDATA Ou	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	Fail		
7 1	8	SDATA Se	1.000 ns		26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	Pass		
8 1	a	SDATA Ho	5.000 ns		43.207 ns	195.261 ns	5.299 us	790.518 ns	114	Pass		
9	V.	Low-Level	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340	Pass		
10	V _H	High-Level	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	Fail		



7. 详细报告



8. 波形和参考点

1 2 V +0.35			2 2	V).98										H 10 ns +4.78 µs	MIPI SPMI Valio Stop S/R: 500	dation <u>MS/s</u>
2	1		1 - 1							MEL1 Detail					×	· · · · · · · ·
									ľ	H Waveform No.	Time Stamp	СМД	Limi	t Min	Limit Max	
Overview D	etail MIPI SP	PMI							Ľ	1-1	484.000 ns	31h	1.44	10 V	1.800 V	
fscux tscux	on t _{scikol}	t _{SCLKOTR}	t _{SDATAOTR} t _D	ts t _H	V _L V _H	Moon	Max			Time	∆ Time	Volt	∆ Volt	Result	-	
1 1-1	484.000 ns	31h	1.440 V	1.800 V	3.046 V	3.303 V	3.601 V	67	1	(966.548 ns, 1.010 µs)	43.261 ns	(2.31 V, 2.31 V)	0 V	Fail	_	
2 2-1	277.000 ns	16h	1.440 V	1.800 V	3.039 V	3.328 V	3.700 V	58	2	(1.061 µs, 1.110 µs)	48.762 ns	(2.31 V, 2.31 V)	0.1	Fail		
3 3-1	222.000 ns	31h	1.440 V	1.800 V	2.997 V	3.283 V	3.531 V	105	3	(1.1/2 µs, 1.220 µs)	48.537 hs	(2.31 V, 2.31 V)	0.1	Fall		
4 4-1	1.806 us		1.440 V	1.800 V	3.176 V	3.366 V	3.588 V	13	4	(1.2/1 µs, 1.320 µs)	40.072 fts	(2.31 V, 2.31 V)	0.1	Fail		
5 5-1	537.000 ns	31h	1.440 V	1.800 V	3.067 V	3.379 V	3.623 V	95	6	(1.3/1 µs, 1.420 µs)	40.720 fts	(2.31 V, 2.31 V)	0.V	Fail		
									2	(1.407 µs, 1.500 µs)	43.201 //S	(2.31 V, 2.31 V)	0.V	Fail		
									2	(11 662 us 11 710 us)	40.014 ms	(2 31 V 2 31 V)	0.V	Fail		
									9	(11.761 us. 11.810 us)	48.851 ps	(2.31 V, 2.31 V)	0 V	Fail		
									P		-				× Close	
									-							



Electrical Validation Report

MSO3124V MSV31240021 12-09-2024 14:54:25 1.8.62 MIPI SPMI

9. Html 报告

Ľ.

ased T&M Instruments	
	Electrical Validation
	Test Instrument Model
	Test Instruments Serial Number
	Test Date 1
	S/W Version
	Protocol

Overview Results:

Total: 10 Pass: 6 Fail: 4

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	^f sclk	SCLK Frequency	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	441.6%	-58.9%	✓Pass
2	t _{SCLKOH}	SCLK Output High Time	12.000 ns		41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	245.0%		✓Pass
3	t _{SCLKOL}	SCLK Output Low Time	12.000 ns		41.351 ns	102.355 ns	5.718 us	501.997 ns	340	244.6%		✓Pass
4	t _{SCLKOTR}	SCLK Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	-53.1%	35.0%	× Fail
5	^t SDATAOTR	SDATA Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	-53.6%	-63.5%	× Fail
6	t _D	SDATA Output Valid Time	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114		48997.2%	×Fail
7	ts	SDATA Setup Time	1.000 ns		26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	2569.4%		✓Pass
8	t _н	SDATA Hold Time	5.000 ns		43.207 ns	195.261 ns	5.299 us	790.518 ns	114	764.1%		✓Pass
9	VL	Low-Level Voltage	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340		-21.2%	✓Pass
10	V _H	High-Level Voltage	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	108.1%	105.5%	≍Fail

f_{SCLK} - Test Result: Pass Description: SCLK Frequency





PDM 电气特性验证解决方案

■ 简介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation E	Open V File						

使用示波器执行 PDM (Pulse Density Modulation) 电气特性验证,以确保其信号符合既定 电气标准规格。在经过长时间持续运行测试后,可以确认待测信号的电气特性是否满足标 准要求。

PDM 协议的电气特性检测通常分为两大类:

- 垂直属性(电压)
- 水平属性(时间/相位)

因此,使用此功能时,必须先设置所选的协议与测试规范,并透过重复测试来取得电气特性报告。测试项目会根据 PDM 传输速率而有所不同。

DIGITAL AUDIO INTERFACE						
PDM_CLK High Frequency Range	fclкн		5.28	8.64	MHz	
PDM_CLK Low Frequency Range	f _{CLKL}		1.84	4.32	MHz	
PDM_CLK High Time	^t PDM_CLKH		40		ns	
PDM_CLK Low Time	tPDM_CLKL		40		ns	

常用 PDM 规格中的部分电气特性项目参数:



常用 PDM 验证报告内容:

0	verview	Deta	ail PDM									
	Name		Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result	
1	f _{CLK}		Clock freq	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass	
2	t _{LOW}		Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3	t _{HIGH}		High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4	t _{iCL}		Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5	t _{fCL}		Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6	t _{fDD}		Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7	t _{rDV}		Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8	t _{rDD}		Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9	t _{rDV}		Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	

电气特性验证_软件画面:



- 1. 频率:时钟频率(Clock Speed)
- 时序参数:建立时间(Set-up Time)、保持时间(Hold Time)、上升时间(Rise Time)、下降时间(Fall Time)与时钟拉伸(Clock Stretching)时间限制
- 3. 电压参数: V_IL (输入低电位)、V_IH (输入高电位) 等



拉伸:

Symbol	Electrical Parameter
f _{SCL}	PDM_CLK Frequency Range

时间:

Symbol	Electrical Parameter
t _{LOW}	Low Period of the Clock
t _{ніGH}	High Period of the Clock
t _{rCL}	Rise time of Clock signal
t- _{fCL}	Fall time of Clock signal
t _{rDD}	Delay time from Clock edge to Data Rise driven
t _{fDD}	Delay time from Clock edge to Data Fall driven
t _{rDV}	Delay time from Clock edge to Data Rise valid
t _{fDV}	Delay time from Clock edge to Data Fall valid

电压:

Symbol	Electrical Parameter
V _{ClkLow}	Low-level Input voltage for clock
V _{ClkHigh}	High-level Input voltage for clock
V _{DataLow}	Low-level Input voltage for data
$V_{DataHigh}$	High-level Input voltage for data



■ PDM 电气特性验证设置

1. 一般设置: 设置通道来源、工作电压与传输速率。

Settings	
General	
*Decode	Channel Settings
×Validation	CLK: DSO Channel 1 V Probe Settings: x10 V
	DATA: DSO Channel 2 V Probe Settings: x10 V
	Working Voltage(V _{DD}): 1.80 V
	PDM Clock Speed: 3072 - KHz
Default	Next

2. 解码设置: 设置 PDM 解码参数

Settings											
✓General →Decode	Audio Settings										
×Validation	Decimation Rate: x64 Audio Frequency 48 KHz										
	Mono & Stereo										
	Mode: Stereo 💌										
Default		Previous Next	ן								



3. 验证参数设置:频率、时序与电压限制条件

on Frequency					
Name	Description	Min	Max		
1 ✓ f _{CLK} Clock frequent	су	0 kHz	3.072 MHz		
∠ Time					
Name	Description	Min	Max		
1 ✓ t _{LOW} Low Period of	f the Clock	130.208 ns	195.312 ns		
2 ✓ t _{HIGH} High Period o	f the Clock	130.208 ns	195.312 ns		
3 ✓ t _{rcL} Rise time of 0	CLK signal	Х	13 ns		
4 ✓ t _{rcL} Fall time of C	LK signal	X	13 ns		
5 ✔ t _{rop} Delay time fro	om Clk edge to Data Rise driven	40 ns	80 ns		
6 ✔ t _{rop} Delay time fro	om Clk edge to Data Fall driven	40 ns	80 ns		
7 ✓ t _{rDV} Delay time fro	om Clk edge to Data Rise Valid	Х	100 ns		
8 ✔ t _{rDV} Delay time fro	om Clk edge to Data Fall Valid	Х	100 ns		
✓ Voltage					
Name	Description	Min	Max		
1 ✓ V _{CIkLow} Low-level i	nput voltage for clock	-0.5 V	0.54 V		
2 ✓ V _{ClkHigh} High-level	input voltage for clock	1.26 V	2.3 V		
3 ✓ V _{DataLow} Low-level i	nput voltage for Data	-0.5 V	0.54 V		
4 ✓ V _{DataHigh} High-level	input voltage for Data	1.26 V	2.3 V		

4. 电气特性验证_软件画面





5. 控制面板



A. 停止条件: 当采集达到 X 次时停止 当测试结果失败超过 X 次时停止

B. 信息: 选择查看波形

. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)

6. 概览报告

1 500 mV -3.50	2 5	00 mV 3.50				н	1 µs -328 ns	T PDM Vali Stop <u>S/I</u>	dation R: 500 MS/s	
POM D'O'B						2 6 0 0000000 0 0 6	6 6 6 000000 0 0 0			
Overview [Detail PDM	Limit Min	Limit Max	Min	Moon	Max	ndard Daviat	Count	Dogult	-
1 f _{CLK}	Clock freq	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass	
2 tLow	Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3 [†] ніон	High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4 tra	Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5 ticL	Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6 t _{roo}	Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7 t _{rDV}	Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8 t _{rDD}	Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9 t _{rDV}	Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	-
<u></u>			-							



7. 详细报告

	500 mV -3.50	2 ⁵¹ -3	00 mV .50				Н	1 µs -328 ns	T PDM Valio	lation <u>:: 500 MS/s</u>
							2 0 0	9 6 9	8 9 0	
PDM 1 Over	IDDIIIIO IDDIIIIO IView Det	ail PDM						010 0100 6 7 8		
fcuk	t _{LOW}									
N		t _{HIGH} t _{rCL}	t _{ICL} t _{IDD}	t _{rDV} t _{rD}	t _{rDV}	V _{ClkLow} V _{Data}	Low V _{ClkHigh}	V _{DataHigh}		
	Vaveform No	t _{HIGH} t _{rCL}	t _{rCL} t _{rDD}	t _{rDV} t _{rD}	D t _{rDV}	V _{ClkLow} V _{Data}	_{aLow} V _{Cliéfligh} Max	V _{DataHigh} Count	Result	
1 1	Vaveform No 1-1	t _{HIGH} t _{rCL} TimeStamp 81.316 us	t _{ICL} t _{IDD}	t _{rDV} t _{rD} Limit Max 3.072 MHz	D t _{rov} V Min 3.027 MHz	V _{CIKLow} V _{Date} Mean 3.030 MHz	Max 3.033 MHz	V _{DataHigh} Count 443	Result Pass	×
1 1 2 2	Vaveform No 1-1 2-1	t _{HIGH} t _{rCL} TimeStamp 81.316 us 81.316 us	t _{RCL} t _{RDD} Limit Min 0.000 Hz 0.000 Hz	t _{rDV} t _{rD} Limit Max 3.072 MHz 3.072 MHz	t _{rDV} N Min 3.027 MHz 3.028 MHz	V _{CIKLow} V _{Data} Mean 3.030 MHz 3.030 MHz	ALOW VCINHigh Max 3.033 MHz 3.033 MHz	V _{DataHigh} Count 443 443	Result Pass Pass	*
1 1 2 2 3 3	Vaveform No 1-1 2-1 3-1	tHIGH t _{FCL} TimeStamp 81.316 us 81.316 us 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	t _{IDV} t _{rD} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz	t _{rDV} N Min 3.027 MHz 3.028 MHz 3.028 MHz	V _{CIH.ow} V _{Date} Mean 3.030 MHz 3.030 MHz 3.030 MHz	Low V _{Cliftigh} Max 3.033 MHz 3.033 MHz 3.034 MHz	V _{DataHigh} Count 443 443 443	Result Pass Pass Pass	
1 1 2 2 3 3 4 4	Vaveform No 1-1 2-1 3-1 1-1	t _{HIGH} t _{FCL} TimeStamp 81.316 us 81.316 us 81.316 us 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	t _{IDV} t _{rD} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	trov Min 3.027 MHz 3.028 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz	V _{CIH.on} V _{Dat} Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Vcliefigh Max 3.033 MHz 3.033 MHz 3.034 MHz 3.032 MHz	V _{DataHigh} Count 443 443 443 443	Result Pass Pass Pass Pass	
1 1 2 2 3 3 4 4 5 5	Vaveform No 1-1 2-1 3-1 1-1 5-1	tHIGH trcL TimeStamp 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us	t _{CL} t _{DD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	t _{rov} t _{ro} Limit Max 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	trov N Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.028 MHz 3.029 MHz	VCINLOW VData Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Kon V Cliffigh Max 3.033 MHz 3.033 MHz 3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz 3.032 MHz	VDatatifigh Count 443 443 443 443 443 443	Result Pass Pass Pass Pass Pass	
1 1 2 2 3 3 4 4 5 5 6 6	Vaveform No 1-1 2-1 3-1 1-1 5-1 5-1	tHIGH trct TimeStamp 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	t _o t _o Limit Max 3.072 MHz 3.072 MHz	trov Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.029 MHz	V _{CI64,200} V _{Date} Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	V V V V V V V V V V N	V _{Datafiah} <u>Count</u> 443 443 443 443 443 443 443 44	Result Pass Pass Pass Pass Pass Pass	
1 1 2 2 3 3 4 4 5 5 6 6 7 7	Vaveform No 1-1 2-1 3-1 1-1 5-1 5-1 7-1	tHIGH tract TimeStamp 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	t _o t _o t _o Limit Ma 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz 3.072 MHz	trow Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.029 MHz 3.027 MHz 3.029 MHz	VCIE4.com V Dote: Mean 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Vcilifigh Max 3.033 MHz 3.033 MHz 3.034 MHz 3.033 MHz 3.033 MHz 3.033 MHz 3.033 MHz 3.033 MHz 3.032 MHz 3.033 MHz 3.033 MHz 3.033 MHz 3.033 MHz	VDatatilish 443 443 443 443 443 443 443 443 443 443 443 443	Result Pass Pass Pass Pass Pass Pass Pass	
1 1 2 2 3 3 4 4 5 5 6 6 7 7 8 8	Vaveform No 1-1 2-1 3-1 4-1 5-1 5-1 7-1 7-1	tHIGH t-ct. TimeStamp 81.316 us 81.316 us	t _{ICL} t _{IDD} Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	tov tov Limit Max 3.072 MHz	tow tow Min 3.027 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.028 MHz 3.028 MHz 3.029 MHz 3.029 MHz 3.027 MHz 3.027 MHz 3.027 MHz	V _{CII4.000} V _{Date} 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz 3.030 MHz	Voilefigh Max 3.033 MHz 3.033 MHz 3.034 MHz 3.032 MHz 3.033 MHz	VDataFligh 443 443 443 443 443 443 443 443 443 443 443 443 443 443 443	Result Pass Pass	

8. 波形和参考点





9. Html 报告



Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

Total: 13 Pass: 13 Fail: 0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fclk	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	***	-1.2%	Pass
2	LOW	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	Pass
3	tHIGH	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	Pass
4	4CL	Rise time of CLK signal		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930		-85.7%	Pass
5	4CL	Fall time of CLK signal		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930		-85.7%	Pass
6	4DD	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	Pass
7	t _{fDV}	Delay time from Clk edge to Data Fall Valid	***	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500		-20.7%	✓Pass
8	trop	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	Pass
9	trDV	Delay time from Clk edge to Data Rise Valid	***	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440		-24.8%	✓Pass
10	VCIkLow	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	Pass
11	VDataLow	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	Pass
12	VClkHigh	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	Pass
13	VDataHigh	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	Pass

f_{CLK} - Test Result: Pass Description: Clock frequency

Limit Min Limit Max Min Mean Max Standard Deviation Count	Margin Min Margin	Max	
Histogram	1.6.70		
Occurance (%) Total 4430	Value Range	Occurance Count	
100	3.027 MHz ~ 3.028 MHz	13	
90 -	3.028 MHz ~ 3.028 MHz	70	
70	3.028 MHz ~ 3.029 MHz	298	
60 - 50 -	3.029 MHz ~ 3.03 MHz	813	
40 33.0	3.03 MHz ~ 3.03 MHz	1464	
24.2	3.03 MHz ~ 3.031 MHz	1073	
10 03 1.6 6.7 30 0.6 0.2 Test Value	3.031 MHz ~ 3.032 MHz	529	
3.027 MHz 3.034 MHz	3.032 MHz ~ 3.032 MHz	135	
Test Value 3.027 MHz 3.034 MHz (-1.2%)	3.032 MHz ~ 3.033 MHz	27	
Limit 3 072 MHz	3.033 MHz ~ 3.034 MHz	8	
Min Detail Report Row: 1, Te	st Index: 340 Max	K	Detail Report Row: 3, Test Index: 431
3.50 mV 2 500 mV 100 ms 100 ms S00 mV 2 3.50 Stop S00 mV 2 3.50 Stop S00 mV 2 112.198 μs 1 Stop S00 S00 S00 S00 S00 S00 S00 S00 S00 S0	MS/s	500 mV 2 500 mV -3.50 -3.50	100 ns -142.228 µs PDM Validation Stop S/R: 500 MS/s
		·····	
Muma municipation Muman	hanning	Warman Are	ward Windows warman



SMBus 电气特性验证解决方案

■ 简介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器执行 SMBus (System Management Bus) 电气特性验证,以确保其信号符合所 定义的电气特性规格。在经过长时间持续运行测试后,可确认待测信号的电气特性是否达 标。

SMBus 协议的电气特性检测方式与 I2C 类似,通常分为两大类:

- 垂直属性(电压)
- 水平属性(时间/相位)

因此,使用此功能前,须先设置所选协议与规格,并透过反复测试以取得电气特性测试报告。测试项目会根据 SMBus 的传输速率而有所不同。



SMBus 验证报告内容:

0	verview	Detail	SMBus								
	Name	De	scription	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f _{SCL}	SC	L clock	0.000 Hz	100.000 KHz	3.142 KHz	198.650 KHz	200.008 KHz	13.737 KHz	450	Fail
2	t _{HD,STA}	Hol	d time(4.000 us		2.498 us	2.498 us	2.499 us	234.000 ps	19	Fail
3	t _{SU,STA}	Set	t-up tim	4.700 us		2.093 us	2.097 us	2.104 us	4.275 ns	6	Fail
4	t _{HD,DAT}	Dat	ta hold	5.000 us		118.950 ns	1.242 us	1.374 us	273.845 ns	180	Fail
5	t _{su,dat}	Dat	ta Set-u	250.000 ns		969.002 ns	1.239 us	2.509 us	326.581 ns	180	Pass
6	tsu,sto	Set	t-up tim	4.000 us		2.508 us	2.521 us	2.530 us	6.103 ns	13	Fail
7	t _{LOW}	Lov	v Perio	4.700 us		2.450 us	2.638 us	3.749 us	108.381 ns	468	Fail
8	t _{HIGH}	Hig	h Perio	4.000 us		2.062 us	2.094 us	2.107 us	6.704 ns	496	Fail
9	tra	Ris	e time		1.000 us	264.997 ns	277.670 ns	306.498 ns	4.317 ns	477	Pass
10	t _{ICL}	Fal	l time o		300.000 ns	1.260 ns	1.421 ns	1.598 ns	103.000 ps	556	Pass
11	t _{rDA}	Ris	e time		1.000 us	269.758 ns	277.633 ns	283.758 ns	2.679 ns	118	Pass
12	t _{fDA}	Fal	l time o		300.000 ns	997.000 ps	1.383 ns	1.551 ns	121.000 ps	145	Pass
13	t _{BUP}	Bu	s free ti	4.700 us		256.676 us	782.918 us	2.669 ms	944.462 us	10	Pass
14	t _{VD,DAT}	Dat	ta valid		3.450 us	110.469 ns	1.380 us	1.655 us	357.855 ns	193	Pass
45	turner	Det	in unlin		2 450 110	E06 751 pc	2 145 112	2 750	100 065 00	97	Daga

电气特性验证_软件画面:



- 1. 不同的传输速率模式,包括 Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
- 2. 频率:频率速度
- 时序参数:建立时间(Set-up Time)、保持时间(Hold Time)、上升时间(Rise Time)、 下降时间(Fall Time)与时钟拉伸(Clock Stretching)时间限制
- 4. 电压参数: V_IL (输入低电位)、V_IH (输入高电位) 等



■ SMBus 电气特性验证设置

1. 一般设置: 设置通道来源、工作电压与传输速率

EV Electrical Validatio	n	×
120	Settings	Import Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SMBus SPI UART(RS232)	General ► Decode ► Maildation SMBUS CLK: DSO Channel 1 ▼ Probe Settings: SMBUS DAT: DSO Channel 2 ▼ Probe Settings: Working Voltage(Vob): 3 30 V ♀ Speed Mode Standard Mode (Max: 100Kbit/s) Fast Mode (Max: 400Kbit/s) Fast Mode + (Max: 100Kbit/s) Fast Mode + (Max: 100Kbit/s) High Speed Mode (Max: 3.4Mbit/s) Customized Speed 100 Kbit/s ●	

2. 解码设置: 设置 SMBus 解码参数

Settings			
✓General →Decode	Address Mode		
XValidation	7-bit Addressing		
	O 8-bit Addressing (Including R/W in Address)		
	Startup Settings		
	□ PEC		
	Device		
	MCTP		
	SBS (Smart Battery System)		
	SPD (Serial Presence Detect) DDR4		
Default		Draviaua	Next
Default		Previous	Next



3. 验证项目设置: 包含频率、时序与电压限制条件

Validation	Frequency											
		Name	Description	Min	Max							
	1	1 I SCL clock frequency 0 kHz 100										
		īme										
		Name	Description	Min	Max							
	1	✓ t _{HD,STA}	Hold time(repeated) START condition	4 us	×							
	2	✓ t _{SU,STA}	Set-up time for a repeated START condition	4.7 us	X							
	3	✓ t _{HD,DAT}	Data hold time	5 us	X							
	4	✓ t _{SU,DAT}	Data Set-up time	250 ns	X							
	5	✓ t _{SU,STO}	Set-up time for STOP condition	4 us	X							
	6	✓ t _{LOW}	Low Period of the SCL Clock	4.7 us	X							
	7	✓ t _{HIGH}	High Period of the SCL Clock	4 us	X							
	8	✓ t _{rCL}	Rise time of SCL signal	X	1 us							
	9	✓ t _{fCL}	Fall time of SCL signal	X	300 ns							
	1(0 ✓ t _{rDA}	Rise time of SDA signal	X	1 us							
	1	1 ✔ t _{fDA}	Fall time of SDA signal	×	300 ns							

4. 电气特性验证_软件画面





5. 控制面板



A. 停止条件: 当采集达到 X 次时停止 当测试结果失败超过 X 次时停止

. **信息**: 选择查看波形

C. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)

6. 概览报告

1 V -3.50 Div			2 11	V 50 Div									H 400 μs -1 827 ms	H 400 µs -1 827 ms T SMBus Validation Stop S/R: 500 MS/4
	•								++++					
****				[]/ <mark> </mark> []/			www.		-	ł				
	3			·				0						
SMBus	- 101		50 30 50 1					14 16			50 18 (A (C	50 (8 (4 (0	50 18 14 (C) 50 18 20 22 24 50 50 28 28 28 CO -	50 18 (L, IC) 50 18 29 22 24 50 50 28 28 28 50 50 28 28 20 50 28 20 50 28 20 50 28 20 50 28 20 50 50 50 20 50 50 50 50 50 50 50 50 50 50 50 50 50
120	- 00		50 00 50 1	[0]	50 12		[50	14 16			50 18 IA IC	50 18 LA IC	10 12 14 1C	50 18 1A IC
	attl 226.	856 µs	626,856	i u <mark>s</mark>	1.0 <mark>27 /</mark> ms		1.427 ms	an ann a	1.827 ms		2.2 <mark>2</mark> ? ms	2.627 ms 2.627 ms	2.627 ms 2.627 ms 3.027 ms	2,627,ms 2,627,ms 3.027,ms 3.427,ms 2025-05-
Overview E	Detail SMBus													
Name	Description	Limit Min	Limit Max	Min	Mean	Max 200.007 KHz	ndard Devia	Count	Result	,				
2 HDSTA	Hold time(4.000 us		2.498 us	2.498 us	2.499 us	131.000 ps	10	Fail					
3 tsusta	Set-up tim	4.700 us		2.083 us	2.083 us	2.083 us	0.000 ps	1	Fail					
4 tHILDAT	Data hold	5.000 us		119.745 ns	479.688 ns	1.372 us	490.528 ns	136	Fail	1				
5 tsudat	Data Set-u	250.000 ns		974.424 ns	1.872 us	2.509 us	546.814 ns	160	Pass					
6 tsusto	Set-up tim	4.000 us		2.508 us	2.519 us	2.523 us	4.359 ns	9	Fail	1				
7 Low	Low Perio	4.700 us		2.621 us	2.628 us	2.641 us	3.306 ns	247	Fail					
8 thich	High Perio	4.000 us		2.069 us	2.092 us	2.109 us	7.042 ns	272	Fail					
9 ta	Rise time		1.000 us	263.576 ns	278.151 ns	297.576 ns	5.070 ns	315	Pass					
10 trc.	Fall time o		300.000 ns	1.233 ns	1.411 ns	1.576 ns	103.000 ps	315	Pass	ļ				
11 t _{rDA}	Rise time		1.000 us	270.193 ns	277.390 ns	286.193 ns	3.157 ns	91	Pass					
12 tea	Fall time o		300.000 ns	969.000 ps	1.311 ns	1.610 ns	172.000 ps	99	Pass					
13 tele	Bus free ti	4.700 us		259.681 us	323.345 us	446.687 us	65.990 us	8	Pass					
14 WOLDAT	Data valid		3.450 us	111.416 ns	619.060 ns	1.656 us	516.073 ns	145	Pass	1				
16 towser	Cumulativ		25.000 ms	2 454 us	2.210 US	4.631 us	479 655 ns	306	Pass					
17 LOWMENT	Cumulativ		10.000 ms	2.454 us	2.791 us	4.631 us	479.555 ps	306	Pass	1				



7. 详细报告

1 V -3.50 Div			2 1 V -3.9	/ 50 Div									H 400 μs -1.827 ms	SMBus Validation Stop S/R: 500 MS/s
									++++				ļ	7 V
			20 00 100 100		20 12 10 12		P 44 - 10 44 10 10 10 10 10 10 10 10 10 10 10 10 10	1 4 16 14 16		0188 (A) (C)		20 (E) 20 (Z) 24 (E) 24		4 ∨ 4 ∨ 2 ∨ 0 22 ≥ 2 ≥ 1 1
1	226.	356 µs	626,856	us	1.0 <mark>27 ms</mark>		1.427 ms	l ann a star	1.827 ms	2.2	27 ms	2.627 ms	3.027 ms	0 V 3.427 ms 2025-05-13 08:51:52
Overview De	tail SMBus													
f _{SCL} t _{HD,STA}	t _{su,sta} t	HD.DAT tsu.DA	r t _{su,sto}	t _{LOW} t _{HIGE}	t _{rol} t _{rol}	L t _{rDA} 1	t _{IDA} t _{BUF}	t _{VD,DAT} t _{VI}	DACK LOWISE	xT tLOWMEXT	V _{Los} V	V _{High} V _{Max} V _{Min}		
Naveform N	o TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result			
1 1-1	249.982 us	START	00		4.700 us									
2 1-2	500.337 us	START	50		4.700 us		446.687 us	446.687 us	446.687 us	1	Pass			
3 1-3	549.412 us	RESTART	50	10	4.700 us									
4 1-4	750.716 us	START	50	12	4.700 us		301.538 us	301.538 us	301.538 us	1	Pass			
5 1-5	1.001 ms	START	50	14 16	4.700 us		399.960 us	399.960 us	399.960 us	1	Pass			
6 1-6	1.252 ms	START	50	18 1A 1C	4.700 us		352.884 us	352.884 us	352.884 us	1	Pass			
7 1-7	1.502 ms	START	50	1E 20 22 24	4.700 us		306.308 us	306.308 us	306.308 us	1	Pass			
8 1-8	1.753 ms	START	50	26 28 2A 2C	4.700 us	-	259.964 us	259.964 us	259.964 us	1	Pass			
9 1-9	2.003 ms	START	50	2E 30 32 34	4.700 us		259.681 us	259.681 us	259.681 us	1	Pass			
10 1-10	2.253 ms	START	50	36 38 3A 3C	4.700 us		259.735 us	259.735 us	259.735 us	1	Pass			

8. 波形和参考点

1 V -3.50 Div			2 1 V -3:	V 50 Div									Η 1 μs -505.32 μs	T SMBu Stop
SMBus I2C						I							Addr(7b): 50 84dr(7b): 50	• • • • • •
1	 501.	32 µs.		hs	³ 0,3,32,ца		-50	4.32 (is 505		506.32 µs	507.32 µs		50 <mark>8,32 µs</mark>	509
Overview	Detail SMBus						(🖗 Detail						X
· · · ·			1				_	Countral Cou						^
f _{SCL} t _{HD,S}	TA t _{SU,STA} t	HD,DAT tsu,D	AT t _{SU,STD}	t _{LOW} t _{HIGP}	t _{rCL} t _i	CL t _{rDA}	tida	t _{SU,DAT}						
f _{SCL} t _{HD,8} Naveform 1 1-1	TA t _{SU,STA} t No TimeStamp 249.982 us	HD,DAT t _{SU,D} Status START	AT t _{SU,STD} Address	t _{LOW} t _{HIGH} D0-D7	t _{rCL} t _i Limit Min 250.000 ns	CL t _{rDA}	t _{©A}	t _{SU,DAT} Waveform No.	TimeStamp 500.337 us	Status START	Ad	dress 50	D0-D7	
f _{SCL} t _{HD,S} Naveform 1 1-1 2 1-2	TA t _{SU,STA} t No TimeStamp 249.982 us 500.337 us	HD.DAT t _{SU,D} Status START START	AT t _{SU,STO} Address 00 50	t _{LOW} t _{HIGP} D0-D7	t t _{rCL} t _f Limit Min 250.000 ns 250.000 ns	CL t _{rDA} Limit Max	t _{IDA}	tsu,DAT Waveform No. 1-2 Time	Time Stamp 500.337 us ∆ Time	Status START Volt	Ad ∆ ∛olt	dress 50 Result	D0-D7	
f _{SCL} t _{HD,5} Naveform 1 1-1 2 1-2 3 1-3	TA t _{SU,STA} t No TimeStamp 249.982 us 500.337 us 549.412 us	START RESTART	AT t _{SU,STD} Address 00 50 50	t _{LOW} t _{HIGP} D0-D7	t _{rcL} t _i Limit Min 250.000 ns 250.000 ns 250.000 ns	Limit Max	t _{IDA} 97 98	Waveform No. 1-2 Time 1 (1.005 ms, 1.006 ms)	Time Stamp 500.337 us Δ Time 976.212 ns	Status START Volt (3.5 V, 1.5 V)	Ad ∆ Volt -2 V	dress 50 Result Pass	D0-D7	
f _{SCL} t _{HD,S} Naveform 1 1-1 2 1-2 3 1-3 4 1-4	TA tsu.stA t INO TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 750.716 us	START START RESTART START	ит t _{SU,STO} Address 00 50 50 50	t _{LOW} t _{HIGH} D0-D7	t _{rcL} t _r Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns	Limit Max	t _{⊡∧} 97 98 97	Yes Yes Uaveform No. 1-2 Time 1 1 (1.005 ms, 1.006 ms) 2 2 (1.009 ms, 1.011 ms) 1.011 ms)	Time Stamp 500.337 us △ Time 976.212 ns 1.386 µs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Ad △ ₹olt -2 ∨ 0 ∨	Idress 50 Result Pass Pass	D0-D7	
f _{SCL} t _{HD,S} Waveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5	tsu.sth t No TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 1.001 ms 1.001 ms	INDURT TAULO START START RESTART START START	t t <tht< th=""> t t t</tht<>	tLow tHese D0-D7 10 12 14 16	t _{rCL} t _r Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns	trDA Limit Max	t _{⊡A} 97 98 97 97	Tsu.Dat Waveform No. 1-2 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V)	△ Volt -2 V 0 V -2 V	Idress 50 Result Pass Pass Pass	D0-D7	
fscL t _{HD,S} Waveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6	tsusst t NO TimeStamp 249.982 us s 500.337 us s 549.412 us s 750.716 us 1.001 ms 1.252 ms 1.252 ms	ND.DAT tsu.D. Status START START RESTART START START START	Art tsustro Address 00 50 50 50 50 50	tLOW tHEF DO-D7 10 12 14 16 18 1A 1C	t _{rCL} t _r Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns	Limit Max	+DA 97 97 97 97 97 97	Tsu,DAT Waveform No. 1-2 1 (1.005 ms, 1.006 ms) 2 1.009 ms, 1.011 ms) 3 1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Ad △ ∀olt -2 ∨ 0 ∨ -2 ∨ 0 ∨ 0 ∨	dress 50 Result Pass Pass Pass Pass	D0.D7	
fscL t+tb.5 Naveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7	t t t No TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 1.001 ms 1.252 ms 1.502 ms	START START START RESTART START START START START	At tsusmo Address 00 50 50 50 50 50 50	tuow teso to to test test test test test tes	t _{rCL} t, Limit Min 250.000 ns 250.000 ns 250.000 ns	trpA Limit Max	t _{DA} 91 92 91 91 92 91 91 91 91 91 91	Tsu,DAT Waveform No. 1-2 1	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	△ ∀oit -2 ∨ 0 ∨ -2 ∨ 0 ∨ 0 ∨	dress 50 Result Pass Pass Pass Pass	D0-D7	
fscl. t _{HD.5} Waveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7 8 1-8	t tsussa t No TimeStamp 249.982 us 500.337 us 549.412 us 549.412 us 1.001 ms 1.252 ms 1.502 ms 1.502 ms 1.753 ms	START START START RESTART START START START START START	Att Susstol Address 00 50 50 50 50 50 50 50 50 50 50	tuow tessee D0-D7 10 12 14 16 18 1A 1C 1E 20 22 24 26 28 2A 2C	t,cL t, Limit Min 250.000 ns 250.000 ns 250.000 ns	trpA trpA	t _{DA} 97 97 97 97 97 97 97 97 97 97	Image: state	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	△ ¥olt -2 V 0 V -2 V 0 V -2 V 0 V	dress 50 Result Pass Pass Pass	D0-D7	
fsct titot. Maxeform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7 8 1-8 9 1-9	t tsusta t No TimeStamp 249.982 us 500.337 us 509.412 us 549.412 us 750.716 us 1.001 ms 1.252 ms 1.502 ms 1.502 ms 2.003 ms 2.003 ms	taub taub Status Start START Start	vr t _{SU,STO} Address 0 50 50 50 50 50 50 50 50 50 50	tuow tinos D0-D7 10 12 14 16 18 1A 1C 1E 20 22 24 26 28 2A 2C 2E 30 32 34	t _{cL} t _n Limit Min 250.000 ns 250.000 ns 250.000 ns	Limit Max	t _{DA} 91 91 91 91 91 91 91 91 91 91 91 91 91	Tsu,DAT Waveform No. 1-2 1	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 15 V) (1.5 V, 15 V) (3.5 V, 15 V) (1.5 V, 15 V)	Δ Volt -2 V 0 V -2 V 0 V -2 V	Idress 50 Result Pass Pass Pass	D0-D7	
fscz. tu:0.4 Naveform 1 2 1.2 3 1.3 4 1.4 5 1.5 6 1.6 7 1.7 8 1.8 9 1.9 10 1.10	t tsusta t No TimeStamp 249.982 us 500.337 us 509.412 us 549.412 us 1.001 ms 1.252 ms 1.502 ms 1.753 ms 2.003 ms 2.253 ms 1.252 ms	taub taub Status Startus START Start RESTART Start START Start	v t _{SUSD} Address 50 50 50 50 50 50 50 50 50 50 50 50 50	tune tune D0-D7 0 10 10 12 11 14 16 18 1A 12 22 24 26 28 2A 22 23 36 38 36 38	t _{ct} t _i Limit Min 250.000 ns 250.000 ns 250.000 ns	LL toA	t _{⊡A} 91 91 91 91 91 91 91 91 91 91 91 91 91	Tsu,DAT Waveform No. 1-2 1	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Ad Δ Volt -2 V 0 V -2 V 0 V	Idress 50 Result Pass Pass Pass Pass	D0-D7	
fack tun, n Naveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7 8 1-8 9 1-9 10 1-10	t t t No TimeStamp 249.982 us 500.337 us 509.412 us 549.412 us 750.716 us 1.001 ms 1.252 ms 1.502 ms 2.003 ms 2.003 ms 2.253 ms	HELDER & GUIDER CONTRACT START START START START START START START START START START START START	vr t _{susm} Address 50 - 50	tuov two D0-D7 10 12 14 16 18 1A 1⊂ 16 20 22 24 26 28 2A 2C 2E 30 32 34 36 38 3A 3C	t t _{ct} t, Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns	EL E.	t _{⊡A} 91 91 91 91 91 91 91 91 91 91 91 91 91	Tsu,DAT Waveform No. 1-2 1	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	△ ¥0h -2 V 0 V -2 V 0 V -2 V 0 V	Idress 50 Pass Pass Pass Pass	D0-D7	



9. Html 报告



Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

Total: 13 Pass: 13 Fail: 0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fclk	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	***	-1.2%	Pass
2	LOW	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	Pass
3	tHIGH	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	Pass
4	4CL	Rise time of CLK signal		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930		-85.7%	Pass
5	4CL	Fall time of CLK signal		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930		-85.7%	Pass
6	4DD	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	Pass
7	t _{fDV}	Delay time from Clk edge to Data Fall Valid	***	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500		-20.7%	✓Pass
8	trop	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	Pass
9	trDV	Delay time from Clk edge to Data Rise Valid	***	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440		-24.8%	✓Pass
10	VCIkLow	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	Pass
11	VDataLow	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	Pass
12	VClkHigh	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	Pass
13	VDataHigh	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	Pass

f_{CLK} - Test Result: Pass Description: Clock frequency

Limit Min Limit Max Min Mean Max Standard De	viation Count	Margin Min Marg	n Max			
0.000 Hz 3.072 MHz3.027 MHz3.030 MHz3.034 MHz17.798 KHz Histogram	4430			1		
Instogram		Value Range	Occurance Count			
Occurance (%), Total 4430		3 027 MHz ~ 3 028 M	2 13			
100		2.022.184-2.2.022.18	70			
80 -		3.020 MP12 - 3.020 MP				
70 -		3.028 MHz ~ 3.029 MH	z 295			
50		3.029 MHz ~ 3.03 MHz	813			
40 33.0 30 24.2		3.03 MHz ~ 3.03 MHz	1464			
20 18.4 11.9		3.03 MHz ~ 3.031 MHz	1073			
10 0.3 1.6 0.7 30 0.5 0.2	Test Value	3.031 MHz ~ 3.032 MH	z 529			
3.027 MHz 3.0	34 MHz	3.032 MHz ~ 3.032 MH	z 135			
Test Value 3.027 MHz 3.03	4 MHz (-1.2%)	3.032 MHz ~ 3.033 MH	z 27			
Limit 3.0	12 MHz	3.033 MHz ~ 3.034 MH	z 8			
Min Detail Repo	rt Row: 1, Tes	t Index: 340 Ma	x	· · · · · · · · · · · · · · · · · · ·	Detail Report Re	ow: 3, Test Index: 431
500 mV 2 500 mV 112.198 μs	PDM Validation Stop S/R: 500 M	IS/6	500 mV 500 mV 3.50	mV)	100 ns PDI -142.228 µs 🚺 Sto	M Validation p <u>S/R: 500 MS/s</u>
	El Margan					



SPI 电气特性验证解决方案

File / Settings Dis	splay Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	en iile					

使用示波器执行 SPI(Serial Peripheral Interface)电气特性验证,以确保其信号符合所定义的电气规格。在经过长时间持续运行测试后,可确认待测信号的电气特性是否达标。



■ SPI 电气特性验证设置

1. 一般设置:根据总线配置选择 SPI 类型(4-wire SPI 或 3-wire SPI)。

Settinas							Import	Export
 General Decode 	Channel	Settings						
×Trigger	Type:	4-wire SPI	•					
XValidation	SCLK:	DSO Channel 1	 Probe Settings: 	x10 -	x10 >>			
	CS:	DSO Channel 2	 Probe Settings: 	x10 -		-		
	SDI:	DSO Channel 3	 Probe Settings: 	x10 -		-		
	SDO:	DSO Channel 4	 Probe Settings: 	x10 -		-		
Default								Next

4-wire 设置:

Channel S	Settings			
Type:	4-wire SPI	•		
SCLK:	DSO Channel 1	 Probe Settings: 	x10	
CS:	DSO Channel 2	Probe Settings:	x10	
SDI:	DSO Channel 3	Probe Settings:	x10	
SDO:	DSO Channel 4	 Probe Settings: 	x10	

3-wire 设置:

hannel S	Settings								
Type:	3-wire SPI	*							
SCLK:	DSO Channel 1	Ŧ	Probe Settings:	x10		10 =			
CS:	DSO Channel 2	Ŧ	Probe Settings:	x10		10 =-			
SDA:	DSO Channel 3	Ŧ	Probe Settings:	x10	-	10			



2. 解码设置:设置 SPI 的数据格式以及各个通道的 Latching Edge。这里所设

Settings				Import	Export
 ✓General 	4-wire SPI				
 Decode Trigger Validation 	Chip Select Edge SDI Edge SDO Edge	Active Low Rising Falling			
	Data Format				
	Bit Order	MSB First 👻			
	Word Size	8 bits			
Default				Previous	Next

置的 SPI 数据格式会同时套用至解码与触发设置中。

3. 触发设置:数据格式已在上一页设置完毕。本部分剩下的设置重点是数据

地址与要触发的数据脚位。

Settinas							Import	Export
 ✓General ✓Decode 	Trigger on							
 Trigger 	Data Pin	Data In - SDI	•					
X Validation	Data							
	Fixed	Offset 0		Byte(s)				
	Data 1	XXh	Data 5	XXh				
	Data 2	XXh	Data 6	XXh				
	Data 3	XXh	Data 7	XXh				
	Data 4	XXh	Data 8	XXh				
Default							Previous	Next



4. 验证参数设置

code	 Customized E 	EV Parameter:		
iger idation	Freque	ncy		
dution	Name	Description	Min	Max
	1 ✔ f _{SCLK} S	CLK Clock Frequency	0 MHz	10 MHz
	Times			
	A nme Name	Description	Min	Max
	1 ✔ t _{su,sp}	SDI Setup Time	5 ns	x
	2 ✔ t _{HD,SD}	SDI Hold Time	15 ns	x
	3 🗌 t _{DIO}	SDI Output Delay Time	Х	х
	4 ✔ t _{su,sp}	₀SDO Setup Time	5 ns	x
	5 ✔ t _{HD,SD}	oSDO Hold Time	5 ns	x
	6 ✔ t _D	SDO Output Delay Time	X	6 ns
	7 ✔ t _{HIGH}	SCLK Clock High Time	5 ns	x
	8 🗸 t _{LOW}	SCLK Clock Low Time	5 ns	x
	9 ✔ t _{su,cs}	CS Chip Select Setup Time	5 ns	x
	10 ✔ t _{HD,CS}	CS Chip Select Hold Time	20 ns	x
	11 ✔ t _{cs}	Chip Select Deselect time (Chip Select High Time)	50 ns	x

由于 SPI 总线并未有行业标准的测量门限值,因此用户在进行验证时请自行定义合适的门限值。

本部分显示三项特性参数表,包括:

- 频率
- 时序参数
- 电压需求

所有支持的验证参数项目与说明如下:



SPI Frequency Requirements

Symbol	Electrical Parameter
f _{SCLK}	SCLK Clock Frequency

SPI Timing Requirements

Symbol	Electrical Parameter
t _{su,sdi}	SDI Setup Time
t _{HD,SDI}	SDI Hold Time
t _{DIO}	SDI Output Delay Time
t- _{SU,SDO}	SDO Setup Time
t _{HU,SDO}	SDO Hold Time
t _D	SDO Output Delay Time
t _{ніgн}	SCLK High Time
t _{LOW}	SCLK Low Time
t _{su,cs}	CS Chip Select Setup Time
t _{su,cs}	CS Chip Select Hold Time
t _{cs}	Chip Select Deselect time (Chip Select High Time)
t _{CLKr}	SCLK Clock Rise Time
t- _{CLKf}	SCLK Clock Fall Time

SPI Voltage Requirements

Symbol	Electrical Parameter
V _{IL}	Low-Level Input Voltage
V _{IH}	High-level Input Voltage
V _{OL}	Low-level Output Voltage
V _{OH}	High-level Output Voltage



UART 电气特性验证解决方案

■ 简介:

File / Settings D)isplay Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Op Validation EV	en File					

使用示波器进行 UART 电气特性验证,以确认 UART 是否符合所定义的规格。在长时间 持续运行测试之后,可验证被测信号的电气特性是否达标。

对于协议的电气验证, UART 协议的电气特性检测通常分为两种: 垂直(电压)与水平 (时间/相位)。

因此,使用本功能前,需先设置协议类型与规格,然后重复测试以获得电气特性测试报告。测试项目会依 UART 传输速率不同而有不同的规格与标准。



UART 验证报告:

(Overview	Detail	UART(F	RS232)							
	Name	De	scription	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	\mathbf{f}_{UART}	Bau	d rate	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	Pass
2	V _{Low}	Low	-level i	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	Fail
3	V _{High}	High	I-level i	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	Pass

电气特性验证_软件画面:



- 1. 频率:时钟速率
- 时序参数:建立时间(Set-up Time)、保持时间(Hold Time)、上升时间(Rise Time)、 下降时间(Fall Time)与时钟拉伸(Clock Stretching)时间限制
- 3. 电压参数: V_IL (输入低电位)、V_IH (输入高电位)等



■ UART 电气特性验证设置

1. 一般设置: 通道来源、工作电压与传输速率

		· · · ·	
Settings			
 General Decode 	Channel Settings		
XValidation	Data: DSO Channel 1 V Probe Settings: x10 V		
	Voltage High(V _{tEgh}): 5.00 V ♀ Voltage Low(V _{Low}): -5.00 V ♀		
	Baud Rate		
	9600 v bps		
Default			Next

2. 解码设置: UART 解码设置

Settings			·
✓General	Format		
Decode Molidation	Data Bits	Polarity	
- validation	8	▼ Idle High ▼	
	Parity	Stop Bits	
	None	• 1 •	
	MSB First Invert Bi Report Size: 16 💌	IS	



3. 验证参数设置:频率、时序与电压限制条件

Baud Rate			
Name 1 ✓ f _{UART} Baud rate for UART	Description	-0.5 %	0.5 %
 Ime			
Name	Description	Min	Max
1 tr Edge rise time		X	Х
2 t _f Edge fall time		Х	X
3 ✔ t _{high} High time		98.958 µs	109.375 µs
4 d t _{iow} Low time		98.958 µs	109.375 µs
✓ Voltage			
Name	Description	Min	Max
1 ✓ V _{Low} Low-level input voltage		-4.5 V	-5.5 V
2 ✓ V _{High} High-level input voltage		4.5 V	5.5 V
Name 1 ▼ V _{Low} 2 ▼ V _{Hight} High-level input voltage	Description	Min -4.5 V 4.5 V	Max -5.5 V 5.5 V

4. 电气特性验证_软件画面





5. 控制面板



D. 停止条件:
 当采集达到 X 次时停止
 当测试结果失败超过 X 次时停止

E. 信息: 选择查看波形

. 储存档案:

储存为 HTML 格式 储存为 .MOW (Acute软件专用格式)

6. 概览报告





7. 详细报告



8. 波形和参考点





9. Html 报告

Acute. PC-based T&M Instruments	
	Electrical Validation Report Test Instrument Model MSO3124V Test Instruments Serial Number MSO3124017 Unit of the serial Number MSO3124017
	Instruction 04-27-2025 1007-32 SMV Version 1.0.25 Protocol UART(RS232)
Overview Results: Total: 3 Pass: 2 Fail: 1	
Index Name Description Limit Min Limit Max Min Mean Max	Standard Deviation Count Margin Min Margin Max Result
1 f _{UART} Baud rate for UART -0.5 % 0.5 % 0.0 % 0.0 % 0.1 %	0.0 % 32 -100.0% -80.0% VPass
2 VLow Low-level input voltage 7.200 V -8.800 V -8.759 V -7.541 V 0.000 u	/16.20 V 104 21.7% -100.0% ¥Fail
5 VHigh High-level input voltage 1.200 V 0.800 V 0.541 V 0.555 V 0.015 V	01.390 IIIV D2 10.076 -2.176 PB35
V _{Low} - Test Result: Fail Description: Low-level input voltage	
Limit Min Limit Max Min Mean Max Standard Deviation Count Margin Min Marg -7.200 V -8.800 V -8.759 V -7.541 V 0.000 uV 16.920 V 104 21.7% -100	No market
Histogram	
Occurance (%), Total 102	
1000.739 V	
80	
70	
50 -	
30	32 0 0
20 137 4.38 V 3	
-2.626 V ~ -	
-8.759 V (21.7%) 0.000 uV (+100.0%)	
Min Detail Report Row: 18 Test Index	2 May Datail Bonort Pour 16. Test Index 2
SV_ SV_ SV_ SV_ SV_ SV_ UART(RS232) Validation	South Control
+0.00	B +0.00 ¹² +0.00 ¹² +0.00 ¹ +0.00 B +0.00 B +0.00 B Stop <u>S.R. 1.MS/s</u>
Smale 61	Devisit 73 P 2



HTML 报告导出

■ 简介

每次 EV 测试皆支持导出 HTML 报告。HTML 报告包含每个测试项目、测试结果、最大/最小值、直方图与波形截图。

li 另存為 HTML	×
C:\Users\sam\OneDrive\文件/Acute/MS3K//EV_Report	瀏覽
報告標題 Electrical Validation Report	
儲存設定	
將 HTML 儲存為: 不合併 ▼ □ 設定用戶標誌	瀏覽
進階設定 OK	Cancel

储存设置:

A. 将 HTML 储存为: 不合并/合并

不合并:图片会与 HTML 分开储存。

合并:图片会嵌入在 HTML 档案中(单一档案)。

B. 设置用户标志 Logo:

勾选后可选择图片文件作为报告中的公司/用户标志。

C. 附加用户信息:

可在此输入任何想要加入到报告中的补充说明或用户信息。



进阶设置:

	Name	User-Defined Name	Mag. Min	Mag. Max		
1	f _{SCL}		1	1	f _{SCL} User Defined Name	
2	t _{HD,STA}		1	1		
3	t _{su,sta}		1	1	Magnification Minimu	ım Im
4	t _{HD,DAT}		1	1	x1	
5	t _{SU,DAT}		1	1	Magnification Maxim	um Im
6	tsu,sto		1	1	x1	
7	tLow		1	1		
8	thigh		1	1	Apply	

A. 用户可自定义测试项目于 HTML 报告中的显示名称

B. 用户亦可调整 HTML 报告中图片的显示倍率



进阶设置

■ 简介

EV 测试允许使用者根据每次采集的需求,调整预设的采集时间。由于不同的 协议有不同的预设频率或传输速率,这些差异主要来自于协议的传输速度与 数据包长度的不同。有时候,为了更准确地分析数据,可能需要采集更长的 数据包。因此,Acute 提供了 进阶设置 功能,让用户可以个别调整各项参 数的采集时间。

*仅在进入 EV 参数设置 时,才会显示 进阶设置 按钮



EV 进阶设置:





MSO/TS3000 系列多机叠加

■ 简介

Acute MSO3K / TS3K示波器的特点之一是其多机组合叠加功能,这使得最多可叠加16台示波器,同时实现64通道最高250MS/s,或是16通道最高1GS/s的测量能力。在机壳设计方面,MSO3K / TS3K专为叠加应用而设计,具备精心设计的定位导槽,使示波器在叠加配置中能够完美摆放。此外,示波器的散热性能也得到了充分考虑,配置了双侧散热孔,确保长时间运行时不会出现过热问题。

在信号连接方面,用户可以选择直接将待测信号通过标准BNC接头连接到示波器,或者使用被动探棒或差分探棒进行更广泛性的测量。此外,Acute还提供了BNC to Probe Tip Adaptor,可以改善传统探棒在连接上常见的测量连接质量问题,确保用户获得最准确的测量结果。



■ 软件画面

1. 64Channel @ 250MS/s



2. 16Channel @ 1GS/s







2. 搭配被动探棒测量




3. 搭配被动探棒以及BNC to Probe Tip Adaptor测量



4. 搭配高压差分探棒测量









■ 注意事项

- MSO3K / TS3K 示波器为 USB3.0 接口界面的仪器,运作时需消耗
 4.5~7.7W,使用时建议连接至台式电脑后方的 USB3.0 插槽或是使用具有独立供电的 USB3.0 hub,以提供最佳的电力供应及最佳的测量性能。
- 2. MSO3K / TS3K 示波器经过内部测试,在叠加状态下仍可保持长时间运作不 致过热,但若长时间于高温或不利于散热环境使用时,仍须注意示波器工 作温度并适度提供额外散热方式,以避免示波器过热 (>80 度 C) 而影响操 作。



 多机叠加时,各机器间根据采样率不同,会产生一定程度的相位差,以 1GS/s 采样率为例,主机和第一台从机间的相位差为 <±2ns,和最后一台 从机间的相位差为 <±3ns。





主机和最后一台从机(16th)的相位差

1	500 mV +0.00 5	500 mV +0.00 9	500 mV +0.00 ¹³	500 mV +0.00	500 mV +0.00 ²¹	500 mV +0.00 ²⁵	500 mV 29 50 +0.00 29 +0	0 mV 33 500 r 00 33 +0.00	nV 37 500 mV +0.00 41	500 m +0.00	V45 500	00 00 5	600 mV -0.00	600 mV 6.00 57	600 mV ⊧0.00	500 mV +0.00 H	10 ns +0 s	Trig'd S	11 mV R: 1 GS/s	
	@:-722 ps ∆:6.468 ns																			
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