2025

Acute®
PC-based T&M Instruments

電氣特性驗證說明

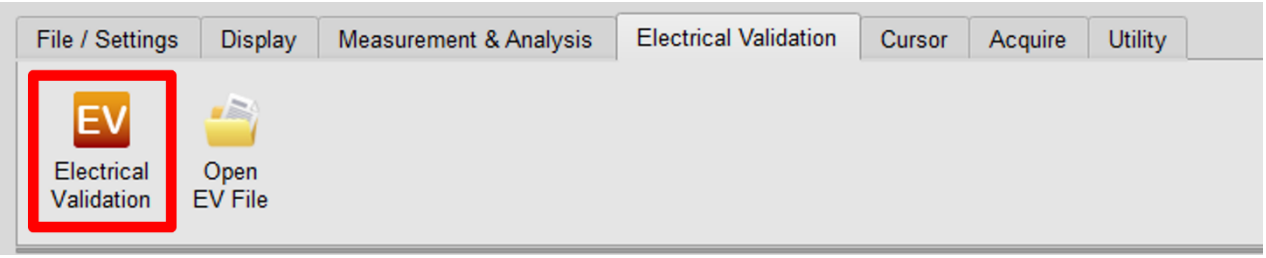
目錄

Protocols

其他設定

I²C 電氣特性驗證解決方案

■ 簡介:



使用示波器進行 I²C 電氣特性驗證，以確保 I²C 符合定義的規範。在經過長時間的燒機測試後，可以確認所測試的訊號電氣特性符合規範。

I²C 協定的電氣特性檢測通常分為兩種類型：垂直（電壓）與水平（時間/相位）。

因此，在使用此功能時，必須先設定所選的協定與規格，然後重複測試以取得電氣特性測試報告。測試項目會依據 I²C 的速度而有所不同。

常見 I²C 規格中的部分電氣特性規格：

Table 13. Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I²C-bus devices[1]

Symbol	Parameter	Conditions	C_b = 100 pF (max)		C_b = 400 pF[2]		Unit
			Min	Max	Min	Max	
f_{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
$t_{SU;STA}$	set-up time for a repeated START condition		160	-	160	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		160	-	320	-	ns
t_{HIGH}	HIGH period of the SCL clock		60	-	120	-	ns
$t_{SU;DAT}$	data set-up time		10	-	10	-	ns
$t_{HD;DAT}$	data hold time		0[3]	70	0[3]	150	ns
t_{rCL}	rise time of SCLH signal		10	40	20	80	ns
t_{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
t_{fCL}	fall time of SCLH signal		10	40	20	80	ns

I²C 電氣特性驗證 報告內容：

Overview | Detail | I2C

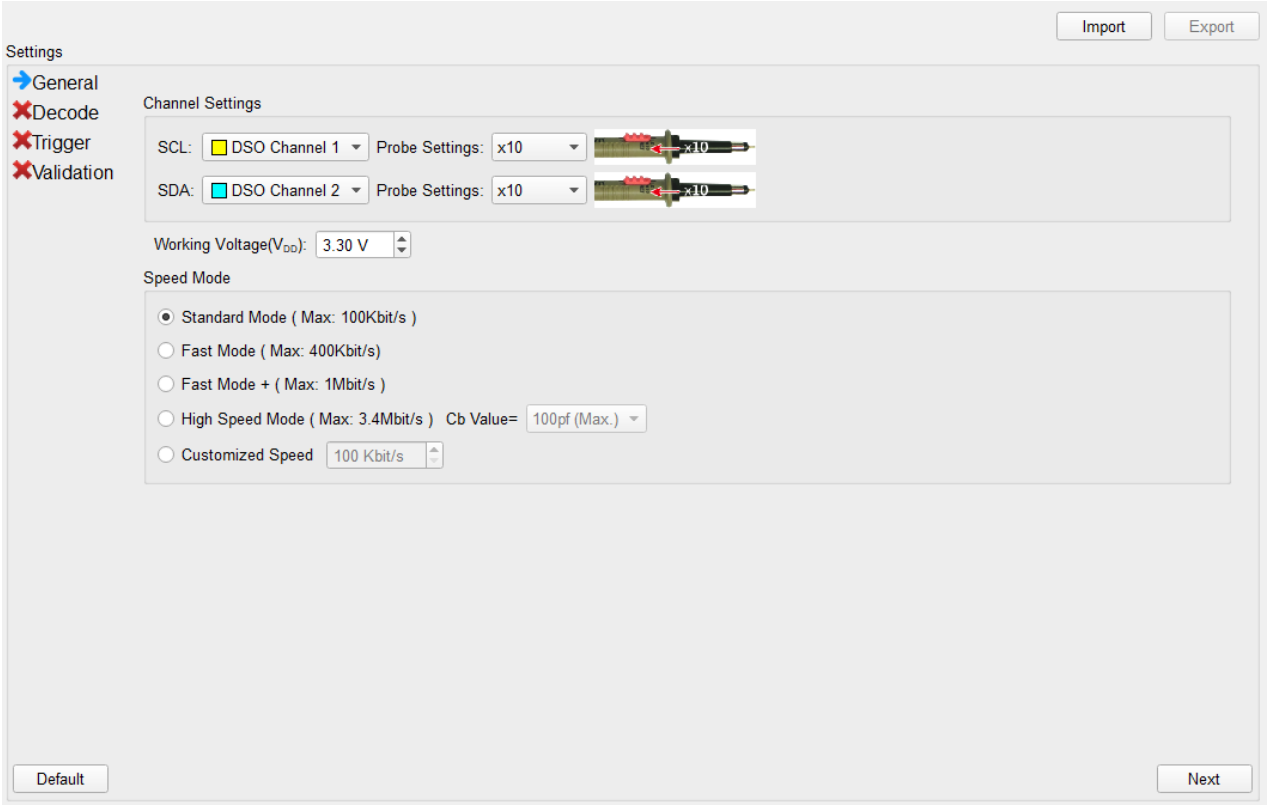
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	f_{SCL}	SCL clock frequencey	0.000 Hz	400.000 KHz	387.596 KHz	387.683 KHz	387.897 KHz	34200	Pass
2	$t_{HD;STA}$	Hold time(repeated) START condition	600.000 ns	—	1.536 us	1.537 us	1.540 us	200	Pass
3	$t_{SU;STA}$	Set-up time for a repeated START condition	600.000 ns	—	2.010 us	2.012 us	2.014 us	100	Pass
4	$t_{HD;DAT}$	Data hold time	—	—	94.000 ns	274.110 ns	1.028 us	17250	Pass
5	$t_{SU;DAT}$	Data Set-up time	100.000 ns	—	472.000 ns	1.066 us	1.444 us	25100	Pass
6	$t_{SU;STO}$	Set-up time for STOP condition	—	—	—	—	—	0	—
7	t_{LOW}	Low Period of the SCL Clock	1.300 us	—	1.538 us	1.542 us	1.544 us	34100	Pass
8	t_{HIGH}	High Period of the SCL Clock	600.000 ns	—	974.000 ns	982.475 ns	3.560 us	41800	Pass
9	t_{rCL}	Rise time of SCL signal	20.000 ns	300.000 ns	45.999 ns	50.304 ns	51.999 ns	41800	Pass
10	t_{fCL}	Fall time of SCL signal	20.000 ns	300.000 ns	10.000 ns	10.528 ns	11.999 ns	41800	Fail
11	t_{rDA}	Rise time of SDA signal	20.000 ns	300.000 ns	37.999 ns	39.210 ns	41.999 ns	9300	Pass
12	t_{fDA}	Fall time of SDA signal	20.000 ns	300.000 ns	4.000 ns	6.714 ns	10.000 ns	9900	Fail
13	t_{BUF}	Bus free time between a STOP and START condition	—	—	—	—	—	0	—
14	$t_{VD;DAT}$	Data valid time	—	900.000 ns	98.000 ns	267.062 ns	1.068 us	15750	Fail
15	$t_{VD;ACK}$	Data valid acknowledge time	—	900.000 ns	98.000 ns	623.009 ns	1.068 us	1500	Fail

電氣特性驗證 軟體畫面：

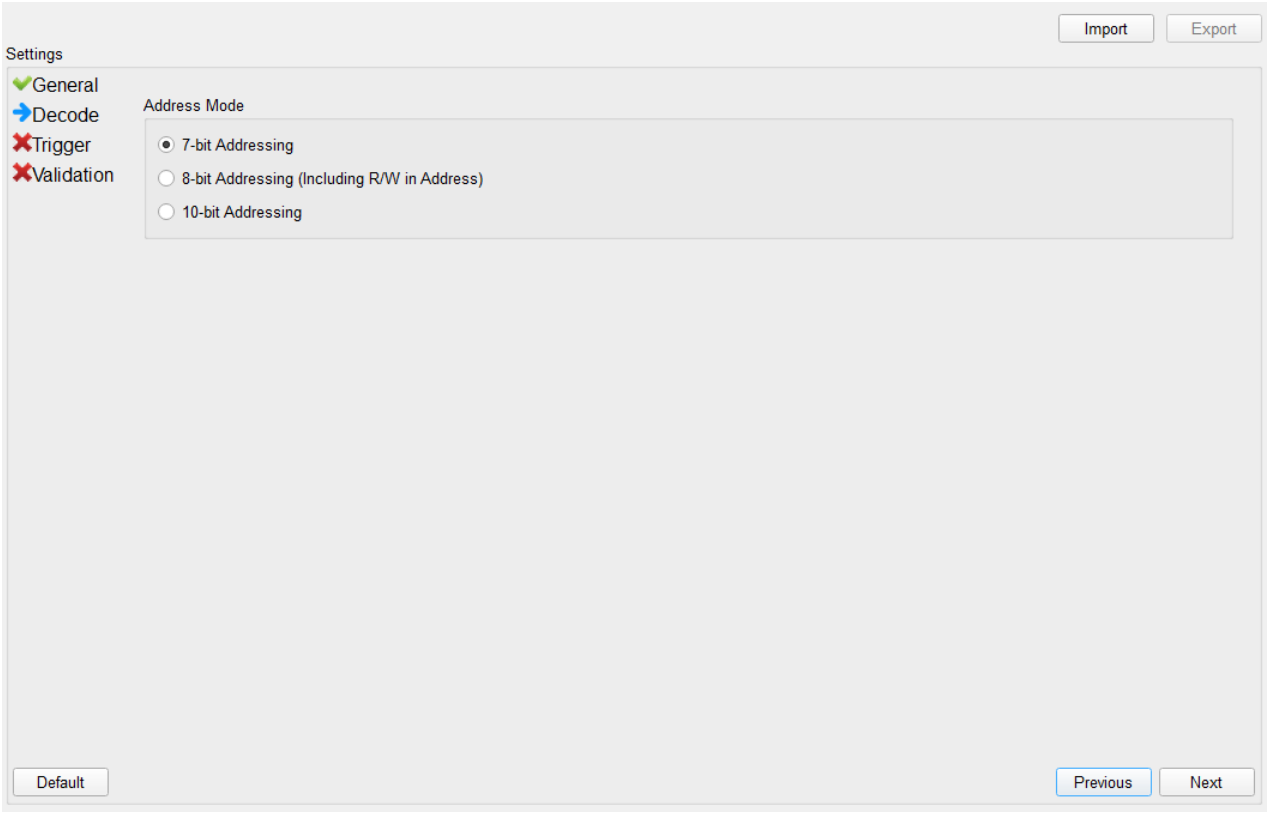
1. 不同的速度模式，包含標準模式（Standard Speed Mode，約 100kHz）／快速模式（Fast Mode，約 400kHz）／快速模式+（Fast Mode+，約 1MHz）／高速模式（HS Mode，約 3.4MHz）
2. 頻率：時鐘頻率（Clock Speed）
3. 時序參數：Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
4. 電壓參數：V_IL（輸入低電位）、V_IH（輸入高電位）等

I²C 電氣特性驗證設定

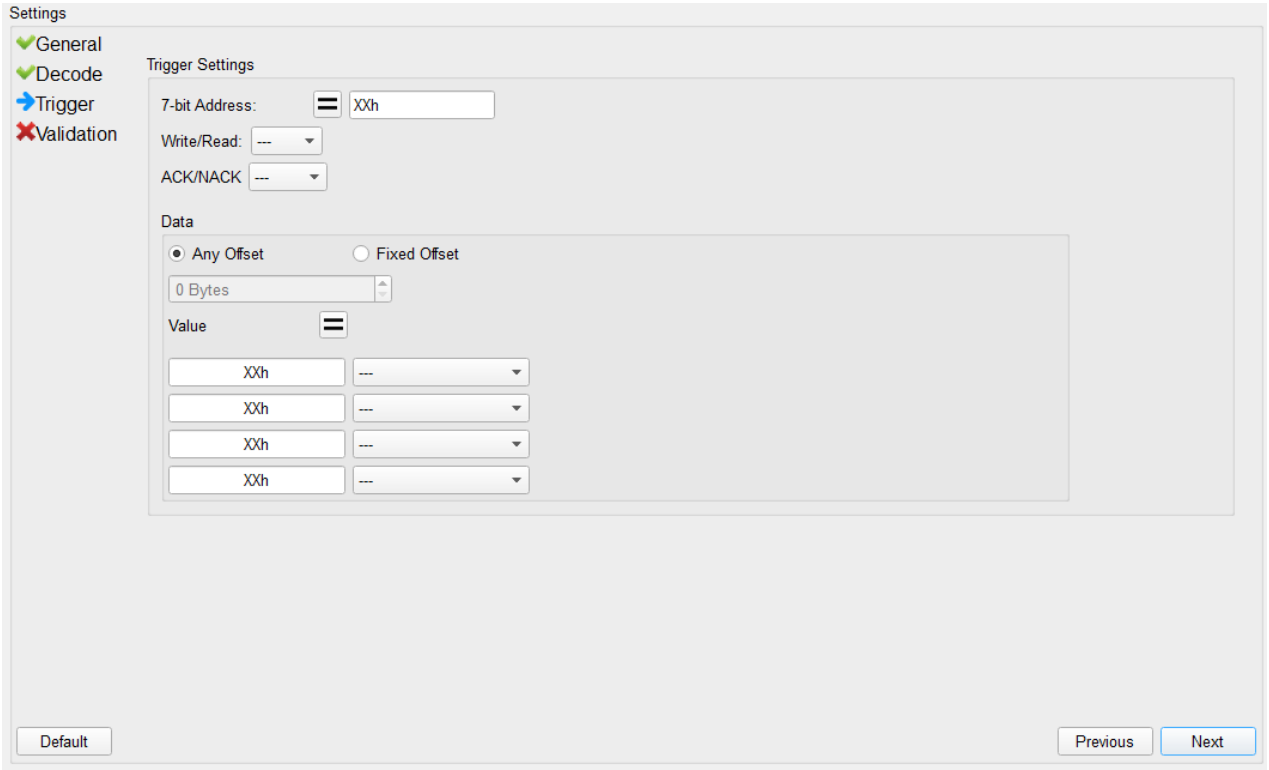
1. 一般設定：通道來源、工作電壓與速度



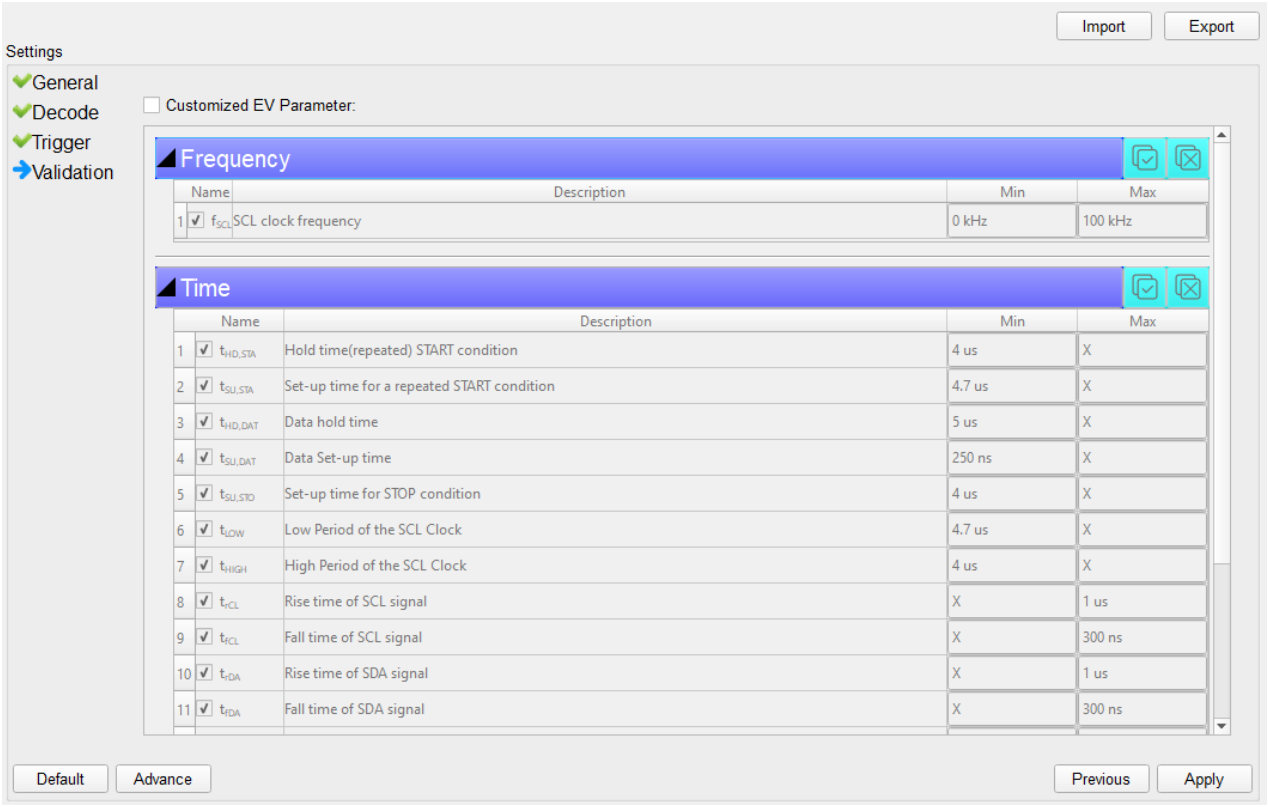
2. 解碼設定：I²C 解碼設定

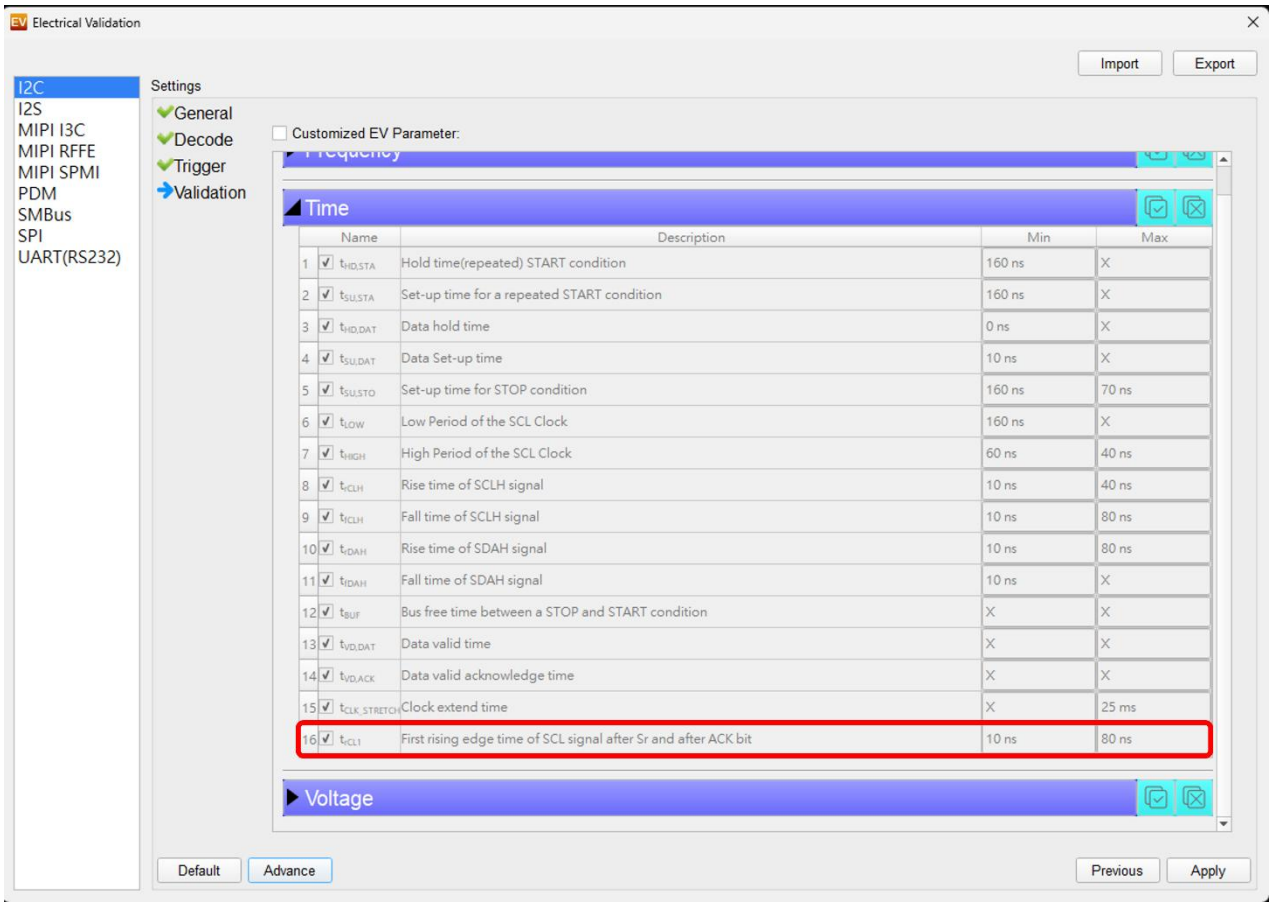


3. 觸發設定：I²C Address、Data 觸發條件



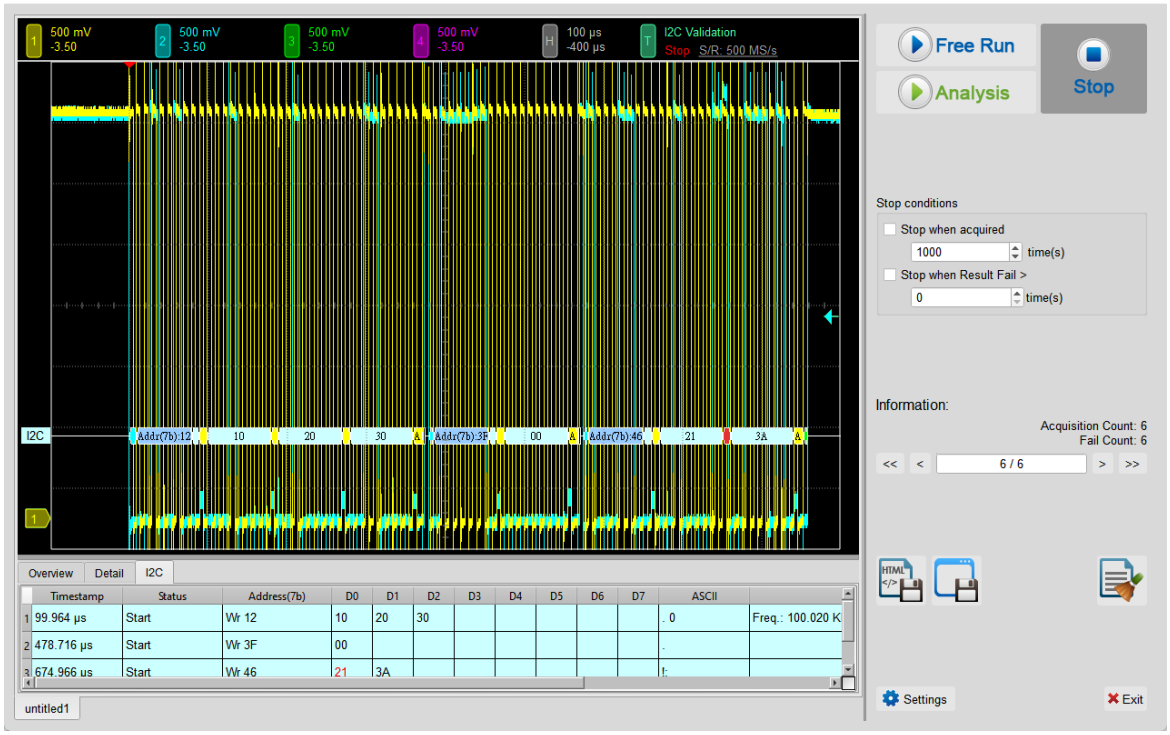
4. 驗證參數設定：頻率、時序與電壓限制



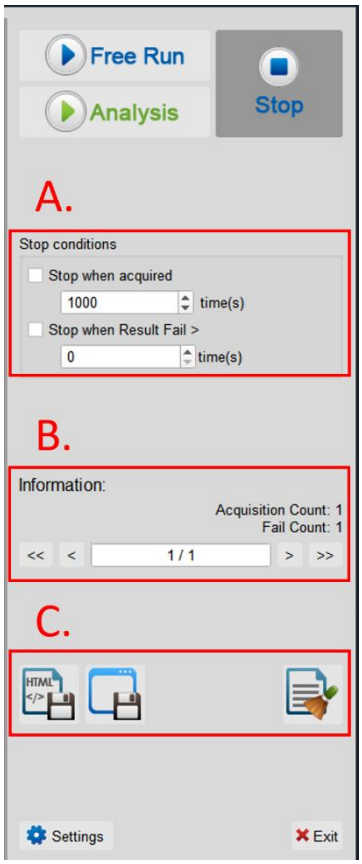


*第 16 項選項僅在 I²C 速度模式設定為**高速模式（High Speed Mode）**時可見*

5. 電氣特性驗證 軟體畫面



6. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

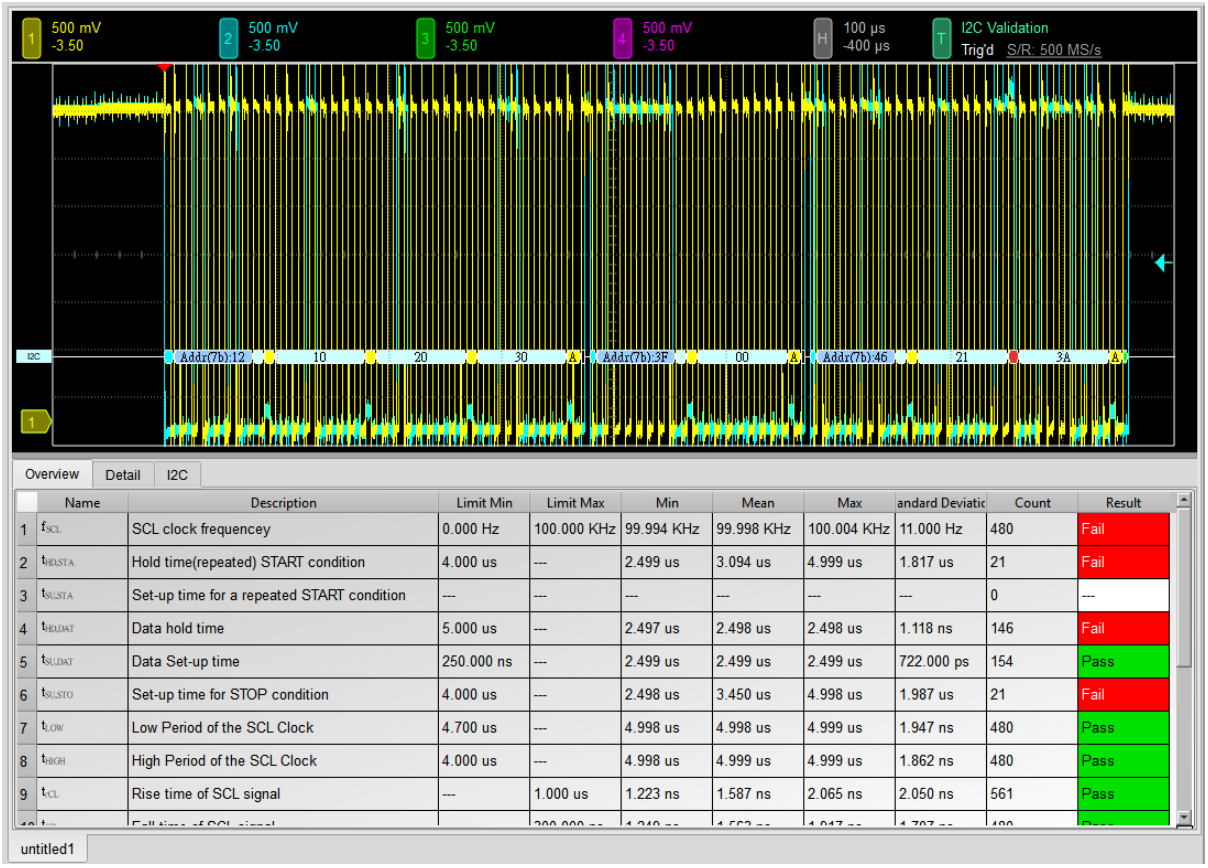
選擇查看波形

C. 儲存檔案：

儲存為 HTML 格式

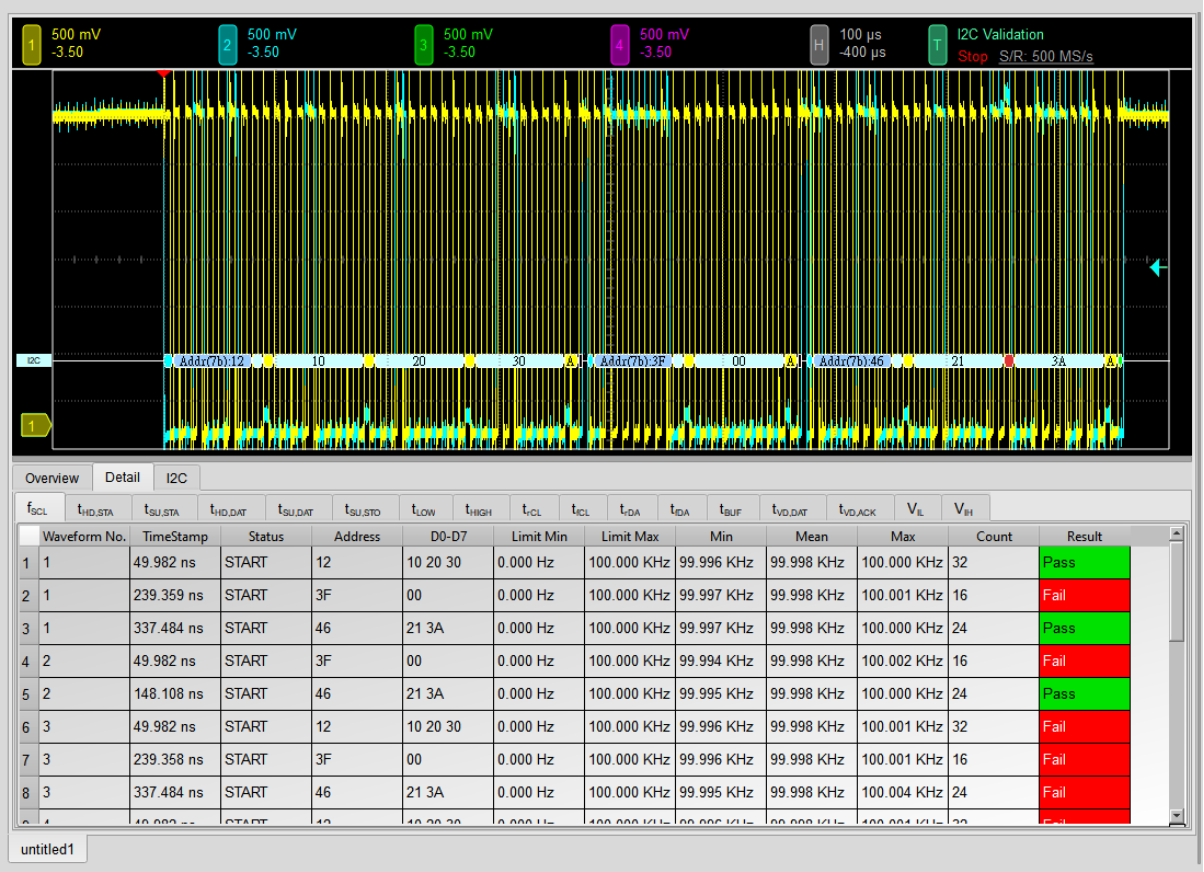
儲存為 .MOW（Acute軟體專用格式）

7. 概覽報告



	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviatic	Count	Result
1	f_{SCL}	SCL clock frequencey	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.004 KHz	11.000 Hz	480	Fail
2	$t_{HD,STA}$	Hold time(repeated) START condition	4.000 us	---	2.499 us	3.094 us	4.999 us	1.817 us	21	Fail
3	$t_{SU,STA}$	Set-up time for a repeated START condition	---	---	---	---	---	---	0	---
4	$t_{HD,DAT}$	Data hold time	5.000 us	---	2.497 us	2.498 us	2.498 us	1.118 ns	146	Fail
5	$t_{SU,DAT}$	Data Set-up time	250.000 ns	---	2.499 us	2.499 us	2.499 us	722.000 ps	154	Pass
6	$t_{SU,STO}$	Set-up time for STOP condition	4.000 us	---	2.498 us	3.450 us	4.998 us	1.987 us	21	Fail
7	t_{LOW}	Low Period of the SCL Clock	4.700 us	---	4.998 us	4.998 us	4.999 us	1.947 ns	480	Pass
8	t_{HIGH}	High Period of the SCL Clock	4.000 us	---	4.998 us	4.999 us	4.999 us	1.862 ns	480	Pass
9	t_{rCL}	Rise time of SCL signal	---	1.000 us	1.223 ns	1.587 ns	2.065 ns	2.050 ns	561	Pass

8. 詳細報告



	Waveform No.	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.000 KHz	32	Pass
2	1	239.359 ns	START	3F	00	0.000 Hz	100.000 KHz	99.997 KHz	99.998 KHz	100.001 KHz	16	Fail
3	1	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.997 KHz	99.998 KHz	100.000 KHz	24	Pass
4	2	49.982 ns	START	3F	00	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.002 KHz	16	Fail
5	2	148.108 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.995 KHz	99.998 KHz	100.000 KHz	24	Pass
6	3	49.982 ns	START	12	10 20 30	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.001 KHz	32	Fail
7	3	239.358 ns	START	3F	00	0.000 Hz	100.000 KHz	99.996 KHz	99.998 KHz	100.001 KHz	16	Fail
8	3	337.484 ns	START	46	21 3A	0.000 Hz	100.000 KHz	99.995 KHz	99.998 KHz	100.004 KHz	24	Fail

9. 波形和參考點

Waveform No.	TimeStamp	Status	Address	D0-D7
1	239.359 ns	START	3F	00

	Time	Δ Time	Volt	Δ Volt	Result
1	(489.967 µs, 499.967 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail
2	(499.967 µs, 509.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
3	(509.968 µs, 519.967 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail
4	(519.967 µs, 529.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
5	(529.968 µs, 539.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
6	(539.968 µs, 549.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
7	(549.968 µs, 559.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Fail
8	(559.968 µs, 569.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass
9	(579.968 µs, 589.968 µs)	10.000 µs	(990 mV, 990 mV)	0 V	Pass

10. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	24554
Test Date	04-17-2023 14:46:14
S/W Version	1.0.25
Protocol	I2C

```
/*****************************/
DUT INFO

Speed: 400KHz

EEPROM Communication
/*****************************/
```

Overview Results:

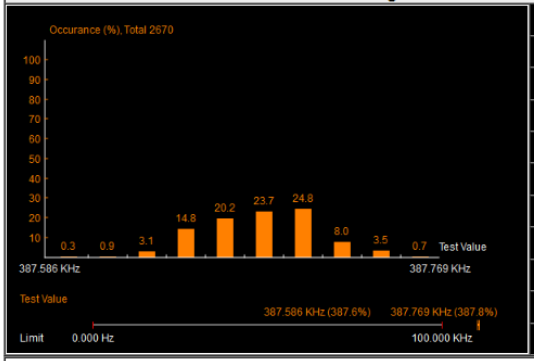
Total: 17
Pass: 9
Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCL}	SCL clock frequency	0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%	✘Fail
2	$t_{HD,STA}$	Hold time(repeated) START condition	4.000 us	---	1.538 us	1.538 us	1.539 us	427.000 ps	20	-61.6%	---	✘Fail
3	$t_{SU,STA}$	Set-up time for a repeated START condition	4.700 us	---	2.013 us	2.014 us	2.015 us	579.000 ps	10	-57.2%	---	✘Fail
4	$t_{HD,DAT}$	Data hold time	5.000 us	---	94.249 ns	247.342 ns	1.026 us	4.244 us	1575	-98.1%	---	✘Fail
5	$t_{SU,DAT}$	Data Set-up time	250.000 ns	---	472.837 ns	1.187 us	1.443 us	5.255 us	1767	18.7%	---	✔Pass
6	$t_{SU,STO}$	Set-up time for STOP condition	---	---	---	---	---	---	0	---	---	---
7	t_{LOW}	Low Period of the SCL Clock	4.700 us	---	1.539 us	1.541 us	1.543 us	9.208 ns	2670	-67.3%	---	✘Fail
8	t_{HIGH}	High Period of the SCL Clock	4.000 us	---	977.699 ns	979.666 ns	984.826 ns	20.914 ns	3040	-75.6%	---	✘Fail
9	t_{rCL}	Rise time of SCL signal	---	1.000 us	45.022 ns	48.118 ns	49.835 ns	14.531 ns	3430	---	0.5%	✔Pass
10	t_{fCL}	Fall time of SCL signal	---	300.000 ns	9.888 ns	10.237 ns	10.583 ns	1.448 ns	3430	---	0.2%	✔Pass
11	t_{rDA}	Rise time of SDA signal	---	1.000 us	37.719 ns	39.529 ns	41.848 ns	5.148 ns	927	---	0.4%	✔Pass
12	t_{fDA}	Fall time of SDA signal	---	300.000 ns	4.616 ns	6.893 ns	9.828 ns	24.035 ns	947	---	1.8%	✔Pass
13	t_{BUF}	Bus free time between a STOP and START condition	---	---	---	---	---	---	0	---	---	---
14	$t_{VD,DAT}$	Data valid time	---	3.450 us	98.898 ns	270.164 ns	1.067 us	4.200 us	1585	---	28.9%	✔Pass
15	$t_{VD,ACK}$	Data valid acknowledge time	---	3.450 us	141.017 ns	730.257 ns	1.067 us	1.344 us	91	---	28.0%	✔Pass
16	V_{IL}	Low-level input voltage	-500.000 mV	990.000 mV	-105.670 mV	27.063 mV	104.081 mV	760.863 mV	4367	26.5%	40.5%	✔Pass
17	V_{IH}	High-level input voltage	2.310 V	3.800 V	3.225 V	3.267 V	3.417 V	1.250 V	4367	61.4%	74.3%	✔Pass

f_{SCL} - Test Result: Fail
Description: SCL clock frequency

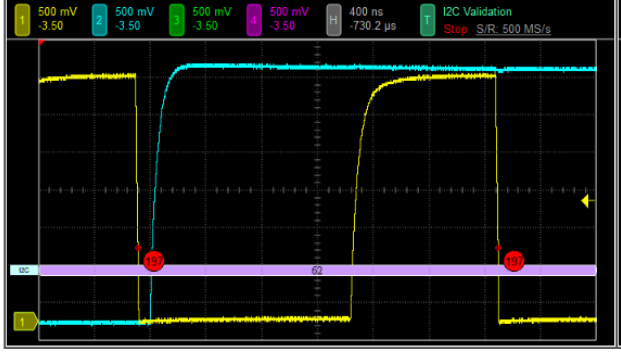
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%

Histogram

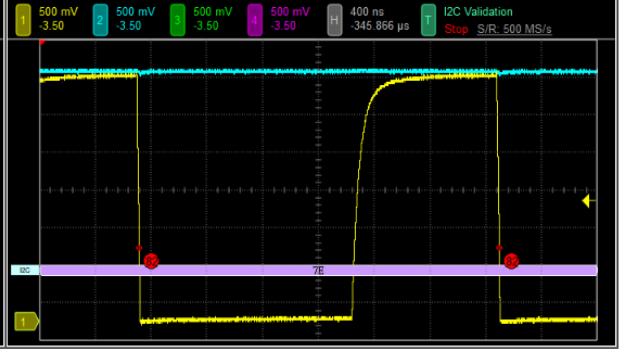


Value Range	Occurance Count
387.586 kHz ~ 387.604 kHz	9
387.604 kHz ~ 387.623 kHz	23
387.623 kHz ~ 387.641 kHz	84
387.641 kHz ~ 387.659 kHz	395
387.659 kHz ~ 387.677 kHz	539
387.677 kHz ~ 387.696 kHz	632
387.696 kHz ~ 387.714 kHz	663
387.714 kHz ~ 387.732 kHz	213
387.732 kHz ~ 387.751 kHz	94
387.751 kHz ~ 387.769 kHz	18

Min Detail Report Row: 12, Test Index: 197

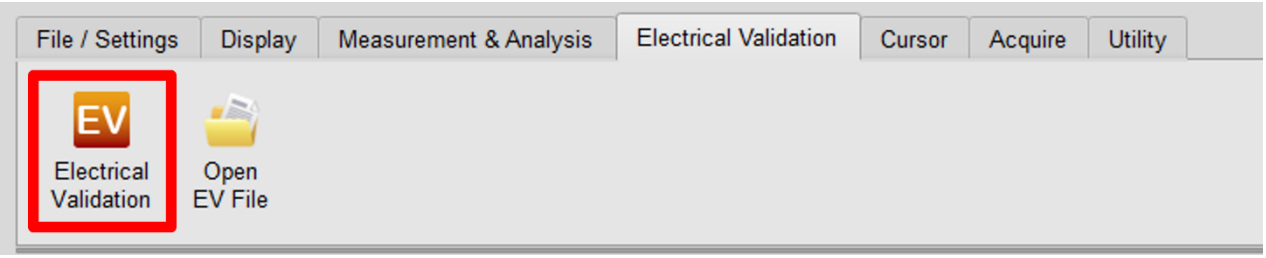


Max Detail Report Row: 10, Test Index: 82



I2S 電氣特性驗證解決方案

■ 簡介：



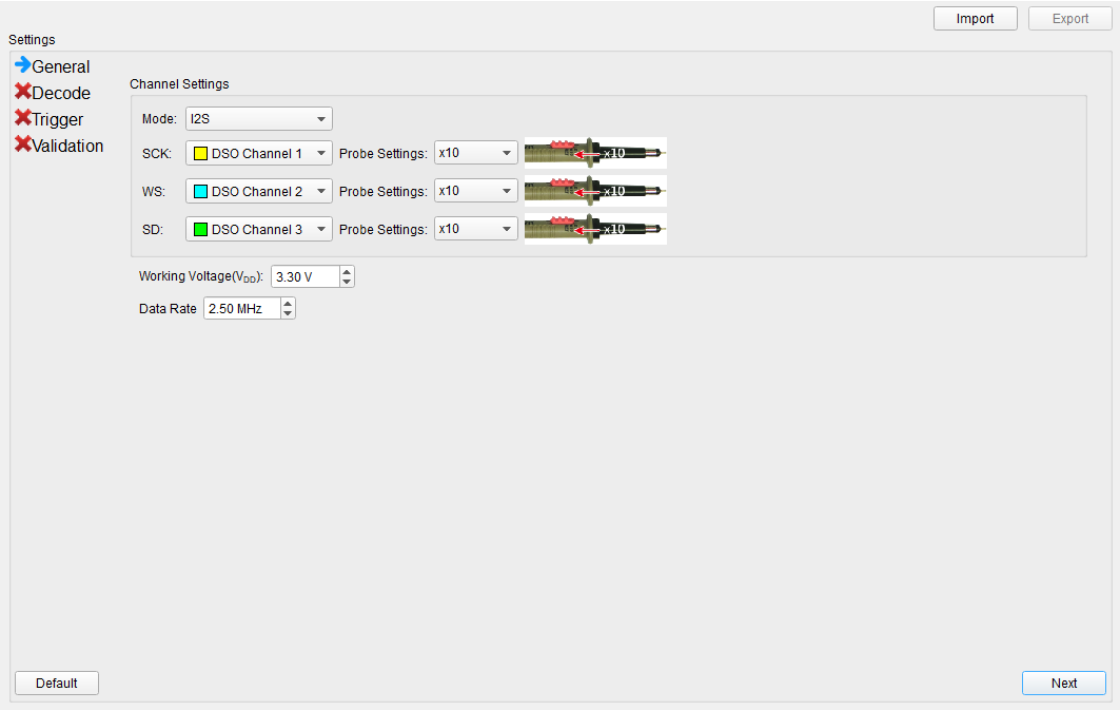
使用示波器執行 I2S 電氣特性驗證，以確保 I2S 符合既定規格。在經過長時間燒機測試後，可以確認所測試的訊號電氣特性符合規範。

I²S（Inter-IC Sound）是一種標準的序列匯流排介面，用於連接數位音訊裝置，例如音訊編碼器、數位類比轉換器（DAC）與類比數位轉換器（ADC）。它常見於嵌入式系統、音訊處理器與高品質音訊設備中。

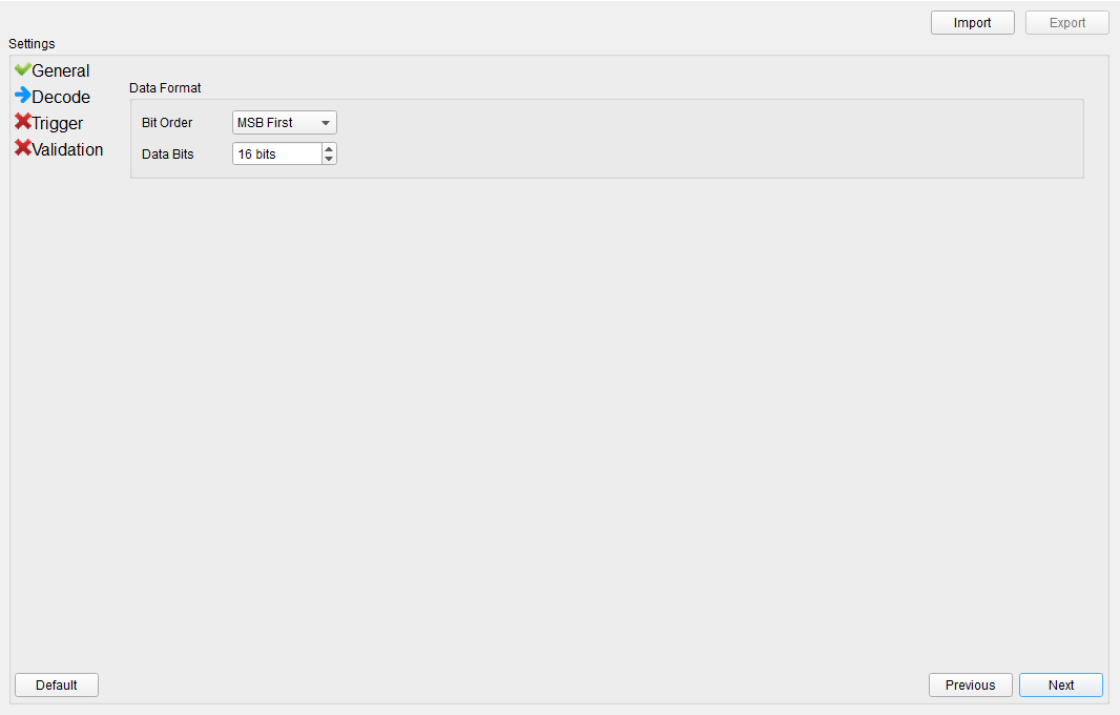
I²S 是一種結構簡單但功能強大的介面，可在裝置之間以高精度、低延遲地傳送數位音訊資料。

I2S 電氣特性驗證設定

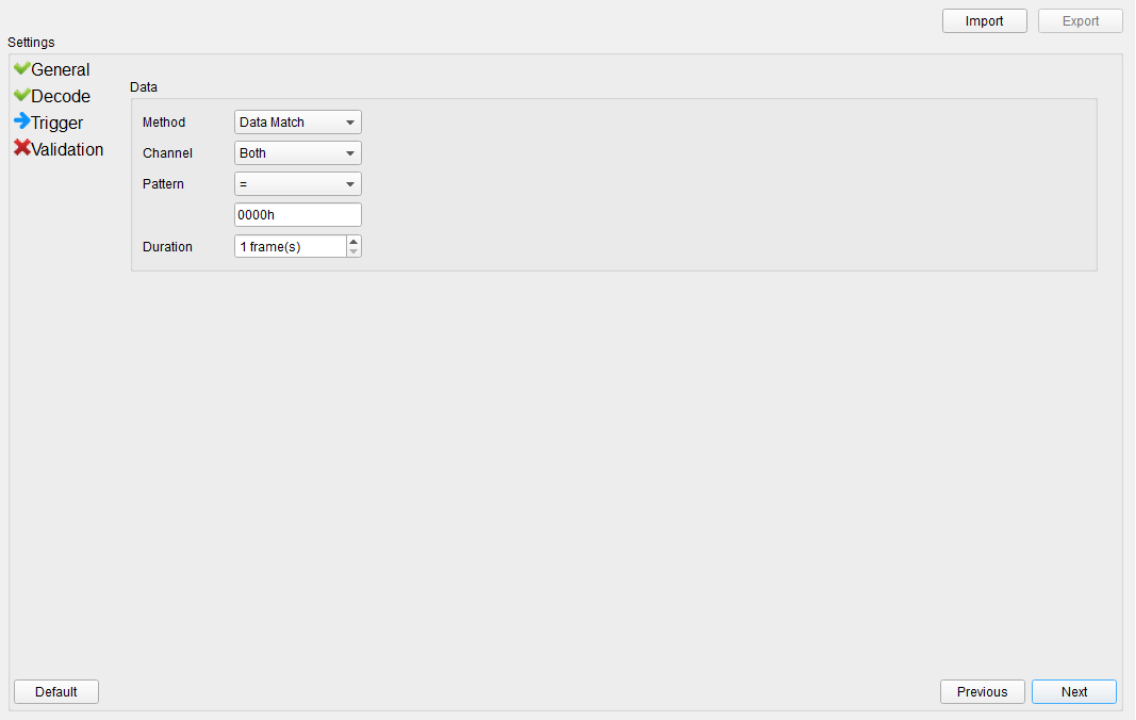
1. **一般設定**：設定匯流排配置，包括 I2S 模式類型（I2S、Left Justified、PCM、TDM）、通道設定、工作電壓與資料速率。



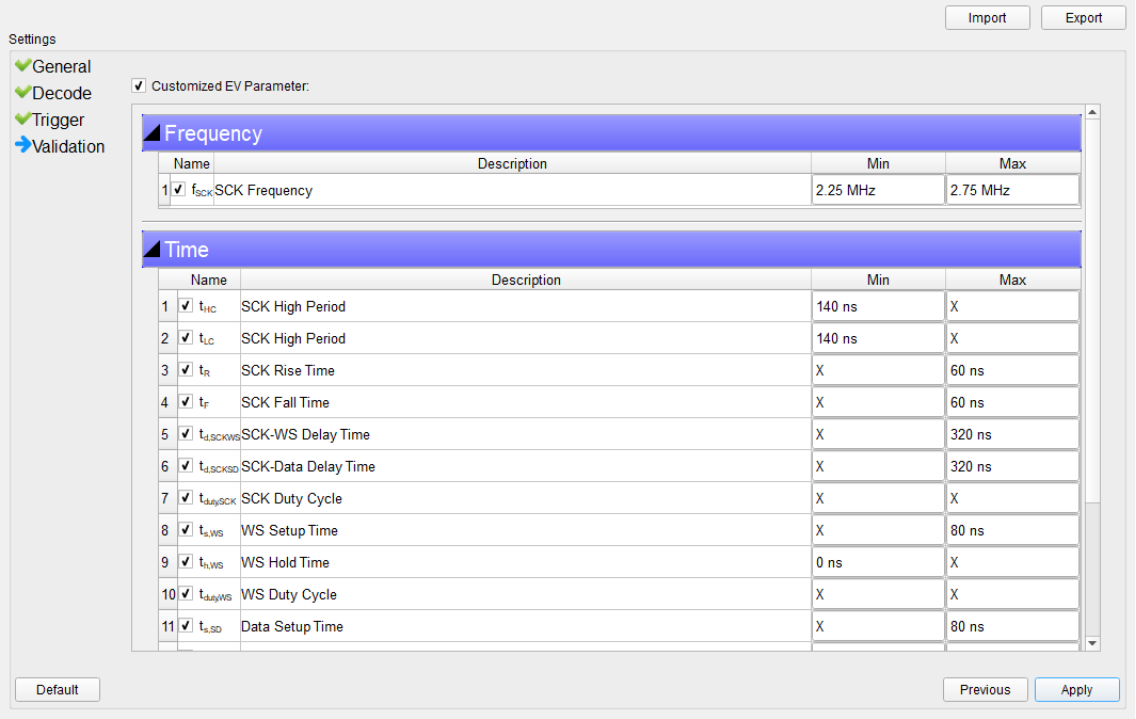
2. **解碼設定**：設定 I2S 資料格式。位元順序可選擇 MSB First 或 LSB First。資料位元數可設定為 1 到 32 位元之間。



3. **觸發設定**：設定使用者需要觸發的資料模式。資料格式已在前一頁的解碼設定中設定完成，其餘設定僅與資料樣式相關。此處共提供 6 種觸發方式：Data Match, Rising, Falling, Glitch, Mute, and Clip。



4. **驗證參數設定**



此部分提供三張特性參數表，包含：

- 頻率
- 時序參數
- 電壓要求

預設值參考自 I2S 規範 Rev3.0。下方列出所有支援的驗證參數符號與說明：

- **I2S Frequency Requirements**

Symbol	**Electrical Parameter**
f_{SCK}	SCK Clock Frequency

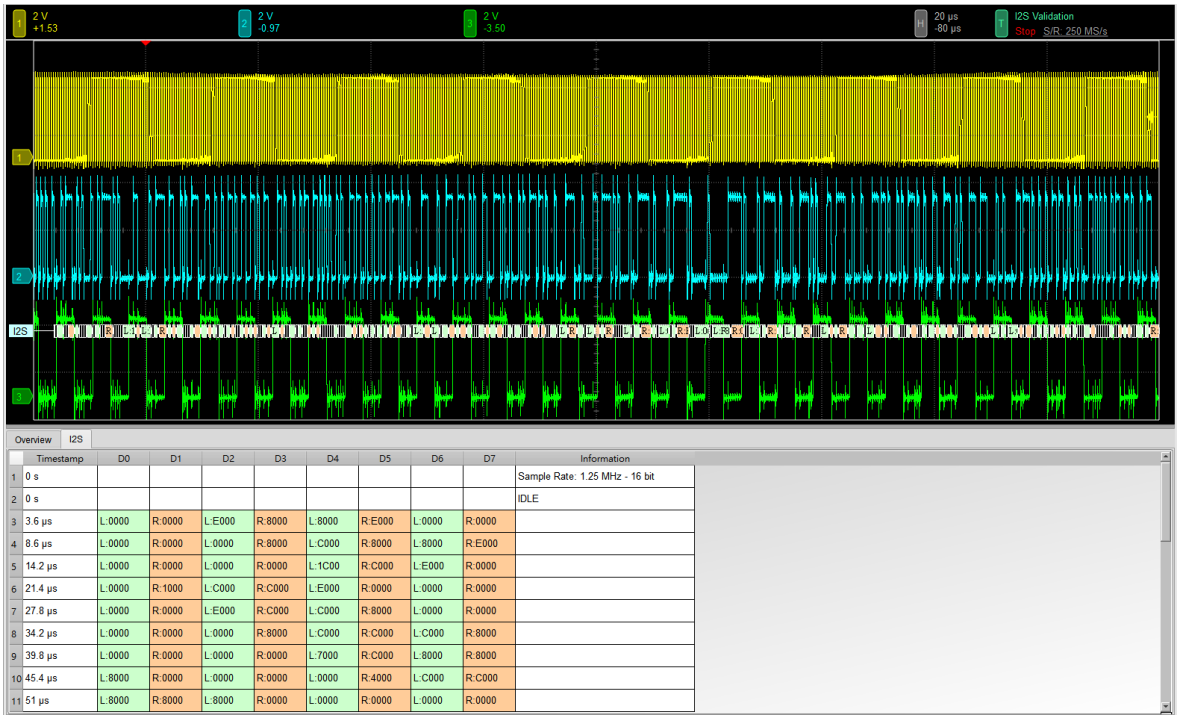
- **I2S Timing Requirements**

Symbol	**Electrical Parameter**
t_{HC}	SCK High Period
t_{LC}	SCK Low Period
t_{R}	SCK Rise Time
t_{F}	SCK Fall Time
$t_{d,SCKWS}$	SCK-WS Delay Time
$t_{duty,SCK}$	SCK Duty Cycle
$t_{s,WS}$	WS Setup Time
$t_{h,WS}$	WS Hold Time
$t_{duty,WS}$	WS Duty Cycle
$t_{s,SD}$	Data Setup Time
$t_{h,SD}$	Data Hold Time

- **I2S Voltage Requirements**

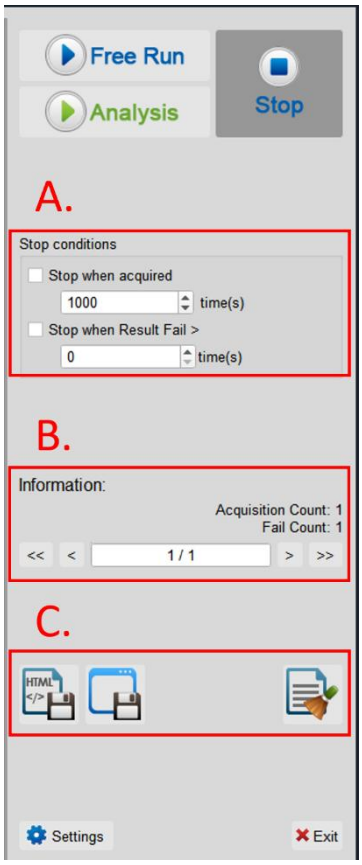
Symbol	**Electrical Parameter**
V_L	Low-Level Voltage
V_H	High-level Voltage

5. 電氣特性驗證 軟體畫面



	Timestamp	D0	D1	D2	D3	D4	D5	D6	D7	Information
1	0 s									Sample Rate: 1.25 MHz - 16 bit
2	0 s									IDLE
3	3.6 µs	L:0000	R:0000	L:E000	R:8000	L:8000	R:E000	L:0000	R:0000	
4	8.6 µs	L:0000	R:0000	L:0000	R:8000	L:C000	R:8000	L:8000	R:E000	
5	14.2 µs	L:0000	R:0000	L:0000	R:0000	L:1C00	R:C000	L:E000	R:0000	
6	21.4 µs	L:0000	R:1000	L:C000	R:C000	L:E000	R:0000	L:0000	R:0000	
7	27.8 µs	L:0000	R:0000	L:E000	R:C000	L:C000	R:8000	L:0000	R:0000	
8	34.2 µs	L:0000	R:0000	L:0000	R:8000	L:C000	R:C000	L:C000	R:8000	
9	39.8 µs	L:0000	R:0000	L:0000	R:0000	L:7000	R:C000	L:8000	R:8000	
10	45.4 µs	L:8000	R:0000	L:0000	R:0000	L:0000	R:4000	L:C000	R:C000	
11	51 µs	L:8000	R:8000	L:8000	R:0000	L:0000	R:0000	L:0000	R:0000	

6. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

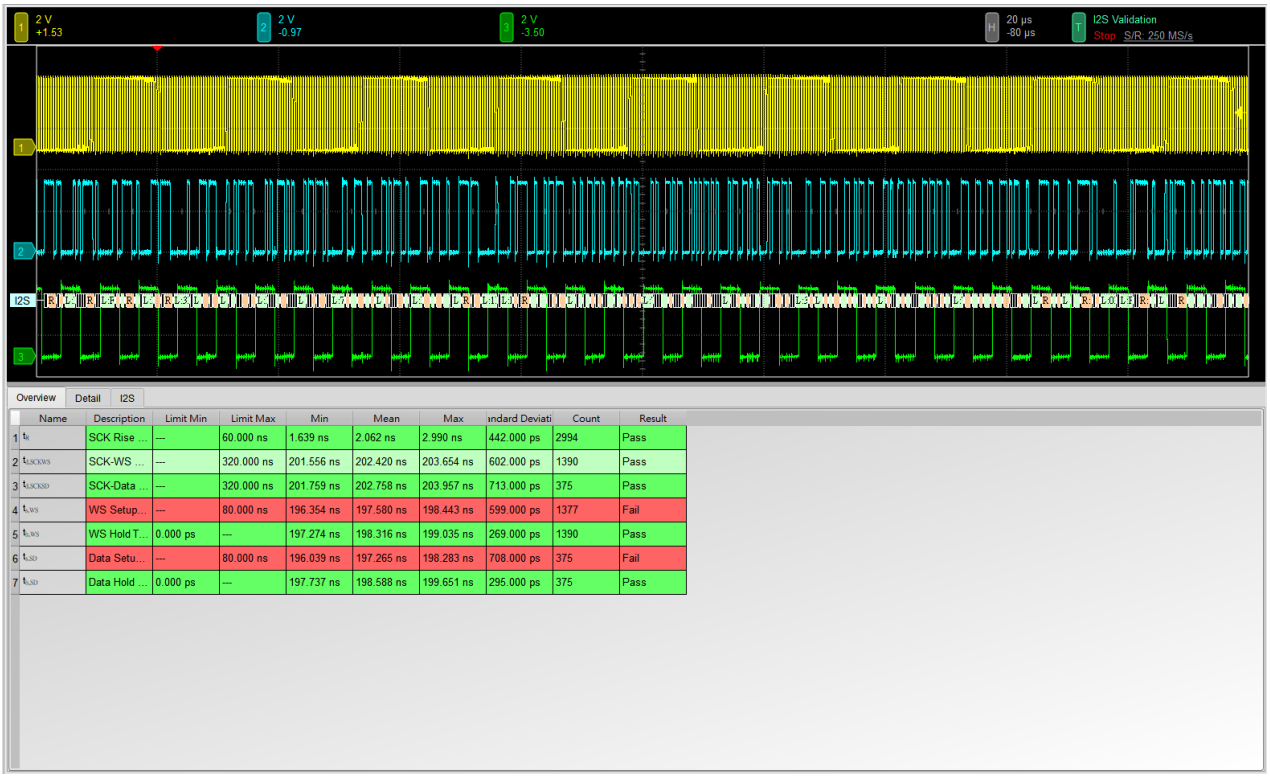
選擇查看波形

C. 儲存檔案：

儲存為 HTML 格式

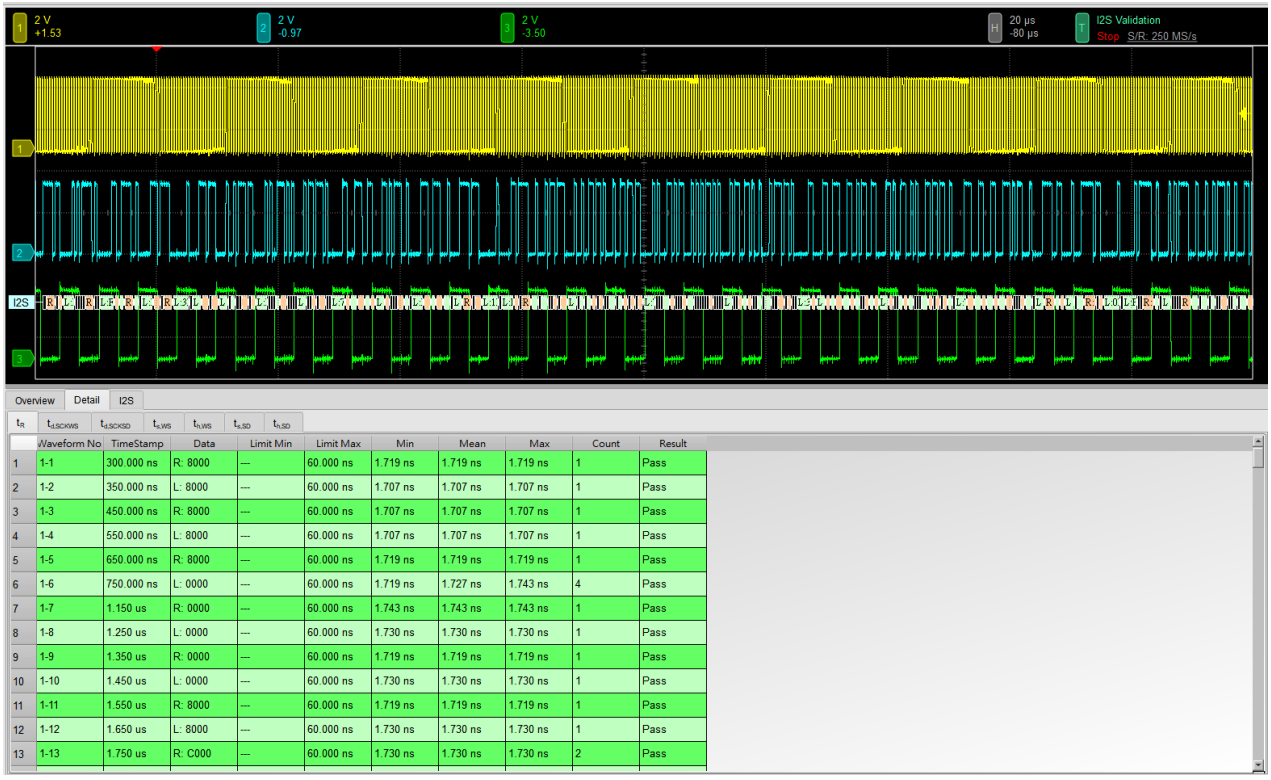
儲存為 .MOW（Acute軟體專用格式）

7. 概覽報告



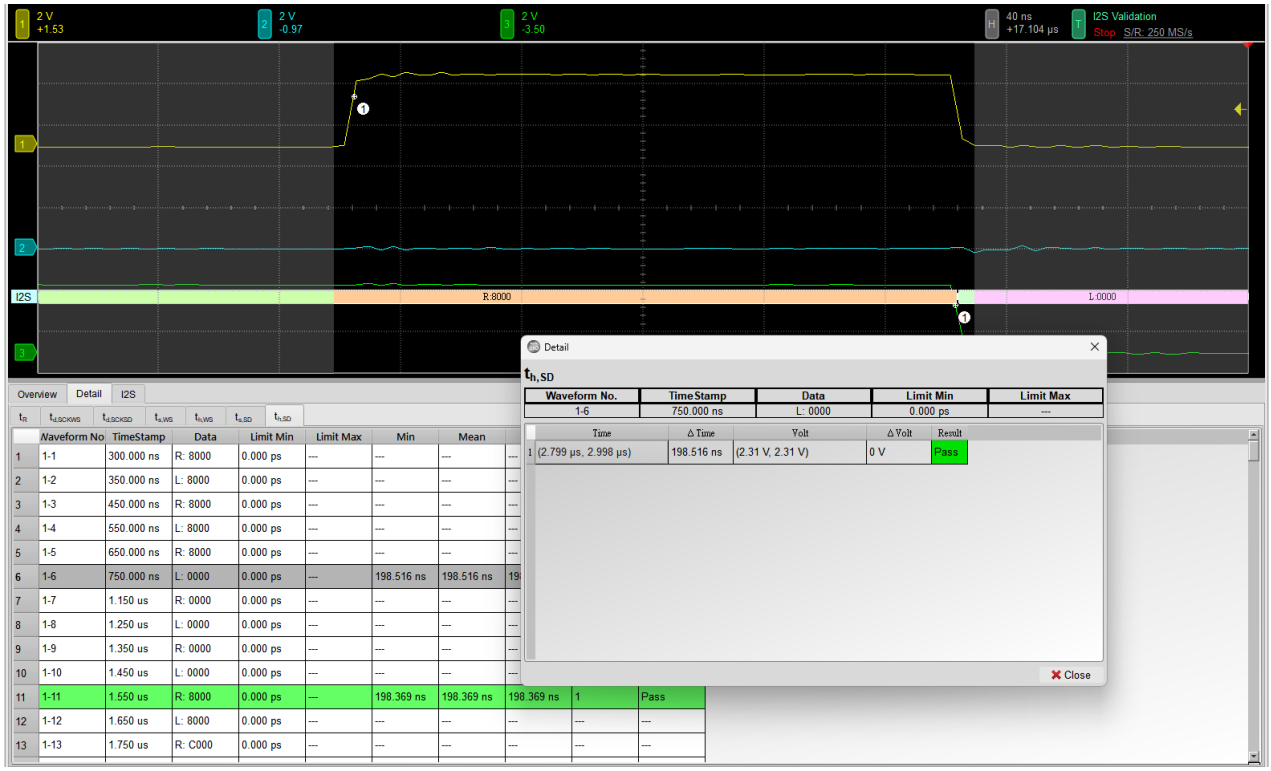
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ındard Deviati	Count	Result
1	t_R	SCK Rise ...	---	60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994	Pass
2	t_{LSCKWS}	SCK-WS ...	---	320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390	Pass
3	t_{LSCKSD}	SCK-Data ...	---	320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375	Pass
4	t_{LWS}	WS Setup...	---	80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377	Fail
5	t_{LWS}	WS Hold T...	0.000 ps	---	197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390	Pass
6	t_{LSD}	Data Setu...	---	80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375	Fail
7	t_{LSD}	Data Hold ...	0.000 ps	---	197.737 ns	198.588 ns	199.651 ns	295.000 ps	375	Pass

8. 詳細報告



	Waveform No	TimeStamp	Data	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	300.000 ns	R: 8000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
2	1-2	350.000 ns	L: 8000	---	60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass
3	1-3	450.000 ns	R: 8000	---	60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass
4	1-4	550.000 ns	L: 8000	---	60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass
5	1-5	650.000 ns	R: 8000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
6	1-6	750.000 ns	L: 0000	---	60.000 ns	1.719 ns	1.727 ns	1.743 ns	4	Pass
7	1-7	1.150 us	R: 0000	---	60.000 ns	1.743 ns	1.743 ns	1.743 ns	1	Pass
8	1-8	1.250 us	L: 0000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass
9	1-9	1.350 us	R: 0000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
10	1-10	1.450 us	L: 0000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass
11	1-11	1.550 us	R: 8000	---	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass
12	1-12	1.650 us	L: 8000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass
13	1-13	1.750 us	R: C000	---	60.000 ns	1.730 ns	1.730 ns	1.730 ns	2	Pass

9. 波形和參考點



10. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 13:34:37
S/W Version	1.8.62
Protocol	I2S

Overview Results:

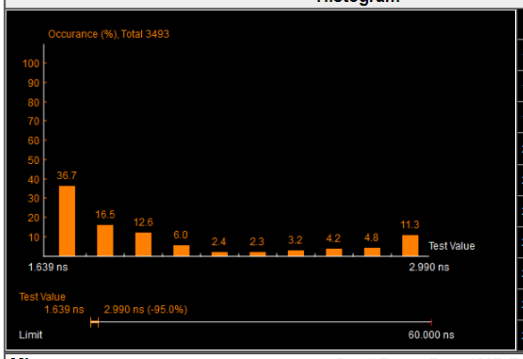
Total: 7
Pass: 5
Fail: 2

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	t_R	SCK Rise Time	---	60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994	---	-95.0%	Pass
2	$t_{d,SCKWS}$	SCK-WS Delay Time	---	320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390	---	-36.4%	Pass
3	$t_{d,SCKSD}$	SCK-Data Delay Time	---	320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375	---	-36.3%	Pass
4	$t_{s,WS}$	WS Setup Time	---	80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377	---	148.1%	Fail
5	$t_{h,WS}$	WS Hold Time	0.000 ps	---	197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390	---	---	Pass
6	$t_{s,SD}$	Data Setup Time	---	80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375	---	147.9%	Fail
7	$t_{h,SD}$	Data Hold Time	0.000 ps	---	197.737 ns	198.588 ns	199.651 ns	295.000 ps	375	---	---	Pass

t_R - Test Result: Pass
Description: SCK Rise Time

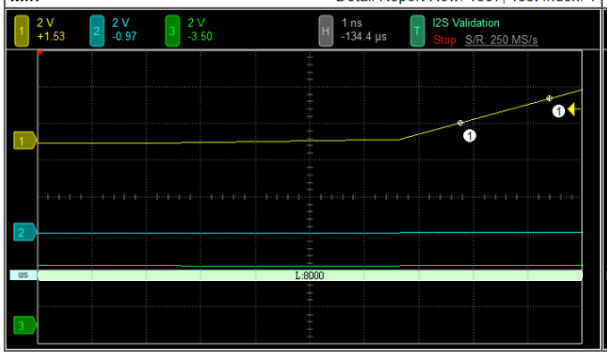
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
---	60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994	---	-95.0%

Histogram

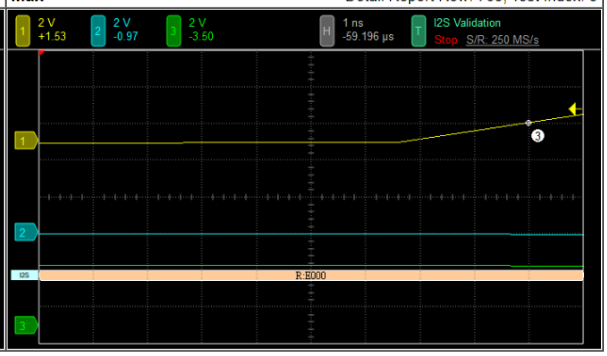


Value Range	Occurance Count
1.639 ns ~ 1.774 ns	1283
1.774 ns ~ 1.909 ns	578
1.909 ns ~ 2.044 ns	439
2.044 ns ~ 2.179 ns	210
2.179 ns ~ 2.314 ns	84
2.314 ns ~ 2.450 ns	80
2.450 ns ~ 2.585 ns	112
2.585 ns ~ 2.720 ns	147
2.720 ns ~ 2.855 ns	167
2.855 ns ~ 2.990 ns	393

Min Detail Report Row: 1337, Test Index: 1

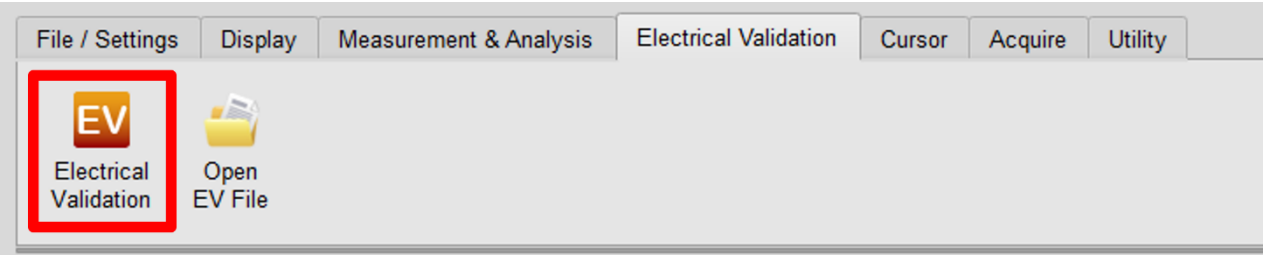


Max Detail Report Row: 765, Test Index: 3



MIPI I3C 電氣特性驗證解決方案

■ 簡介：

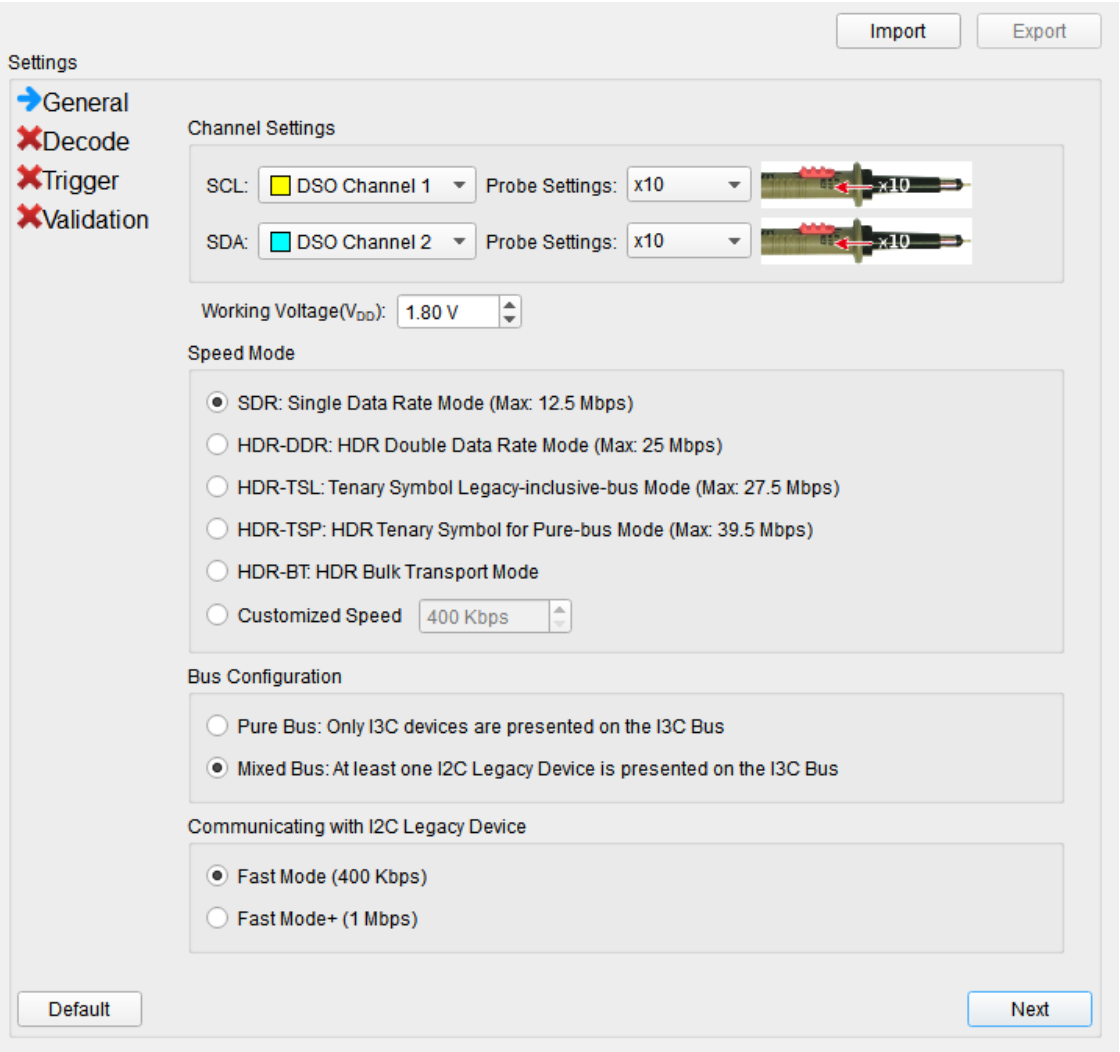


MIPI I3C 向下相容許多傳統 I²C 裝置，但同時 I3C 裝置還支援更高速傳輸速率（SCL 頻率可達 12.5 MHz）與全新的通訊模式。MIPI I3C 工作模式包含 **Single Data Rate (SDR) Mode**, **High Data Rate (HDR) Mode**. HDR Mode 進一步細分為 **Dual Data Rate (HDR-DDR) Mode**, **Ternary Symbol Legacy Mode (HDR-TTL) Mode**, **Ternary Symbol Pure-bus (HDR-TSP) Mode**, **Bulk Transport (HDR-BT) Mode**.

MIPI I3C 電氣特性驗證提供多項符合 MIPI I3C 規格的電氣測量項目（目前支援 MIPI I3C 版本 1.1.1）。

MIPI I3C Electrical Validation Settings:

1. 一般設定：設定通道來源、工作電壓與傳輸速率。



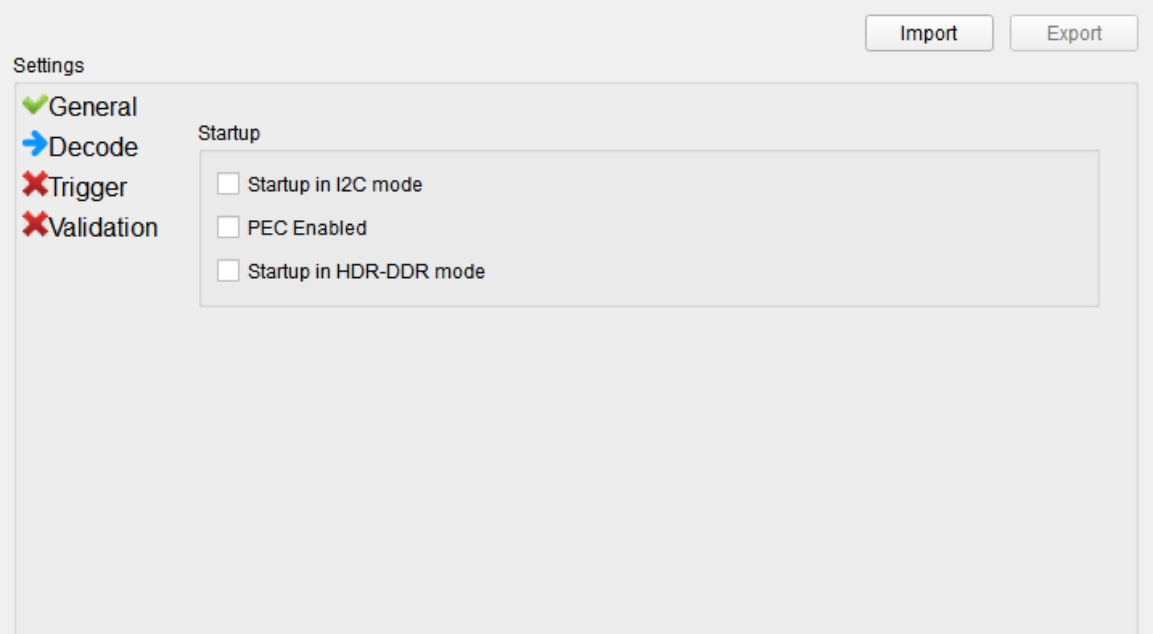
在此部分中，所選的速度模式會影響驗證所需的取樣率，同時也會影響後續「驗證設定」部分中的時序規格表。例如，在 HDR-TSL 與 HDR-TSP 模式下，將額外顯示專屬的時序規格。

13	✓	t_{EDGE}	Edge-to-Edge Period	32 ns	X
14	✓	t_{SKEW}	Allow Difference Between Signals for 'Simultaneous' Change	X	12.8 ns
15	✓	t_{EYE}	Stable Condition Between Signals	12 ns	X
16	✓	t_{SYMBOL}	Time Between Successive Symbols	32 ns	X
17	✓	t_{CLOCK}	Symbol Clock	77.5 ns	X

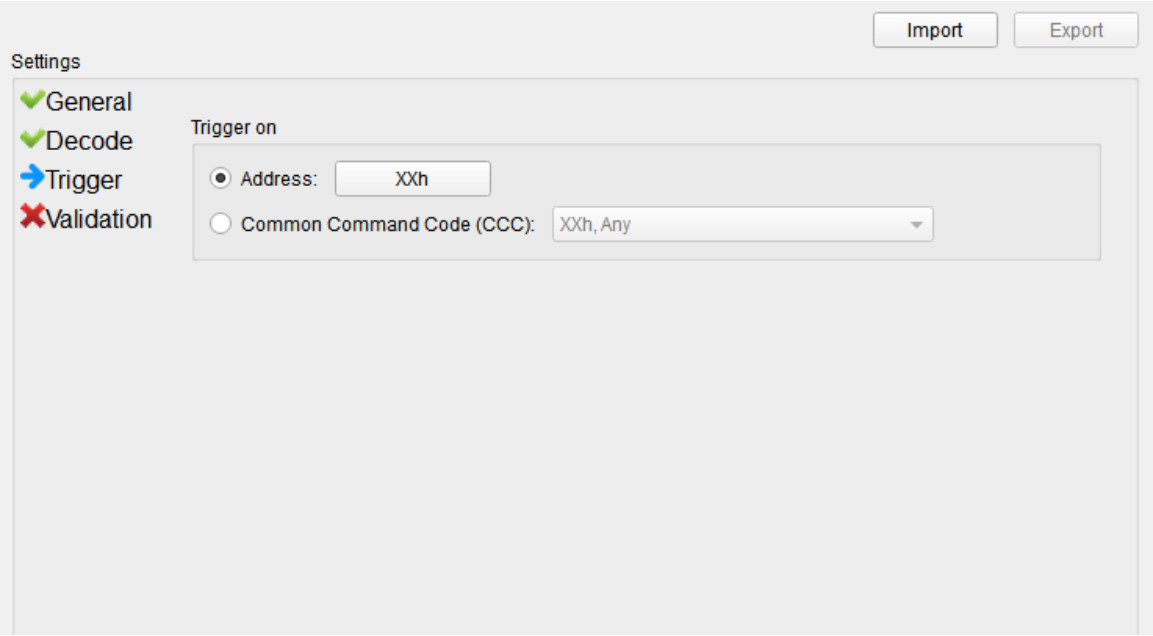
此外，在「Bus Configuration」中需指定匯流排上連接的裝置類型：

- **純 I3C 匯流排（Pure-Bus）**：不需要 I²C 時序規格。
- **混合匯流排（Mixed Bus）**：需加入 I²C 相容裝置的時序規格，預設值採用 Fast Mode（Fm）或 Fast Mode+（Fm+）設定，與 I²C 驗證設定相同。

2. 解碼設定

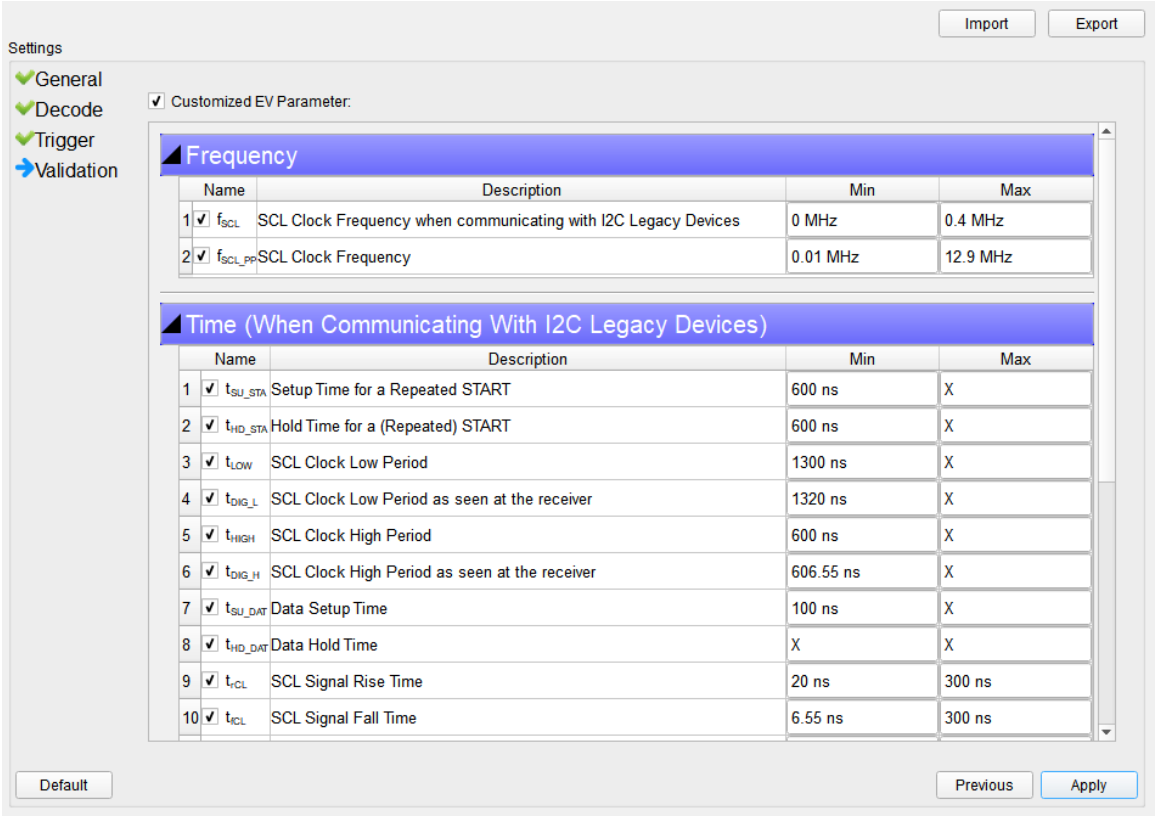


3. 觸發設定



若需要分析特定裝置位址，可設定特定位置為觸發條件。如圖中 "XX" 表示「任意」的位元，將會觸發所有位址。此外亦支援針對常用命令碼（CCC）的觸發，可透過廣播位址 7'h7E 指定。

4. 驗證參數設定



本部分共包含五種參數表：

- Frequency
- I3C timing requirements when communicating with I²C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

若為純 I3C 匯流排，則不會顯示與 I²C 裝置相關的時序表，也不會顯示 f_{SCL} 頻率參數。

MIPI I3C Frequency Requirements

Symbol	Electrical Parameter
f_{SCL}	SCL Clock Frequency when communicating with I²C Legacy Devices[1]
t_{SCL_PP}	SCL Clock Frequency
t_{BT_FREQ}	HDR-BT SCL Clock Frequency

MIPI I3C Timing Requirements When Communicating With I²C Legacy Devices[1]

Symbol		Electrical Parameter
t_{SU_STA}		Setup Time for a REPEATED START
t_{HD_STA}		Hold Time for a (REPEATED) START
t_{LOW}		SCL Clock Low Period
t_{DIG_L}		SCL Clock Low Period as seen at the receiver
t_{HIGH}		SCL Clock High Period
t_{DIG_H}		SCL Clock High Period as seen at the receiver
t_{SU_DAT}		Data Setup Time
t_{HD_DAT}		Data Hold Time
t_{rCL}		SCL Signal Rise Time
t_{fCL}		SCL Signal Fall Time
t_{rDA}		SDA Signal Rise Time
t_{rDA_OD}		SDA Signal Rise Time (Open Drain)
t_{fDA}		SDA Signal Fall Time
t_{SU_STO}		Setup Time for STOP
t_{BUF}		Bus Free Time Between a STOP and a START
t_{SPIKE}		Pulse Width of Spikes that Spike Filter Must Suppress

[1] Only available when the bus configuration is set to Mixed Bus (i.e. at least one I²C legacy device is presented on the I3C bus).

MIPI I3C Open Drain Timing Requirements

Symbol	Electrical Parameter
t_{LOW_OD}	SCL Clock Low Period
$t_{DIG\_OD\_L}$	SCL Clock Low Period as seen at the receiver
t_{HIGH_INIT}	High Period of SCL Clock (for First Broadcast Address)
t_{HIGH_OD}	SCL Clock High Period
$t_{DIG\_OD\_H}$	SCL Clock High Period as seen at the receiver
t_{fDA_OD}	SDA Data Fall Time
t_{SU_OD}	SDA Data Setup Time During Open Drain Mode
t_{CAS}	Clock After START (S) Condition
t_{CBP}	Clock Before STOP (P) Condition
$t_{CRHPOverlap}$	Active Controller to Secondary Overlap time during handoff
t_{AVAL}	Bus Available Condition
t_{IDLE}	Bus Idle Condition
$t_{NEWCRLock}$	Time Interval Where New Controller Not Driving SDA Low

MIPI I3C Push-Pull Timing Requirements

Symbol	Electrical Parameter
t_{LOW}	SCL Clock Low Period
t_{DIG_L}	SCL Clock Low Period as seen at the receiver
t_{HIGH}	SCL Clock High Period
t_{DIG_H}	SCL Clock High Period as seen at the receiver
t_{SCO}	Clock in to Data Out for Target
t_{CR_PP}	SCL Clock Rise Time
t_{CF_PP}	SCL Clock Fall Time
$t_{HD\_PP\_Controller}$	SDA Signal Data Hold (Controller)
$t_{HD\_PP\_Target}$	SDA Signal Data Hold (Target)
t_{SU_PP}	SDA Signal Data Setup
t_{CASr}	Clock After Repeated START (Sr) Condition
t_{CBSr}	Clock Before Repeated START (Sr) Condition
t_{BT_HO}	HDR-BT Master to Slave Hand Off Delay
t_{BT_STALL}	HDR-BT Clocked Not-Ready Data-Block Headers

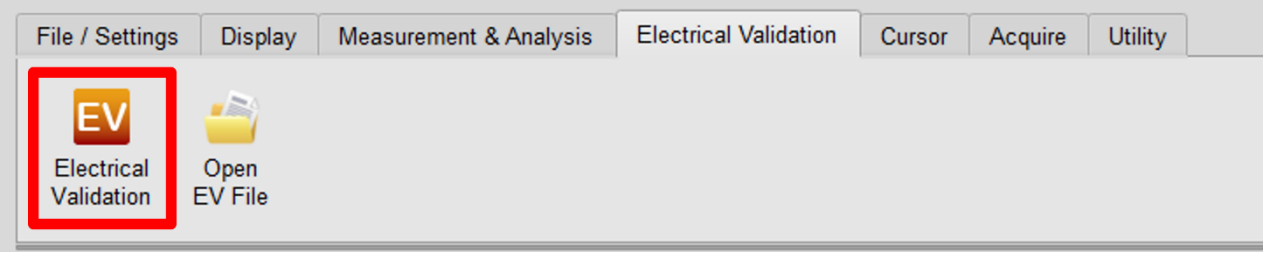
MIPI I3C I/O Stage Characteristics Voltage Requirements

Symbol	Electrical Parameter
V_{IL}	Low-Level Input Voltage
V_{IH}	High-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage

5. 電氣特性驗證 軟體畫面

MIPI RFFE 電氣特性驗證解決方案

■ 簡介：

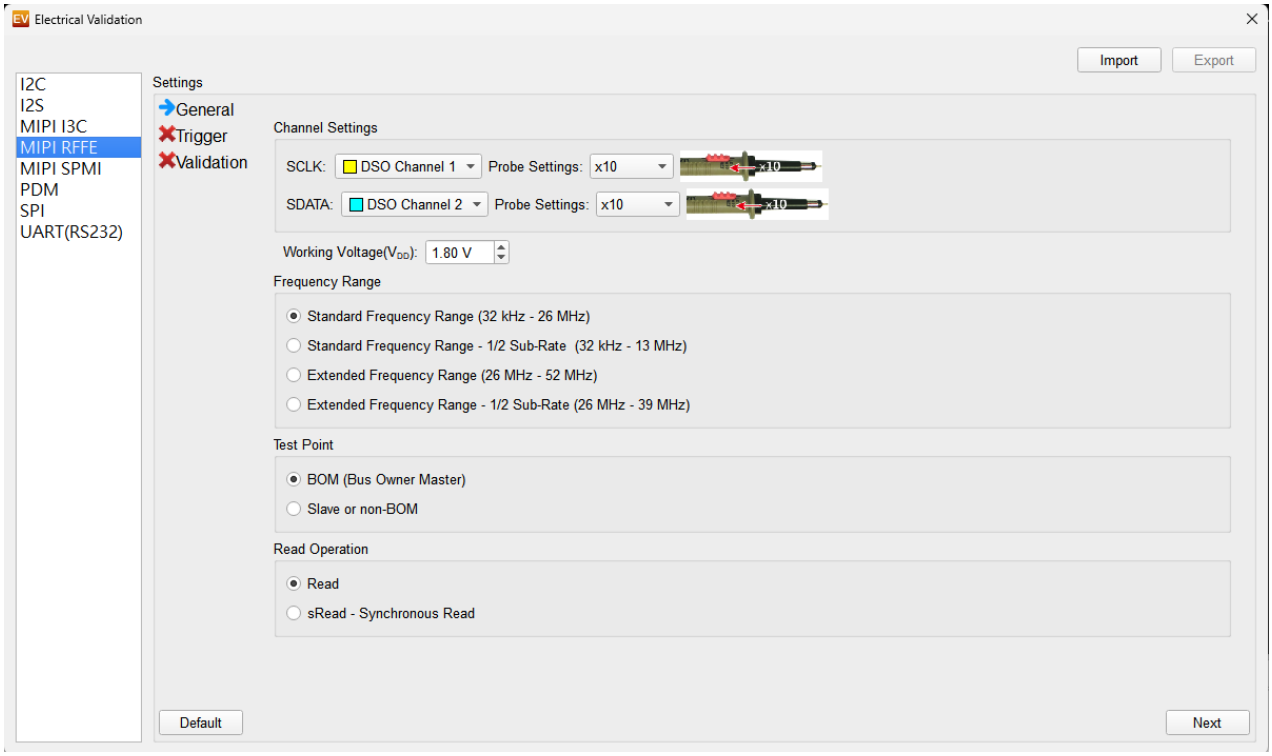


MIPI RFFE（Radio Frequency Front-End）是由 MIPI 聯盟所制定的標準規範，用以定義行動裝置（如智慧型手機和平板電腦）中基頻處理器與射頻前端模組之間的通訊標準。這是 MIPI (Mobile Industry Processor Interface) 標準家族的重要部分，涵蓋多種針對行動與嵌入式設備中元件之間通訊效率所設計的標準。

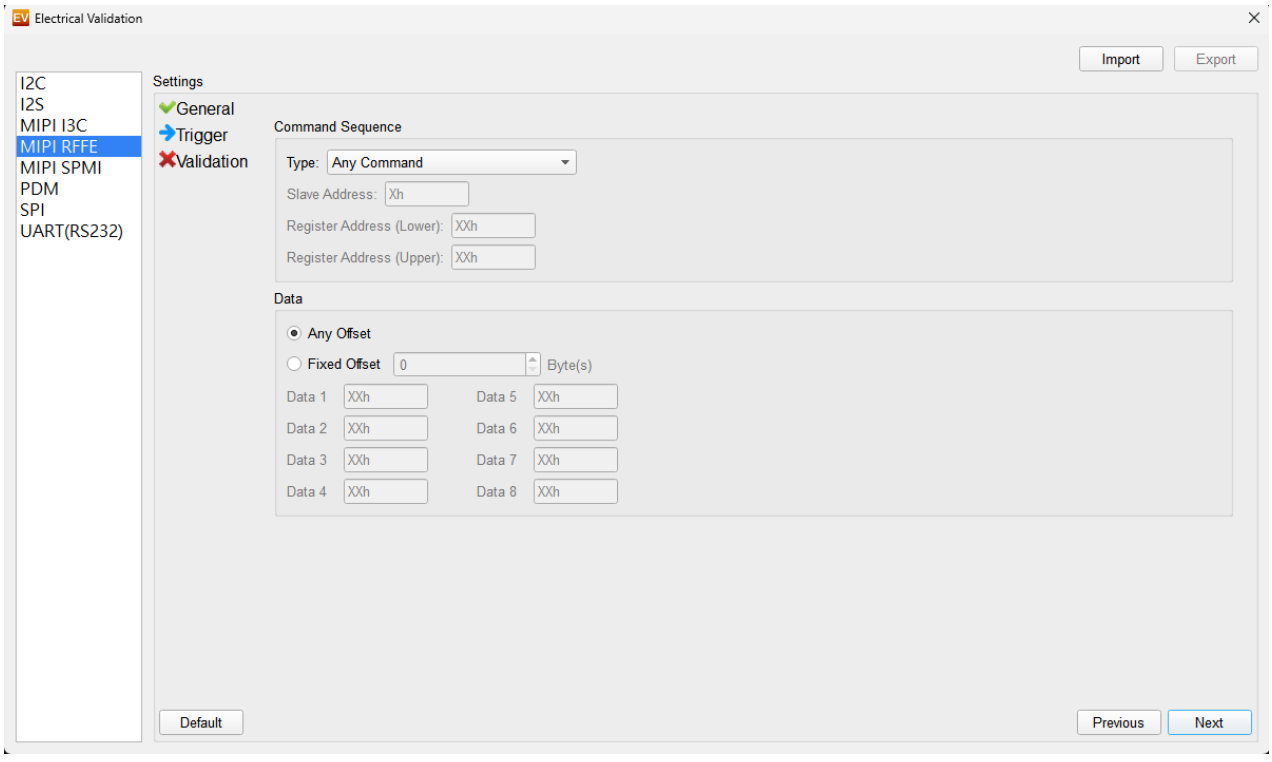
MIPI RFFE 是現代無線設備的關鍵技術，提供一個標準化且高效的介面，用於控制無線通訊系統中的射頻前端元件。

MIPI RFFE 電氣特性驗證設定：

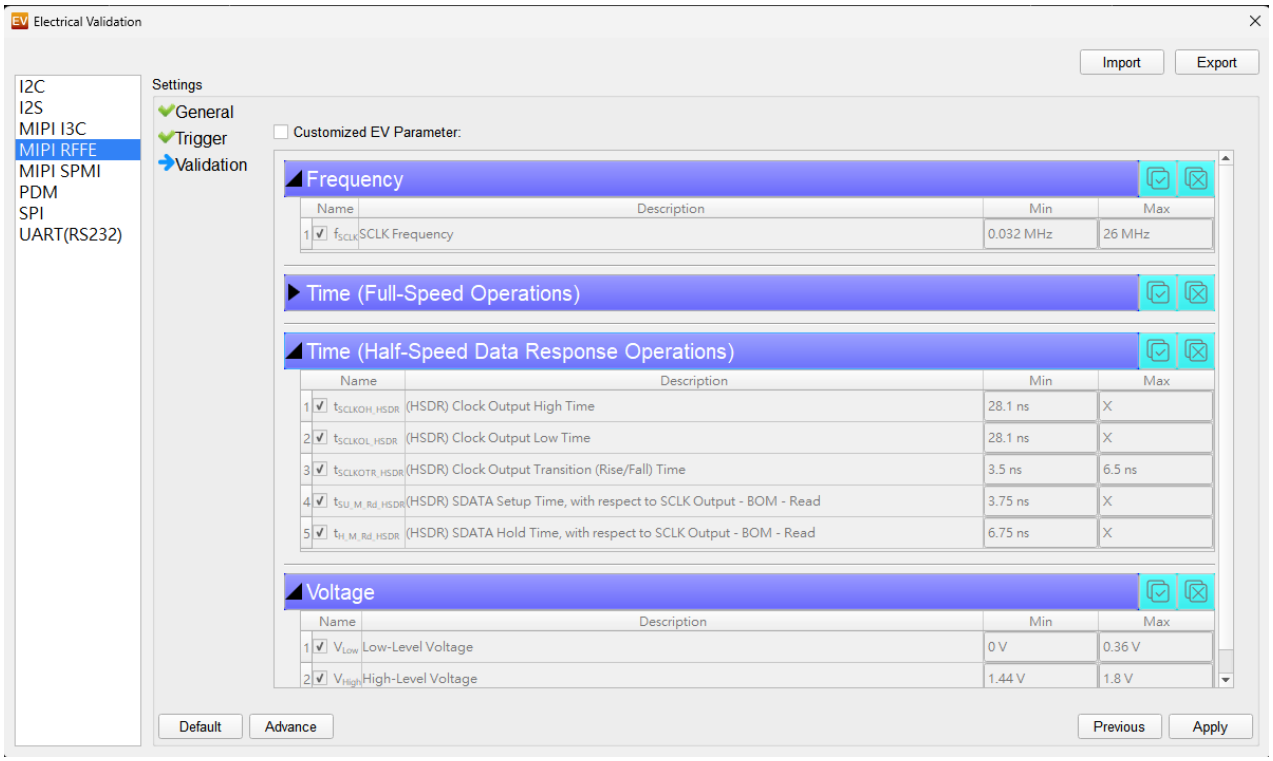
1. 一般設定：設定通道來源、工作電壓、頻率範圍、Test Point 和 Read Operation。



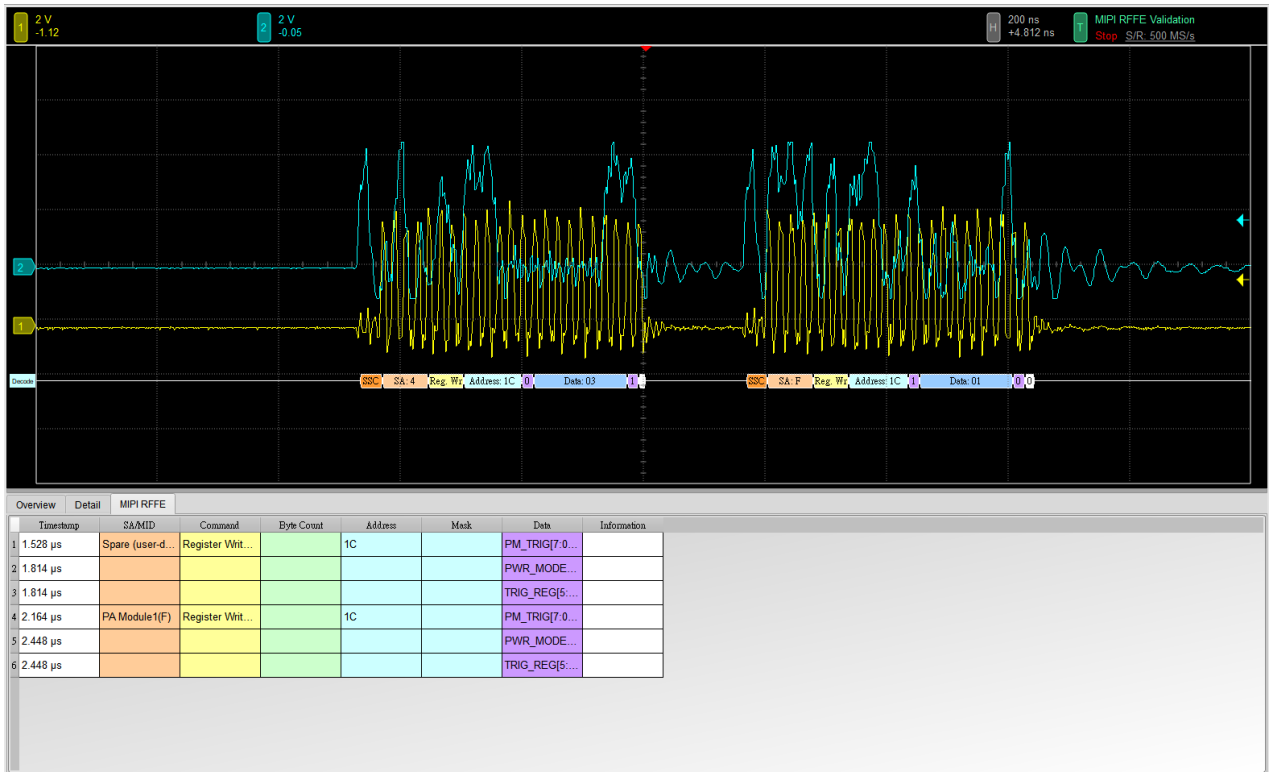
2. 觸發設定



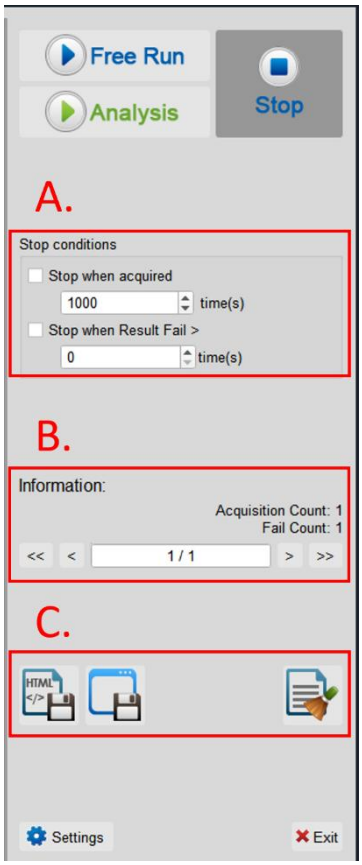
3. 驗證設定：包含電壓、時序與頻率的限制條件



4. 電氣特性驗證 軟體畫面



5. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

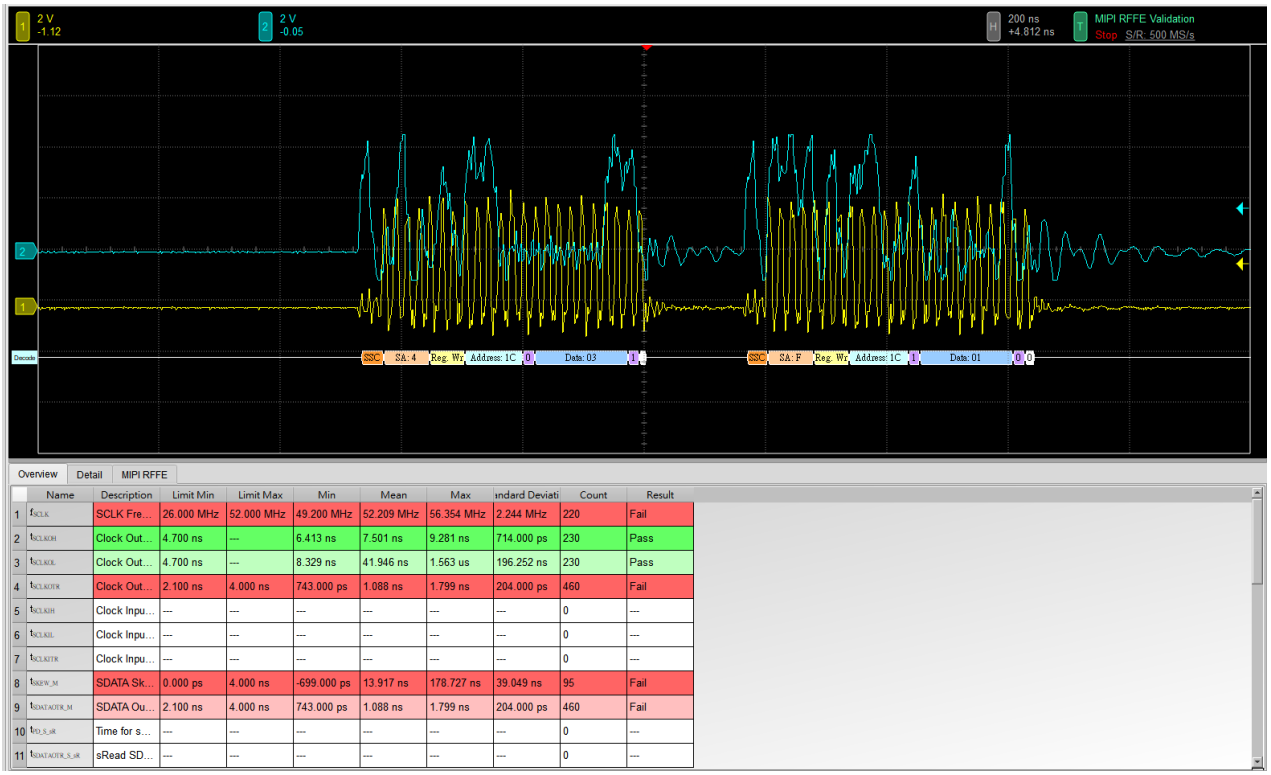
選擇查看波形

C. 儲存檔案：

儲存為 HTML 格式

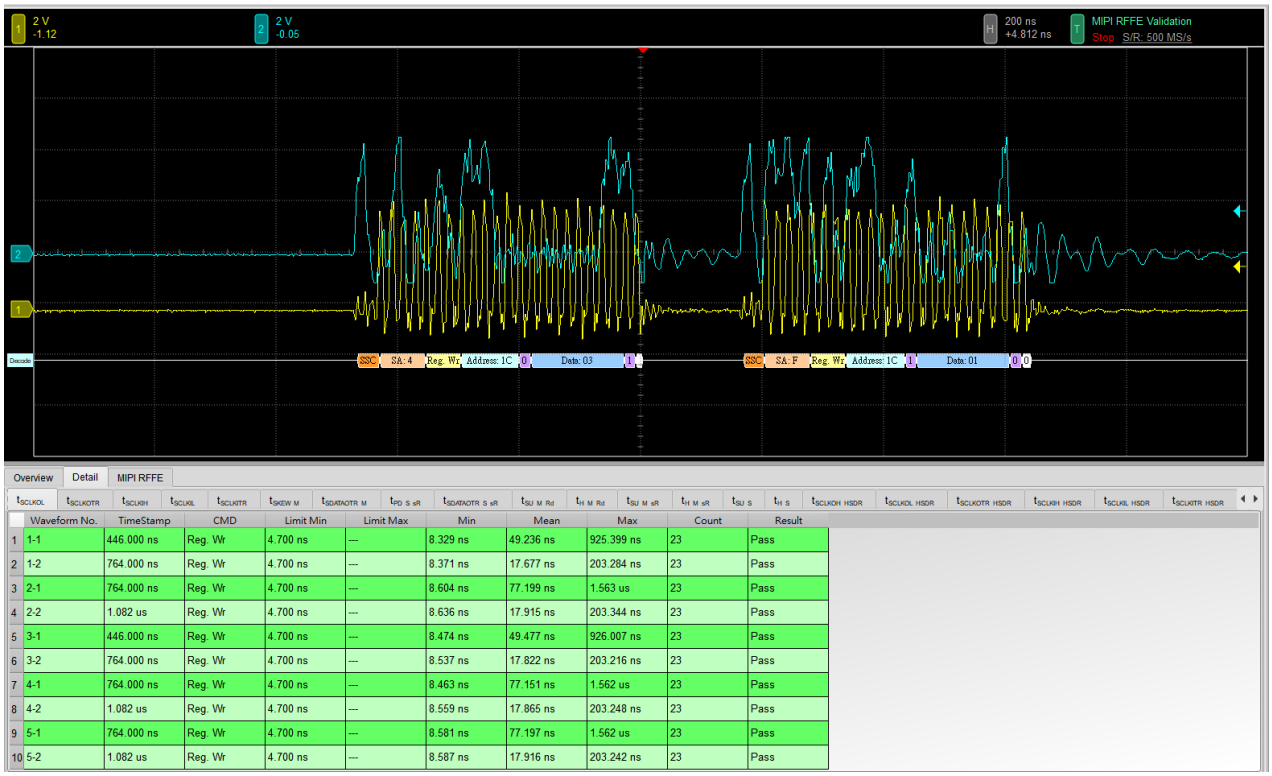
儲存為 .MOW（Acute軟體專用格式）

6. 概覽報告



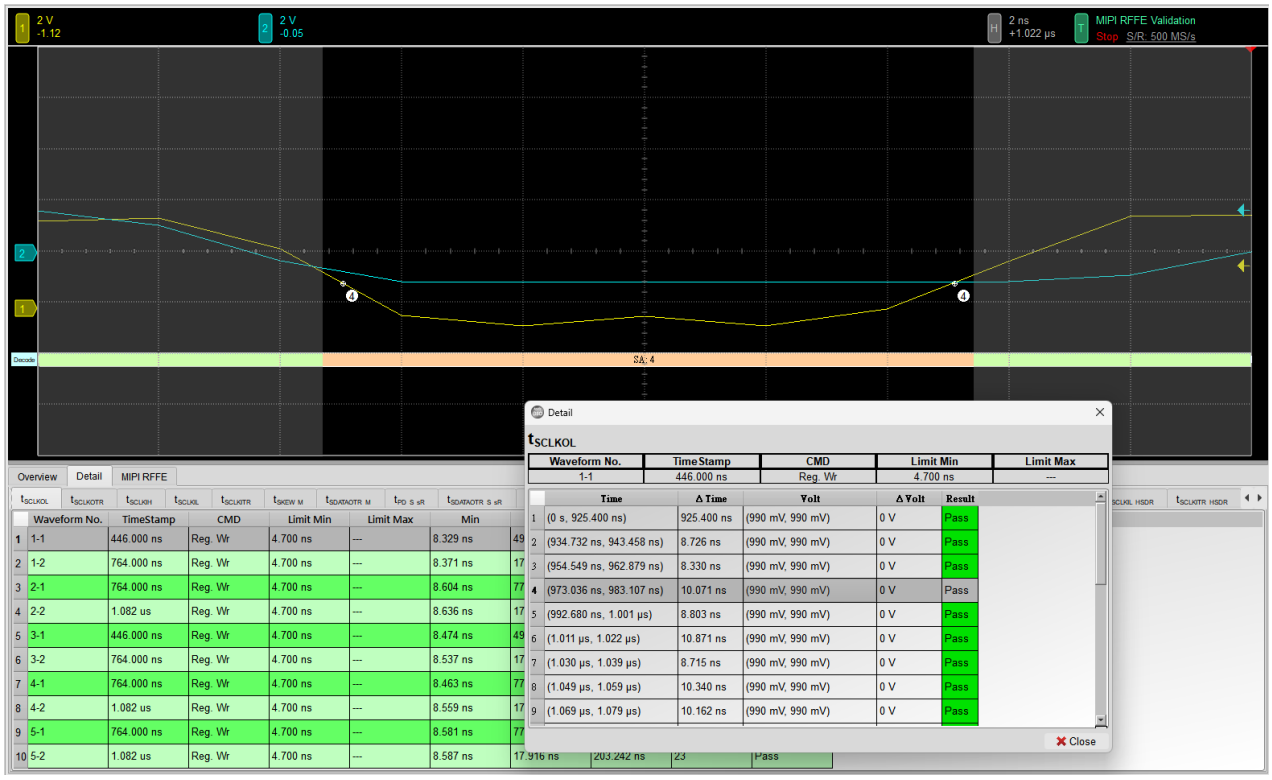
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviati	Count	Result
1	f_{SCLK}	SCLK Fre...	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	Fail
2	t_{SCLKOH}	Clock Out...	4.700 ns	---	6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	Pass
3	t_{SCLKOL}	Clock Out...	4.700 ns	---	8.329 ns	41.946 ns	1.563 us	196.252 ns	230	Pass
4	$t_{SCLKOTR}$	Clock Out...	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail
5	t_{SCLKIH}	Clock Inpu...	---	---	---	---	---	---	0	---
6	t_{SCLKIL}	Clock Inpu...	---	---	---	---	---	---	0	---
7	$t_{SCLKITR}$	Clock Inpu...	---	---	---	---	---	---	0	---
8	t_{SKEW_M}	SDATA Sk...	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95	Fail
9	$t_{SDATAOTR\_M}$	SDATA Ou...	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail
10	$t_{SO\_S\_sR}$	Time for s...	---	---	---	---	---	---	0	---
11	$t_{SDATAOTR\_S\_sR}$	sRead SD...	---	---	---	---	---	---	0	---

7. 詳細報告



	Waveform No.	TimeStamp	CMD	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	446.000 ns	Reg. Wr	4.700 ns	---	8.329 ns	49.236 ns	925.399 ns	23	Pass
2	1-2	764.000 ns	Reg. Wr	4.700 ns	---	8.371 ns	17.677 ns	203.284 ns	23	Pass
3	2-1	764.000 ns	Reg. Wr	4.700 ns	---	8.604 ns	77.199 ns	1.563 us	23	Pass
4	2-2	1.082 us	Reg. Wr	4.700 ns	---	8.636 ns	17.915 ns	203.344 ns	23	Pass
5	3-1	446.000 ns	Reg. Wr	4.700 ns	---	8.474 ns	49.477 ns	926.007 ns	23	Pass
6	3-2	764.000 ns	Reg. Wr	4.700 ns	---	8.537 ns	17.822 ns	203.216 ns	23	Pass
7	4-1	764.000 ns	Reg. Wr	4.700 ns	---	8.463 ns	77.151 ns	1.562 us	23	Pass
8	4-2	1.082 us	Reg. Wr	4.700 ns	---	8.559 ns	17.865 ns	203.248 ns	23	Pass
9	5-1	764.000 ns	Reg. Wr	4.700 ns	---	8.581 ns	77.197 ns	1.562 us	23	Pass
10	5-2	1.082 us	Reg. Wr	4.700 ns	---	8.587 ns	17.916 ns	203.242 ns	23	Pass

8. 波形和參考點



9. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 15:32:11
S/W Version	1.8.62
Protocol	MIPI RFFE

Overview Results:

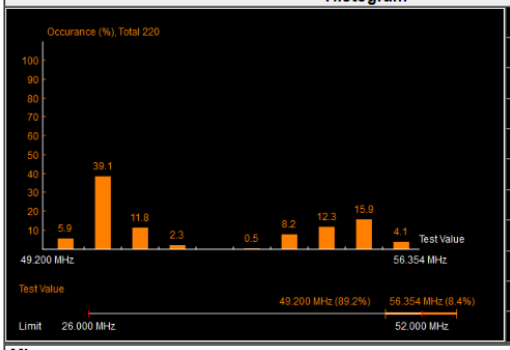
Total: 33
Pass: 2
Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCLK}	SCLK Frequency	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	89.2%	8.4%	✖Fail
2	t_{SCLKOH}	Clock Output High Time	4.700 ns	---	6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	36.4%	---	✔Pass
3	t_{SCLKOL}	Clock Output Low Time	4.700 ns	---	8.329 ns	41.946 ns	1.563 us	196.252 ns	230	77.2%	---	✔Pass
4	$t_{SCLKOTR}$	Clock Output Transition (Rise/Fall) Time	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	✖Fail
5	t_{SCLKIH}	Clock Input High Time	---	---	---	---	---	---	0	---	---	---
6	t_{SCLKIL}	Clock Input Low Time	---	---	---	---	---	---	0	---	---	---
7	$t_{SCLKITR}$	Clock Input Transition (Rise/Fall) Time	---	---	---	---	---	---	0	---	---	---
8	t_{SKEW_M}	SDATA Skew Relative to SCLK, BOM Master Output	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95	---	4368.2%	✖Fail
9	$t_{SDATAOTR\_M}$	SDATA Output Transition (Rise/Fall) Time, BOM Master	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	✖Fail
10	$t_{PD\_S\_sR}$	Time for sRead Data Output Valid from SCLK Rising Edge - Slave	---	---	---	---	---	---	0	---	---	---
11	$t_{SDATAOTR\_S\_sR}$	sRead SDATA Output Transition (Rise/Fall) Time - Slave	---	---	---	---	---	---	0	---	---	---
12	$t_{SU\_M\_Rd}$	SDATA Setup Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---
13	$t_{H\_M\_Rd}$	SDATA Hold Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---
14	$t_{SU\_M\_sR}$	SDATA Setup Time, with respect to SCLK Output - BOM - sRead	---	---	---	---	---	---	0	---	---	---
15	$t_{H\_M\_sR}$	SDATA Hold Time, with respect to SCLK Output - BOM - sRead	---	---	---	---	---	---	0	---	---	---
16	t_{SU_S}	SDATA Setup Time, with respect to SCLK Input - Slave (or non-BOM)	---	---	---	---	---	---	0	---	---	---
17	t_{H_S}	SDATA Hold Time, with respect to SCLK Input - Slave (or non-BOM)	---	---	---	---	---	---	0	---	---	---
18	t_{SCLKOH_HSDR}	(HSDR) Clock Output High Time	---	---	---	---	---	---	0	---	---	---
19	t_{SCLKOL_HSDR}	(HSDR) Clock Output Low Time	---	---	---	---	---	---	0	---	---	---
20	$t_{SCLKOTR\_HSDR}$	(HSDR) Clock Output Transition (Rise/Fall) Time	---	---	---	---	---	---	0	---	---	---
21	t_{SCLKIH_HSDR}	(HSDR) Clock Input High Time	---	---	---	---	---	---	0	---	---	---
22	t_{SCLKIL_HSDR}	(HSDR) Clock Input Low Time	---	---	---	---	---	---	0	---	---	---
23	$t_{SCLKITR\_HSDR}$	(HSDR) Clock Input Transition (Rise/Fall) Time	---	---	---	---	---	---	0	---	---	---
24	$t_{PD\_S\_Rd\_HSDR}$	(HSDR) Time for Read Data Output Valid from SCLK Rising Edge - Slave	---	---	---	---	---	---	0	---	---	---
25	$t_{SDATAOTR\_S\_Rd\_HSDR}$	(HSDR) Read SDATA Output Transition (Rise/Fall) Time - Slave	---	---	---	---	---	---	0	---	---	---
26	$t_{PD\_S\_sR\_HSDR}$	(HSDR) Time for sRead Data Output Valid from SCLK Rising Edge - Slave	---	---	---	---	---	---	0	---	---	---
27	$t_{SDATAOTR\_S\_sR\_HSDR}$	(HSDR) sRead SDATA Output Transition (Rise/Fall) Time - Slave	---	---	---	---	---	---	0	---	---	---
28	$t_{SU\_M\_Rd\_HSDR}$	(HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---
29	$t_{H\_M\_Rd\_HSDR}$	(HSDR) SDATA Hold Time, with respect to SCLK Output - BOM - Read	---	---	---	---	---	---	0	---	---	---

f_{SCLK} - Test Result: Fail
Description: SCLK Frequency

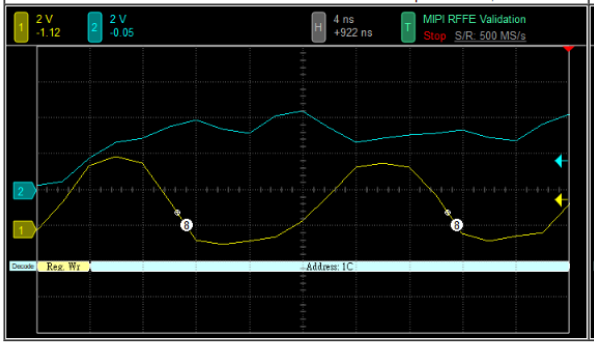
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	89.2%	8.4%

Histogram

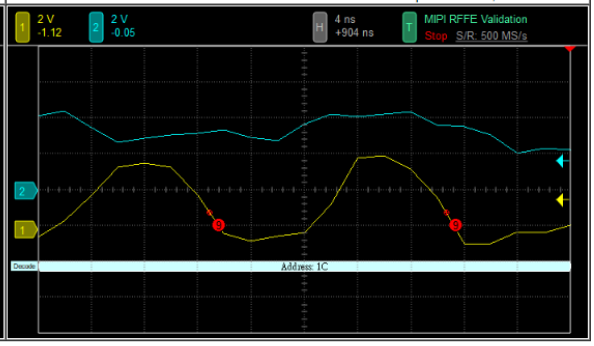


Value Range	Occurance Count
49.2 MHz ~ 49.916 MHz	13
49.916 MHz ~ 50.631 MHz	86
50.631 MHz ~ 51.347 MHz	26
51.347 MHz ~ 52.062 MHz	5
52.062 MHz ~ 52.777 MHz	0
52.777 MHz ~ 53.493 MHz	1
53.493 MHz ~ 54.208 MHz	18
54.208 MHz ~ 54.923 MHz	27
54.923 MHz ~ 55.639 MHz	35
55.639 MHz ~ 56.354 MHz	9

Min Detail Report Row: 1, Test Index: 8

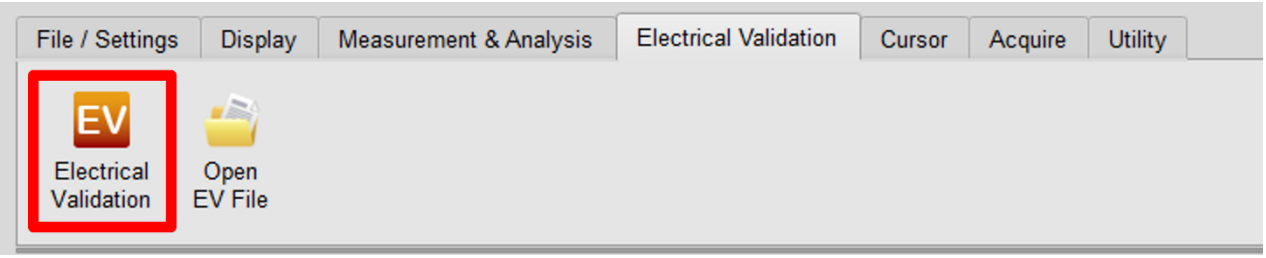


Max Detail Report Row: 1, Test Index: 9



MIPI SPMI 電氣特性驗證解決方案

■ 簡介：

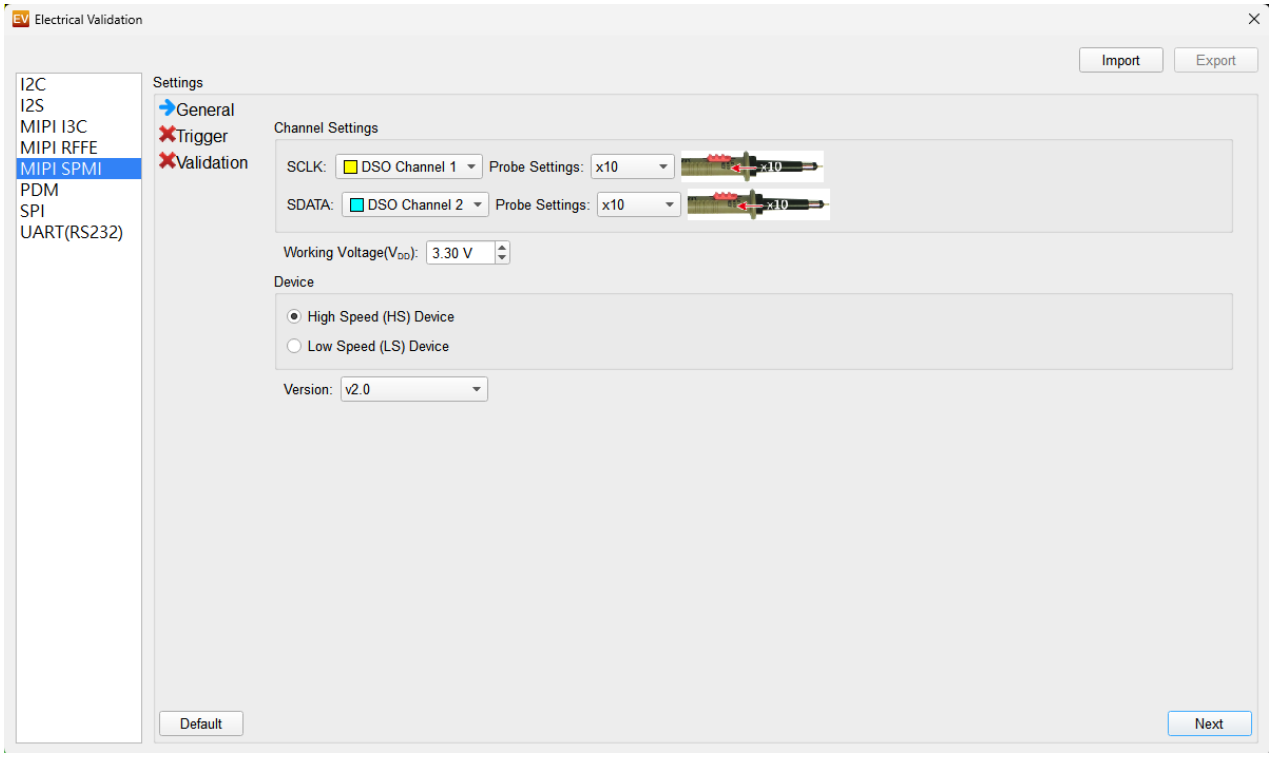


使用示波器執行 MIPI SPMI 電氣特性驗證，以確保 MIPI SPMI 協定符合既定規格。在經過長時間燒機測試後，可確認所測試的訊號電氣特性是否符合標準。

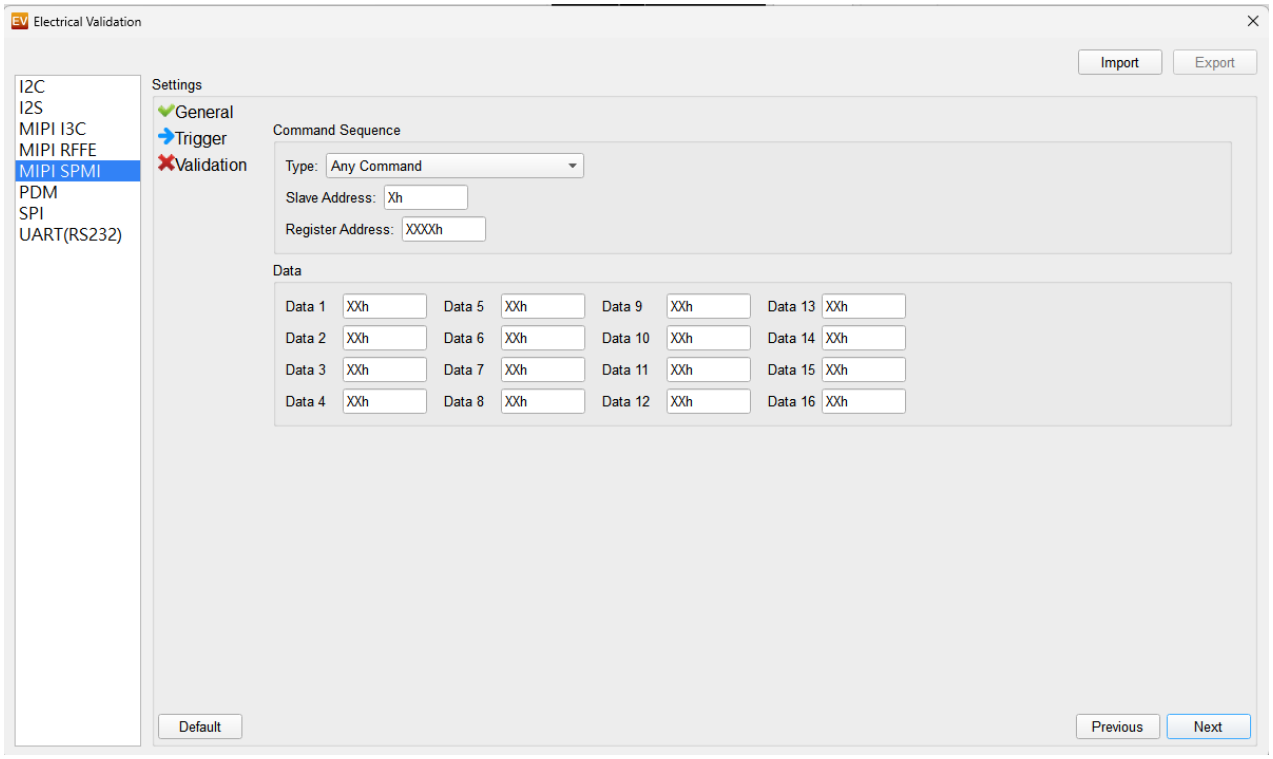
MIPI SPMI（System Power Management Interface）是由 MIPI 聯盟（Mobile Industry Processor Interface）制定的標準規範，主要目的是為了在行動與嵌入式系統中實現電源管理。SPMI 提供標準化的通訊介面，用於在電源管理 IC（PMIC）與各個系統元件之間有效地分配電力與管理電源狀態，常見於智慧型手機、平板電腦等裝置中。

MIPI SPMI 電氣特性驗證設定

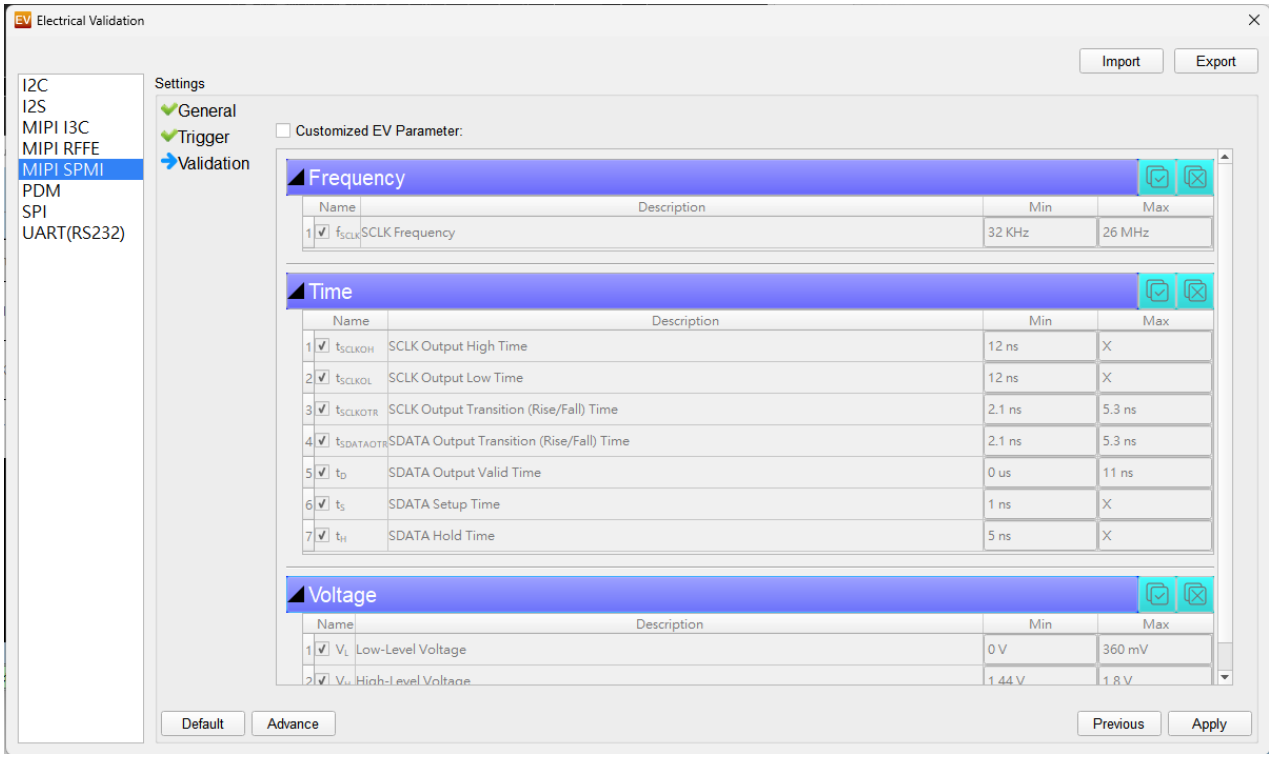
1. 一般設定：設定通道來源、工作電壓、傳輸速率與協定版本。



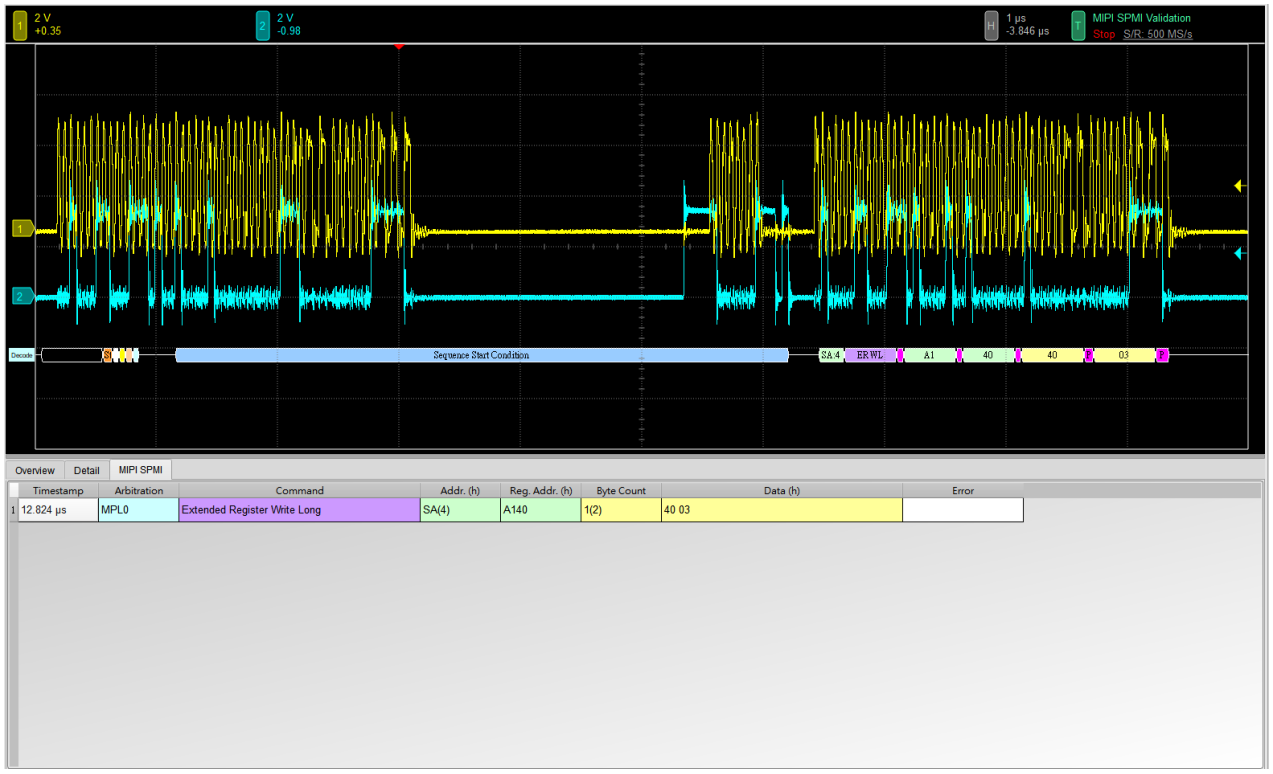
2. 觸發設定



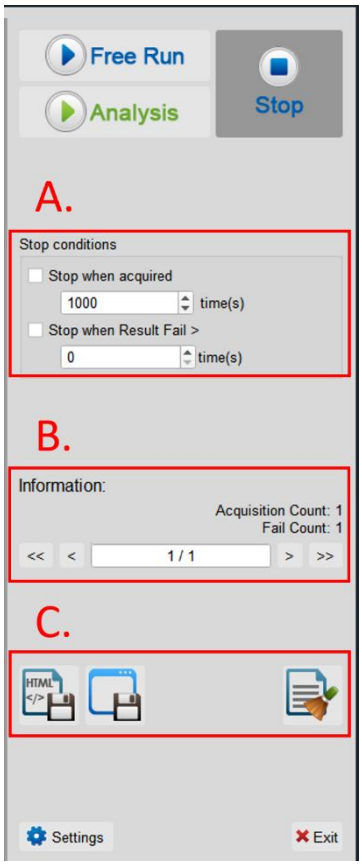
3. 驗證參數設定：包含頻率、時間與電壓限制



4. 電氣特性驗證 軟體畫面



5. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

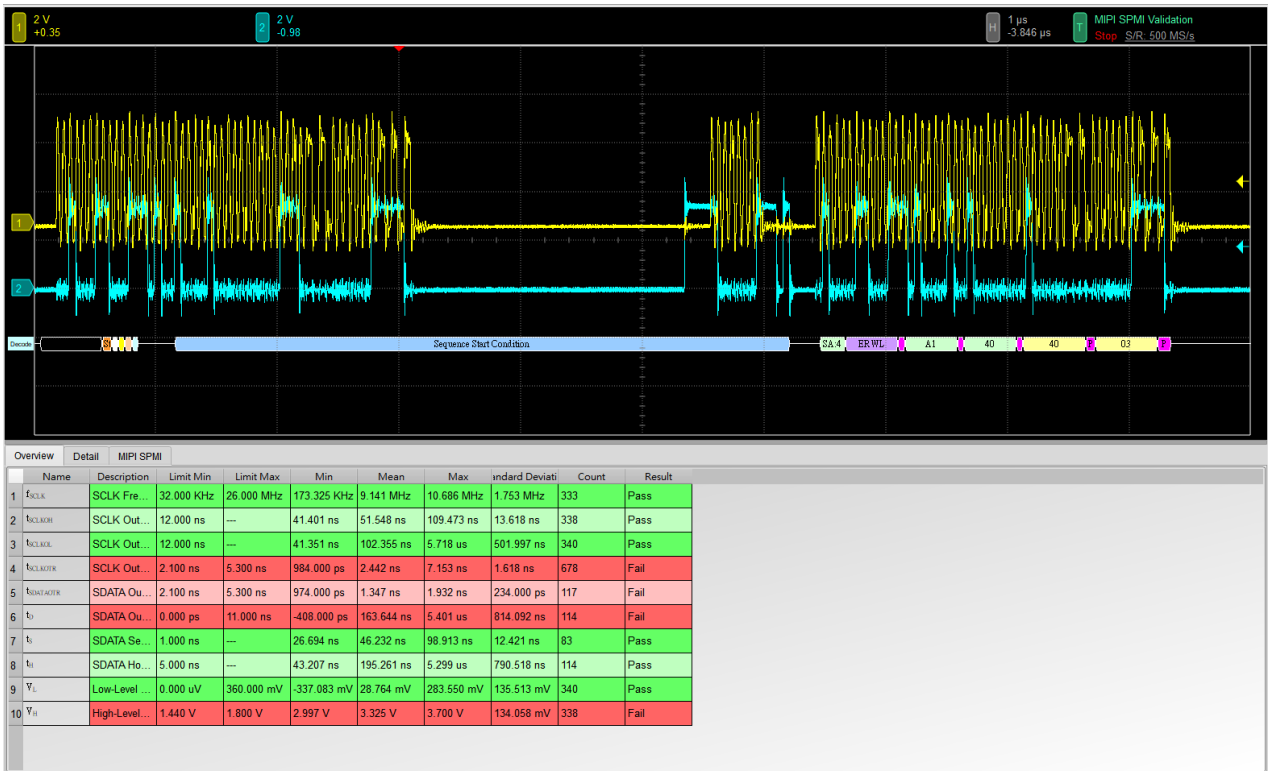
選擇查看波形

C. 儲存檔案：

儲存為 HTML 格式

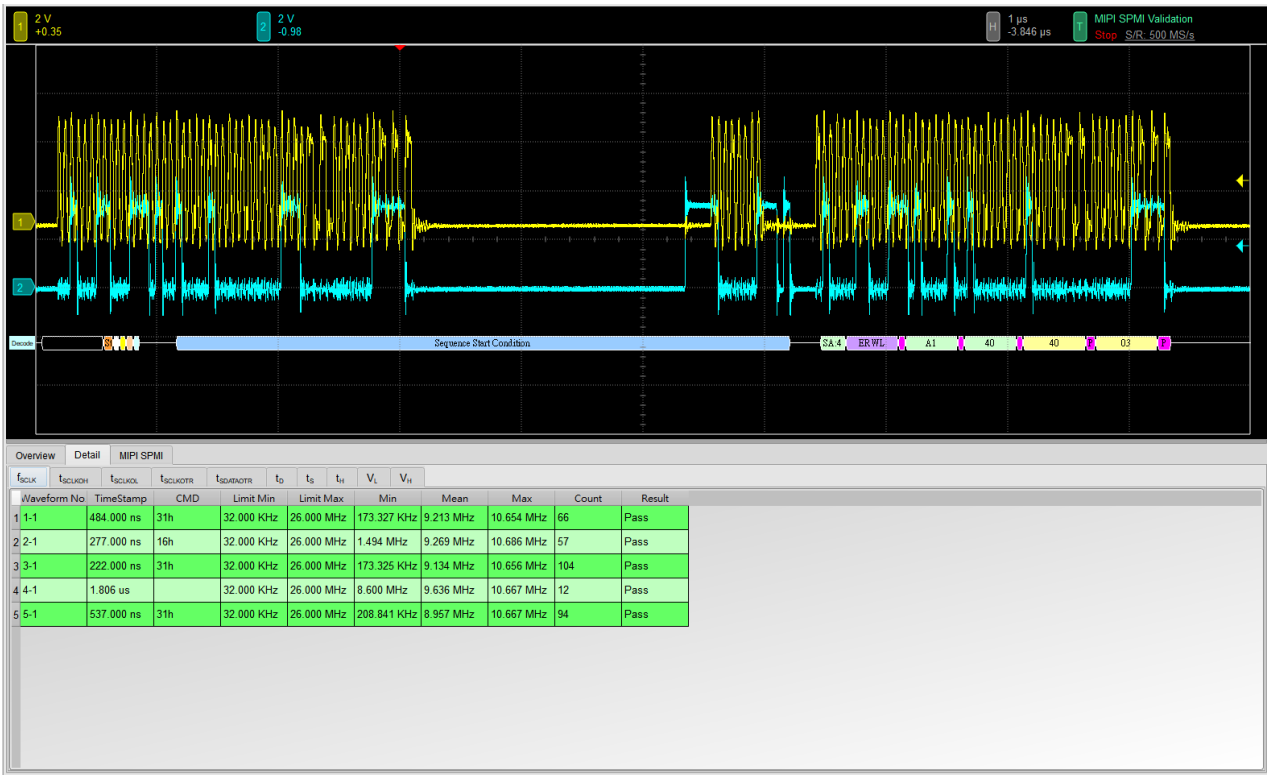
儲存為 .MOW（Acute軟體專用格式）

6. 概覽報告



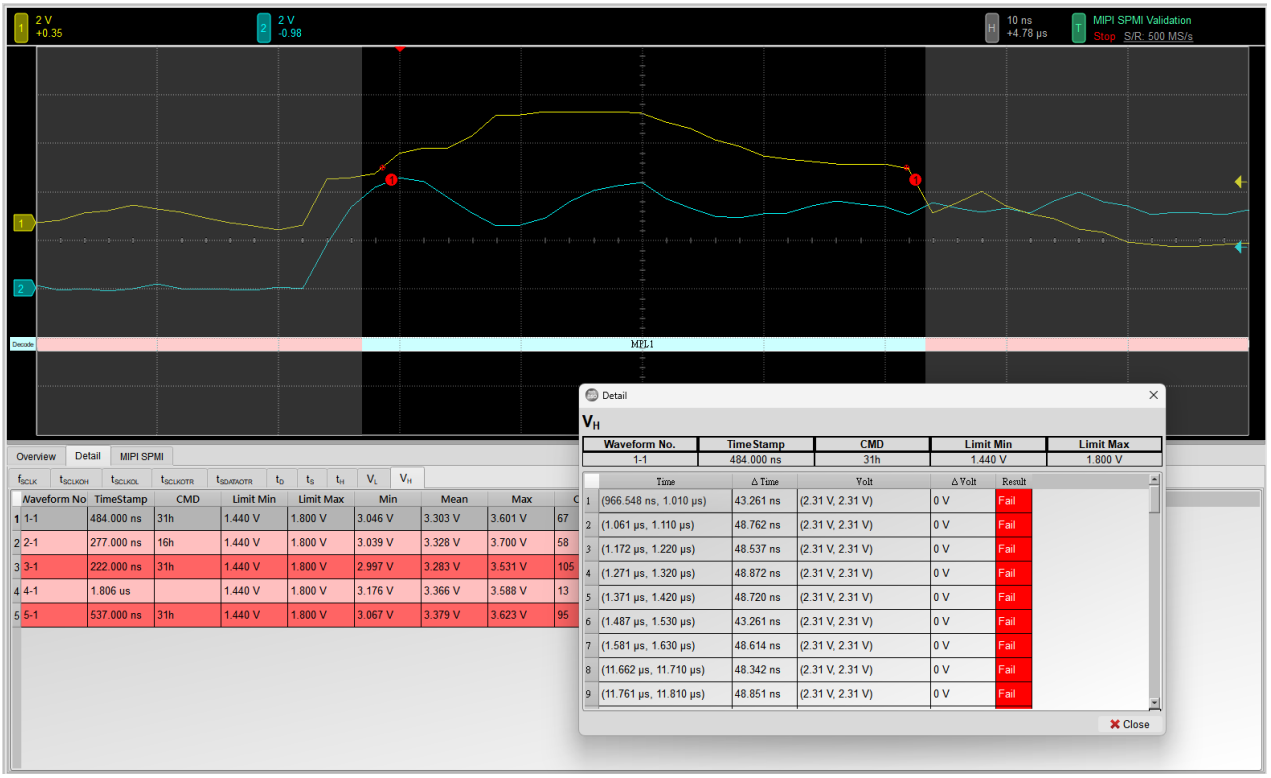
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviati	Count	Result
1	t_{SCLK}	SCLK Fre...	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	Pass
2	t_{SCLKOH}	SCLK Out...	12.000 ns	---	41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	Pass
3	t_{SCLKOL}	SCLK Out...	12.000 ns	---	41.351 ns	102.355 ns	5.718 us	501.997 ns	340	Pass
4	$t_{SCLKOTR}$	SCLK Out...	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	Fail
5	$t_{SDATAOTR}$	SDATA Ou...	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	Fail
6	t_D	SDATA Ou...	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	Fail
7	t_S	SDATA Se...	1.000 ns	---	26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	Pass
8	t_H	SDATA Ho...	5.000 ns	---	43.207 ns	195.261 ns	5.299 us	790.518 ns	114	Pass
9	V_L	Low-Level ...	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340	Pass
10	V_H	High-Level...	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	Fail

7. 詳細報告



Waveform No	TimeStamp	CMD	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1 1-1	484.000 ns	31h	32.000 KHz	26.000 MHz	173.327 KHz	9.213 MHz	10.654 MHz	66	Pass
2 2-1	277.000 ns	16h	32.000 KHz	26.000 MHz	1.494 MHz	9.269 MHz	10.686 MHz	57	Pass
3 3-1	222.000 ns	31h	32.000 KHz	26.000 MHz	173.325 KHz	9.134 MHz	10.656 MHz	104	Pass
4 4-1	1.806 us		32.000 KHz	26.000 MHz	8.600 MHz	9.636 MHz	10.667 MHz	12	Pass
5 5-1	537.000 ns	31h	32.000 KHz	26.000 MHz	208.841 KHz	8.957 MHz	10.667 MHz	94	Pass

8. 波形和參考點



Waveform No.	TimeStamp	CMD	Limit Min	Limit Max
1-1	484.000 ns	31h	1.440 V	1.800 V

Waveform No	TimeStamp	CMD	Limit Min	Limit Max	Min	Mean	Max	C
1 1-1	484.000 ns	31h	1.440 V	1.800 V	3.046 V	3.303 V	3.601 V	67
2 2-1	277.000 ns	16h	1.440 V	1.800 V	3.039 V	3.328 V	3.700 V	58
3 3-1	222.000 ns	31h	1.440 V	1.800 V	2.997 V	3.283 V	3.531 V	105
4 4-1	1.806 us		1.440 V	1.800 V	3.176 V	3.366 V	3.588 V	13
5 5-1	537.000 ns	31h	1.440 V	1.800 V	3.067 V	3.379 V	3.623 V	95

	Time	Δ Time	Volt	Δ Volt	Result
1	(966.548 ns, 1.010 µs)	43.261 ns	(2.31 V, 2.31 V)	0 V	Fail
2	(1.061 µs, 1.110 µs)	48.762 ns	(2.31 V, 2.31 V)	0 V	Fail
3	(1.172 µs, 1.220 µs)	48.537 ns	(2.31 V, 2.31 V)	0 V	Fail
4	(1.271 µs, 1.320 µs)	48.872 ns	(2.31 V, 2.31 V)	0 V	Fail
5	(1.371 µs, 1.420 µs)	48.720 ns	(2.31 V, 2.31 V)	0 V	Fail
6	(1.487 µs, 1.530 µs)	43.261 ns	(2.31 V, 2.31 V)	0 V	Fail
7	(1.581 µs, 1.630 µs)	48.614 ns	(2.31 V, 2.31 V)	0 V	Fail
8	(11.662 µs, 11.710 µs)	48.342 ns	(2.31 V, 2.31 V)	0 V	Fail
9	(11.761 µs, 11.810 µs)	48.851 ns	(2.31 V, 2.31 V)	0 V	Fail

Close

9. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 14:54:25
S/W Version	1.8.62
Protocol	MIPI SPMI

Overview Results:

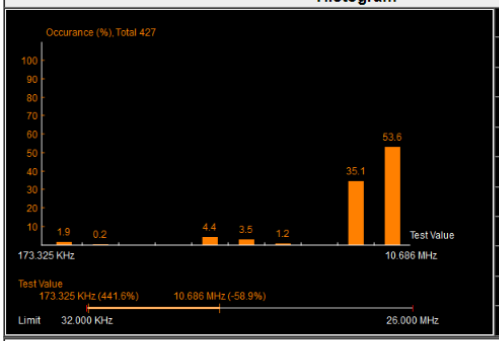
Total: 10
Pass: 6
Fail: 4

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{SCLK}	SCLK Frequency	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	441.6%	-58.9%	Pass
2	t_{SCLKOH}	SCLK Output High Time	12.000 ns	---	41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	245.0%	---	Pass
3	t_{SCLKOL}	SCLK Output Low Time	12.000 ns	---	41.351 ns	102.355 ns	5.718 us	501.997 ns	340	244.6%	---	Pass
4	$t_{SCLKOTR}$	SCLK Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	-53.1%	35.0%	Fail
5	$t_{SDATAOTR}$	SDATA Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	-53.6%	-63.5%	Fail
6	t_D	SDATA Output Valid Time	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	---	48997.2%	Fail
7	t_S	SDATA Setup Time	1.000 ns	---	26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	2569.4%	---	Pass
8	t_H	SDATA Hold Time	5.000 ns	---	43.207 ns	195.261 ns	5.299 us	790.518 ns	114	764.1%	---	Pass
9	V_L	Low-Level Voltage	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340	---	-21.2%	Pass
10	V_H	High-Level Voltage	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	108.1%	105.5%	Fail

f_{SCLK} - Test Result: Pass
Description: SCLK Frequency

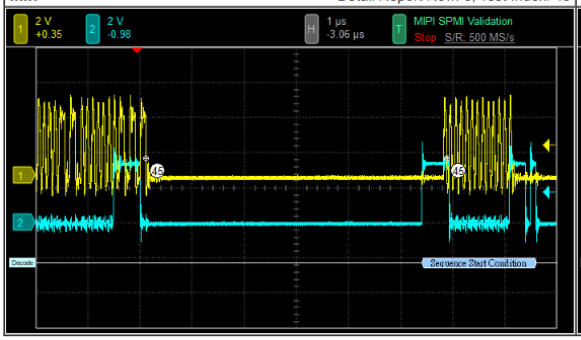
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	441.6%	-58.9%

Histogram

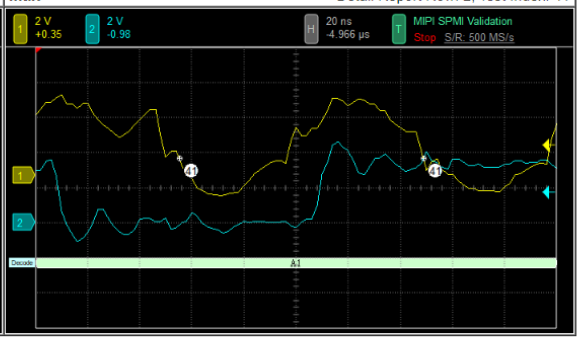


Value Range	Occurance Count
173.325 kHz ~ 1.225 MHz	8
1.225 MHz ~ 2.276 MHz	1
2.276 MHz ~ 3.327 MHz	0
3.327 MHz ~ 4.378 MHz	0
4.378 MHz ~ 5.429 MHz	19
5.429 MHz ~ 6.481 MHz	15
6.481 MHz ~ 7.532 MHz	5
7.532 MHz ~ 8.583 MHz	0
8.583 MHz ~ 9.634 MHz	150
9.634 MHz ~ 10.686 MHz	229

Min Detail Report Row: 3, Test Index: 45

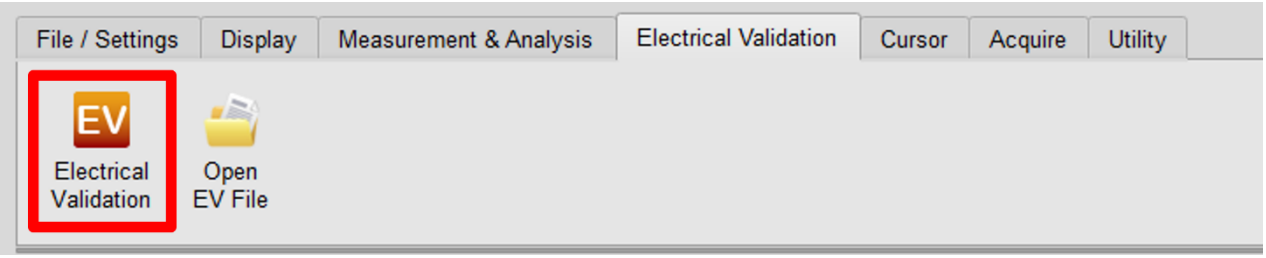


Max Detail Report Row: 2, Test Index: 41



PDM 電氣特性驗證解決方案

■ 簡介：



使用示波器執行 PDM（Pulse Density Modulation）電氣特性驗證，以確保其訊號符合既定電氣標準規格。在經過長時間燒機測試後，可以確認待測訊號的電氣特性是否滿足標準要求。

PDM 協定的電氣特性檢測通常分為兩大類：

- 垂直屬性（電壓）
- 水平屬性（時間／相位）

因此，使用此功能時，必須先設定所選的協定與測試規範，並透過重複測試來取得電氣特性報告。測試項目會根據 PDM 傳輸速率而有所不同。

常用 PDM 規格中的部分電氣特性項目參數：

DIGITAL AUDIO INTERFACE					
PDM_CLK High Frequency Range	f_{CLKH}		5.28	8.64	MHz
PDM_CLK Low Frequency Range	f_{CLKL}		1.84	4.32	MHz
PDM_CLK High Time	t_{PDM_CLKH}		40		ns
PDM_CLK Low Time	t_{PDM_CLKL}		40		ns

常用 PDM 驗證報告內容：

Overview | Detail | PDM

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f_{CLK}	Clock freq...	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass
2	t_{LOW}	Low Perio...	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass
3	t_{HIGH}	High Perio...	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass
4	t_{rCL}	Rise time ...	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass
5	t_{fCL}	Fall time o...	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass
6	t_{DD}	Delay time...	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass
7	t_{DV}	Delay time...	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass
8	t_{DD}	Delay time...	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass
9	t_{DV}	Delay time...	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass

電氣特性驗證 軟體畫面：

1. 頻率：時鐘頻率（Clock Speed）
2. 時序參數：Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
3. 電壓參數：V_IL（輸入低電位）、V_IH（輸入高電位）等

Frequency:

Symbol	Electrical Parameter
f_{SCL}	PDM_CLK Frequency Range

Time:

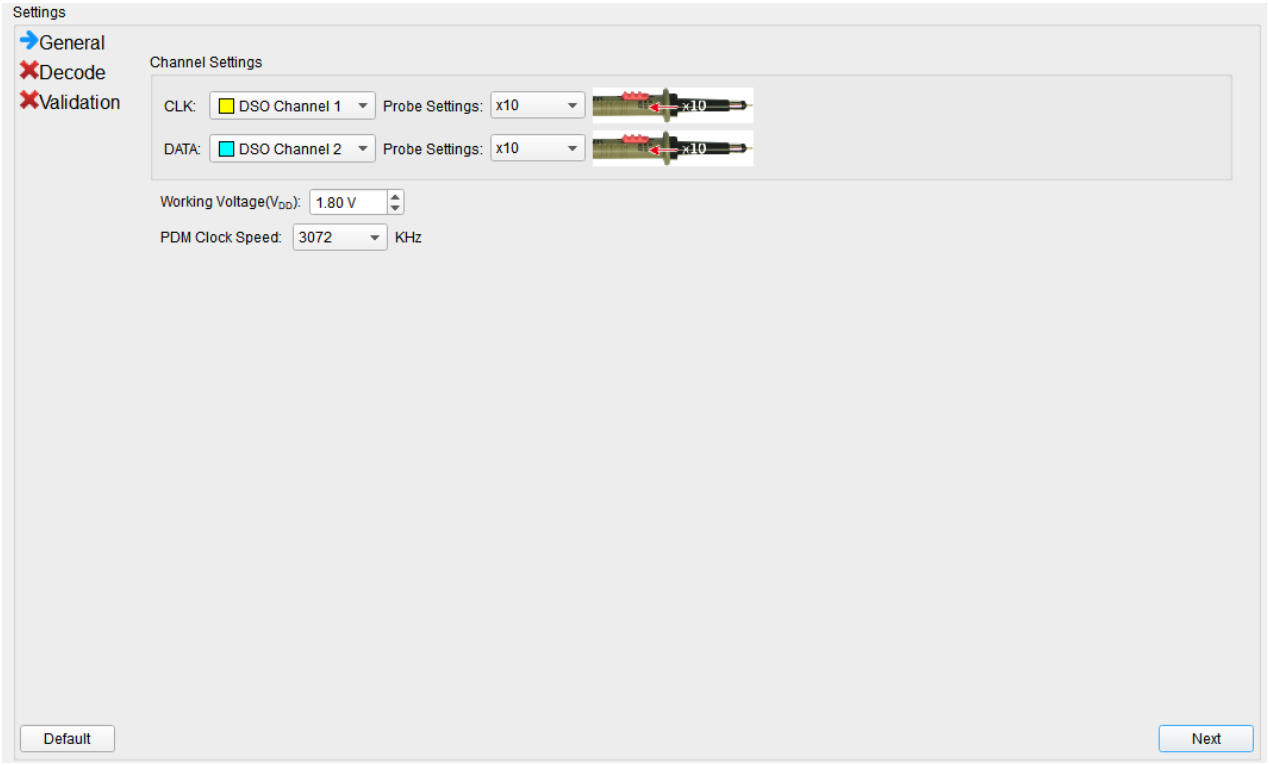
Symbol	Electrical Parameter
t_{LOW}	Low Period of the Clock
t_{HIGH}	High Period of the Clock
t_{rCL}	Rise time of Clock signal
t_{fCL}	Fall time of Clock signal
t_{rDD}	Delay time from Clock edge to Data Rise driven
t_{fDD}	Delay time from Clock edge to Data Fall driven
t_{rDV}	Delay time from Clock edge to Data Rise valid
t_{fDV}	Delay time from Clock edge to Data Fall valid

Voltage:

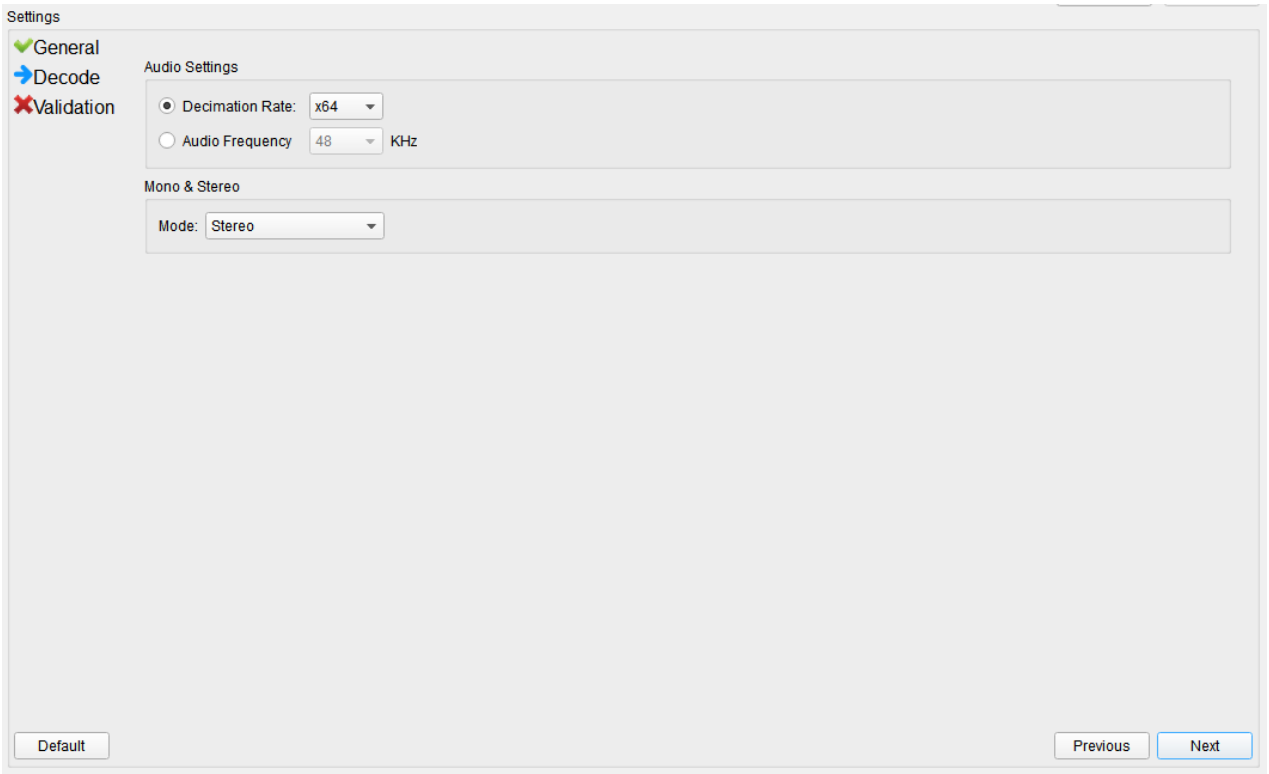
Symbol	Electrical Parameter
V_{ClkLow}	Low-level Input voltage for clock
$V_{ClkHigh}$	High-level Input voltage for clock
$V_{DataLow}$	Low-level Input voltage for data
$V_{DataHigh}$	High-level Input voltage for data

PDM 電氣特性驗證設定

1. 一般設定：設定通道來源、工作電壓與傳輸速率。



2. 解碼設定：設定 PDM 解碼參數



3. 驗證參數設定：頻率、時序與電壓限制

Settings

General
Decode
Validation

Customized EV Parameter:

Frequency

	Name	Description	Min	Max
1	f_{CLK}	Clock frequency	0 kHz	3.072 MHz

Time

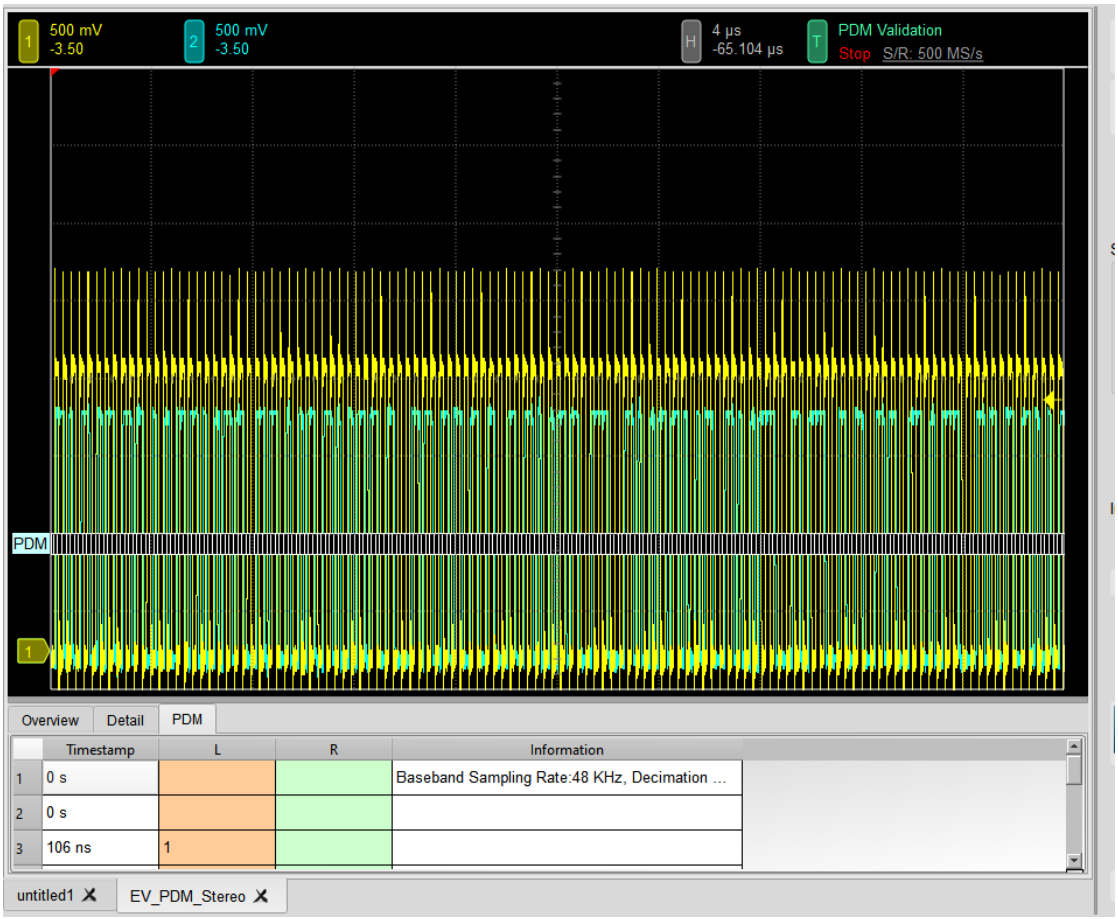
	Name	Description	Min	Max
1	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns
2	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns
3	t_{rCL}	Rise time of CLK signal	X	13 ns
4	t_{fCL}	Fall time of CLK signal	X	13 ns
5	t_{rDD}	Delay time from Clk edge to Data Rise driven	40 ns	80 ns
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40 ns	80 ns
7	t_{rDV}	Delay time from Clk edge to Data Rise Valid	X	100 ns
8	t_{fDV}	Delay time from Clk edge to Data Fall Valid	X	100 ns

Voltage

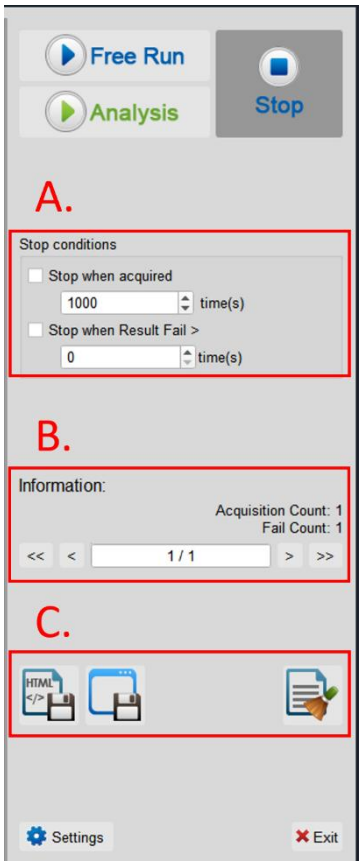
	Name	Description	Min	Max
1	V_{ClkLow}	Low-level input voltage for clock	-0.5 V	0.54 V
2	$V_{ClkHigh}$	High-level input voltage for clock	1.26 V	2.3 V
3	$V_{DataLow}$	Low-level input voltage for Data	-0.5 V	0.54 V
4	$V_{DataHigh}$	High-level input voltage for Data	1.26 V	2.3 V

Default | Advance | Previous | Apply

4. 電氣特性驗證 軟體畫面



5. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

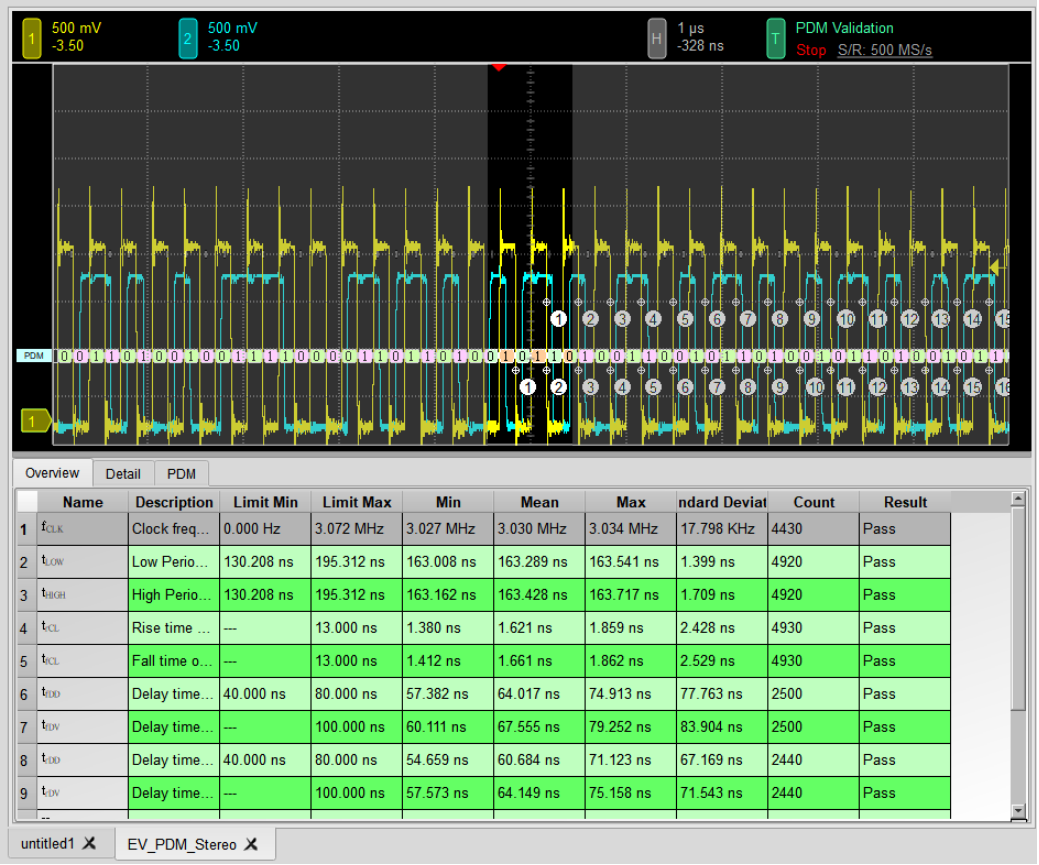
選擇查看波形

C. 儲存檔案：

儲存為 HTML 格式

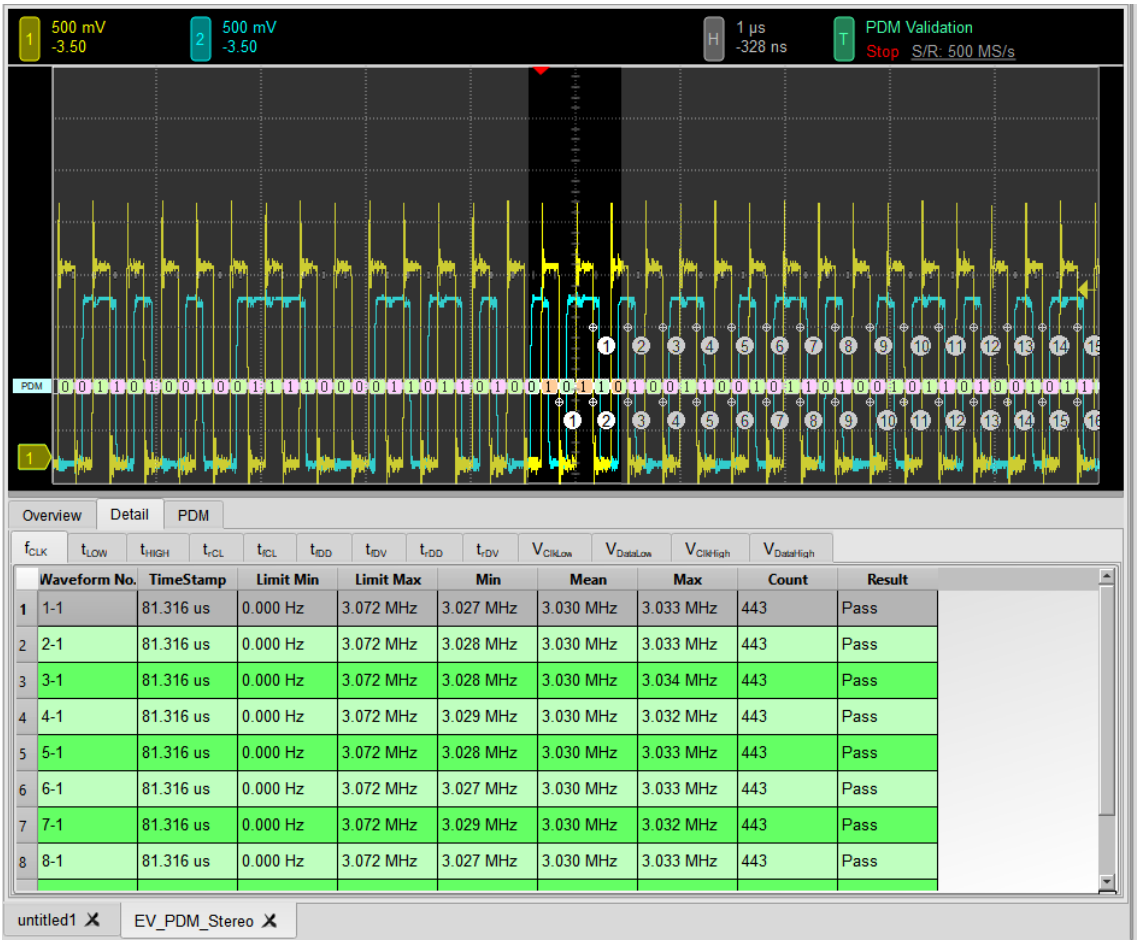
儲存為 .MOW（Acute軟體專用格式）

6. 概覽報告



	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	t_{CLK}	Clock freq...	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass
2	t_{LOW}	Low Perio...	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass
3	t_{HIGH}	High Perio...	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass
4	t_{CL}	Rise time ...	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass
5	t_{CL}	Fall time o...	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass
6	t_{DD}	Delay time...	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass
7	t_{DV}	Delay time...	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass
8	t_{DD}	Delay time...	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass
9	t_{DV}	Delay time...	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass

7. 詳細報告



	Waveform No.	TimeStamp	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass
2	2-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass
3	3-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.034 MHz	443	Pass
4	4-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass
5	5-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass
6	6-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass
7	7-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass
8	8-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass

8. 波形和參考點

Waveform No.	TimeStamp	Limit Min	Limit Max	Min
1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz

	Time	Δ Time	Volt	Δ Volt	Result
1	(16.439 µs, 16.769 µs)	330.000 ns	(540 mV, 1.26 V)	720 mV	Pass
2	(16.769 µs, 17.099 µs)	330.022 ns	(540 mV, 1.26 V)	720 mV	Pass
3	(17.099 µs, 17.429 µs)	329.944 ns	(540 mV, 1.26 V)	720 mV	Pass
4	(17.429 µs, 17.759 µs)	330.069 ns	(540 mV, 1.26 V)	720 mV	Pass
5	(17.759 µs, 18.089 µs)	330.059 ns	(540 mV, 1.26 V)	720 mV	Pass
6	(18.089 µs, 18.419 µs)	329.840 ns	(540 mV, 1.26 V)	720 mV	Pass
7	(18.419 µs, 18.749 µs)	330.122 ns	(540 mV, 1.26 V)	720 mV	Pass
8	(18.749 µs, 19.079 µs)	330.000 ns	(540 mV, 1.26 V)	720 mV	Pass
9	(19.079 µs, 19.409 µs)	329.943 ns	(540 mV, 1.26 V)	720 mV	Pass

9. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

Total: 13
Pass: 13
Fail: 0

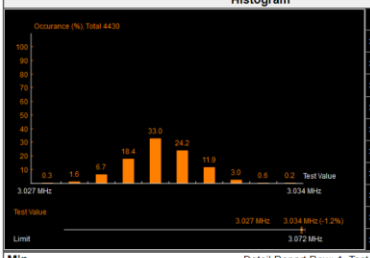
Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{CLK}	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%	✓Pass
2	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	t_{rCL}	Rise time of CLK signal	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	---	-85.7%	✓Pass
5	t_{fCL}	Fall time of CLK signal	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	---	-85.7%	✓Pass
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	t_{fDV}	Delay time from Clk edge to Data Fall Valid	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	---	-20.7%	✓Pass
8	t_{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	✓Pass
9	t_{rDV}	Delay time from Clk edge to Data Rise Valid	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	---	-24.8%	✓Pass
10	V_{ClkLow}	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	$V_{DataLow}$	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	$V_{ClkHigh}$	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	✓Pass
13	$V_{DataHigh}$	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

---

f_{CLK} - Test Result: Pass
Description: Clock frequency

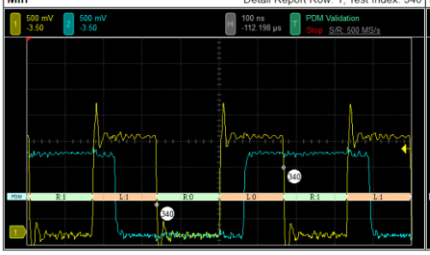
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%

Histogram

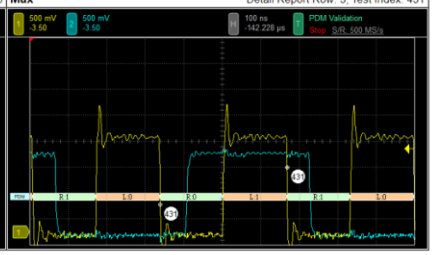


Value Range	Occurance Count
3.027 MHz ~ 3.028 MHz	13
3.028 MHz ~ 3.028 MHz	70
3.028 MHz ~ 3.029 MHz	298
3.029 MHz ~ 3.03 MHz	813
3.03 MHz ~ 3.03 MHz	1464
3.03 MHz ~ 3.031 MHz	1073
3.031 MHz ~ 3.032 MHz	529
3.032 MHz ~ 3.032 MHz	135
3.032 MHz ~ 3.033 MHz	27
3.033 MHz ~ 3.034 MHz	8

Min Detail Report Row: 1, Test Index: 340

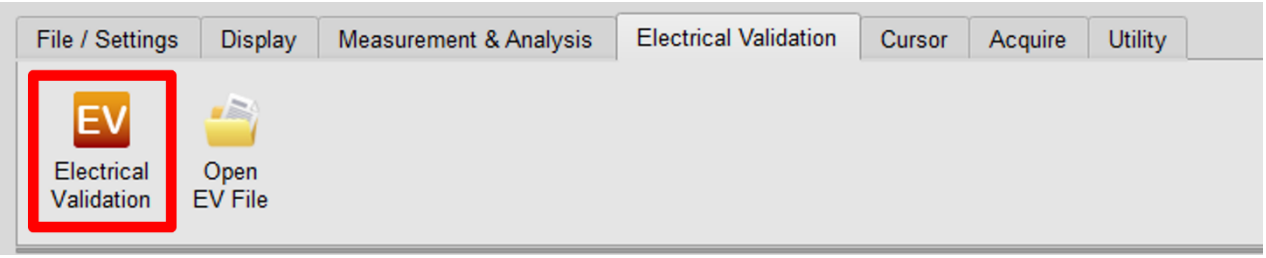


Max Detail Report Row: 3, Test Index: 431



SMBus 電氣特性驗證解決方案

■ 簡介:



使用示波器執行 SMBus（System Management Bus）電氣特性驗證，以確保其訊號符合所定義的電氣特性規格。在經過長時間燒機測試後，可確認待測訊號的電氣特性是否達標。

SMBus 協定的電氣特性檢測方式與 I²C 類似，通常分為兩大類：

- 垂直屬性（電壓）
- 水平屬性（時間／相位）

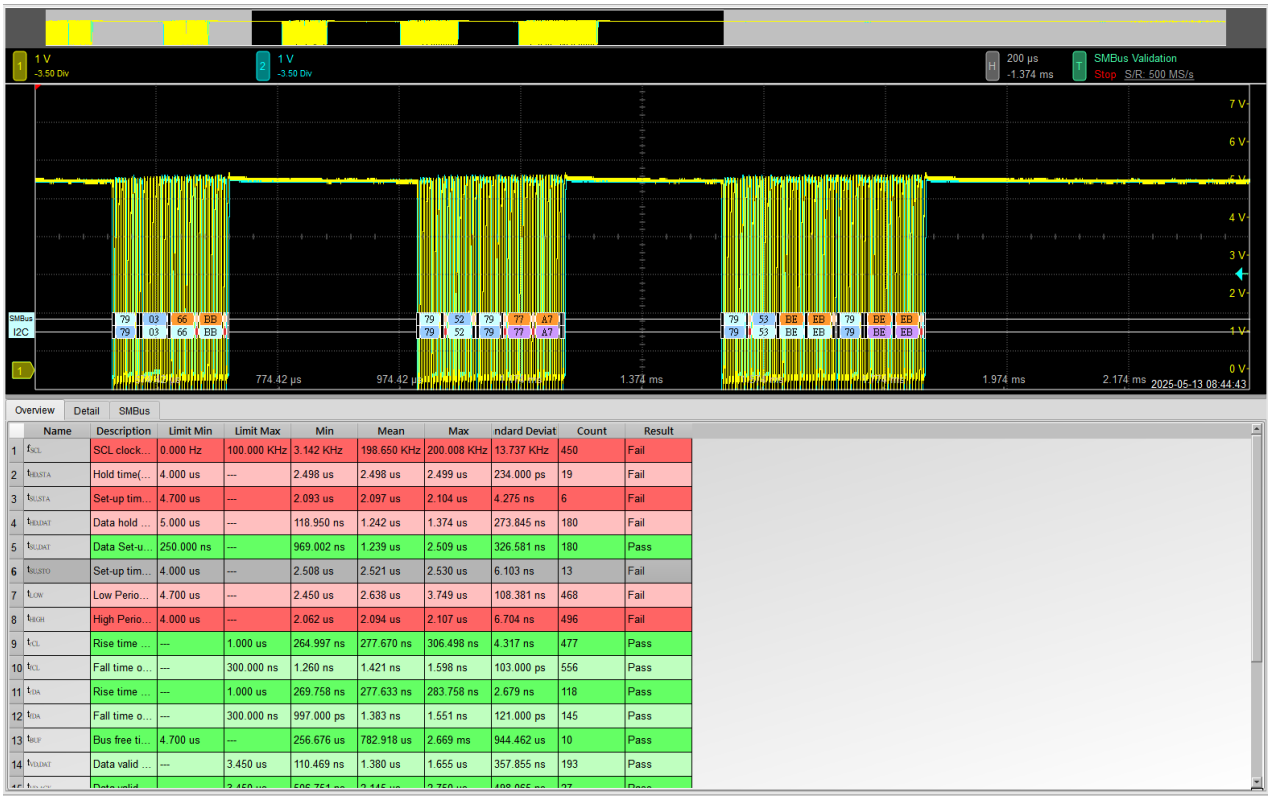
因此，使用此功能前，須先設定所選協定與規格，並透過反覆測試以取得電氣特性測試報告。測試項目會根據 SMBus 的傳輸速率而有所不同。

SMBus 驗證報告內容：

Overview | Detail | SMBus

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f_{SCL}	SCL clock...	0.000 Hz	100.000 KHz	3.142 KHz	198.650 KHz	200.008 KHz	13.737 KHz	450	Fail
2	$t_{HD,STA}$	Hold time(...	4.000 us	---	2.498 us	2.498 us	2.499 us	234.000 ps	19	Fail
3	$t_{SU,STA}$	Set-up tim...	4.700 us	---	2.093 us	2.097 us	2.104 us	4.275 ns	6	Fail
4	$t_{HD,DAT}$	Data hold ...	5.000 us	---	118.950 ns	1.242 us	1.374 us	273.845 ns	180	Fail
5	$t_{SU,DAT}$	Data Set-u...	250.000 ns	---	969.002 ns	1.239 us	2.509 us	326.581 ns	180	Pass
6	$t_{SU,STO}$	Set-up tim...	4.000 us	---	2.508 us	2.521 us	2.530 us	6.103 ns	13	Fail
7	t_{LOW}	Low Perio...	4.700 us	---	2.450 us	2.638 us	3.749 us	108.381 ns	468	Fail
8	t_{HIGH}	High Perio...	4.000 us	---	2.062 us	2.094 us	2.107 us	6.704 ns	496	Fail
9	t_{rCL}	Rise time ...	---	1.000 us	264.997 ns	277.670 ns	306.498 ns	4.317 ns	477	Pass
10	t_{fCL}	Fall time o...	---	300.000 ns	1.260 ns	1.421 ns	1.598 ns	103.000 ps	556	Pass
11	t_{rDA}	Rise time ...	---	1.000 us	269.758 ns	277.633 ns	283.758 ns	2.679 ns	118	Pass
12	t_{fDA}	Fall time o...	---	300.000 ns	997.000 ps	1.383 ns	1.551 ns	121.000 ps	145	Pass
13	t_{BUF}	Bus free ti...	4.700 us	---	256.676 us	782.918 us	2.669 ms	944.462 us	10	Pass
14	$t_{VD,DAT}$	Data valid ...	---	3.450 us	110.469 ns	1.380 us	1.655 us	357.855 ns	193	Pass

電氣特性驗證 軟體畫面：



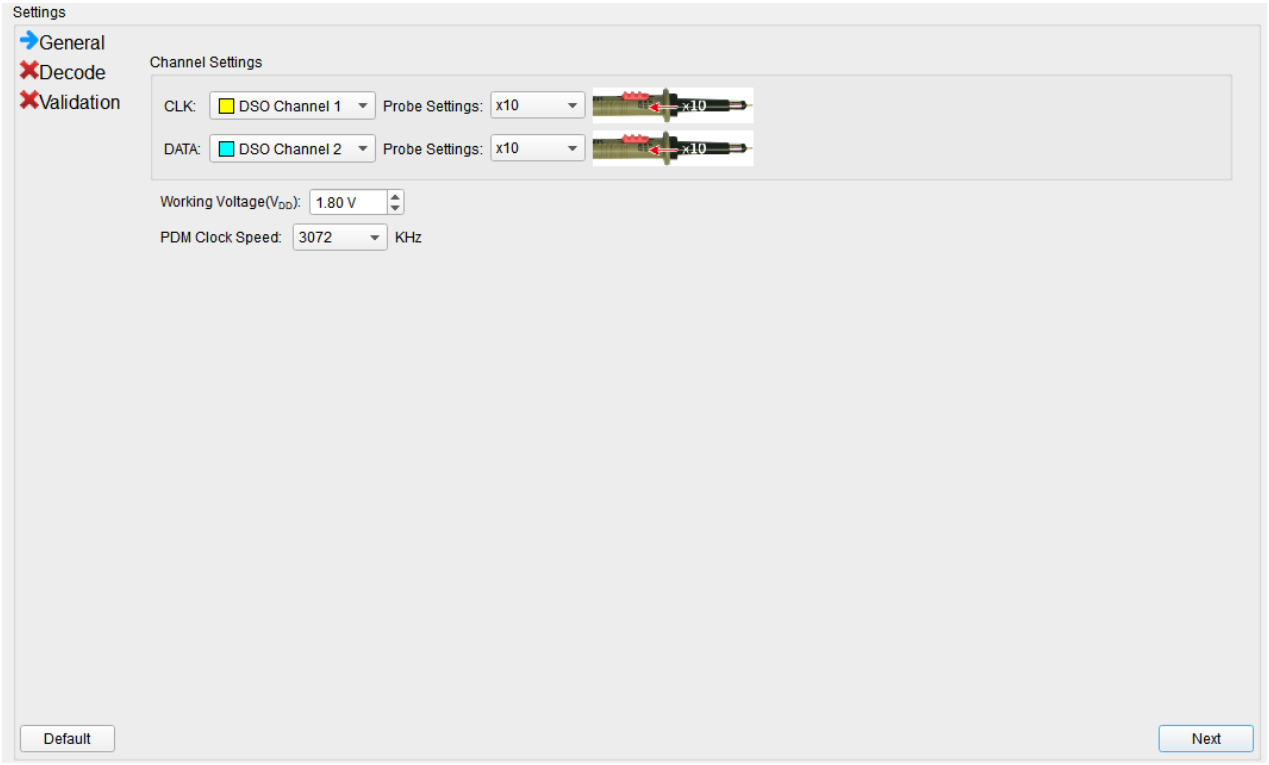
Overview | Detail | SMBus

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f_{SCL}	SCL clock...	0.000 Hz	100.000 KHz	3.142 KHz	198.650 KHz	200.008 KHz	13.737 KHz	450	Fail
2	$t_{HD,STA}$	Hold time(...	4.000 us	---	2.498 us	2.498 us	2.499 us	234.000 ps	19	Fail
3	$t_{SU,STA}$	Set-up tim...	4.700 us	---	2.093 us	2.097 us	2.104 us	4.275 ns	6	Fail
4	$t_{HD,DAT}$	Data hold ...	5.000 us	---	118.950 ns	1.242 us	1.374 us	273.845 ns	180	Fail
5	$t_{SU,DAT}$	Data Set-u...	250.000 ns	---	969.002 ns	1.239 us	2.509 us	326.581 ns	180	Pass
6	$t_{SU,STO}$	Set-up tim...	4.000 us	---	2.508 us	2.521 us	2.530 us	6.103 ns	13	Fail
7	t_{LOW}	Low Perio...	4.700 us	---	2.450 us	2.638 us	3.749 us	108.381 ns	468	Fail
8	t_{HIGH}	High Perio...	4.000 us	---	2.062 us	2.094 us	2.107 us	6.704 ns	496	Fail
9	t_{rCL}	Rise time ...	---	1.000 us	264.997 ns	277.670 ns	306.498 ns	4.317 ns	477	Pass
10	t_{fCL}	Fall time o...	---	300.000 ns	1.260 ns	1.421 ns	1.598 ns	103.000 ps	556	Pass
11	t_{rDA}	Rise time ...	---	1.000 us	269.758 ns	277.633 ns	283.758 ns	2.679 ns	118	Pass
12	t_{fDA}	Fall time o...	---	300.000 ns	997.000 ps	1.383 ns	1.551 ns	121.000 ps	145	Pass
13	t_{BUF}	Bus free ti...	4.700 us	---	256.676 us	782.918 us	2.669 ms	944.462 us	10	Pass
14	$t_{VD,DAT}$	Data valid ...	---	3.450 us	110.469 ns	1.380 us	1.655 us	357.855 ns	193	Pass

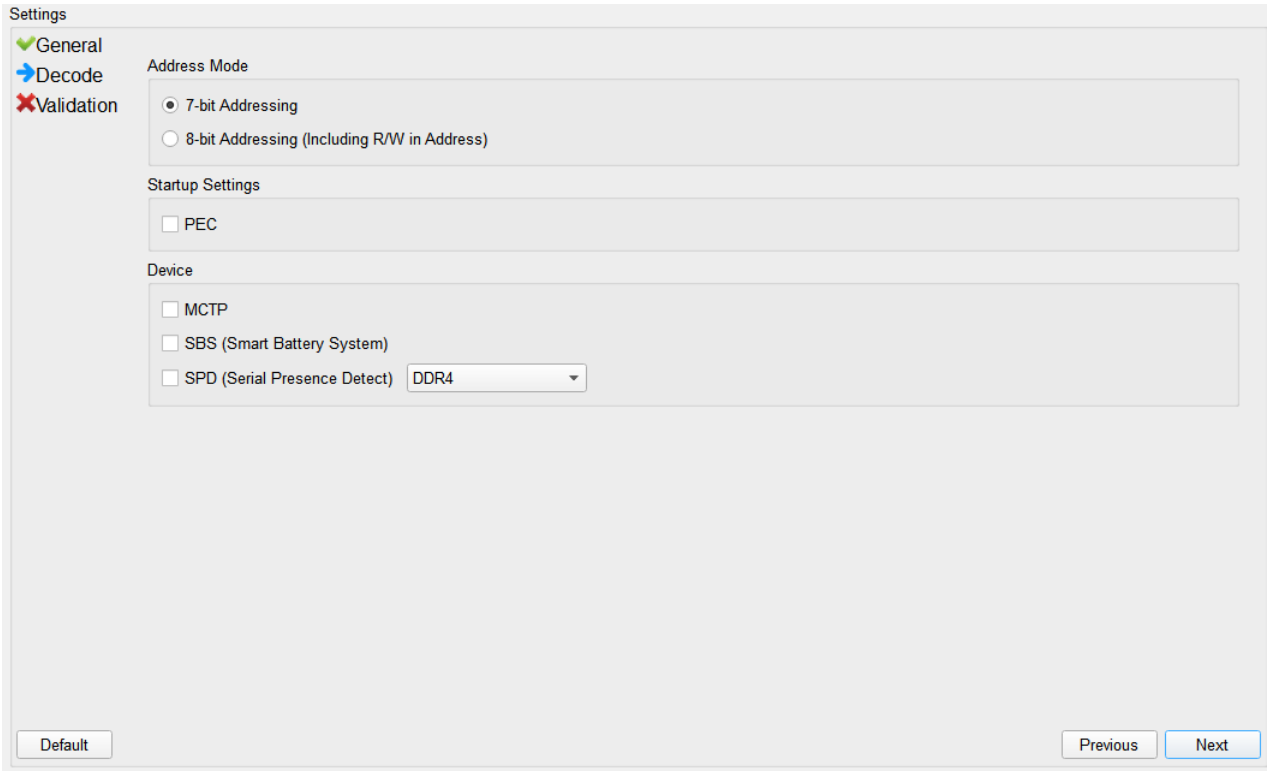
1. 不同的傳輸速率模式，包括 Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
2. 頻率：時脈速度
3. 時序：Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
4. 電壓：V_L, V_H 等

SMBus 電氣特性驗證設定

1. 一般設定：設定通道來源、工作電壓與傳輸速率



2. 解碼設定：設定 SMBus 解碼參數



3. 驗證項目設定：包含頻率、時序與電壓限制

Settings

- General
- Decode
- Validation

Customized EV Parameter:

Frequency

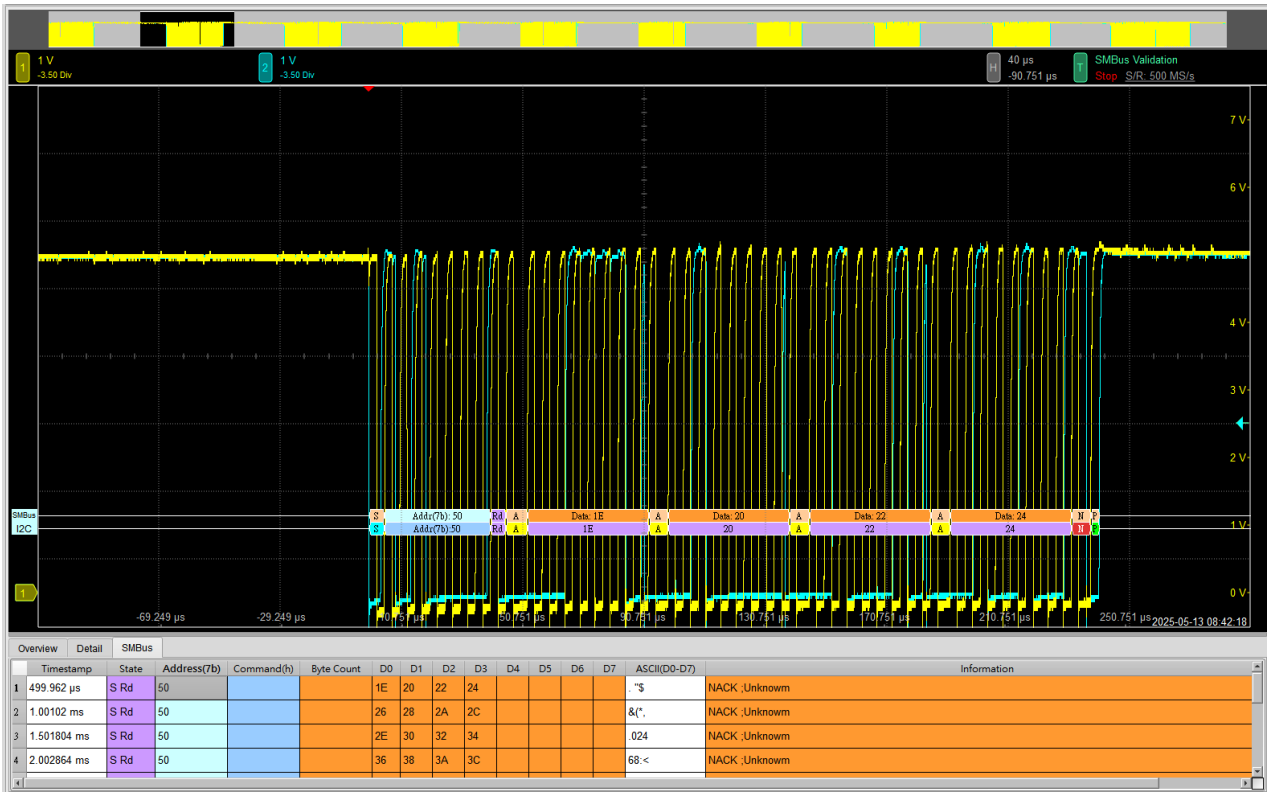
	Name	Description	Min	Max
1	✓ f_{SCL}	SCL clock frequency	0 kHz	100 kHz

Time

	Name	Description	Min	Max
1	✓ $t_{HD,STA}$	Hold time(repeated) START condition	4 us	X
2	✓ $t_{SU,STA}$	Set-up time for a repeated START condition	4.7 us	X
3	✓ $t_{HD,DAT}$	Data hold time	5 us	X
4	✓ $t_{SU,DAT}$	Data Set-up time	250 ns	X
5	✓ $t_{SU,STO}$	Set-up time for STOP condition	4 us	X
6	✓ t_{LOW}	Low Period of the SCL Clock	4.7 us	X
7	✓ t_{HIGH}	High Period of the SCL Clock	4 us	X
8	✓ t_{rCL}	Rise time of SCL signal	X	1 us
9	✓ t_{fCL}	Fall time of SCL signal	X	300 ns
10	✓ t_{rDA}	Rise time of SDA signal	X	1 us
11	✓ t_{fDA}	Fall time of SDA signal	X	300 ns

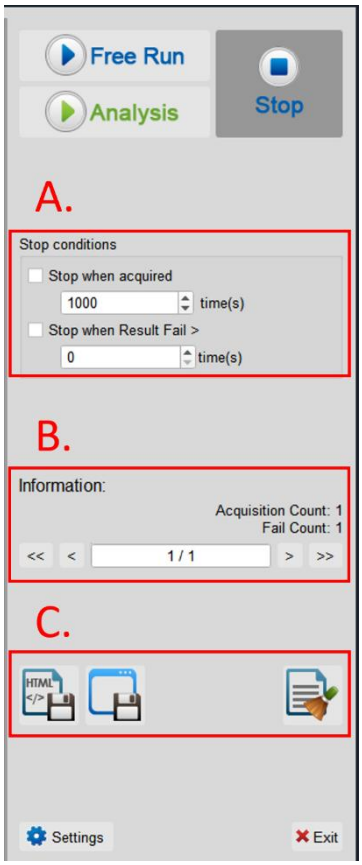
Default | Advance | Previous | Apply

4. 電氣特性驗證 軟體畫面



	Timestamp	State	Address(7b)	Command(h)	Byte Count	D0	D1	D2	D3	D4	D5	D6	D7	ASCII(D0-D7)	Information
1	499.962 µs	S Rd	50			1E	20	22	24					.'$	NACK ;Unknown
2	1.00102 ms	S Rd	50			26	28	2A	2C					&(*,	NACK ;Unknown
3	1.501804 ms	S Rd	50			2E	30	32	34					.024	NACK ;Unknown
4	2.002864 ms	S Rd	50			36	38	3A	3C					68:<	NACK ;Unknown

5. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

選擇查看波形

C. 儲存檔案：

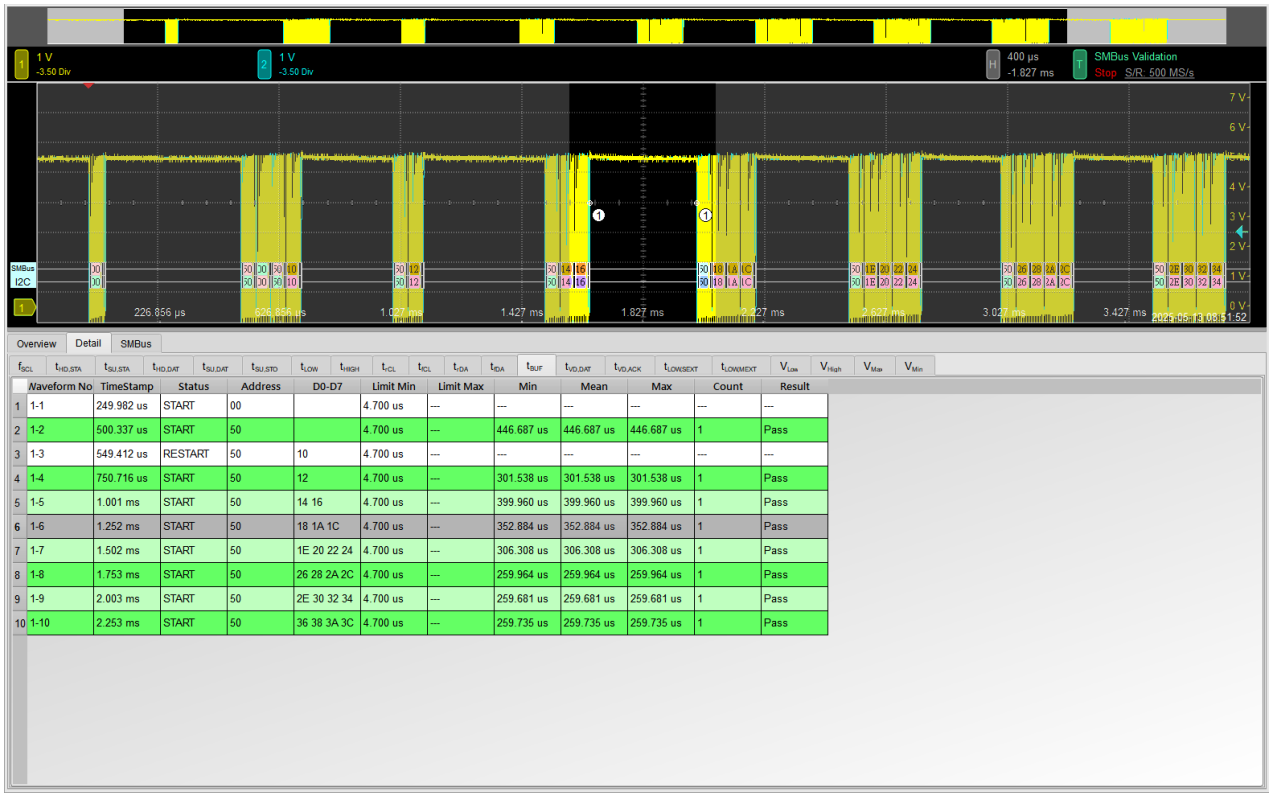
儲存為 HTML 格式

儲存為 .MOW（Acute軟體專用格式）

6. 概覽報告

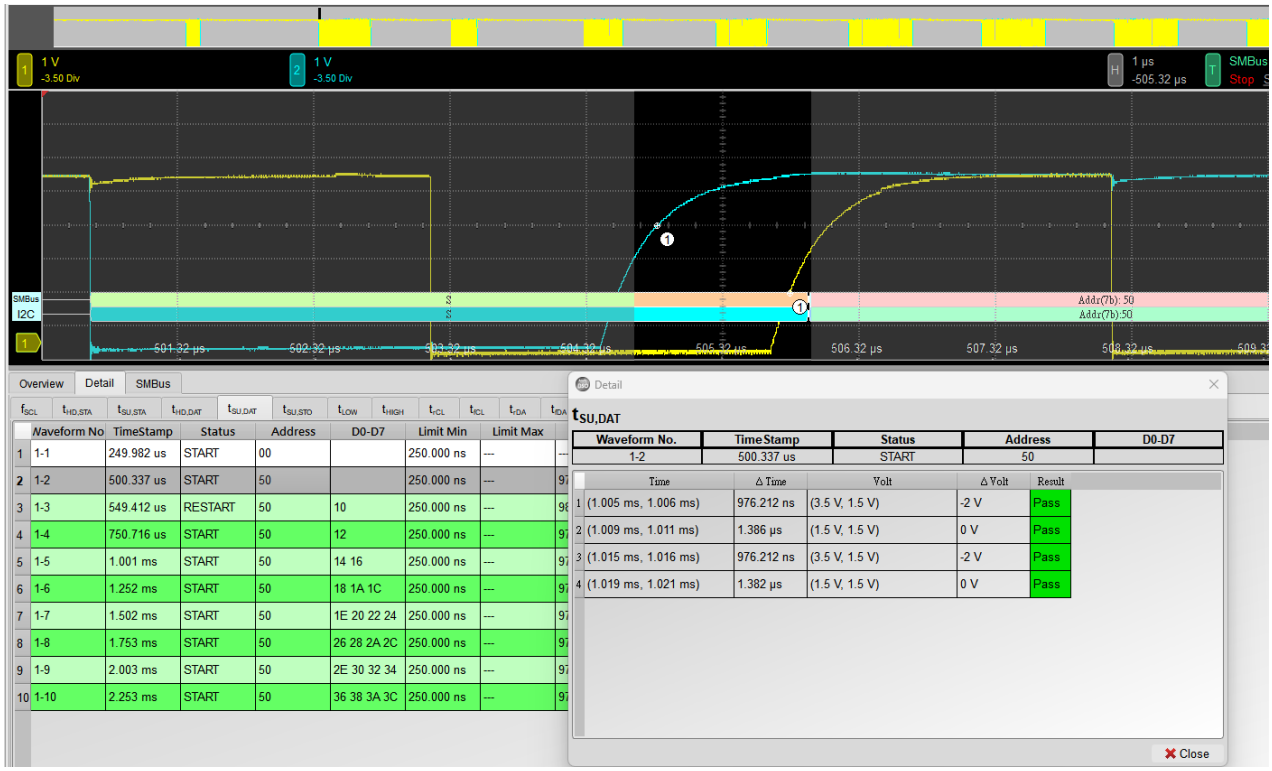
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f_{SCL}	SCL clock...	0.000 Hz	100.000 KHz	199.982 KHz	199.995 KHz	200.007 KHz	4.000 Hz	247	Fail
2	$t_{HD;STA}$	Hold time(...	4.000 us	---	2.498 us	2.498 us	2.499 us	131.000 ps	10	Fail
3	$t_{SU;STA}$	Set-up tim...	4.700 us	---	2.083 us	2.083 us	2.083 us	0.000 ps	1	Fail
4	$t_{HD;DAT}$	Data hold ...	5.000 us	---	119.745 ns	479.688 ns	1.372 us	490.528 ns	136	Fail
5	$t_{SU;DAT}$	Data Set-u...	250.000 ns	---	974.424 ns	1.872 us	2.509 us	546.814 ns	160	Pass
6	$t_{SU;STO}$	Set-up tim...	4.000 us	---	2.508 us	2.519 us	2.523 us	4.359 ns	9	Fail
7	t_{LOW}	Low Perio...	4.700 us	---	2.621 us	2.628 us	2.641 us	3.306 ns	247	Fail
8	t_{HIGH}	High Perio...	4.000 us	---	2.069 us	2.092 us	2.109 us	7.042 ns	272	Fail
9	t_{rCL}	Rise time ...	---	1.000 us	263.576 ns	278.151 ns	297.576 ns	5.070 ns	315	Pass
10	t_{fCL}	Fall time o...	---	300.000 ns	1.233 ns	1.411 ns	1.576 ns	103.000 ps	315	Pass
11	t_{rDA}	Rise time ...	---	1.000 us	270.193 ns	277.390 ns	286.193 ns	3.157 ns	91	Pass
12	t_{fDA}	Fall time o...	---	300.000 ns	969.000 ps	1.311 ns	1.610 ns	172.000 ps	99	Pass
13	t_{BUF}	Bus free ti...	4.700 us	---	259.681 us	323.345 us	446.687 us	65.990 us	8	Pass
14	$t_{VD;DAT}$	Data valid ...	---	3.450 us	111.416 ns	619.060 ns	1.656 us	516.073 ns	145	Pass
15	$t_{VD;ACK}$	Data valid ...	---	3.450 us	505.339 ns	2.218 us	2.750 us	822.999 ns	11	Pass
16	$t_{LOW;SEXT}$	Cumulativ...	---	25.000 ms	2.454 us	2.791 us	4.631 us	479.555 ns	306	Pass
17	$t_{LOW;MEXT}$	Cumulativ...	---	10.000 ms	2.454 us	2.791 us	4.631 us	479.555 ns	306	Pass

7. 詳細報告



	Waveform No	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	1-1	249.982 us	START	00		4.700 us	---	---	---	---	---	---
2	1-2	500.337 us	START	50		4.700 us	---	446.687 us	446.687 us	446.687 us	1	Pass
3	1-3	549.412 us	RESTART	50	10	4.700 us	---	---	---	---	---	---
4	1-4	750.716 us	START	50	12	4.700 us	---	301.538 us	301.538 us	301.538 us	1	Pass
5	1-5	1.001 ms	START	50	14 16	4.700 us	---	399.960 us	399.960 us	399.960 us	1	Pass
6	1-6	1.252 ms	START	50	18 1A 1C	4.700 us	---	352.884 us	352.884 us	352.884 us	1	Pass
7	1-7	1.502 ms	START	50	1E 20 22 24	4.700 us	---	306.308 us	306.308 us	306.308 us	1	Pass
8	1-8	1.753 ms	START	50	26 28 2A 2C	4.700 us	---	259.964 us	259.964 us	259.964 us	1	Pass
9	1-9	2.003 ms	START	50	2E 30 32 34	4.700 us	---	259.681 us	259.681 us	259.681 us	1	Pass
10	1-10	2.253 ms	START	50	36 38 3A 3C	4.700 us	---	259.735 us	259.735 us	259.735 us	1	Pass

8. 波形和參考點



	Waveform No	TimeStamp	Status	Address	D0-D7	Limit Min	Limit Max
1	1-1	249.982 us	START	00		250.000 ns	---
2	1-2	500.337 us	START	50		250.000 ns	---
3	1-3	549.412 us	RESTART	50	10	250.000 ns	---
4	1-4	750.716 us	START	50	12	250.000 ns	---
5	1-5	1.001 ms	START	50	14 16	250.000 ns	---
6	1-6	1.252 ms	START	50	18 1A 1C	250.000 ns	---
7	1-7	1.502 ms	START	50	1E 20 22 24	250.000 ns	---
8	1-8	1.753 ms	START	50	26 28 2A 2C	250.000 ns	---
9	1-9	2.003 ms	START	50	2E 30 32 34	250.000 ns	---
10	1-10	2.253 ms	START	50	36 38 3A 3C	250.000 ns	---

Waveform No.	TimeStamp	Status	Address	D0-D7
1-2	500.337 us	START	50	

	Time	Δ Time	Volt	Δ Volt	Result
1	(1.005 ms, 1.006 ms)	976.212 ns	(3.5 V, 1.5 V)	-2 V	Pass
2	(1.009 ms, 1.011 ms)	1.386 µs	(1.5 V, 1.5 V)	0 V	Pass
3	(1.015 ms, 1.016 ms)	976.212 ns	(3.5 V, 1.5 V)	-2 V	Pass
4	(1.019 ms, 1.021 ms)	1.382 µs	(1.5 V, 1.5 V)	0 V	Pass

Close

9. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

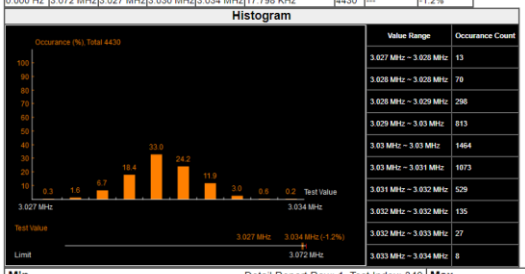
Total: 13
Pass: 13
Fail: 0

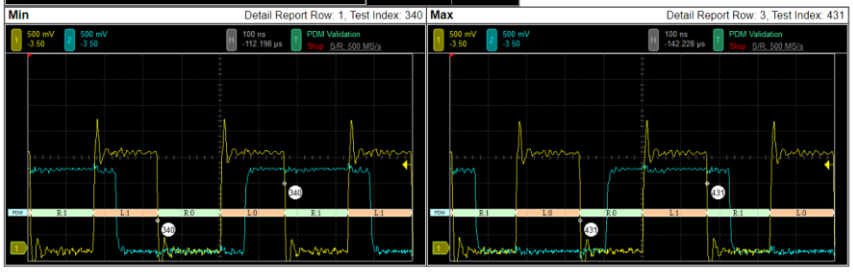
Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{CLK}	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%	✓Pass
2	t_{LOW}	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	✓Pass
3	t_{HIGH}	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	✓Pass
4	t_{rCL}	Rise time of CLK signal	---	13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	---	-85.7%	✓Pass
5	t_{fCL}	Fall time of CLK signal	---	13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	---	-85.7%	✓Pass
6	t_{fDD}	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	✓Pass
7	t_{fDV}	Delay time from Clk edge to Data Fall Valid	---	100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	---	-20.7%	✓Pass
8	t_{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	✓Pass
9	t_{rDV}	Delay time from Clk edge to Data Rise Valid	---	100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	---	-24.8%	✓Pass
10	V_{ClkLow}	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	✓Pass
11	$V_{DataLow}$	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	✓Pass
12	$V_{ClkHigh}$	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	✓Pass
13	$V_{DataHigh}$	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	✓Pass

---

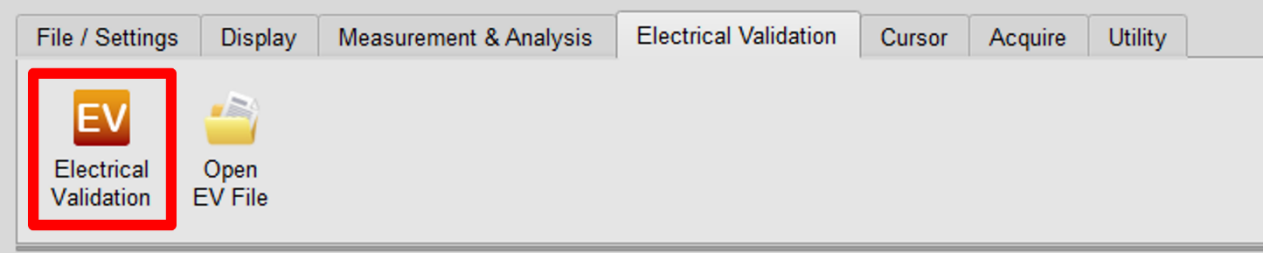
f_{CLK} - Test Result: Pass
Description: Clock frequency

Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	---	-1.2%





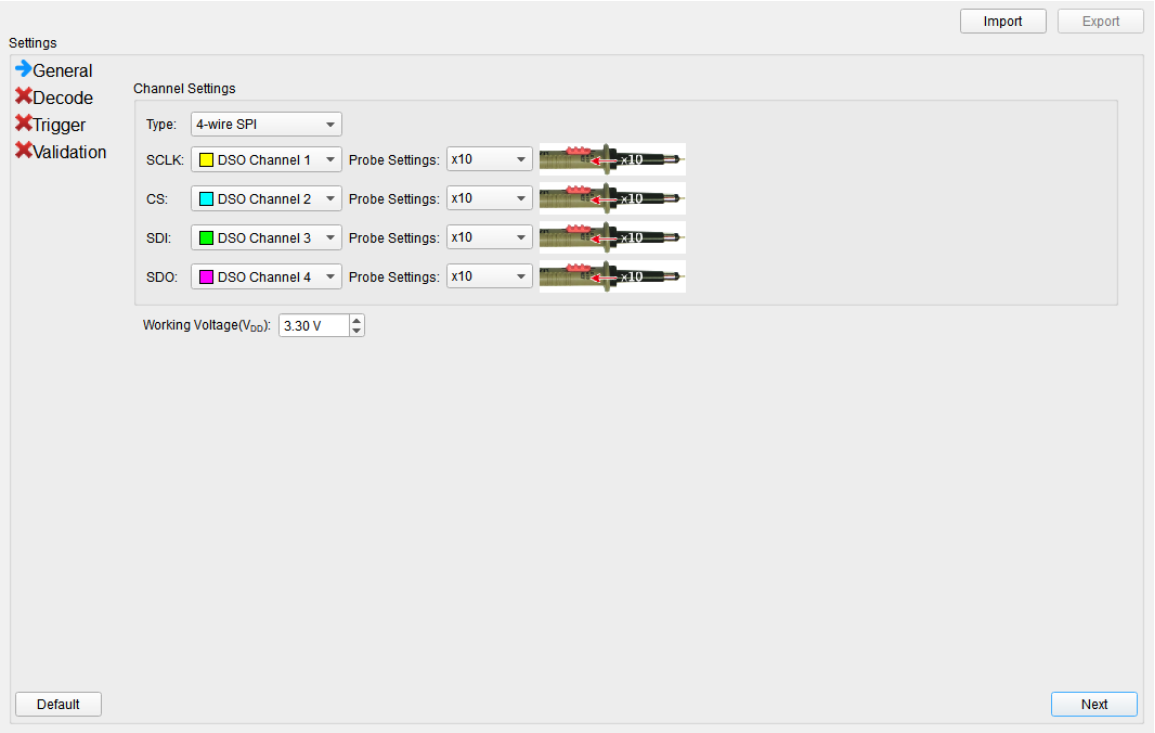
SPI 電氣特性驗證解決方案



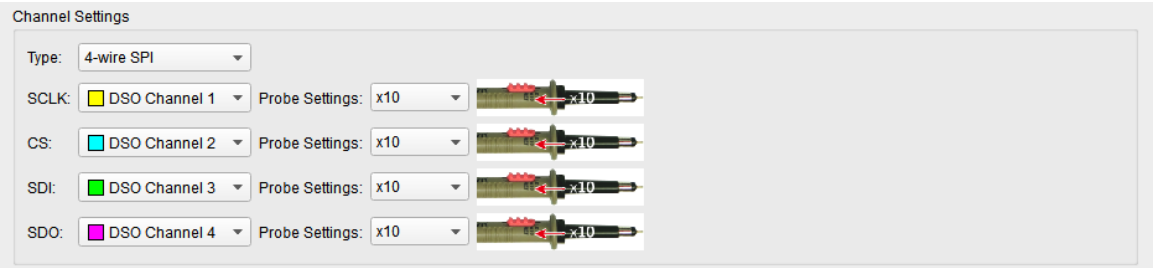
使用示波器執行 SPI（Serial Peripheral Interface）電氣特性驗證，以確保其訊號符合所定義的電氣規格。在經過長時間燒機測試後，可確認待測訊號的電氣特性是否達標。

SPI 電氣特性驗證設定

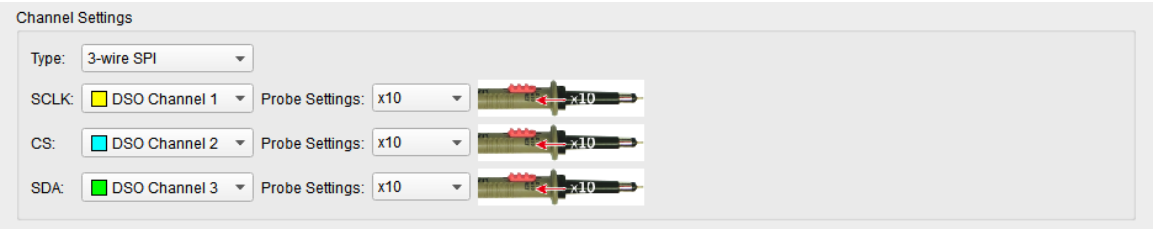
1. 一般設定：根據匯流排配置選擇 SPI 類型（4-wire SPI 或 3-wire SPI）。



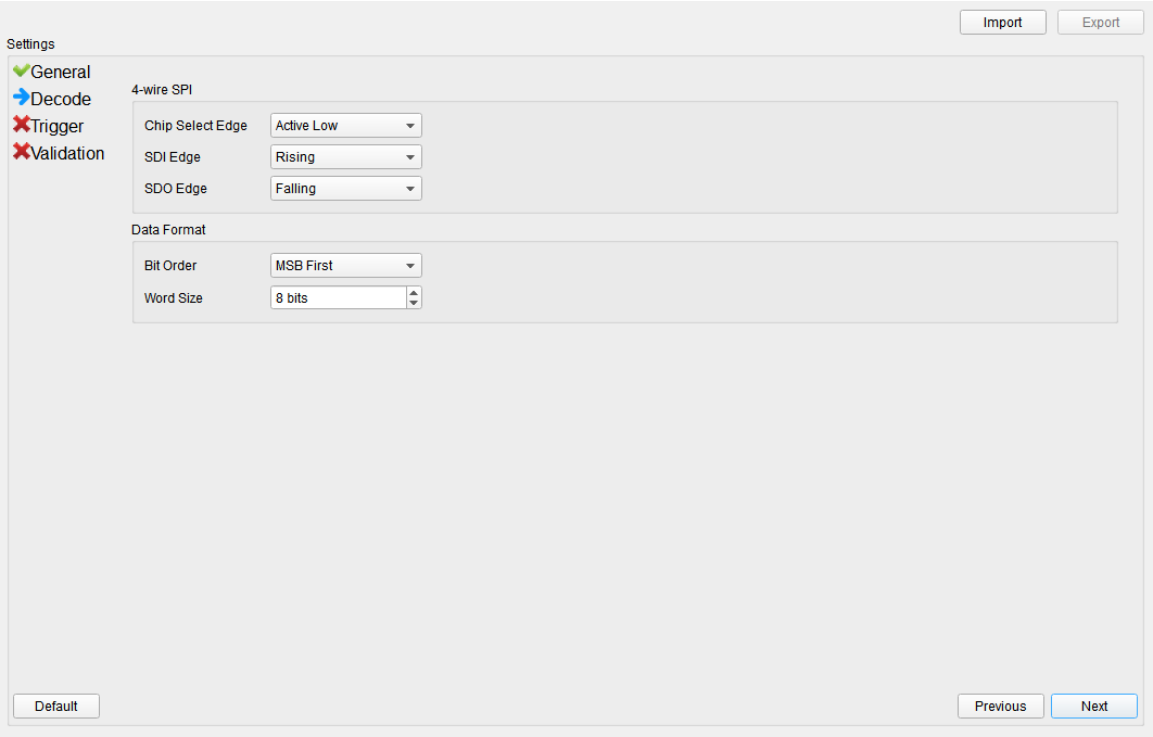
4-wire 設定：



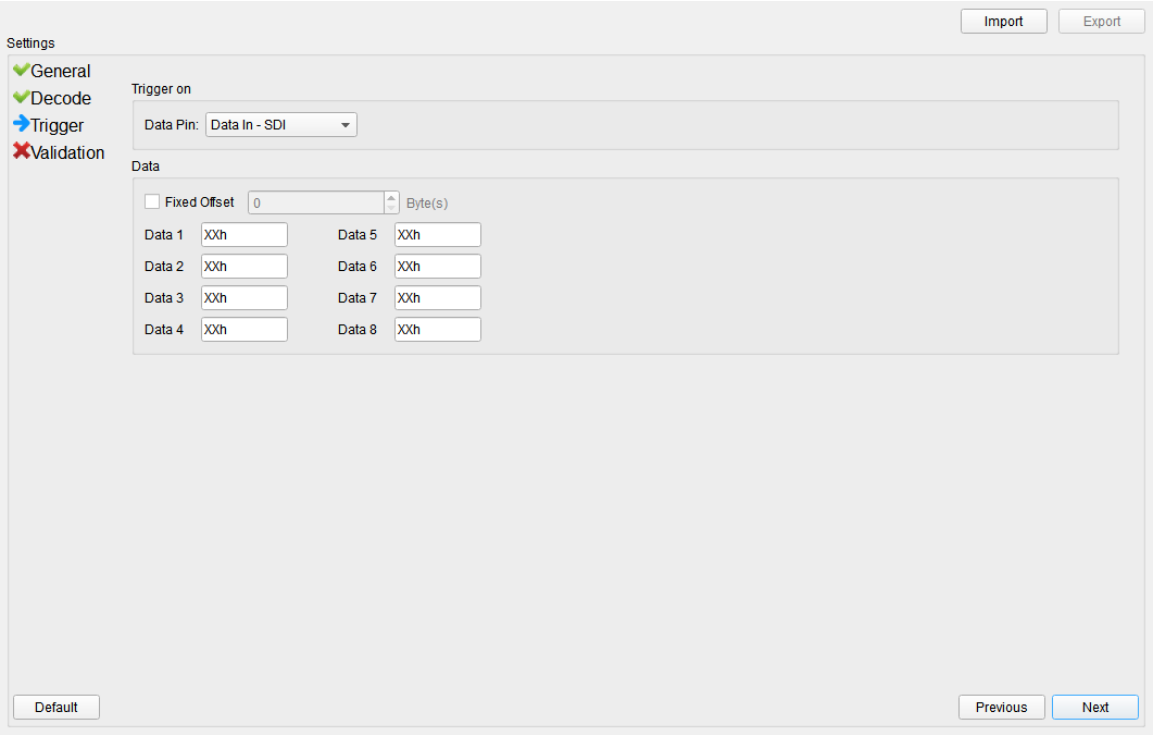
3-wire 設定：



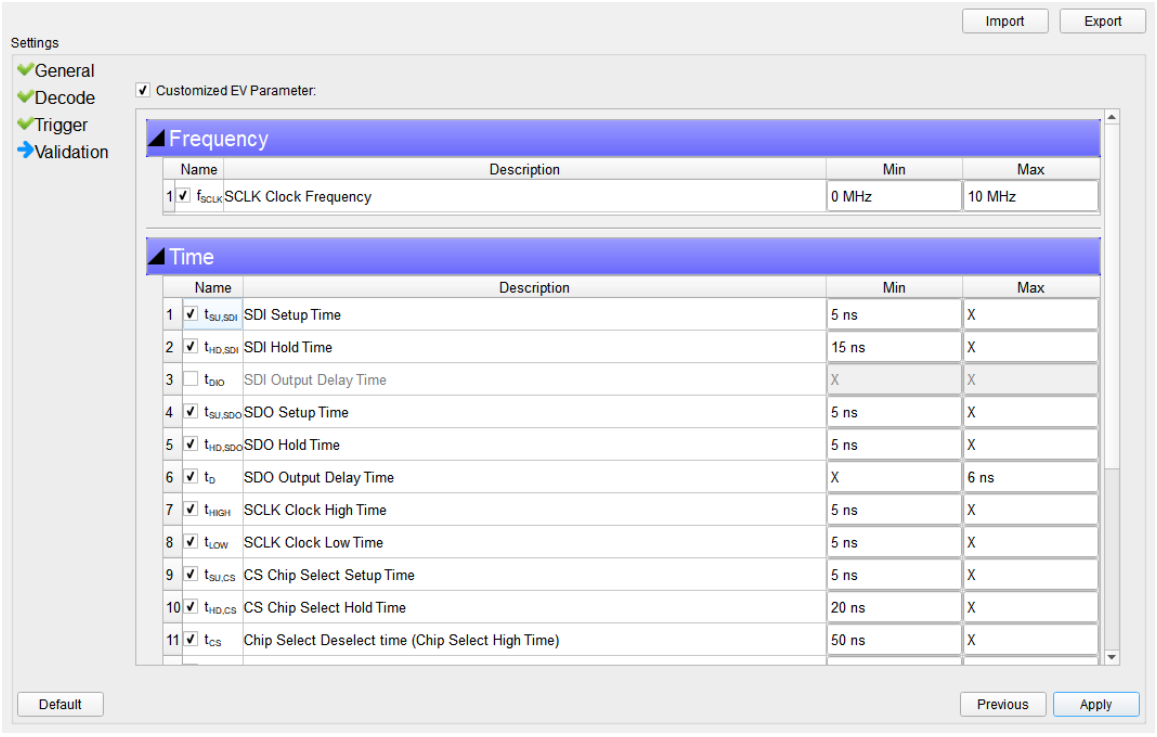
2. 解碼設定：設定 SPI 的資料格式以及各個通道的 Latching Edge。這裡所設定的 SPI 資料格式會同時套用至解碼與觸發設定中。



3. 觸發設定：資料格式已在上一頁設定完畢。本部分剩下的設定重點是資料位址與要觸發的資料腳位。



4. 驗證參數設定



由於 SPI 匯流排並未有官方標準的測量門檻，因此在進行驗證時，請使用者自行定義合適的參數限制。

本區塊顯示三項特性參數表，包括：

- 頻率
- 時序參數
- 電壓需求

所有支援的驗證參數項目與說明如下：

SPI Frequency Requirements

Symbol	Electrical Parameter
f_{SCLK}	SCLK Clock Frequency

SPI Timing Requirements

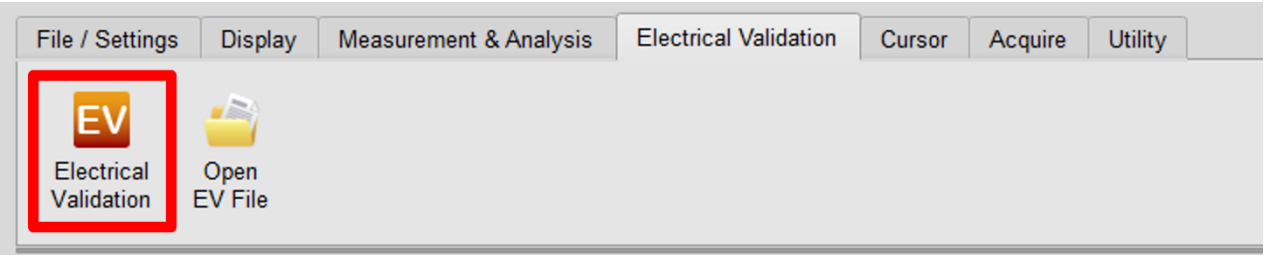
Symbol	Electrical Parameter
$t_{SU,SDI}$	SDI Setup Time
$t_{HD,SDI}$	SDI Hold Time
t_{DIO}	SDI Output Delay Time
$t_{SU,SDO}$	SDO Setup Time
$t_{HU,SDO}$	SDO Hold Time
t_{D}	SDO Output Delay Time
t_{HIGH}	SCLK High Time
t_{LOW}	SCLK Low Time
$t_{SU,CS}$	CS Chip Select Setup Time
$t_{SU,CS}$	CS Chip Select Hold Time
t_{CS}	Chip Select Deselect time (Chip Select High Time)
t_{CLKr}	SCLK Clock Rise Time
t_{CLKf}	SCLK Clock Fall Time

SPI Voltage Requirements

Symbol	Electrical Parameter
V_{IL}	Low-Level Input Voltage
V_{IH}	High-level Input Voltage
V_{OL}	Low-level Output Voltage
V_{OH}	High-level Output Voltage

UART 電氣特性驗證解決方案

■ 簡介：



使用示波器進行 UART 電氣特性驗證，以確認 UART 是否符合所定義的規格。在長時間燒機測試之後，可驗證被測訊號的電氣特性是否達標。

對於協定的電氣驗證，UART 協定的電氣特性檢測通常分為兩種：**垂直（電壓）與水平（時間/相位）**。

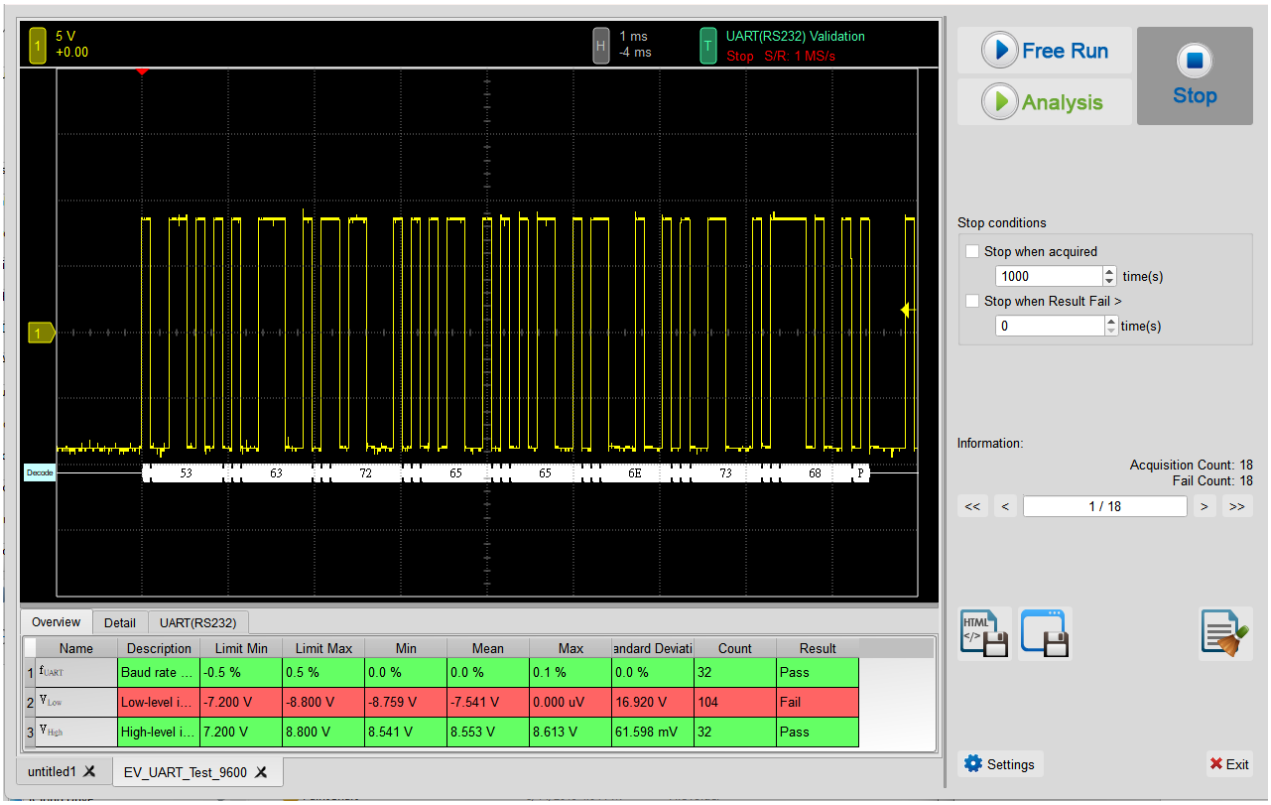
因此，使用本功能前，需先設定協定類型與規格，然後重複測試以獲得電氣特性測試報告。測試項目會依 UART 傳輸速率不同而有不同的規格與標準。

UART 驗證報告：

Overview | Detail | UART(RS232)

	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f_{UART}	Baud rate ...	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	Pass
2	V_{Low}	Low-level i...	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	Fail
3	V_{High}	High-level i...	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	Pass

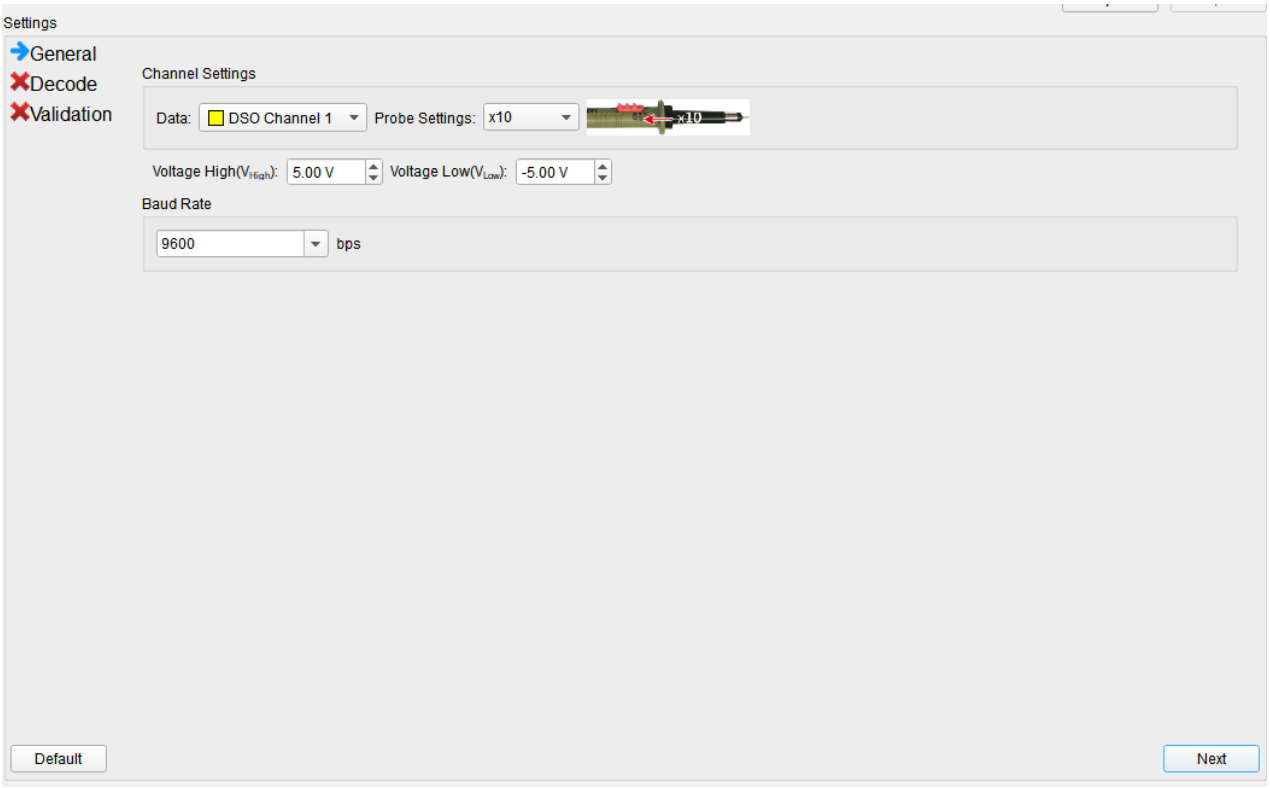
電氣特性驗證_軟體頁面：



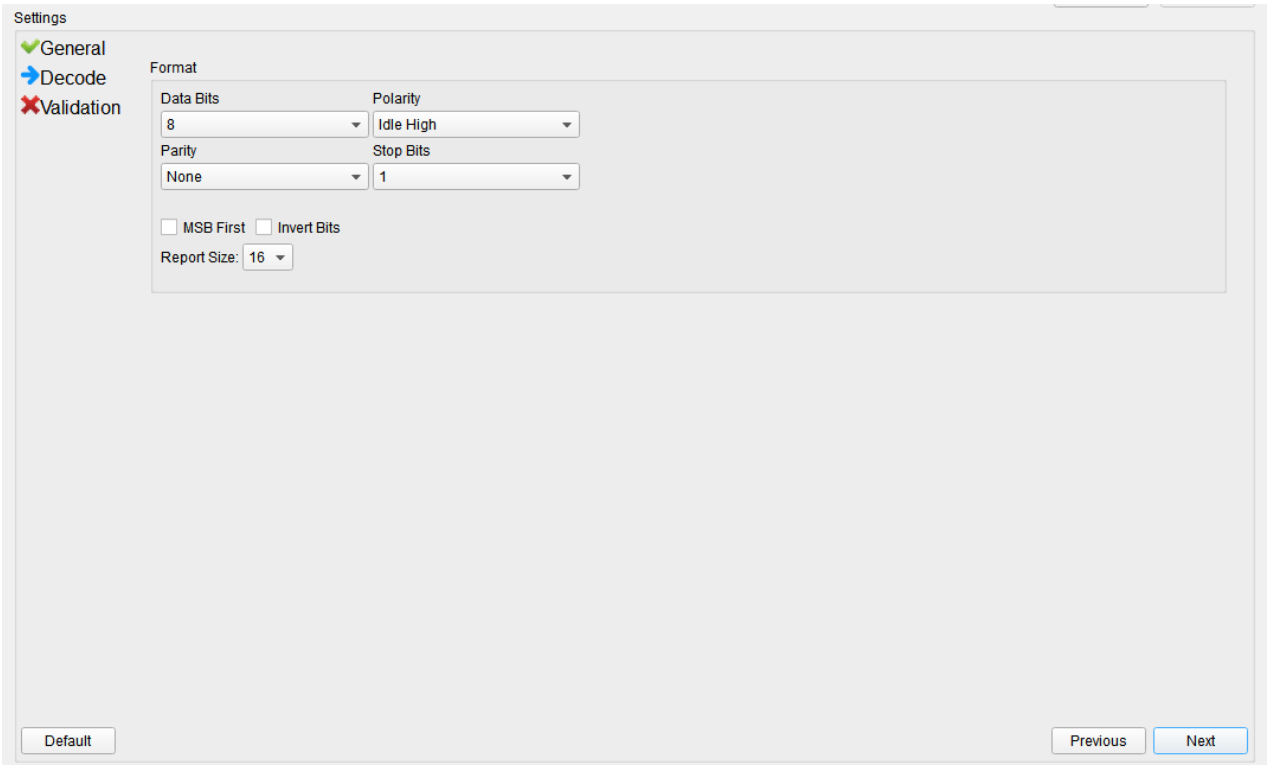
1. 頻率：時脈速率
2. 時序：Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
3. 電壓：V_L, V_H, etc.

UART 電氣特性驗證設定

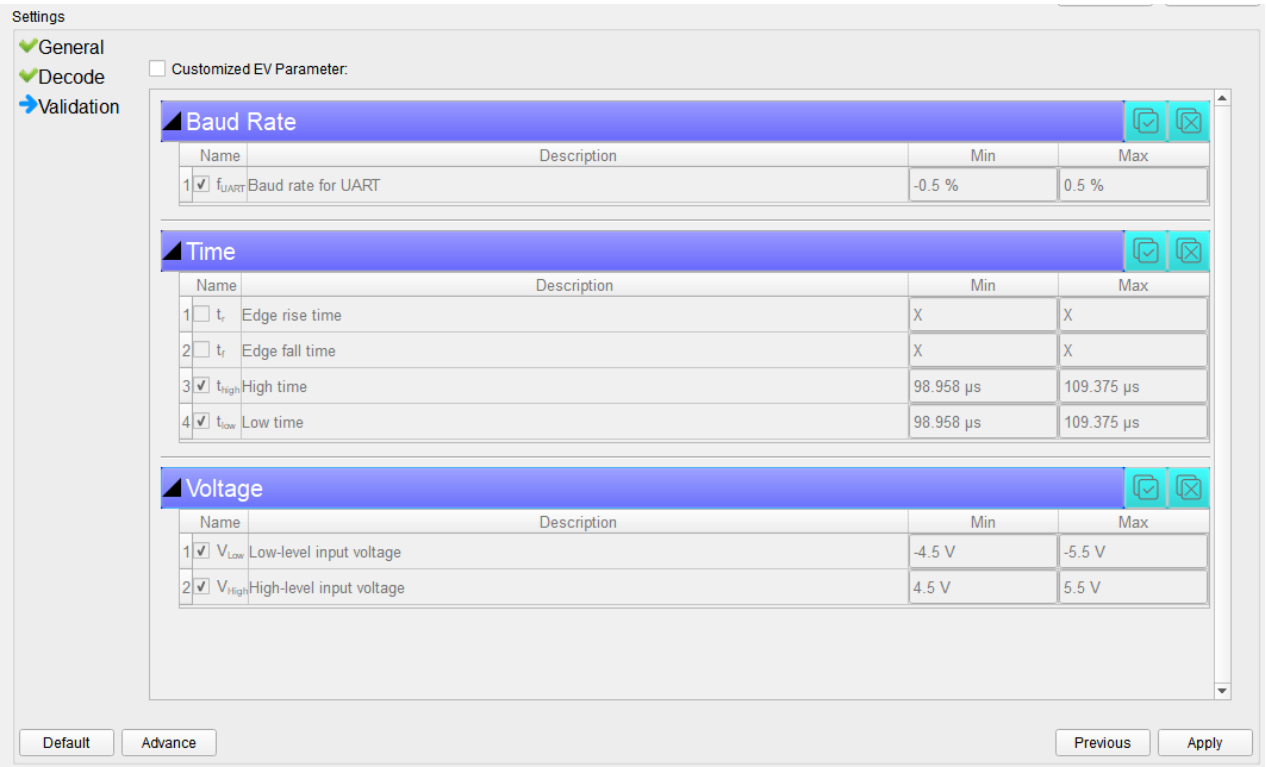
1. 一般設定：通道來源、工作電壓與傳輸速率



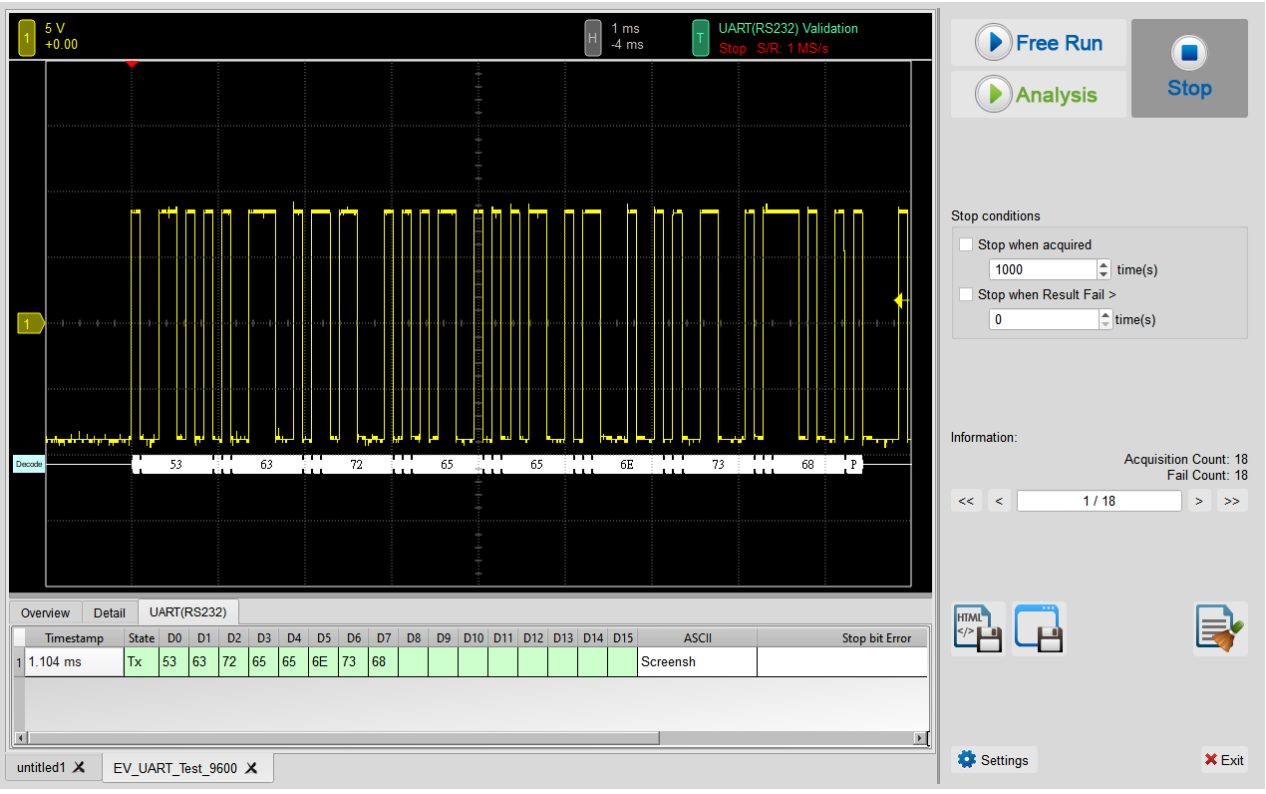
2. 解碼設定：UART 解碼設定



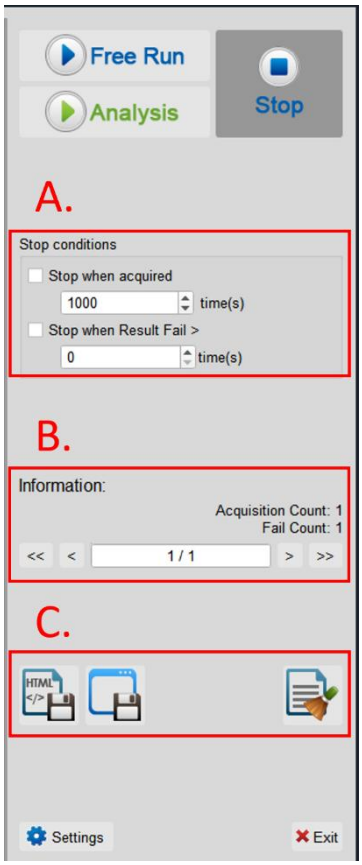
3. 驗證參數設定：頻率、時序與電壓限制



4. 電氣特性驗證 軟體畫面



5. 控制面板



A. 停止條件：

當擷取達到 X 次時停止

當測試結果失敗超過 X 次時停止

B. 資訊：

選擇查看波形

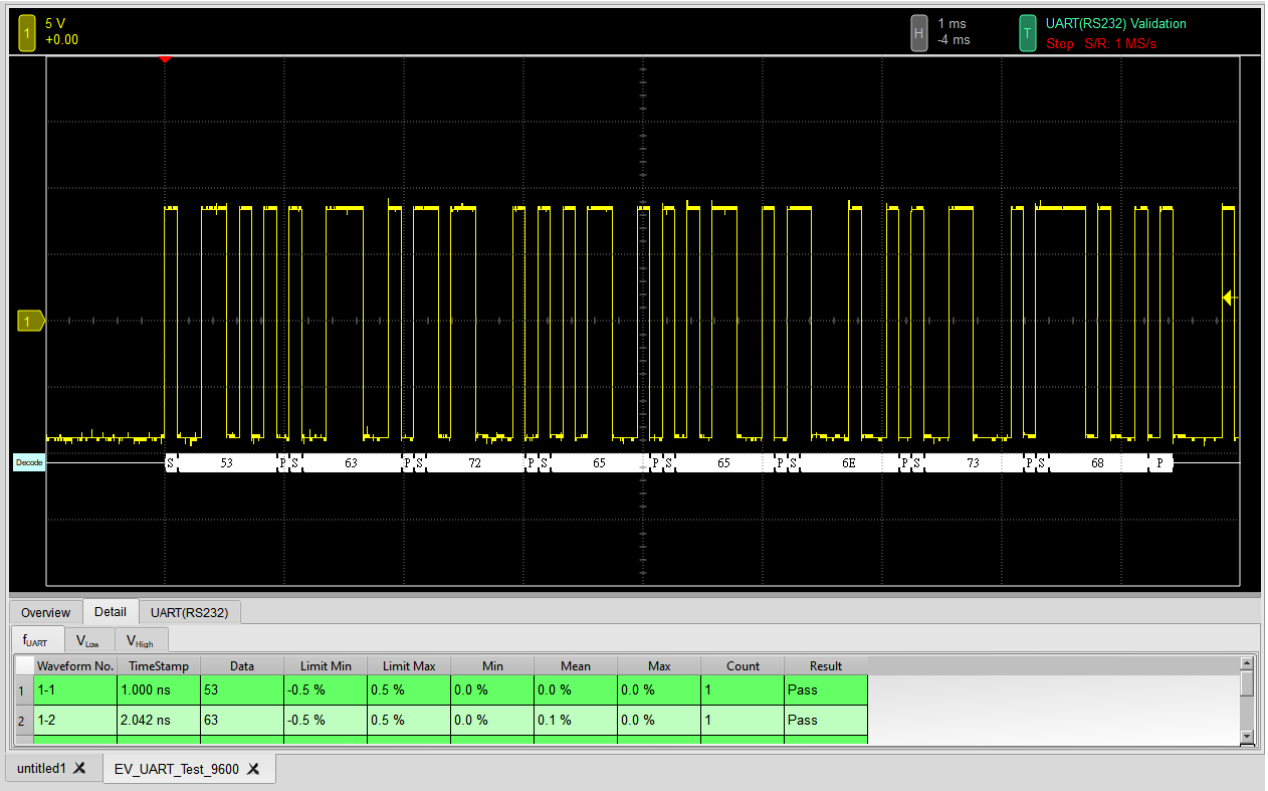
C. 儲存檔案：

儲存為 HTML 格式

儲存為 .MOW（Acute軟體專用格式）

6. 概覽報告

7. 詳細報告



8. 波形和參考點

9. Html 報告

Acute
PC-based T&M Instruments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	04-27-2023 15:07:32
S/W Version	1.0.25
Protocol	UART(RS232)

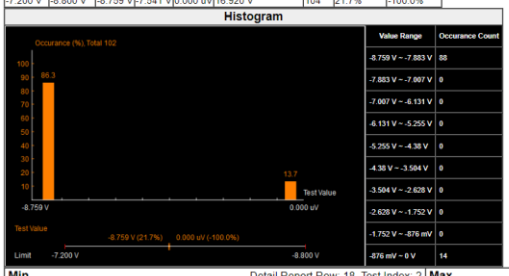
Overview Results:

Total: 3
Pass: 2
Fail: 1

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f_{UART}	Baud rate for UART	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	-100.0%	-80.0%	✓Pass
2	V_{Low}	Low-level input voltage	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	21.7%	-100.0%	✗Fail
3	V_{High}	High-level input voltage	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	18.6%	-2.1%	✓Pass

V_{Low} - Test Result: Fail
Description: Low-level input voltage

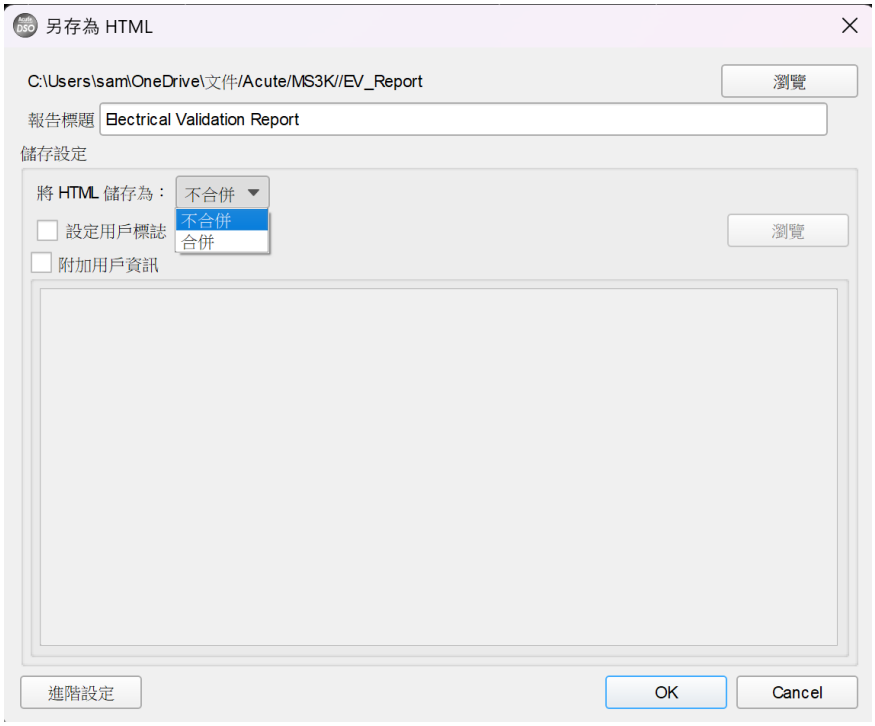
Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max
-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	21.7%	-100.0%



HTML 報告匯出

■ 簡介

每次 EV 測試皆支援匯出 HTML 報告。HTML 報告包含每個測試項目、測試結果、最大/最小值、長條圖與波形截圖。



儲存設定：

A. 將 HTML 儲存為：不合併/合併

不合併：圖片會與 HTML 分開儲存。

合併：圖片會嵌入在 HTML 檔案中（單一檔案）。

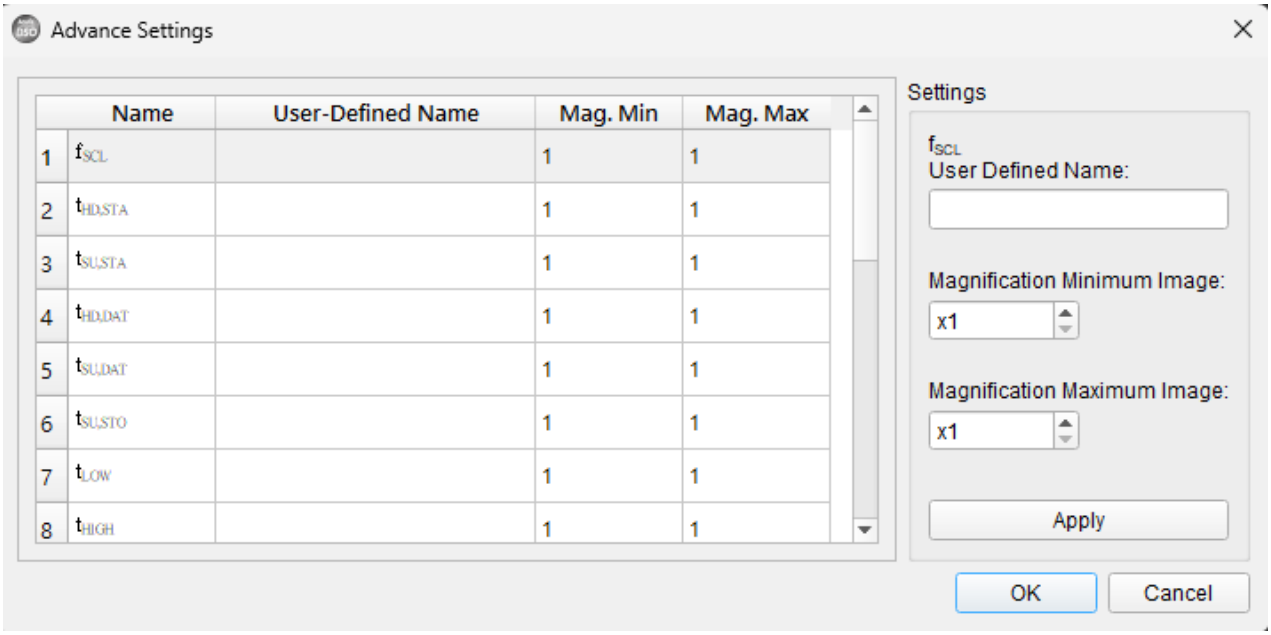
B. 設定用戶標誌 Logo：

勾選後可選擇圖片檔作為報告中的公司/用戶標誌。

C. 附加用戶資訊：

可在此輸入任何想要加入到報告中的補充說明或使用者資訊。

進階設定：



A. 使用者可自訂測試項目於 HTML 報告中的顯示名稱

B. 使用者亦可調整 HTML 報告中圖片的顯示倍率

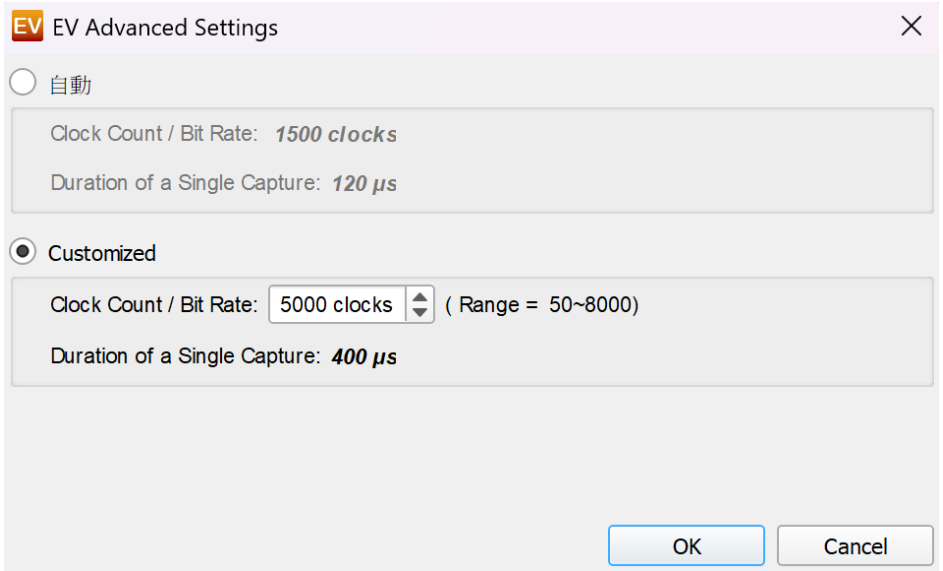
進階設定

■ 簡介

EV 測試允許使用者根據每次擷取的需求，調整預設的擷取時間。由於不同的協定有不同的預設時脈或傳輸速率，這些差異主要來自於協定的傳輸速度與封包長度的不同。有時候，為了更準確地分析資料，可能需要擷取更長的封包。因此，**Acute** 提供了 **進階設定** 功能，讓使用者可以個別調整各項參數的擷取時間。

***僅在進入 EV 參數設定 時，才會顯示 進階設定 按鈕**

EV 進階設定：



MSO/TS3000 系列多機堆疊

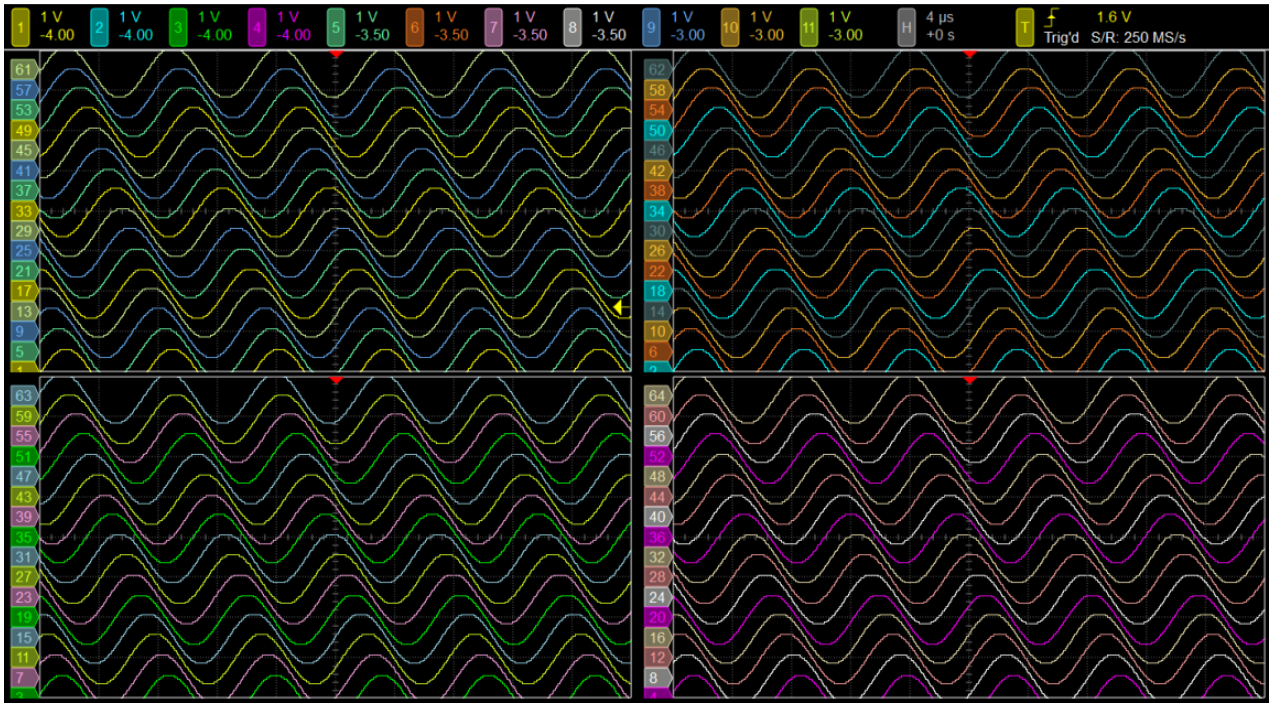
■ 簡介

Acute MSO3K / TS3K示波器的特點之一是其多機組合堆疊功能，這使得最多可堆疊16台示波器，同時實現64通道最高250MS/s，或是16通道最高1GS/s的量測能力。在機殼設計方面，MSO3K / TS3K專為堆疊應用而設計，具備精心設計的定位導槽，使示波器在堆疊配置中能夠完美擺放。此外，示波器的散熱性能也得到了充分考慮，配置了雙側散熱孔，確保長時間運行時不會出現過熱問題。

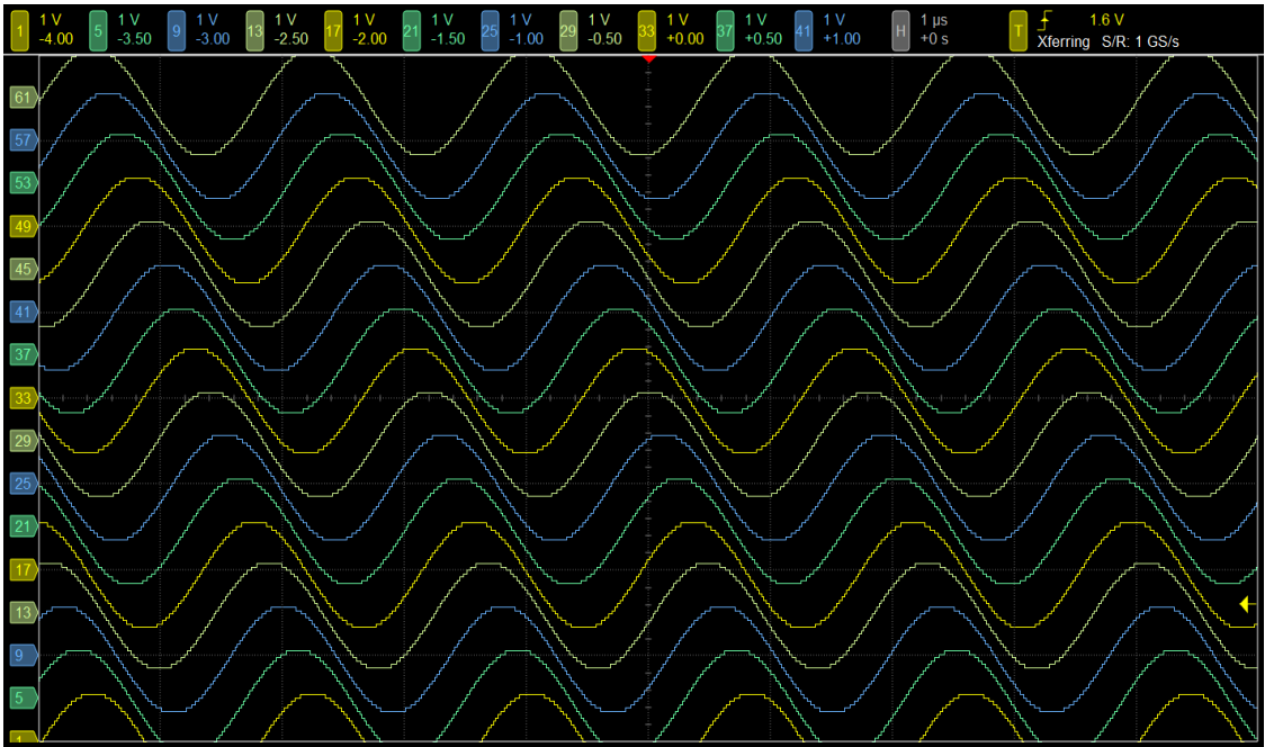
在訊號連接方面，使用者可以選擇直接將待測訊號通過標準BNC接頭連接到示波器，或者使用被動探棒或差動探棒進行更廣泛性的量測。此外，Acute還提供了BNC to Probe Tip Adaptor，可以改善傳統探棒在連接上常見的量測連接品質問題，確保用戶獲得最準確的測量結果。

軟體畫面

1. 64Channel @ 250MS/s



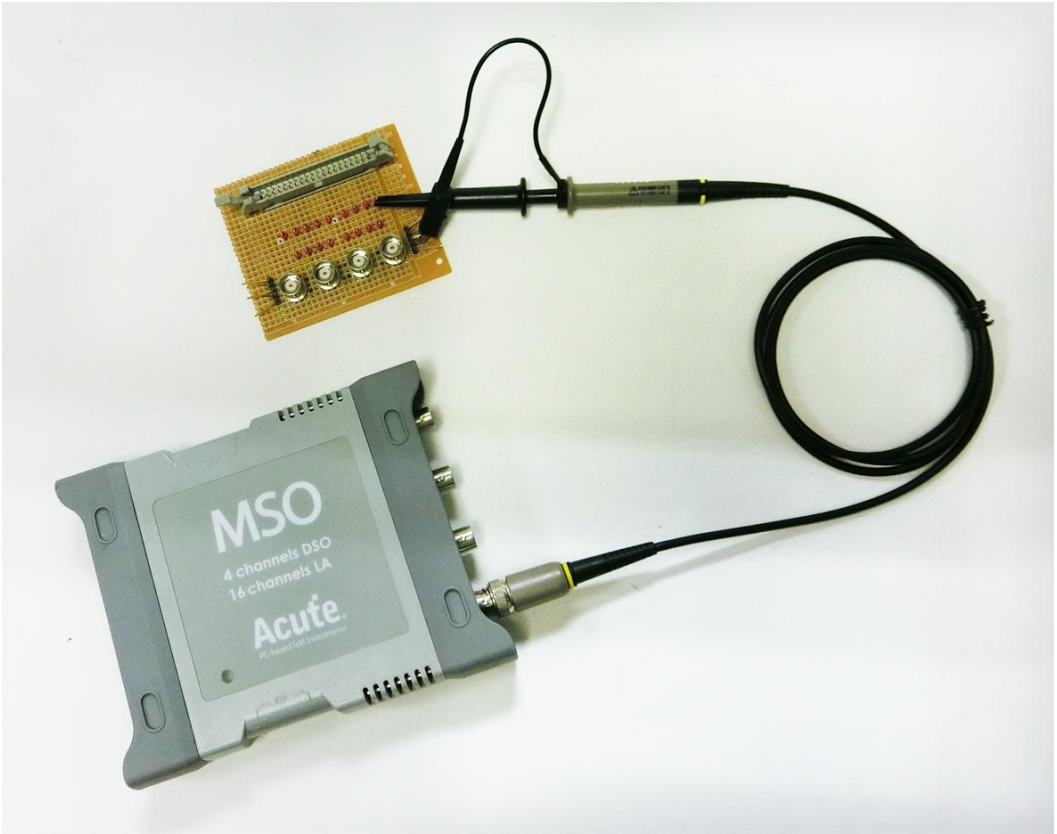
2. 16Channel @ 1GS/s



各種訊號連接方式

1. 訊號線直接透過BNC to BNC接頭連接

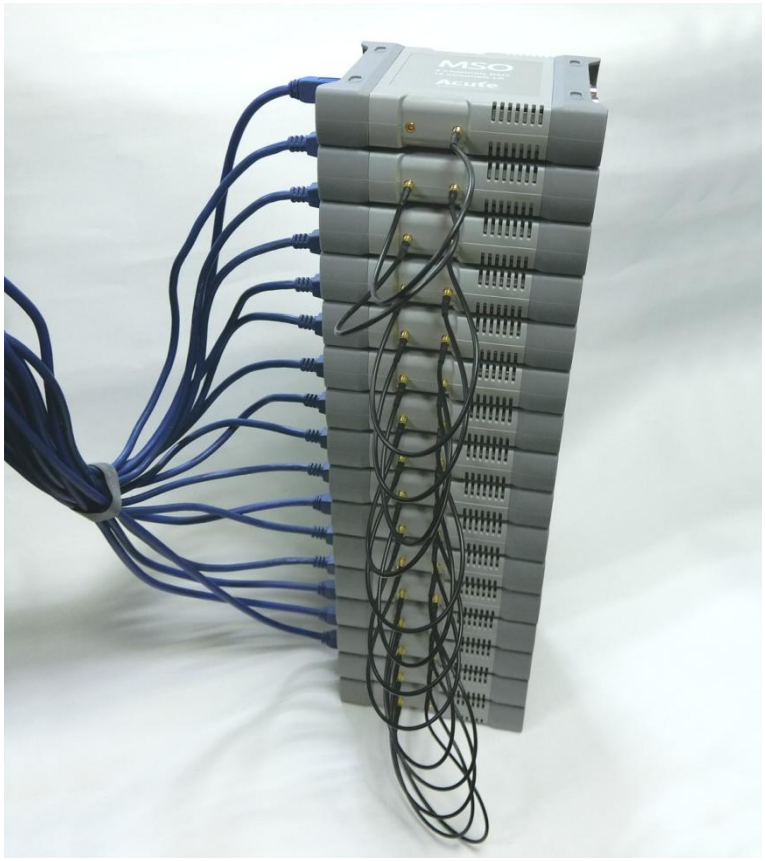
2. 搭配被動探棒量測



3. 搭配被動探棒以及BNC to Probe Tip Adaptor量測

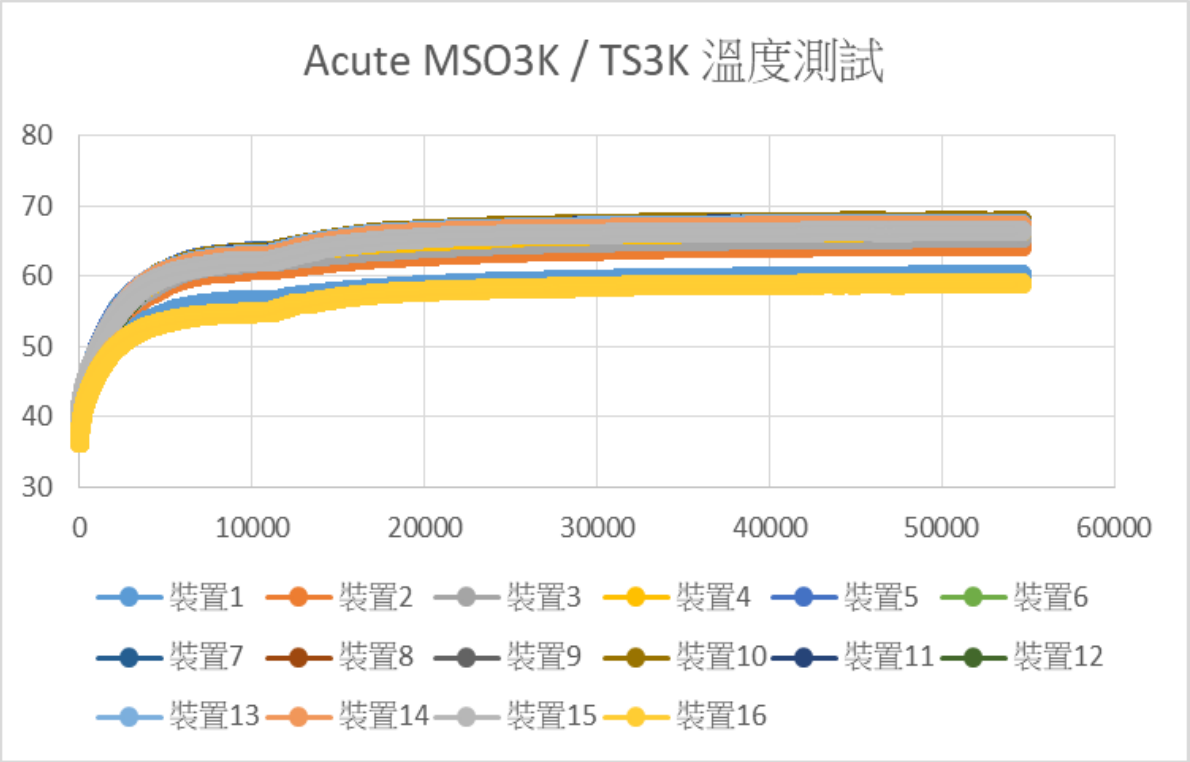
4. 搭配高壓差動探棒量測

5. 實際堆疊畫面 16台(64 Channels)



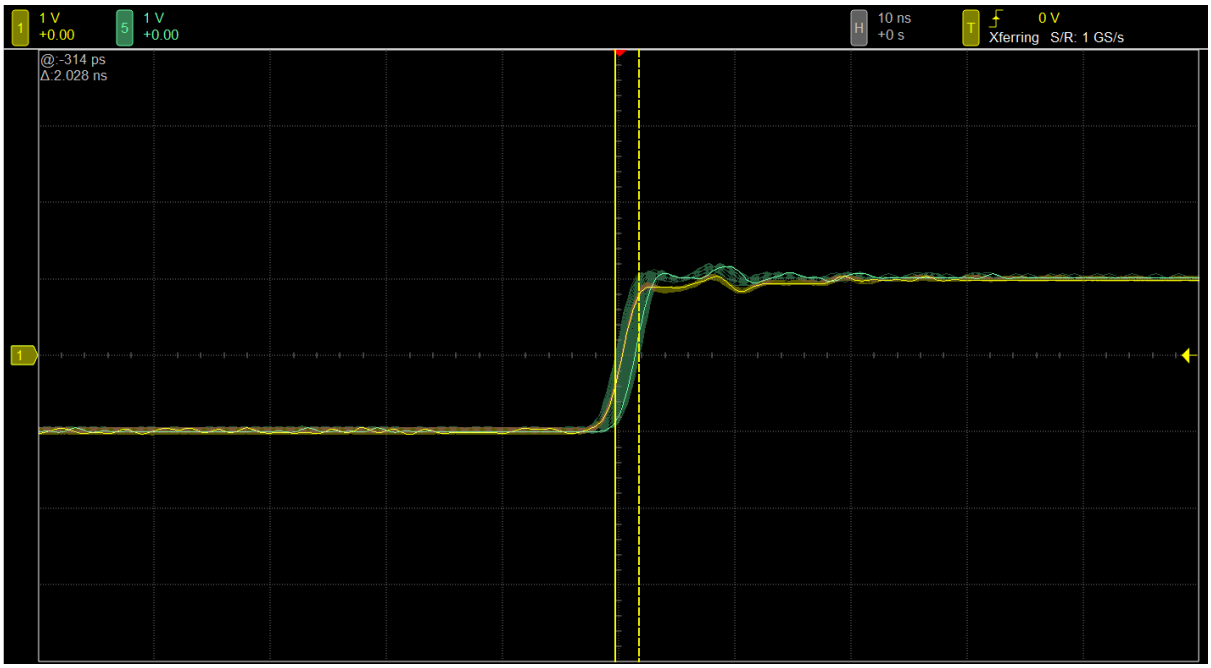
注意事項

1. MSO3K / TS3K 示波器為 USB3.0 介面的儀器，運作時需消耗 4.5~7.7W，使用時建議連接至電腦後方的 USB3.0 插槽或是使用具有獨立供電的 USB3.0 hub，以提供最佳的電力供應及最佳量測性能。
2. MSO3K / TS3K 示波器經過內部測試，在堆疊狀態下仍可保持長時間運作不致過熱，但若長時間於高溫或不利於散熱環境使用時，仍須注意示波器使用溫度並適度提供額外散熱方式，以避免示波器過熱 (> 80 度 C) 而影響操作。



3. 多機堆疊時，各機器間根據取樣率不同，會產生一定程度的相位差，以 1GS/s 取樣率為例，主機和第一台從機間的相位差為 <±2ns，和最後一台從機間的相位差為 <±3ns。

主機和第一台從機(2nd)的相位差



主機和最後一台從機(16th)的相位差