

電氣特性驗證說明





目錄

Protocols

其他設定

HTML 報告匯出	66
進階設定	68
MSO/TS3000 系列多機堆疊	. 69



I²C 電氣特性驗證解決方案

■ 簡介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器進行 I²C 電氣特性驗證,以確保 I²C 符合定義的規範。在經過長時間的燒機 測試後,可以確認所測試的訊號電氣特性符合規範。

1²C 協定的電氣特性檢測通常分為兩種類型:垂直(電壓)與水平(時間/相位)。

因此,在使用此功能時,必須先設定所選的協定與規格,然後重複測試以取得電氣特性測 試報告。測試項目會依據 I²C 的速度而有所不同。

常見 I²C 規格中的部分電氣特性規格:

Symbol	Parameter	Conditions	C _b = 100	pF (max)	C _b = 4	00 pF ^[2]	Unit
			Min	Max	Min	Max	
f _{SCLH}	SCLH clock frequency		0	3.4	0	1.7	MHz
t _{SU;STA}	set-up time for a repeated START condition		160	-	160	*	ns
t _{HD;STA}	hold time (repeated) START condition		160		160		ns
tLOW	LOW period of the SCL clock		160		320	1	ns
t _{HIGH}	HIGH period of the SCL clock		60	-	120	-	ns
t _{SU;DAT}	data set-up time		10		10	8	ns
t _{HD;DAT}	data hold time		0 ^[3]	70	0 ^[3]	150	ns
t _{rCL}	rise time of SCLH signal		10	40	20	80	ns
t _{rCL1}	rise time of SCLH signal after a repeated START condition and after an acknowledge bit		10	80	20	160	ns
tfCL	fall time of SCLH signal		10	40	20	80	ns

Table 13. Characteristics of the SDAH, SCLH, SDA and SCL bus lines for Hs-mode I²C-bus devices^[1]



I²C 電氣特性驗證 報告內容:

C	verview De	etail I2C							
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Count	Result
1	fact	SCL clock frequencey	0.000 Hz	400.000 KHz	387.596 KHz	387.683 KHz	387.897 KHz	34200	Pass
2	1HDUST A	Hold time(repeated) START condition	600.000 ns	-	1.536 us	1.537 us	1.540 us	200	Pass
3	ISU,STA	Set-up time for a repeated START condition	600.000 ns	-	2.010 us	2.012 us	2.014 us	100	Pass
4	1HDLDAT	Data hold time	-	-	94.000 ns	274.110 ns	1.028 us	17250	Pass
5	loudat.	Data Set-up time	100.000 ns	-	472.000 ns	1.066 us	1.444 us	25100	Pass
6	leusto	Set-up time for STOP condition	-	-	-	-	-	0	-
7	tLow	Low Period of the SCL Clock	1.300 us	-	1.538 us	1.542 us	1.544 us	34100	Pass
8	U HIOH	High Period of the SCL Clock	600.000 ns	-	974.000 ns	982.475 ns	3.560 us	41800	Pass
9	łec.	Rise time of SCL signal	20.000 ns	300.000 ns	45.999 ns	50.304 ns	51.999 ns	41800	Pass
10	tres.	Fall time of SCL signal	20.000 ns	300.000 ns	10.000 ns	10.528 ns	11.999 ns	41800	Fail
11	\$DA	Rise time of SDA signal	20.000 ns	300.000 ns	37.999 ns	39.210 ns	41.999 ns	9300	Pass
12	10A	Fall time of SDA signal	20.000 ns	300.000 ns	4.000 ns	6.714 ns	10.000 ns	9900	Fail
13	teur	Bus free time between a STOP and START condition	-	-	-	-	-	0	-
14	IVD,DAT	Data valid time	-	900.000 ns	98.000 ns	267.062 ns	1.068 us	15750	Fail
15	TVDLACK	Data valid acknowledge time	-	900.000 ns	98.000 ns	623.009 ns	1.068 us	1500	Fail

電氣特性驗證 軟體畫面:



- 不同的速度模式,包含標準模式(Standard Speed Mode,約 100kHz)/快速模式 (Fast Mode,約 400kHz)/快速模式+(Fast Mode+,約 1MHz)/高速模式(HS Mode,約 3.4MHz)
- 2. 頻率:時鐘頻率(Clock Speed)
- 3. 時序參數:Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 4. 電壓參數:V_IL (輸入低電位)、V_IH (輸入高電位)等



■ I²C 電氣特性驗證設定

1. 一般設定:通道來源、工作電壓與速度

Settings		Import	Export
General	Channel Settings		
TriggerValidation	SCL: □ DSO Channel 1 ▼ Probe Settings: x10 ▼ x10 → SDA: □ DSO Channel 2 ▼ Probe Settings: x10 ▼ x10 →		
	Working Voltage(V _{DD}): 3.30 V ♀ Speed Mode		
	 Standard Mode (Max: 100Kbit/s) Fast Mode (Max: 400Kbit/s) 		
	 ○ Fast Mode + (Max: 1Mbit/s) ○ High Speed Mode (Max: 3.4Mbit/s) Cb Value= 100pf (Max.) ▼ 		
	Customized Speed 100 Kbit/s		
Default		[Next

2. 解碼設定: I²C 解碼設定

Settings		Import	Export
 ✓General →Decode 	Address Mode		
 Trigger Validation 	 7-bit Addressing 8-bit Addressing (Including R/W in Address) 10-bit Addressing 		
Default		Previous	Next



3. 觸發設定:I²C Address、Data 觸發條件

Settings		
✓General	Trigger Settings	
 Decode Trigger Validation 	7-bit Address: XXh Write/Read: ACK/NACK	
	Data	
	Any Offset Fixed Offset	
	0 Bytes	
	Value	
	XXh 💌	
	XXh 👻	
	XXh	
	XXh •	
Default		Previous Next

4. 驗證參數設定:頻率、時序與電壓限制

	requenc	2V		
-	Name	Description	Min	Max
1	✓ f _{SCL} SCL cl	ock frequency	0 kHz	100 kHz
	Time			
	Name	Description	Min	Max
1	✓ t _{HD,STA}	Hold time(repeated) START condition	4 us	X
2	✓ t _{SU,STA}	Set-up time for a repeated START condition	4.7 us	x
3	✓ t _{HD,DAT}	Data hold time	5 us	X
4	✓ t _{SU,DAT}	Data Set-up time	250 ns	X
5	✓ t _{SU,STO}	Set-up time for STOP condition	4 us	х
6	✓ t _{LOW}	Low Period of the SCL Clock	4.7 us	x
7	✓ t _{HIGH}	High Period of the SCL Clock	4 us	X
8	✓ t _{rCL}	Rise time of SCL signal	х	1 us
9	✓ t _{fCL}	Fall time of SCL signal	х	300 ns
10) ✓ t _{rDA}	Rise time of SDA signal	X	1 us
11	✓ t _{fDA}	Fall time of SDA signal	x	300 ns



Electrical Validation	n O uri				Import Export
I2C I2S MIPI I3C MIPI RFFE MIPI SPMI	✓General ✓Decode ✓Trigger	Customized EV	Parameter:		<u>40</u> 42 ▲
PDM SMBus	Validation	⊿ Time			
SPI		Name	Description	Min	Max
ART(RS232)		1 🗹 t _{HD,STA}	Hold time(repeated) START condition	160 ns	×
		2 🗹 t _{SU,STA}	Set-up time for a repeated START condition	160 ns	X
		3 🗹 t _{HD,DAT}	Data hold time	0 ns	×
		4 ✓ t _{SU,DAT}	Data Set-up time	10 ns	×
		5 🗹 t _{su,sto}	Set-up time for STOP condition	160 ns	70 ns
		6 ✔ t _{LOW}	Low Period of the SCL Clock	160 ns	×
		7 🗹 t _{HIGH}	High Period of the SCL Clock	60 ns	40 ns
		8 🗹 t _{rCLH}	Rise time of SCLH signal	10 ns	40 ns
		9 V ticch	Fall time of SCLH signal	10 ns	80 ns
		10 I t _{rDAH}	Rise time of SDAH signal	10 ns	80 ns
		11 🗹 t _{IDAH}	Fall time of SDAH signal	10 ns	×
		12 ✓ t _{BUF}	Bus free time between a STOP and START condition	x	X
		13 🗹 t _{VD,DAT}	Data valid time	×	×
		14 VD,ACK	Data valid acknowledge time	×	×
		15 t _{CLK_STRET}	CHClock extend time	×	25 ms
		16 🗸 t _{rCL1}	First rising edge time of SCL signal after Sr and after ACK bit	10 ns	80 ns
		► Voltage			
	Default	Advance			Previous Apply

第 16 項選項僅在 I²C 速度模式設定為高速模式 (High Speed Mode) 時可見



5. 電氣特性驗證 軟體畫面



6. 控制面板



A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止

B. 資訊:選擇查看波形

C. 储存檔案: 储存為 HTML 格式 储存為 .MOW (Acute軟體專用格式)

7. 概覽報告

1	500 mV -3.50	2 500 mV -3.50 3	500 mV -3.50		4 500 mV -3.50		Н 100 µs -400 µs	T I2C Trig	Validation d <u>S/R: 500 N</u>	<u>1S/s</u>
	ու ու ու երել				1.1.1.1.1.1					u . Materia
	a na pana ana amin'ny fanita amin'ny fanita amin'ny fanita amin'ny fanita amin'ny fanita amin'ny fanita amin'ny				<mark>n su to n</mark> it i ki		adoly a birny y			t t in monore
12	c	(, Addr(7b):12), (2) 10 (2) 20	30	A, Ad	lr(7b):3F	. 00 <mark>. A</mark>	Addr(7b):46	21	3A	
		and de la data data a data data data data								
0	verview Det	ail I2C								
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviatio	Count	Result 🔺
1	f _{SCL}	SCL clock frequencey	0.000 Hz	100.000 KHz	99.994 KHz	99.998 KHz	100.004 KHz	11.000 Hz	480	Fail
2	t _{HD,STA}	Hold time(repeated) START condition	4.000 us		2.499 us	3.094 us	4.999 us	1.817 us	21	Fail
3	t _{SU,STA}	Set-up time for a repeated START condition							0	
4	t _{HD,DAT}	Data hold time	5.000 us		2.497 us	2.498 us	2.498 us	1.118 ns	146	Fail
5	t _{SU,DAT}	Data Set-up time	250.000 ns		2.499 us	2.499 us	2.499 us	722.000 ps	154	Pass
6	tsu,sto	Set-up time for STOP condition	4.000 us		2.498 us	3.450 us	4.998 us	1.987 us	21	Fail
7	tLow	Low Period of the SCL Clock	4.700 us		4.998 us	4.998 us	4.999 us	1.947 ns	480	Pass
8	t _{HIGH}	High Period of the SCL Clock	4.000 us		4.998 us	4.999 us	4.999 us	1.862 ns	480	Pass
9	t _{ICL}	Rise time of SCL signal		1.000 us	1.223 ns	1.587 ns	2.065 ns	2.050 ns	561	Pass
4.	tion			200 000	4 040	4 500	4 047	4 707	400	D
un	titled1									



8. 詳細報告

1 500 mV -3.50	2 500 mV -3.50	3 500 m -3.50		4 500 mV -3.50	H 100) µs 0 µs T	I2C Validation Stop S/R: 500 MS/s	
	Addx(7b):12.							
Overview Detail 12		I YAN MANYA MANANANA MANANANA MANANA Mananana mananana mananana mananana mananana manana manana manana manana manana manana manana manana manana man Manana manana						
Overview Detail 12 f _{SCL} t _{HD,STA} t _{SU,STA}	DAU INTERNI INA DA HERARA MARA INTERNI INTERNI INTERNI INTERNI C tholoar tsuloar	tsu,sto t _{LOW} t _{HIG}	nings frankrigen frankrigen ning and and an an shi t _{rol} t _{rol}	t _{rDA} t _{rDA}	teur t _{vo.ox} r t _{vo.}			
Overview Detail 12 f _{SCL} t _{HD,STA} t _{SU,STA} Waveform No. TimeS	DAU HYTEYL MAUDA HYTEYL YN HYTEY HANN AN L CHWYDD AL MYLL MAU C L tholoar tsulaar tamp Status	tsusto tLow tino Address D0-D7	allig providence of the second	t _{rDA} t _{DA}	t _{aur} t _{vo.ov} t _{vo.}		V _H Count Resul	
Overview Detail 12 fsc.t t _{HD,STA} t _{SU,STA} Waveform No. TimeS 1 1 49.982	RUL TIT I INNE KENT I IN RUL IN AUTO ALI INI INI INI C titodar tsudar tsudar tamp Status ns START 12	tsusto t _{Low} t _{HC} Address D0-D7 10.20.30	se troc to the test of tes	t _{-DA} t _{DA} Limit Max N 00.000 KHz 99.996	t _{BUF} t _{VD.DAT} t _{VD.} t _{BUF} t _{VD.DAT} t _{VD.} tin Mean 5 KHz 99.998 KHz	Max 100.000 KHz 3	Vin Count Result 2 Pass	t A
Overview Detail 12 fscL tit0.sth tsu.sth Waveform No. TimeS 1 1 49.982 2 1 239.35	AULINITE INALA STATU AN AULINI STATUS LINDAT LUDAT tamp Status ns START 12 9 ns START 3F	tousto t _{Low} t _{HC} Address D0-D7 10.20.30 00	Limit Hildshers All U Hall Strandstate Limit Min 0.000 Hz 0.000 Hz	t _{DA} t _{DA} Limit Max N 00.000 KHz 99.996 00.000 KHz 99.997	t _{виг} t _{vo.ov} t _{vo.} t _{виг} t _{vo.ov} t _{vo.} tin <u>Mean</u> 5 KHz 99.998 KHz 7 KHz 99.998 KHz	AGK V _E V Max 100.000 KHz 3 100.001 KHz 1	Ver Count Result 12 Pass 16 Fail	t
Overview Detail 12 fsci. t _{H0.57A} t _{50.57A} t _{50.57A} Waveform No. TimeS 1 49.962 2 1 239.35 3 1 337.48	anu 1977 / Manta 1979 (J. 400) name of a cost of All Advanced C temp Status ns START 12 9 ns START 3F 4 ns START 46	tou.sro t _{LOW} t _{HO} Address D0-D7 10 20 30 00 21 3A	Limit Min 1 0.000 Hz 11 0.000 Hz 11 0.000 Hz 11 0.000 Hz 11	t _{DA} t _{DA} Limit Max N 00.000 KHz 99.990 00.000 KHz 99.997 00.000 KHz 99.997	t _{aur} t _{vo.ov} t _{vo.} iin Mean 6 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz	ACK VL V Max 100.000 KHz 1 100.000 KHz 1 100.000 KHz 2	V _{at} Count Result 12 Pass 16 Fail 14 Pass	
Overview Detail 12 fscL t _{H0.57A} t _{50.57A} t _{50.57A} Waveform No. Times 1 1 49.982 2 1 239.35 3 1 337.48 4 2 49.982 4 9.982	AULINITY I IAADA (1997) AN IIII IIIII IIIIIIIIIIIIIIIIIIIIIIIIII	tsu.sto t _{LOW} t _{HO} Address D0-D7 10 20 30 21 3A 00	Limit Min Limit Min 0.000 Hz 11	Limit Max N 00.000 KHz 99.997 00.000 KHz 99.997 00.000 KHz 99.997 00.000 KHz 99.997	t _{BUF} t _{VD_DAT} t _{VD} t _{BUF} t _{VD_DAT} t _{VD} iin Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz 1 KHz 99.998 KHz	ACK VL V Max 100.000 KHz 1 100.001 KHz 1 100.000 KHz 1 100.000 KHz 1 100.002 KHz 1	Vin Count Result 22 Pass 16 Fail 12 Pass 16 Fail	t f
Overview Detail 12 fscL t _{HD.STA} t _{SU.STA} t _{SU.STA} Waveform No. TimeS 1 49.982 2 1 239.35 3 1 337.48 4 2 49.982 5 2 148.10	Number of the second of	tsu.sto tuow two Address D0-D7 10 20 30 21 3A 00 21 3A	Limit Min Limit Min 0.000 Hz 11	Limit Max N 00.000 KHz 99.997 00.000 KHz 99.997 00.000 KHz 99.997 00.000 KHz 99.997 00.000 KHz 99.994	t _{BUF} t _{VD.DAT} t _{VD} t _{BUF} t _{VD.DAT} t _{VD} tin Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz 8 KHz 99.998 KHz 8 KHz 99.998 KHz	Max VE	Ven Count Result 22 Pass 66 Fail 24 Pass 66 Fail 24 Pass	t
Image: Constraint of the sector of	Automatical and automatical and automatical automate automate automatical automatical automatical automatical aut	tsu.sto t_Low t_mc Address D0-D7 10 20 30 00 21 3A 00 21 3A 10 20 30 10 20 30	Limit Min Limit Min 0.000 Hz 11	t _{DA} t _{DA} M Limit Max M 00.000 KHz 99.997 00.000 KHz 99.997 00.000 KHz 99.992 00.000 KHz 99.992 00.000 KHz 99.992 00.000 KHz 99.992	t _{aur} t _{vo.Dvr} t _{vo.} t _{aur} t _{vo.Dvr} t _{vo.} tim Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 1 KHz 99.998 KHz 1 KHz 99.998 KHz 5 KHz 99.998 KHz 5 KHz 99.998 KHz	ACK VE 1 Max 1 100.000 KHz 3 100.000 KHz 1 100.000 KHz 1 100.000 KHz 2 100.000 KHz 2 100.000 KHz 2	Venter production of a production (AULT de matter) Count Result Count	
Image: Detail Iz Fsc. t _{H0,570} t _{B0,570} Waveform No. TimeS 1 49,982 2 1 239,35 3 1 337,48 4 2 49,982 5 2 148,10 6 3 49,982 7 3 239,35	Automatical and automatical and automatical automate automate automatical automatical automatical automatical aut	test.store test.store <thtest.store< th=""> test.store test.sto</thtest.store<>	Limit Min Limit Min 0.000 Hz 11	t _{DA} t _{DA} Limit Max M 00.000 KHz 99.994	taur tyopar typ taur tyopar typ tim Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz 6 KHz 99.998 KHz 5 KHz 99.998 KHz 5 KHz 99.998 KHz 5 KHz 99.998 KHz	Max	Ver Count Result 22 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 25 Fail	
Image: Detail Image: D	Automatical Particulation Automatical Particulation C	tousno tuonen t	Limit Min Lic Lic 0.000 Hz 11	Limit Max N 00.000 KHz 99.994 00.000 KHz 99.997 00.000 KHz 99.996	t _{sur} t _{vo.Dvr} t _{vo.} tin Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz 6 KHz 99.998 KHz	ACK VE	Ven Count Result 22 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 26 Fail	
Image: Detail Image: Detail <thimage: de<="" td=""><td>Automatical part of the second se</td><td>tousto tuon tuon tuon tuon tuon tuon tuon tu</td><td>Limit Min Lic Lic 0.000 Hz 11 0.000 Hz 11</td><td>Limit Max N 00.000 KHz 99.994 00.000 KHz 99.997 00.000 KHz 99.996 00.000 KHz 99.997 00.000 KHz 99.996 00.000 KHz 99.997 00.000 KHz 90.0000 KHz</td><td>t_{sur} t_{vo.Dar} t_{vo.} tin Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz 8 KHz 99.998 KHz</td><td>ACK VE VE</td><td>Ven Count Result 22 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 26 Fail 26 Fail</td><td></td></thimage:>	Automatical part of the second se	tousto tuon tuon tuon tuon tuon tuon tuon tu	Limit Min Lic Lic 0.000 Hz 11	Limit Max N 00.000 KHz 99.994 00.000 KHz 99.997 00.000 KHz 99.996 00.000 KHz 99.997 00.000 KHz 99.996 00.000 KHz 99.997 00.000 KHz 90.0000 KHz	t _{sur} t _{vo.Dar} t _{vo.} tin Mean 5 KHz 99.998 KHz 7 KHz 99.998 KHz 7 KHz 99.998 KHz 8 KHz 99.998 KHz	ACK VE	Ven Count Result 22 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 24 Pass 16 Fail 26 Fail 26 Fail	

9. 波形和參考點

1 -3.50 mV		2 500 mV -3.50		3 500 m ^v -3.50		4 50 -3.	0 m 50	V F	2 µs -394	з 1.966 µs Т	I2C Validation Stop S/R: 500 MS/s			Free Run	ſ
	-													Analysis	St
	• • • • • • • • • • • • • • • • • • •					Addr(7b):3F				÷ 2		······································	Stop conditi Stop w 1000 Stop w 0	ons hen acquired) ↓ tim hen Result Fail > ¢ tim	e(s) e(s)
							6	Detail							×
				ە, انكىنىدىنىمە			fs	CL							
Overview De	etali i2C														
for two	1		- t	t			F	Waveform No.		Time Stamp	Status	Ad	ddress	D0-D7	tio
f _{SCL} t _{HD,STA}	t _{SU,STA} t	HD,DAT t _{SU,D} /	r t _{su,sto}	t _{LOW} t _{HIG}	H t _{rCL} t _r	ICL t _{rDA}	E	Waveform No. 1 Time	1	Time Stamp 239.359 ns	Status START	A	ddress 3F Result	D0-D7 00	tio Fa
f _{SCL} t _{HD,STA} Waveform Ne 1 1	t _{SU,STA} t o. TimeStamp 49.982 ns	HD,DAT t _{SU,DA} Status START	r t _{su,sto} Address	t _{LOW} t _{HIG} D0-D7 10 20 30	H t _{rCL} tr Limit Min 0.000 Hz	ICL LIMIT MAX		Waveform No. 1 [489.967 µs, 499.967	us)	Time Stamp 239.359 ns ∆ Time 10.000 µs	Status START Volt (990 mV, 990 mV)	∆ Volt	ddress 3F Result Fail	D0-D7	tio Fa
f _{SCL} t _{HD,STA} Waveform No. 1 1 2 1	t _{SU,STA} t TimeStamp 49.982 ns 239.359 ns	HD.DAT tSU.DA Status START START	r t _{SU,STO} Address 12 3F	tLow tHIG D0-D7 10 20 30 00	H t _{rCL} t _f Limit Min 0.000 Hz 0.000 Hz	ICL t _{-DA}	1	Time (489.967 μs, 499.967 (499.967 μs, 509.968	hs)	Time Stamp 239.359 ns Δ Time 10.000 μs 10.000 μs	Status START Voit (990 mV, 990 mV) (990 mV, 990 mV)	△ Volt 0 V 0 V	ddress 3F Result Fail Pass	00-D7	tio Fa
fscL t _{HD,STA} Waveform No 1 1 1 2 1 3 1	t _{SU,STA} t t <u>SU,STA</u> t 49.982 ns 239.359 ns 337.484 ns	START START	r t _{su,sto} Address 12 3F 46	t _{LOW} t _{HIG} D0-D7 10 20 30 00 21 3A	H t _{rcL} t _r Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	CL t _{rDA} Limit Max 100.000 KH 100.000 KH 100.000 KH	1	Waveform No. 1 Time (489.967 μs, 499.967 (499.967 μs, 509.968 (509.968 μs, 519.967	hs) hs)	Time Stamp 239.359 ns ∆ Time 10.000 µs 10.000 µs 10.000 µs	Status START Voit (990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV)	△ Volt 0 V 0 V 0 V 0 V	ddress 3F Result Fail Pass Fail	00-D7	tic Fa
fscl t _{HD.STA} Waveform Nr 1 1 2 1 3 1 4 2	t _{SU,STA} t 5. TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns	START START START	т t _{SU,STO} Address 12 3F 46 3F	t _{LOW} t _{HIG} D0-D7 10 20 30 00 21 3A 00	H t _{rcL} t ₄ Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	Limit Max 100.000 KF 100.000 KF 100.000 KF 100.000 KF	1	Waveform No. 1 1 Time (489.967 µs, 499.967 (499.967 µs, 509.968 (509.968 µs, 519.967 (519.967 µs, 529.968	hs) hs)	Time Stamp 239.359 ns Δ Time 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs	Status START Volt (990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV) (990 mV, 990 mV)	△ Volt 0 V 0 V 0 V 0 V	ddress 3F Result Fail Pass Fail Pass	00 00	tic Fa
fscl t _{HD.STA} Waveform Net 1 1 1 2 1 3 1 4 2 5 2	tsu.sta t tsu.sta t 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns	ND.DAT LSU.DAT Status START START START START START	r t _{SU,STO} Address 12 3F 46 3F 46	tLow tHis D0-D7 10 20 30 00 21 3A 00 21 3A	H t _{CL} t ₄ Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	Limit Max Limit Max 100.000 KH 100.000 KH 100.000 KH 100.000 KH		Waveform No. 1 Time (489.967 μs, 499.967 (499.967 μs, 509.968 (509.968 μs, 519.967 (519.967 μs, 529.968 (529.968 μs, 539.968	hs) hs)	Time Stamp 239.359 ns Δ Time 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs 10.000 μs	Status START Yolt (990 mV, 990 mV)	△ Volt 0 V 0 V 0 V 0 V 0 V	ddress 3F Result Fail Pass Fail Pass Pass	D0-D7 00	tio Fa
fscl. t _{HD,STA} Waveform Nr 1 1 1 2 1 3 1 4 2 5 2 6 3	tsu.srx t 0. TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns 49.982 ns 148.108 ns 49.982 ns 148.208 ns	START START START START START START START START	r t _{SU,STO} Address 12 3F 46 3F 46 12	tLow tring D0-D7 10 20 30 00 21 3A 10 20 30	H t _{rCL} t _d Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	Limit Max 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH	1 2 3 4 5 6	Waveform No. 1 Time (489.967 μs. 499.967 (499.967 μs. 509.968 (509.968 μs. 519.967 (519.967 μs. 529.968 (529.968 μs. 539.968 (529.968 μs. 539.968 (539.968 μs. 549.968	µs) µs) µs) µs)	Time Stamp 239.359 ns Δ Time 10.000 μs	Status START Yoli (990 mV, 990 mV)	Ac △ Volt 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨ 0 ∨	ddress 3F Result Fail Pass Pass Pass Pass	00-D7 00	tio
Fact. LUD.STA Waveform N 1 1 1 2 1 3 1 4 2 5 2 6 3 7 3	tsu.sta t o. TimeStamp 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 239.359 ns 337.484 ns	START START START START START START START START START	r t _{SU,STO} Address 12 3F 46 3F 46 12 3F 46 3F 3F	tLOW tHIG D0-D7 10 20 30 00 21 3A 00 21 3A 10 20 30 00 00	trcL tr Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	Limit Mas Limit Mas 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH	1 1 2 3 4 5 6	Waveform No. 1 1 1 (489.967 μs. 499.967 (499.967 μs. 509.968 (509.968 μs. 519.967 (519.967 μs. 529.968 (529.968 μs. 539.968 (539.968 μs. 549.968 (539.968 μs. 549.968 (549.968 μs. 559.968	µs) µs) µs) µs) µs)	Time Stamp 239.359 ns Δ Time 10.000 μs	Status START Yoli (990 mV, 990 mV)	△ ¥olt 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V	ddress 3F Result Fail Pass Fail Pass Pass Pass Fail	00-D7 00	Fa
Fact Usperiod Waveform N 1 2 3 4 5 6 3 7 3 8	tsusta t 49.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 148.108 ns 49.982 ns 337.484 ns 337.484 ns	NDDAT LSUDA Status START START START START START START START START	r t _{su.sto} Address 12 3F 46 3F 46 12 3F 46 12 3F 46 46 46 46 46 46 46 46 46 46	tLOW tHER D0-D7 10 20 30 00 21 3A 00 21 3A 10 20 30 00 21 3A 10 20 30 00 21 3A	t,cc. t, Limit Min 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz 0.000 Hz	CL LOA Limit Maa 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH 100.000 KH	1 1 2 3 4 5 7 8	Waveform No. 1 1 1 (489 967 μs. 499 967 (499 967 μs. 509 968 (509 968 μs. 519 967 (519 967 μs. 529 968 (529 968 μs. 539 968 (539 968 μs. 549 968 (549 962 μs. 559 968 (549 968 μs. 569 968	нs) (нs) (нs) (нs) (нs) (нs) (нs) (нs)	Time Stamp 239.359 ns Δ Time 10.000 μs	Status START Yoli (990 mV, 990 mV)	Act Act	ddress 3F Result Fail Pass Pass Pass Pass Fail Fail Pass	D0-D7 00	tio
Fact Uspace Waveform N 1 2 3 4 2 5 2 6 3 7 8 3	tsusta t tsusta t d9.982 ns 239.359 ns 337.484 ns 49.982 ns 148.108 ns 49.982 ns 148.108 ns 49.982 ns 337.484 ns 337.484 ns	START START START START START START START START START START START	tau.sto Address 12 3F 46 3F 46 12 3F 46 12 3F 46 12 3F 46 12	t.cow tenso D0-D7 10 20 30 00 21 3A 10 20 30 00 21 3A 10 20 30 00 21 3A 10 20 30 00	trol tr Limit Min 0.000 Hz 0.000 Hz 0.000 Hz	CL L _{0A} Limit Max 100.000 Kł 100.000 Kł 100.000 Kł 100.000 Kł 100.000 Kł 100.000 Kł 100.000 Kł 100.000 Kł 100.000 Kł		Waveform No. 1 1 (489 967 μs. 499 967 (499 967 μs. 509 968 (509 968 μs. 519 967 (519 967 μs. 529 968 (529 968 μs. 539 968 (539 968 μs. 549 968 (549 967 μs. 569 968 (559 968 μs. 569 968 (559 968 μs. 569 968 (579 968 μs. 569 968	445) 445) 445) 445) 445) 445) 445) 445)	Time Stamp 239.359 ns Δ Time 10.000 μs 10.000 μs	Status START Yoli (990 mV, 990 mV) (990 mV, 990 mV)	Ad △ Yoit 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V 0 V	ddress 3F Result Fail Pass Fail Pass Pass Fail Pass Fail	D0-D7 00	tio





Electrical Validation Report

Test Instrument Model	MSO3124V		
Test Instruments Serial Number	24554		
Test Date	04-17-2023 14:46:14		
S/W Version	1.0.25		
Protocol	12C		
/*************************************	······································		

Overview Results:

Total: 17 Pass: 9 Fail: 6

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	f _{SCL}	SCL clock frequency	0.000 Hz	100.000 KHz	387.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%	×Fail
2	t _{HD,STA}	Hold time(repeated) START condition	4.000 us		1.538 us	1.538 us	1.539 us	427.000 ps	20	-61.6%		×Fail
3	t _{su,sta}	Set-up time for a repeated START condition	4.700 us		2.013 us	2.014 us	2.015 us	579.000 ps	10	-57.2%		×Fail
4	t _{HD,DAT}	Data hold time	5.000 us		94.249 ns	247.342 ns	1.026 us	4.244 us	1575	-98.1%		×Fail
5	t _{SU,DAT}	Data Set-up time	250.000 ns		472.837 ns	1.187 us	1.443 us	5.255 us	1767	18.7%		✓Pass
6	t _{SU,STO}	Set-up time for STOP condition							0			
7	t _{LOW}	Low Period of the SCL Clock	4.700 us		1.539 us	1.541 us	1.543 us	9.208 ns	2670	-67.3%		×Fail
8	t _{HIGH}	High Period of the SCL Clock	4.000 us		977.699 ns	979.666 ns	984.826 ns	20.914 ns	3040	-75.6%		×Fail
9	t _{rCL}	Rise time of SCL signal		1.000 us	45.022 ns	48.118 ns	49.835 ns	14.531 ns	3430		0.5%	✓Pass
10	t _{fCL}	Fall time of SCL signal		300.000 ns	9.888 ns	10.237 ns	10.583 ns	1.448 ns	3430		0.2%	✓Pass
11	t _{rDA}	Rise time of SDA signal		1.000 us	37.719 ns	39.529 ns	41.848 ns	5.148 ns	927		0.4%	✓Pass
12	t _{fDA}	Fall time of SDA signal		300.000 ns	4.616 ns	6.893 ns	9.828 ns	24.035 ns	947		1.8%	✓Pass
13	t _{BUF}	Bus free time between a STOP and START condition							0			
14	t _{VD,DAT}	<u>Data valid time</u>		3.450 us	98.898 ns	270.164 ns	1.067 us	4.200 us	1585		28.9%	✓Pass
15	t _{VD,ACK}	Data valid acknowledge time		3.450 us	141.017 ns	730.257 ns	1.067 us	1.344 us	91		28.0%	✓Pass
16	VIL	Low-level input voltage	-500.000 mV	990.000 mV	-105.670 mV	27.063 mV	104.081 mV	760.863 mV	4367	26.5%	40.5%	✓Pass
17	VIH	<u>High-level input voltage</u>	2.310 V	3.800 V	3.225 V	3.267 V	3.417 V	1.250 V	4367	61.4%	74.3%	✓Pass

f_{SCL} - Test Result: Fail Description: SCL clock frequency

Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	n Count	t Margin Mi	n Margin Max	1					
0.000 Hz	100.000 KHz 38	87.586 KHz	387.683 KHz	387.769 KHz	437.000 Hz	2670	387.6%	387.8%						
				Histogr	am									
Occi	urance (%), Total 267					V	alue Range	Occurance C	ount					
100						387.586	kHz ~ 387.604	dHz 9						
90 -						387.604	kHz ~ 387.623	tHz 23						
80 - 70 -						387.623	kHz ~ 387.641	tHz 84						
60 - 50 -						387.641	kHz ~ 387.659	Hz 395						
40 -						387.659	kHz ~ 387.677	Hz 539						
30 - 20 -		14.8	23.7 24.8			387.677	kHz ~ 387.696	Hz 632						
10 - _{0.}	3 0.9 3.1			8.0	0.7 Test Value	387.696	kHz ~ 387.714	(Hz 663						
387.586 Ki	Hz				387.769 KHz	387.714	kHz ~ 387.732	Hz 213						
Test Value			387.586 KHz	(387.6%) 387	7.769 KHz (387.8%)	387.732	kHz ~ 387.751	dHz 94						
Limit	0.000 Hz				100.000 KHz	387.751	kHz ~ 387.769	tHz 18						
Min				Detail Re	port Row: 12, Test	t Index	: 197 Ma	x				Detail Rep	ort Row: 10, Te	st Index: 82
1 500 m -3.50	V 2 500 mV -3.50	3 500 mV -3.50	4 500 mV -3.50	H 400 ns -730.2 µs	I2C Validation Stop S/R: 500 N	IS/s	1	500 mV 2 50 -3.50 2 -3	0 mV .50	3 500 mV -3.50	500 mV -3.50	400 ns -345.866 µs	T I2C Validation Stop S/R: 500 N	1S/s
						-								
				1								1		
							•							÷
	197				197				82		1-1-1-			
120			62				120				7E			
											1			



12S 電氣特性驗證解決方案

■ 簡介:

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器執行 I2S 電氣特性驗證,以確保 I2S 符合既定規格。在經過長時間燒機測試後,可以確認所測試的訊號電氣特性符合規範。

I²S(Inter-IC Sound)是一種標準的序列匯流排介面,用於連接數位音訊裝置,例如音訊編碼器、數位類比轉換器(DAC)與類比數位轉換器(ADC)。它常見於嵌入式系統、音訊處理器與高品質音訊設備中。

1²S 是一種結構簡單但功能強大的介面,可在裝置之間以高精度、低延遲地傳送數位音訊 資料。



■ 12S 電氣特性驗證設定

1. 一般設定:設定匯流排配置,包括 I2S 模式類型(I2S、Left Justified、

PCM、TDM)、通道設定、工作電壓與資料速率。

Settings							Import	Export
General Control	Channel	Settings						
★Trigger★Validation	Mode: SCK: WS: SD:	I2S DSO Channel 1 DSO Channel 2 DSO Channel 3	Probe Settings: Probe Settings: Probe Settings:	x10 • x10 • x10 •	x10	3- 3-		
	Working Data Ri	g Voltage(V _{DD}): 3.30 V ate 2.50 MHz	•					

2. 解碼設定:設定 I2S 資料格式。位元順序可選擇 MSB First 或 LSB First。

資料位元數可設定為 1 到 32 位元之間。

Settings					Import	Export
✓General →Decode	Data Format					
 Trigger Validation 	Bit Order Data Bits	MSB First				
Default					Previous	Next



獨發設定:設定使用者需要觸發的資料模式。資料格式已在前一頁的解碼 設定中設定完成,其餘設定僅與資料樣式相關。此處共提供 6 種觸發方

式:Data Match, Rising, Falling, Glitch, Mute, and Clip。

Settinas						Import	Export
 ✓General ✓Decode 	Data						
 Trigger Validation 	Method Channel Pattern	Data Match					
	Duration	1 frame(s)					

4. 驗證參數設定

ode	 Customized EV Para 	meter:		
ger dation	Frequency			
	Name	Description	Min	Max
	1 ✓ f _{SCK} SCK Free	juency	2.25 MHz	2.75 MHz
	Time			
	Name	Description	Min	Max
	1 🗸 t _{HC} SCK	High Period	140 ns	x
	2 🗸 t _{LC} SCK	High Period	140 ns	x
	3 🗸 t _R SCK	Rise Time	X	60 ns
	4 ✔ t _F SCK	Fall Time	X	60 ns
	5 V t _{d,SCKWS} SCK	-WS Delay Time	x	320 ns
	6 V t _{d,SCKSD} SCK	-Data Delay Time	x	320 ns
	7 V tdutySCK SCK	Duty Cycle	x	х
	8 🗸 t _{s,WS} WS	Setup Time	x	80 ns
	9 ✔ t _{h,WS} WS	Hold Time	0 ns	x
	10 ✓ t _{dutyWS} WS	Duty Cycle	X	x
	11 ✔ t _{ssp} Data	Setup Time	X	80 ns



此部分提供三張特性參數表,包含:

- 頻率
- 時序參數
- 電壓要求

預設值參考自 12S 規範 Rev3.0。下方列出所有支援的驗證參數符號與說明:

• I2S Frequency Requirements

Symbol	Electrical Parameter
f _{SCK}	SCK Clock Frequency

• I2S Timing Requirements

Symbol	Electrical Parameter
t _{HC}	SCK High Period
t _{LC}	SCK Low Period
t _R	SCK Rise Time
t _F	SCK Fall Time
t _{d,SCKWS}	SCK-WS Delay Time
t _{duty,SCK}	SCK Duty Cycle
t _{s,WS}	WS Setup Time
t _{h,WS}	WS Hold Time
t _{duty,WS}	WS Duty Cycle
t _{s,SD}	Data Setup Time
t _{h,SD}	Data Hold Time

• I2S Voltage Requirements

Symbol	Electrical Parameter
VL	Low-Level Voltage
V _H	High-level Voltage



5. 電氣特性驗證 軟體畫面

1 2 V +1.53			2	2 V -0.97				3 2 V -3.50			H 20 µs -80 µs	T I2S Validation Stop S/R: 250 MS/s	
				n hh hh Liùi	hin i h	1))) () () () () () () () () () () () () () () () (11-1433 (m. 1. 16-14) (m. 1. 16-14) 11-143 (m. 17-14) (m. 17-14) 11-144 (m. 17-14) (m. 17-14)	n popular popular popular kao popular popular popular			
Overview 12S Timestamp													
	DO	D1	D2	D3	D4	D5	D6	D7	Information				1
1 0 s	D0	D1	D2	D3	D4	D5	D6	D7	Information Sample Rate: 1.25 MHz - 16 bit				
1 0 s 2 0 s	D0	D1	D2	D3	D4	D5	D6	D7	Information Sample Rate: 1.25 MHz - 16 bit IDLE				
1 0 s 2 0 s 3 3.6 µs	D0 00 00 00 00 00 00 00 00 00 00 00 00 0	D1	D2	D3	D4	D5 R:E000	D6	D7 R:0000	Information Sample Rate: 1.25 MHz - 16 bit IDLE				*
1 0 s 2 0 s 3 3.6 μs 4 8.6 μs	D0 10 10 10 10 10 10 10 10 10 10 10 10 10	D1	D2 E000 F	D3 R:8000 R:8000	D4 L:8000 L:C000	D5 R:E000 R:8000	D6 L:0000 L:8000	D7 R:0000 R:E000	Information Sample Rate: 1.25 MHz - 16 bit IDLE				
1 0 s 2 0 s 3 3.6 μs 4 8.6 μs 5 14.2 μs	D0 E E E E E E E E E E E E E E E E E E E	D1	D2 E000 F 0000 F	D3 R:8000 R:8000 R:0000	D4 L:8000 L:C000 L:1C00	D5 R:E000 R:8000 R:C000	D6 L:0000 L:8000 L:E000	D7 R:0000 R:E000 R:0000	Information Sample Rate: 1.25 MHz - 16 bit IDLE				•
1 0 s 2 0 s 3 3.6 μs 4 8.6 μs 5 14.2 μs 6 21.4 μs	D0 D	D1 22 20000 L:0 2:0000 L:0 2:0000 L:0 2:0000 L:0	D2 E000 F 0000 F 0000 F 0000 F	D3 R:8000 R:8000 R:0000 R:C000	D4 L:8000 L:C000 L:1C00 L:E000	D5 R:E000 R:8000 R:C000 R:0000	D6 L:0000 L:8000 L:E000 L:0000	D7 R:0000 R:E000 R:0000 R:0000	Information Sample Rate. 1.25 MHz - 16 bit IDLE				
1 0 s 2 0 s 3 3.6 µs 4 8.6 µs 5 14.2 µs 6 21.4 µs 7 27.8 µs	D0 L:0000 R L:0000 R L:0000 R L:0000 R L:0000 R	D1 20000 L:0 R:0000 L:0 R:0000 L:0 R:0000 L:0 R:1000 L:0 R:0000 L:0	D2 E000 F 00000 F 00000 F C0000 F E000 F	D3 R:8000 R:0000 R:0000 R:C000	D4 L:8000 L:C000 L:1C00 L:E000 L:C000	D5 R:E000 R:8000 R:C000 R:0000 R:8000	D6 L:0000 L:8000 L:E000 L:0000 L:0000	D7 R:0000 R:E000 R:0000 R:0000 R:0000	Information Sample Rate: 1.25 MHz - 16 bit IDLE				*
1 0 s 2 0 s 3 3.6 µs 4 8.6 µs 5 14.2 µs 6 21.4 µs 7 27.8 µs 8 34.2 µs 2 0 s	D0 L:0000 R L:0000 R L:0000 R L:0000 R L:0000 R L:0000 R	D1 2:0000 L:0 2:0000 L:0 2:0000 L:0 2:1000 L:0 2:1000 L:0 2:0000 L:0 2:0000 L:0	D2 F E000 F 0000 F C000 F E000 F E000 F E000 F	D3 R:8000 R:8000 R:0000 R:C000 R:C000 R:C000 R:8000	D4 L:8000 L:C000 L:1C00 L:E000 L:C000 L:C000	D5 R:E000 R:8000 R:0000 R:0000 R:0000 R:0000	D6 L:0000 L:8000 L:E000 L:0000 L:0000 L:C000	D7 R:0000 R:E000 R:0000 R:0000 R:0000 R:0000 R:8000	Information Sample Rate: 1.25 MHz - 16 bit IDLE				
1 0 s 2 0 s 3 3.6 μs 4 8.6 μs 5 14.2 μs 6 21.4 μs 7 27.8 μs 8 34.2 μs 9 39.8 μs 50 4.6 μs	D0 L:0000 R L:0000 R L:0000 R L:0000 R L:0000 R L:0000 R L:0000 R	D1	D2 50000 F 60000 F 60000 F 60000 F 60000 F 60000 F 60000 F 60000 F	D3 R:8000 R:0000 R:0000 R:C000 R:C000 R:0000 R:0000 R:0000 R:0000	D4 L:8000 L:C000 L:1C00 L:C000 L:C000 L:C000 L:C000	D5 R:E000 R:6000 R:0000 R:0000 R:8000 R:6000 R:6000 R:6000	D6 L:0000 L:8000 L:0000 L:0000 L:0000 L:0000 L:0000	D7 R:0000 R:E000 R:0000 R:0000 R:0000 R:8000 R:8000 R:8000	Information Sample Rate: 1.25 MHz - 16 bit IDLE				

6. 控制面板



A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止

B. 資訊:選擇查看波形

C. 儲存檔案:

儲存為 HTML 格式 儲存為 .MOW (Acute軟體專用格式)



7. 概覽報告



8. 詳細報告

1	2 V +1.53			2 2 V -0.97				3 2 V -3.50					H 2	:0µs 80µs	T I2 S	S Validat top <u>S/R</u>	ion : 250 MS/s	5	
1																			
2								╷╎╷╷╷											
12S 3	R L R	RE R De F							20140 (1114) 			 , ₁₁₁₁		L R					
Over	view Detail	125	1. T																
L _R	Vaveform No	TimeStamp	s t _{hws} Data	Limit Min	Limit Max	Min	Mean	Max	Count	Result									
1	1-1	300.000 ns	R: 8000	-	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass									1
2	1-2	350.000 ns	L: 8000		60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass									
3	1-3	450.000 ns	R: 8000		60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass									
4	1-4	550.000 ns	L: 8000		60.000 ns	1.707 ns	1.707 ns	1.707 ns	1	Pass									
5	1-5	650.000 ns	R: 8000	-	60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass									
6	1-6	750.000 ns	L: 0000		60.000 ns	1.719 ns	1.727 ns	1.743 ns	4	Pass									
7	1-7	1.150 us	R: 0000		60.000 ns	1.743 ns	1.743 ns	1.743 ns	1	Pass									
8	1-8	1.250 us	L: 0000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass									1
9	1-9	1.350 us	R: 0000		60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass									
10	1-10	1.450 us	L: 0000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass									
11	1-11	1.550 us	R: 8000		60.000 ns	1.719 ns	1.719 ns	1.719 ns	1	Pass									
12	1-12	1.650 us	L: 8000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	1	Pass									
13	1-13	1.750 us	R: C000		60.000 ns	1.730 ns	1.730 ns	1.730 ns	2	Pass									



9. 波形和參考點

1	2 V +1.53			2 2 V -0.97				3	2 V 3.50							H 40 ns +17.104 μs	T I2S Valio	lation /R: 250 MS/s	
1					ſ														4
2			·····		•·····••••••••••••••••••••••••••••••••			00	······	······•						•	¢		e
125							K.80	00							1		1:0000		
3									🔘 Detail								×		
									t _{h,SD}								_		
Over	view Detail	128						-	Wave	eform No. 1-6	Time St 750.00	amp) ns	Data 1 · 0000	Lim	it Min 00 ps	Limit Ma	×		
t _R	t _{d,SCKWS} t Naveform No	TimeStamp	s t _{h,ws} Data	t _{s,SD} t _{h,SD}	Limit Max	Min	Mean	1		Time	۵Ti	ne	Yolt	∆Volt	Result				-
1	1-1	300.000 ns	R: 8000	0.000 ps					1 (2.799	µs, 2.998 µs)	198.51	ins (2.3	11 V, 2.31 V)	0 V	Pass				
2	1-2	350.000 ns	L: 8000	0.000 ps															
3	1-3	450.000 ns	R: 8000	0.000 ps															
4	1-4	550.000 ns	L: 8000	0.000 ps															
5	1-5	650.000 ns	R: 8000	0.000 ps															
6	1-6	750.000 ns	L: 0000	0.000 ps		198.516 ns	198.516 ns	19											
7	1-7	1.150 us	R: 0000	0.000 ps															
8	1-8	1.250 us	L: 0000	0.000 ps															
9	1-9	1.350 us	R: 0000	0.000 ps															
10	1-10	1.450 us	L: 0000	0.000 ps						_						×	Close		
11	1-11	1.550 us	R: 8000	0.000 ps		198.369 ns	198.369 ns	198	.369 ns	1	Pass								
12	1-12	1.650 us	L: 8000	0.000 ps															
13	1-13	1.750 us	R: C000	0.000 ps															_



10. Html 報告



Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240021
Test Date	12-09-2024 13:34:37
S/W Version	1.8.62
Protocol	12S

Overview Results:

t_R - Test Result: Pass Description: SCK Rise Time

Total:	7
Pass:	5
Fail:	2

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	t _R	SCK Rise Time		60.000 ns	1.639 ns	2.062 ns	2.990 ns	442.000 ps	2994		-95.0%	✓Pass
2	t _{d,SCKWS}	SCK-WS Delay Time		320.000 ns	201.556 ns	202.420 ns	203.654 ns	602.000 ps	1390		-36.4%	✓Pass
3	t _{d,SCKSD}	SCK-Data Delay Time		320.000 ns	201.759 ns	202.758 ns	203.957 ns	713.000 ps	375		-36.3%	✓Pass
4	t _{s,WS}	WS Setup Time		80.000 ns	196.354 ns	197.580 ns	198.443 ns	599.000 ps	1377		148.1%	≍Fail
5	t _{h,WS}	WS Hold Time	0.000 ps		197.274 ns	198.316 ns	199.035 ns	269.000 ps	1390			✓Pass
6	t _{s,SD}	<u>Data Setup Time</u>		80.000 ns	196.039 ns	197.265 ns	198.283 ns	708.000 ps	375		147.9%	≍Fail
7	t _{h,SD}	Data Hold Time	0.000 ps		197.737 ns	198.588 ns	199.651 ns	295.000 ps	375			✓Pass

Limit Min Limit Max Min Mean Max Standard Deviation Count Margin Min Margin Max 60.000 ns 1.639 ns 2.062 ns 2.990 ns 442.000 ps Histogram Value Range Oc 1.639 ns ~ 1.774 ns | 1283 100 90 80 70 60 50 40 30 1.774 ns ~ 1.909 ns 578 1.909 ns ~ 2.044 ns 439 2.044 ns ~ 2.179 ns 210 2.179 ns ~ 2.314 ns 84 2.314 ns ~ 2.450 ns 80 2.450 ns ~ 2.585 ns 112 2.585 ns ~ 2.720 ns 147 2.720 ns ~ 2.855 ns 167 60.000 ns 2.855 ns ~ 2.990 ns 393 Detail Report Row: 1337, Test Index: 1 Max Detail Report Row: 765, Test Index: 3 Min 2 V +1.53 H 1 ns -59.196 µs 1 ns -134.4 µs 2 V .0 97 1 1 3



MIPI I3C 電氣特性驗證解決方案

■ 簡介:

File / Settings Di	isplay Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	en File					

MIPI I3C 向下相容許多傳統 I²C 裝置,但同時 I3C 裝置還支援更高速傳輸速率(SCL 頻率 可達 12.5 MHz) 與全新的通訊模式。MIPI I3C 工作模式包含 Single Data Rate (SDR) Mode, High Data Rate (HDR) Mode. HDR Mode 進一步細分為 Dual Data Rate (HDR-DDR) Mode, Ternary Symbol Legacy Mode (HDR-TTL) Mode, Ternary Symbol Pure-bus (HDR-TSP) Mode, Bulk Transport (HDR-BT) Mode.

MIPI I3C 電氣特性驗證提供多項符合 MIPI I3C 規格的電氣測量項目(目前支援 MIPI I3C 版本 1.1.1)。



MIPI I3C Electrical Validation Settings:

1. 一般設定:設定通道來源、工作電壓與傳輸速率。

Sottings	Imp	ort	Export
→General	Channel Settings		
 Trigger Validation 	SCL: DSO Channel 1 Probe Settings: x10 x10 SDA: DSO Channel 2 Probe Settings: x10 x10		
	Working Voltage(V _{DD}): 1.80 V		
	 SDR: Single Data Rate Mode (Max: 12.5 Mbps) HDR-DDR: HDR Double Data Rate Mode (Max: 25 Mbps) 		
	 HDR-TSL: Tenary Symbol Legacy-inclusive-bus Mode (Max: 27.5 Mbps) HDR-TSP: HDR Tenary Symbol for Pure-bus Mode (Max: 39.5 Mbps) 		
	 HDR-BT: HDR Bulk Transport Mode Customized Speed 400 Kbps \$\$ 		
	Bus Configuration		
	 Pure Bus: Only I3C devices are presented on the I3C Bus Mixed Bus: At least one I2C Legacy Device is presented on the I3C Bus 		
	Communicating with I2C Legacy Device		
	 Fast Mode (400 Kbps) Fast Mode+ (1 Mbps) 		
Default			Next

在此部分中,所選的速度模式會影響驗證所需的取樣率,同時也會影響後續「驗證設定」 部分中的時序規格表。例如,在 HDR-TSL 與 HDR-TSP 模式下,將額外顯示專屬的時序規 格。

13 ✔ t _{EDGE}	Edge-to-Edge Period	32 ns	х
14 ✔ t _{skew}	Allow Difference Between Signals for 'Simultaneous' Change	x	12.8 ns
15 ✔ t _{EYE}	Stable Condition Between Signals	12 ns	х
16 ✓ t _{SYMBOL}	Time Between Successive Symbols	32 ns	х
17 ✓ t _{сьоск}	Symbol Clock	77.5 ns	x

此外,在「Bus Configuration」中需指定匯流排上連接的裝置類型:

- 純 I3C 匯流排 (Pure-Bus): 不需要 I²C 時序規格。
- 混合匯流排(Mixed Bus): 需加入 I²C 相容裝置的時序規格,預設值採用 Fast
 Mode(Fm)或 Fast Mode+(Fm+)設定,與 I²C 驗證設定相同。



2. 解碼設定

ttings		Import	Export
General	Startup		
Trigger Validation	 Startup in I2C mode PEC Enabled Startup in HDR-DDR mode 		

3. 觸發設定

Settings		Import Export
✓General✓Decode	Trigger on	
 Trigger Xalidation 	Address: XXh Common Command Code (CCC): XXh, Any	-

若需要分析特定裝置位址,可設定特定位置為觸發條件。如圖中 "XX" 表示「任意」的位元,將會觸發所有位址。此外亦支援針對常用命令碼(CCC)的觸發,可透過廣播位址 7'h7E 指定。



4. 驗證參數設定

eidi				
ode	Customized E	V Parameter:		
ger dation	Freque	ncy		
atton	Name	Description	Min	Max
	1 ✔ f _{SCL} 5	CL Clock Frequency when communicating with I2C Legacy Devices	0 MHz	0.4 MHz
	2 ✔ f _{SCL_PP} S	CL Clock Frequency	0.01 MHz	12.9 MHz
	Time (V	Vhen Communicating With I2C Legacy Devices)		
	Name	Description	Min	Max
	1 ✔ t _{su_st/}	Setup Time for a Repeated START	600 ns	X
		Used Time for a (Demonted) CTADT	600 pc	x
	2 ✓ t _{HD_ST}	Inoid Time for a (Repeated) START	000 113	
	2 ✓ t _{HD_ST/} 3 ✓ t _{LOW}	SCL Clock Low Period	1300 ns	X
	2 ✓ t _{HD_ST/} 3 ✓ t _{LOW} 4 ✓ t _{DIG_L}	SCL Clock Low Period SCL Clock Low Period SCL Clock Low Period as seen at the receiver	1300 ns 1320 ns	X X
	2 V t _{HD_ST} 3 V t _{LOW} 4 V t _{DIG_L} 5 V t _{HIGH}	SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period	1300 ns 1320 ns 600 ns	X X X X
	2 ✓ t _{HD_ST/} 3 ✓ t _{LOW} 4 ✓ t _{DIG_L} 5 ✓ t _{HIGH} 6 ✓ t _{DIG_H}	SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period SCL Clock High Period as seen at the receiver	1300 ns 1320 ns 600 ns 606.55 ns	x x x x x x
	2 ✓ t _{H0_577} 3 ✓ t _{L0W} 4 ✓ t _{DIG_L} 5 ✓ t _{HIGH} 6 ✓ t _{DIG_H} 7 ✓ t _{SU_DA}	SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver Data Setup Time	000 hs 1300 ns 1320 ns 600 ns 606.55 ns 100 ns	x x x x x x x x x
	2	SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver Data Setup Time	1300 ns 1320 ns 600 ns 600 ns 606.55 ns 100 ns X	x x x x x x x x x x x
	2 ✓ t _{H0,577} 3 ✓ t _{L0W} 4 ✓ t _{DIG_L} 5 ✓ t _{HIGH} 6 ✓ t _{DIG_M} 7 ✓ t _{SU_DM} 8 ✓ t _{H0_DM} 9 ✓ t _{CL}	SCL Clock Low Period SCL Clock Low Period as seen at the receiver SCL Clock High Period SCL Clock High Period as seen at the receiver Data Setup Time Data Hold Time SCL Signal Rise Time	300 ns 1300 ns 1320 ns 600 ns 606.55 ns 100 ns X 20 ns	X X X X X X X X 300 ns

本部分共包含五種參數表:

- Frequency
- I3C timing requirements when communicating with I²C Legacy Devices
- I3C Open Drain timing parameters
- I3C Push-Pull timing parameters
- I3C I/O stage characteristics voltage requirements

若為純 I3C 匯流排,則不會顯示與 I²C 裝置相關的時序表,也不會顯示 fscl 頻率參數。



MIPI I3C Frequency Requirements

Symbol	Electrical Parameter
f _{SCL}	SCL Clock Frequency when communicating with I ² C Legacy Devices ¹
t _{SCL_PP}	SCL Clock Frequency
$t_{\text{BT}_{\text{FREQ}}}$	HDR-BT SCL Clock Frequency

MIPI I3C Timing Requirements When Communicating With I²C Legacy Devices¹

Symbol	Electrical Parameter
t _{su_sta}	Setup Time for a REPEATED START
t _{HD_STA}	Hold Time for a (REPEATED) START
t _{LOW}	SCL Clock Low Period
t _{DIG_L}	SCL Clock Low Period as seen at the
	receiver
t _{нібн}	SCL Clock High Period
t _{DIG_H}	SCL Clock High Period as seen at the
	receiver
t _{su_dat}	Data Setup Time
t _{HD_DAT}	Data Hold Time
t _{rCL}	SCL Signal Rise Time
t _{fCL}	SCL Signal Fall Time
t _{rDA}	SDA Signal Rise Time
t _{rDA_OD}	SDA Signal Rise Time (Open Drain)
t _{fDA}	SDA Signal Fall Time
t _{su_sto}	Setup Time for STOP
t _{BUF}	Bus Free Time Between a STOP and a
	START
t _{spike}	Pulse Width of Spikes that Spike Filter
	Must Suppress

¹ Only available when the bus configuration is set to Mixed Bus (i.e. at least one I²C legacy device is presented on the I3C bus).



Symbol	Electrical Parameter
t _{low_od}	SCL Clock Low Period
t _{DIG_OD_L}	SCL Clock Low Period as seen at the receiver
t _{HIGH_INIT}	High Period of SCL Clock (for First Broadcast Address)
t _{HIGH_OD}	SCL Clock High Period
t _{DIG_OD_H}	SCL Clock High Period as seen at the receiver
t _{fDA_OD}	SDA Data Fall Time
t _{su_od}	SDA Data Setup Time During Open Drain Mode
t _{CAS}	Clock After START (S) Condition
t _{CBP}	Clock Before STOP (P) Condition
t _{CRHPOverlap}	Active Controller to Secondary Overlap time during handoff
taval	Bus Available Condition
tidle	Bus Idle Condition
t _{NEWCRLock}	Time Interval Where New Controller Not Driving SDA Low

MIPI I3C Open Drain Timing Requirements



Symbol	Electrical Parameter
t _{LOW}	SCL Clock Low Period
t _{DIG_L}	SCL Clock Low Period as seen at the receiver
t _{нібн}	SCL Clock High Period
t _{DIG_H}	SCL Clock High Period as seen at the receiver
t _{sco}	Clock in to Data Out for Target
t _{CR_PP}	SCL Clock Rise Time
t _{CF_PP}	SCL Clock Fall Time
t _{HD_PP_Controller}	SDA Signal Data Hold (Controller)
t _{HD_PP_Target}	SDA Signal Data Hold (Target)
t _{su_pp}	SDA Signal Data Setup
t _{CASr}	Clock After Repeated START (Sr) Condition
t _{CBSr}	Clock Before Repeated START (Sr) Condition
t _{вт_но}	HDR-BT Master to Slave Hand Off Delay
t _{BT_STALL}	HDR-BT Clocked Not-Ready Data-Block Headers

MIPI I3C Push-Pull Timing Requirements



MIPI I3C I/O Stage Characteristics Voltage Require	ements
--	--------

Symbol	Electrical Parameter
V _{IL}	Low-Level Input Voltage
VIH	High-level Input Voltage
V _{OL}	Low-level Output Voltage
V _{OH}	High-level Output Voltage



5. 電氣特性驗證 軟體畫面





MIPI RFFE 電氣特性驗證解決方案

■ 簡介:

File / Sett	ngs Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrica Validatio	I Open EV File			1			

MIPI RFFE (Radio Frequency Front-End) 是由 MIPI 聯盟所制定的標準規範,用以定義行動裝置(如智慧型手機和平板電腦)中基頻處理器與射頻前端模組之間的通訊標準。這是 MIPI (Mobile Industry Processor Interface) 標準家族的重要部分,涵蓋多種針對行動與嵌入式設備中元件之間通訊效率所設計的標準。

MIPI RFFE 是現代無線設備的關鍵技術,提供一個標準化且高效的介面,用於控制無線通 訊系統中的射頻前端元件。



■ MIPI RFFE 電氣特性驗證設定:

1. 一般設定:設定通道來源、工作電壓、頻率範圍、Test Point 和 Read

Operation •

EV Electrical Validatio	n		>
120	Settings		Import Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	General Trigger Validation	Channel Settings SCLK: DSO Channel 1 Probe Settings: x10 Probe Se	
			INEXL

2. 觸發設定

EV Electrical Validation	I.		×
12C	Settings		Import Export
IZS MIPI I3C MIPI SPMI PDM SPI UART(RS232)	 ✓ General → Trigger ★ Validation 	Type: Any Command Slave Address: Xh Register Address (Lower): XXh Register Address (Upper): XXh Data • Any Offset • Fixed Offset • Byte(s) Data 1 XAh Data 5 Data 2 XXh Data 6 Data 3 XXh Data 7 Data 4 XXh Data 8	Previous Next



3. 驗證設定:包含電壓、時序與頻率的限制條件

EV Electrical Validation	1				;					
120	Settings				Import Export					
I2S MIPI I3C	 ✓General ✓Trigger 	Customized EV Parameter:								
MIPI SPMI PDM	Validation	Frequency								
SPI		Name	Description	Min	Max					
UART(RS232)		1 ✔ f _{SCLK} SCLK Frequency		0.032 MHz	26 MHz					
		► Time (Full-Speed C	Operations)							
		▲ Time (Half-Speed I	Data Response Operations)							
		Name	Description	Min	Max					
		1 ✓ t _{SCLKOH_HSDR} (HSDR) Clock	1 ✓ t _{SCLKOH, HSDR} (HSDR) Clock Output High Time							
		2 ✓ t _{SCLKOL_HSDR} (HSDR) Clock	k Output Low Time	28.1 ns	X					
		3 🗹 t _{SCLKOTR_HSDR} (HSDR) Clock	1 ♥ t _{SCLKOH, HSDR} (HSDR) Clock Output High Time 28.1 ns 2 ♥ t _{SCLKOH, HSDR} (HSDR) Clock Output Low Time 28.1 ns 3 ♥ t _{SCLKOTR, HSDR} (HSDR) Clock Output Transition (Rise/Fall) Time 3.5 ns							
		4 ✔ t _{SU.M.Rd.HSDR} (HSDR) SDATA Setup Time, with respect to SCLK Output - BOM - Read	3.75 ns	X						
		5 v t _{H_M_Rd_HSDR} (HSDR) SDAT	TA Hold Time, with respect to SCLK Output - BOM - Read	6.75 ns	×					
		∠ Voltage								
		Name	Description	Min	Max					
		1 ✔ V _{Low} Low-Level Voltage		0 V	0.36 V					
		2 🗸 V _{High} High-Level Voltage		1.44 V	1.8 V 💌					
	Default	Advance			Previous Apply					

4. 電氣特性驗證 軟體畫面





5. 控制面板



- A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止
- B. 資訊:選擇查看波形
- C. 储存檔案: 储存為 HTML 格式 储存為 .MOW (Acute軟體專用格式)

6. 概覽報告

	2 V -1.12			2 2 <u>-</u> 0	/ 05						800 ns +4.812 ns III RFFE Validation Stop <u>StrR: 500 MS/s</u>
									M		+4.312 //s Clop S/R-500 MS/s
De						SSC SA:4	Reg. Wr. Addn	ess: 1C <mark>0</mark>	Data: 03	10 10 10 10 10 10 10 10 10 10 10 10 10 1	CEC SA:F Reg Wr Addrew IC 1 Dam 0 0 0
	verview Det	tail MIPI RFI	E					1.10.14		0 h	
1	f _{SCLK}	SCLK Fre	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	Fail	
2	tsclkon	Clock Out	4.700 ns		6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	Pass	
3	tscl.kol	Clock Out	4.700 ns		8.329 ns	41.946 ns	1.563 us	196.252 ns	230	Pass	
4	t SCLKOTR	Clock Out	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail	-
5	tsci.kin	Clock Inpu							0		
6	tsclkil	Clock Inpu							0		
7	İ SCLKITR	Clock Inpu							0		
8	t _{skew_M}	SDATA Sk	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95	Fail	
9	SDATAOTR_M	SDATA Ou	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	Fail	
1	teo_s_R	Time for s							0		
1	tSDATAOTR_S_IR	sRead SD							0		y and the second se



7. 詳細報告



8. 波形和參考點





9. Html 報告

Cobased T&M Instruments Fc-based T&M Instruments Electrical Validation Report Test Instrument Model MSV31240021 Test Instruments File 12:09-2024 15:32:11 SW Version 18:82 Protocol MIPI RFFE												
Total: Pass:	33 2											
Fail:	6											
Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Devia	ation Count	Margin Min	Margin Max	Result
1	ISCI K	SCLK Frequency	26.000 MHz	52.000 MHz	49.200 MHz	52.209 MHz	56.354 MHz	2.244 MHz	220	89.2%	8.4%	×Fail
2	tSCLKOH	Clock Output High Time	4.700 ns		6.413 ns	7.501 ns	9.281 ns	714.000 ps	230	36.4%		✓Pass
3	t _{SCLKOL}	Clock Output Low Time	4.700 ns		8.329 ns	41.946 ns	1.563 us	196.252 ns	230	77.2%		✓Pass
4	t _{SCLKOTR}	Clock Output Transition (Rise/Fall) Time	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	×Fail
5	t _{SCLKIH}	Clock Input High Time							0			
6	t _{SCLKIL}	Clock Input Low Time							0			
7	t _{SCLKITR}	Clock Input Transition (Rise/Fall) Time							0			
8	t _{skew_M}	SDATA Skew Relative to SCLK, BOM Master Output	0.000 ps	4.000 ns	-699.000 ps	13.917 ns	178.727 ns	39.049 ns	95		4368.2%	×Fail
9	t _{SDATAOTR_M}	SDATA Output Transition (Rise/Fall) Time, BOM Master	2.100 ns	4.000 ns	743.000 ps	1.088 ns	1.799 ns	204.000 ps	460	-64.6%	-55.0%	×Fail
10	t _{PD_S_sR}	Time for sRead Data Output Valid from SCLK Rising Edge - Slave							0			
11	t _{SDATAOTR_S_SR}	sRead SDATA Output Transition (Rise/Fall) Time - Slave							0			
12	t _{SU_M_Rd}	SDATA Setup Time, with respect to SCLK Output - BOM - Read							0			
13	t _{H_M_Rd}	SDATA Hold Time, with respect to SCLK Output - BOM - Read							0			
14	t _{SU_M_sR}	SDATA Setup Time, with respect to SCLK Output - BOM - sRead							0			
15	t _{H_M_sR}	SDATA Hold Time, with respect to SCLK Output - BOM - sRead							0			
16	t _{s∪_s}	SDATA Setup Time, with respect to SCLK Input - Slave (or non-BOM)							0			
17	t _{H_S}	SDATA Hold Time, with respect to SCLK Input - Slave (or non-BOM)							0			
18	tSCLKOH_HSDR	(HSDR) Clock Output High Time							0			
19	tSCLKOL_HSDR	(HSDR) Clock Output Low Time							0			
20	SCLKOTR_HSDR	(HSDR) Clock Output Transition (Rise/Fall) Time							0			
21	SCLKIH_HSDR	(HSDR) Clock Input High Time							0			
22	SCLKIL_HSDR	(HSDR) Clock Input Low Time							0			
23	SCLKITR_HSDR	(HSDR) Clock input Transition (Rise/Fall) Time							0			
24	PD_S_Rd_HSDR	(HSDR) Time for Read Data Output Valid from SCLK Rising Edge - Slave							0			
20	SDATAOTR_S_Rd_HSDR	(HSDR) Read SDATA Output Transition (Rise/Fall) Time - Stave							0			
20	PD_S_R_HSDR	(HSDR) sRead CDATA Output Transition (Pice/Fall) Time - Office							0			
27	SDATAOTR_S_SR_HSDR	(HSDR) SDATA Satus Time with respect to SCI K Output - Slave							0			
20	SU_M_Rd_HSDR	USDD) SDATA Setup Time, with respect to SCLK Output - BOM - Read							0			

f_{SCLK} - Test Result: Fail Description: SCLK Frequency







MIPI SPMI 電氣特性驗證解決方案

■ 簡介:

	File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
	EV Electrical Validation	Open EV File						
L								

使用示波器執行 MIPI SPMI 電氣特性驗證,以確保 MIPI SPMI 協定符合既定規格。在經過 長時間燒機測試後,可確認所測試的訊號電氣特性是否符合標準。

MIPI SPMI (System Power Management Interface) 是由 MIPI 聯盟 (Mobile Industry Processor Interface) 制定的標準規範,主要目的是為了在行動與嵌入式系統中實現電源管理。SPMI 提供標準化的通訊介面,用於在電源管理 IC (PMIC) 與各個系統元件之間有效 地分配電力與管理電源狀態,常見於智慧型手機、平板電腦等裝置中。



■ MIPI SPMI 電氣特性驗證設定

1. 一般設定:設定通道來源、工作電壓、傳輸速率與協定版本。

Evertrical Validation	×
I2C Settings	Import Export
IZS MIPI I3C MIPI SFM PDM SPI UART(RS232) Channel Settings CLAnnel Settings CLANNEL Settings: x10 • • • • • • • • • • • • • • • • • • •	
Default	Next

2. 觸發設定

EV Electrical Validation											×
120	Settings									Import	Export
I2S MIPI I3C MIPI RFFE MIPI SPMI PDM SPI UART(RS232)	 ✓General →Trigger ★Validation 	Command Sequence Type: Any Command Slave Address: Xh Register Address: XXXXh Data									
		Data 1	XXh	Data 5	XXh	Data 9	XXh	Data 13	XXh		
		Data 2	XXh	Data 6	XXh	Data 10	XXh	Data 14	XXh		
		Data 3	XXh	Data 7	XXh	Data 11	XXh	Data 15	XXh		
		Data 4	XXh	Data 8	XXh	Data 12	XXh	Data 16	XXh		
	Default									Previous	Next



3. 驗證參數設定:包含頻率、時間與電壓限制

Electrical Validatio	n									
120	Settings				Import Expo					
I2S MIPI I3C	 ✓General ✓Trigger 	Customized EV Parameter:								
MIPI KFFE MIPI SPMI PDM	Validation	Frequence	у							
SPI		Name	Description	Min	Max					
JART(RS232)		1 ✓ f _{SCLK} SCLK	Frequency	32 KHz	26 MHz					
		⊿ Time								
		Name	Description	Min	Max					
		1 ✓ t _{SCLKOH}	SCLK Output High Time	12 ns	х					
		2 ✓ t _{SCLKOL}	SCLK Output Low Time	12 ns	x					
		3 ✓ t _{SCLKOTR}	SCLK Output Transition (Rise/Fall) Time	2.1 ns	5.3 ns					
		4 ✓ t _{sdataotr}	SDATA Output Transition (Rise/Fall) Time	2.1 ns	5.3 ns					
		5 ✔ t _D	SDATA Output Valid Time	0 us	11 ns					
		6 √ t _s	SDATA Setup Time	1 ns	×					
		7 🗸 t _H	SDATA Hold Time	5 ns	x					
		✓ Voltage								
		Name	Description	Min	Max					
		1 ✔ V _L Low-L	evel Voltage	0 V	360 mV					
			L IV b	4.444	1.01/					

4. 電氣特性驗證 軟體畫面




5. 控制面板



- A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止
- B. 資訊:選擇查看波形
- C. 儲存檔案: 儲存為 HTML 格式 儲存為 .MOW (Acute軟體專用格式)

6. 概覽報告

1	2 V +0.35		a de la companya de la Companya de la companya				Sequence Start	t Condition			El 1 µs 3 846 µs T MIPI SPMI Validation Shop SrR. 500 MS/s 4 40 40 8 03 8 5 44 ER WL A1 40 40 8 03 8	
Ove	erview Det	tail MIPI SPI						1.15.11		D 1		
1 1	SCLK	SCLK Fre	32.000 KHz	26.000 MHz	173.325 KHz	9.141 MHz	10.686 MHz	1.753 MHz	333	Pass		
2 1	SCLKOH	SCLK Out	12.000 ns		41.401 ns	51.548 ns	109.473 ns	13.618 ns	338	Pass		
3 1	SCLKOL	SCLK Out	12.000 ns		41.351 ns	102.355 ns	5.718 us	501.997 ns	340	Pass		
4	SCLKOTR	SCLK Out	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678	Fail		
5 1	SDATAOTR	SDATA Ou	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117	Fail		
6 1	6	SDATA Ou	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	Fail		
7 1	8	SDATA Se	1.000 ns		26.694 ns	46.232 ns	98.913 ns	12.421 ns	83	Pass		
8 1	a	SDATA Ho	5.000 ns		43.207 ns	195.261 ns	5.299 us	790.518 ns	114	Pass		
9	V.	Low-Level	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 mV	135.513 mV	340	Pass		
10	V _H	High-Level	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338	Fail		



7. 詳細報告



8. 波形和參考點

1 2 V +0.35			2 2	V).98										H 10 ns +4.78 µs	MIPI SPMI Valio Stop S/R: 500	dation <u>MS/s</u>
2	1		1 - 1							MEL1 Detail					×	· · · · · · · ·
									ľ	H Waveform No.	Time Stamp	СМД	Limi	t Min	Limit Max	
Overview D	etail MIPI SP	PMI							Ľ	1-1	484.000 ns	31h	1.44	10 V	1.800 V	
fscux tscux	on t _{scikol}	t _{SCLKOTR}	t _{SDATAOTR} t _D	ts t _H	V _L V _H	Moon	Max			Time	∆ Time	Volt	∆ Volt	Result	-	
1 1-1	484.000 ns	31h	1.440 V	1.800 V	3.046 V	3.303 V	3.601 V	67	1	(966.548 ns, 1.010 µs)	43.261 ns	(2.31 V, 2.31 V)	0 V	Fail	_	
2 2-1	277.000 ns	16h	1.440 V	1.800 V	3.039 V	3.328 V	3.700 V	58	2	(1.061 µs, 1.110 µs)	48.762 ns	(2.31 V, 2.31 V)	0.1	Fail		
3 3-1	222.000 ns	31h	1.440 V	1.800 V	2.997 V	3.283 V	3.531 V	105	3	(1.1/2 µs, 1.220 µs)	48.537 hs	(2.31 V, 2.31 V)	0.0	Fall		
4 4-1	1.806 us		1.440 V	1.800 V	3.176 V	3.366 V	3.588 V	13	4	(1.2/1 µs, 1.320 µs)	40.072 fts	(2.31 V, 2.31 V)	0.1	Fail		
5 5-1	537.000 ns	31h	1.440 V	1.800 V	3.067 V	3.379 V	3.623 V	95	6	(1.3/1 µs, 1.420 µs)	40.720 fts	(2.31 V, 2.31 V)	0.V	Fail		
										(1.407 µs, 1.500 µs)	43.201 //S	(2.31 V, 2.31 V)	0.V	Fail		
									2	(11 662 us 11 710 us)	40.014 ms	(2 31 V 2 31 V)	0.V	Fail		
									9	(11.761 us. 11.810 us)	48.851 ps	(2.31 V, 2.31 V)	0 V	Fail		
									P		-				× Close	
									-							



9. Html 報告

PC-k	CU based T&A	linstruments					1	Electrical V Test Instrument N est Instruments Seria Test Date	alidat Iodel Il Numbe	tion Re MSC r MSV3 12-09-20	eport 03124V 1240021 24 14:54:25	
							-	S/W Version		1.	8.62	
							L	Protocol			I SPMI	
Over Total: Pass: Fail:	10 6 4	sults:		[1							
Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count M	largin Min	Margin Max	Result
1	SCLK	SCLK Frequency	32.000 KHZ	26.000 MHZ	173.325 KHZ	9.141 MHZ	10.686 MH	Z[1.753 MHZ	333 4	41.6%	-58.9%	✓Pass
2	SCLKOH	SCLK Output High Time	12.000 ns		41.401 ns	51.548 ns	109.473 ns	13.618 ns	338 24	45.0%		✓Pass
3	SCLKOL	SCLK Output Low Time	12.000 ns		41.351 ns	102.355 ns	5.718 us	501.997 ns	340 24	44.6%		✓Pass
4	ISCLKOTR	SCLK Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	984.000 ps	2.442 ns	7.153 ns	1.618 ns	678 -5	53.1%	35.0%	×Fail
5	^t SDATAOTR	SDATA Output Transition (Rise/Fall) Time	2.100 ns	5.300 ns	974.000 ps	1.347 ns	1.932 ns	234.000 ps	117 -5	53.6%	-63.5%	×Fail
6	t _D	SDATA Output Valid Time	0.000 ps	11.000 ns	-408.000 ps	163.644 ns	5.401 us	814.092 ns	114	-	48997.2%	×Fail
7	ts	SDATA Setup Time	1.000 ns		26.694 ns	46.232 ns	98.913 ns	12.421 ns	83 2	569.4%		✓Pass
8	tн	SDATA Hold Time	5.000 ns		43.207 ns	195.261 ns	5.299 us	790.518 ns	114 70	64.1%		✓Pass
9	VL	Low-Level Voltage	0.000 uV	360.000 mV	-337.083 mV	28.764 mV	283.550 m	V 135.513 mV	340	-	-21.2%	✓Pass
10	V _H	High-Level Voltage	1.440 V	1.800 V	2.997 V	3.325 V	3.700 V	134.058 mV	338 10	08.1%	105.5%	×Fail

f_{SCLK} - Test Result: Pass Description: SCLK Frequency





PDM 電氣特性驗證解決方案

■ 簡介:

File / Settings Display Measurement & Analysis Electrical Validation	Cursor Acquire Utility
Electrical Validation EV File	

使用示波器執行 PDM (Pulse Density Modulation) 電氣特性驗證,以確保其訊號符合既定 電氣標準規格。在經過長時間燒機測試後,可以確認待測訊號的電氣特性是否滿足標準要 求。

PDM 協定的電氣特性檢測通常分為兩大類:

- • 重直屬性(電壓)
- 水平屬性(時間/相位)

因此,使用此功能時,必須先設定所選的協定與測試規範,並透過重複測試來取得電氣特 性報告。測試項目會根據 PDM 傳輸速率而有所不同。

DIGITAL AUDIO INTERFACE					
PDM_CLK High Frequency Range	fclкн		5.28	8.64	MHz
PDM_CLK Low Frequency Range	f _{CLKL}		1.84	4.32	MHz
PDM_CLK High Time	^t PDM_CLKH		40		ns
PDM_CLK Low Time	tPDM_CLKL		40		ns

常用 PDM 規格中的部分電氣特性項目參數:



常用 PDM 驗證報告內容:

C	verview Det	ail PDM									
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result	
1	f _{CLK}	Clock freq	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	Pass	
2	tLow	Low Perio	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	Pass	
3	t _{HIGH}	High Perio	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	Pass	
4	t _{rCL}	Rise time		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930	Pass	
5	t _{rCL}	Fall time o		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930	Pass	
6	t _{rDD}	Delay time	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	Pass	
7	t _{fDV}	Delay time		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500	Pass	
8	t _{rDD}	Delay time	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	Pass	
9	t _{rDV}	Delay time		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440	Pass	

電氣特性驗證 軟體畫面:



- 1. 頻率:時鐘頻率 (Clock Speed)
- 2. 時序参數:Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 3. 電壓參數: V_IL (輸入低電位)、V_IH (輸入高電位)等



Frequency:

Symbol	Electrical Parameter
f _{SCL}	PDM_CLK Frequency Range

Time:

Symbol	Electrical Parameter
t _{LOW}	Low Period of the Clock
t _{ніGH}	High Period of the Clock
t _{rCL}	Rise time of Clock signal
t _{fCL}	Fall time of Clock signal
t _{rDD}	Delay time from Clock edge to Data Rise driven
t _{fDD}	Delay time from Clock edge to Data Fall driven
t _{rDV}	Delay time from Clock edge to Data Rise valid
t _{fDV}	Delay time from Clock edge to Data Fall valid

Voltage:

Symbol	Electrical Parameter
V _{ClkLow}	Low-level Input voltage for clock
V _{ClkHigh}	High-level Input voltage for clock
V _{DataLow}	Low-level Input voltage for data
$V_{DataHigh}$	High-level Input voltage for data



■ PDM 電氣特性驗證設定

1. 一般設定:設定通道來源、工作電壓與傳輸速率。

Settings	
 General Decode 	Channel Settings
×Validation	CLK: DSO Channel 1 V Probe Settings: x10 V
	Working Voltage(V _{DD}): 1.80 V
	PDM Clock Speed: 3072 VHz
Default	Next

2. 解碼設定:設定 PDM 解碼參數

Settings		
 ✓General →Decode 	Audio Settings	
×Validation	Decimation Rate: x64 Audio Frequency 48 KHz	
	Mono & Stereo	
	Mode: Stereo 💌	
Default	Previous	xt



3. 驗證參數設定:頻率、時序與電壓限制

idation	✓ Frequency		
	Name Description	Min	Max
	1 € I _{CLK} Clock frequency	0 kHz	3.072 MHz
	⊿ Time		
	Name Description	Min	Max
	1 ✓ t _{Low} Low Period of the Clock	130.208 ns	195.312 ns
	2 ✓ t _{HIGH} High Period of the Clock	130.208 ns	195.312 ns
	3 ✔ t _{rcL} Rise time of CLK signal	Х	13 ns
	4 ✔ t _{ICL} Fall time of CLK signal	Х	13 ns
	5 ✔ t _{rDD} Delay time from Clk edge to Data Rise driven	40 ns	80 ns
	6 ✔ t _{DD} Delay time from Clk edge to Data Fall driven	40 ns	80 ns
	7 ✓ t _{rDV} Delay time from Clk edge to Data Rise Valid	х	100 ns
	$8 \fbox{I}_{\text{DV}}$ Delay time from Clk edge to Data Fall Valid	X	100 ns
	✓ Voltage		
	Name Description	Min	Max
	1 ✓ V _{Ciktow} Low-level input voltage for clock	-0.5 V	0.54 V
	2 ✔ V _{Cliffigh} High-level input voltage for clock	1.26 V	2.3 V
	3 ✔ V _{Datat.ow} Low-level input voltage for Data	-0.5 V	0.54 V
	4 ✓ V _{DataHigh} High-level input voltage for Data	1.26 V	2.3 V

4. 電氣特性驗證 軟體畫面





5. 控制面板



- A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止
- B. 資訊:選擇查看波形
- C. 儲存檔案:
 儲存為 HTML 格式
 儲存為 .MOW (Acute軟體專用格式)

6. 概覽報告

1 500 mV -3.50	2 5	00 mV 3.50				н	1 µs -328 ns	T PDM Vali	idation R: 500 MS/s	
					+++++					
 	M M M	M. M. M.	M	h h h	1. <mark>71</mark> <mark>7</mark>		 =, e, e		n h	۳ ۲
	m m	┍┝╾┶	╎┟┶╾┥	** <u>1</u>					`] (`] (`]	
					1	234	667	890	• • • •	
20M 0 0 1 1	000000	0111110	000110							
					1.2	999	• • •	P		
	<mark>∦ e</mark> rer e ere		a- 944 94 94	• •• •••		*** **				₩ ŀ
Overview De	etail PDM	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result	U U
1 Dverview De Name fcLk	etail PDM Description Clock freq	Limit Min 0.000 Hz	Limit Max 3.072 MHz	Min 3.027 MHz	Mean 3.030 MHz	Max 3.034 MHz	ndard Deviat	Count 4430	Result Pass	
Dverview De Name f _{CLK} t _{LOW}	etail PDM Description Clock freq Low Perio	Limit Min 0.000 Hz 130.208 ns	Limit Max 3.072 MHz 195.312 ns	Min 3.027 MHz 163.008 ns	Mean 3.030 MHz 163.289 ns	Max 3.034 MHz 163.541 ns	ndard Deviat 17.798 KHz 1.399 ns	Count 4430 4920	Result Pass Pass	
Dverview De Name fcLk t.cw t.cw t.cw	Image: state	Limit Min 0.000 Hz 130.208 ns 130.208 ns	Limit Max 3.072 MHz 195.312 ns 195.312 ns	Min 3.027 MHz 163.008 ns 163.162 ns	Mean 3.030 MHz 163.289 ns 163.428 ns	Max 3.034 MHz 163.541 ns 163.717 ns	ndard Deviat 17.798 KHz 1.399 ns 1.709 ns	Count 4430 4920 4920	Result Pass Pass Pass	
Deerview Deerview Verview Deerview I fcl.x 2 t.cox 3 tacce 4 t.cox	PDM Description Clock freq Low Perio High Perio Rise time	Limit Min 0.000 Hz 130.208 ns 130.208 ns	Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns	Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns	Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns	Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns	ndard Deviat 17.798 KHz 1.399 ns 1.709 ns 2.428 ns	Count 4430 4920 4920 4930	Result Pass Pass Pass Pass	
Dverview De Name fcl.x fcl.x stock g tcc. g tcc.	etail PDM Description Clock freq Low Perio High Perio Rise time Fall time o	Limit Min 0.000 Hz 130.208 ns 130.208 ns 	Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns 13.000 ns	Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns 1.412 ns	Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns 1.661 ns	Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns 1.862 ns	ndard Deviat 17.798 KHz 1.399 ns 1.709 ns 2.428 ns 2.529 ns	Count 4430 4920 4920 4930 4930	Result Pass Pass Pass Pass Pass Pass	
Overview De Name 1 f.c.x 2 t.cow 3 t.c. 5 t.co 5	etail PDM Description Clock freq Low Perio Rise time Fall time o Delay time	Limit Min 0.000 Hz 130.208 ns 130.208 ns 40.000 ns	Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns 13.000 ns 80.000 ns	Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns 1.412 ns 57.382 ns	Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns 1.661 ns 64.017 ns	Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns 1.862 ns 74.913 ns	ndard Deviat 17.798 KHz 1.399 ns 1.709 ns 2.428 ns 2.529 ns 77.763 ns	Count 4430 4920 4920 4930 4930 2500	Result Pass Pass Pass Pass Pass Pass Pass	
Overview De Name 1 fcl.k 2 toos 4 fcl.k 4 fcl.k 4 fcl.k 5 fcl.k <td>PDM Description Clock freq Low Perio High Perio Rise time Pall time o Delay time</td> <td>Limit Min 0.000 Hz 130.208 ns 130.208 ns 40.000 ns </td> <td>Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns 13.000 ns 80.000 ns 100.000 ns</td> <td>Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns 1.412 ns 57.382 ns 60.111 ns</td> <td>Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns 1.661 ns 64.017 ns 67.555 ns</td> <td>Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns 1.862 ns 74.913 ns 79.252 ns</td> <td>ndard Deviat 17.798 KHz 1.399 ns 1.709 ns 2.428 ns 2.529 ns 77.763 ns 83.904 ns</td> <td>Count 4430 4920 4920 4920 4930 4930 2500 2500</td> <td>Result Pass Pass Pass Pass Pass Pass Pass Pas</td> <td></td>	PDM Description Clock freq Low Perio High Perio Rise time Pall time o Delay time	Limit Min 0.000 Hz 130.208 ns 130.208 ns 40.000 ns 	Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns 13.000 ns 80.000 ns 100.000 ns	Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns 1.412 ns 57.382 ns 60.111 ns	Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns 1.661 ns 64.017 ns 67.555 ns	Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns 1.862 ns 74.913 ns 79.252 ns	ndard Deviat 17.798 KHz 1.399 ns 1.709 ns 2.428 ns 2.529 ns 77.763 ns 83.904 ns	Count 4430 4920 4920 4920 4930 4930 2500 2500	Result Pass Pass Pass Pass Pass Pass Pass Pas	
Devention Devention Facus Facus facus Facus g facus	PDM Description Clock freq Low Perio High Perio Rise time Pall time o Delay time Delay time Delay time	Limit Min 0.000 Hz 130.208 ns 130.208 ns 130.208 ns 40.000 ns 40.000 ns	Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns 13.000 ns 80.000 ns 100.000 ns 80.000 ns	Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns 1.412 ns 57.382 ns 60.111 ns 54.659 ns	Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns 1.661 ns 64.017 ns 67.555 ns 60.684 ns	Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns 1.862 ns 74.913 ns 79.252 ns 71.123 ns	Indard Deviat 17.798 KHz 1.399 ns 1.709 ns 2.428 ns 2.529 ns 77.763 ns 83.904 ns 67.169 ns	Count 4430 4920 4920 4930 4930 2500 2500 2440	Result Pass	
Overview De fc.u. fc.u. fc.u. tc.ov tc.ov tc.ov tc.ov tc.ov tc.ov tc.ov	PDM Description Clock freq Low Perio High Perio Rise time Pall time o Delay time Delay time Delay time Delay time	Limit Min 0.000 Hz 130.208 ns 130.208 ns 130.208 ns 40.000 ns 40.000 ns 	Limit Max 3.072 MHz 195.312 ns 195.312 ns 13.000 ns 13.000 ns 80.000 ns 80.000 ns 100.000 ns 100.000 ns	Min 3.027 MHz 163.008 ns 163.162 ns 1.380 ns 1.412 ns 57.382 ns 60.111 ns 54.659 ns 57.573 ns	Mean 3.030 MHz 163.289 ns 163.428 ns 1.621 ns 1.661 ns 64.017 ns 67.555 ns 60.684 ns 64.149 ns	Max 3.034 MHz 163.541 ns 163.717 ns 1.859 ns 1.862 ns 74.913 ns 79.252 ns 71.123 ns 75.158 ns	Indard Deviat 17.798 KHz 1.399 ns 1.709 s 2.428 ns 2.529 ns 77.763 ns 83.904 ns 67.169 ns 71.543 ns	Count 4430 4920 4920 4930 4930 2500 2500 2440 2440	Result Pass Pass	



7. 詳細報告

1	500 mV -3.50	2 5	00 mV 3.50				Н	1 µs -328 ns	T PDM Valid Stop <u>S/R</u>	lation <u>:: 500 MS/s</u>
							2 8 0			
PDM 1	erview Det	2, 12, 0, 0, 11, 0 , 12, 0, 0, 11, 0 , 14, 0, 0, 0, 11, 0 , 14, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 14, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 , 14, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,				0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		010110 6 7 8		
fcu	k t _{LOW}	t _{HIGH} t _{rCL}	t _{ICL} t _{IDD}	t _{rDV} t _{rD}	D t _{rDV}	V _{ClkLow} V _{Data}	Low V _{ClkHigh}	V _{DataHigh}		
	Waveform No.	TimeStamp	Limit Min	Limit Max	Min	Mean	Max	Count	Result	<u> </u>
1	1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass	
2	2-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass	
3	3-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.034 MHz	443	Pass	
4	4-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass	
5	5-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3.033 MHz	443	Pass	
6	6-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass	
7	7-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3.032 MHz	443	Pass	
8	8-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.033 MHz	443	Pass	-
unti	tled1 🗶	EV_PDM_Ste	reo 🗙							·

8. 波形和參考點

500 mV -3.50		2 50 -3	00 mV .50							H 100 ns -328 ns		OM Validatio op <u>S/R: 50</u>	on 00 MS/s
	RO	fr fr			• •	RO	Detail	 L	 			٨	
Overview [Detail PDM						CLK Waveform No.	Tiı	meStamp	Limit Min	Limit	Max	Min
f _{CLK} t _{LOW}	t _{HIGH} t _{rCL}	t _{ICL} t _{IDD}	t _{rDV} t _{rl}	DD t _{rDV}	V _{ClikLow} V _{Data}		1-1	8	1.316 us	0.000 Hz	3.072	MHz	3.027 MHz
Waveform	No. TimeStamp	Limit Min	Limit Max	Min	Mean		Time		∆ Time	Volt	∆ Volt	Result	-
1 1-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	2 1	(16.439 µs, 16.769 µ	µs)	330.000 ns	(540 mV, 1.26 V)	/20 mV	Pass	_
2 2-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3 2	(16.769 µs, 17.099 µ	µs)	330.022 ns	(540 mV, 1.26 V)	720 mV	Pass	
3 3-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3	(17.099 µs, 17.429 µ	µs)	329.944 ns	(540 mV, 1.26 V)	720 mV	Pass	
4 4-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3 4	(17.429 µs, 17.759 µ	µs)	330.069 ns	(540 mV, 1.26 V)	720 mV	Pass	
5 5-1	81.316 us	0.000 Hz	3.072 MHz	3.028 MHz	3.030 MHz	3 5	(17.759 µs, 18.089 µ	µs)	330.059 ns	(540 mV, 1.26 V)	720 mV	Pass	
6 6-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3 6	(18.089 µs, 18.419 µ	µs)	329.840 ns	(540 mV, 1.26 V)	720 mV	Pass	
7 7-1	81.316 us	0.000 Hz	3.072 MHz	3.029 MHz	3.030 MHz	3 7	(18.419 µs, 18.749 µ	µs)	330.122 ns	(540 mV, 1.26 V)	720 mV	Pass	
8 8-1	81.316 us	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3 8	(18.749 µs, 19.079 µ	µs)	330.000 ns	(540 mV, 1.26 V)	720 mV	Pass	
							(40.070 40.400		200.042	1540 14 4 00 10	700 14	-	
						9	(19.079 µs, 19.409 µ	us)	329.943 ns	(540 mV, 1.26 V)	720 mV	Pass	-



9. Html 報告

Δ	C	J	f	e
PC-ba	ased Ta	&M In	strur	ments

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

Total: 13 Pass: 13 Fail: 0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fclk	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	***	-1.2%	Pass
2	t _{LOW}	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	Pass
3	tнівн	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	Pass
4	t _{rCL}	Rise time of CLK signal		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930		-85.7%	Pass
5	4 _{CL}	Fall time of CLK signal		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930		-85.7%	Pass
6	t _{fDD}	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	Pass
7	trov	Delay time from Clk edge to Data Fall Valid		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500		-20.7%	✓Pass
8	t _{rDD}	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	Pass
9	t _{rDV}	Delay time from Clk edge to Data Rise Valid		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440		-24.8%	✓Pass
10	VCIkLow	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	Pass
11	VDataLow	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	Pass
12	VClkHigh	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	Pass
13	VDataHigh	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	Pass

f_{CLK} - Test Result: Pass Description: Clock frequency

Limit Min Limit Max Min Mean Max Standard De	viation Count	Margin Min Marg	n Max			
0.000 Hz 3.072 MHz3.027 MHz3.030 MHz3.034 MHz17.798 KHz	4430			1		
Instogram		Value Range	Occurance Count			
Occurance (%), Total 4430		3 027 MHz ~ 3 028 M	2 13			
100		2.022.184-2.2.022.18	70			
80 -		3.020 MP12 - 3.020 MP				
70 -		3.028 MHz ~ 3.029 MH	z 295			
50		3.029 MHz ~ 3.03 MHz	813			
40 33.0 30 24.2		3.03 MHz ~ 3.03 MHz	1464			
20 18.4 11.9		3.03 MHz ~ 3.031 MHz	1073			
10 0.3 1.6 0.7 30 0.5 0.2	Test Value	3.031 MHz ~ 3.032 MH	z 529			
3.027 MHz 3.0	34 MHz	3.032 MHz ~ 3.032 MH	z 135			
Test Value 3.027 MHz 3.03	4 MHz (-1.2%)	3.032 MHz ~ 3.033 MH	z 27			
Limit 3.0	12 MHz	3.033 MHz ~ 3.034 MH	z 8			
Min Detail Repo	rt Row: 1, Tes	t Index: 340 Ma	x	· · · · · · · · · · · · · · · · · · ·	Detail Report Re	ow: 3, Test Index: 431
500 mV 2 500 mV 112.198 μs	PDM Validation Stop S/R: 500 M	IS/6	500 mV 500 mV 3.50	mV)	100 ns PDI -142.228 µs 🚺 Sto	M Validation p <u>S/R: 500 MS/s</u>
	El Margan					



SMBus 電氣特性驗證解決方案

■ 簡介:

File / Setting	s Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器執行 SMBus (System Management Bus) 電氣特性驗證,以確保其訊號符合所 定義的電氣特性規格。在經過長時間燒機測試後,可確認待測訊號的電氣特性是否達標。

SMBus 協定的電氣特性檢測方式與 I²C 類似,通常分為兩大類:

- 垂直屬性(電壓)
- 水平屬性(時間/相位)

因此,使用此功能前,須先設定所選協定與規格,並透過反覆測試以取得電氣特性測試報告。測試項目會根據 SMBus 的傳輸速率而有所不同。



SMBus 驗證報告內容:

0	verview [Detail	SMBus								
	Name	De	scription	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result
1	f _{SCL}	SCI	L clock	0.000 Hz	100.000 KHz	3.142 KHz	198.650 KHz	200.008 KHz	13.737 KHz	450	Fail
2	t _{HD,STA}	Hol	d time(4.000 us		2.498 us	2.498 us	2.499 us	234.000 ps	19	Fail
3	t _{su,sta}	Set	-up tim	4.700 us		2.093 us	2.097 us	2.104 us	4.275 ns	6	Fail
4	t _{HD,DAT}	Dat	a hold	5.000 us		118.950 ns	1.242 us	1.374 us	273.845 ns	180	Fail
5	t _{SU,DAT}	Dat	a Set-u	250.000 ns		969.002 ns	1.239 us	2.509 us	326.581 ns	180	Pass
6	tsu,sto	Set	-up tim	4.000 us		2.508 us	2.521 us	2.530 us	6.103 ns	13	Fail
7	tLOW	Low	v Perio	4.700 us		2.450 us	2.638 us	3.749 us	108.381 ns	468	Fail
8	t _{HIGH}	Hig	h Perio	4.000 us		2.062 us	2.094 us	2.107 us	6.704 ns	496	Fail
9	t _{rCL}	Ris	e time		1.000 us	264.997 ns	277.670 ns	306.498 ns	4.317 ns	477	Pass
10	t _{rCL}	Fall	time o		300.000 ns	1.260 ns	1.421 ns	1.598 ns	103.000 ps	556	Pass
11	t _{rDA}	Ris	e time		1.000 us	269.758 ns	277.633 ns	283.758 ns	2.679 ns	118	Pass
12	t _{fDA}	Fall	time o		300.000 ns	997.000 ps	1.383 ns	1.551 ns	121.000 ps	145	Pass
13	t _{BUP}	Bus	s free ti	4.700 us		256.676 us	782.918 us	2.669 ms	944.462 us	10	Pass
14	t _{VD,DAT}	Dat	a valid		3.450 us	110.469 ns	1.380 us	1.655 us	357.855 ns	193	Pass
45	turs area	Det	a valid		2 450 110	ENG 751 pc	0.145.00	0.750.00	100 065 55	07	Daga

電氣特性驗證 軟體畫面:



- 1. 不同的傳輸速率模式,包括 Standard Speed Mode (~100kHz) / Fast Mode (~400kHz) / Fast Mode+ (~1MHz) / HS Mode(~3.4MHz)
- 2. 頻率:時脈速度
- 3. 時序:Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 4. 電壓:V_L, V_H 等



■ SMBus 電氣特性驗證設定

1. 一般設定:設定通道來源、工作電壓與傳輸速率

Settings	
General	Channel Satisan
XDecode	
XValidation	CLK: DSO Channel 1 Probe Settings: x10
	DATA: DSO Channel 2 Probe Settings: x10
	Working Voltage(V _{DD}): 1.80 V
	PDM Clock Speed: 3072 - KHz
Default	Next

2. 解碼設定:設定 SMBus 解碼參數

Settings			
✓General →Decode	Address Mode		
XValidation	7-bit Addressing		
	○ 8-bit Addressing (Including R/W in Address)		
	Startup Settings		
	□ PEC		
	Device		
	MCTP		
	SBS (Smart Battery System)		
	SPD (Serial Presence Detect) DDR4		
Default		Previous	Next



3. 驗證項目設定:包含頻率、時序與電壓限制

eneral ecode	Customized E	V Parameter:		
alidation	Frequen	су		
	Name	Description	Min	Max
	1 ✔ f _{SCL} SCL	clock frequency	0 kHz	100 kHz
	▲ Time			
	Name	Description	Min	Max
	1 ✔ t _{HD,STA}	Hold time(repeated) START condition	4 us	×
	2 ✓ t _{SU,STA}	Set-up time for a repeated START condition	4.7 us	x
	3 ✔ t _{HD,DAT}	Data hold time	5 us	x
	4 ✔ t _{SU,DAT}	Data Set-up time	250 ns	х
	5 ✔ t _{SU,STO}	Set-up time for STOP condition	4 us	х
	6 ✔ t _{LOW}	Low Period of the SCL Clock	4.7 us	х
	7 ✓ t _{HIGH}	High Period of the SCL Clock	4 us	x
	8 🗸 t _{rCL}	Rise time of SCL signal	X	1 us
	9 ✔ t _{fCL}	Fall time of SCL signal	×	300 ns
	10 ✓ t _{rDA}	Rise time of SDA signal	X	1 us
	11 ✓ t _{fDA}	Fall time of SDA signal	×	300 ns
			r	

4. 電氣特性驗證 軟體畫面





5. 控制面板



- A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止
- B. 資訊:選擇查看波形
- C. 储存檔案: 儲存為 HTML 格式 儲存為 .MOW (Acute軟體專用格式)

6. 概覽報告

1 V -3.50 Div			2 1 V -3.0	V 50 Div								H 400 μs T	SMBus Validation Stop S/R: 500 MS/s
	•								- ÷ - † - † -				
*******	1			Muura aire	••••••••••••••••••••••••••••••••••••••		www.weinewiji		, i mene				
								0		0			
SMBus I2C			50 00 50 1 50 00 50 1	0] 0]	50 <mark>12</mark> 50 12			14 16	-	50 18 1A 1C	50 1E 20 22 24 50 1E 20 22 24	50 26 28 24 2C	50 2E 30 32 34 50 2E 30 32 34
1	226.	356 µs	626,856	u <mark>s</mark>	1.0 <mark>27 /</mark> ms		1.427 ms		1.827 ms	2.227 ms	2.627 msum	3.027 ms	3.427 ms 2025-05-13.08
Overview De	etail SMBus												
Name	Description	Limit Min	Limit Max	Min	Mean	Max	ndard Deviat	Count	Result				
1 f _{SCL}	SCL clock	0.000 Hz	100.000 KHz	199.982 KHz	199.995 KHz	200.007 KHz	4.000 Hz	247	Fail				
2 thd,sta	Hold time(4.000 us		2.498 us	2.498 us	2.499 us	131.000 ps	10	Fail				
3 tsusta	Set-up tim	4.700 us		2.083 us	2.083 us	2.083 us	0.000 ps	1	Fail				
4 thildat	Data hold	5.000 us		119.745 ns	479.688 ns	1.372 us	490.528 ns	136	Fail				
5 tsudar	Data Set-u	250.000 ns		974.424 ns	1.872 us	2.509 us	546.814 ns	160	Pass				
5 tsusto	Set-up tim	4.000 us		2.508 us	2.519 us	2.523 us	4.359 ns	9	Fail				
7 Low	Low Perio	4.700 us		2.621 us	2.628 us	2.641 us	3.306 ns	247	Fail				
B thich	High Perio	4.000 us		2.069 us	2.092 us	2.109 us	7.042 ns	272	Fail				
9 ta	Rise time		1.000 us	263.576 ns	278.151 ns	297.576 ns	5.070 ns	315	Pass				
10 ticl.	Fall time o		300.000 ns	1.233 ns	1.411 ns	1.576 ns	103.000 ps	315	Pass				
11 toA	Rise time		1.000 us	270.193 ns	277.390 ns	286.193 ns	3.157 ns	91	Pass				
12 t _{EDA}	Fall time o		300.000 ns	969.000 ps	1.311 ns	1.610 ns	172.000 ps	99	Pass				
13 t _{BUF}	Bus free ti	4.700 us		259.681 us	323.345 us	446.687 us	65.990 us	8	Pass				
14 tyddar	Data valid		3.450 us	111.416 ns	619.060 ns	1.656 us	516.073 ns	145	Pass				
15 typack	Data valid		3.450 us	505.339 ns	2.218 us	2.750 us	822.999 ns	11	Pass				
16 LOW,SEXT	Cumulativ		25.000 ms	2.454 us	2.791 us	4.631 us	479.555 ns	306	Pass				
17 LOWMENT	Cumulativ		10.000 ms	2.454 us	2.791 us	4.631 us	479.555 ns	306	Pass				



7. 詳細報告

1	1 V -3.50 Div			2 1 V -3.9	/ 50 Div									H 400 μs -1.827 ms	SMBus Validation Stop S/R: 500 MS/s
		-	5							-+++					7'
	**************************************								1		0 0				
CMD		lm			01								FO 17 191 99 194		2 '
120)0		30 10 10 1	0	50 12		50	14 16		50 18 LA IC		50 1E 20 22 24	30 26 28 2A 2C	50 2E 30 32 34
1		aut 226.	356 µs	626,856	s	1.0 <mark>27 ms</mark>		1.427 ms	i anni	.827 ms		27 ms	2.627 ms	3.0 <mark>2</mark> 7 ms	3.427 ms 2025-05-13 08:51:5
0	erview De	tail SMBus													
fs	CL t _{HD,STA}	t _{su,sta} t	HD,DAT tsu,DA	r t _{su,sto}	t _{LOW} t _{HIGH}	t _{rol} t _{io}	L t _{rDA} 1	IDA t _{BUF}	t _{VD,DAT} t _{VD}	DACK LOWISE	T tLOWMENT	V _{Los} V	High V _{Max} V _{Min}		
1	Naveform No 1-1	o TimeStamp	START	Address	D0-D7	Limit Min	Limit Max	Min	Mean	Max	Count	Result			
2	1-2	500.337 us	START	50		4.700 us		446.687 us	446.687 us	446.687 us	1	Pass			
3	1-3	549.412 us	RESTART	50	10	4.700 us									
4	1-4	750.716 us	START	50	12	4.700 us		301.538 us	301.538 us	301.538 us	1	Pass			
5	1-5	1.001 ms	START	50	14 16	4.700 us		399.960 us	399.960 us	399.960 us	1	Pass			
6	1-6	1.252 ms	START	50	18 1A 1C	4.700 us		352.884 us	352.884 us	352.884 us	1	Pass			
7	1-7	1.502 ms	START	50	1E 20 22 24	4.700 us		306.308 us	306.308 us	306.308 us	1	Pass			
8	1-8	1.753 ms	START	50	26 28 2A 2C	4.700 us		259.964 us	259.964 us	259.964 us	1	Pass			
9	1-9	2.003 ms	START	50	2E 30 32 34	4.700 us		259.681 us	259.681 us	259.681 us	1	Pass			
10	1-10	2.253 ms	START	50	36 38 3A 3C	4.700 us		259.735 us	259.735 us	259.735 us	1	Pass			

8. 波形和參考點

1 V -3.50 Div			2 1 ¹ -3.	V 50 Div									Η 1 μs -505.32 μs	T SMBus Stop
SMBus 12C)])]	φ	•.••••••••••••••••••••••••••••••••••••	hB.orean constant		4				506.32 µs	<u>-</u> 507.32 µs		sdar(7b): 50 Addr(7b): 50 5(18.32 us.	• • • •
Overview	Detail SMBus						(O a a a						
f. t.	turn t	tere tere				. Ital	t	🞯 Detail						×
f _{SCL} t _{HD.5}	sta t _{SU,STA} t n No TimeStamp	HD,DAT t _{SU,D}	r t _{su,sto} Address	t _{LOW} t _{HIGP}	i t _{rCL} tj	cL t _{rDA}	t _{IDA}		7. 0.				00.07	
f _{SCL} t _{HD,1} Naveform 1 1-1	sta t _{SU,STA} t n No TimeStamp 249.982 us	HD,DAT tsu,DA Status START	rr t _{su,sto} Address	t _{LOW} t _{HIG}	t _{rCL} t _r Limit Min 250.000 ns	CL t _{rDA}	t _{IDA}	Waveform No.	TimeStamp 500.337 us	Status START	Ad	dress 50	D0-D7	
f _{SCL} t _{HD,1} Naveform 1 1-1 2 1-2	sta t _{SU,STA} t n No TimeStamp 249.982 us 500.337 us	START	AT t _{SU,STO} Address 00 50	t _{LOW} t _{HIG}	t _{rCL} t _i Limit Min 250.000 ns 250.000 ns	CL t _{rDA} Limit Max	t _{IDA}	U Detail tsu,DAT Waveform No. 1-2 Time	Time Stamp 500.337 us ∆ Time	Status START Volt	Ad ∆ ∛olt	dress 50 Result	D0-D7	
f _{SCL} t _{HD,6} Naveform 1 1 1-1 2 1-2 3 1-3	stA t _{SU,STA} t n No TimeStamp 249.982 us 500.337 us 549.412 us	START START RESTART	Art t _{SU,STO} Address 00 50 50	t _{LOW} t _{HIGH} D0-D7	t t _{rCL} t _t Limit Min 250.000 ns 250.000 ns 250.000 ns	CL trDA Limit Max	t _{IDA} 97 98	Detail Vaveform No. 1-2 Time 1 (1.005 ms, 1.006 ms)	Time Stamp 500.337 us Δ Time 976.212 ns	Status START Volt (3.5 V, 1.5 V)	Ad ∆∛olt -2 V	dress 50 Result Pass	D0-D7	
fscL t _{HD,3} Naveform 1 1 1-1 2 1-2 3 1-3 4 1-4	STA t _{SU,STA} t n No TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 750.716 us	START START RESTART START	т t _{su.sto} Address 00 50 50 50	t _{LOW} t _{HIGH} D0-D7	t _{rcL} t _i Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns	CL t _{rDA} Limit Max 	t _{IDA} 97 98 97	Tetal tsu,DAT Waveform No. 1-2 1 (1.005 ms, 1.006 ms) 2 1.009 ms, 1.011 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Ad △ Volt -2 V 0 V	dress 50 Result Pass Pass	D0-D7	
fscl. t _{HD.1} Waveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5	tsu.stx t n No TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 1.001 ms 1.001 ms	START START RESTART START START START	v t _{su,sto} Address 50 50 50 50	tLOW tHIGH D0-D7 10 12 14 16	t _{rCL} t ₄ Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns	CL t _{rDA}	t _{⊡A} 97 97 97 97	Tetal tsu,DAT 1-2 Time 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V)	▲ ¥oit -2 V 0 V -2 V	dress 50 Result Pass Pass Pass	D0-D7	
fsci. t _{HD.8} Waveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6	sth tsu.sth tsu.sth n No TimeStamp 249.962 us 500.337 us 549.412 us 750.716 us 1.001 ms 1.252 ms	NODAT TSUDA START START RESTART START START START	 t_{SU,STO} Address 50 50 50 50 	t.cow trace D0-D7 10 12 14 16 18 1A 1C	t _{rCL} t _r Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns	Limit Max Limit Max	t _{IDA} 97 97 97 97 97 97 97	Tetal tsu,DAT 1-2 Time 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)	Time Stamp 500.337 us △ Time 976.212 ns 1.386 µs 976.212 ns 1.382 µs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Δ Volt -2 V 0 V -2 V 0 V	dress 50 Result Pass Pass Pass Pass	D0-D7	
fscl. tHb. Maveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7	Construction Construction struction TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 1.001 ms 1.252 ms 1.502 ms 1.502 ms	HD.DAT t_SU.D. START START RESTART START START START START	t t <tht< th=""> t t t</tht<>	tLow tries D0-D7 10 12 14 16 18 1A 1C 1E 20 22 24	trock t Limit Min 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns 250.000 ns	trDA Limit Max	t _{DA} 97 97 97 97 97 97 97 97 97	Tetal tsu,DAT 1-2 Time 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	△ ¥oit -2 V 0 V -2 V 0 V -2 V 0 V	dress 50 Result Pass Pass Pass Pass	D0-D7	
fscl. tHDJ Maveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7 8 1-8	tausta tausta tausta n No TimeStamp 249.982 us 500.337 us 549.412 us 750.716 us 1.001 ms 1.252 ms 1.502 ms 1.753 ms 1.753 ms	tsup Status START START RESTART START START START START START START	t USUSTO Address 00 50 50 50 50 50 50	tLow trace D0-D7 10 12 14 16 18 1A 1C 1E 20 22 24 26 28 2A 2C	t _{rCL} t Limit Min 250.000 ns 250.000 ns 250.000 ns	trDA Limit Max	t _{IDA} 97 97 97 97 97 97 97 97 97 97	Tetal tsu,Dat 1-2 Time 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Δ Yolt -2 V 0 V -2 V 0 V -2 V 0 V	dress 50 Pass Pass Pass Pass	D0-D7	
fact tab. Maveda 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1-7 8 1-8 9 1-9	трана т	START START START RESTART START START START START START START	tsu.sno Address 00 50 50 50 50 50 50 50 50 50 50 50 50 50	t.cw tesse D0-D7 10 12 14 16 18 1A 1C 1E 20 22 24 26 28 2A 2C 2E 30 32 34	t,cL t, 10mit Min 250.000 ns 250.000 ns 250.000 ns	Limit Max	Image: state	Tetal tsu,DAT Waveform No. 1-2 Time 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Ad △ Yolt -2 V 0 V -2 V 0 V	dress 50 Pass Pass Pass Pass	D0-D7	
International Internatis International International International Internationa	таки таки	tsub. Start	r tausno Address 00 50 50 50 50 50 50 50 50 50 50 50 50	t.cow t.max D0-D7 10 10 12 14 16 18 1A 12 22 24 26 28 2A 22 30 36 38	t_cL t. Limit Min 250.000 ns 250.000 ns 250.000 ns	ton ton timit Max	t _{DA} 97 97 97 97 97 97 97 97 97 97 97 97	Tetal tsu,Dat Waveform No. 1-2 1 <tr< th=""><th>Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs</th><th>Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)</th><th>Δ \[Volt] -2 \(V) 0 \(V) -2 \(V) 0 \(V)</th><th>dress 50 Pass Pass Pass</th><th>D0-D7</th><th></th></tr<>	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Δ \[Volt] -2 \(V) 0 \(V) -2 \(V) 0 \(V)	dress 50 Pass Pass Pass	D0-D7	
Fect turos foct turos Naveform 1 1 1-1 2 1-2 3 1-3 4 1-4 5 1-5 6 1-6 7 1.7 8 1-8 9 1-9 10 1-10	трана (1997) трана (1997) т	taux Status Starts Starts	t tausno Address 50 ↓ 50 ↓ 50 ↓ 50 ↓ 50 ↓ 50 ↓ 50 ↓ 50 ↓	Low Law D0-D7 10 10 11 12 11 14 16 18 1A 12 22 24 26 28 2A 26 30 36 38	Let U Limit Min 250.000 ns 250.000 ns 250.000 ns	tudit tudit Imit Max Imit Imit Imit </th <th>t_{IDA} 97 97 97 97 97 97 97 9</th> <th>Tetal Waveform No. 1-2 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)</th> <th>Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs</th> <th>Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)</th> <th>Δ Volt -2 V 0 V -2 V 0 V -2 V 0 V</th> <th>dress 50 Pass Pass Pass Pass</th> <th>D0-D7</th> <th></th>	t _{IDA} 97 97 97 97 97 97 97 9	Tetal Waveform No. 1-2 1 (1.005 ms, 1.006 ms) 2 (1.009 ms, 1.011 ms) 3 (1.015 ms, 1.016 ms) 4 (1.019 ms, 1.021 ms)	Time Stamp 500.337 us Δ Time 976.212 ns 1.386 μs 976.212 ns 1.382 μs	Status START Volt (3.5 V, 1.5 V) (1.5 V, 1.5 V) (3.5 V, 1.5 V) (1.5 V, 1.5 V)	Δ Volt -2 V 0 V -2 V 0 V -2 V 0 V	dress 50 Pass Pass Pass Pass	D0-D7	



9. Html 報告

A	C	U	ť	e.
PC-ba	sedT	&M In	strur	nents

Electrical Validation Report

Test Instrument Model	MSO3124V
Test Instruments Serial Number	MSV31240017
Test Date	09-21-2023 10:27:35
S/W Version	1.7.59
Protocol	PDM

PDM Testing

Overview Results:

Total: 13 Pass: 13 Fail: 0

Index	Name	Description	Limit Min	Limit Max	Min	Mean	Max	Standard Deviation	Count	Margin Min	Margin Max	Result
1	fclk	Clock frequency	0.000 Hz	3.072 MHz	3.027 MHz	3.030 MHz	3.034 MHz	17.798 KHz	4430	***	-1.2%	Pass
2	LOW	Low Period of the Clock	130.208 ns	195.312 ns	163.008 ns	163.289 ns	163.541 ns	1.399 ns	4920	25.2%	-16.3%	Pass
3	tHIGH	High Period of the Clock	130.208 ns	195.312 ns	163.162 ns	163.428 ns	163.717 ns	1.709 ns	4920	25.3%	-16.2%	Pass
4	4 _{CL}	Rise time of CLK signal		13.000 ns	1.380 ns	1.621 ns	1.859 ns	2.428 ns	4930		-85.7%	Pass
5	4CL	Fall time of CLK signal		13.000 ns	1.412 ns	1.661 ns	1.862 ns	2.529 ns	4930		-85.7%	Pass
6	4DD	Delay time from Clk edge to Data Fall driven	40.000 ns	80.000 ns	57.382 ns	64.017 ns	74.913 ns	77.763 ns	2500	43.5%	-6.4%	Pass
7	t _{fDV}	Delay time from Clk edge to Data Fall Valid		100.000 ns	60.111 ns	67.555 ns	79.252 ns	83.904 ns	2500		-20.7%	✓Pass
8	trop	Delay time from Clk edge to Data Rise driven	40.000 ns	80.000 ns	54.659 ns	60.684 ns	71.123 ns	67.169 ns	2440	36.6%	-11.1%	Pass
9	trDV	Delay time from Clk edge to Data Rise Valid		100.000 ns	57.573 ns	64.149 ns	75.158 ns	71.543 ns	2440		-24.8%	Pass
10	VCIkLow	Low-level input voltage for clock	-500.000 mV	540.000 mV	-56.786 mV	-50.438 mV	-42.405 mV	49.004 mV	4920	-88.6%	-107.9%	Pass
11	VDataLow	Low-level input voltage for Data	-500.000 mV	540.000 mV	-55.069 mV	-49.177 mV	-35.569 mV	51.321 mV	2467	-89.0%	-106.6%	Pass
12	VClkHigh	High-level input voltage for clock	1.260 V	2.300 V	1.825 V	1.835 V	1.850 V	93.739 mV	4930	44.8%	-19.6%	Pass
13	VDataHigh	High-level input voltage for Data	1.260 V	2.300 V	1.499 V	1.515 V	1.531 V	77.266 mV	2467	19.0%	-33.4%	Pass

f_{CLK} - Test Result: Pass Description: Clock frequency

Limit Min Limit Max Min Mean Ma	ax Standard Deviation Count	Margin Min Margir	Max	
0.000 Hz [3.072 MHz]3.027 MHz[3.030 MHz]3.034	Histogram	1.2%		
	mstogram	Makua Passaa	Occurance Count	
Occurance (%), Total 4430		value range	Occurance Counc	
100 -		3.027 MHz ~ 3.028 MHz	13	
90		3.028 MHz ~ 3.028 MHz	70	
70 -		3.028 MHz ~ 3.029 MHz	298	
60 - 50 -		3.029 MHz ~ 3.03 MHz	813	
40 33.0		3.03 MHz ~ 3.03 MHz	1454	
30 24.2 20 18.4 11.0		3.03 MHz ~ 3.031 MHz	1073	
10 0.3 1.6 6.7	3.0 0.6 0.2 Test Value	3.031 MHz ~ 3.032 MHz	529	
3.027 MHz	3.034 MHz	3.032 MHz ~ 3.032 MHz	135	
Test Value		3.032 MHz ~ 3.033 MHz	27	
Limit	3.072 MHz	3.033 MHz ~ 3.034 MHz	8	
Min	Detail Report Row: 1, Tes	st Index: 340 Ma:	x	Detail Report Row: 3, Test Index: 431
500 mV 2 500 mV -3.50 -3.50	100 ns -112.198 µs T PDM Validation Step S/R: 500 l	MS/s	500 mV -3.50 -3.50	100 ns -142.228 ps PDM Validation Stop <u>S/R: 500 MS/s</u>



SPI 電氣特性驗證解決方案

File / Settings	Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation)pen / File						

使用示波器執行 SPI (Serial Peripheral Interface) 電氣特性驗證,以確保其訊號符合所定義 的電氣規格。在經過長時間燒機測試後,可確認待測訊號的電氣特性是否達標。



■ SPI 電氣特性驗證設定

1. 一般設定:根據匯流排配置選擇 SPI 類型(4-wire SPI 或 3-wire SPI)。

Settings							Import	Export
→General	Channel	Settings						
XTrigger XValidation	Type: SCLK: CS:	4-wire SPI DSO Channel 1 DSO Channel 2	 Probe Settings: Probe Settings: 	x10 • x10 •				
	SDI: SDO:	DSO Channel 3	 Probe Settings: Probe Settings: 	x10 -	x10 >			
	Working	g Voltage(V _{DD}): 3.30 V	* *					
Default								Next

4-wire 設定:

Channel S	Settings			
Type:	4-wire SPI	•		
SCLK:	DSO Channel 1	Probe Settings:	x10	▼ 10
CS:	DSO Channel 2	Probe Settings:	x10	
SDI:	DSO Channel 3	Probe Settings:	x10	
SDO:	DSO Channel 4	Probe Settings:	x10	▼ 10 × 10 × 10

3-wire 設定:

Settings								
3-wire SPI	Ŧ							
DSO Channel 1	•	Probe Settings:	x10	- x10	-			
DSO Channel 2	¥	Probe Settings:	x10	- x10	>			
DSO Channel 3	•	Probe Settings:	x10	x10	•			
	Settings 3-wire SPI DSO Channel 1 DSO Channel 2 DSO Channel 3	Settings 3-wire SPI • DSO Channel 1 • DSO Channel 2 • DSO Channel 3 •	Settings 3-wire SPI DSO Channel 1 Probe Settings: DSO Channel 2 Probe Settings: DSO Channel 3 Probe Settings:	Settings 3-wire SPI DSO Channel 1 Probe Settings: x10 SO Channel 2 Probe Settings: x10 SO Channel 3 Probe Settings: x10 X10 So Channel 3 Probe Settings: x10 So Channel 3 Probe Settings: x10 So Channel 3 Probe Settings: x10 So Channel 3 Probe Settings: x10 So Channel 3 So Channel 4 So Channel 4 S	Settings 3-wire SPI DSO Channel 1 Probe Settings: x10 x10 DSO Channel 2 Probe Settings: x10	Settings 3-wire SPI DSO Channel 1 Probe Settings: x10 SO Channel 2 Probe Settings: x10 Probe Setti	Settings 3-wire SPI DSO Channel 1 Probe Settings: x10 Probe Settings	Settings 3-wire SPI DSO Channel 1 Probe Settings: x10 Probe Settings



2. 解碼設定:設定 SPI 的資料格式以及各個通道的 Latching Edge。這裡所設

Cottingo				Import Export	
✓General	4 with ODI				
 Decode Trigger Validation 	Chip Select Edge SDI Edge SDO Edge	Active Low Rising Falling			
	Data Format				
	Bit Order	MSB First 👻			
	Word Size	8 bits			
Default				Previous Next	

定的 SPI 資料格式會同時套用至解碼與觸發設定中。

3. 觸發設定:資料格式已在上一頁設定完畢。本部分剩下的設定重點是資料

					Import	Export
Settings						
✓General	Trigger on					
 Trigger 	Data Pin:	Data In - SDI	•			
XValidation	Data					
	Fixed	Offset 0		Byte(s)		
	Data 1	XXh	Data 5	XXh		
	Data 2	XXh	Data 6	XXh		
	Data 3	XXh	Data 7	XXh		
	Data 4	XXh	Data 8	XXh		
Default					Previous	Next

位址與要觸發的資料腳位。



4. 驗證參數設定

code	Customized EV	Parameter:		
gger	Frequen	cv		
lidation	Name	Description	Min	Max
	1 ✔ f _{SCLK} SCL	K Clock Frequency	0 MHz	10 MHz
	∠ Time			
	1 Vame	Description	5 ns	X
	2 ✓ t _{HD,SDI} S	DI Hold Time	15 ns	x
	3 🗌 t _{DIO} S	SDI Output Delay Time	x	X
	4 ✔ t _{su,spo} S	SDO Setup Time	5 ns	x
	5 ✓ t _{HD,SDO} S	SDO Hold Time	5 ns	x
	6 ✔ t₀ S	SDO Output Delay Time	х	6 ns
	7 ✓ t _{HIGH} S	SCLK Clock High Time	5 ns	x
	8 ✔ t _{LOW} 5	SCLK Clock Low Time	5 ns	x
	9 ✔ t _{su,cs} 0	CS Chip Select Setup Time	5 ns	x
	10 ✓ t _{HD,CS} C	CS Chip Select Hold Time	20 ns	x
	11 ✔ t _{cs} 0	Chip Select Deselect time (Chip Select High Time)	50 ns	x

由於 SPI 匯流排並未有官方標準的測量門檻,因此在進行驗證時,請使用者自行定義合適的參數限制。

本區塊顯示三項特性參數表,包括:

- 頻率
- 時序參數
- 電壓需求

所有支援的驗證參數項目與說明如下:



SPI Frequency Requirements

Symbol	Electrical Parameter
f _{SCLK}	SCLK Clock Frequency

SPI Timing Requirements

Symbol	Electrical Parameter
t _{su,sdi}	SDI Setup Time
t _{HD,SDI}	SDI Hold Time
t _{DIO}	SDI Output Delay Time
t _{su,sdo}	SDO Setup Time
thu,sdo	SDO Hold Time
to	SDO Output Delay Time
t _{нібн}	SCLK High Time
t _{LOW}	SCLK Low Time
t _{su,cs}	CS Chip Select Setup Time
t _{su,cs}	CS Chip Select Hold Time
t _{cs}	Chip Select Deselect time (Chip Select High Time)
t _{CLKr}	SCLK Clock Rise Time
t _{CLKf}	SCLK Clock Fall Time

SPI Voltage Requirements

Symbol	Electrical Parameter
V _{IL}	Low-Level Input Voltage
VIH	High-level Input Voltage
V _{OL}	Low-level Output Voltage
V _{OH}	High-level Output Voltage



UART 電氣特性驗證解決方案

■ 簡介:

File / Setting	s Display	Measurement & Analysis	Electrical Validation	Cursor	Acquire	Utility	
EV Electrical Validation	Open EV File						

使用示波器進行 UART 電氣特性驗證,以確認 UART 是否符合所定義的規格。在長時間 燒機測試之後,可驗證被測訊號的電氣特性是否達標。

對於協定的電氣驗證, UART 協定的電氣特性檢測通常分為兩種: **垂直(電壓)與水平** (時間/相位)。

因此,使用本功能前,需先設定協定類型與規格,然後重複測試以獲得電氣特性測試報告。測試項目會依 UART 傳輸速率不同而有不同的規格與標準。



UART 驗證報告:

Overview Detail UART(RS232)										
	Name	Description	Limit Min	Limit Max	Min	Mean	Max	andard Deviati	Count	Result
1	f _{UART}	Baud rate	-0.5 %	0.5 %	0.0 %	0.0 %	0.1 %	0.0 %	32	Pass
2	VLow	Low-level i	-7.200 V	-8.800 V	-8.759 V	-7.541 V	0.000 uV	16.920 V	104	Fail
3	V _{High}	High-level i	7.200 V	8.800 V	8.541 V	8.553 V	8.613 V	61.598 mV	32	Pass

電氣特性驗證_軟體頁面:



- 1. 頻率:時脈速率
- 2. 時序: Set-up Time / Hold Time / Rise Time / Fall Time & Clock Stretching Timing limitation
- 3. 電壓:V_L, V_H, etc.



■ UART 電氣特性驗證設定

1. 一般設定:通道來源、工作電壓與傳輸速率

Settings Channel Settings Channel 1 Probe Settings: X1 Votage High(Vi _{iii}): 5:00 Baud Rate 9600 P bps			· · ·	J	
Channel Settings Data: DSC Channel 1 Probe Settings: X0 Validation Value Bacd Rate e600 Default Default Nett Nett	Settings				
Chamel Settings Data: DSO Chamel 1 Probe Settings: Voltage High(V _{trad}): 5:00 V Baud Rate 9600 Default Default Nett	General				
Data: DBO Channel 1 Probe Settings: Voltage High(Vitug): 5.00 V () Baud Rate 9600 P bps	*Decode	Channel Settings			
Default Next	XValidation	Data: DSO Channel 1 - Probe Settings: x10 - x10 -			
Baud Rate		Voltage High(V _{tligh}): 5.00 V ♦ Voltage Low(V _{Low}): -5.00 V ♦			
Default		Baud Rate			
Default		9600 v bps			
Default					
	Default			Next	

2. 解碼設定: UART 解碼設定

eungs				
General	Format			
Velidation	Data Bits	Polarity		
Validation	8	▼ Idle High	•	
	Parity	Stop Bits		
	None	▼ 1	•	
	MSB First Inv Report Size: 16 -	ert Bits		



3. 驗證參數設定:頻率、時序與電壓限制

Validation	⊿ Baud Rate		
	Name Description	Min	Max
	1 Junit Baud rate for UART	-0.5 %	0.5 %
	⊿ Time		
	Name Description	Min	Max
	1 t _r Edge rise time	X	X
	2 t _f Edge fall time	X	X
	3 ☑ t _{righ} High time	98.958 µs	109.375 µs
	4	98.958 µs	109.375 µs
	✓ Voltage		
	Name Description	Min	Max
	1 ✓ V _{Low} Low-level input voltage	-4.5 V	-5.5 V
	2 ✓ V _{High} High-level input voltage	4.5 V	5.5 V

4. 電氣特性驗證 軟體畫面





5. 控制面板



- A. 停止條件: 當擷取達到 X 次時停止 當測試結果失敗超過 X 次時停止
- B. 資訊:選擇查看波形
- C. 储存檔案: 儲存為 HTML 格式 儲存為 .MOW (Acute軟體專用格式)

6. 概覽報告





7. 詳細報告



8. 波形和参考點





9. Html 報告

Acute.		
	Electrical Valida	tion Report
	Test Instrument Model	MS03124V er MSV31240017
	Test Date S/W Version	04-27-2023 15:07:32
	Protocol	UART(RS232)
Overview Results:		
Total: 3 Pass: 2 Fail: 1		
Index Name Description Limit Min Limit Max Min Mean M	ax Standard Deviation Count Margin Min Margin I	Max Result
I Fugar Baud rate for UART -0.5 % 0.5 % 0.0 % 0.0 % 0.1 2 VLow Low-level input voltage -7.200 V -8.800 V -8.759 V -7.541 V 0.0	% 0.0 % 32 -100.0% -80.0% 0 uV 16.920 V 104 21.7% -100.0%	vPass → ¥Fail
3 VHigh High-level input voltage 7.200 V 8.800 V 8.541 V 8.553 V 8.6	3 V 61.598 mV 32 18.6% -2.1%	✓Pass
V _{Low} - Test Result: Fail Description: Low-level input voltage Emmit Mini Limit Maxi Mini Mean Maxi Standard Deviation Count Margin Mini Terroru La Rovi 7 a stavi 7 a stavi 7 a stavi 0 and 6 son v	argin Max	
Histogram	0000	
Occurate (%), 164 102 We 100	Range Decemanos Count 3633 V 88 7.002 V 8 6.025 V 8 6.025 V 8 6.025 V 8	
30	-3.504 V 0	
10 Test Value -3.504	/~-2.628 V 0	
-8.759 V 0.000 eV -2.628	(~-1.752 V 0	
-8.759 V (21.7%) 0.000 uV (-100.0%) -1.752 Limit -7.200 V -8.800 V -8.800 V	/~-876 mV 0 /~0 V 14	
Min Detail Report Row: 18, Test Ir	dex: 2 Max	Detail Report Row: 16, Test Index: 2
		2 2 2 m Variation Va



HTML 報告匯出

■ 簡介

每次 EV 測試皆支援匯出 HTML 報告。HTML 報告包含每個測試項目、測試

結果、最大/最小值、長條圖與波形截圖。

🐻 另存為 HTML	×
C:\Users\sam\OneDrive\文件/Acute/MS3K//EV_Report	瀏覽
報告標題 Bectrical Validation Report	
儲存設定	
將 HTML 儲存為: 不合併 ▼ 設定用戶標誌 不合併	瀏覽
□ 附加用戶資訊	
進階設定 OK	Cancel

儲存設定:

A. 將 HTML 儲存為:不合併/合併

不合併:圖片會與 HTML 分開儲存。

合併:圖片會嵌入在 HTML 檔案中(單一檔案)。

B. 設定用户標誌 Logo:

勾選後可選擇圖片檔作為報告中的公司/用戶標誌。

C. 附加用戶資訊:

可在此輸入任何想要加入到報告中的補充說明或使用者資訊。



進階設定:

	Name	User-Defined Name	Mag. Min	Mag. Max		f _{SCL} User Defined Name:
1	f _{SCL}		1	1		
2	t _{HD,STA}		1	1		
3	t _{su,sta}		1	1		Magnification Minimum Im
4	t _{HD,DAT}		1	1		x1
5	t _{SU,DAT}		1	1		Magnification Maximum II
6	tsu,sto		1	1		x1
7	tLow		1	1		
8	thigh		1	1	•	Apply

A. 使用者可自訂測試項目於 HTML 報告中的顯示名稱

B. 使用者亦可調整 HTML 報告中圖片的顯示倍率



進階設定

■ 簡介

EV 测试允許使用者根據每次擷取的需求,調整預設的擷取時間。由於不同的協定有不同的預設時脈或傳輸速率,這些差異主要來自於協定的傳輸速度與 封包長度的不同。有時候,為了更準確地分析資料,可能需要擷取更長的封 包。因此,Acute 提供了 進階設定 功能,讓使用者可以個別調整各項參數 的擷取時間。

*僅在進入 EV 參數設定 時,才會顯示 進階設定 按鈕



EV 進階設定:





MSO/TS3000 系列多機堆疊

■ 簡介

Acute MSO3K / TS3K示波器的特點之一是其多機組合堆疊功能,這使得最多可 堆疊16台示波器,同時實現64通道最高250MS/s,或是16通道最高1GS/s的量 測能力。在機殼設計方面,MSO3K / TS3K專為堆疊應用而設計,具備精心設計 的定位導槽,使示波器在堆疊配置中能夠完美擺放。此外,示波器的散熱性 能也得到了充分考慮,配置了雙側散熱孔,確保長時間運行時不會出現過熱 問題。

在訊號連接方面,使用者可以選擇直接將待測訊號通過標準BNC接頭連接到示 波器,或者使用被動探棒或差動探棒進行更廣泛性的量測。此外,Acute還提 供了BNC to Probe Tip Adaptor,可以改善傳統探棒在連接上常見的量測連接品 質問題,確保用戶獲得最準確的測量結果。



■ 軟體畫面

1. 64Channel @ 250MS/s



2. 16Channel @ 1GS/s







1. 訊號線直接透過BNC to BNC接頭連接



2. 搭配被動探棒量测




3. 搭配被動探棒以及BNC to Probe Tip Adaptor量测



4. 搭配高壓差動探棒量測









■ 注意事項

- MSO3K / TS3K 示波器為 USB3.0 介面的儀器,運作時需消耗 4.5~7.7W,使 用時建議連接至電腦後方的 USB3.0 插槽或是使用具有獨立供電的 USB3.0 hub,以提供最佳的電力供應及最佳量測性能。
- MSO3K / TS3K 示波器經過內部測試,在堆疊狀態下仍可保持長時間運作不 致過熱,但若長時間於高溫或不利於散熱環境使用時,仍須注意示波器使 用溫度並適度提供額外散熱方式,以避免示波器過熱 (>80 度 C) 而影響操 作。



 3. 多機堆疊時,各機器間根據取樣率不同,會產生一定程度的相位差,以 1GS/s 取樣率為例,主機和第一台從機間的相位差為 <±2ns,和最後一台 從機間的相位差為 <±3ns。







主機和最後一台從機(16th)的相位差

1	500 mV +0.00 5	500 mV +0.00 9	500 mV +0.00 13 500 +0.0	mV17 500 mV21 00 17 +0.00 21	500 mV +0.00 25 500 mV +0.00	29 500 mV 500 m +0.00 33 +0.00	500 mV 5 +0.00 41 +	600 mV 45 5	00 mV 500 m\ 0.00 +0.00	53 500 mV +0.00 57	500 mV +0.00 ⁶¹	500 mV H 10 n +0.00 H +0 s	is Trig'd S/	11 mV R: 1 GS/s
	@:-722 p: ∆:6.468 n	ŝ						- -						
									\sim					
1		****	0.0000		00004-0000	000000000	*******			000000			0000000	
								-						