Acute®
PC-based T&M Instruments

BF7264B MIPI D-PHY analyzer

Feature:

The BF7264B is an MIPI D-PHY analyzer and offers other protocol analyzer options like eMMC5, NAND flash, SD3, or SD4 as its predecessor, the BF6264B.

Specifications:

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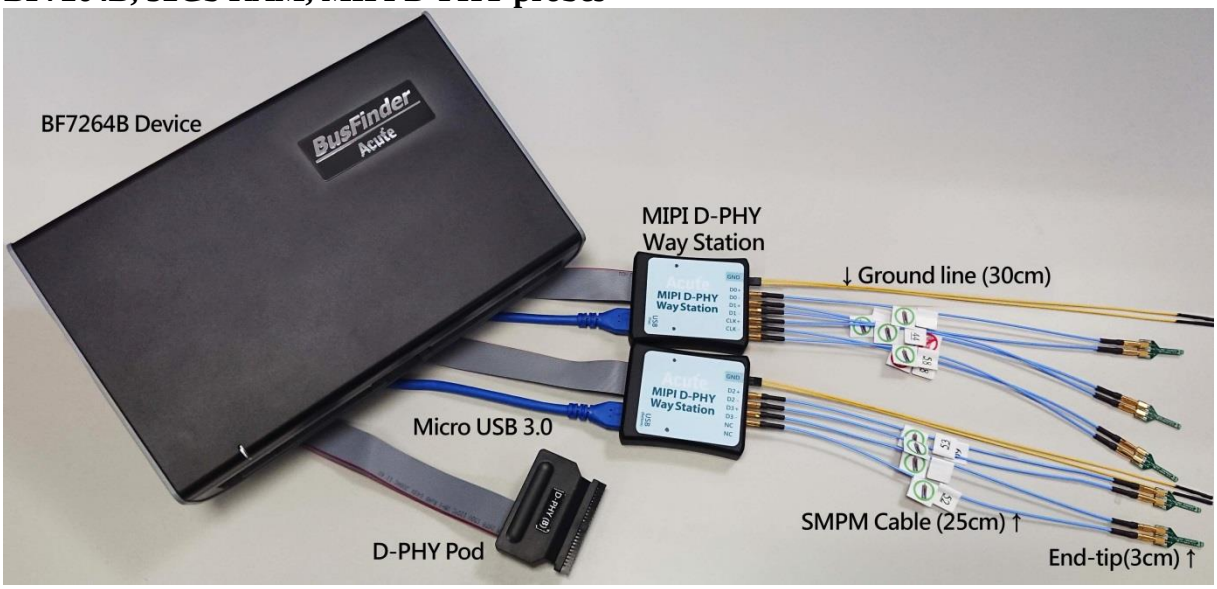
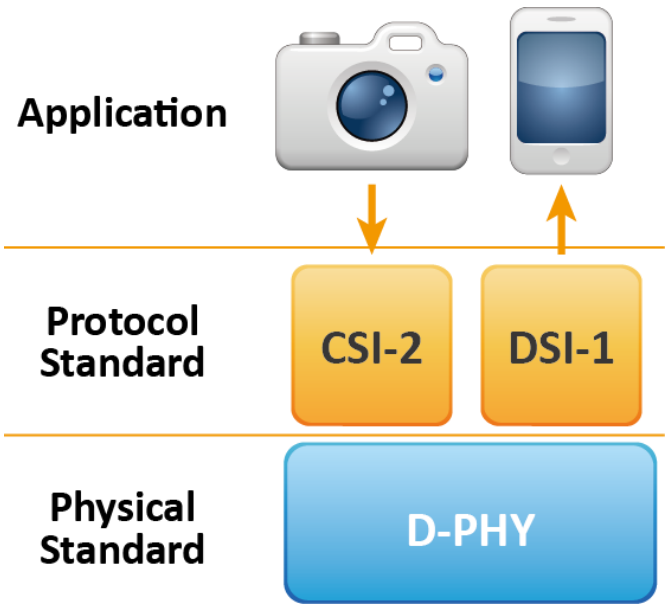
1. BF7264B, 32Gb RAM, MIPI D-PHY probes



2. supports D-PHY V1.2

Up to 2.0Gbps per lane, 1 + 4 Lanes



3. **CSI-2 1.3 or DSI 1.3 protocol packets displayed as below with the DSI DCS 1.3 commands**

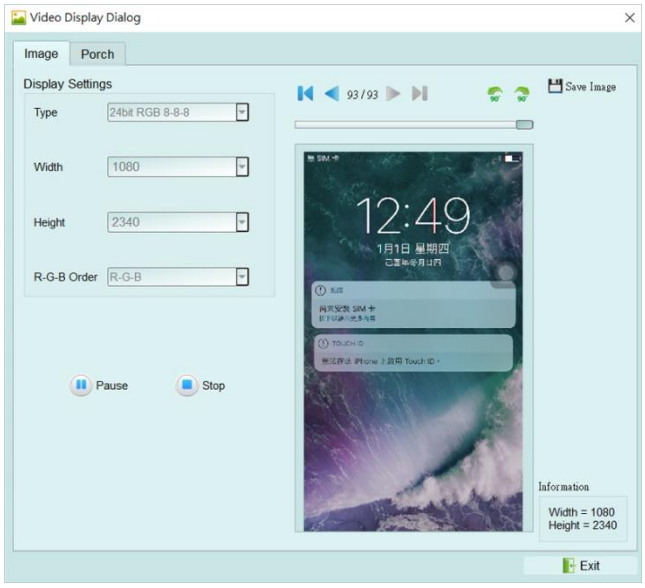
	Timestamp (h:mm:ss.ms.us.ns dur)	Mode	VC	Data Type	DCS (h)	WC	Data (h)	Transaction Type	ECC (h)	CRC (h)
10	10.637.049.8…	LP (LPDT)	0	Generic Long Wri…		2	B0 03	Host proces…	00 (OK)	F84D (OK)
11	10.637.060.1…	LP (LPDT)	0	DCS Short WRITE,…	53 (write_control_display)		24	Host proces…	08 (OK)	
12	10.637.066.5…	LP (LPDT)	0	DCS Short WRITE,…	35 (set_tear_on)		00	Host proces…	2F (OK)	
13	10.637.083.3…	LP (LPDT)	0	Generic Long Wri…		2	B0 04	Host proces…	00 (OK)	8CF2 (OK)
14	10.637.105.0…	LP (LPDT)	0	Generic Long Wri…		3	EB 00 83	Host proces…	1A (OK)	AFA7 (OK)
15	10.637.124.2…	LP (LPDT)	0	Generic Long Wri…		2	FB 00	Host proces…	00 (OK)	6818 (OK)
16	10.637.179.2…	LP (LPDT)	0	Generic Long Wri…		20	C8 01 00 04 FB FC CD 00...	Host proces…	19 (OK)	B76A (OK)
17	10.637.196.0…	LP (LPDT)	0	Generic Long Wri…		2	D6 01	Host proces…	00 (OK)	EADA (OK)
18	10.637.208.8…	LP (LPDT)	0	Generic Long Wri…		2	B0 03	Host proces…	00 (OK)	F84D (OK)
19	10.637.219.1…	LP (LPDT)	0	DCS Short WRITE,…	11 (exit_sleep_mode)		00	Host proces…	36 (OK)	
20	10.837.205.4…	LP (LPDT)	0	DCS Short WRITE,…	29 (set_display_on)		00	Host proces…	1C (OK)	
21	10.870.540.9…	LP (LPDT)	0	DCS Short WRITE,…	51 (set_display_brightness)		FE	Host proces…	0D (OK)	
22	10.870.560.9…	LP (LPDT)	0	DCS READ, no par…	DA		00	Host proces…	1F (OK)	
23	10.870.562.6…	BTA								
24	10.870.571.3…	LP (LPDT)	0	DCS Short READ R…			E1 00	Peripheral …	27 (OK)	
25	10.870.573.4…	BTA								
26	10.897.116.1…	HS	0	DCS Long Write/w…	2C (write_memory_start)	2881	DC AC AA 9A 5A DC DE D2...	Host proces…	04 (OK)	
27	10.897.116.1…	HS	0	End of Transmiss…			0F 0F	Host proces…	01 (OK)	
28	10.897.134.6…	HS	0	DCS Long Write/w…	3C (write_memory_continue)	2881	CA 1B CC EC 7A 5C 55 D2...	Host proces…	04 (OK)	
29	10.897.134.6…	HS	0	End of Transmiss…			0F 0F	Host proces…	01 (OK)	
30	10.897.153.2…	HS	0	DCS Long Write/w…	3C (write_memory_continue)	2881	CA FD C2 CF F1 B0 3B 77...	Host proces…	04 (OK)	
31	10.897.153.2…	HS	0	End of Transmiss…			0F 0F	Host proces…	01 (OK)	
32	10.897.171.7…	HS	0	DCS Long Write/w…	3C (write_memory_continue)	2881	3A 62 52 93 5E 8A 1B 77...	Host proces…	04 (OK)	
33	10.897.171.7…	HS	0	End of Transmiss…			0F 0F	Host proces…	01 (OK)	
34	10.897.190.2…	HS	0	DCS Long Write/w…	3C (write_memory_continue)	2881	BA 15 C3 CF E5 B8 1E 6D...	Host proces…	04 (OK)	

4. **Use 32Gb RAM as the buffer to stream all D-PHY data into the SSD HD in order to record all data flow from Low Power Mode to High Speed Mode**

Recordable data without streaming into the SSD HD:

Resolutions	Recordable frames	Note
1K (FHD 1080x1920)	~500	
2K (WQHD 1440x2560)	~280	
4K (UHD 2160x3840)	~120	8 lanes or 4 lanes with DSC compression
8K (4320x8192)	Not available	Not available

5. **“Data Filter” filters unwanted video data to save memory**
6. **“Search” searches specific data**
7. **“ECC/CRC Packet” displays and counts ECC and CRC**
8. **Display DSI(CSI) image data including RGB, YCbCr, RAW format or compressed DSC packets, and count the Porch from raw data. For more information, please refer to Appendix 2.**



9. D-PHY command statistics include numbers of packets, individual command, different data length, and errors

Discription	Txns	Bytes
Sampled Bus Error	2455	
DSI Error Report	0	
DSI Bus		
VC 0	1044640	29739051
VC 1	18	37
VC 2	245	493
VC 3	499	628
BTA	14	
Data Type	1044899	29740212
DCS Command	521835	28694276
Packet Count	1044900	

Statistics	Txns	Bytes
5E (set_CABC…	1	1
55 (write_pow…	2	4
53 (write_cont…	1	1
35 (set_tear_on)	1	1
11 (exit_sleep_…	1	1
29 (set_displa…	1	1
51 (set_displa…	1	1
DA	1	1
2C (write_me…	407	22385
3C (write_me…	521293	28670727
20 (exit_invert…	3	129
78	2	86
1E	2	86
60	2	44
80	1	43

10. D-PHY command trigger

a. Trigger parameters include commands and 32 bytes data in order to cover all short packets and most of non-video long packets.

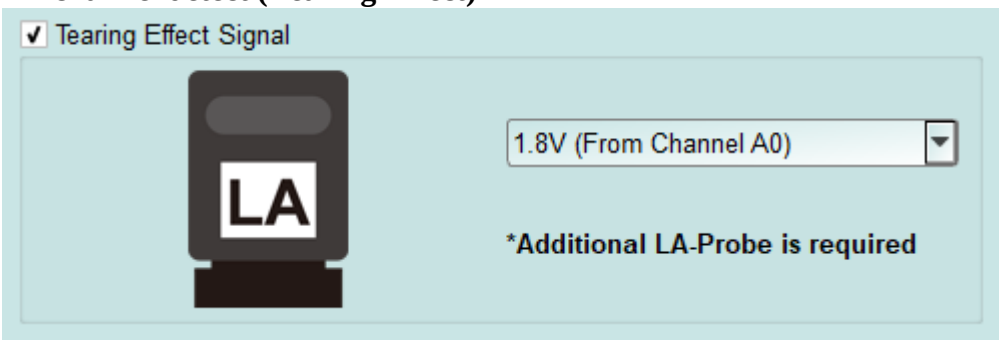
Short Packet: 4-bytes Header

Long Packet: 4-bytes Header + 28-bytes Data

b. CRC/ECC error trigger

c. The Trigger-Out port is to trigger a DSO to capture waveforms

11. TE channel detect (Tearing Effect)



Detect the TE signal from the screen. Must purchase LA Probe to use this function. Please refer to Appendix 1 for details.

FAQ

Q1. What MIPI DSI version is supported, any limitation for differential ports?

A: D-PHY V1.2, up to 2.0Gbps per lane, 1 + 4 lanes.

Q2. Is C-PHY supported?

A: No. Not now or in the future.

Q3. Is DSI-2 supported?

A: No, DSI-2 includes C-PHY signal which is not supported in this solution, the VDC-M image compression/decompression in DSI-2 is also not supported.

Q4. Will signal quality be affected while measuring?

A: Yes, that is why the end-tips and the SMPM coaxial cables are used to minimize the affections of signal quality.

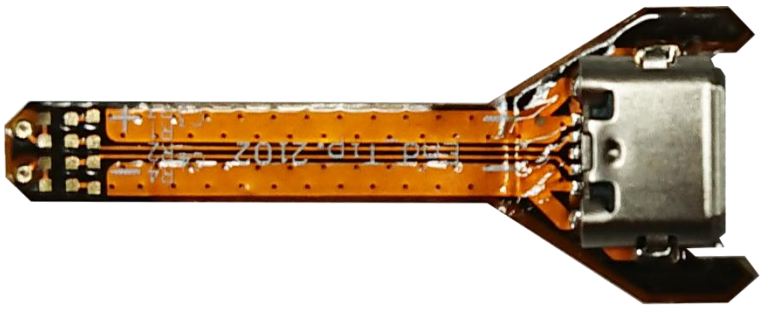
Q5. Is Tx supported?

A: No.

Q6. How to connect the probes with the DUT?

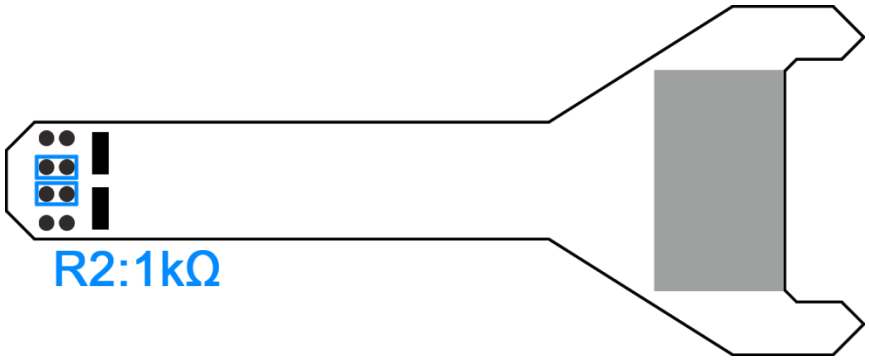
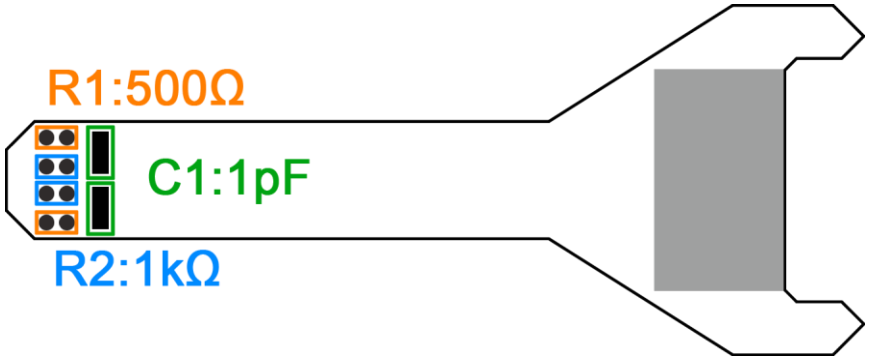
A：①Weld the DUT:

FPC End-tip:



(Do not bend excessively to avoid internal open circuit of the FPC)

Solder R1, R2 to the corresponding resistor in the table, and C1 to the corresponding capacitor, and follow the PCB End-tip steps to complete the connection with the DUT

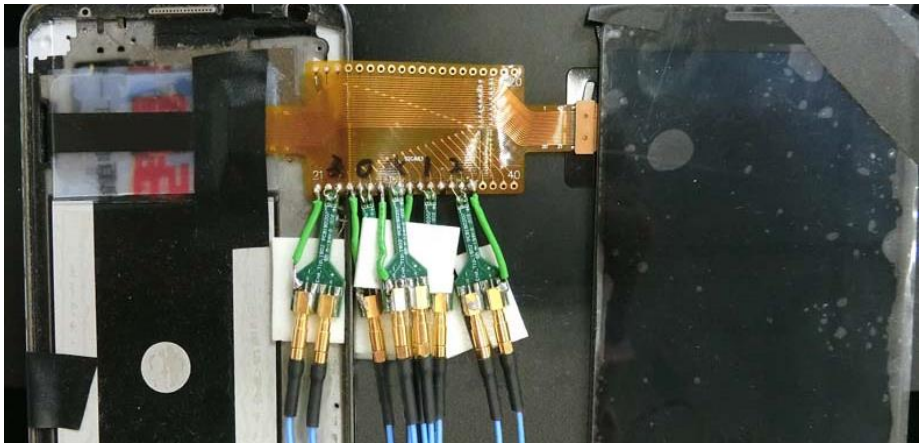
CLK	FPC End Tip
< 800Mhz	
>= 800Mhz	

PCB End-tip:

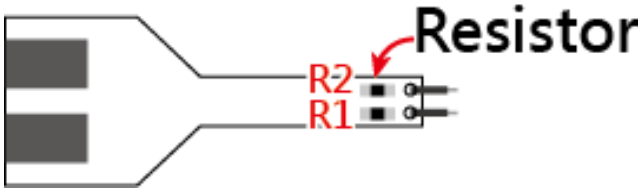
The welding line MUST be < 5mm.
On the DUT, you are highly recommended to weld a 100Ω resistor and connect it to the End tip with a 3cm line.

Step 1: Connect the SMPM-SMPM cable to the End-tip first.

Step 2: Weld the End-tip to the DUT after Step 1.



※ End-tip R1/R2 resistor is 1kΩ/0402 which can be replaced if it breaks.



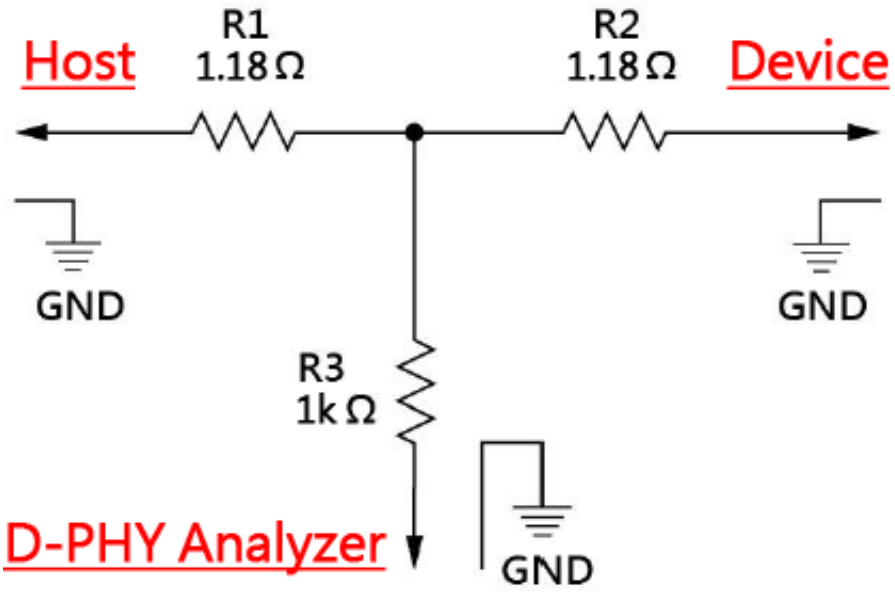
②2.0mm pin header (PH): though easier to use, but will lead to lower signal quality due to stub effect.

Weld 1kΩ resistor on the DUT, then the pin socket; Weld the PH on the End-tip and short the End-tip's 1kΩ resistor to lower the stub effect.

Note: Use hot melt adhesive to reinforce the End-tip.

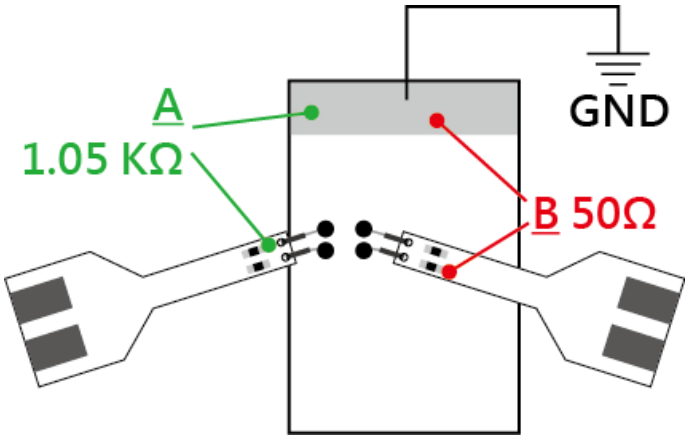
③User-tip：User can design his own End-tip with 1kΩ resistor to connect the DUT, then use the 50Ω impedance PCB trace to plug the SMPM connector.

④Breakout: User can design his own EV board with the SMPM connector to connect Acute MIPI D-PHY analyzer by breaking out the D-PHY host and device on the PCB board as the chart below. R1/R2/R3 must be as close as possible by using 50Ω impedance.



Q7. Use multimeter to check the short circuit.

After connections as below.



Check point **A**: End-tip resistor front to ground, green line ==> no sound from a multimeter.

Check point **B**: End-tip resistor back to ground, red line ==> sound from a multimeter, any short circuit?

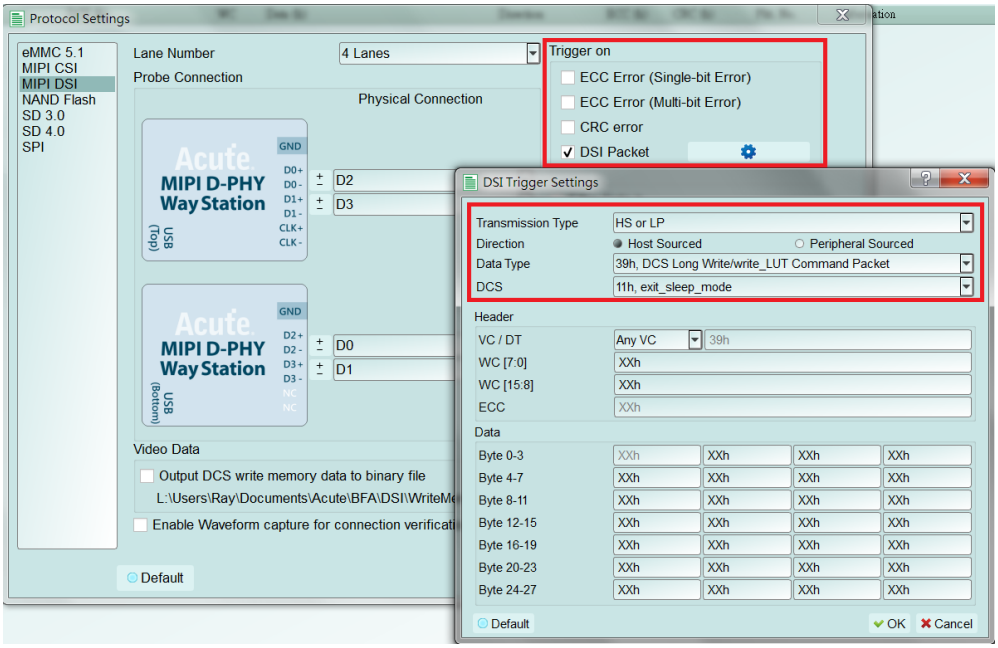
A sound from a multimeter at point **B** is normal because it is low impedance of 50Ω at the resistor back. So, there is no short circuit if the resistor front of 1.05 KΩ without any sound.

Q8. How to connect the ground?

Two ways to connect the ground: End-tip or Way Station. It is better connect the End-tip ground to the DUT ground to have the better quality; but the user may the use to Way Station ground for convenience but to have lower quality signal.

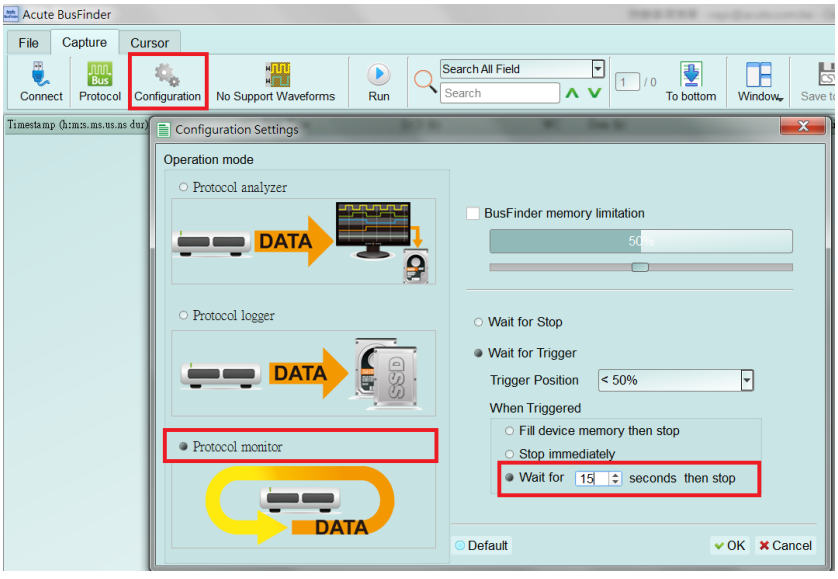
Q9. Is DSI/CSI Data Type or Data trigger supported?

A: Yes, Data Type, DCS Command and Data trigger are supported by BF7264.



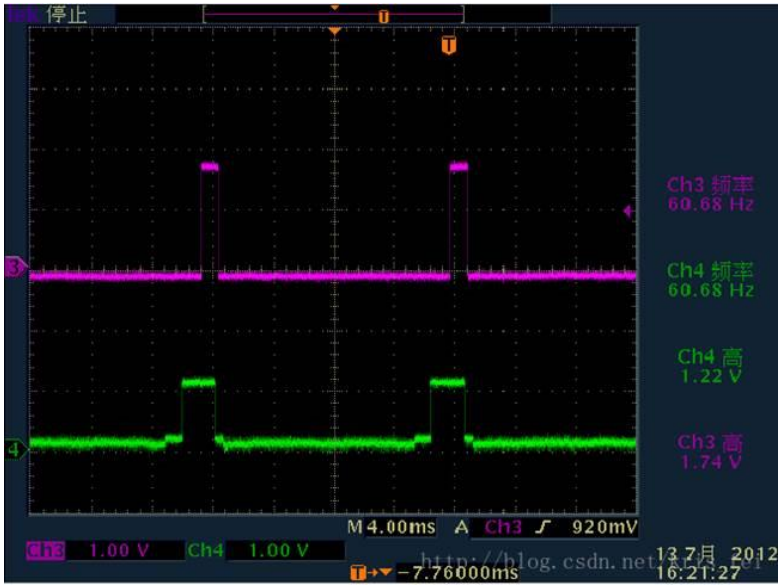
Q10. Is that possible to setup a HS, LP or DCS command as a start condition and then capture data within specified time range?

A: Yes, after setup the HS, LP or DCS in the trigger settings as start condition, move to Configuration and change the operation mode to Protocol Monitor mode, then you can specify the required capture time range.



Appendix 1: Tearing Effect Signal

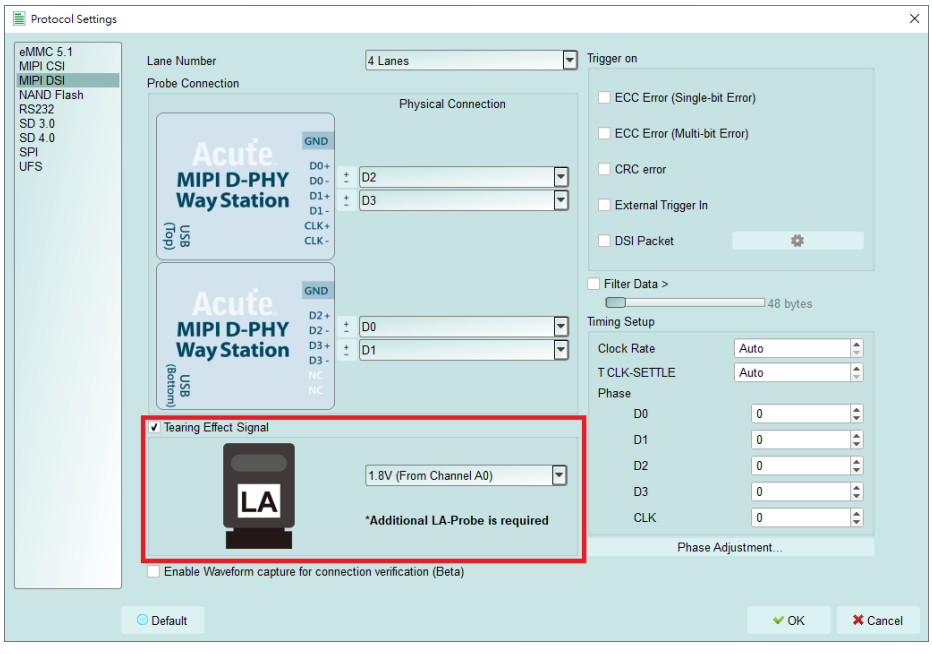
Tearing Effect (TE) pin signal detect.



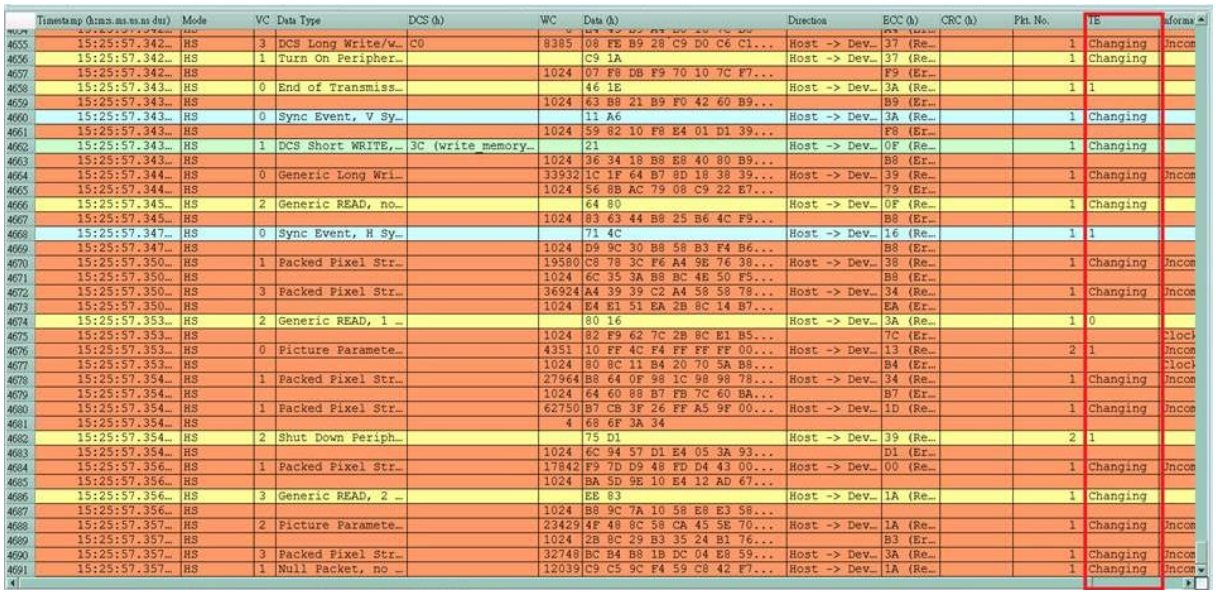
(Image Source: https://blog.csdn.net/kris_fei/article/details/77775553)

The TE pin is used by the display to inform the Host. At present, the data cannot be updated during the screen graphics drawing. If the screen is updated when TE = High, a horizontal break line will appear on the image. This function can clearly identify the failure to follow TE state operation instructions, reduce the time required to guess the problem and set up an oscilloscope to verify

The TE function requires the user to purchase an additional set of LA Probe to support it. The default input is from channel 0, which supports two operating voltage modes of 3.3V and 1.8V. The setting is as follows,



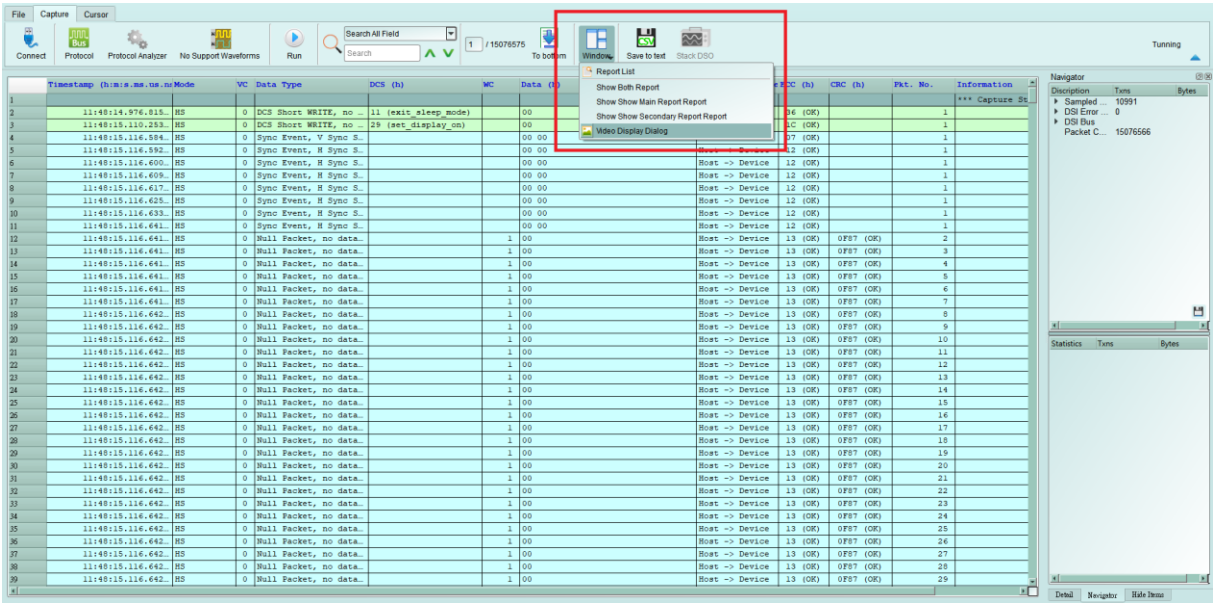
Result:

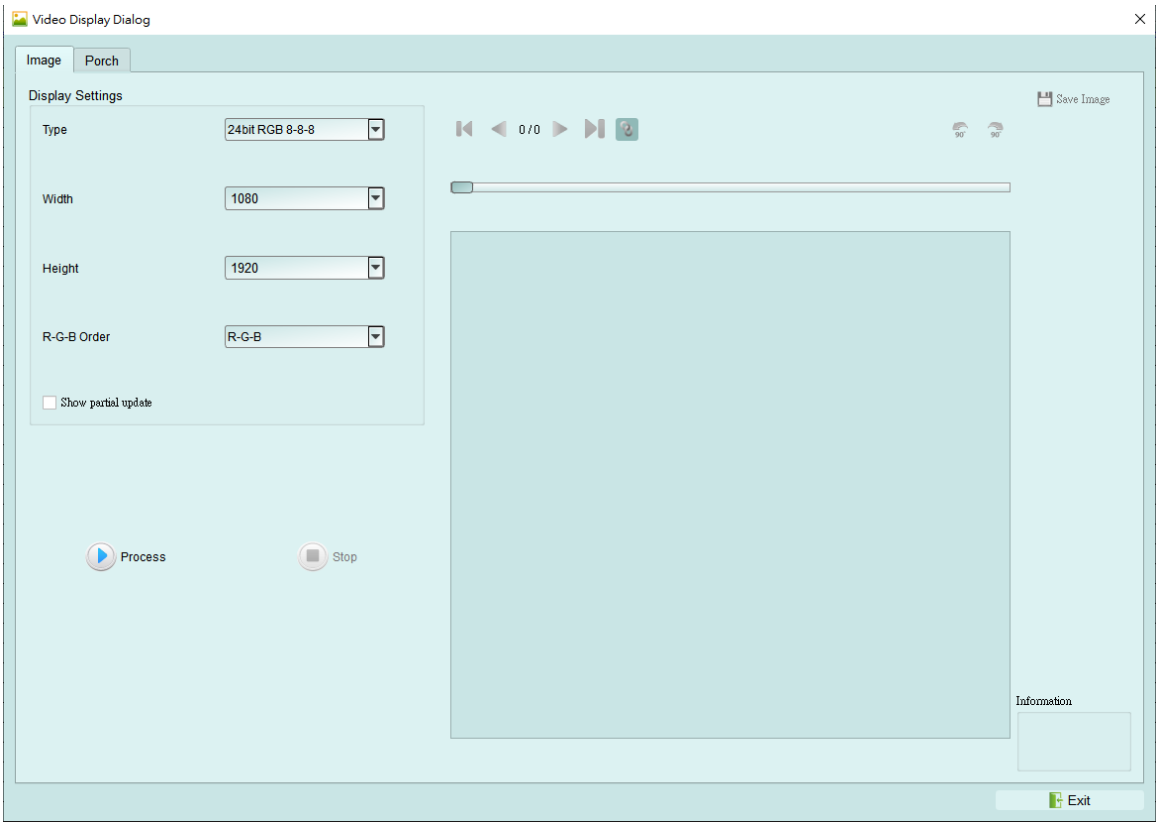


	Timestamp (hrs.ms.us.ns dur)	Mode	VC	Data Type	DCS (h)	WC	Data (h)	Direction	ECC (h)	CRC (h)	Pkt. No.	TE	Informa
4654													
4655	15:25:57.342…	HS	3	DCS Long Write/w…	C0	8385	08 FE B9 28 C9 D0 C6 C1...	Host -> Dev…	37 (Re…		1	Changing	Uncom
4656	15:25:57.342…	HS	1	Turn On Peripher…			C9 1A	Host -> Dev…	37 (Re…		1	Changing	
4657	15:25:57.342…	HS				1024	07 F8 DB F9 70 10 7C F7...		F9 (Er…				
4658	15:25:57.343…	HS	0	End of Transmiss…			46 1E	Host -> Dev…	3A (Re…		1	1	
4659	15:25:57.343…	HS				1024	63 B8 21 B9 F0 42 60 B9...		B9 (Er…				
4660	15:25:57.343…	HS	0	Sync Event, V Sy…			11 A6	Host -> Dev…	3A (Re…		1	Changing	
4661	15:25:57.343…	HS				1024	59 82 10 F8 E4 01 D1 39...		F8 (Er…				
4662	15:25:57.343…	HS	1	DCS Short WRITE,…	3C (write_memory…		21	Host -> Dev…	0F (Re…		1	Changing	
4663	15:25:57.343…	HS				1024	36 34 18 B8 E8 40 80 B9...		B8 (Er…				
4664	15:25:57.344…	HS	0	Generic Long Wri…		33932	1C 1F 64 B7 8D 18 38 39...	Host -> Dev…	39 (Re…		1	Changing	Uncom
4665	15:25:57.344…	HS				1024	56 8B AC 79 08 C9 22 E7...		79 (Er…				
4666	15:25:57.345…	HS	2	Generic READ, no…			64 80	Host -> Dev…	0F (Re…		1	Changing	
4667	15:25:57.345…	HS				1024	83 63 44 B8 25 B6 4C F9...		B8 (Er…				
4668	15:25:57.347…	HS	0	Sync Event, H Sy…			71 4C	Host -> Dev…	16 (Re…		1	1	
4669	15:25:57.347…	HS				1024	D9 9C 30 B8 58 B3 F4 B6...		B8 (Er…				
4670	15:25:57.350…	HS	1	Packed Pixel Str…		19580	C8 78 3C F6 A4 9E 76 38...	Host -> Dev…	38 (Re…		1	Changing	Uncom
4671	15:25:57.350…	HS				1024	6C 35 3A B8 BC 4E 50 F5...		B8 (Er…				
4672	15:25:57.350…	HS	3	Packed Pixel Str…		36924	A4 39 39 C2 A4 58 58 78...	Host -> Dev…	34 (Re…		1	Changing	Uncom
4673	15:25:57.350…	HS				1024	E4 E1 51 EA 2B 8C 14 B7...		EA (Er…				
4674	15:25:57.353…	HS	2	Generic READ, 1 …			80 16	Host -> Dev…	3A (Re…		1	0	
4675	15:25:57.353…	HS				1024	82 F9 62 7C 2B 8C E1 B5...		7C (Er…				Clock
4676	15:25:57.353…	HS	0	Picture Paramete…		4351	10 FF 4C F4 FF FF FF 00...	Host -> Dev…	13 (Re…		2	1	Uncom
4677	15:25:57.353…	HS				1024	80 8C 11 B4 20 70 5A B8...		B4 (Er…				Clock
4678	15:25:57.354…	HS	1	Packed Pixel Str…		27964	B8 64 0F 98 1C 98 98 78...	Host -> Dev…	34 (Re…		1	Changing	Uncom
4679	15:25:57.354…	HS				1024	64 60 88 B7 FB 7C 60 BA...		B7 (Er…				
4680	15:25:57.354…	HS	1	Packed Pixel Str…		62750	B7 CB 3F 26 FF A5 9F 00...	Host -> Dev…	1D (Re…		1	Changing	Uncom
4681	15:25:57.354…	HS				4	68 6F 3A 34						
4682	15:25:57.354…	HS	2	Shut Down Periph…			75 D1	Host -> Dev…	39 (Re…		2	1	
4683	15:25:57.354…	HS				1024	6C 94 57 D1 E4 05 3A 93...		D1 (Er…				
4684	15:25:57.356…	HS	1	Packed Pixel Str…		17842	F9 7D D9 48 FD D4 43 00...	Host -> Dev…	00 (Re…		1	Changing	Uncom
4685	15:25:57.356…	HS				1024	BA 5D 9E 10 E4 12 AD 67...						
4686	15:25:57.356…	HS	3	Generic READ, 2 …			EE 83	Host -> Dev…	1A (Re…		1	Changing	
4687	15:25:57.356…	HS				1024	B8 9C 7A 10 58 E8 E3 58...						
4688	15:25:57.357…	HS	2	Picture Paramete…		23429	4F 48 8C 58 CA 45 5E 70...	Host -> Dev…	1A (Re…		1	Changing	Uncom
4689	15:25:57.357…	HS				1024	2B 8C 29 B3 35 24 B1 76...		B3 (Er…				
4690	15:25:57.357…	HS	3	Packed Pixel Str…		32748	BC B4 B8 1B DC 04 E8 59...	Host -> Dev…	3A (Re…		1	Changing	Uncom
4691	15:25:57.357…	HS	1	Null Packet, no …		12039	C9 C5 9C F4 59 C8 42 F7...	Host -> Dev…	1A (Re…		1	Changing	Uncom

Appendix 2: Video Display Dialog

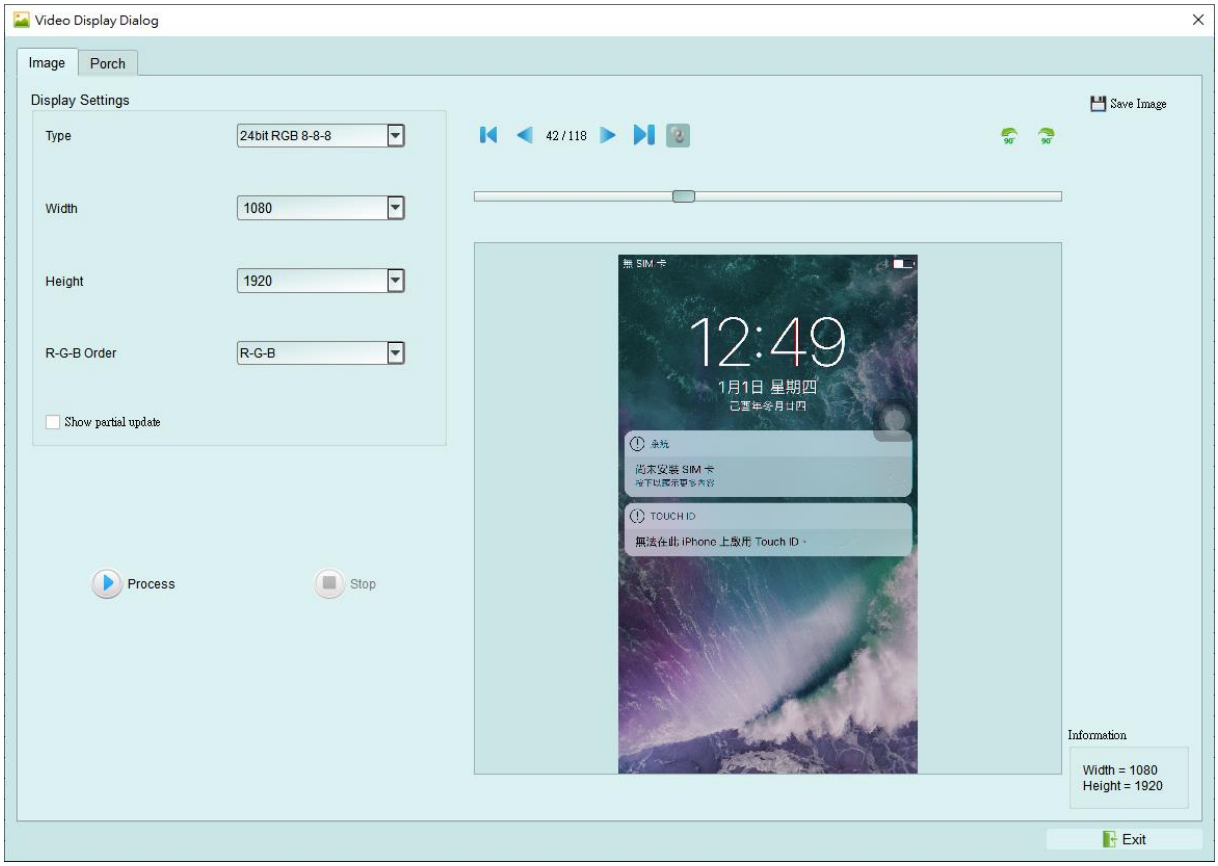
Click Window-> Video Display Dialog to open the video display dialog,





Please set the DSI, CSI format, resolution, RGB order, and then press Process to restore the image. Partial analysis function is also provided. If the DUT only updates part of the screen, this option can be checked to display part of the updated content.

Example:



It also provides a linkage function with the data in the main report area, making it easy to find the location of the image data.

Save Image can output the restored image as .jpg / .bmp / .bin.

If DSI transmits image data in Video mode, there is also a Porch function that can count the format sent by each image. Ex: VSA, VBP, VFP, HBP, HFP, image.

If you choose TYPE-DSC restore, please select DSC Command mode use DCS Command.

If you use V-Sync / H-Sync format, please select DSC Video mode. Specify the PPS file (format .txt) to restore. PPS will also be replaced with the Picture Parameter Set (0A) command.

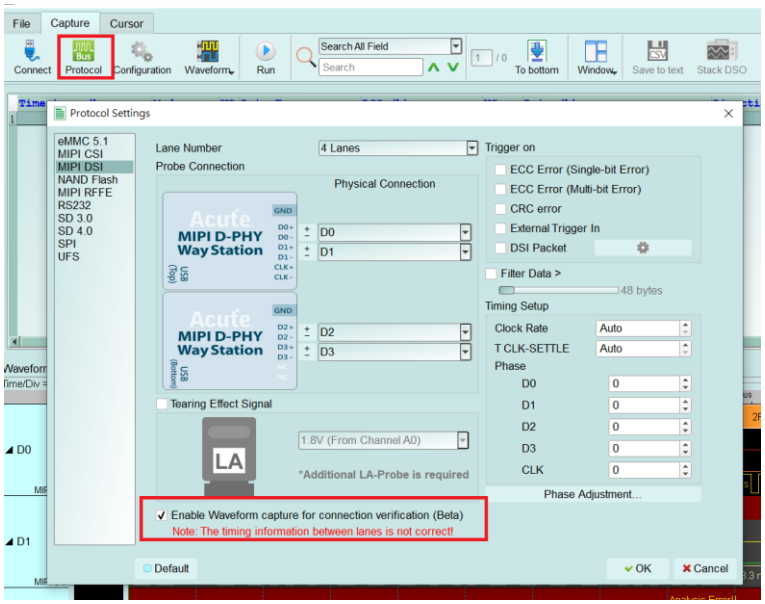
Appendix 3: Unable to Measure / Only Measure the LP Mode Signal / Too Many Errors Solution:

Step 1: Please check whether the 2 USBs between the probe and the BudFinder are not connected well.

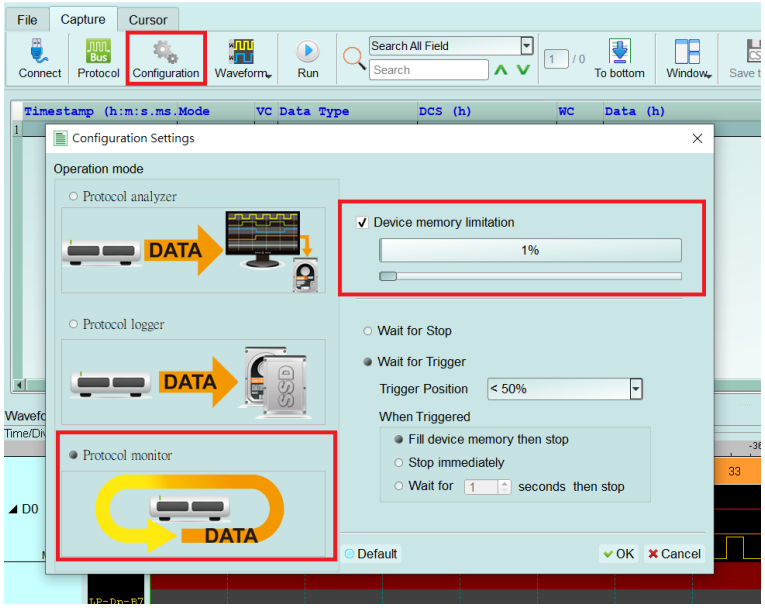
Step 2: Please check if the Lane/CLK wire is within 5mm of the regulation, and make sure that each end-tip is connected to Gnd.

Step 3: Turn on the waveform viewing function and send out the HS signal to make sure the connection is correct.

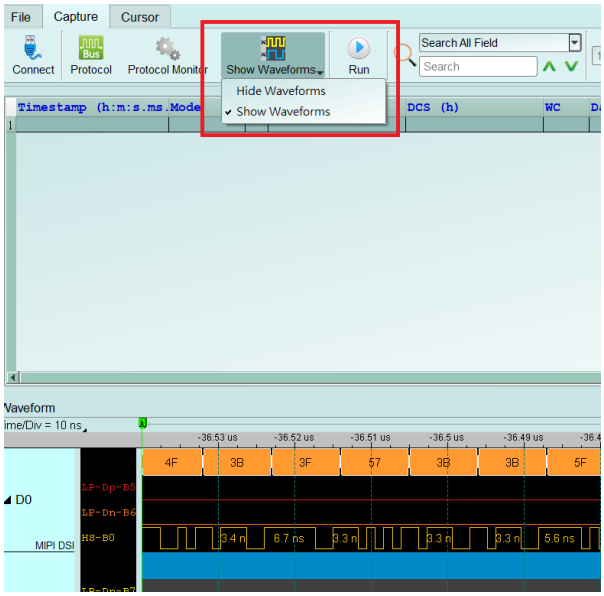
Step 3.1: Enable Waveform capture for connection verification (Beta)



Step 3.2: Switch the “Configuration Settings”. Use the “Protocol Monitor mode” and limit the memory to 1-3%. If the problem is solved, switch back to “Protocol Analyzer mode”

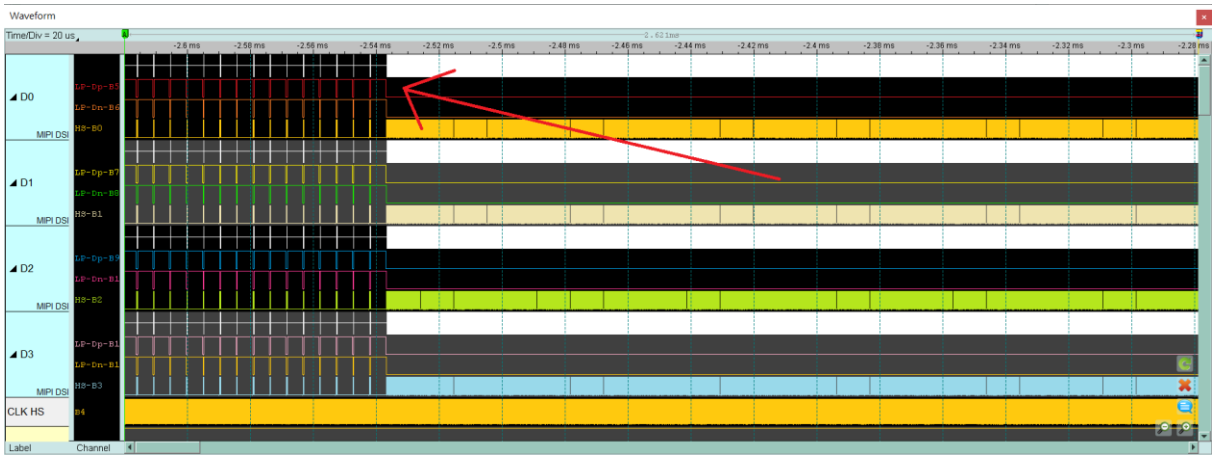


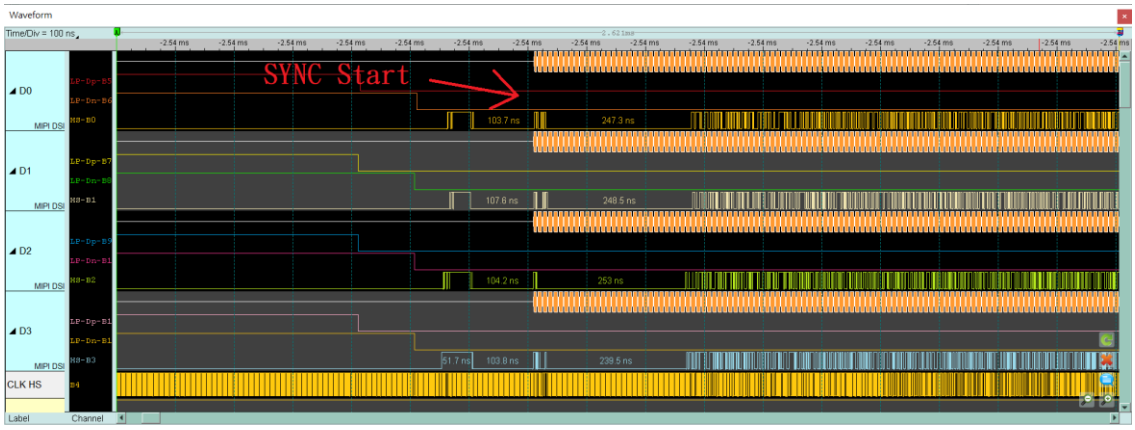
Step 3.3: Show Waveforms



Step 3.4: Capture the waveform

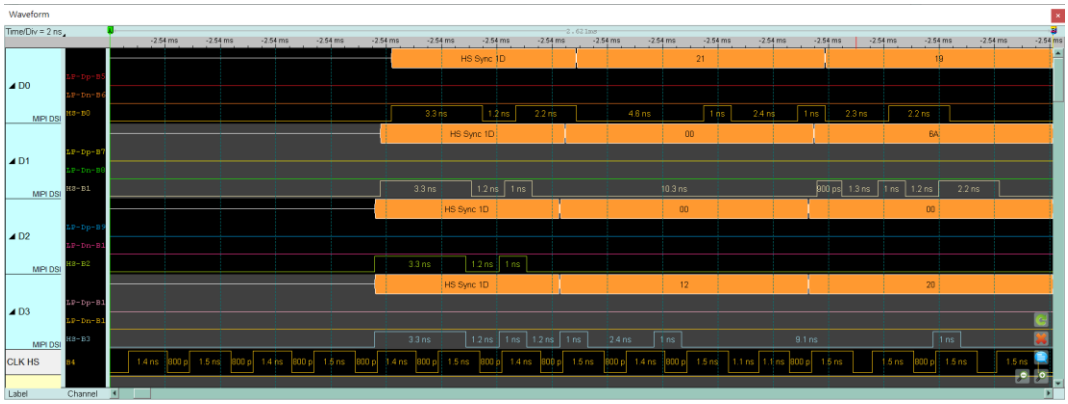
Step 3.5: Analyze whether there is an HS signal. Before the red arrow is the LP signal, and after the waveform is the HS signal. (At the position of the red arrow, the LP signal of P/N becomes low, and HS starts to have signal.) Please find a similar position and zoom in to view the waveform. If the collection is repeated many times, the intersection of LP and HS still cannot be found. The Lane/CLK may be disconnected. Please refer to the FAQ 7.





Step 3.6: Confirm whether the CLK Duty is 50:50, and check the width of each edge of Lane 0-3 behind HS SYNC. Normally, it is the width of half a CLK cycle or multiple. If it is abnormal, please check whether the bonding wire meets the requirements again. If it meets the regulations, there will still be noise or CLK Duty problems, please continue to shorten the wire length, and need to use the GND closest to the signal.

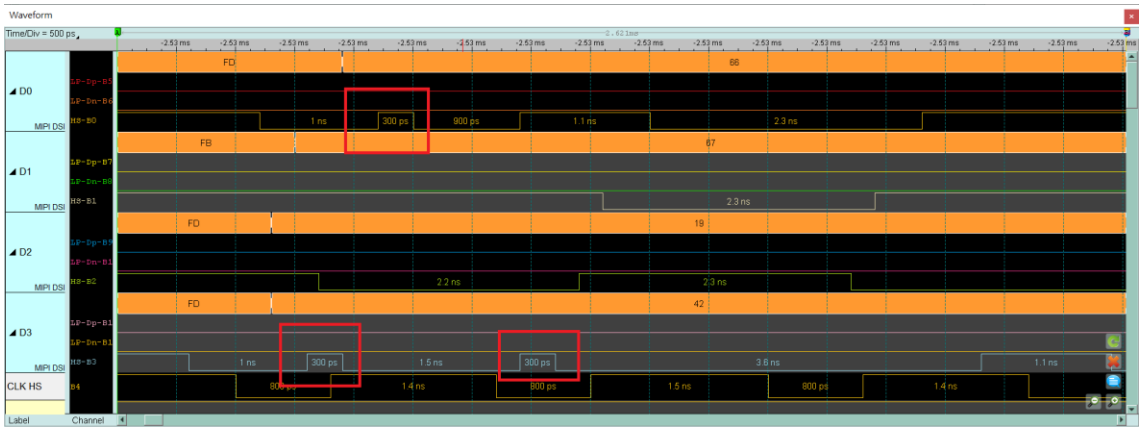
Ex: Bad CLK duty, 65:35, 1.4ns:0.8ns



Ex: The width of high pulse in Lane 0, Lane 3 is not the width of half CLK cycle

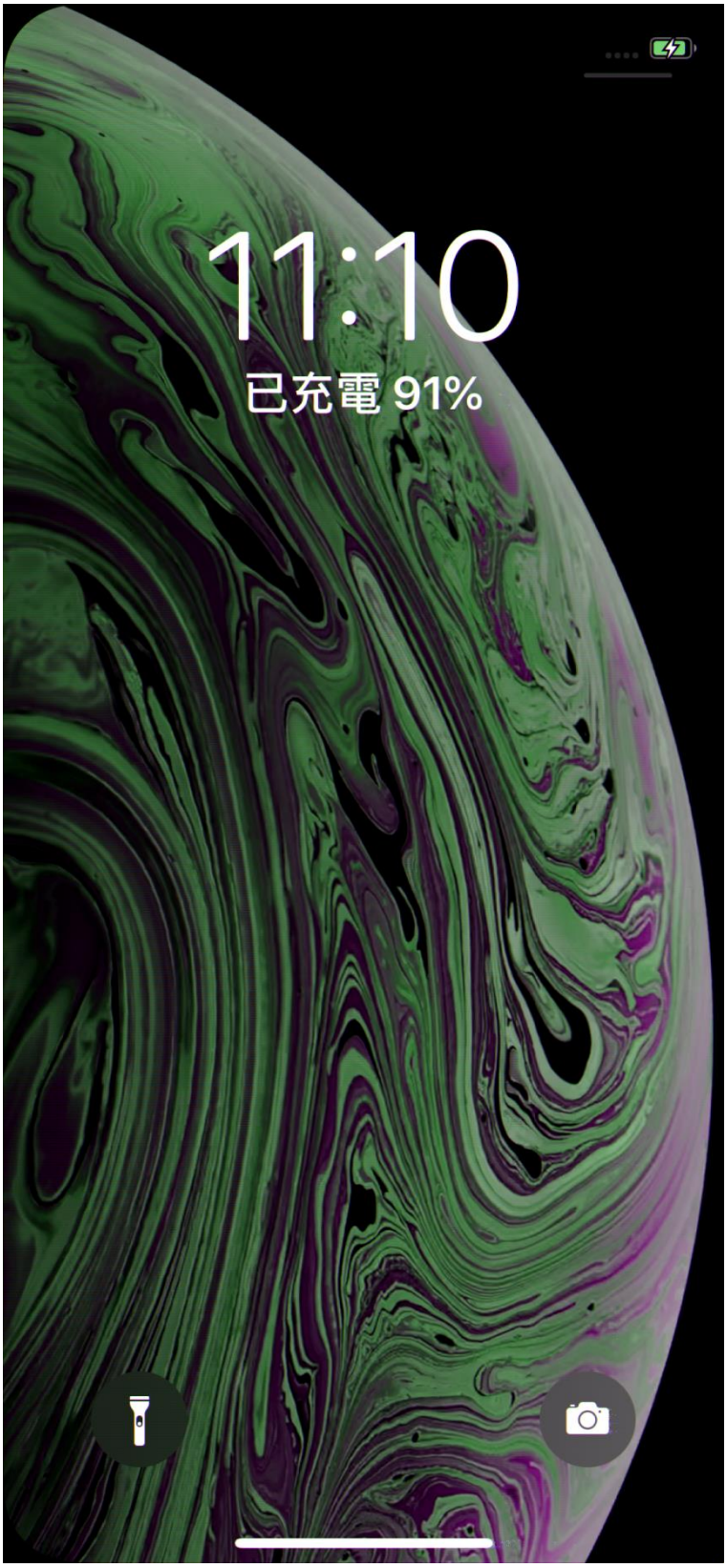
Half CLK cycle = (1.4 + 0.8) / 2 = 1.1 (ns)

Under normal conditions, the width is about 1.1ns or multiple.

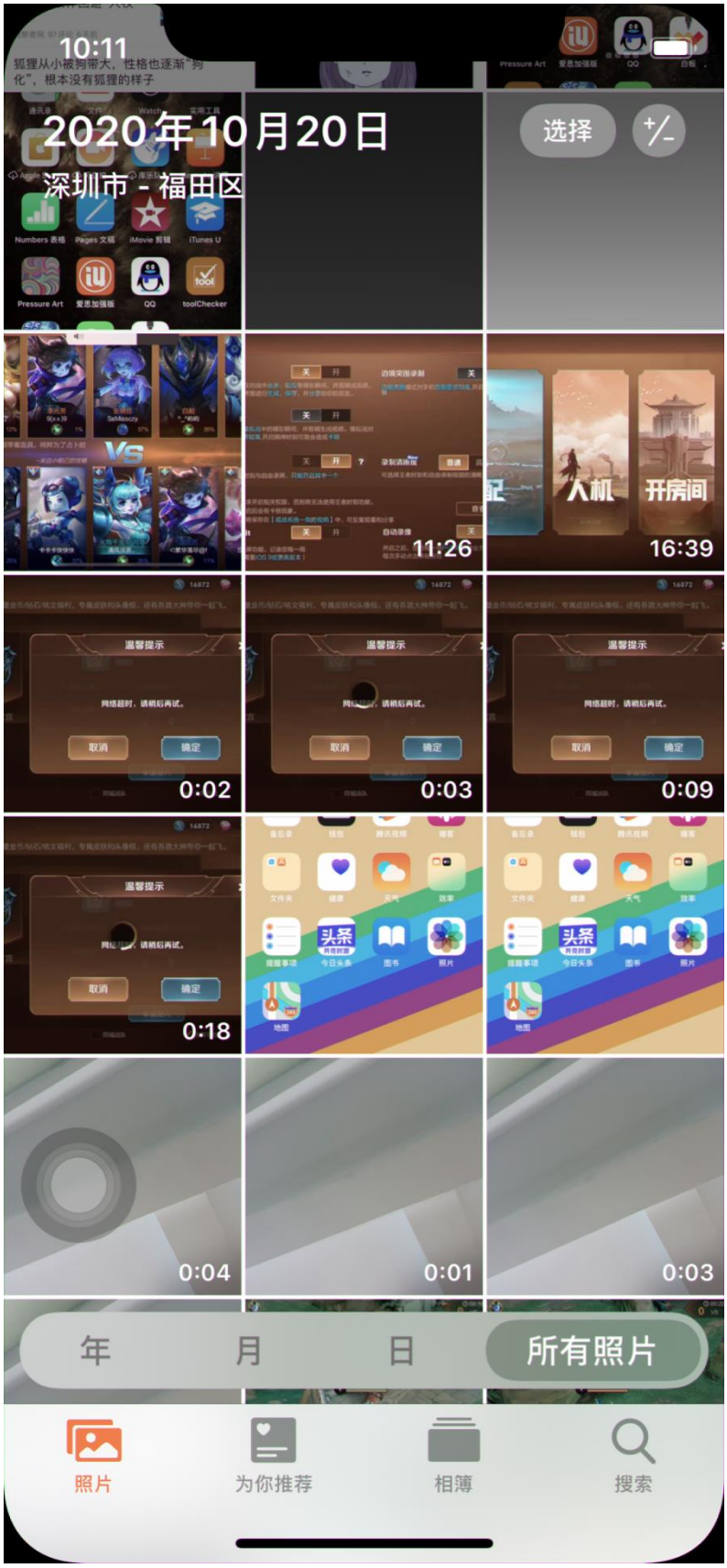


Appendix 4: List of restored images

1. Video mode - 1125 * 2436



2. CMD mode – 1125 * 2436



3. CMD mode – 1170 * 2532